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Characterization and Modeling of 4H-SiC Low Voltage MOSFETs and Power MOSFETs

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By

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Abstract

The integration of low voltage and high voltage circuits on SiC has profound applications. SiC power devices have proved their superiority in terms of high temperature operation, faster switching frequencies and larger power densities when compared with Si power devices. The control of SiC power devices however, lies in the hands of low voltage circuits built on Si. Thus, there exists a separation in the overall system between the low voltage and high voltage side, which increases system cost, weight and reduces efficiency. With the advancement in low voltage SiC processing technology, low voltage control circuits can be made on the same die as power devices, and power systems will become compact, robust and more efficient.

A new low voltage process in 4H-SiC has been characterized and modeled. In order to design circuits with the low voltage process, designers need accurate device models for simulation. Currently, there exist no compact models in the public domain for low voltage SiC MOSFETs. This work aims at filling that void, by providing a modified PSP model for SiC MOSFETs. In addition, a new compact model for SiC power MOSFETs has also been developed and validated with characterization data from a commercially available 1200 V, 20 A power MOSFET. A gate driver chip has been designed and fabricated in 4H-SiC using the developed models. The gate driver chip will drive commercially available power MOSFETs in an integrated AC/DC converter application.

This dissertation is approved for
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Chapter 1

Introduction

1.1 Motivation

The fundamental requirements for all electrical systems is the supply of constant regulated power. Without the availability of good quality power, even the most sophisticated systems cannot function. The power supplied by the utility is in the form of Alternating Current (AC) supplied at a low frequency of 50/60 Hz. With the explosive growth in the popularity of digital integrated electronics, the demand for efficient and compact AC to DC converters has surged. Traditionally, power supplies consisted of linear power systems which consisted of a dissipative resistor with a transformer connected to the main power supply, often operating at 50/60 Hz. The low operating frequency meant most of the energy was stored in the reactive core of the transformer, which had to be extremely large and heavy to meet the power requirements. Moreover, due to higher losses in the core, linear power system efficiency was limited in the range of 30%. The large size and low efficiency of linear power systems were two major drawbacks of the linear power system.

With the rapid development of power semiconductor devices, a new breed of power supplies emerged which were known as Switch-Mode Power Supplies (SMPS) [2]. SMPS are typically used to supply a constant DC voltage output with an AC input, usually from the main power supply as shown in Fig. 1.1. The SMPS chops the AC signal coming in from the main power supply at a high frequency, which is then filtered easily into a regulated DC output. The higher frequency of operation enables a tremendous reduction in the size and weight of the power transformer as well as other filtering components. By switching at 100 kHz instead of 60 Hz, the overall system size

can be reduced by more than a factor of eight. This means that the power supply can be made very efficient as well as compact for any given power density. The development of SMPS represents a remarkable improvement over the traditional linear power systems. SMPS are now employed in almost every power system and are crucial to their operation.

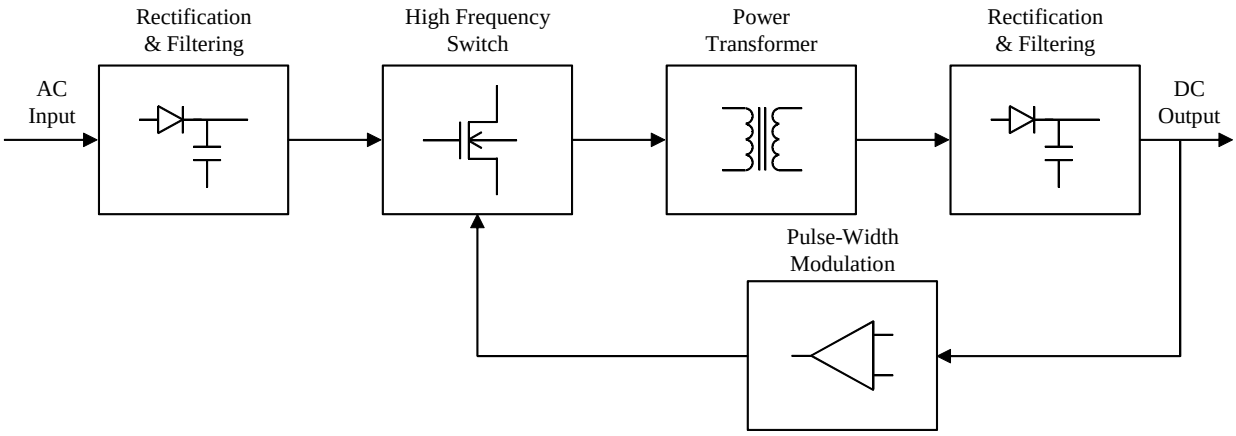


Fig. 1.1: General schematic of a Switch-Mode Power Supply

At the heart of any SMPS is a high frequency inverter consisting mainly of power semiconductor devices like Bipolar Junction Transistors (BJTs), power Metal-Oxide Semiconductor Field Effect Transistors (MOSFETs), Junction Field Effect Transistors (JFETs), Insulated Gate Bipolar Transistors (IGBTs) etc. In addition to the power devices, the inverter also consists of rectifiers, inductors, capacitors and a transformer. The arrangement of all the components determines the topology of the inverter and determines the modes of operation, direction of power flow and other important characteristics of the SMPS. The selection of the type and material of the power semiconductor device inside the inverter plays a pivotal role in the performance of the system.

Power transistors can be broadly classified as bipolar or unipolar devices. Power BJTs have excellent low on-state resistance but are slow at turning off due to their bipolar nature. IGBTs also suffer from the same problem, and have a ‘tail-current” while turning off. This tail-effect is due to

the finite time required for the excess carriers in the base region of bipolar transistors to recombine before the transistor can start blocking again. As a result, BJTs and IGBTs are suitable for low frequency, high voltage blocking applications with low-on state conduction losses. Due to their higher turn-off time, their switching losses overtake the conduction losses and the bipolar devices become unsuitable at higher frequencies due to low efficiency.

On the other hand, unipolar devices like power MOSFETs have excellent switching characteristics as there is no recombination effect in these devices during switching. The switching of a power MOSFET involves only the charging and discharging of the internal capacitances. As a result, power MOSFETs are highly suitable for high frequency applications. However, since there is no conductivity modulation effect in the unipolar devices, their on-state resistance rises sharply with increasing blocking voltage. Thus, vertical silicon power MOSFETs are limited to applications requiring blocking voltages less than 200 V. At higher blocking voltages, the on-state resistance of silicon based unipolar devices becomes prohibitive from a conduction loss point of view and bipolar devices dominate due to their excellent on-state characteristics.

The lower voltage blocking limit of power MOSFETs holds true for silicon, which has been the staple material for fabricating power MOSFETs until recently. The rapid development of wide bandgap materials like silicon carbide is changing the playing field for unipolar devices. SiC power MOSFETs have shown excellent switching and conduction performance in the 1 kV to 10 kV blocking voltage applications, an application space traditionally dominated by Si IGBTs [3]. SiC power MOSFETs also offer very high switching frequencies without sacrificng power efficiency owing to their unipolar nature, something that IGBTs simply cannot offer due to their bipolar nature. SiC power MOSFETs are becoming very attractive for power applications for the following reasons:

- They are voltage-controlled devices, which require simple gate-drivers thus reducing the cost and complexity of gate-drivers.

- Being unipolar in nature, their on-state resistance increases with temperature which makes current sharing very straight-forward. As a result, power MOSFETs can be paralleled easily to meet any current ratings needed for the application.

- Their unipolar nature allows them to switch at very high frequencies with low switching losses. Operating at higher frequencies is very attractive from a system design point of view because the size and weight of the transformers and other passive components show a tremendous reduction with increasing frequency. Higher frequencies result in a much smaller overall system.

Despite the fact that SiC power MOSFETs are able to switch at higher frequencies, the overall system's operational frequency is still limited by the presence of parasitic inductances introduced by the long wires connecting the different discrete components in the system. In a multi-layered printed circuit board (PCB), several techniques are employed to minimize the inductances of the wire traces in order to be able to switch at higher frequencies. In order to capitalize on the ability of the SiC power MOSFETs to switch at high frequencies, there need to be ways to minimize external parasitic inductances. Since the interconnect wires contribute significantly to the system parasitic inductances, a novel approach to minimizing parasitic inductances is to integrate the gate-driver onto a single chip as shown in Fig. 1.2.

Integrated circuits shrink dimensions by orders of magnitude thereby reducing parasitic inductances to a minimum. In order to integrate the gate-control circuitry on the power MOSFET die or near it (e.g. a flip-chip approach with two separate dies), a low voltage process in SiC is required

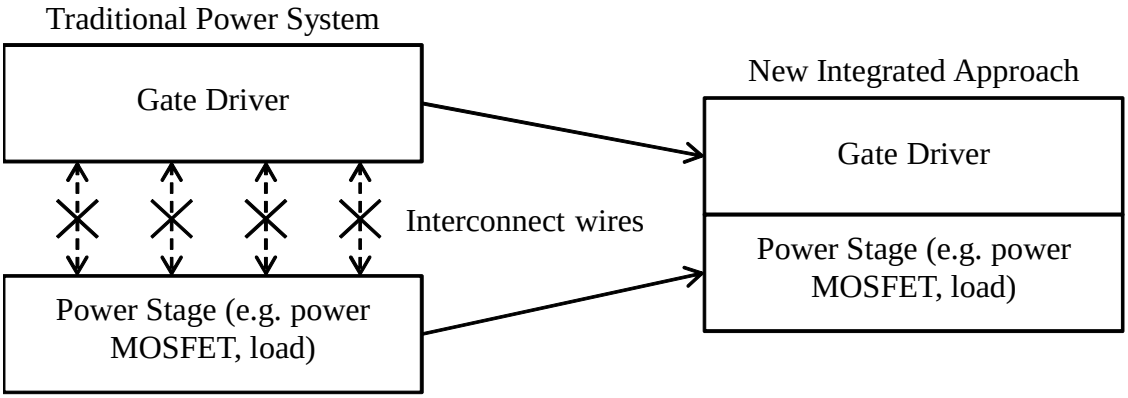


Fig. 1.2: Integration of gate driver with the power MOSFET

to facilitate the development of the gate-driver chip. The low voltage process should be able to support active devices like MOSFETs or JFETs and passive devices like resistors and capacitors, to allow system-level design. Currently, there are no commercial low voltage SiC processes in the market. Thus, there is a strong need to develop such a process in SiC, and characterize it over temperature. In addition, necessary design tools like compact models for the various components in the process must also be developed to enable large-scale integrated circuit design on SiC. With such a process in place, fully integrated power system solutions can be developed which have the power-stage and control stage all on a single die.

Cree Semiconductor Research has developed a new low voltage process in 4H-SiC which can be integrated with their existing 4H-SiC power MOSFET process to build low voltage components on the SiC die. The process supports n-type enhancement and depletion mode MOSFETs as active devices, and resistors and capacitors for passives. Being a new process, it is not well characterized and there exist no compact models to support circuit design for it.

The ultimate objective of this work is to enable the design of a gate driver chip using the low voltage SiC process. The gate driver chip can be integrated with the commercially available SiC

power MOSFET on a single die, minimizing system size and enabling high frequency operation. The gate driver chip will contain digital, analog and mixed-signal integrated circuits using the new SiC process. The objective can be broken down into the following key components:

- Develop a compact model for the commercially available 1200 V, 20 A SiC power MOSFET, which is the key component of the power stage
- Design a test-chip to fully characterize the new low voltage SiC process over temperature
- Using the test-chip, identify the desirable substrate qualities like doping profile, growth type (epilayer vs. implant) to enable all n-MOS circuit design
- Characterize the low voltage n-type enhancement and depletion MOSFETs over temperature
- Develop geometry and temperature scaled compact models for the low voltage SiC MOSFETs
- Validate the compact models by characterization data from devices, and system level simulations

1.2 SiC Power MOSFET Modeling

The key component of the power stage is the 1200 V, 20 A SiC power MOSFET. In order to select the best topology for the application, an accurate compact model of the power MOSFET is needed. With the help of the model, designers can simulate and analyze the performance of their designs for each topology. In addition, the model also provides detailed information about power loss estimates, switching speeds, etc. which help the designers in narrowing down their topology

choices. Designers also have the added advantage of being able to select passive component values and layouts prior to any prototype development of their final topologies. Without the aid of compact device models, designers would need to build prototypes for each topology which is a time-consuming and expensive affair. Thus accurate compact models are an indispensable tool for any development process.

The first part of work presented in the dissertation deals with the development of a compact model for SiC power MOSFETs. The requirements for the power MOSFET model are:

- It should have a good description of the underlying equations that govern device behavior
- It should be accurate and predict the device characteristics well against measured data
- It should converge well in large system level simulations
- It should be able to scale over temperature from 25 °C to 225 °C which is the intended application range
- It should have an efficient and clear way of extracting parameters.

In order for the model to be able to replicate and predict the characteristics of a real 1200 V, 20 A SiC power MOSFET from Cree, the devices are first characterized to extract their electrical characteristics for different test setups. The model's parameters are then extracted using the measured device characteristics. Finally, the model with the new extracted parameters is simulated in different configurations in a virtual test-bench and the results of the simulation are compared with measured results using real devices. This process is called parameter extraction and is vital to the adoption and popularity of any compact model. The power MOSFET model also has built-in

temperature scaling equations which scale its parameters to predict the device characteristics over a wide temperature range.

1.3 SiC Low Voltage MOSFET Modeling

The proposed methodology to reduce system parasitics to a minimum is by integrating the gate-driver circuitry on the power MOSFET wafer or on a separate die which is bonded very close to the power MOSFET. The gate driver will be developed entirely in SiC using depletion and enhancement type n-MOSFETs. In order to characterize the new 4H-SiC low voltage process from Cree, a test-chip has been developed in the first run with several test components on it to characterize the properties of the process. Like in the case of the power MOSFET model, circuit designers require high accuracy device models to enable the design of the gate-driver circuitry. Low voltage MOSFETs are available in several different geometries (different widths and lengths or W/L) which presents a new dimension of geometry scaling in the Low Voltage MOSFET model (LVMOS model) in addition to temperature scaling. Being a new process, there do not exist any models for low voltage SiC MOSFETs. The PSP low voltage MOSFET Model [1, 4] has been chosen as a starting point for developing LVMOS models for SiC MOSFETs as it has shown excellent performance for sub-micron MOSFET technologies down to 20 nm [5] for Si MOSFETs. The PSP model code has been modified to include material specific constants for SiC like band-gap, mobility and carrier concentrations. A big issue in the modification of an existing model is to ensure the continuity of the model across all regions of operations to avoid any convergence issues. The developed model has been shown to scale over geometry as well as temperature (25 °C to 225 °C) and has been used to simulate numerous circuits for the gate-driver chip.

1.4 Dissertation Structure

The dissertation has been organized as follows:

- Chapter 2: Background – The fundamental properties of SiC have been presented with focus on the changes implemented to the Si PSP model. An introduction to the field of compact modeling has also been provided

- Chapter 3: SiC Low Voltage Process – The development of the test chip for characterizing the new low voltage SiC process has been presented. The results of wide temperature characterization of low voltage MOSFET device arrays have also been shown

- Chapter 4: SiC PSP Model – The SiC PSP model has been presented with a brief background and modeling results for the n-MOSFETs in the low volage process

- Chapter 5: Power MOSFET Model – The power MOSFET model along with a new datasheet driven parameter extraction strategy has been described

- Chapter 6: Model Simulation Verification – Results of validation of the models in system-level simulations have been presented

- Chapter 7: Conclusion And Future Work – A summary with key contributions of the work and future work has been presented

Chapter 2

Background

2.1 SiC Material Properties

Silicon carbide has emerged to be one of the most attractive materials for the development of cutting edge power devices which feature very low on-state losses combined with excellent switching performance. Unipolar devices made in SiC like Schottky diodes, Junction Field Effect Transistors and Metal Oxide Semiconductor FETs have demonstrated orders of magnitude improvement in performance from their Si counterparts, thus pushing unipolar devices into the envelope of medium power density, a regime once only possible to their bipolar counterparts. This chapter discusses some of the important properties of SiC that has enabled such drastic improvements in device performance from Si.

Unipolar devices operate on the principle of conduction of majority carriers between two terminals which is controlled by a signal on the third terminal. Being unipolar in nature, the conduction of current is strongly dependent on the fundamental properties of the semiconductor like mobility, intrinsic carrier concentration etc. SiC exists predominantly in 3 poly-types based on its crystal arrangement: 3C, 4H and 6H. Table 2.1 compares the important electrical and thermal properties between different poly-types of SiC and Si. 4H-SiC is preferred over the other poly-types because it has the highest mobility and bandgap among the three.

Note: For the sake of brevity, the term SiC refers to 4H-SiC in this document unless specified otherwise.

Table 2.1: Electrical and thermal properties of Si and polytypes of SiC

	Si	3C-SiC	6H-SiC	4H-SiC
Bandgap (eV)	1.1	2.39	2.86	3.26
Intrinsic Electron Mobility (cm^2/Vs)	1400	1000	600	1070
Critical breakdown Field (MV/cm)	0.3	2	3	3
Thermal Conductivity ($W/K.cm$)	1.5	4.9	4.9	4.9

2.1.1 Band Gap

The biggest difference between SiC and Si is their bandgap which results in different electrical properties. Si has a bandgap of 1.1 eV whereas 4H-SiC has a bandgap of 3.26 eV. A larger bandgap results in a smaller thermal generation of carriers in the depletion region. Since thermally generated carriers constitute the leakage current in the off-state, SiC has considerably less leakage current for a given blocking voltage as compared to Si. The variation of bandgap of 4H-SiC with temperature is given as [6]

$$E_g = 3.26 - 6.5 \times 10^{-4} \frac{T^2}{(T + 1300)} \tag{2.1}$$

The intrinsic carrier concentration is determined by the concentration of thermally generated electron-hole pairs at any given temperature, which is a strong function of the bandgap. For example, the intrinsic carrier concentration of Si increases from $1.01 \times 10^{10}\,cm^{-3}$ at room temperature to $3.90 \times 10^{15}\,cm^{-3}$ at 600K as shown in Fig. 2.1 [7]. The background doping concentration of the lightly doped regions in the device is in the order of $10^{15}\,cm^{-3}$. Thus it can be seen that for Si, the intrinsic carrier concentration overshadows the background doping concentration beyond 600 K, and the region no longer posses the doped properties making the device inoperable. SiC on the other hand has a very low intrinsic carrier concentration, in the order of $10^{-11}\,cm^{-3}$ at room

temperature, and increases to only about $10^{11}\,\mathrm{cm}^{-3}$ at 1000 K. This low carrier concentration at elevated temperatures enables SiC devices to retain their doped region properties over a wide range of temperature.

The intrinsic carrier concentration of SiC as a function of temperature can be modeled as

$$n_i \approx 1.7 \times 10^{16} T^{3/2} e^{-\left(2.08\times 10^4\right)/T} \tag{2.2}$$

Equations (2.1) and (2.2) have been implemented in the SiC PSP model.

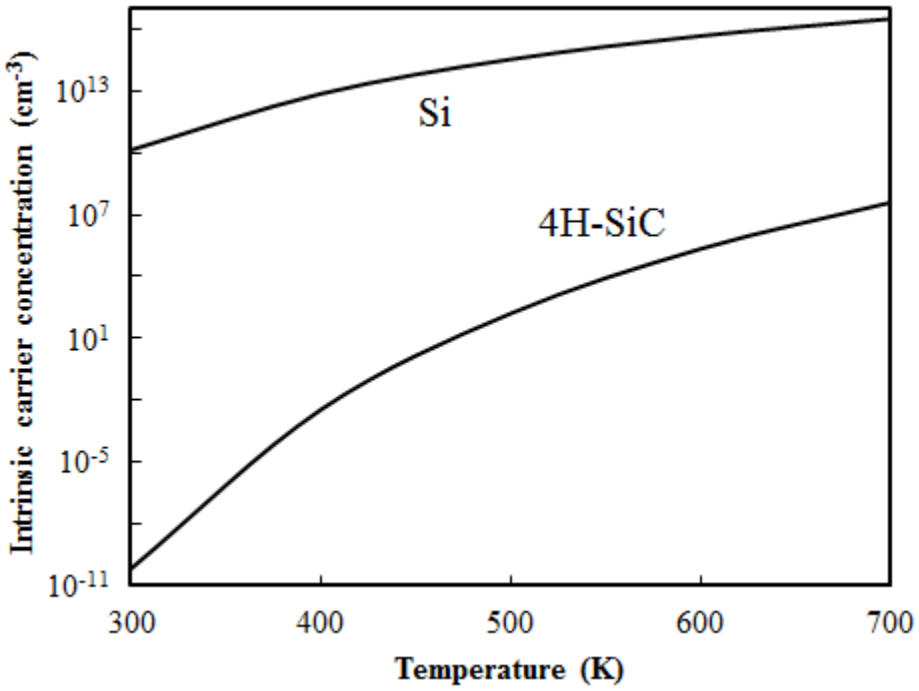


Fig. 2.1: Intrinsic carrier concentration of Si and 4H-SiC over temperature

2.1.2 Critical Breakdown Electric Field

One of the main advantages offered by SiC is a high value of the critical breakdown electric field. The breakdown of a material can be understood by the impact ionization process that takes place

in the presence of an electric field inside the material. A charged particle like an electron, under the influence of an electric field will accelerate in the direction opposite to the applied field. As it accelerates through the material, it will eventually collide with a lattice atom and impart some of its energy to the atom. If the imparted energy is higher than the bandgap of the material, an electron inside the atom absorbs the excess energy and jumps to the conduction band, thus creating an electron-hole pair. This electron-hole pair in turn accelerates in the presence of the external electric field, and in similar fashion have a chance to collide with other lattice atoms. The critical breakdown electric field is defined as the maximum electric field that can be sustained across the material before the generation of electron-hole pairs due to impact ionization becomes a destructive process and results in a sudden large increase in current through the material. The impact ionization process can be described by the Chynoweth Law [8, 9] as

$$\alpha = ae^{-b/E} \tag{2.3}$$

The extracted values of a and b as a function of electric field for Si [10, 11, 12] and SiC [13] are shown in Fig. 2.2. It can be seen that the SiC can support 10 times as much electric field as Si for the same ionization coefficient which directly relates to the critical breakdown voltage.

2.1.3 Bulk Mobility

The resistivity of the drift region is given by

$$\rho_N = \frac{1}{q\mu_N N_D} \tag{2.4}$$

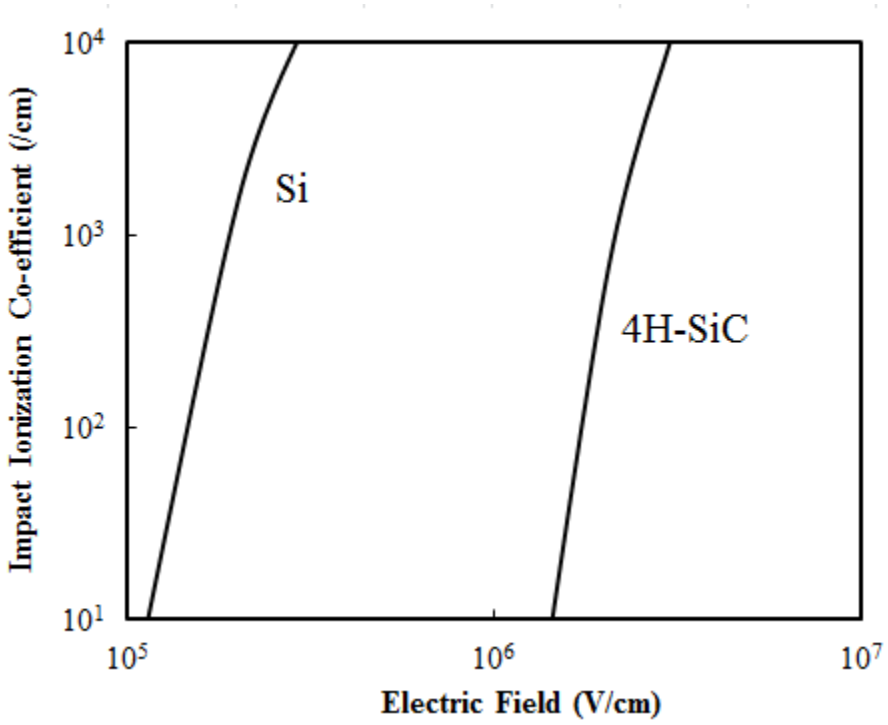


Fig. 2.2: Impact ionization coefficients of Si and 4H-SiC at room temperature

where μ_N is the mobility of electrons in the bulk material and is a function of temperature and doping concentration, N_D. Bulk electron mobility for SiC at room temperature as a function of doping density is modeled as [14]

$$\mu_{N0}(SiC) = \frac{4.05 \times 10^{13} + 20{N_D}^{0.61}}{3.55 \times 10^{10} + {N_D}^{0.61}} \tag{2.5}$$

As can be seen from (2.5), the bulk electron mobility for SiC decreases with increased doping concentration due to increased Coulombic scattering of electrons by the ionized impurities. The variation of bulk mobility with temperature is given as [14]

$$\mu_N(SiC) = \mu_{N0}\left(\frac{T}{300}\right)^{-2.7} \tag{2.6}$$

(2.5) and (2.6) can be combined to yield the mobility variation with temperature and doping density as

$$\mu_N(SiC) = \frac{4.05 \times 10^{13} + 20{N_D}^{0.61}}{3.55 \times 10^{10} + {N_D}^{0.61}} \left(\frac{T}{300}\right)^{-2.7} \tag{2.7}$$

The treatment of surface mobility is very important to the behavior of low voltage SiC MOSFETs, and will be treated in a separate section in Chapter 3.

2.2 SiC Power MOSFET

While the concept of the Field Effect Transistor [15] has been around before the development of the Bipolar Junction Transistor [16], FETs could not be made physically before BJTs due to problems associated with making a good quality interface which is fundamental to their operation. The first power MOSFETs in Si was developed in 1976 after issues related to oxide reliability were resolved by the CMOS community [17]. The proposed power MOSFET was based on the double diffused structure also known as the DDMOSFET structure. It was a P-type Si MOSFET featuring a P-drift region and a P-channel. However, due to the low hole mobility in bulk and the inversion channel in both Si and SiC, power MOSFETs are preferred to be N-type featuring a N-drift region. For example, in SiC the bulk mobility of holes is 125 $\text{cm}^2/\text{V.s}$ while the bulk mobility of electrons is 950 $\text{cm}^2/\text{V.s}$ [18, 19] in the drift region.

The DDMOSFET structure is shown in Fig. 2.3(a). The N^+ source and P^- base region are formed by implanting boron and phosphorus using the self-aligned gate poly-silicon edge as termination. Due to different diffusion rates for the boron and phosphorus in Si (boron having higher diffusivity), their lateral drive-in lengths varies with the drive-in time and temperature. The n-channel in the Si power MOSFET is defined by the lateral extension of the P^- base region under

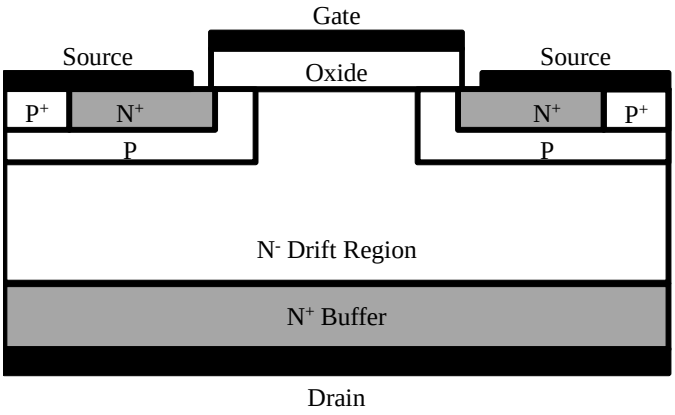
the gate oxide. By accurately controlling the drive-in time, precise sub-micron channel lengths can be obtained without the need for high resolution masks. The elimination of high resolution masks significantly reduces the production cost. The DDMOSFET process proved to be highly succesful in the production of Si power MOSFETs with low costs.

However, due to the low diffusivity of dopants in SiC, a different method is used to fabricate SiC power MOSFETs with the same structure as the DDMOSFET. Instead of using the gate oxide termination edge to define the channel, separate implant edges must be use to define the channel length in a SiC power MOSFET. As a result, for sub-micron channel lengths, high resolution lithography is required which increases the cost of production. This type of process is called the double implant process and the structure is known as DiMOSFET or DMOSFET in short. Despite the differences in the fabrication steps, the final structure for the DDMOSFET and the DiMOSFET look similar (with differences in doping profiles), and the structure shown in Fig. 2.3(a) is valid to study the operation of SiC power MOSFETs. The term DMOSFET in this dissertation refers to the final structure, and it is implied that the DiMOSFET process is used to fabricate SiC power MOSFETs.

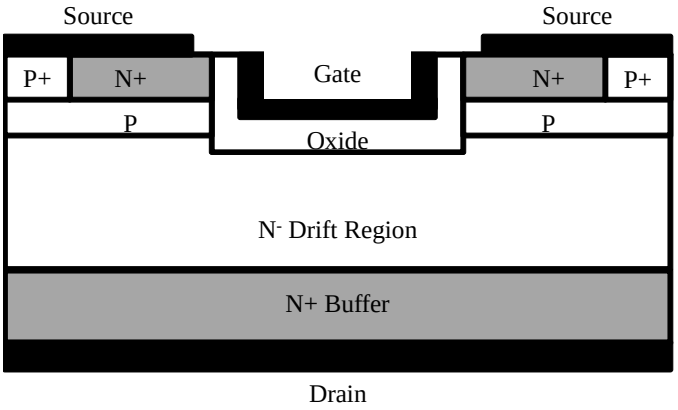
The on-state resistance of the DMOSFET structure is given as

$$R_{ON} = R_{Contacts} + R_{Channel} + R_{JFET} + R_{Drift} \tag{2.8}$$

The various regions contributing to the on-state resistances are shown in Fig. 2.4. Since the major limitation to the performance of the power MOSFET is the on-state resistance, different structures and processing methods have been proposed to reduce the on-state resistance for a given blocking voltage. One such novel approach, borrowed from the DRAM industry in the 90s was



(a) DDMOSFET



(b) UMOSFET

Fig. 2.3: Power MOSFET structures

the UMOSFET structure, shown in Fig. 2.3(b). The UMOSFET structure features a trench-gate with a vertical channel formed in the P-region next to the gate oxide. The UMOSFET structure completely eliminates the JFET region present in the DMOSFET structure, and as a result reduces the effective on-state resistance for the same blocking voltage. In the UMOSFET structure, the sharp trench corners in the gate-oxide become a problem when the devices need to be designed to support higher blocking voltages. The electric field developed in the semiconductor material is also present in the gate oxide, and the relative values for the electric field between the semiconductor

and the oxide is given as

$$\frac{E_{Oxide}}{E_{Semi}} = \frac{\varepsilon_{Semi}}{\varepsilon_{Oxide}} \tag{2.9}$$

where E_{Oxide} is the electric field inside the oxide, E_{Semi} is the electric field inside the semiconductor, ε_{Oxide} is the relative permittivity of the oxide and ε_{Semi} is the relative permittivity of the semiconductor. Thus, (2.9) yields $E_{Oxide} \approx 3E_{Si}$ for Si and $E_{Oxide} \approx 2.5E_{SiC}$ for SiC. The critical breakdown electric field for Si is of the order of 3×10^5 V/cm, which keeps the value of electric field in the oxide to below its critical breakdown value, which is in the order of 3×10^6 V/cm [7]. However, the critical breakdown field for SiC is in the order of 9×10^6 V/cm, which exceeds the critical breakdown limit of the gate-oxide causing reliability issues. Since SiC power MOSFETs are designed to support higher blocking voltages than Si, the UMOSFET structure is not a viable option for SiC MOSFETs without special shielding techniques for the gate oxide [20].

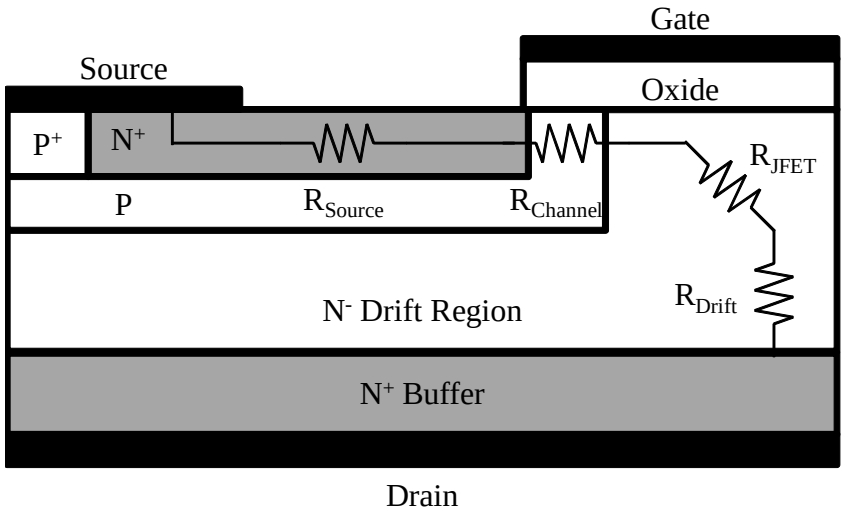


Fig. 2.4: Contributions to the on-state resistance in a DMOSFET structure

The first SiC power MOSFET was demonstrated in 1992 [21] which was based on the UMOSFET structure. It suffered from oxide-breakdown in the trench corners and had low surface in-

version mobility. In order to improve upon the low surface inversion mobility, an accumulation FET (ACCUFET) was proposed in 1997 [22]. The ACCUFET was a vertical 6H-SiC MOSFET structure with a breakdown voltage of 350 V and specific on-state resistance of 18 $\Omega.cm^2$. In order to circumvent the problems of oxide breakdown in the UMOSFET structure, the SiC DMOSFET structure was developed and a SiC DMOSFET with breakdown voltage of 760 V was demonstrated [23]. In 2002, a 2.4 kV 4H-SiC DMOSFET was developed [24] which had a specific on-state resistance of 42 $\Omega.cm^2$. Later in 2002, 3 kV and 5 kV UMOSFETs were demonstrated, which had gate-oxide protection and junction termination extensions [20, 25]. In 2004, a 10 kV power MOSFET was reported in 4H-SiC [26]. Later in 2007, with improvements in SiC manufacturing technology, state-of-the-art 10 kV 4H-SiC DMOSFETs were demonstrated [27] with specific on-state resistance of 111 $\Omega.cm^2$. In 2009, 1200 V, 60A power MOSFETs were demonstrated with on-state specific on-state resistances as low as 9 $\Omega.cm^2$ [28]. 1200 V, 20 A SiC power MOSFETs with current rating of 30 A have also been demonstrated with lower specific on-state resistance of 7.1 $\Omega.cm^2$ [29]. However, due to issues with reliable and repeatable manufacturing of SiC power MOSFETs [30], their commercialization has been very slow. To date, only Cree Inc., offers a set of 1200 V SiC power MOSFETs commercially with different current ratings and on-state resistances [31]. The power MOSFET used for the development of the SiC power MOSFET model in this thesis is the commercially available 1200 V, 20 A SiC power MOSFET from Cree (CMF20120D) [32].

2.3 Development Challenges

While the merits of using SiC over Si in the design of power MOSFETs is great in theory, there are numerous challenges faced by the industry in the commercialization of SiC technology. One of the challenges is the low channel inversion mobility, which arises due to three main reasons: (a) the wide bandgap of SiC results in much higher electric fields at the surface which increase surface scattering, (b) the large density of interface states at the SiC/SiO_2 interface and (c) high degree of surface roughness due to ion implantation and high temperature activation [33, 34].

By definition, inversion occurs in a MOSFET when the bands at the semiconductor/insulator interface bend lower (in case of a P-substrate) by an amount equal to twice the bulk potential (the difference in the energy level of the Fermi level and intrinsic level in the bulk). As a result, due to the wide bandgap in SiC, the bands have to bend a lot more than in Si which implies much larger electric fields at the interface in SiC (due to increased depletion width). It has been shown that surface roughness mobility varies inversly with the square of electric field which leads to lower surface inversion mobility in SiC [35]. The doping density of the P-substrate also affects the surface mobility indirectly by controlling the electric field developed at the surface. As doping is increased, the electric field on the surface increases which adversly affects the surface mobility. Thus, in order to increase the surface mobility, the substrate doping must be reduced.

The requirement of the reduction of substrate doping to improve surface mobility contradicts the requirement of a larger substrate doping for obtaining a reasonable value of the threshold voltage over temperature. The threshold voltage of a MOSFET is given as

$$V_T = V_{FB} + \frac{\sqrt{2q\varepsilon_{SiC}N_A\Phi_s}}{C_0} + \Phi_s \tag{2.10}$$

$$V_{FB} = \Phi_{ms} - \frac{Q_i}{C_0} \tag{2.11}$$

$$C_0 = \frac{\varepsilon_{SiC}}{T_0} \tag{2.12}$$

where Φ_{ms} is the work-function between the metal and semiconductor, Q_i is the trapped charge in the oxide, Φ_s is the surface potential at inversion, N_A is the doping density of the substrate and T_0 is the thickness of the oxide. The threshold voltage of the MOSFET is decreased due to the presence of a large number of trapped positive charges in the oxide (of the order of 10^{12} cm^{-2}, which contribute to the term Q_i in (2.11). As temperature increases, the threshold voltage decreases. In order to ensure reliable operation over high temperature, it is attractive to have a high enough value of threshold voltage so the the drain current stays below 1μA in the off-state even at high temperatures. However, the threshold voltage should not be so large that it places a burden on the gate-driver to switch the device from fully-on to fully-off states at high frequencies. Increasing the doping of the substrate also allows reducing the thickness of the drift region, which reduces the on-state resistance of the power MOSFET. In SiC MOSFETs, it is desirable to reduce the number of positive fixed charges in the oxide so that the doping requirements of the substrate become more relaxed. Striking the balance in the substrate doping to achieve desirable surface mobility and threshold voltage is a challenging task.

Another challenge arises due to the the thinner drift regions in SiC DMOSFETs. In order to reduce the on-state resistances, the drift layer in SiC DMOSFETs is doped 100 times more than in Si, which allows the reduction of drift layer thickness by an factor of 10. The input capacitance of the DMOSFET consists of the overlap capacitance between the gate and the source-metallization C_{GS}, which can be treated as constant for the sake of argument and the capacitance between the gate

and the drain in the form of a series combination of the gate oxide capacitance C_{ox} and the depletion layer capacitance C_{GDj} as shown in Fig. 2.5. The depletion layer capacitance is simply calculated as the parallel plate capacitance between the interface and the edge of the depletion width which varies with the doping density. As the doping density increases, the depletion width reduces which in turn increases the value of the depletion capacitance. Since the depletion capacitance is much smaller than the oxide capacitance when the device is in the blocking state, the effective input capacitance is determined by the value of the depletion capacitance which increases sharply with increasing doping density. This places harsh dv/dt requirements on the DMOSFET as well as the gate driver to switch the device at higher frequencies.

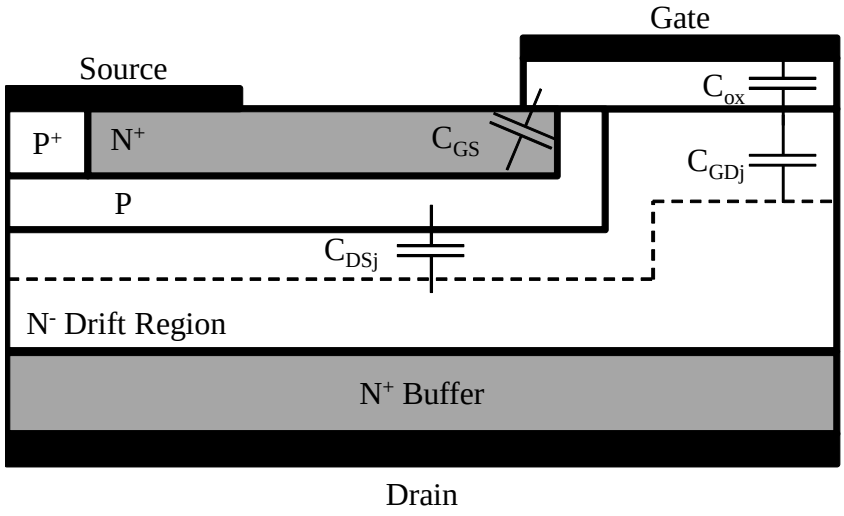


Fig. 2.5: Internal capacitances in the power MOSFET

Finally, the SiC/SiO_2 interface also contains a large density of interface traps [36]. The presence of interface traps has a two-fold effect: (a) when gate voltage is applied, some of the electrons are trapped in the interface states which reduces the electrons available for conduction and (b) the trapped electrons act as scattering centers which increasing Coulumbic scattering effects on the surface. Several improvements for the oxidation of the SiC interface have been proposed which

include Metal Enhanced Oxidation (MEO) and annealing in the presence of NO [37] which aim at reducing the density of interface states at the SiC/SiO_2 interface. Capped activation of anneals with graphitized resists have shown improvement in the roughness of the interface, which would help in improving the overall surface inversion mobility [34]. Further improvements in the processing of the interface would help in the commercialization of a larger array of SiC power MOSFETs.

2.4 Device Modeling

SiC power MOSFETs have seen rapid development in the last decade. While structurally similar to the Si power MOSFET, there are numerous differences in the material properties, device dimensions and the behavior of the internal regions of the device that warrant the development of models specifically for SiC power MOSFETs. Device models can be broadly classified as

- Numerical models
- Compact models
- Table look-up models

2.4.1 Numerical Models

Numerical device models solve the fundamental drift-diffusion equations and current continuity equations in the various regions of the device to yield information about the device characteristics. The inputs to numerical models are device structure, mesh definition, doping profiles, material parameters and other processing information relevant to the device itself. There are several commercial device simulators available like TCAD Sentaurus and Medici from Synopsys [38] and Atlas from Silvaco [39] that provide various tools for each step in building a numerical model of

the device. For example, the TCAD Sentaurus Tool has various tools built in like Sentaurus Process to emulate processing steps, Sentaurus Mesh to create and refine meshes on any structure, Sentaurus Structure Editor that lets the user edit and create device structures using a GUI and Sentaurus Device that simulates the device structures built in the other tools.

There are numerous advantages of using numerical models. Firstly, once calibrated to a certain process, numerical models can reasonably predict device characteristics of structures that have not been characterized or are entirely different devices, as long as all the underlying physical phenomena have been captured and provided to the device simulator. For example, once the mobility of the material being simulated has been properly characterized under various conditions, the device simulator will be able to predict the current through the material of arbitrary geometry under the presence of an electric field. However, unobserved phenomena will not be captured by the numerical simulator and as a result, the quality of material characterization and device simulator equations heavily determines the outcome of numerical models. Since device simulators solve 2 dimensional differential equations at a large number of mesh points, the simulations are often very time consuming. The large number of mesh points also places the burden of properly defining the mesh density in the regions of interest in the device to ensure proper convergence, reasonable simulation time and high resolution of data in the regions of interest. While numerical models are extremely useful in understanding a process and designing and optimizing devices in it, they are computationally intensive. As a result, they are rarely used in circuit simulators to design circuits.

2.4.2 Compact Models

While designing circuits, the circuit designers are not interested in obtaining information about the concentration of electrons and holes in the various regions of the device, nor are they interested

in the built-in electric fields and potential distribution inside the device. They are more interested in accurate prediction of device performance, proper convergence across various bias conditions and quick simulation times of their circuits. Compact models bridge the gap between the requirements of the circuit designer and the plethora of information provided by numerical models. Compact models are generally built for specific device families and are valid for a range of device sizes. Compact models are generally built in different Hardware Description Languages (HDL) like Verilog-A, VHDL and MAST. Different simulators support different HDLs. For example, the HSPICE simulator from Synopsys and the Spectre simulator from Cadence support Verilog-A, while MAST is a proprietary language supported by the Saber simulator from Synopsys. Verilog-A is generally supported by a large number of simulators, and as a result, the compact models developed in this dissertation have been developed in Verilog-A. There are various compact models available in the public domain for different devices like:

- **MOSFET** – BSIM1-BSIM4 from University of California, Berkeley [40], PSP and MOS Model 11 from NXP Semiconductor [1], HiSIM from Hiroshima University [41] and SPICE Level 1-17 from different vendors
- **BJT** – Mextram from NXP Semiconductor [42], VBIC [43] and Gummel Poon [44]
- **Power MOSFET** – UA model [45], Saber model, McNutt model [46]
- **IGBT** – Hefner's IGBT model [47]

In a compact model, the device structure is broken down into various nodes, some of which are external and others are internal. The external nodes are available to the circuit simulator where the various biases are applied to the device. For example, a MOSFET has gate, drain, source and

substrate nodes as external nodes. The internal nodes are defined in order to divide the device structure into different regions based on the physics of operation.

After the structure of the model is defined, equations are formulated for each branch of the device based on actual device physics. The detail in the description of the equations determines the complexity and number of factors accounted by the model. The equations inside a compact model have several model parameters in them, that allow the tailoring of the model to different device characteristics. For example, a simple resistor model has a parameter R, that determines the resistance of the resistor. More advanced models may also contain other parameters like the temperature co-efficient, stress inside the resistor etc. Compact models are often identified by levels. A level 1 model is a very simplified model of a device, and is useful to assist in rough calculations of a circuit. The advantages of a level 1 model are that they are very easy to tailor to a particular device (albeit the fitting of the model to the device may not be very accurate), are fast to simulate and thus are ideal to be used in logic circuits and in general provide a very quick estimate on the performance of a device in a circuit. However, in order to design detailed circuits, more complex models are used which account for several second order effects in the device. A good compact model generally possesses the following qualities:

- **Level of detail** – Since every compact model is designed for an intended application space, the needs of the application space should be sufficiently met by the compact model. For example, compact models for digital applications need to be very fast and may skim on the degree of effects modeled as long as some basic criteria of device characteristics are met. This is because the number of devices used in digital circuits is very large, and models need to be simple enough to simulate in reasonable time. On the other hand, analog applications require a lot more detail

about the device characteristics, and compact models for analog design have to be more thorough, but can be a bit slower as the number of devices in analog circuits is smaller. Another example is the contrast between power device models and IC design models. Since power devices are generally of a given rating and do not vary by geometry, a power device model does not need any device scaling equations. On the other hand, in IC design, devices with different W/L ratios are used, and their models are geometry scaled, where changing the W and L inside the model appropriately affects the outcome of the simulation. Hence, the most important thing when developing a compact model is to properly identify the application space and tailor the model according to it.

- **Parameter Extraction** – While often overlooked in a number of models, the parameters governing the model behavior play a very important role in the adoption of the model. Compact models generally have a parameter extraction procedure to extract parameters for a given process or device. The parameter extraction procedure relies on the availability of a set of measured data from the devices, an optimizer to optimize the parameters to the data and a flow of parameter extraction, where parameters extracted in each step are used for subsequent steps. The problem of parameter extraction is compounded by the fact that modern compact models for state-of-the-art sub-micron processes have over 200 parameters, and the formulation of an extraction strategy is a daunting task. Since several parameter sets can result in very similar device characteristics, the parameter extraction strategy must be able to separate the various parameters during the extraction process and provide reasonable value ranges for the extracted parameters as a sanity check during the extraction process. Parameter extraction determines the degree of adoption of any model by the user community, as a complex and highly accurate model is of no

use to a designer if parameters for it are not readily available.

- **Convergence** – Convergence of compact models is often the bug that bites any compact model developer the hardest. Compact models comprise of several non-linear equations which are all tied together by the various nodes. Different simulators solve the various equations in different ways, but the underlying principles remain the same. SPICE was the first simulator developed for the IC industry [48] at University of California Berkeley. The algorithms defined by SPICE are the general widespread algorithms used in circuit simulators today. In order for the simulator to arrive at a correct solution (with proper tolerances), the equations inside the compact models must properly flatten in the simulator and discontinuities in the formulation of various branches must be avoided. This poses a challenge while developing the model equations for any device. For example, in order to connect the sub-threshold and fully-on regimes of a MOSFET, the channel equations must transition from one regime to the other without any discontinuities. Given the number of regimes possible in a modern sub-micron device, fixing convergence issues in a compact model is quite a challenge, and must be thoroughly tested before a model is released.

2.4.3 Table Look-Up Models

Table look-up models, as the name suggests are entirely based on characterization data from the device. A table look-up model is formed by creating a large database of measured device data, and the model then interpolates all the data to yield device characteristics in between. If sufficient device data is available, table look-up models are an excellent place to start simulating the device quickly and accurately. Some of the advantages offered by table look-up models are that they are

quick and easy to implement, and since they are based on the device data, they are as accurate as the device data. A major limitation of a table look-up model is that since it is based completely on the device data, it cannot predict outside of the available data range. Thus all the regimes of operation of a device must be characterized thoroughly before implementing them in a table look-up model. Another limitation is that if sufficient device data is not available, table look-up models cannot be used since they need explicit values to be able to interpolate all the regimes of operation.

Chapter 3

SiC Low Voltage Process

In order to enable the design of the integrated gate-driver chip on a SiC substrate, Cree has offered the use of their 2μm process. The process is used for their power devices with a few modifications. It features all n-MOS enhancement and depletion type planar-MOSFETs with a target breakdown voltage of 20 V. Being an all n-MOS process, it offers interesting challenges to the circuit designers to take existing CMOS topologies and convert them into all n-MOS architecture while keeping the efficiencies as normally expected.

This process is one of the first of its kind from Cree, developed specifically for the purpose of developing an integrated gate-driver with their commercially available power MOSFETs. Since the process is new with these extensions, it needs to be characterized in order to gain more understanding about the various components fabricated with the process, including LV MOSFETs, resistors and capacitors. In order to do that, a 7 mm $\times$ 7 mm test chip was designed and fabricated with several components that would yield valuable data for the development of a compact model for LV SiC MOSFETs. The following sections will describe the design process of the test-chip with emphasis on the LV MOSFETs.

3.1 Test Chip Design

The purpose of the test-chip was to allow the discrete characterization of different types of components in the process. This included characterization of enhancement and depletion MOSFETs with different W/Ls, metal and poly-resistors of different area and capacitors with different area

and configuration. In addition to characterization of the components, design rules were also verified for consistency. For example, the minimum separation between two metal layers is defined as 5μm. In order to verify this rule, several parallel wires were laid out at a separation of 5μm, which were isolated from each other. A measure of resistance between any two wires in the structure yielded whether the 5μm separation can be uniformly obtained throughout without any of the metal traces shorting to each other. A complete layout of the test-chip is shown in Fig. 3.1. In order to characterize the various components, the test-chip includes the following blocks:

- Device Array
- Large Devices
- Resistors
- Capacitors
- Isolation Structures

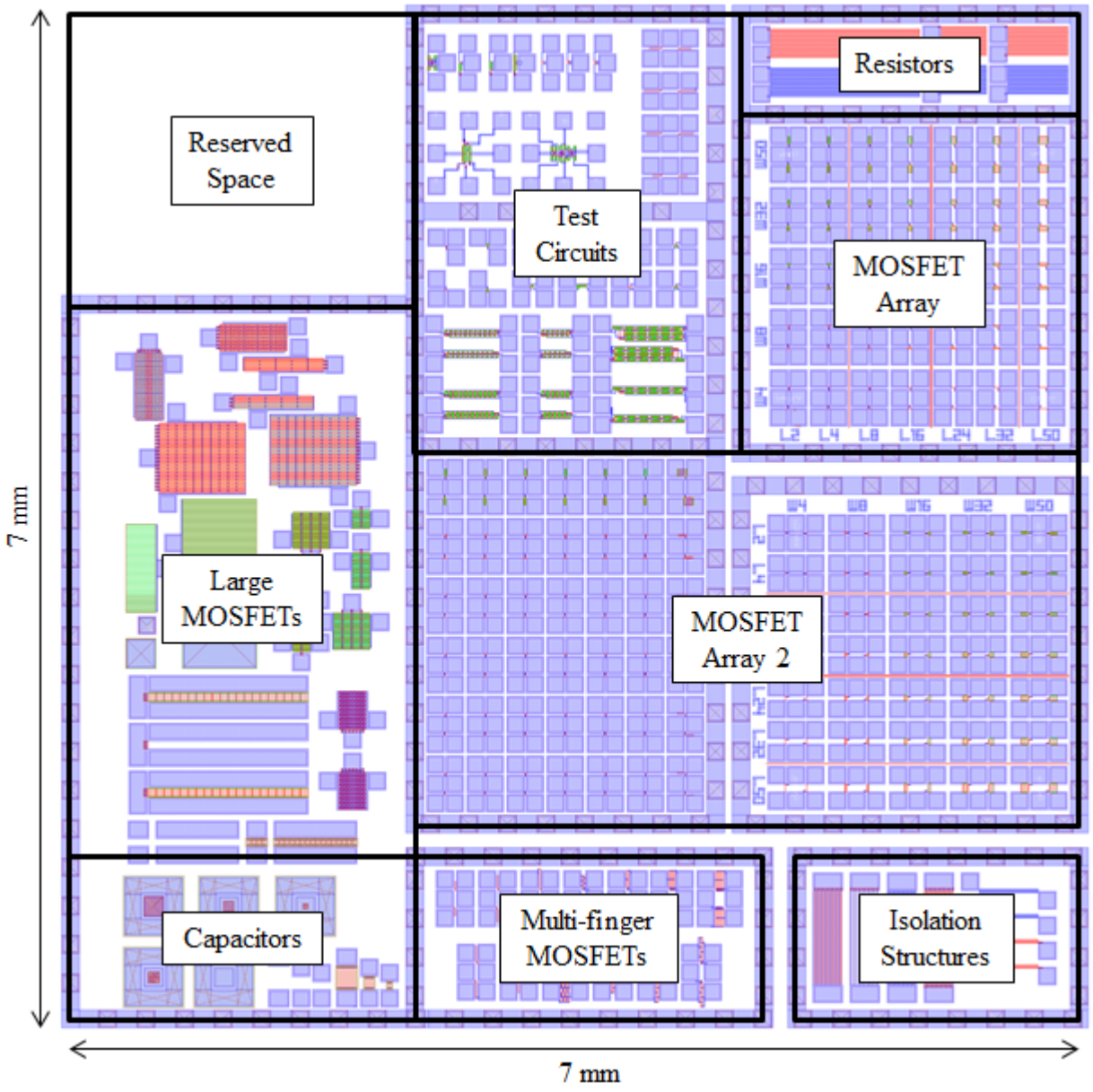


Fig. 3.1: Complete test-chip layout

3.1.1 Device Array

The device arrays comprised of depletion and enhancement type MOSFETs of several W/Ls as shown in Fig. 3.2. The smallest device used was 8 μm x 2 μm and the largest device was 32 μm x 8 μm. All the devices have been laid out in a XY mirrored orientation to save space in the layout as shown in Fig. 3.3. The drain, source and gates have been connected to 120 μm$\times$120 μm pads with pad-openings of 100 μm$\times$100 μm to allow manual probing for characterization.

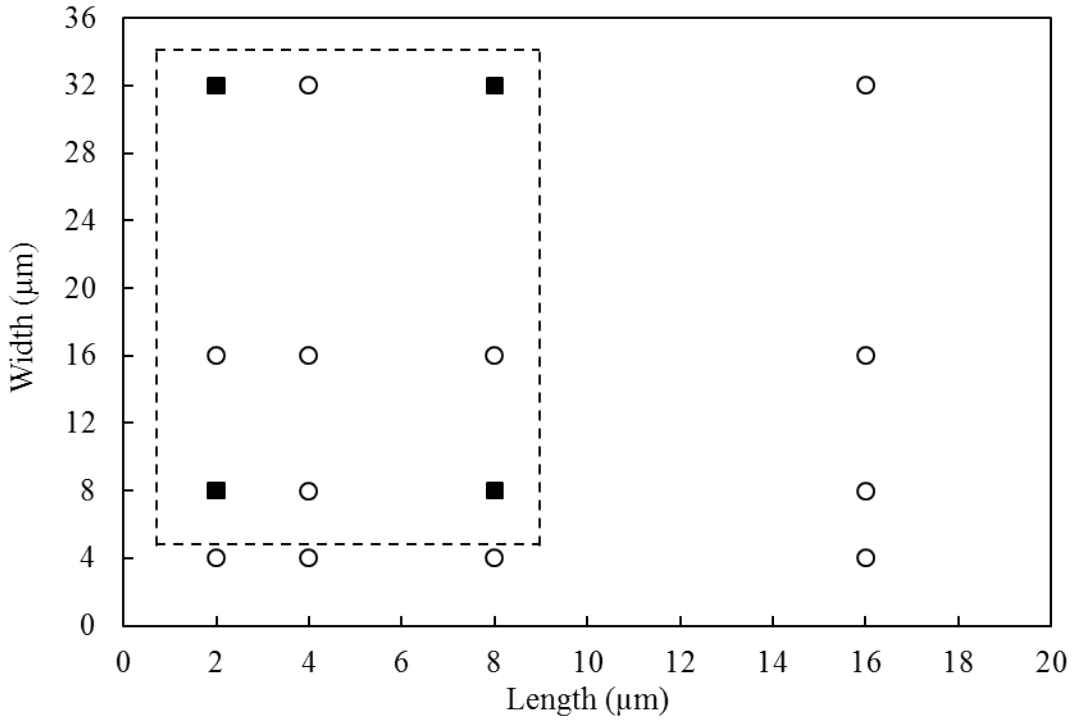


Fig. 3.2: Device sizes in the device array

3.1.2 Large Devices

The gate oxide thickness in the process was specified as 40 nm. A rough estimation of the gate-oxide parallel plate capacitance for the largest device (50 μm$\times$50 μm) was be estimated to be $\approx$ 2.2

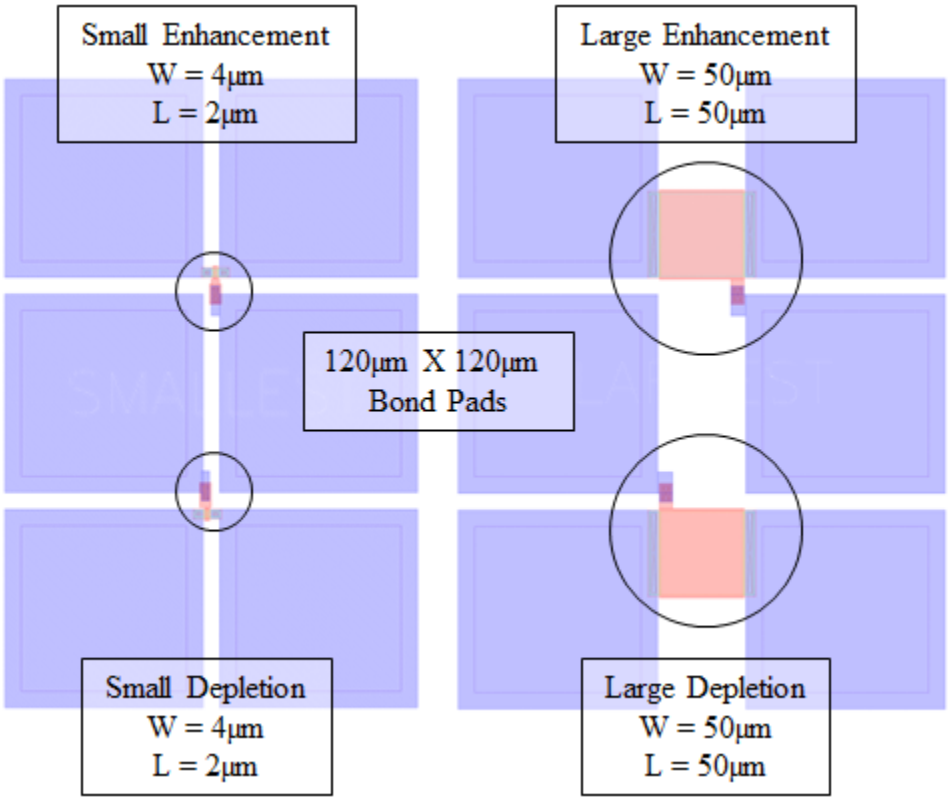


Fig. 3.3: Layout of the smallest and largest device

pF. Typical parasitic capacitances of oscilloscope probes is estimated to be around 90 pF/m [49]. As a result, it is very difficult to physically measure the small capacitances of individual devices on the test-chip.

In order to be able to reliably measure CV characteristics of the low voltage MOSFETs, several devices were laid out in parallel to form a large gate-area transistor. The large device capacitance structure on the test-chip featured 20 large (50 μm$\times$50 μm) transistors in parallel as shown in Fig. 3.4. The estimated capacitance for the large device capacitance structure was $\approx$ 43.1 pF, which could be measured by CV equipment. In order to account for the parasitic inductances of the bond-pads, cables and probes, modern CV instruments use the open test method to de-embed the parasitic capacitances and extract the internal device CV characteristics [50]. An open-test

structure which comprises of just the large device capacitor pads was also been included on the test-chip. Thus, the large device capacitance structure enabled reliable CV characterization of depletion and enhancement devices in the process.

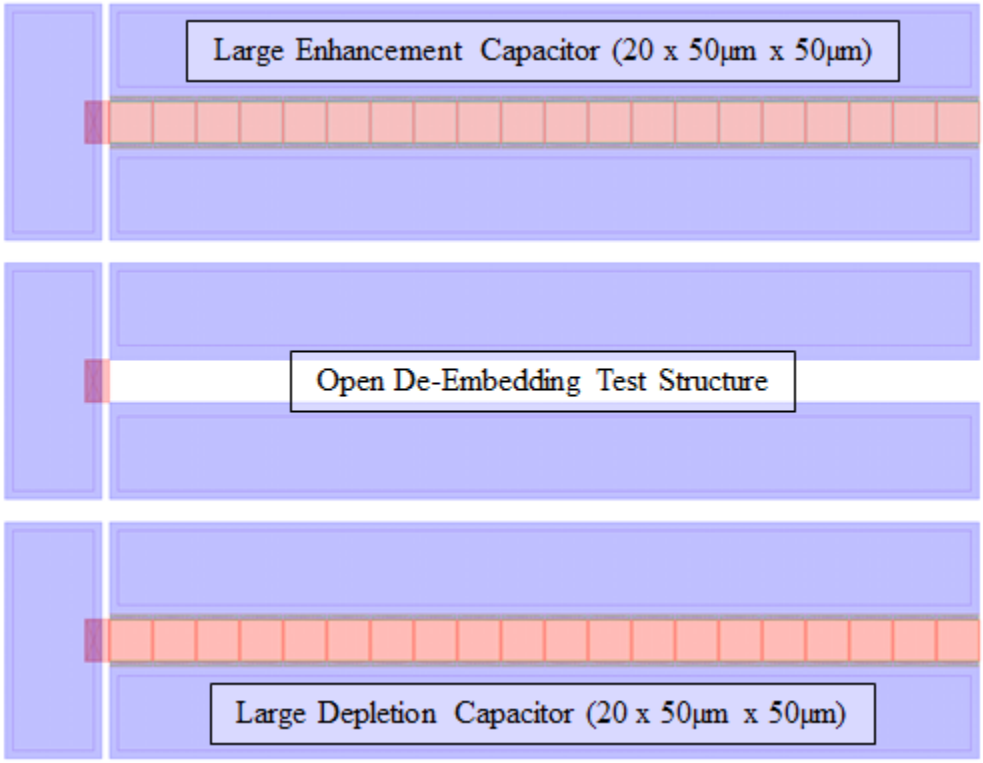


Fig. 3.4: Large device capacitance structure with open de-embedding

3.1.3 Capacitors

In addition to the device capacitor, passive capacitors were also be formed in the LV process between the different layers. A parallel plate capacitor was be formed between (a) metal layer and substrate, and (b) metal layer and poly layer. The capacitance between the poly layer and the substrate is the device gate capacitance and was characterized by the large device capacitance structure.

The test structure to characterize the capacitance between metal and substrate was simply a

parallel metal plate which was probed on top, with a large pad connected to the substrate as shown in Fig. 3.5. Different metal plate sizes were laid out to characterize the area scaling of the metal-substrate capacitor.

Two different configurations for characterizing the capacitance between metal and poly are possible as shown in Fig. 3.6.

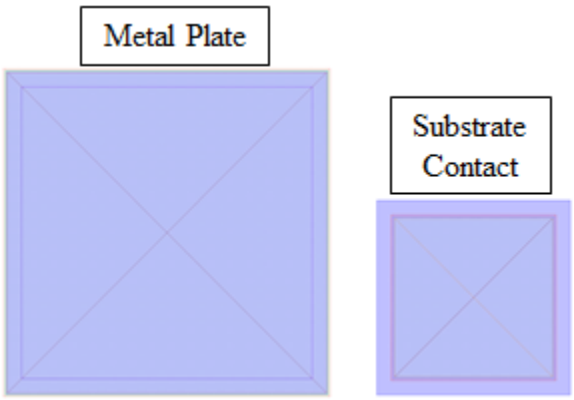


Fig. 3.5: Metal-substrate capacitor test structure

3.1.4 Resistors

The LV process supports 1 metal layer and the poly layer for interconnects. This poses a serious challenge for routing signals throughout the circuits, and increases the overall layout area of the chip. In order to characterize the resistance of the metal and poly traces, long resistors were laid out in a winding fashion to save space as shown in Fig. 3.7. Three different lengths of resistors were laid out in order to confirm the linear scaling of the resistance with trace length. Minimum line width (5 μm) was used for the wound-resistors to yield maximum resistance.

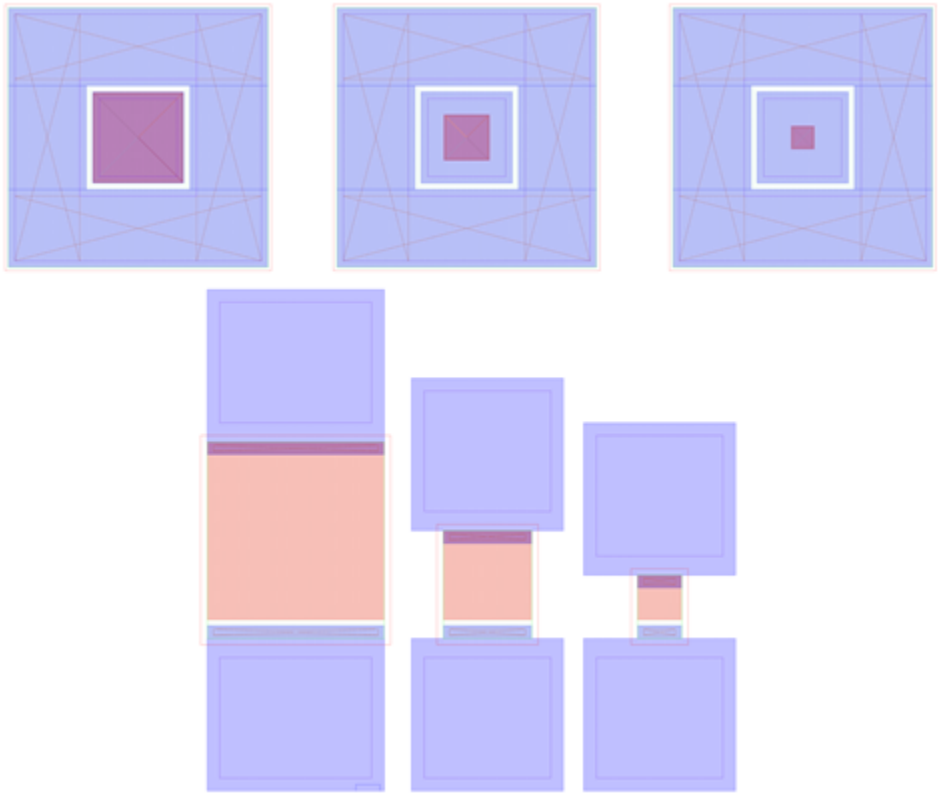


Fig. 3.6: Metal-poly capacitor test structures

3.1.5 Isolation Structures

The minimum metal-metal spacing allowed in the LV process is specified as 5 μm and the minimum metal-width is also specified as 5 μm. In order to verify the quality of the metal and poly traces, and ensure isolation of different traces with minimum separation, isolation test structures were laid out with different lengths. The isolation structure consisted of 4 different types of isolation: (a) metal-poly isolation without overlap, (b) metal-poly isolation with overlap, (c) metal-metal isolation and (d) poly-poly isolation as shown in Fig. 3.8.

When a voltage is applied on the two pads of the isolation structures, no current should flow if the metal/poly traces do not have a short anywhere in the layout. If a current is observed between the two pads, a short is present in the structure which indicates a problem with the defined minimum

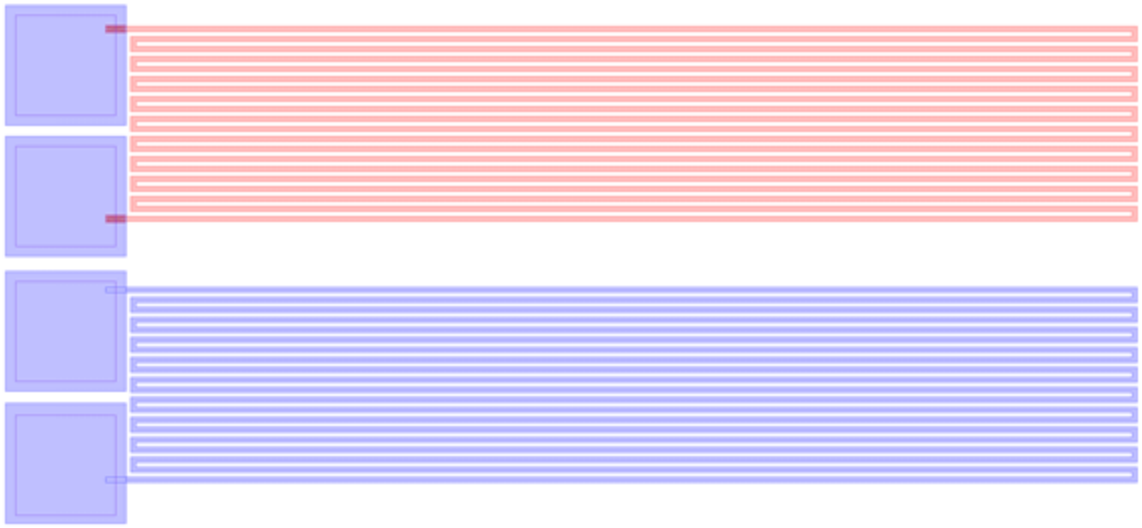


Fig. 3.7: Wound resistors in poly (top) and metal (bottom)

trace width and spacing.

3.2 Substrate Types

In the development of the LV process, the ultimate goal is to be able to integrate the power MOSFET and the low voltage circuits onto a single wafer. One of the possible integration approaches is shown in Fig. 3.9. The power MOSFET is built on a N-type substrate with source and gate on top and drain at the bottom. As a result, the power MOSFET determines the type of the overall wafer to be N-type. In order to develop the NMOS low voltage circuitry on the same wafer, a P-well has to be introduced on the N-type wafer which acts as a common substrate for the entire low voltage chip. There are two ways to obtain the P-well. The first method is to do a selective ion-implantation of the P-well with Al or B ions followed by high temperature annealing. Since the power DiMOSFET structure is also defined using a double-implant process, this method of selective implantation to create the P-well is compatible with the existing power MOSFET process and is favorable from a lower cost point of view. However, due to the low dopant diffusivity in

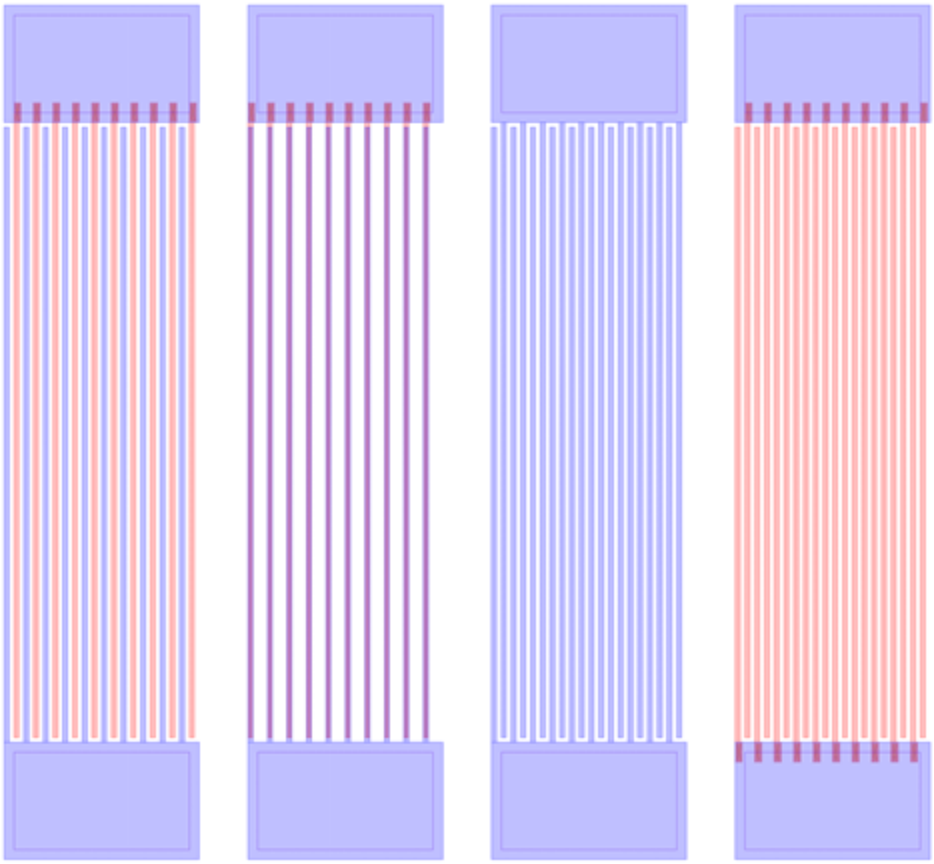


Fig. 3.8: Isolation test structures

SiC, a high energy ion-implantation is needed which damages the SiC/SiO_2 interface, resulting in large density of interface states and surface roughness, which reduce surface mobility. Low surface mobility in the SiC/SiO_2 interface is currently a problem being faced throughout the industry, and the P-well implant process compounds the problem by lowering the surface mobility further which is highly undesirable.

An alternate method to build the P-well is by selective etching of the N-type substrate and growing a P-type epilayer (P-Epi) on the etched surface. The advantage of the P-Epi process is that the P doping concentration in the well can be accurately controlled and there is no damage in the P-well which results in much higher values for surface mobility, which is highly desirable. However, the P-Epi process is not compatible with the existing power MOSFET process, and additional

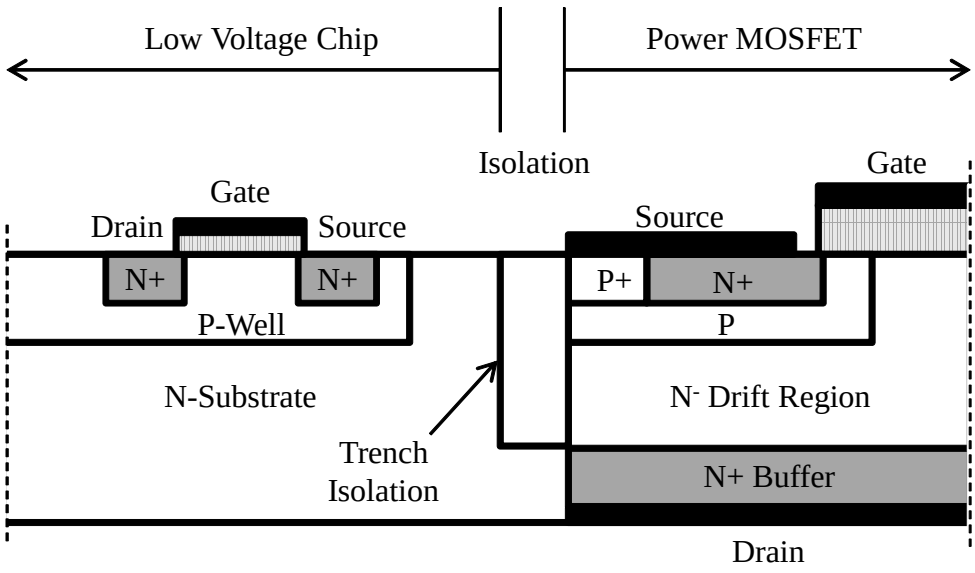


Fig. 3.9: Integration of the power MOSFET and low voltage process

processing steps increase the overall cost of the process. The test chip described in Section 3.1 was fabricated on both types of wells: P-Implanted and P-Epi wells. Test devices from both types were characterized to determine the best possible technology suitable for the development of the gate-driver chip in SiC.

3.3 Device Doping Profiles

Apart from the two different types of P-wells, three types of devices are available in the LV process: (a) depletion, (b) enhancement without threshold adjustment and (c) enhancement with threshold adjustment. A general doping profile for the three type of NMOS devices is shown in Fig. 3.10. In the undoped P-substrate as shown in Fig. 3.10(b), depending on the difference in the work functions of the metal and the substrate, the threshold voltage can be determined by simple calculations. For the sake of argument, it can be assumed that the un-doped structure has a small positive threshold voltage. Such a structure would then behave like an enhancement MOSFET with a low

threshold voltage. As temperature increases, the threshold voltage decreases, and as a result for high temperature operation, a larger threshold voltage is desired to ensure a positive threshold voltage at high temperature. The threshold voltage of the un-doped structure can be increased by increasing the acceptor doping under the gate as shown in Fig. 3.10(c). Such a structure would have a larger threshold voltage than the un-doped structure, and can be referred to as a threshold adjusted enhancement MOSFET. On the other hand, if donor dopants are introduced under the gate as shown in Fig. 3.10(a), a N-type channel is introduced under the gate which exists at zero gate-voltage. Such a device is known as the depletion MOSFET which has a negative threshold voltage.

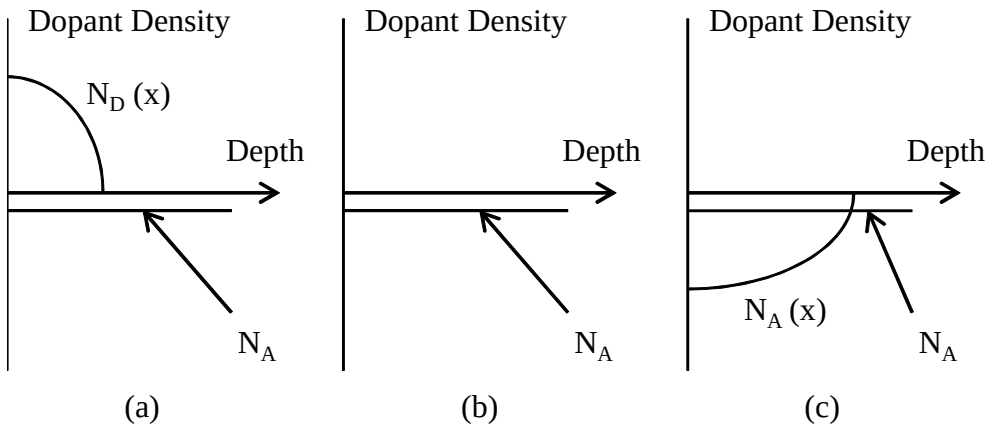


Fig. 3.10: Doping profiles of (a) Depletion, (b) Enhancement without threshold adjust and (c) Enhancement with threshold adjust devices

The depletion MOSFET structure has two depletion regions between the source and the N-channel (Dep1) and the N-channel and the P-substrate regions (Dep2) as shown in Fig. 3.11. The current flows in the N-implanted channel region between Dep1 and Dep2 and can be controlled by controlling the thickness of Dep1 and Dep2, similar to the case of a JFET. Consequently, the depletion MOSFET is also called a buried channel MOSFET. The depletion MOSFET is turned off when a negative voltage is applied to its gate which completely depletes the buried N-channel.

Since a negative gate voltage is required to turn off the device, depletion MOSFETs are normally on and have a negative threshold voltage. The threshold voltage can be controlled by adjusting the donor doping density and the thickness of the N-implant. Depletion MOSFETs are generally less preferred than enhancement MOSFETs due to their normally-on behavior. However, the biggest advantage of depletion MOSFETs in SiC is that since conduction of current happens through the bulk N-implant region and not on the surface, the current is not affected by the poor surface mobility seen in SiC/SiO_2 interfaces.

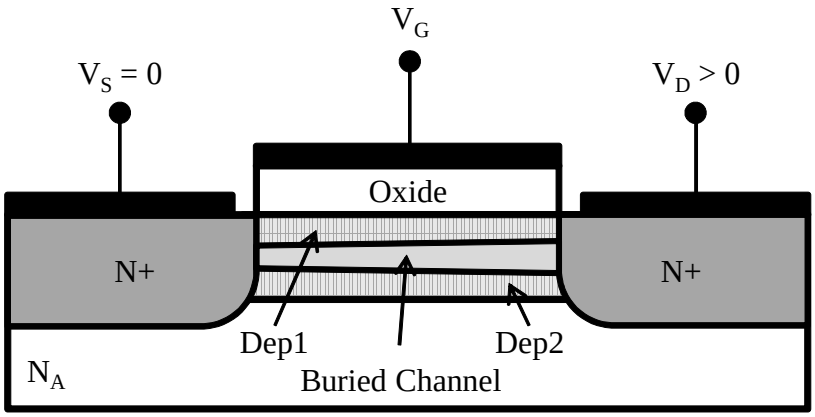


Fig. 3.11: Double depletion layers and buried channel in a depletion MOSFET

Using the information about the substrate types and device doping profiles, several different wafers of the test-chip were fabricated, with each wafer having a different substrate and doping type. Please note that the term *substrate* in the LV process refers to the P-well as shown in Fig. 3.9. Fig. 3.12 shows the different wafer types available in the process. The substrate types are classified into P-Implant and P-Epi types. The P-Epi substrate has been further sub-classified into two types: one with threshold adjustment on the enhancement devices and the other without. Depletion devices in both P-Epi substrate types have the same doping profile.

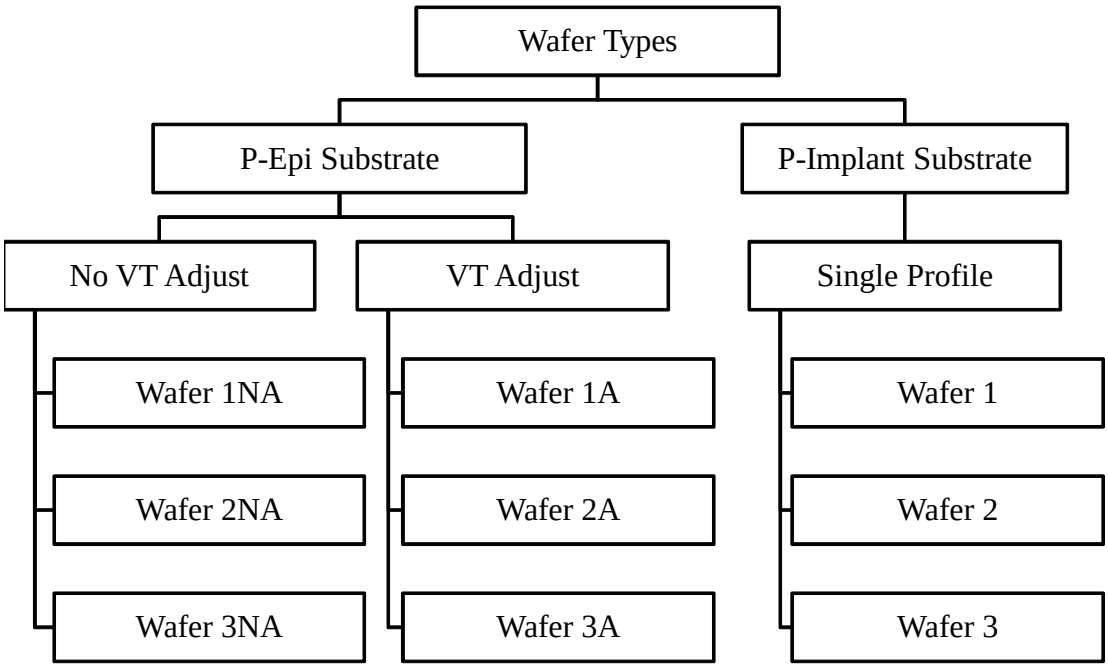


Fig. 3.12: Different wafer types available in the LV process

3.3.1 P-Implant Wafers

The P-Implant wafers are created using the selective P-implant well as described in Section 3.2. The background N doping in the wafer prior to the formation of the P-Implant well has been measured to be 6×10^{15} cm^{-3}. Three different P-well implant profiles have been used to create different P-implant wells in Wafers 1, 2 and 3 as shown in Fig. 3.13. It can be shown from simple MOSFET theory that the higher the P-doping in the substrate near the interface, higher is the threshold voltage of the device. Since the threshold voltage decreases with temperature, it is desirable to have large threshold voltage for enhancement MOSFETs so that with increasing temperature, the threshold voltage remains positive at elevated temperatures. From the simulated

doping profile, it can be observed that Wafer 3 has the largest doping concentration at the surface, followed by Wafer 2 and then Wafer 1. As depth increases, the doping profile for all 3 wafer types is the same. Fig. 3.14 shows the $I_D - V_{GS}$ characteristics of 32 μm$\times$2 μm enhancement devices from the three wafers. It can be seen that Wafer 3 has the largest threshold voltage followed by Wafer 2 and then Wafer 1.

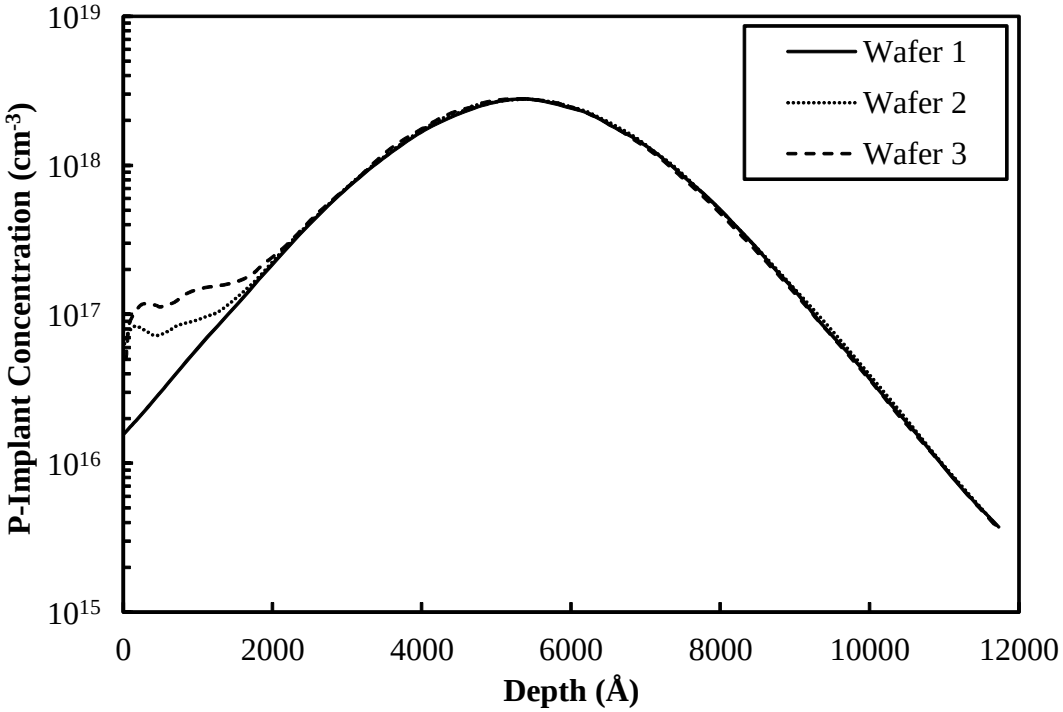


Fig. 3.13: P-implant profile on P-Implant well

In order to form depletion MOSFETs, a N-implant profile as shown in Fig. 3.15 is used for Wafers 1, 2 and 3. Since the implant is N-type, higher N-doping concentration under the gate makes it harder to pinch off the buried channel, which implies that the threshold voltage of the device is more negative for the device. It can be seen that Wafer 3 has higher N-doping concentration than Wafers 1 and 2. The $I_D - V_{GS}$ characteristics of 32 μm$\times$2 μm depletion devices for the three wafers is shown in Fig. 3.16. It can be seen that device from Wafer 3 has the lowest threshold voltage,

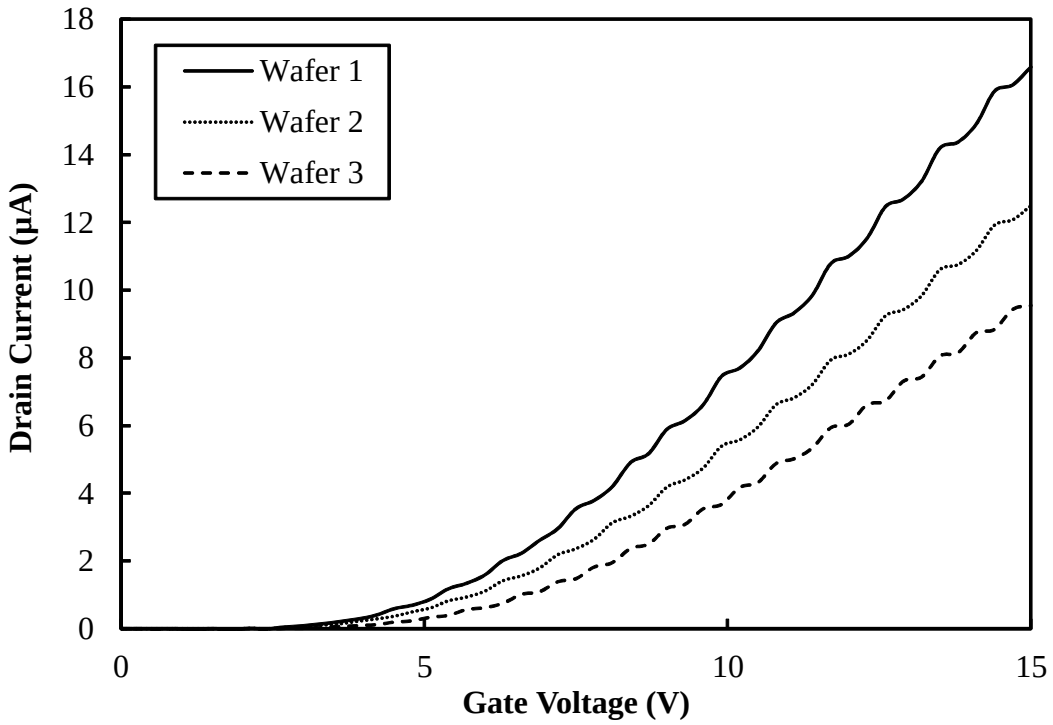


Fig. 3.14: $I_D - V_{GS}$ of 32 μm$\times$2 μm enhancement MOSFET of type P-Implant well

while devices from Wafers 1 and 2 have larger threshold voltage values. However, it can also be seen that the depletion devices from all three P-Implant wafers have a positive threshold voltage which implies that the buried channel is pinched off with no voltage on the gate. As a result, the P-Implant well wafers are not suitable for the design of the gate-driver due to the lack of good depletion devices. Another point to observe is the variation in the $I_D - V_{GS}$ characteristics of the device from Wafer 1 and 2. Despite having the same implant profile (see Fig. 3.16), the $I_D - V_{GS}$ characteristics show the same threshold voltage but different current levels. This is due to variation in the quality of the SiC/SiO_2 interface. Such process variation would not allow the matching of transistors, and would not be suitable for analog circuit design.

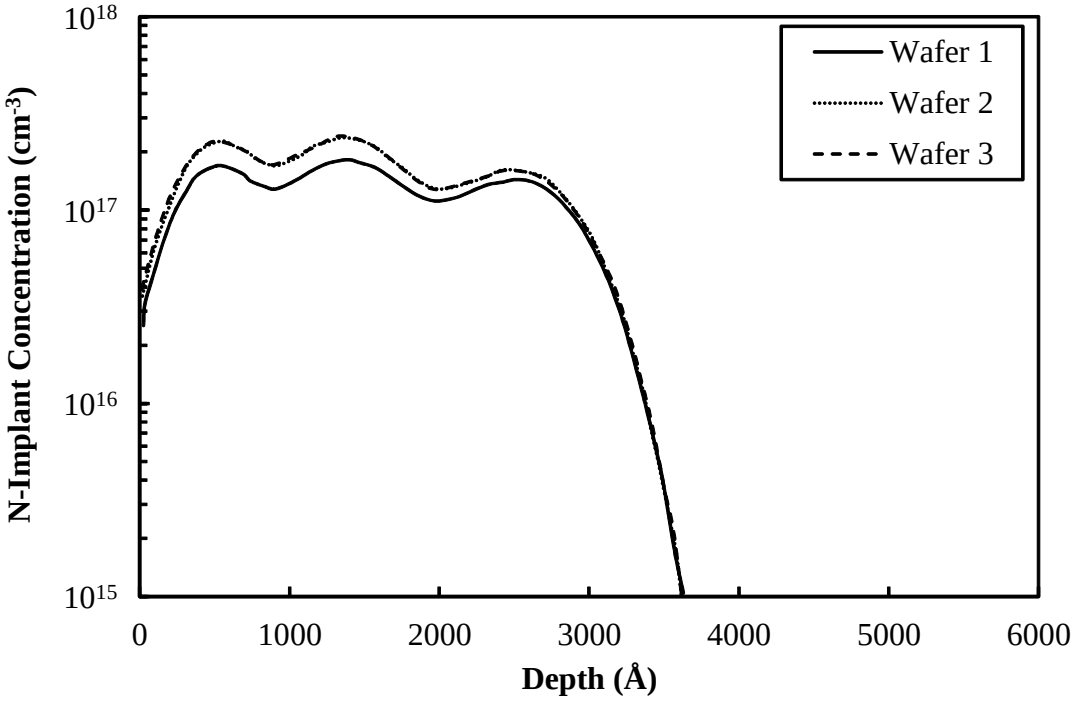


Fig. 3.15: N-implant profile on P-Implant well

3.3.2 P-Epi Wafers

The P-Epi wafers have a P-epilayer substrate with a measured background doping of 5×10^{15} cm^{-3}. Since the epilayer is grown with a constant background P-doping, an additional P-implant is done to tune the threshold voltage of the enhancement MOSFETs. Such an implant in this process is called an ENH implant. ENH implant introduces another layer of P-type dopants in the P-well under the gate-oxide region of the device. The ENH implant only affects enhancement MOSFETs and does not affect the characteristics of depletion MOSFETs. As a result, the P-Epi wafers have been classified into two types based on the presence of the ENH implant in the enhancement MOSFETs.

In order to form the depletion MOSFETs, a simulated N-implant profile is used as shown in Fig. 3.17. The resulting $I_D - V_{GS}$ characteristics for a 32 μm$\times$2 μm depletion MOSFET from all

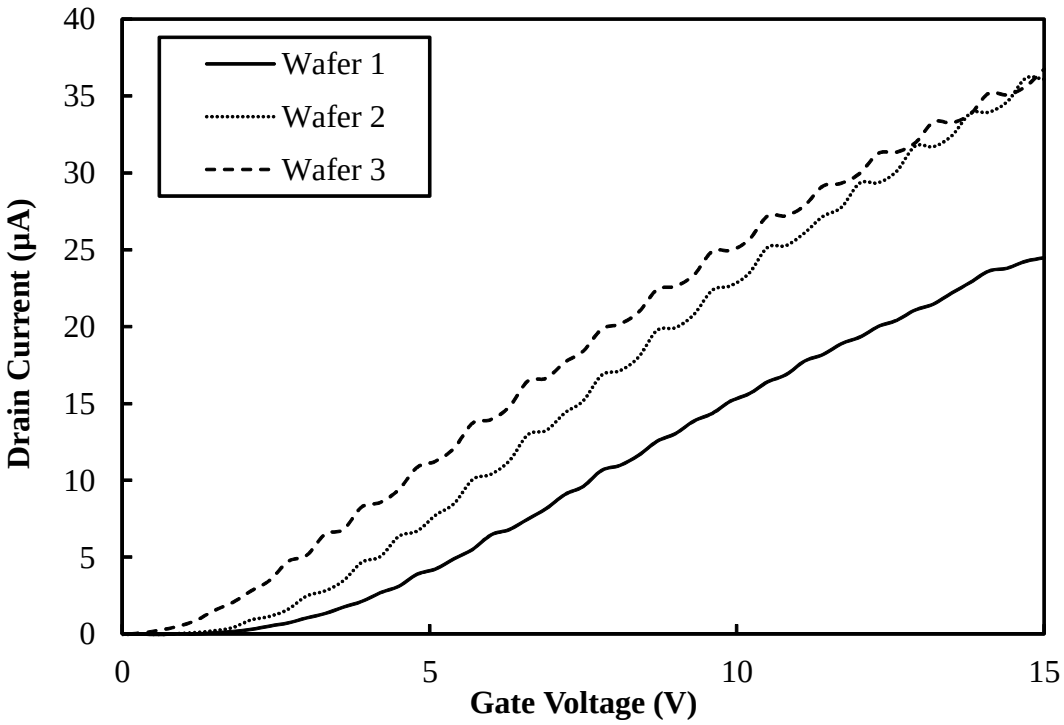


Fig. 3.16: $I_D - V_{GS}$ of 32 μm$\times$2 μm depletion MOSFET of type P-Implant well

the P-Epi wafers are shown in Fig. 3.18. Two important conclusions can be drawn here. Firstly, as expected the depletion devices show very little variation in their characteristics between the wafers with and without the ENH implant, which is meant only to affect the enhancement devices. In addition, it can be seen that Wafers 3A, with and without ENH implant have a very high leakage current in the off-state. It was found that the high leakage current is due to higher implant doses in Wafers 3A, which lead to higher aggregated damage to the SiC crystal. As a result, the doping profiles for Wafers 3A (with and without ENH) are unsuitable to create depletion MOSFETs.

The simulated ENH implant profiles for enhancement Wafers 1A and 2A are shown in Fig. 3.19. It can be seen that the simulated ENH implant profiles for both 1A and 2A are identical. This is confirmed by the comparison between the $I_D - V_{GS}$ characteristics of a 32 μm$\times$2 μm enhancement MOSFET from the two wafer types as shown in Fig. 3.20. It is shown that the effect of the

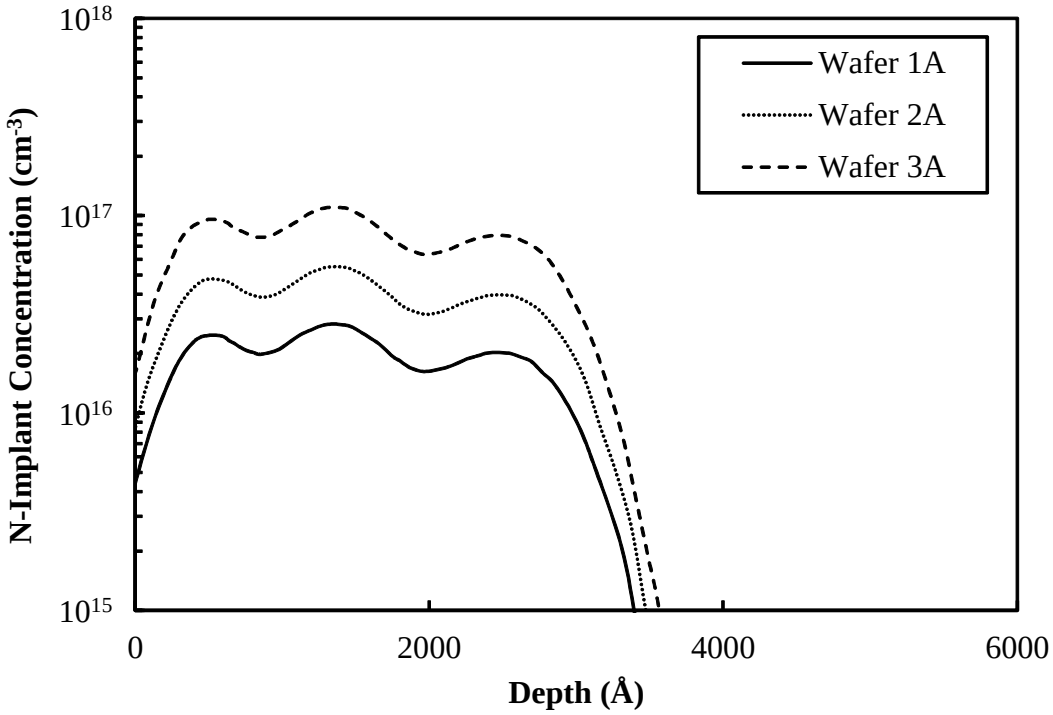


Fig. 3.17: N-implant profile on P-Epi well

ENH implant is to increase the threshold voltage of both Wafer 1A and 2A by $\approx$ 2V. It can be seen from Figs. 3.14, 3.16, 3.18 and 3.20 that **P-Epi Wafer 2A with ENH implant** is the most suitable wafer type with satisfactory performance of both enhancement and depletion MOSFETs.

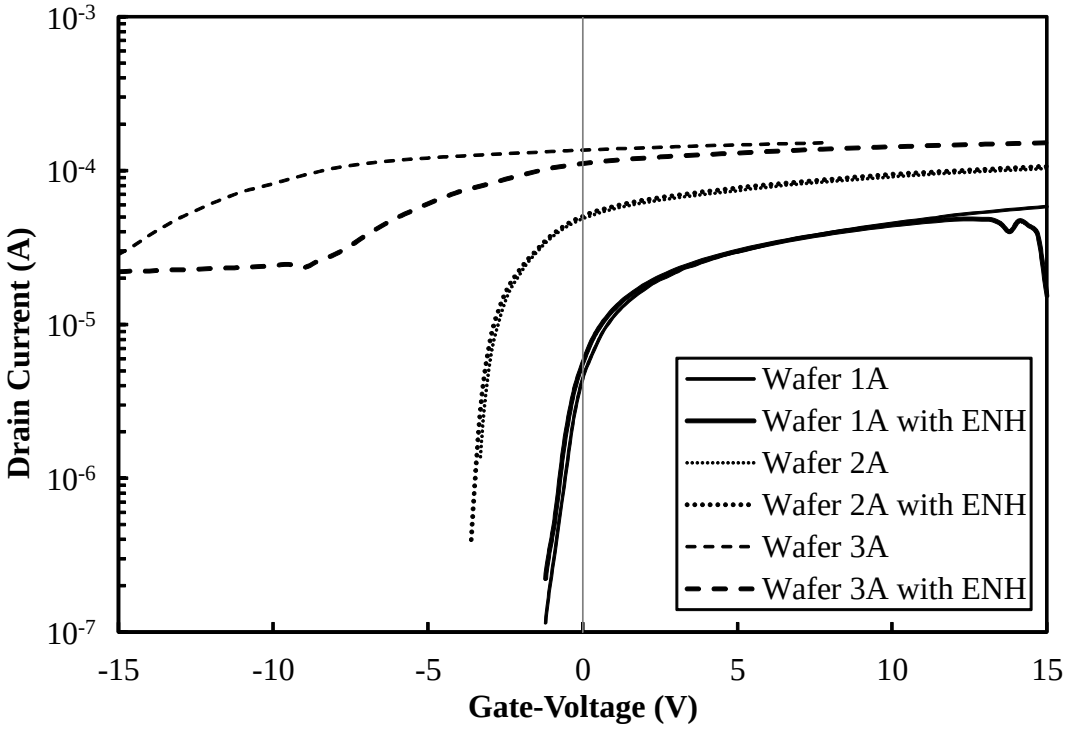


Fig. 3.18: $I_D - V_{GS}$ of 32 μm$\times$2 μm depletion MOSFET of type P-Epi well

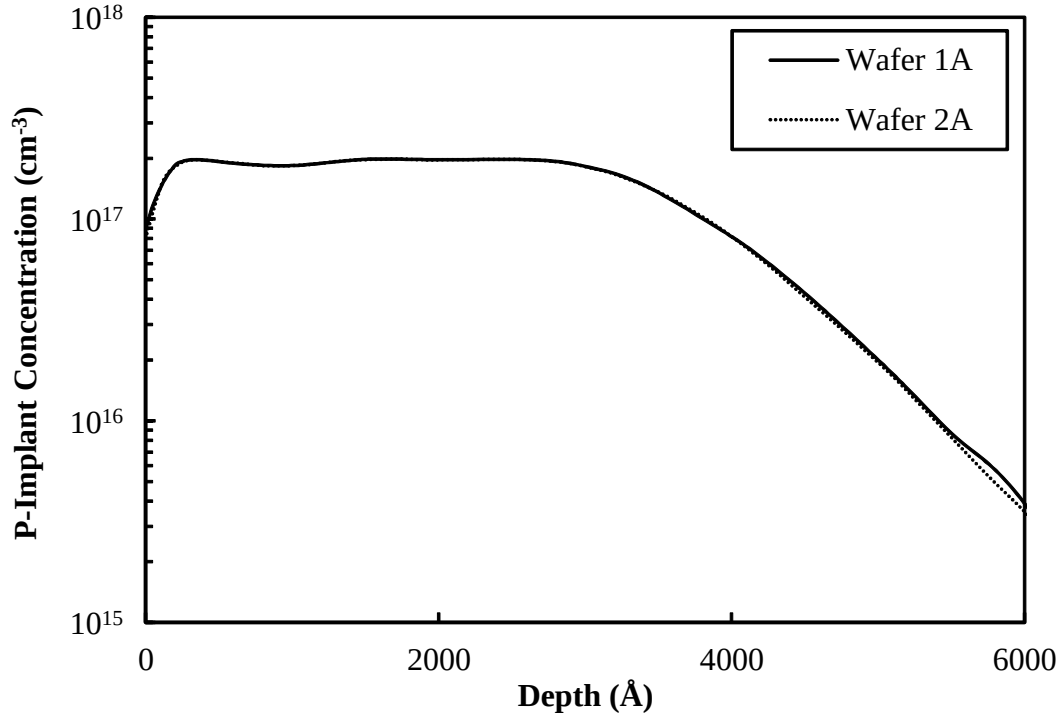


Fig. 3.19: P-implant ENH profile on P-Epi well

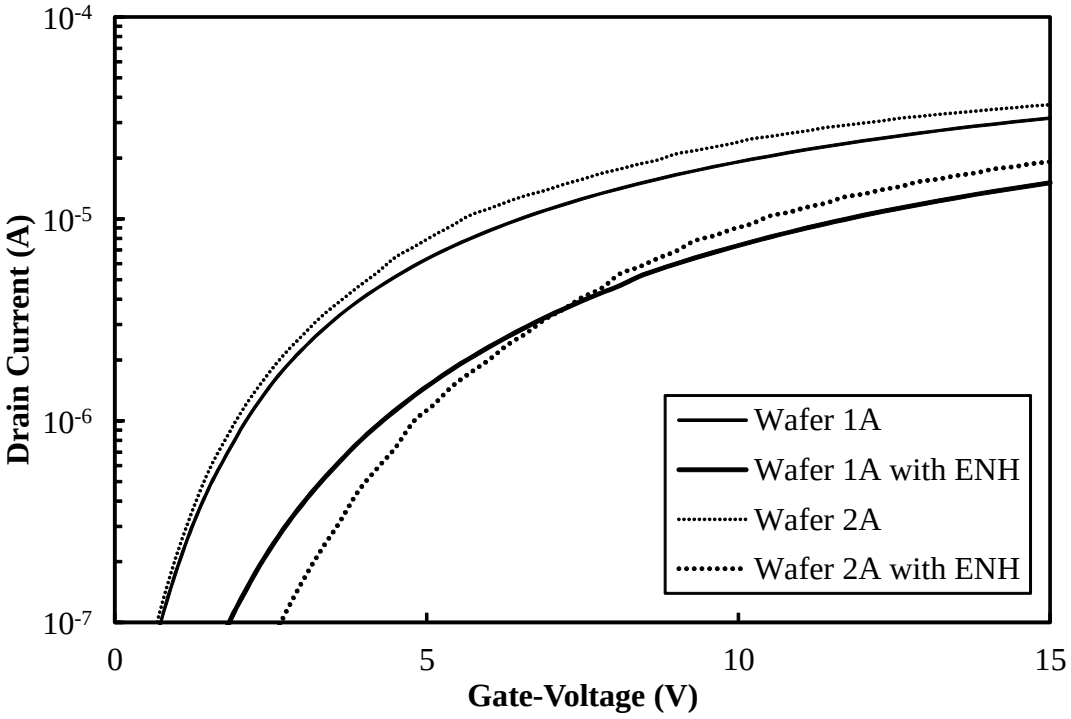


Fig. 3.20: $I_D - V_{GS}$ of 32 μm$\times$2 μm enhancement MOSFET of type P-Epi well

3.4 Depletion MOSFET Characterization

As described in the last section, Wafer 2A with ENH implant has been selected to be the wafer of choice to proceed with designing the gate driver. For sake of brevity, in this section Wafer 2A right is denoted by Wafer 2AR. In order to develop a compact models for MOSFETs from Wafer 2AR, MOSFETs of different W/L ratios as shown in Fig. 3.2 were characterized for their DC performance over temperature. In addition, large MOSFET structures as shown in Fig. 3.4 weree used to extract the C-V gate-capacitance behavior. This section describes the characterization results for depletion MOSFETs of type 2AR and the next section will describe the characterization results for enhancement MOSFETs.

All devices were characterized using a Keithley 4200 Semiconductor Parameter Analyzer with 4 Remote Pre-Amps (Model 4200-PA) installed for low current capability [51]. The SMUs were controlled using Keithley's Interactive Test Environment (KITE). The SMUs were connected to a Signatone High Power Probe Station using shielded BNC cables. Proper shielding and grounding procedures were followed while characterization to minimize noise in the measurements. Signatone SE-20T single-ended probe tips were used for DC characterization and Keithley shielded probe tips were used for C-V measurements.

Note: For all the tests described in subsequent sections, the source terminal is grounded and is taken as the reference, unless specified otherwise.

3.4.1 Gate Capacitance

The gate-capacitance C_{GG} represents the total capacitive load seen at the gate of the MOSFET. It is an important characteristic that needs to be modeled well. C_{GG} yields invaluable information

about the MOSFET channel formation like the flat-band voltage, density of interface states and the quality of the oxide. In digital design, gate of the MOSFET is used as a load for previous stages and an accurate description of the variation of the gate capacitance with bias is important while designing each stage of the digital circuit.

The depletion and enhancement MOSFET C-V structures were used to characterize $C_{GG} - V_G$. The MOSFETs were connected in a gated diode connected where the source, drain and the body were tied together to ground. This connection allowed the n^+ diffusion of the source and drain to provide the required minority carriers to the inversion channel and enabled the proper characterization of $C_{GG} - V_G$.

Fig. 3.21 shows the scaled $C_{GG} - V_G$ characteristics of a $32\mu m \times 8\mu m$ depletion MOSFET at a frequency of 10 kHz and 1MHz. The source, drain and body were tied to ground, and the gate-bias was swept from -15 V to 15 V with a sweep rate of 0.1 V/s. The actual measurement was taken on a much larger $20 \times 50\mu m \times 50\mu m$ C-V structure as shown in Fig. 3.4 and then scaled down for the corresponding device area. The oxide thickness can be calculated from the $C_{GG} - V_G$ curve using the following equation

$$C_{OX} = \frac{\varepsilon_{SiC} A}{T_{OX}} \tag{3.1}$$

where C_{OX} is the maximum capacitance value from the $C_{GG} - V_G$ curve, A is the area of the capacitor plates and T_{OX} is the oxide thickness. Using values of C_{OX} and A from Fig. 3.4 as 0.2 pF and $20 \times 50\mu m \times 50\mu m$ respectively in (3.1) yielded an oxide thickness of 41 nm, which is within 2.5% of the technology specified oxide thickness of 40 nm.

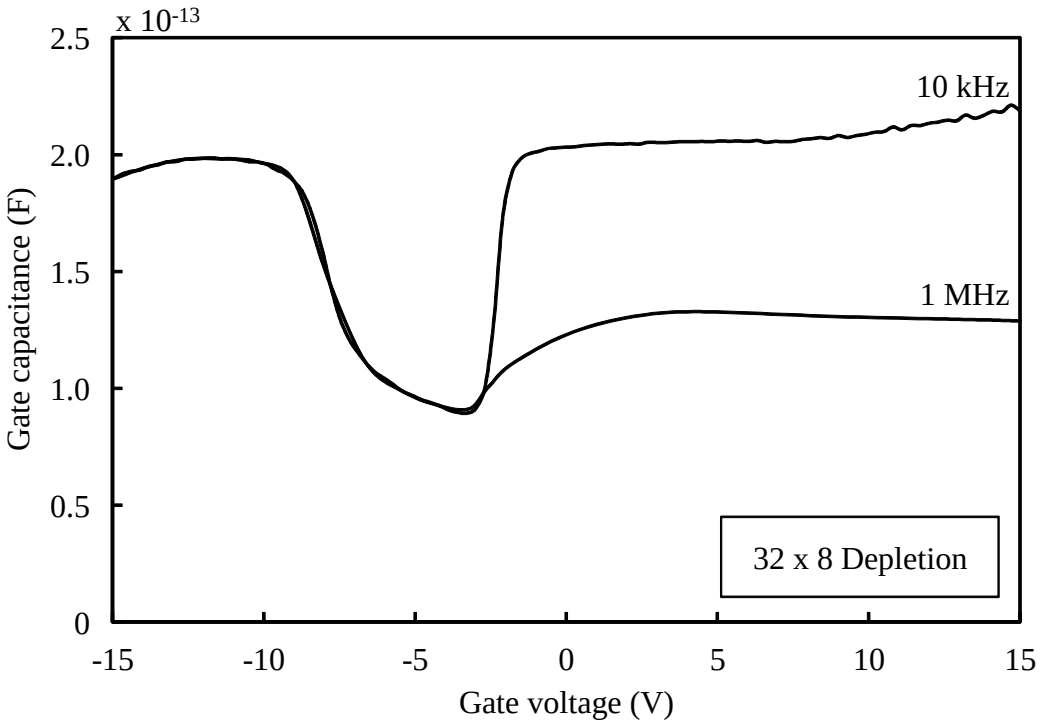


Fig. 3.21: Scaled $C_{GG} - V_G$ characteristics of a $32\mu m \times 8\mu m$ depletion MOSFET at 25 °C

3.4.2 Input Characteristics

For the input characteristics $I_D - V_{GS}$, gate voltage V_{GS} was swept from -6 V to 15 V, drain voltage V_{DS} was held constant at 50 mV and bulk voltage V_{BS} was stepped from 0 V to -15 V in 3 V steps. The input characteristics allow the extraction of threshold voltage V_T and mobility reduction parameters at higher gate-biases. The input characteristics were measured for each device at 25 °C, 125 °C and 225 °C.

From the device array, the device sizes were chosen as follows:

- Largest Device (W/L = 4): $32\mu m \times 8\mu m$
- Widest Device (W/L = 16): $32\mu m \times 2\mu m$
- Narrowest Device (W/L = 1): $8\mu m \times 8\mu m$

Figs. 3.22, 3.23 and 3.24 show the $I_D - V_{GS}$ characteristics of the $32\mu m \times 8\mu m$, $32\mu m \times 2\mu m$ and $8\mu m \times 8\mu m$ depletion MOSFETs at 25 °C respectively. It can be observed that being buried-channel devices, the current flows in the buried channel away from the surface and as a result, the input characteristics are less affected by interface states and Coulumbic scattering. It will be shown later that the presence of a large number of interface states affect the performance of enhancement MOSFETs, which are surface-channel devices. Figs. 3.25, 3.26 and 3.27 show the $g_m - V_{GS}$ characteristics of the same devices at room temperature.

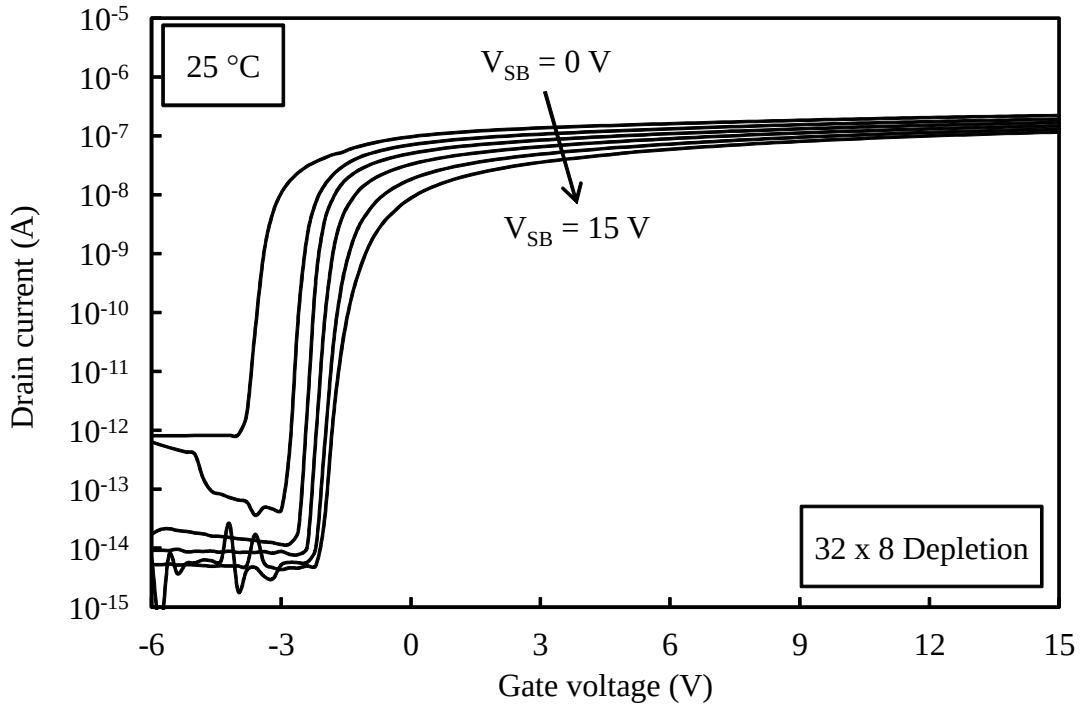


Fig. 3.22: $I_D - V_{GS}$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET at 25 °C

Fig. 3.28 compares the $I_D - V_{GS}$ characteristics of the three devices for zero back bias condition. It can be seen that the $32\mu m \times 2\mu m$ device shows a smaller threshold voltage V_T due to normal short channel effect, but both the $8\mu m$ length devices have the same threshold voltage. The slight increase in the threshold voltage of the $8\mu m \times 8\mu m$ device is due to normal narrow width effect.

The variation of the $I_D - V_{GS}$ characteristics of the $32\mu m \times 8\mu m$, $32\mu m \times 2\mu m$ and $8\mu m \times 8\mu m$

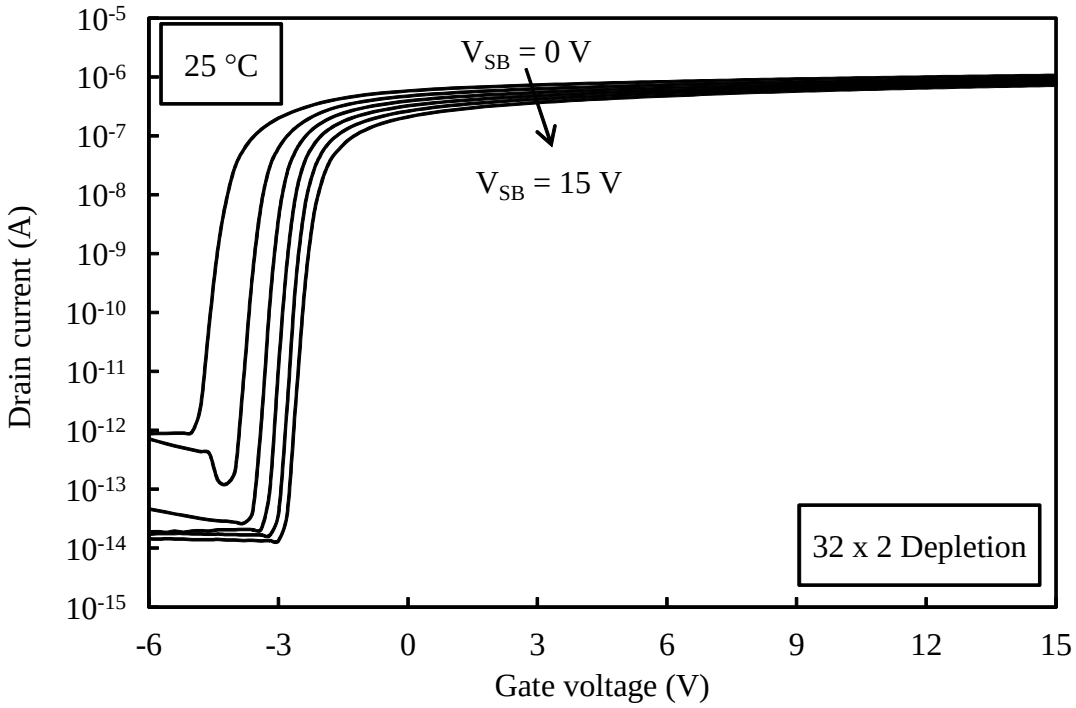


Fig. 3.23: $I_D - V_{GS}$ characteristics of $32\mu m \times 2\mu m$ depletion MOSFET at 25 °C

depletion MOSFETs with temperature are shown in Figs. 3.29, 3.30 and 3.31 respectively. It can be seen that the threshold voltage decreases almost linearly with temperature.

3.4.3 Output Characteristics

The measurement of output characteristics $I_D - V_{DS}$ was done by sweeping drain voltage V_{DS} from 0 V to 15 V, stepping gate voltage V_{GS} from -9 V to 15 V in 3 V steps and keeping bulk voltage V_{BS} constant at 0 V. The output characteristics of $32\mu m \times 8\mu m$, $32\mu m \times 2\mu m$ and $8\mu m \times 8\mu m$ depletion MOSFETs at room temperature are shown in Figs. 3.32, 3.33 and 3.34 respectively. The $g_{DS} - V_{DS}$ characteristics for the same devices are shown in Figs. 3.35, 3.36 and 3.37 respectively.

The comparison between the $I_D - V_{DS}$ characteristics of the three device sizes for $V_{GS} = 6V$ is shown in Fig. 3.41. Fig. 3.33 highlights the channel length modulation effect in the shorter $32\mu m \times 2\mu m$ device. The longer devices have a relatively flat saturation region, and are more

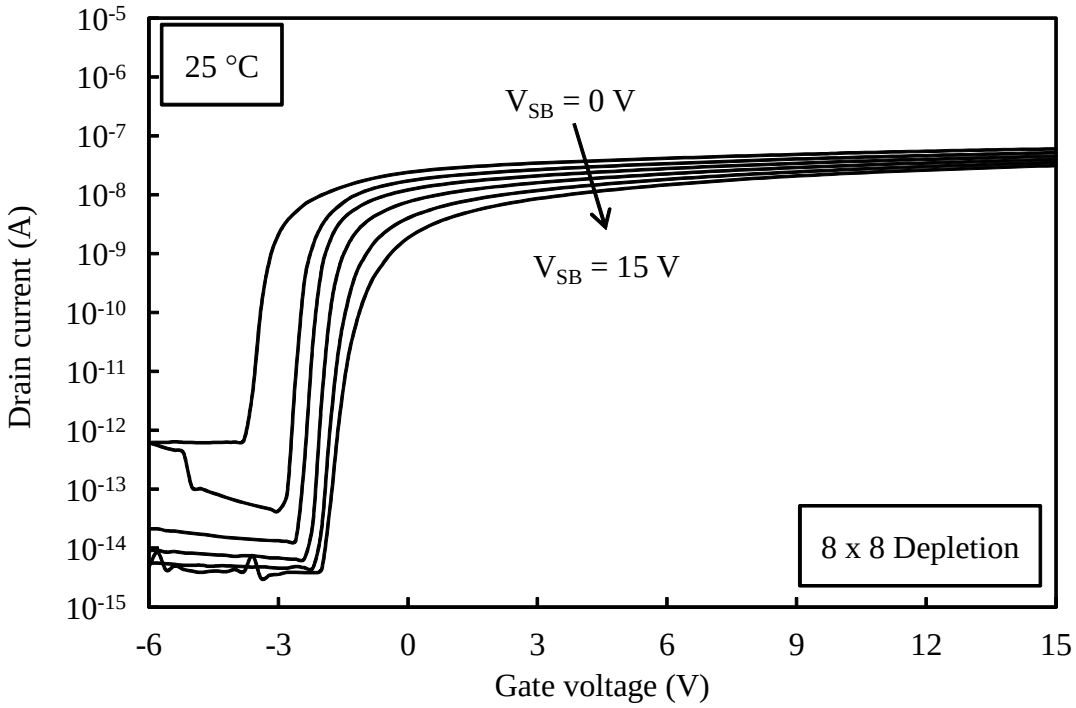


Fig. 3.24: $I_D - V_{GS}$ characteristics of $8\mu m \times 8\mu m$ depletion MOSFET at 25 °C

suitable for applications requiring a high output resistance. The shorter device is more suitable as a pull-up or pull-down transistor due to much larger current for a given gate-voltage. The $I_D - V_{DS}$ characteristics of the three device sizes for $V_{GS} = 6V$ at 25 °C, 125 °C and 225 °C is shown in Figs. 3.38, 3.39 and 3.40 respectively. Due to reduction in bulk mobility with temperature, the current decreases for all 3 devices approximately linearly with temperature.

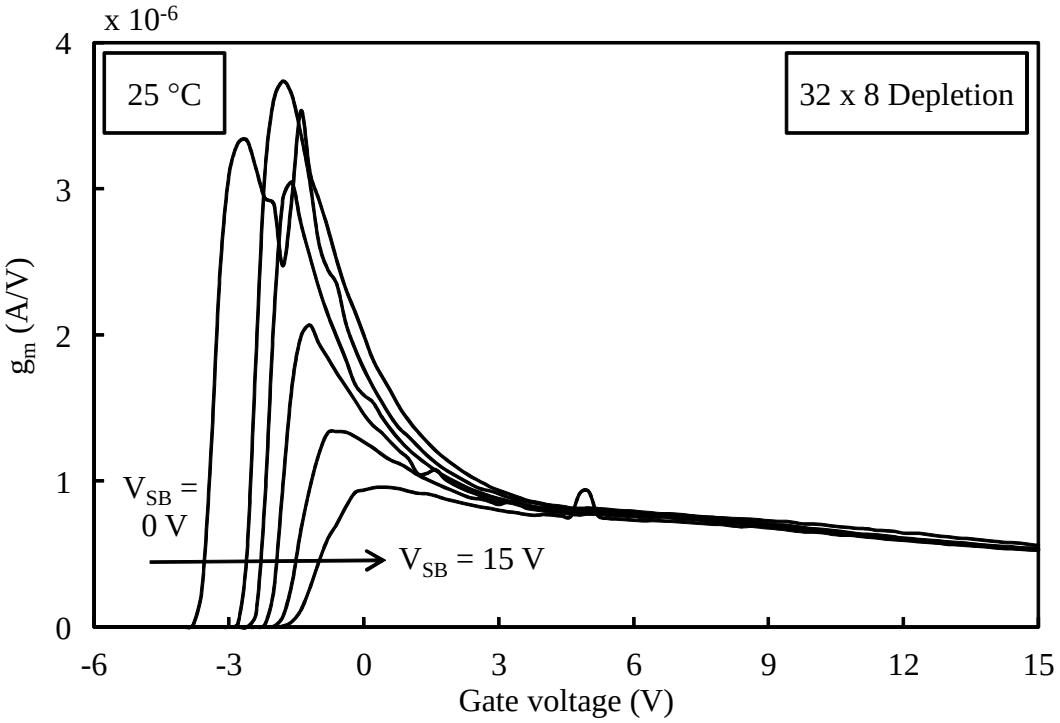


Fig. 3.25: $g_m - V_{GS}$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET at 25 °C

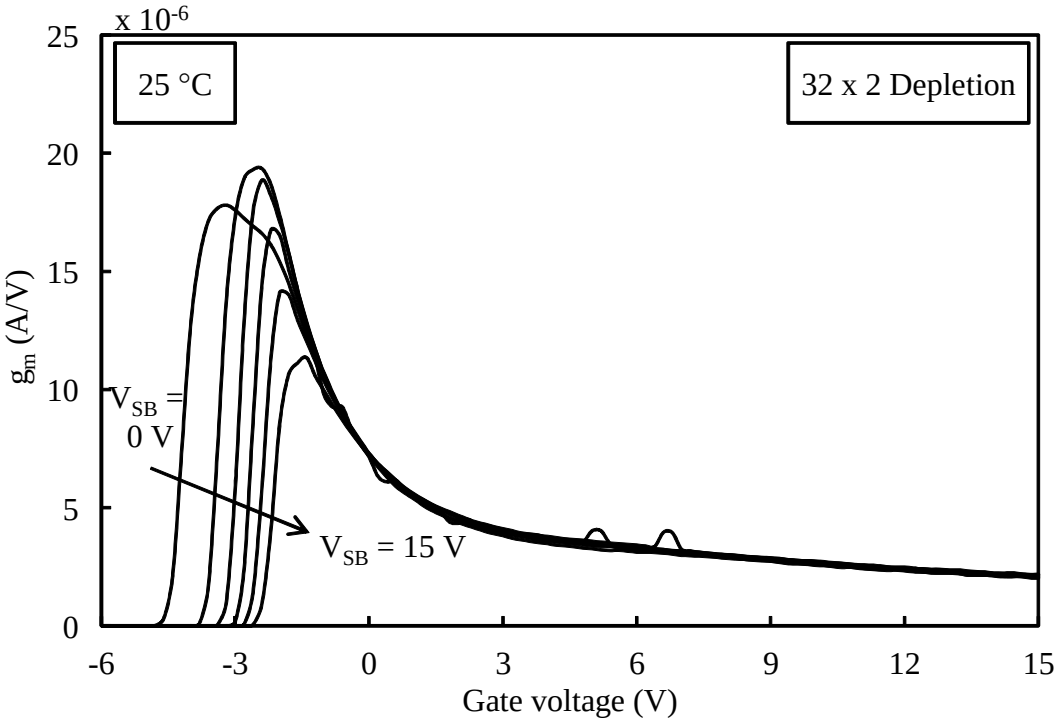


Fig. 3.26: $g_m - V_{GS}$ characteristics of $32\mu m \times 2\mu m$ depletion MOSFET at 25 °C

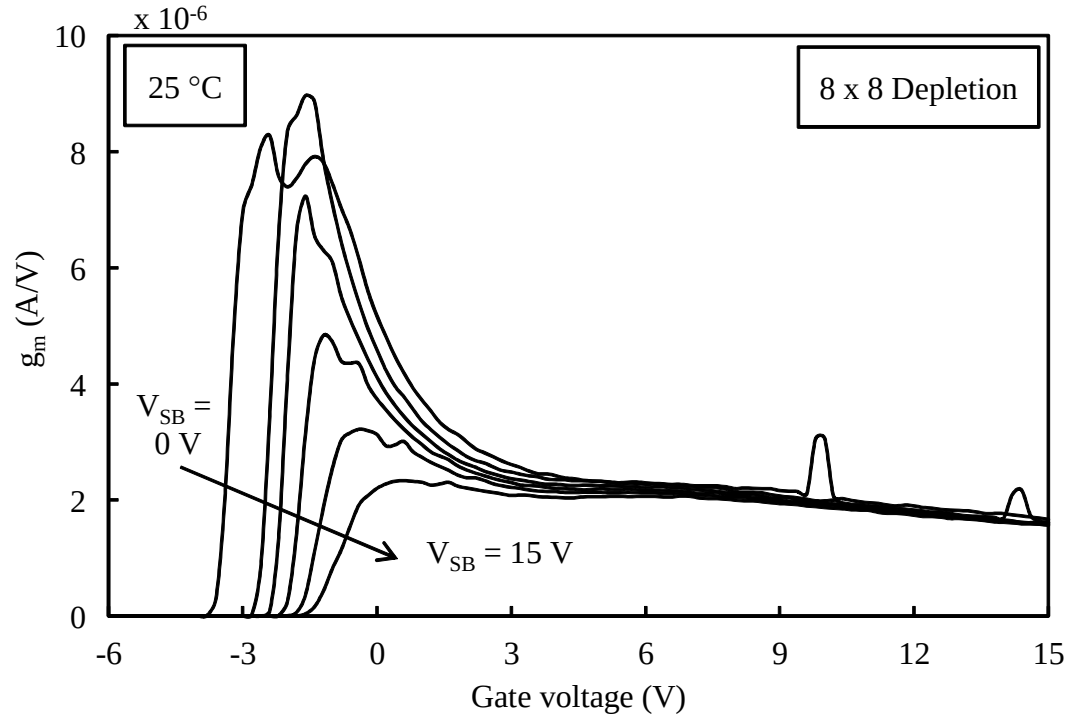


Fig. 3.27: $g_m - V_{GS}$ characteristics of $8\mu m \times 8\mu m$ depletion MOSFET at 25 °C

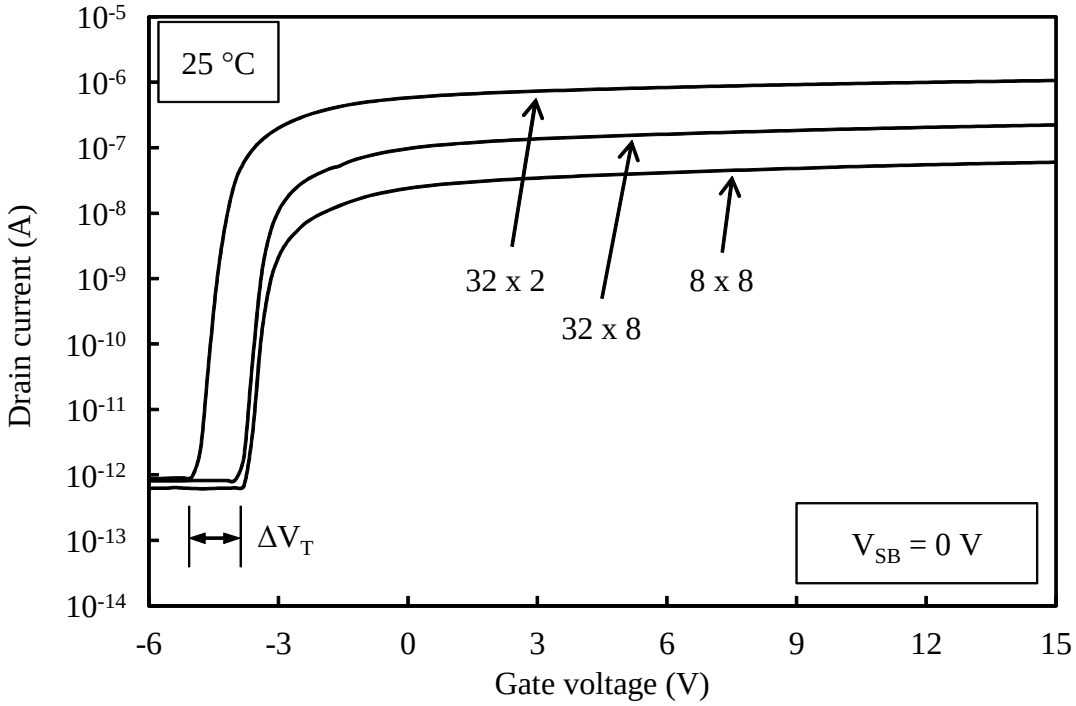


Fig. 3.28: Comparison of $I_D - V_{GS}$ characteristics ($V_{SB} = 0\ V$) of $32\mu m \times 8\mu m$, $32\mu m \times 2\mu m$ and $8\mu m \times 8\mu m$ depletion MOSFETs at 25 °C

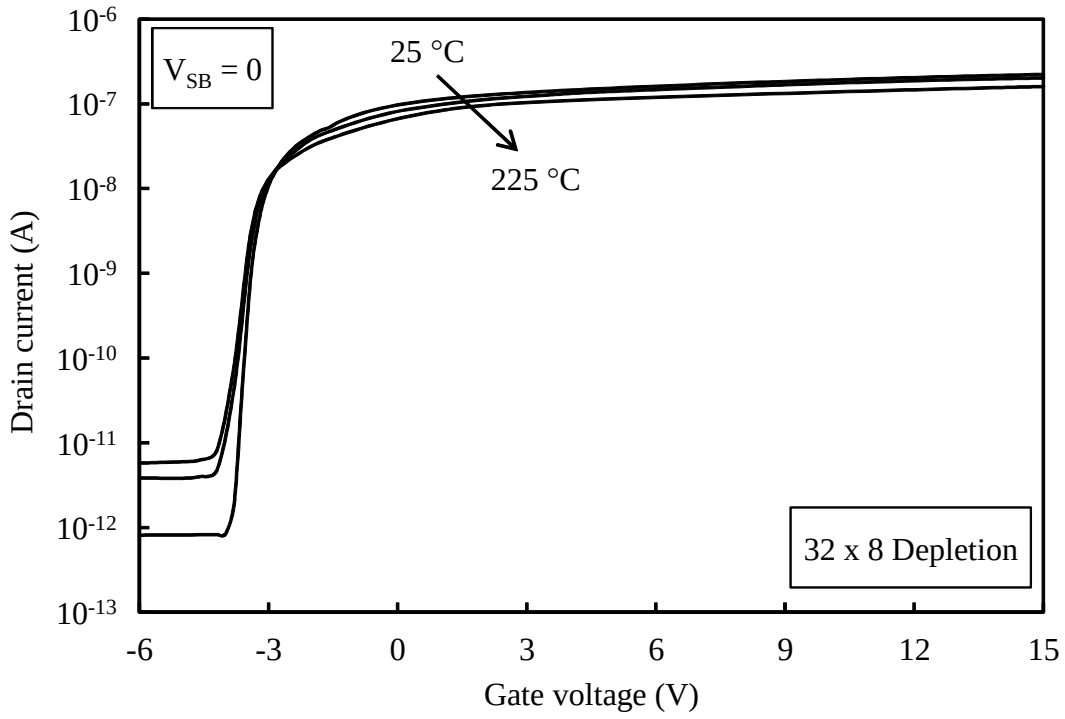


Fig. 3.29: $I_D - V_{GS}$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET at 25 °C, 125 °C and 225 °C

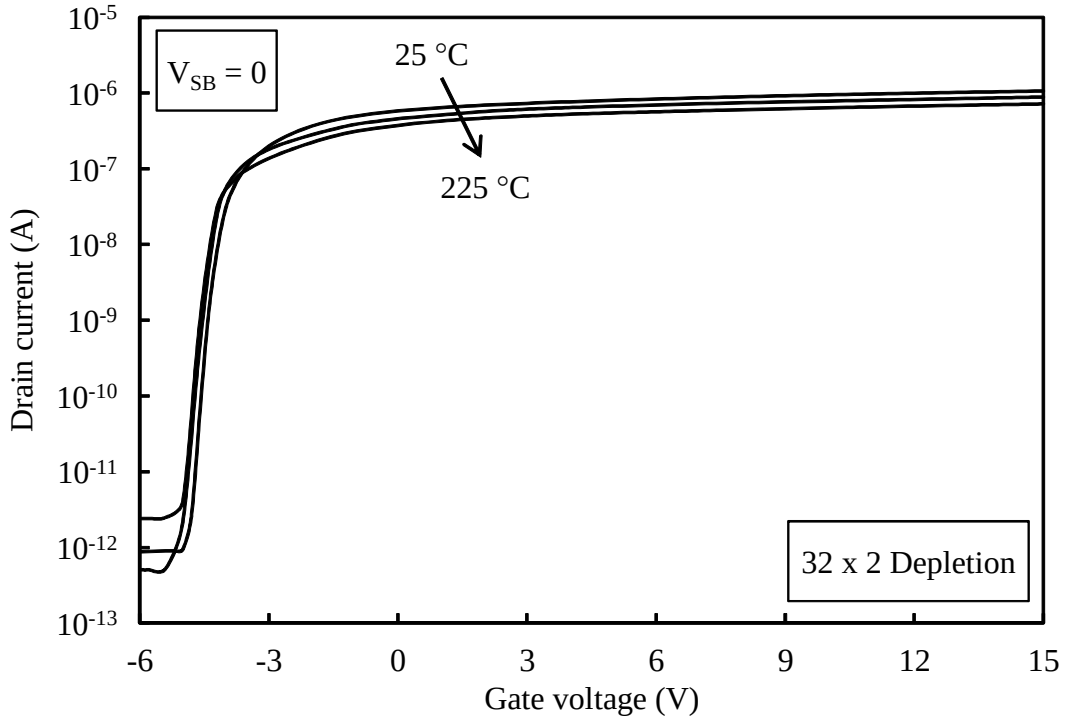


Fig. 3.30: $I_D - V_{GS}$ characteristics of $32\mu m \times 2\mu m$ depletion MOSFET at 25 °C, 125 °C and 225 °C

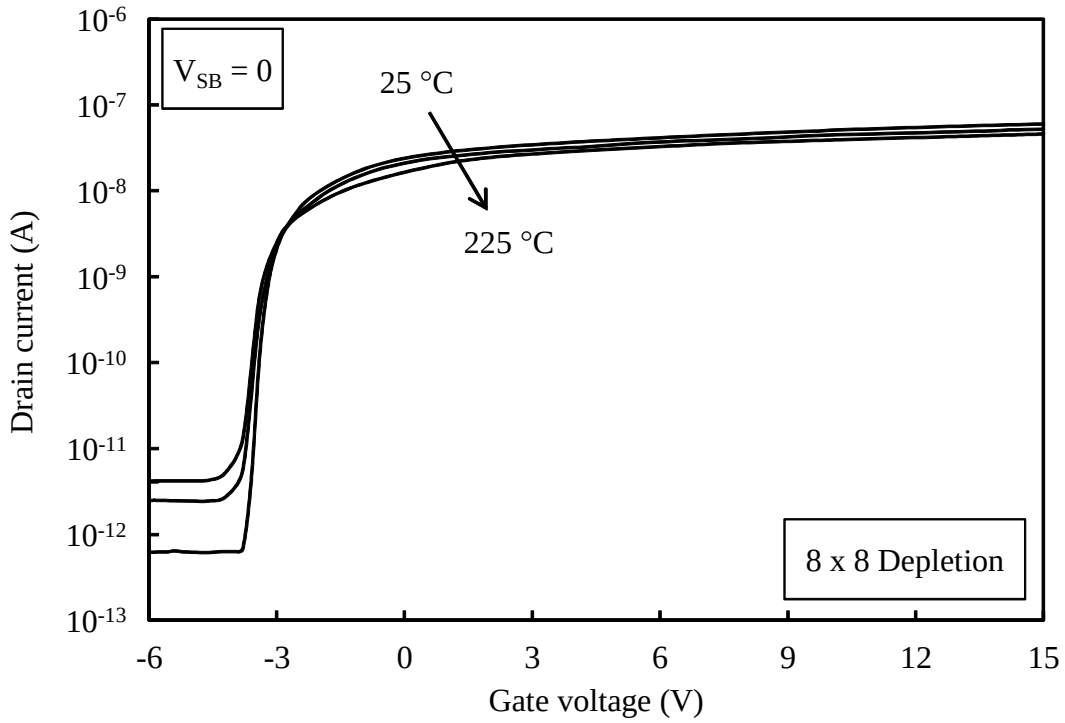


Fig. 3.31: $I_D - V_{GS}$ characteristics of $8\mu m \times 8\mu m$ depletion MOSFET at 25 °C, 125 °C and 225 °C

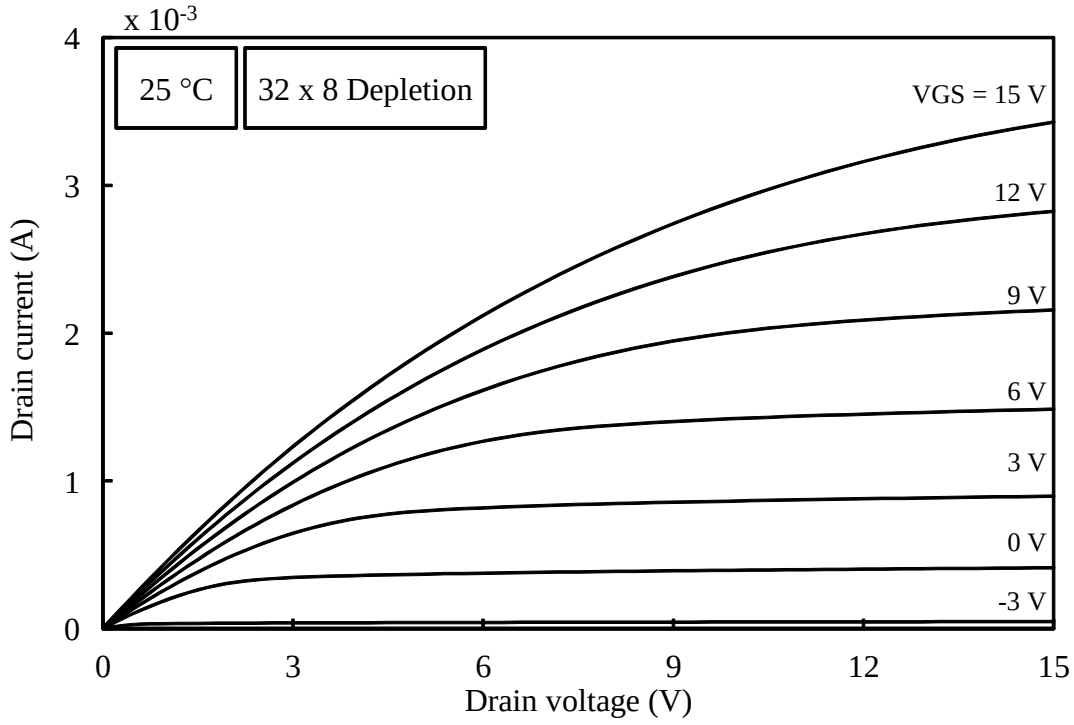


Fig. 3.32: $I_D - V_{DS}$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET at 25 °C

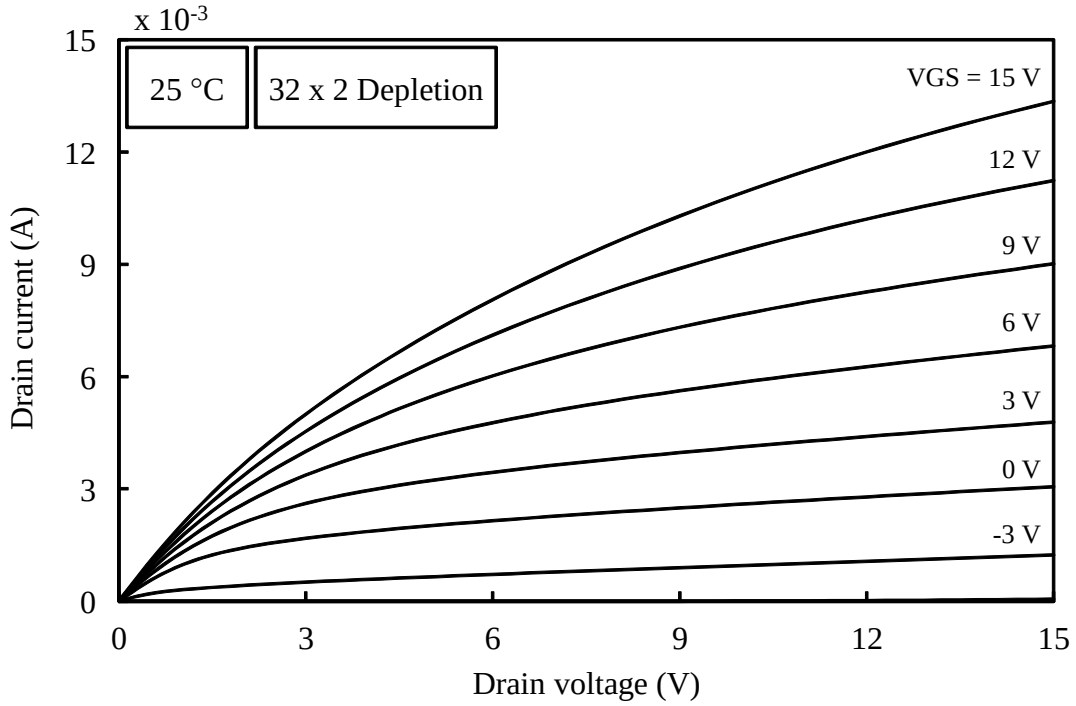


Fig. 3.33: $I_D - V_{DS}$ characteristics of $32\mu m \times 2\mu m$ depletion MOSFET at 25 °C

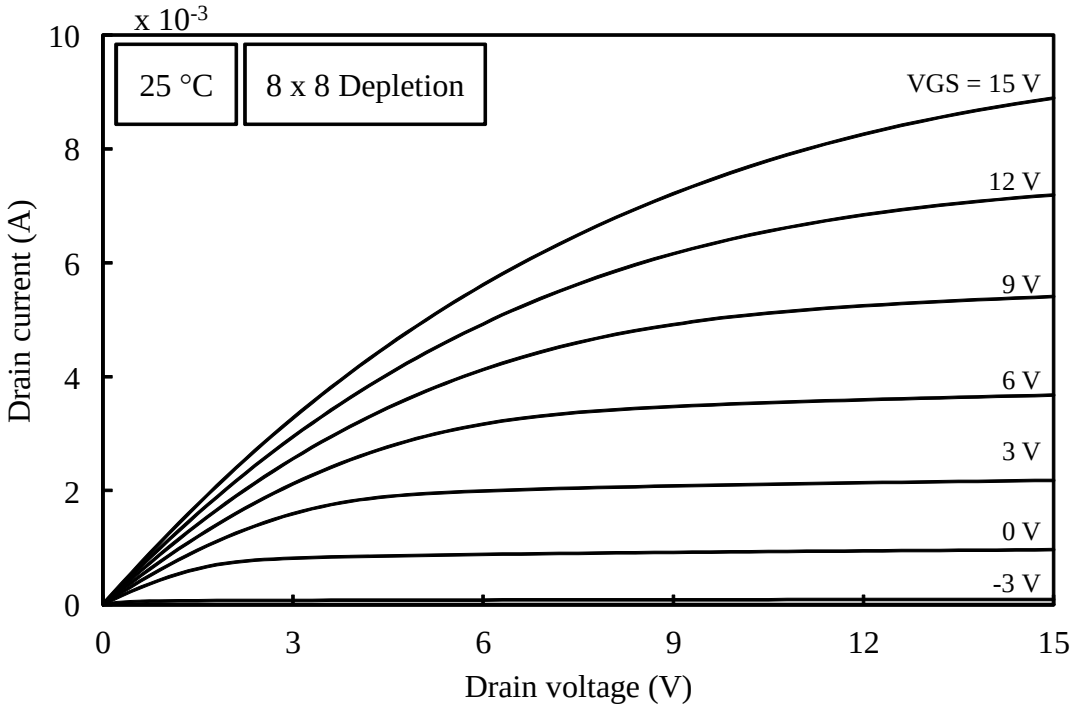


Fig. 3.34: $I_D - V_{DS}$ characteristics of $8\mu m \times 8\mu m$ depletion MOSFET at 25 °C

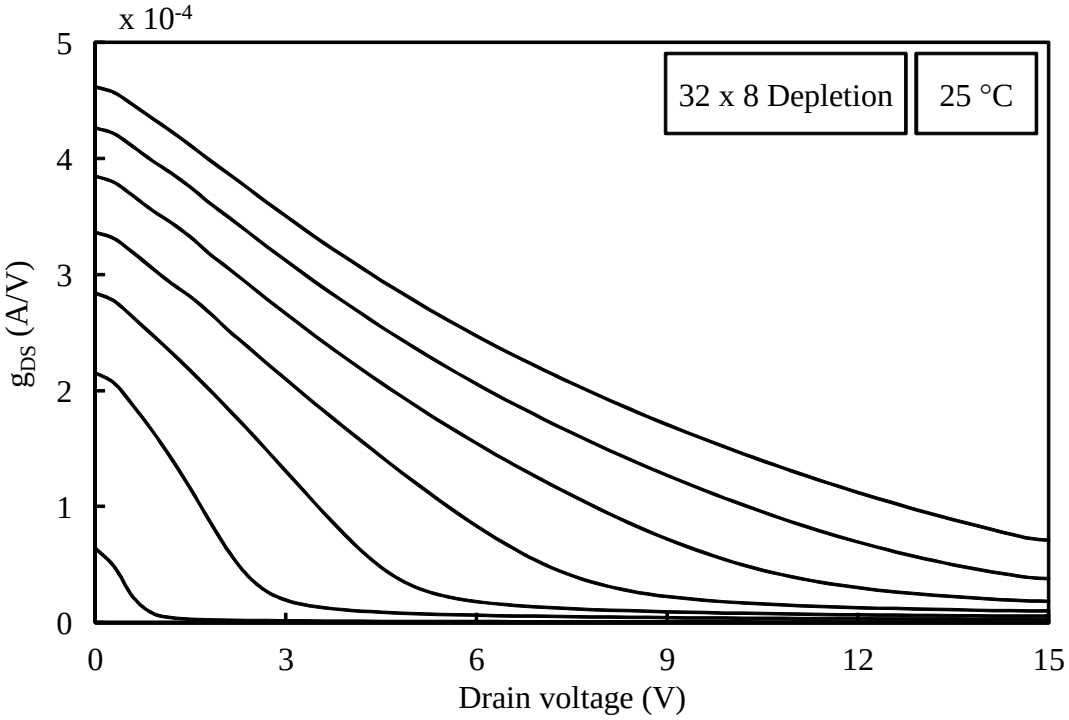


Fig. 3.35: $g_{DS} - V_{DS}$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET at 25 °C

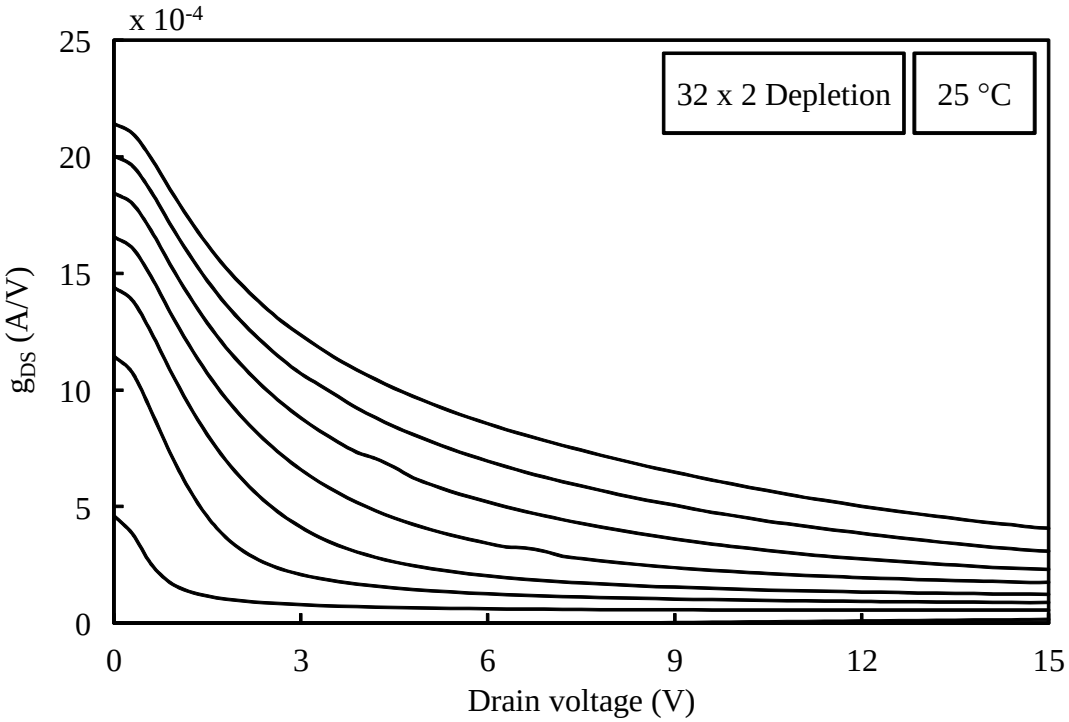


Fig. 3.36: $g_{DS} - V_{DS}$ characteristics of $32\mu m \times 2\mu m$ depletion MOSFET at 25 °C

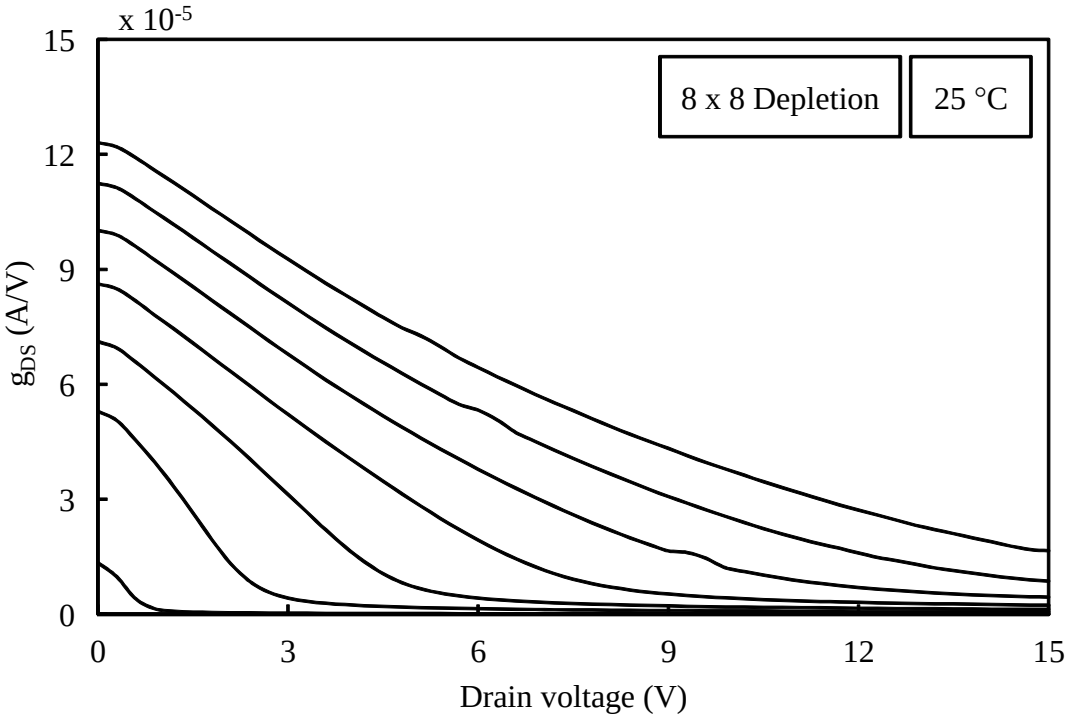


Fig. 3.37: $g_{DS} - V_{DS}$ characteristics of $8\mu m \times 8\mu m$ depletion MOSFET at 25 °C

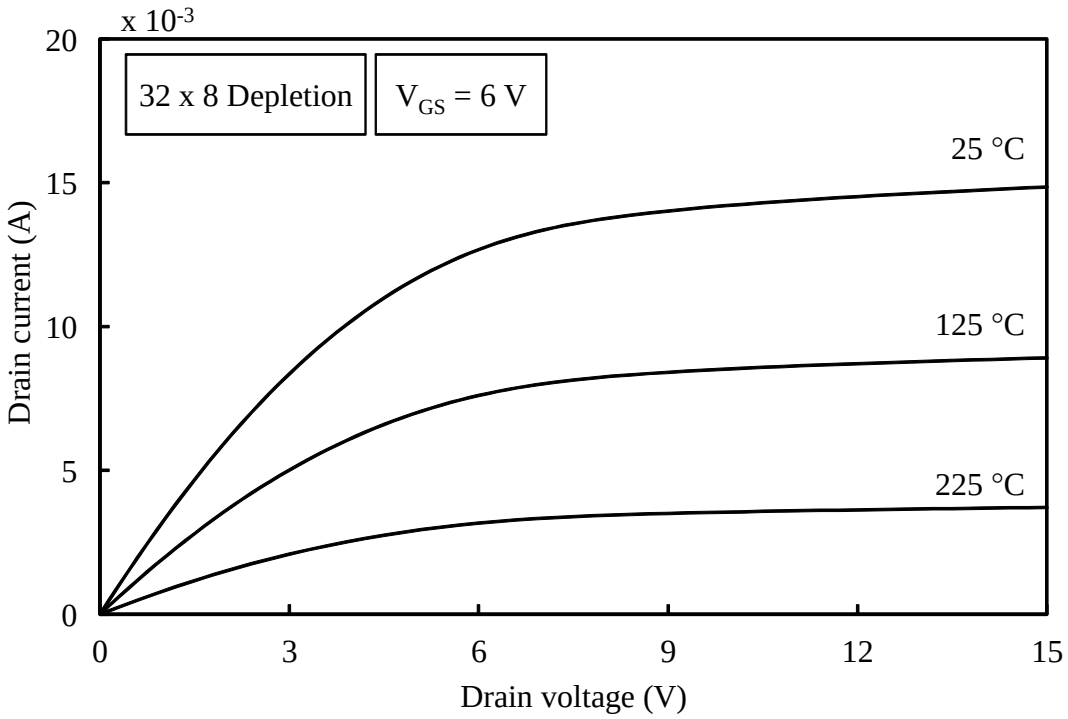


Fig. 3.38: $I_D - V_{DS}$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET over temperature

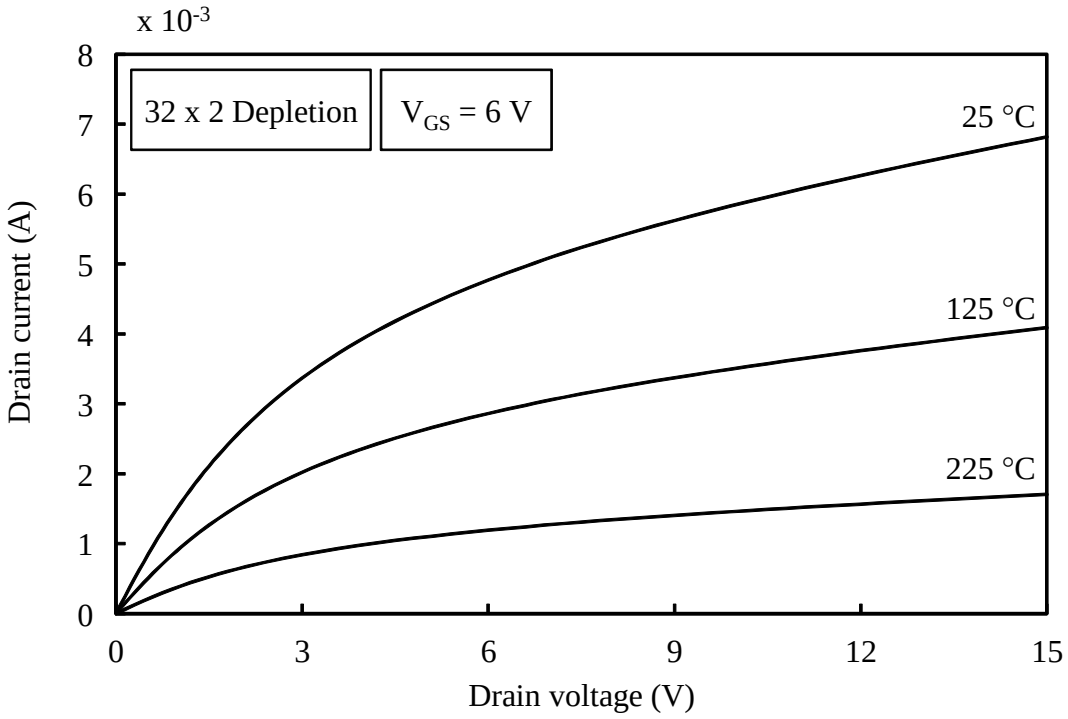


Fig. 3.39: $I_D - V_{DS}$ characteristics of $32\mu m \times 2\mu m$ depletion MOSFET over temperature

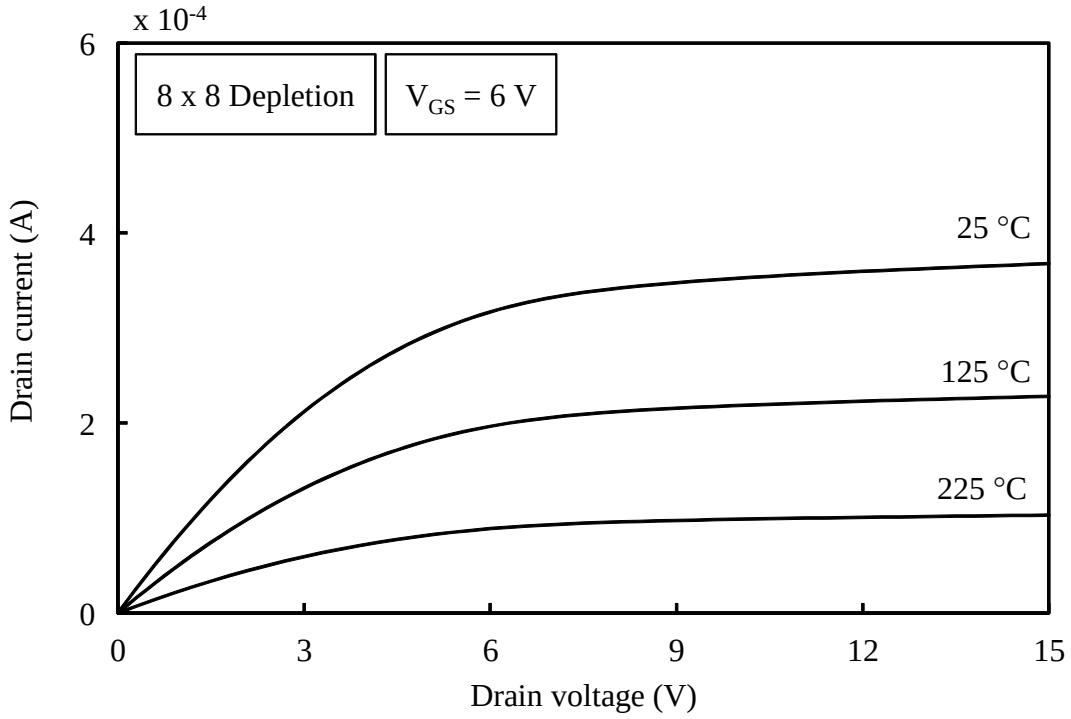


Fig. 3.40: $I_D - V_{DS}$ characteristics of $8\mu m \times 8\mu m$ depletion MOSFET over temperature

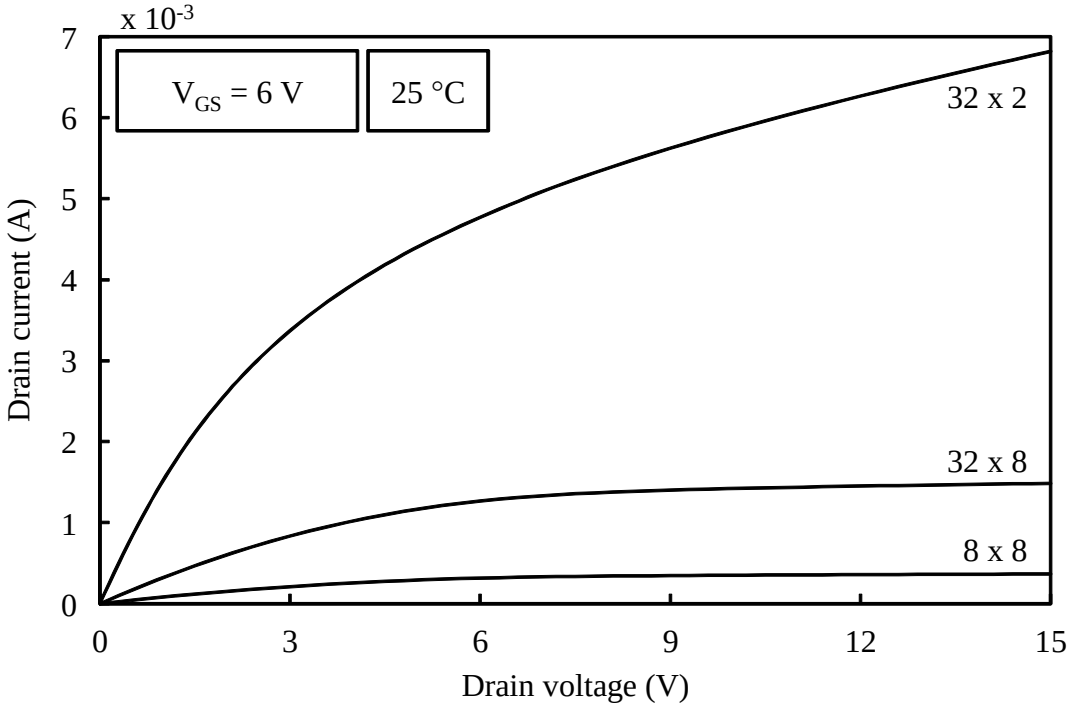


Fig. 3.41: Comparison of $I_D - V_{DS}$ characteristics ($V_{GS} = 6\ V$) of $32\mu m \times 8\mu m$, $32\mu m \times 2\mu m$ and $8\mu m \times 8\mu m$ depletion MOSFETs at 25 °C

3.5 Enhancement MOSFET Characterization

The characterization of enhancement MOSFETs was carried out using the same equipment and procedure as described in Section 3.4.

3.5.1 Gate Capacitance

The characterization of gate-capacitance for enhancement MOSFETs was done in the same way as for depletion MOSFETs as described in Section 3.5.1. Fig. 3.42 shows the scaled $C_{GG} - V_G$ characteristics of a $32\mu m \times 8\mu m$ enhancement MOSFET at a frequency of 10 kHz and 1MHz. The source, drain and body were tied to ground, and the gate-bias was swept from -15 V to 15 V with a sweep rate of 0.1 V/s. The actual measurement was taken on a much larger $20 \times 50\mu m \times 50\mu m$ C-V structure as shown in Fig. 3.4 and then scaled down for the corresponding device area. The $C_{GG} - V_G$ characteristics of the enhancement MOSFET exhibit a peculiar "hook and ledge" characteristics, which arise due to the presence of a large density of interface states in the device [52]. The explanation of the peculiar characteristics is attributed to the large density of interface states present in SiC MOSFETs. In fact, the behavior seen in Fig. 3.42 can be used to characterize the number of interface states on the surface. The next section describes the characterization of interface states and provides an explanation of the physical mechanisms responsible for the $C_{GG} - V_G$ characteristics of the enhancement MOSFET.

3.5.2 Interface States

Several methods to characterize the interface trap distribution have been proposed. Hofmann et al. [53] have demonstrated the characterization of interface traps using a gate charge-pump technique

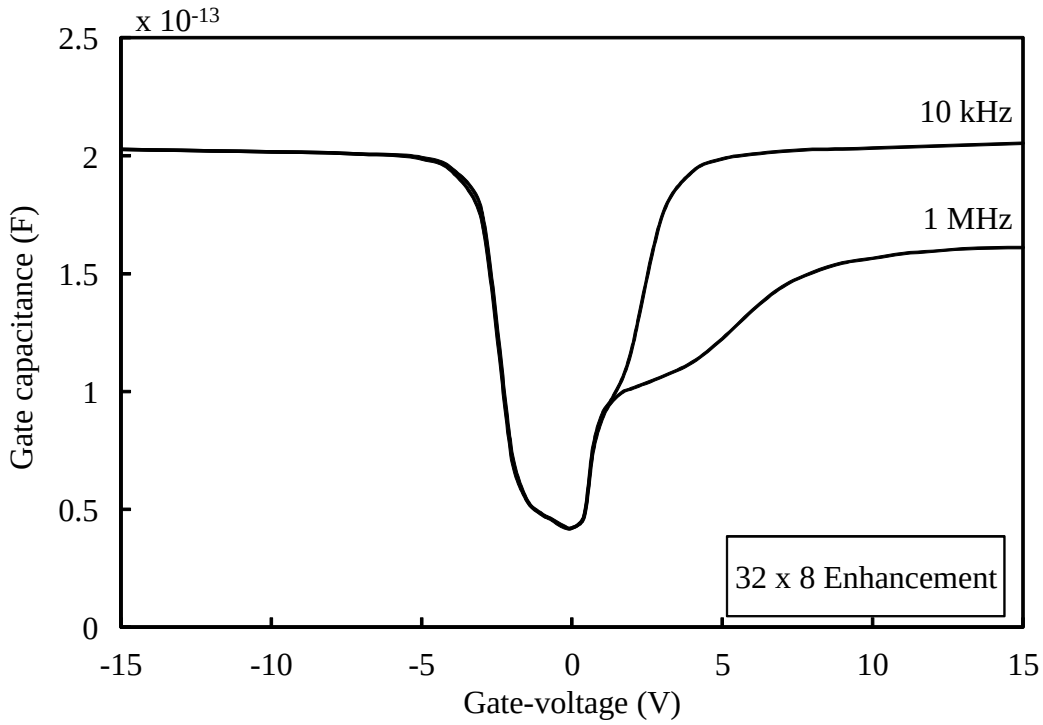


Fig. 3.42: Scaled $C_{GG} - V_G$ characteristics of a $32\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

for geometry-scaled MOSFETs from different technologies. Terman et al. [54] reported a method to extract interface trap density profile D_{it} by comparison of measured high frequency (HF) C-V curves to ideal calculated HF curves. Berglund et al. [55] demonstrated a method to extract D_{it} using a comparison of measured low frequency (LF) C-V and ideal LF C-V curves. Both the HF and LF C-V methods require the calculation of the ideal C-V curves and are not attractive. Castagne et al. [56] presented a method based on comparison of LF and HF measured C-V curves to extract D_{it}. The advantage of this method is that no comparison to ideal curves is required, and D_{it} can easily be obtained using two measurements.

However, C-V methods based on the MOS capacitor rely on the equilibrium of thermally generated carriers with the interface traps. Due to the large band-gap of SiC, the minority carrier thermal generation rate is slow, and an equilibrium of the minority carriers with interface traps cannot be

attained during bias sweeps. Thus, a deep depletion characteristic is seen when characterizing SiC MOS capacitors in the dark [57], [58].

To tackle this problem, MOS gated-diodes or MOSFETs connected as gated diodes are used instead of MOS capacitor structures. In MOSFETs connected as gated diodes, the source and drains are tied together, and kept at zero or a small reverse bias with respect to the substrate. In the inversion region, the source and drain diffusion regions provide the minority carriers in the inversion channel. Due to an abundant source of minority carriers from the source/drain regions, MOSFETs connected as gated diodes are more suitable to extract interface state densities using C-V methods.

Sheppard et al. [59] demonstrated a C-V based method using MOS gated-diodes to characterize the density of interface states in inversion-channel and buried-channel 6H-SiC MOS devices. Saks et al. [60] showed a Hall-effect based method to characterize the density of interface states. It has also been reported that the Hall-effect based method is more accurate than the C-V method to characterize trap densities close to the conduction band edge in SiC [61]. However, the Hall-effect based method requires fabrication of special test structures, and Hall-effect characterizing equipment, which is not always available. The C-V based method to determine trap density in the 4H-SiC samples has been used in this work, since C-V data was readily available for a wide variety of bias conditions.

Fig. 3.43 shows the measured $C_{GG} - V_G$ of a $32\mu m \times 8\mu m$ inversion-channel enhancement MOSFET with several regions of interest. The "hook and ledge" characteristic was first reported by Goetzberger et al. for silicon MOS devices at 77K [52], and has been reported for 6H-SiC MOSFETs by Sheppard et al. [59]. The $C_{GG} - V_G$ characteristics can be explained as follows. At point A in Fig. 3.43, it is assumed that the interface states at the surface are in equilibrium with

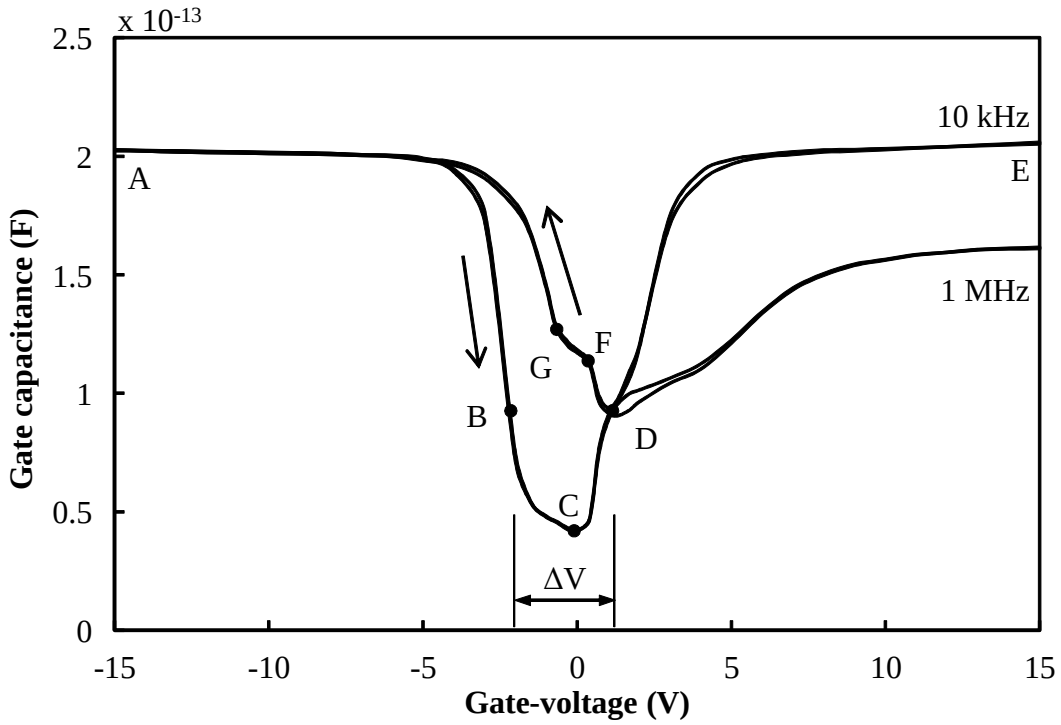


Fig. 3.43: $C_{GG} - V_G$ of a $32\mu m \times 8\mu m$ inversion-channel enhancement MOSFET. Bias sweep rate is 0.1 V/s

the Fermi level and are filled with holes. As the gate bias is increased, the empty states start falling below the bulk Fermi level and the depletion region begins to form. Since minority carriers are absent in the depletion region, electron capture in the empty states is not possible. Only the states near the valence band edge equilibriate via hole emission to the valence band and vice versa. The rest of the states below the Fermi level but away from E_V remain empty.

At point B, the semiconductor surface reaches strong inversion, but due to the barrier that exists for the electrons at the n^+p junction of source/drain diffusion, electrons adjacent to the n^+p junction remain trapped in surface states, causing a decrease in the surface potential near the junctions. As a result, the inversion layer in the center of the channel region is not able to connect to the source/drain diffusion region, and the center region goes into deep depletion. The deep depletion occurs as the bias is moved from B to C. As point C is reached, the surface states in

the barrier region get completely filled and the barrier region is able to invert, connecting the n^+ diffusion with the region under the gate. As the bias moves from C to D, strong inversion occurs everywhere under the gate and the measured capacitance ramps up. The region between B and D is referred to as the "hook" region of the characteristics.

The frequency dependence of inversion region can be seen from the region between D and E and is attributed to the resistance of the channel region and the induced RC delay. An approximate total number of surface states can be calculated by measuring the shift in voltage from B to D, ΔV as

$$N_{IT} = \frac{\Delta V C_{ox}}{q} \tag{3.2}$$

For the $C_{GG} - V_G$ curve shown in Fig. 3.43 and using (3.2), N_{IT} is estimated to be 1.7×10^{12} cm^{-2}. As the bias moves from point D to E, the low-frequency behavior of the C-V curve is seen, because the n^+ diffusion is connected to the inversion layer and supplies the minority carriers needed to follow the AC signal.

In the reverse sweep from E to D, the "ledge" characteristics of the C-V curve can be seen. At point E, the channel region is in strong inversion. As the bias moves towards D, the charge from the corners of the inversion region near the n^+ diffusion is removed quickly, but the surface remains in equilibrium. At D, depletion starts and the band-bending starts reducing towards the flat-band condition. In this region, the occupied trap states also move above the Fermi level, but the electrons in the center region cannot leave the occupied traps and continue to follow the DC sweep. Since the charge occupancy between D and F stays close to the value of D, the voltage shift seen between D and F is constant. At F, the surface hole concentration becomes sufficient and the trapped electrons begin to combine with the holes by hole capture. Beyond point G, there is a

voltage shift which suggests charge trapping in the oxide.

3.5.3 Mobile Ion Contamination

During the characterization of enhancement MOSFETs, it was found that input characteristics of some of the devices shifted after repeated measurements. In addition, the shift was pronounced at elevated temperatures. For example, Fig. 3.44 shows the $I_D - V_{GS}$ characteristics ($V_{BS} = 0\ V$) of a $32\mu m \times 2\mu m$ enhancement MOSFET; first measurement taken on a fresh device and the second measurement taken after other measurements were performed on the same device. It can be seen that the threshold voltage of the device reduced drastically when characterized the second time. In order to characterize the amount of shift, the same sample was measured repeatedly with few dummy measurements in between, but it was found that the shift was permanent and fixed in magnitude for every case. Such behavior has been attributed to the presence of mobile alkali ion contaminants (MAIC) in the gate-oxide [62].

The introduction of MAIC is due to contamination during processing of the wafer. Several gettering techniques like the use of a top layer of Phosphosilicate Glass (PSG) [63]-[66] or a cap-layer of Si_3N_4 have been proposed to trap the mobile ions on the top of the oxide surface away from the interface, thereby minimizing there effects on the device characteristics. After the discovery of MAIC in the enhancement devices, Cree has taken steps to ensure that proper gettering methods will be employed for the next round of fabrication, to eliminate the MAIC problem.

Fortunately, several dies of the test-chip on the same wafer type (2AR) were available during characterization. In order to proceed with model development, different measurements were performed only once on a fresh die, so the first measurement could be reliably obtained before MAIC would shift the device characteristics. While it is possible that the characteristics measured the first

time may also be affected by MAIC, each measurement was performed twice on the same device on two different dies and compared to ensure consistency in the device characteristics. For elevated temperature characterization, the same procedure of using a fresh die for each measurement has been ensured, and consistency check tests have been done so that compact models could be generated for circuit design.

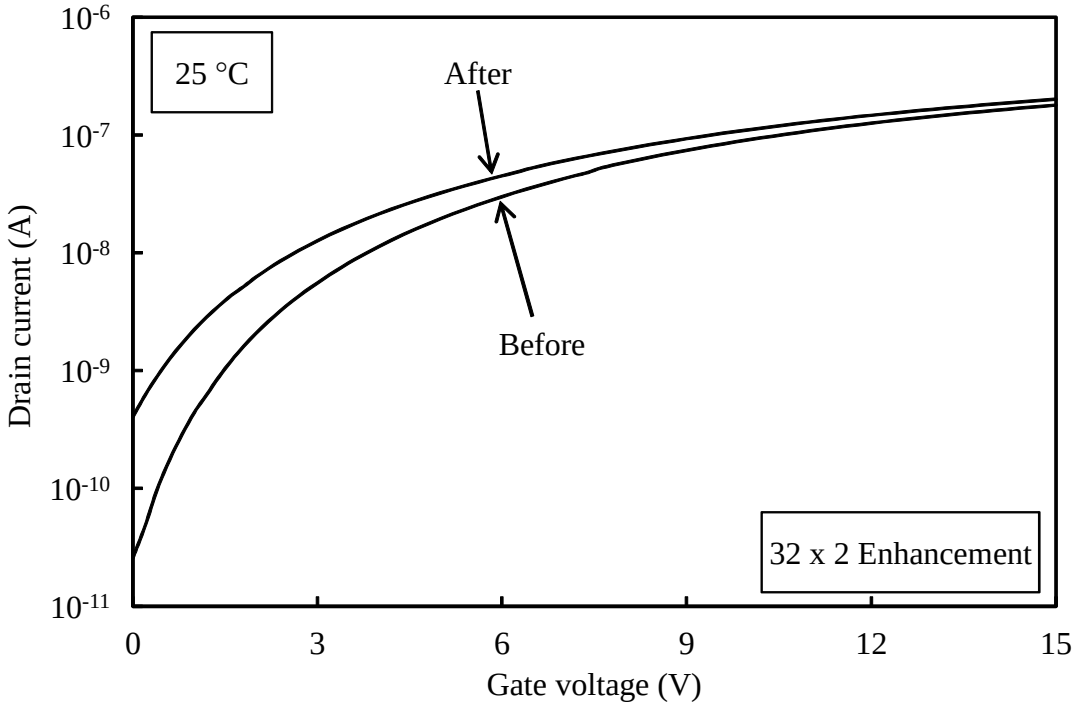


Fig. 3.44: Change in the $I_D - V_{GS}$ characteristics of a $32\mu m \times 2\mu m$ enhancement MOSFET, on a fresh device (Before) and after some electrical measurements (After) at 25 °C

3.5.4 Input Characteristics

For the input characteristics $I_D - V_{GS}$, gate voltage V_{GS} was swept from -6 V to 15 V, drain voltage V_{DS} was held constant at 50 mV and bulk voltage V_{BS} was stepped from 0 V to -15 V in 3 V steps. The input characteristics allow the extraction of threshold voltage V_T and mobility reduction parameters at higher gate-biases. Input characteristics were measured for each device at 25 °C,

125 °C and 225 °C. During characterization, a large amount of leakage current was observed in three samples of the $32\mu m \times 8\mu m$ enhancement device. As a result, the largest enhancement device for geometry scaling has been chosen to be the $16\mu m \times 8\mu m$ device instead. In order to use the $32\mu m \times 8\mu m$ MOSFET in the design, two $16\mu m \times 8\mu m$ MOSFETs have been used in parallel, both in layout and schematic.

From the device array, the device sizes were chosen as follows:

- Largest Device (W/L = 2): $16\mu m \times 8\mu m$
- Widest Device (W/L = 16): $32\mu m \times 2\mu m$
- Narrowest Device (W/L = 1): $8\mu m \times 8\mu m$

Figs. 3.45, 3.46 and 3.47 show the $I_D - V_{GS}$ characteristics of the $16\mu m \times 8\mu m$, $32\mu m \times 2\mu m$ and $8\mu m \times 8\mu m$ enhancement MOSFETs at 25 °C respectively. It can be observed that being surface-channel devices, the current flows in the inversion channel on the surface and as a result, the input characteristics are heavily dominated by the high density of interface states which cause Coulumbic scattering. The effect is predominantly seen in the weak and moderate inversion regions, where the devices show a gradual transition from weak/moderate to strong inversion unlike the depletion MOSFETs. At higher gate-biases, effects of surface roughness scattering is also predominant. It will be shown later how the presence of a large number of interface states affect the performance of the surface-channel enhancement MOSFETs. Figs. 3.48, 3.49 and 3.50 show the $g_m - V_{GS}$ characteristics of the same devices at room temperature.

Fig. 3.51 compares the $I_D - V_{GS}$ characteristics of the three devices for zero back bias condition. It can be seen that the $32\mu m \times 2\mu m$ device shows a smaller threshold voltage V_T due to normal short channel effect, but both the $8\mu m$ length devices have the same threshold voltage.

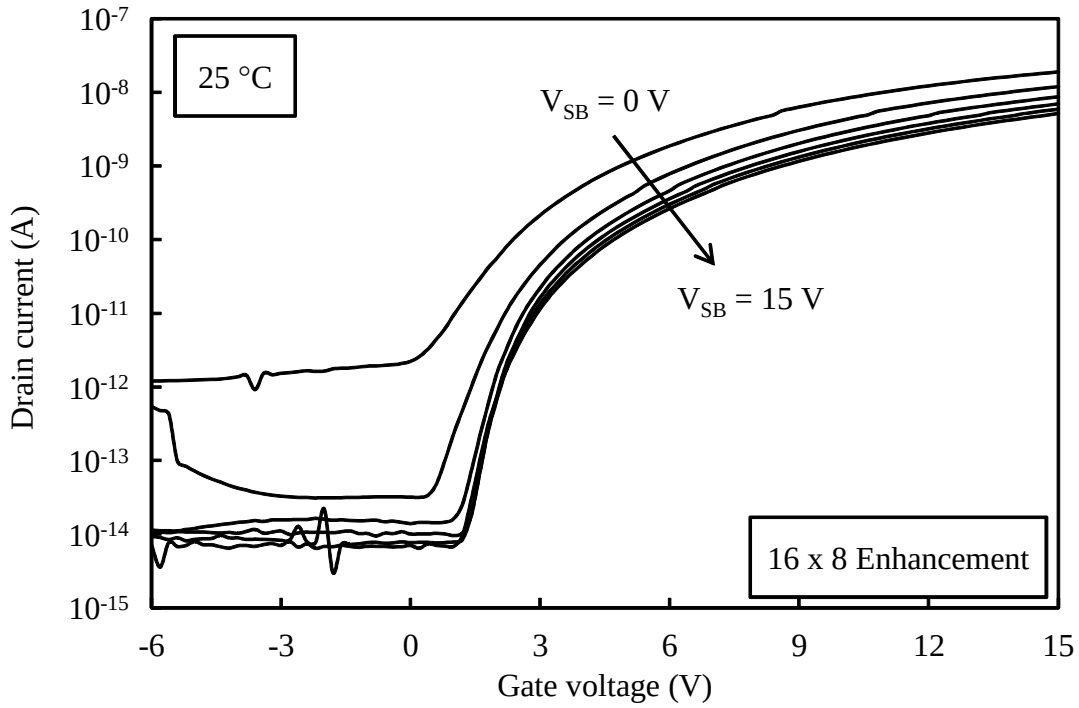


Fig. 3.45: $I_D - V_{GS}$ characteristics of $16\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

The variation of the $I_D - V_{GS}$ characteristics of the $16\mu m \times 8\mu m$, $32\mu m \times 2\mu m$ and $8\mu m \times 8\mu m$ enhancement MOSFETs with temperature is shown in Figs. 3.52, 3.53 and 3.54 respectively. It can be seen that the threshold voltage decreases linearly with temperature as expected.

3.5.5 Output Characteristics

The measurement of output characteristics $I_D - V_{DS}$ was done by sweeping drain voltage V_{DS} from 0 V to 15 V, stepping gate voltage V_{GS} from -9 V to 15 V in 3 V steps and keeping bulk voltage V_{BS} constant at 0 V. The output characteristics of $16\mu m \times 8\mu m$, $32\mu m \times 2\mu m$ and $8\mu m \times 8\mu m$ enhancement MOSFETs at room temperature are shown in Figs. 3.55, 3.56 and 3.57 respectively. The $g_{DS} - V_{DS}$ characteristics for the same devices are shown in Figs. 3.58, 3.59 and 3.60 respectively.

The comparison between the $I_D - V_{DS}$ characteristics of the three device sizes for $V_{GS} = 15V$ is shown in Fig. 3.64. Fig. 3.56 highlights the channel length modulation effect in the shorter

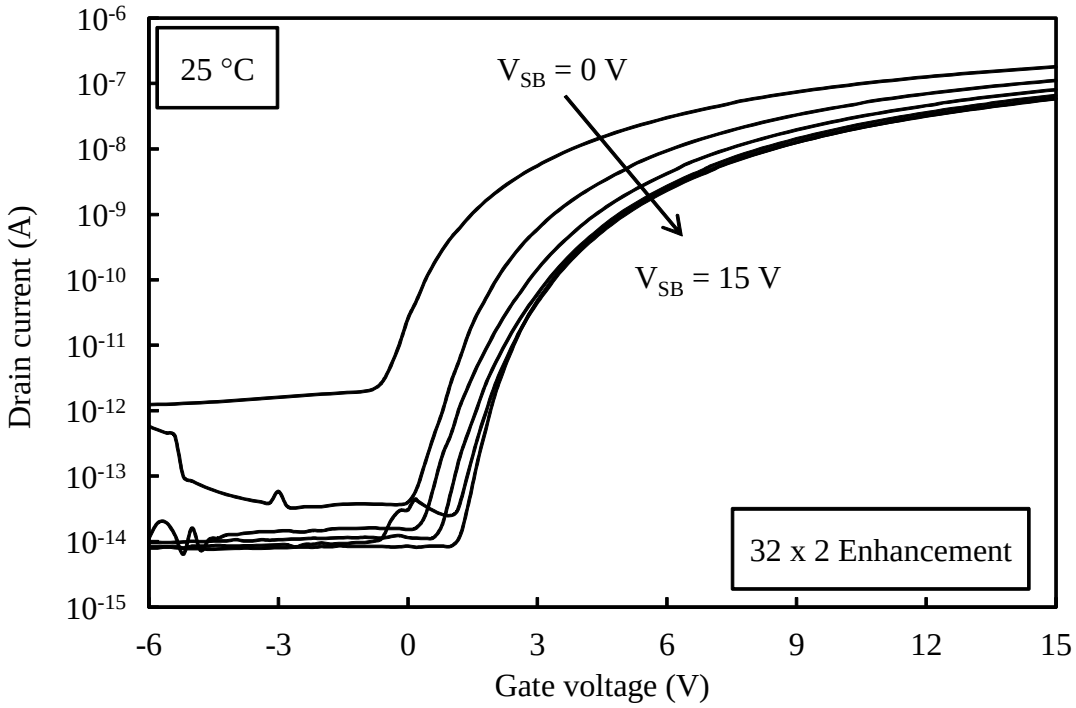


Fig. 3.46: $I_D - V_{GS}$ characteristics of $32\mu m \times 2\mu m$ enhancement MOSFET at 25 °C

$32\mu m \times 2\mu m$ device. The longer devices have a relatively flat saturation region, and are more suitable for applications requiring a high output resistance. The shorter device is more suitable as a pull-up or pull-down transistor due to much larger current for a given gate-voltage.

The $I_D - V_{DS}$ characteristics of the three device sizes for $V_{GS} = 15V$ at 25 °C, 125 °C and 225 °C is shown in Figs. 3.61, 3.62 and 3.63 respectively. The large signal on-state resistance is simply given by

$$R_{ON} = \frac{V_{DS}}{I_D} \tag{3.3}$$

for any given V_{GS}. Thus, it can be seen from Figs. 3.61, 3.62 and 3.63 that for a fixed V_{GS} and V_{GS}, I_D increases with temperature for each device. This implies that the on-state resistance of the enhancement MOSFETs *reduces* with temperature, which is opposite to what is found for Si MOSFETs. The reduction of resistance is most prominent in sub-threshold region, where Coulumbic

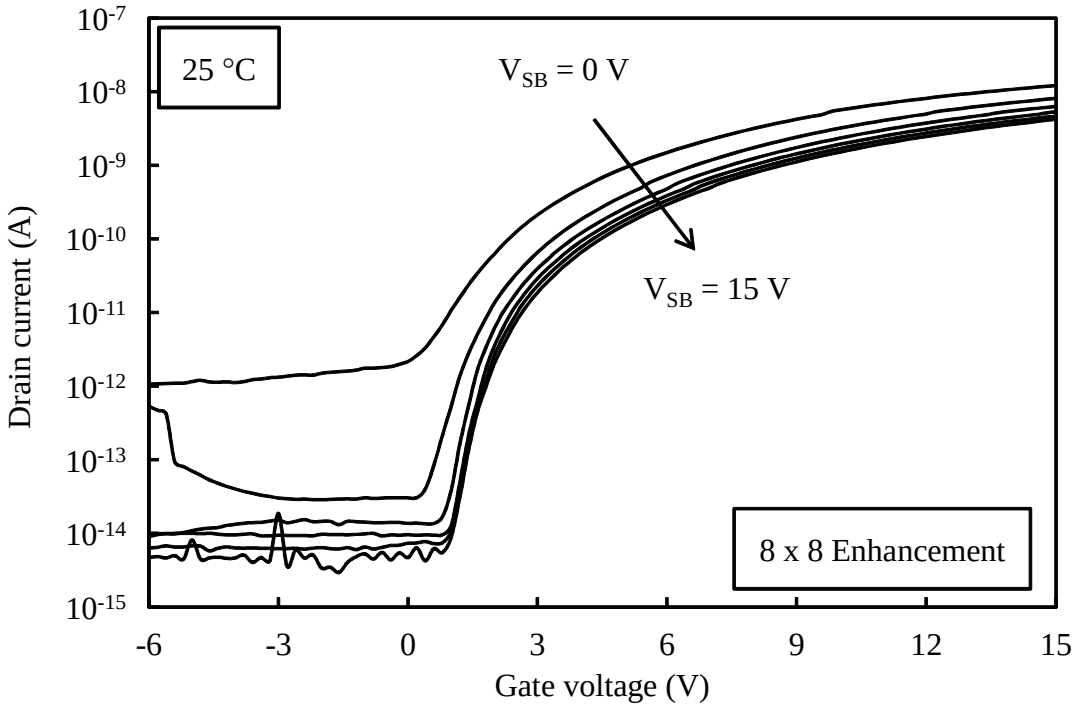


Fig. 3.47: $I_D - V_{GS}$ characteristics of $8\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

scattering is dominant. At higher gate-biases, surface scattering becomes the dominant limiting effect for surface mobility [67]. The main reason for the opposite behavior of the on-state resistance is because as the temperature increases, the electrons in the channel have more thermal energy to overcome Coulumbic scattering effects. Thus, while phonon scattering in the channel increases with temperature as in the case of Si MOSFETs, Coulumbic scattering is suppressed and the overall effect is a modest improvement in channel mobility with temperature, which is seen by the rise in current with temperature.

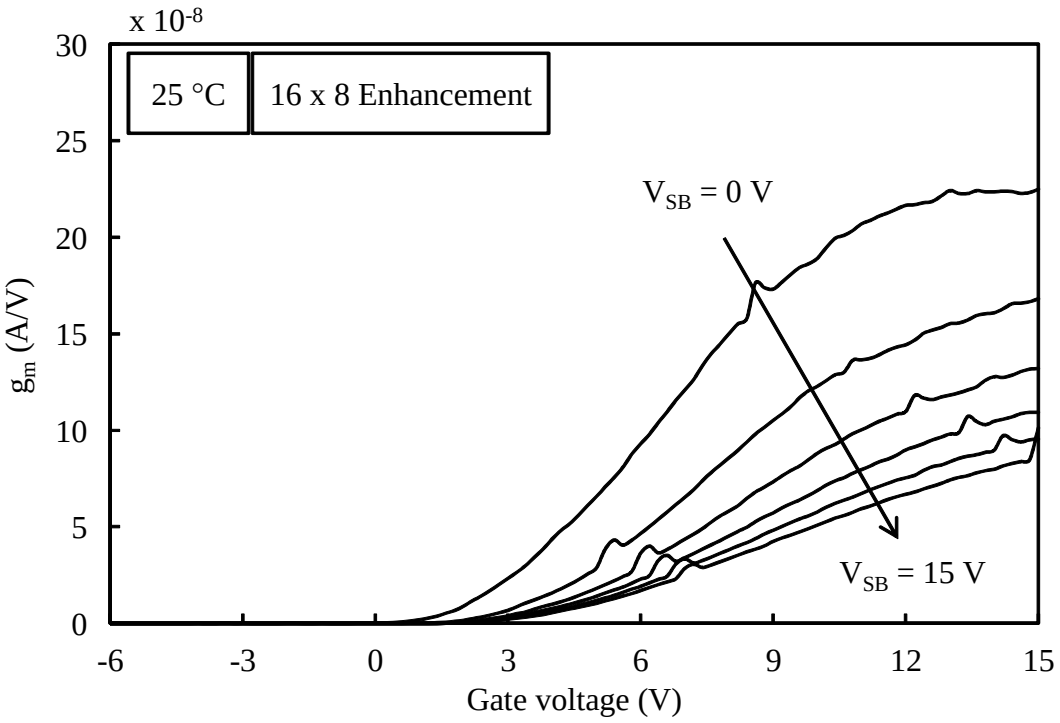


Fig. 3.48: $g_m - V_{GS}$ characteristics of $16\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

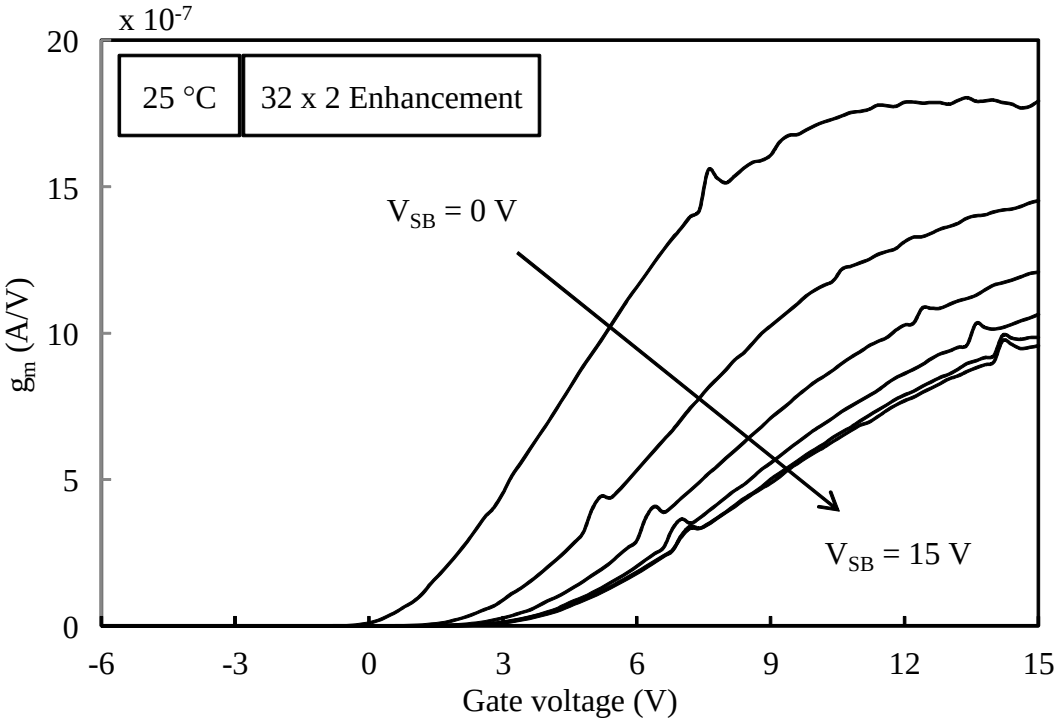


Fig. 3.49: $g_m - V_{GS}$ characteristics of $32\mu m \times 2\mu m$ enhancement MOSFET at 25 °C

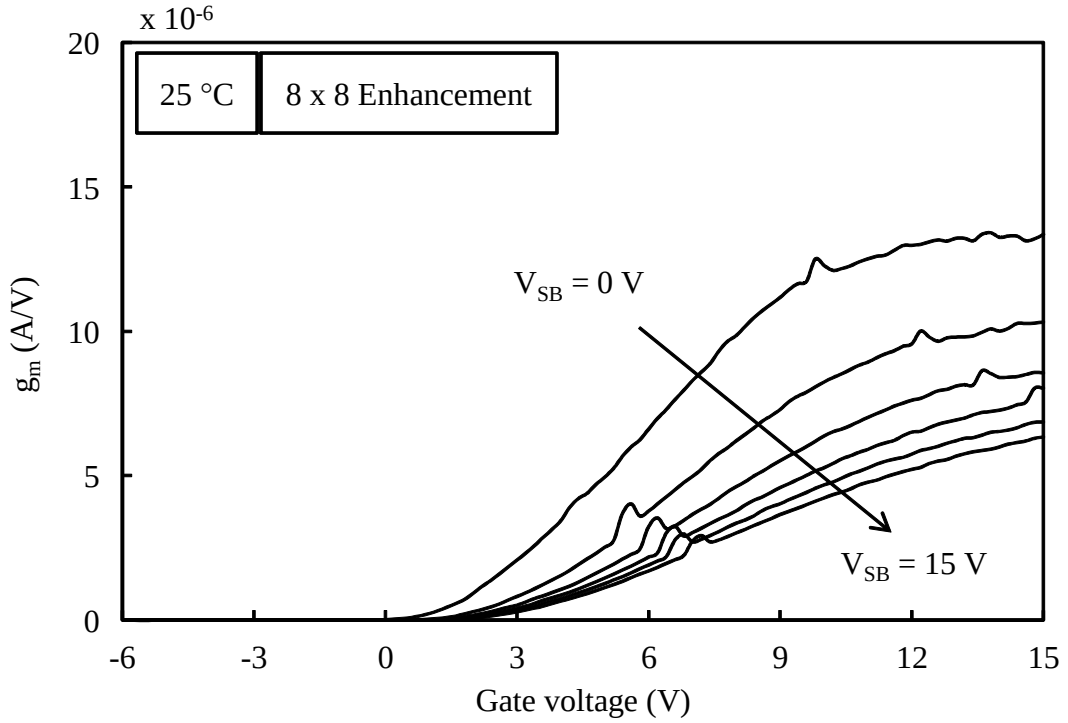


Fig. 3.50: $g_m - V_{GS}$ characteristics of $8\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

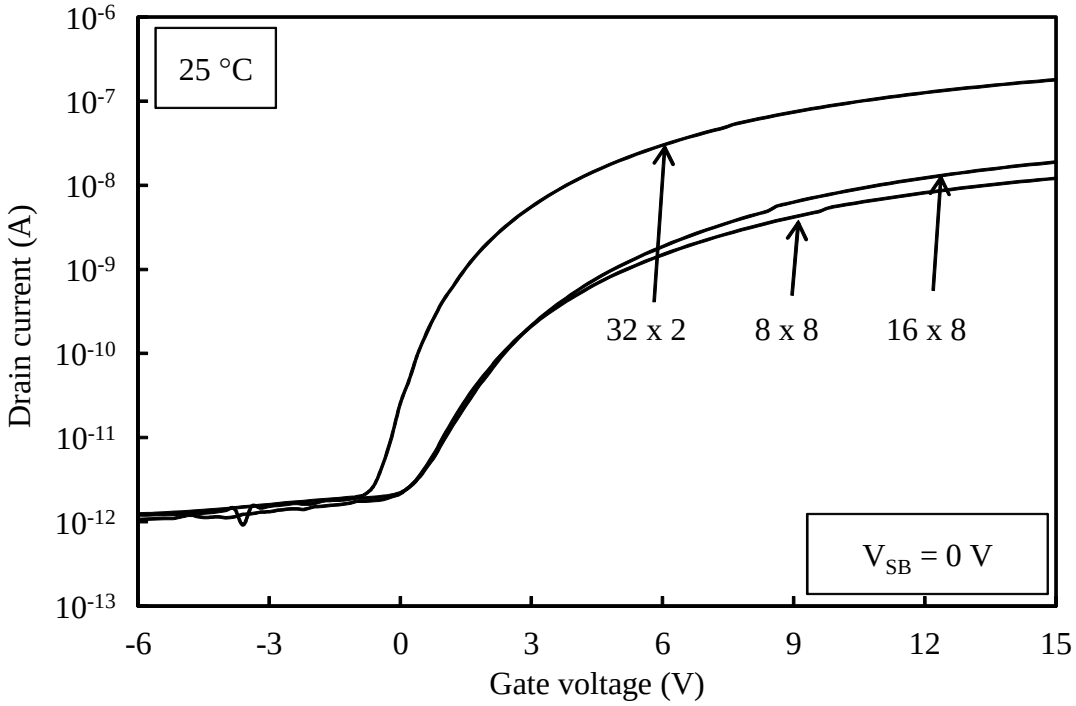


Fig. 3.51: Comparison of $I_D - V_{GS}$ characteristics ($V_{SB} = 0\ V$) of $16\mu m \times 8\mu m$, $32\mu m \times 2\mu m$ and $8\mu m \times 8\mu m$ enhancement MOSFETs at 25 °C

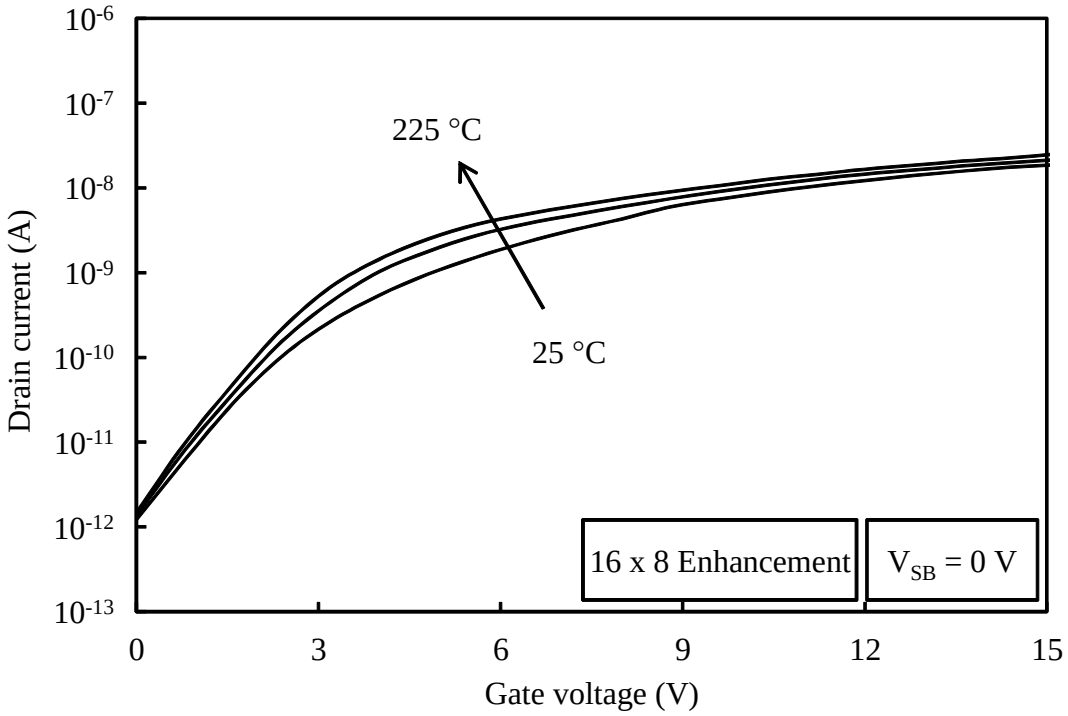


Fig. 3.52: $I_D - V_{GS}$ characteristics of $16\mu m \times 8\mu m$ enhancement MOSFET at 25 °C, 125 °C and 225 °C

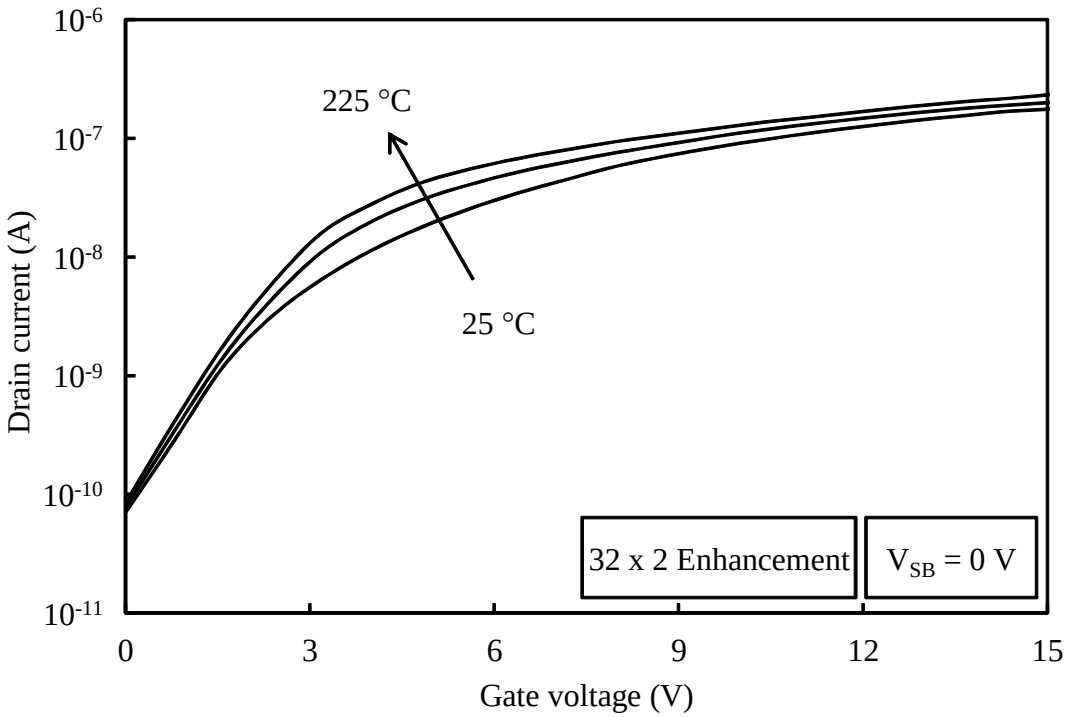


Fig. 3.53: $I_D - V_{GS}$ characteristics of $32\mu m \times 2\mu m$ enhancement MOSFET at 25 °C, 125 °C and 225 °C

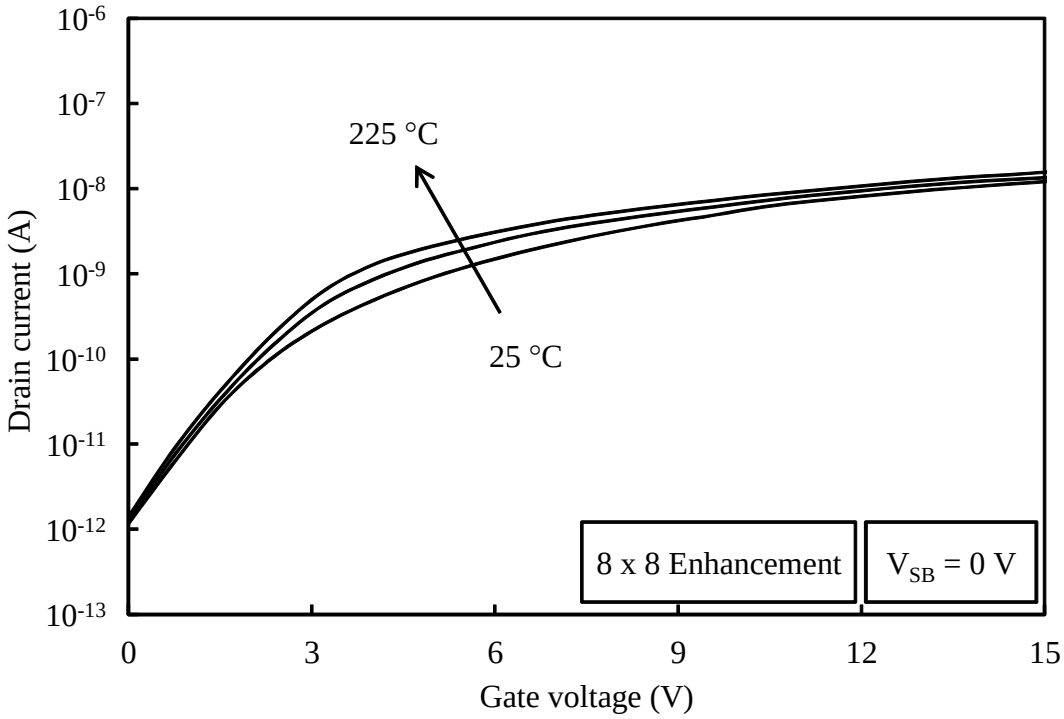


Fig. 3.54: $I_D - V_{GS}$ characteristics of $8\mu m \times 8\mu m$ enhancement MOSFET at 25 °C, 125 °C and 225 °C

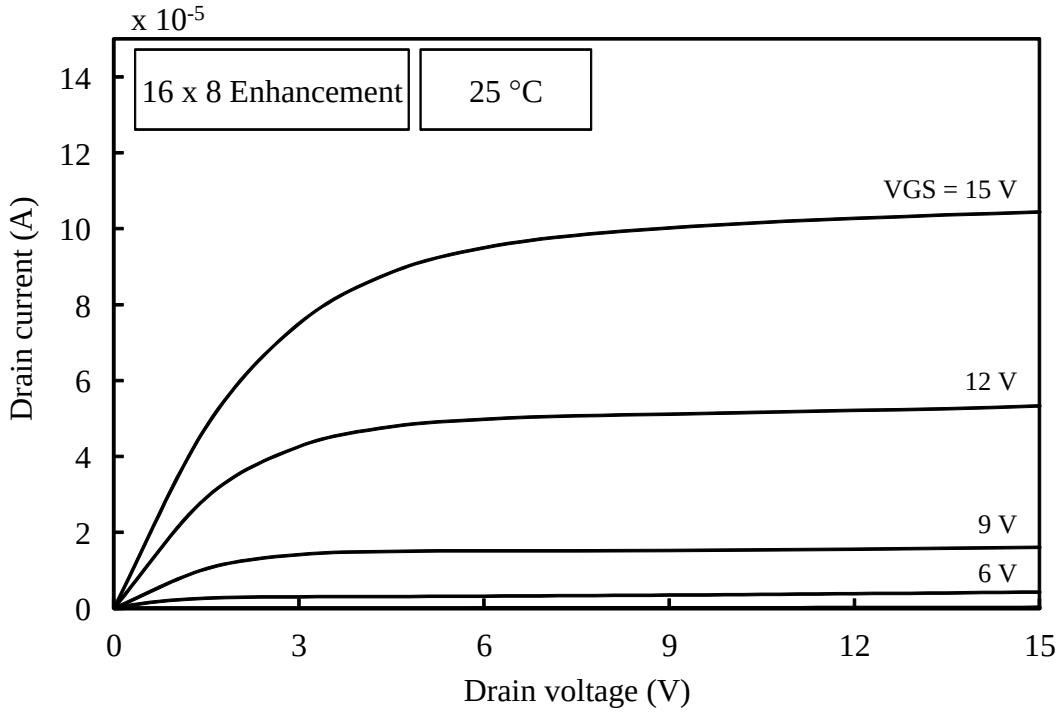


Fig. 3.55: $I_D - V_{DS}$ characteristics of $16\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

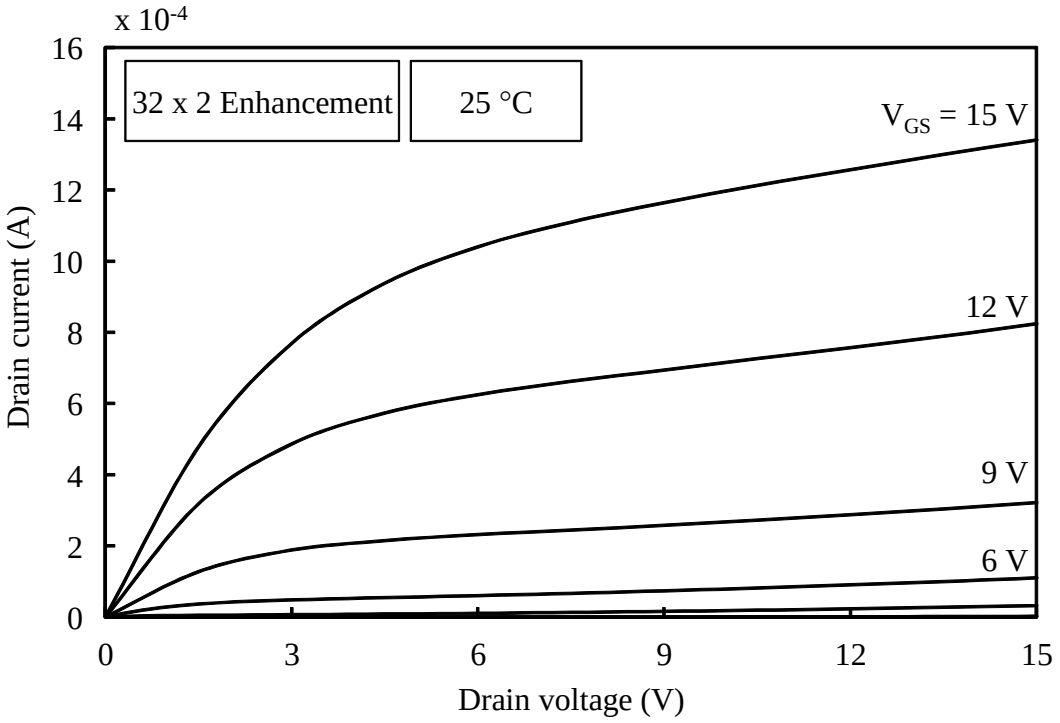


Fig. 3.56: $I_D - V_{DS}$ characteristics of $32\mu m \times 2\mu m$ enhancement MOSFET at 25 °C

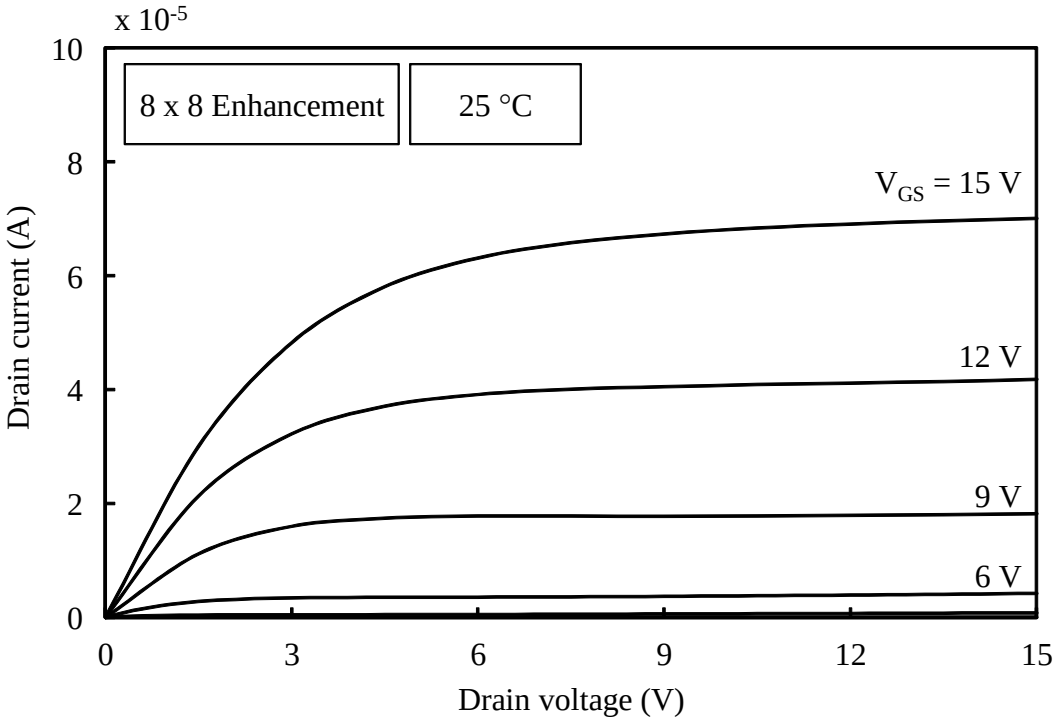


Fig. 3.57: $I_D - V_{DS}$ characteristics of $8\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

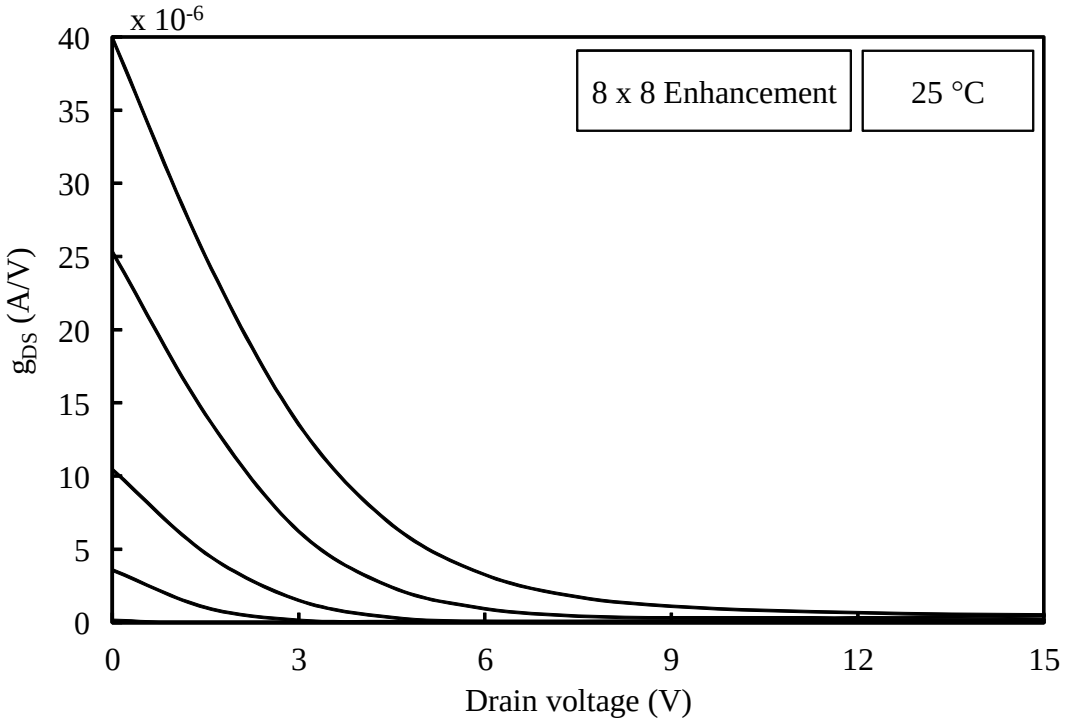


Fig. 3.58: $g_{DS} - V_{DS}$ characteristics of $16\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

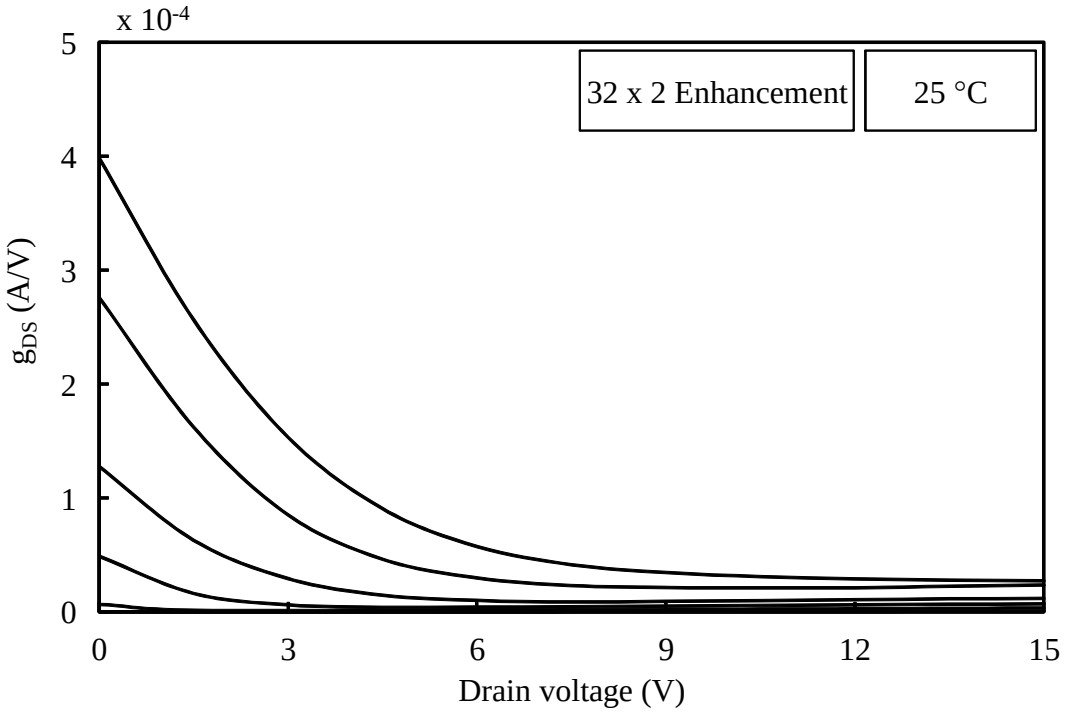


Fig. 3.59: $g_{DS} - V_{DS}$ characteristics of $32\mu m \times 2\mu m$ enhancement MOSFET at 25 °C

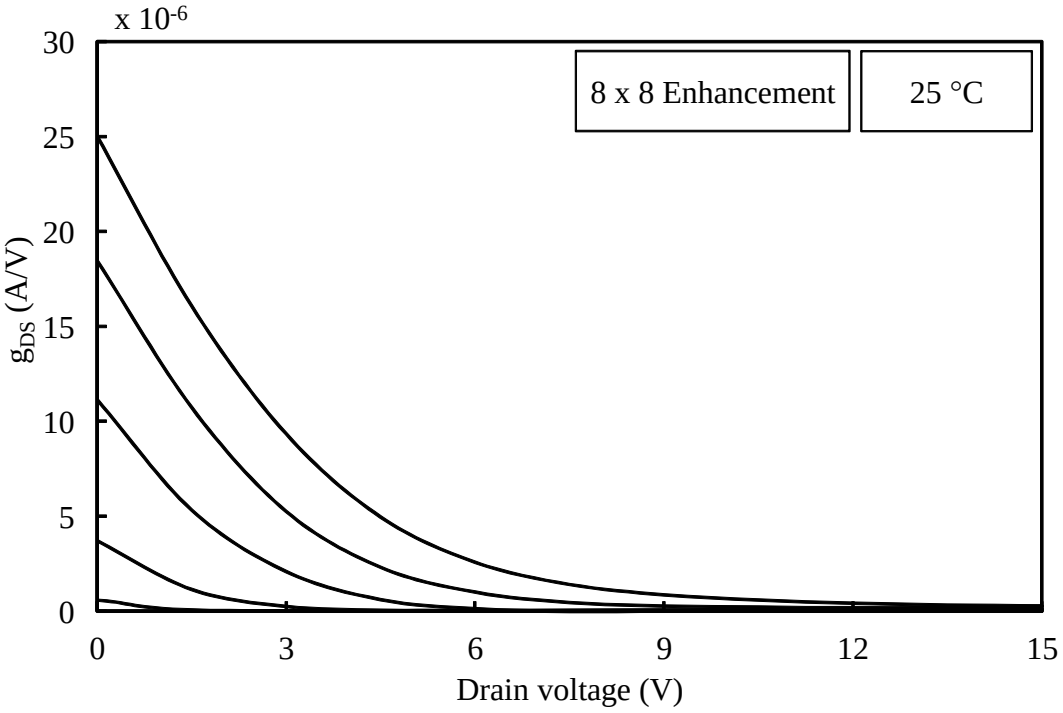


Fig. 3.60: $g_{DS} - V_{DS}$ characteristics of $8\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

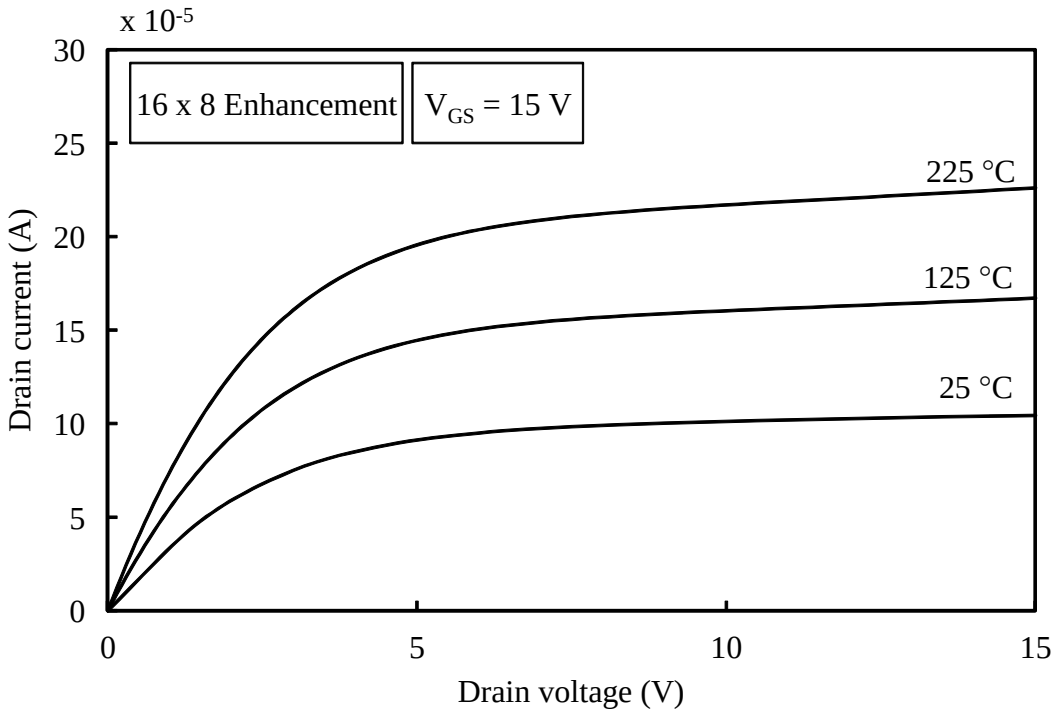


Fig. 3.61: $I_D - V_{DS}$ characteristics of $16\mu m \times 8\mu m$ enhancement MOSFET over temperature

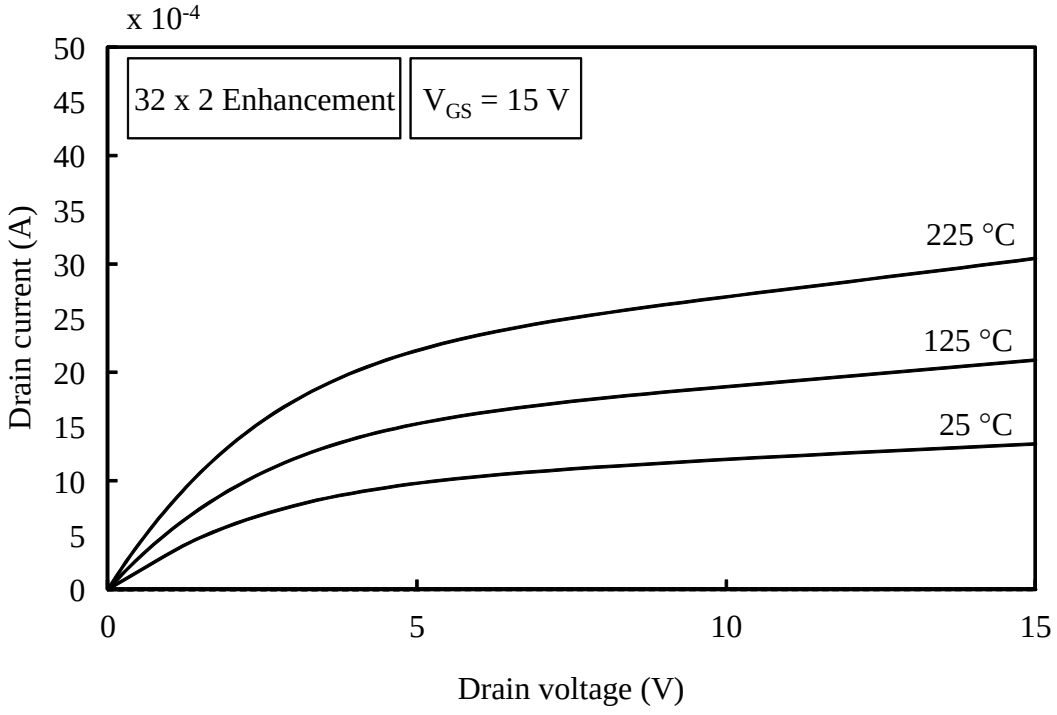


Fig. 3.62: $I_D - V_{DS}$ characteristics of $32\mu m \times 2\mu m$ enhancement MOSFET over temperature

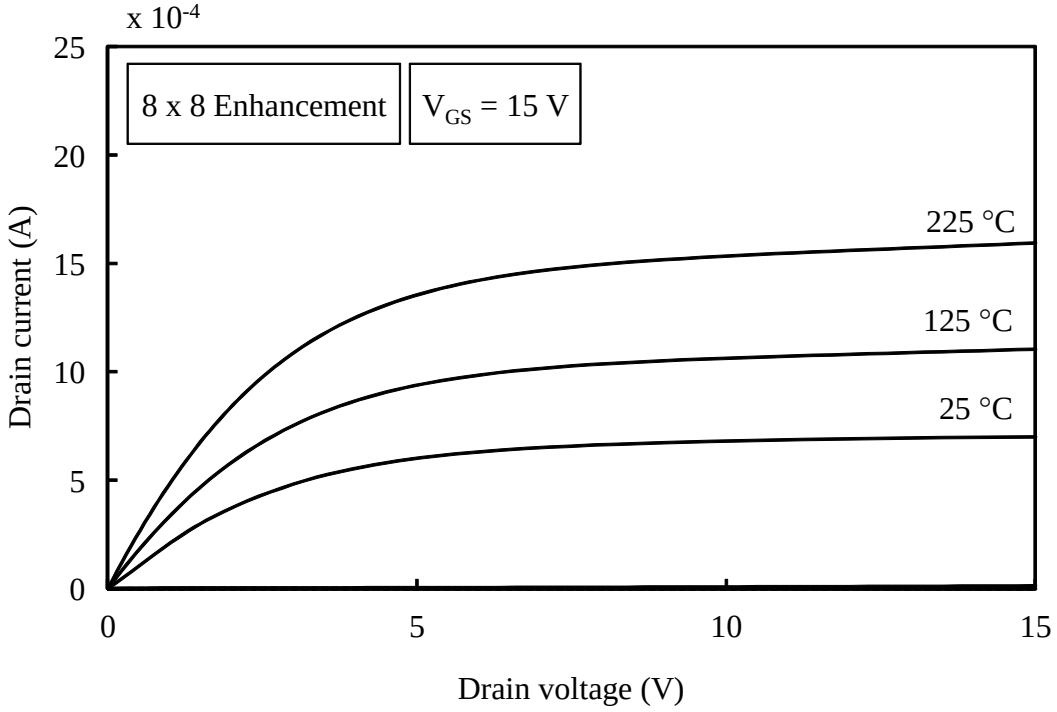


Fig. 3.63: $I_D - V_{DS}$ characteristics of $8\mu m \times 8\mu m$ enhancement MOSFET over temperature

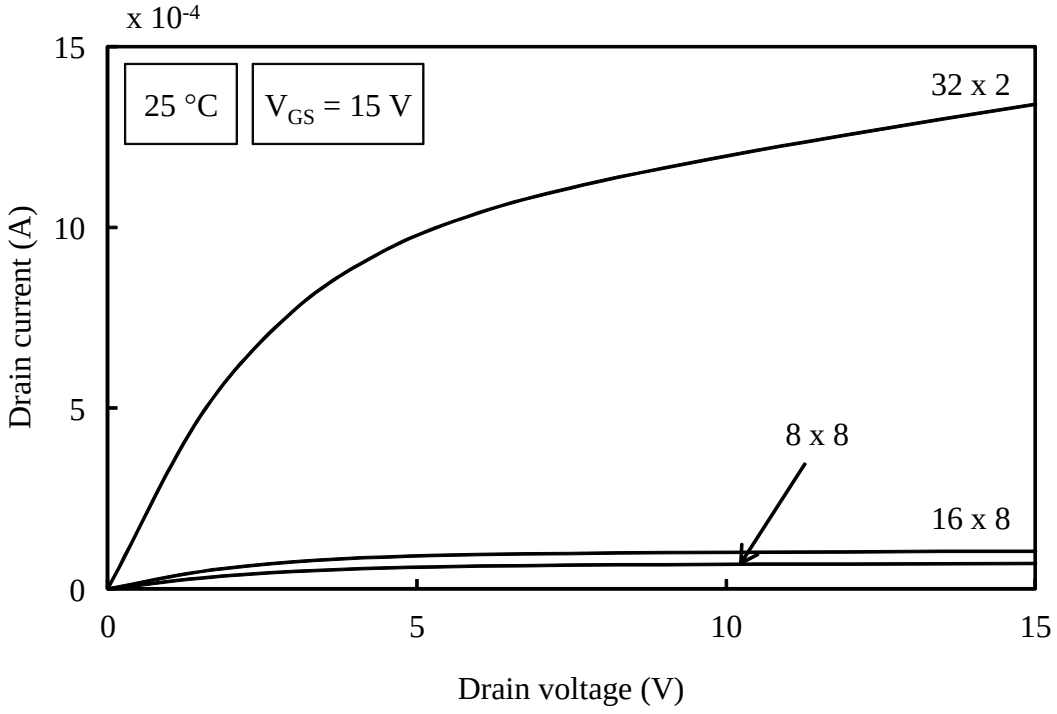


Fig. 3.64: Comparison of $I_D - V_{DS}$ characteristics ($V_{GS} = 15\ V$) of $16\mu m \times 8\mu m$, $32\mu m \times 2\mu m$ and $8\mu m \times 8\mu m$ enhancement MOSFETs at 25 °C

Chapter 4

SiC PSP Model

MOSFET technology has evolved at a tremendous pace in the last four decades, since the invention of the first planar MOSFET. A new technology node is developed almost every two years, following the prediction of Moore's law that the number of transistors are doubled approximately every two years [68]. With the shrinking of device sizes, new effects are being observed in smaller devices that were invisible a decade ago.

In order to enable the development of circuits with rapidly changing MOSFET technology, compact models for MOSFETs need to match strides with the evolving device technology. There are several MOSFET models available on a variety of simulator platforms. In an effort to standardize compact models from different sources, several members from the industry and academia formed the Compact Model Council (CMC) in 1996 [69]. The CMC maintains and supports the official industry standard models for different device families. The models supported by CMC are widely used and included by most of the circuit simulator vendors on all platforms.

The two most widely used MOSFET models are the Berkeley Short-Channel IGFET Model (BSIM) from University of California, Berkeley [70] and the PSP model from Arizona State University and NXP Semiconductor Research [1]. BSIM model is available in numerous versions, and BSIM3v3 model [71] was chosen by CMC as the industry standard model between 1996-1999. BSIM3v3 was subsequently replaced by BSIM4 [40] in 2000, and BSIM4 continued to be the industry standard model until 2006, when it was replaced by the PSP model.

A MOSFET is a 2-Dimensional device by definition, where the input on the gate is applied in a

direction perpendicular to the semiconductor surface, which modulates the current flow parallel to the semiconductor surface. The 2-D operation of the MOSFET must be decomposed into two 1-D problems in order to formulate a compact model for the MOSFET. The Pao-Sah double integral formula [72] provides a solution of the 2-D problem. The presence of the double integral in the formula makes the evaluation possible only by numerical methods and is unsuitable for compact models. However, the formulation is very physical and is still used to date as a reference for accuracy of other methods. Based on the Pao-Sah formula, charge-sheet approximation methods [73], [74], [75] were developed which treat the inversion layer charge as a 2-D sheet of zero thickness. Despite the elimination of the double integral from the Pao-Sah formula, the charge sheet approximations still provide an implicit solution of the surface potential as a function of the terminal voltages. When these models were proposed, due to limitations of computing power, the charge sheet methods could not be used in compact models.

Further simplifications were made to the surface-potential equation. The earliest MOSFET compact models were threshold voltage based (V_T-based), where surface potential was defined as a function of the gate-voltage. In V_T-based models, when gate voltage is greater than V_T, surface potential is treated as constant. For gate voltages less than V_T, the surface potential is a linear function of the gate-voltage. Thus the on-state characteristics of the MOSFET is divided into piece-wise linear regions, and smoothing functions were implemented by the compact model to overcome convergence problems in the simulator.

V_T-based models have come a long way from this simple description. The BSIM family of compact models for MOSFETs are V_T-based and have been tremendously successful in the industry. The earliest version of BSIM1 was released in 1972 and it was available with the free distribution of SPICE simulator which led to the widespread adoption of the model. The model formulation

was highly empirical in order to improve convergence, but its accuracy degraded as the device technology moved to sub-micron channel lengths. In addition, the description of main current in the original BSIM1 model was divided into several regions of operation, leading to discontinuities in higher order derivatives which caused convergence problems in larger simulations.

BSIM2 was released in 1990 to address the convergence problems of BSIM1 and to make the model more suitable for analog circuit design. However, the main current description was still divided into regions, which would often result in non-convergence. Eventually, BSIM3 was released which incorporated several smoothing functions to join the different operating regions of the device into a single equation. This improved the convergence performance of the model in both DC and CV simulations. BSIM3 has evolved into three versions: BSIM3v1, BSIM3v2 and BSIM3v3. The first two versions had a lot of mathematical problems and BSIM3v3 eventually became the de-facto standard. BSIM3v3 has shown excellent performance down to 0.18 μm technologies, and has served the industry well. Considerable effort has been made by the EDA industry to implement BSIM3v3 model code in their proprietary tools, and the model is still widely used today due to the large knowledge-base of users. BSIM4 was released in 2000, and was developed for deep sub-micron technologies and RF applications.

Despite the widespread adoption and popularity of BSIM3v3 and BSIM4, both models are inherently V_T-based and suffer from some limitations. Firstly, in order to maintain symmetry between source and drain (interchanging S and D should not affect performance), third-order derivatives for currents and charges must exist and be continuous [5]. This is difficult to accomplish with V_T-based models due to extensive use of smoothing functions which are not always symmetric. Another problem is the symmetry of capacitances in the model. For example, when V_{DS} is 0, the drain and source capacitances should be symmetrical. However, it has been shown that BSIM4

suffers from problems of non-symmetrical capacitance formulations [76]. Due to the problems with V_T-based modeling of MOSFETs, the industry is gradually moving towards surface-potential based models which are inherently more physical in nature and provide a continuous formulation for the channel current and charges.

In order to develop a low voltage compact model for SiC MOSFETs, PSP model has been chosen as the starting point, and modifications have been made to account for SiC-specific features. There are two main reasons for choosing PSP model over BSIM. Firstly, as described above, PSP model is surface-potential based and is more physical in its formulation than the V_T-based BSIM3v3 and BSIM4 models. PSP model contains all the necessary features required to describe deep sub-micron technologies, and is currently the industry standard model for MOSFETs. As a result, by using PSP model as a starting point, all the improvements introduced by the surface-potential method are automatically included in the SiC model. Additionally, the PSP model code is available in Verilog-A which is a universal Hardware Description Language (HDL) for writing compact models. Verilog-A code allows easy access to the model's internal equations and formulations, and allows logical modifications to the model core without breaking the flow of the mathematical description. Thus, PSP model is the natural choice as a starting point for the SiC low voltage model.

In order to describe the development of the SiC MOSFET model, a brief physical derivation of the surface-potential relation for modeling MOSFETs has been presented in the next section. The application of the surface potential method in PSP model is then described. Finally, SiC-specific changes to the PSP model have been described in order to form a logical flow of model development.

4.1 Surface Potential Relation

This section introduces the concept of surface potential equation which relates the surface potential ψ_s to the terminal voltages V_G, V_D, V_S and V_B of the MOSFET. A detailed derivation of the Surface Potential Equation (SPE) is available in several text-books on solid-state devices [10]. Before the discussion on the MOSFET structure can proceed, an understanding of the nomenclature is necessary. Fig. 4.1(a) shows a cross-section view of the Metal-Oxide-Semiconductor (MOS) structure and the associated energy band diagram at equilibrium is shown in Fig. 4.1(b). In the present discussion, an ideal MOS capacitor structure is assumed where there is no metal-semiconductor work function difference ($\phi_{ms} = 0$), and all charges in the oxide can be neglected. The non-ideal effects can be easily accounted for by adding a flat-band voltage term V_{FB} as described later.

In an ideal MOS capacitor, under zero bias conditions, flat-band condition exists in the structure. When a positive voltage V_F is applied to the gate, the energy band structure changes as shown in Fig. 4.1(c). The Fermi-level of the metal is pushed down by a value qV_F. Since no current can flow in the semiconductor due to the presence of the oxide, the Fermi level in the semiconductor stays flat ($dE_F/dx = 0$) and bands in the semiconductor bend.

The total band-bending in the semiconductor is due to the build-up of a depletion layer in the substrate near the interface due to the applied positive bias on the gate. The amount of band-bending at any point in the semiconductor is characterized by the semiconductor potential $\psi_p(x)$. The potential at the surface ($x = 0$) of the semiconductor/insulator interface is called the surface potential ψ_s. For the sake of brevity, $\psi_p(x)$ is written as ψ_p in the equations and is assumed to vary

Table 4.1: Operating regions of the MOS-CAP

Region	**Description**
$\psi_s < 0$	Accumulation of holes
$\psi_s = 0$	Flat-band condition
$0 < \psi_s < \psi_{Bp}$	Depletion
$\psi_s = \psi_{Bp}$	Intrinsic point, Fermi-level at mid-gap
$\psi_{Bp} < \psi_s \leq 2\psi_{Bp}$	Weak inversion
$\psi_s > 2\psi_{Bp}$	Strong inversion

with x. The concentration of electrons and holes in the depletion region is given as

$$n_p(x) = n_{p0} \exp\left(\frac{q\psi_p}{kT}\right) = n_{p0} \exp(\beta\psi_p) \tag{4.1}$$

$$p_p(x) = p_{p0} \exp\left(\frac{-q\psi_p}{kT}\right) = p_{p0} \exp(-\beta\psi_p) \tag{4.2}$$

where $\beta \equiv q/kT$ and ψ_p is positive for a downward bending of the bands. Thus, the densities of electron and holes at the surface can be written as

$$n_p(0) = n_{p0} \exp(\beta\psi_s) \tag{4.3}$$

$$p_p(0) = p_{p0} \exp(-\beta\psi_s) \tag{4.4}$$

Based on the definition of ψ_s, the different operating regions of the MOS structure have been defined in table 4.1. The potential at any point in the depletion region, ψ_p can be calculated by

using Poisson's equation inside the depletion region as

$$\frac{d^2\psi_p}{dx^2} = \frac{-\rho(x)}{\varepsilon_s} \tag{4.5}$$

where the charge density in the depletion region is given by

$$\rho(x) = q\left(N_D^+ + p_p - N_A^- - n_p\right) \tag{4.6}$$

where N_D^+ and N_A^- are the charges due to ionized dopant donors and acceptors respectively. Away from the surface in the bulk region, charge neutrality exists which implies $\rho(x) = 0$ and $\psi_p(\infty) = 0$. Thus, a condition for neutrality in the bulk region is obtained as

$$N_D^+ - N_A^- = n_{p0} - p_{p0} \tag{4.7}$$

Substituting (4.7) in (4.5) and using values of n_p and p_p from (4.1) and (4.2) respectively results in

$$\begin{aligned}\frac{d^2\psi_p}{dx^2} &= -\frac{q}{\varepsilon_s}\left(n_{p0} - p_{p0} + p_p - n_p\right) \\ &= -\frac{q}{\varepsilon_s}\left\{p_{p0}\left[\exp\left(-\beta\psi_p\right) - 1\right] - n_{p0}\left[\exp\left(\beta\psi_p\right) - 1\right]\right\}\end{aligned} \tag{4.8}$$

Integrating (4.8) from the surface ($x = 0$) to bulk gives

$$\int_0^{d\psi_p/dx} \frac{d\psi_p}{dx}\, d\left(\frac{d\psi_p}{dx}\right) = -\frac{q}{\varepsilon_s}\int_0^{\psi_p} \left\{p_{p0}\left[\exp\left(-\beta\psi_p\right) - 1\right] - n_{p0}\left[\exp\left(\beta\psi_p\right) - 1\right]\right\} d\psi_p \tag{4.9}$$

Since electric field E is related to potential ψ_p as $E = -d\psi_p/dx$, (4.9) can be integrated for E as

$$E^2 = \left(\frac{2kT}{q}\right)^2 \left(\frac{qp_{p0}\beta}{2\varepsilon_s}\right) \left\{ [\exp(-\beta\psi_p) + \beta\psi_p - 1] + \frac{n_{p0}}{p_{p0}} [\exp(\beta\psi_p) - \beta\psi_p - 1] \right\} \tag{4.10}$$

Some abbreviations can be defined to simplify (4.10)

$$L_D \equiv \sqrt{\frac{kT\varepsilon_s}{p_{p0}q^2}} \equiv \sqrt{\frac{\varepsilon_s}{qp_{p0}\beta}} \tag{4.11}$$

$$F\left(\beta\psi_p, \frac{n_{p0}}{p_{p0}}\right) \equiv \sqrt{[\exp(-\beta\psi_p) + \beta\psi_p - 1] + \frac{n_{p0}}{p_{p0}} [\exp(\beta\psi_p) - \beta\psi_p - 1]} \tag{4.12}$$

where L_D is known as the Debye length. Thus, with the appropriate abbreviations, the electric field at the surface is given as

$$E_S = \pm \frac{\sqrt{2}kT}{qL_D} F\left(\beta\psi_s, \frac{n_{p0}}{p_{p0}}\right) \tag{4.13}$$

where E_S is positive for a positive applied voltage (bands bending down). Applying Gauss's law at the surface, the total charge in the semiconductor is obtained as

$$\begin{aligned} Q_s &= -\varepsilon_s E_s \\ &= \mp \frac{\sqrt{2}\varepsilon_s kT}{qL_D} F\left(\beta\psi_s, \frac{n_{p0}}{p_{p0}}\right) \end{aligned} \tag{4.14}$$

Now it is easy to see that when a positive voltage is applied to the gate, E_S is positive and Q_s is negative, as inversion occurs at the surface, with excess electrons in the P-substrate. The applied bias at the gate (with bulk as the reference) is divided as

$$V_G = \phi_{ox} + \psi_s \tag{4.15}$$

where ϕ_{ox} is the voltage drop across the oxide, and is given by

$$\phi_{ox} = \frac{-Q_s}{C_{ox}} \tag{4.16}$$

where C_{ox} is the oxide capacitance per unit area given as $C_{ox} = \varepsilon_s/d$. Thus from (4.14), (4.15) and (4.16) the final SPE in the raw form is obtained as

$$V_G = \psi_s + \frac{\sqrt{2}\varepsilon_s kT}{qL_D C_{ox}} F\left(\beta\psi_s, \frac{n_{p0}}{p_{p0}}\right) \tag{4.17}$$

A few comments need to be made about (4.17). Firstly, although the equation has been derived using a MOS-CAP structure, it can be extended for a MOSFET structure also because no MOS-CAP specific simplifications have been made. In order to extend the SPE for a MOSFET in non-equilibrium, the position dependent electron and hole quasi-Fermi levels need to be used in (4.12). Secondly, the SPE in its present form cannot be solved analytically to obtain ψ_s as a function of V_G. Different surface potential based modeling approaches provide simplifications to (4.17) in order to provide an analytical solution. The PSP model formulation is based on an approximate analytical formulation of the SPE [77]. The non-ideal effects in the MOSFET structure can be included by using a flat-band voltage term V_{FB}, given as

$$V_G - V_{FB} = \psi_s + \frac{\sqrt{2}\varepsilon_s kT}{qL_D C_{ox}} F\left(\beta\psi_s, \frac{n_{p0}}{p_{p0}}\right) \tag{4.18}$$

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_{ox}} \tag{4.19}$$

where ϕ_{ms} is the metal-semiconductor work-function difference, Q_f is the number of fixed charge

on the interface per unit area, Q_m is the number of mobile ions in the oxide per unit area and Q_{ot} is the number of trapped charges in the oxide due to hot-electron injection.

4.1.1 The Two Dimensional Problem

Once the surface-potential equation is derived for a general case, the specific case of a MOSFET with bias on the drain and the gate can be analyzed. A 2-D structure of the MOSFET with a coordinate system is shown in Fig. 4.2(a). The energy band diagram of the MOSFET structure in zero-bias equilibrium ($V_D = V_G = V_S = V_B = 0$) is shown in Fig. 4.2(b). When a positive voltage is applied to the gate, the device is still in equilibrium ($V_{DS} = V_{BS} = 0$) and band bending occurs in the p-substrate under the gate as shown in Fig. 4.2(c). When the gate-bias is increased to threshold value V_T, inversion occurs on the surface which is seen by the crossing of the Fermi level E_F from below the intrinsic level E_i to above it on the surface. When a drain bias is introduced, the device leaves the equilibrium condition, and the Fermi levels for holes (E_{Fp}) and electrons (E_{Fn}) in the substrate split as shown in Fig. 4.2(d).

In order to analyze the MOSFET structure, some assumptions and simplifications are made. The first simplification is the Gradual Channel Approximation (GCA) in the Poisson's equation, which assumes that the variation of the electric field and potential along the channel is much smaller as compared to the vertical variation

$$\left|\frac{\partial^2\psi}{\partial y^2}\right| \ll \left|\frac{\partial^2\psi}{\partial x^2}\right| \tag{4.20}$$

As a result of the GCA, the Poisson equation for a MOSFET can be given by (4.5). In the channel, the component of hole current is much smaller than the electron current, and thus the variation of

hole Fermi level E_{Fn} is very small, and is assumed to be constant and equal to the bulk value. For electrons, variation in the quasi-Fermi level with position is important, and the position dependent concentration of electrons is given by

$$n_p(x,y) = n_{p0} \exp\left[\beta\left(\psi_p(x) - \phi_n(x,y)\right)\right] \tag{4.21}$$

where $\phi_n(y)$ is the splitting of the Fermi-levels along the channel due to the applied drain bias and is given as

$$\phi_n(x,y) = \left(E_{Fp} - E_{Fn}(x,y)\right)/q \tag{4.22}$$

The two dimensional problem encountered in the MOSFET is clearly highlighted in (4.21), where one can see that the electron concentration in the channel is both a function of the gate-bias and the drain-bias. Using (4.21) and (4.22), the Poisson equation can now be written as

$$\frac{d^2\psi_p}{dx^2} = -\frac{q}{\varepsilon_s}\left\{p_{p0}\left[e^{-\beta\psi_p} - 1\right] - n_{p0}\left[ke^{\beta\psi_p} - 1\right]\right\} = \frac{q}{\varepsilon_s}\,\rho \tag{4.23}$$

where

$$k = \exp(-\beta\phi_n(x,y)) \tag{4.24}$$

Following the same procedure as described in (4.9)-(4.13), we obtain

$$E_s^2 = -\frac{2kTp_{p0}}{\varepsilon_s}\int_0^{\psi_s} \rho\, d\psi \tag{4.25}$$

The integral in (4.25) cannot be solved analytically due to the presence of k in ρ (4.23) which is position dependent. One of the simplifications that is made is to assume the electron Fermi-level

to be independent of x and assume k to be k_0 where

$$k_0 = \exp(-\beta\phi_{ns}) \tag{4.26}$$

where ϕ_{ns} is the Fermi-level splitting at the interface. The value of ϕ_{ns} at the drain is equal to applied drain bias V_D. Using the static approximation for ϕ_{ns}, (4.25) can now be evaluated as

$$E_s = \pm\frac{\sqrt{2}kT}{qL_D}F_{PS}\left(\beta\psi_s, \frac{n_{p0}}{p_{p0}}, V_D\right) \tag{4.27}$$

where F_{PS} is the position-static evaluation of the integral, and is given as

$$F_{PS}\left(u, \frac{n_{p0}}{p_{p0}}, V_D\right) = \left[e^{-u} + u - 1 + \frac{n_{p0}}{p_{p0}}k_0\left(e^{u} - \frac{u}{k_0} - 1\right)\right]^{\frac{1}{2}} \tag{4.28}$$

$$u = \beta\psi_s \tag{4.29}$$

The formulation for F_{PS} is fully valid for MOS capacitors ($k_0 = 1$) and works well for MOSFETs [78]. However, it has been shown that the expression inside the square brackets in (4.28) becomes negative for a very small bias range near the flat-band ($\psi_s = 0$), which is un-physical and causes convergence problems in simulators [79], [77]. The discrepancy comes from the assumption that the electron Fermi-level E_{Fn} is independent of x. As a result, the PSP model [1] has been derived by taking into account the position dependence of E_{Fn} [78].

4.1.2 PSP Surface Potential Equation

As described in the last section, the assumption of position-independent electron Fermi level causes problems in the simulation of the SPE. As a result, the PSP SPE is derived without using the assumption of $\partial\phi_n/\partial x = 0$. Detailed derivation can be found at [4], [78]. If the integral on the right hand side of (4.25) is denoted by $h(u)$, then

$$\begin{aligned} h(u) &= \int_0^{\psi_s} \rho \, d\psi \\ &= e^{-u} + u - 1 + \frac{n_{p0}}{p_{p0}} \left[\int_0^u k\,(e^{\omega} - 1)\, d\omega + \int_0^u (k-1)\, d\omega \right] \end{aligned} \tag{4.30}$$

Applying the mean-value theorem in (4.30),

$$\int_0^u k\,(e^{\omega} - 1)\, d\omega = k\,(\xi) \int_0^u (e^{\omega} - 1)\, d\omega; \quad \xi \in (0, u) \tag{4.31}$$

Thus, (4.30) can be simplified as

$$h(u) = e^{-u} + u - 1 + \frac{n_{p0}}{p_{p0}} \left[k\,(\xi)\,(e^{u} - u - 1) + (k_{av} - 1)\, u \right] \tag{4.32}$$

where

$$k_{av} = \frac{1}{u} \int_0^u k \, d\omega \tag{4.33}$$

The addition of two parameters $k(\xi)$ and k_{av} allows the improvement of (4.28), where $k(\xi)$ and k_{av} can still be made independent of u, but can solve the problem of the negative term inside the square-root in (4.27). In strong inversion, it is safe to assume that $h(u) = F_{PS}^2 \left(u, \frac{n_{p0}}{p_{p0}}, V_D \right)$. Thus,

the value of $k(\xi)$ is obtained as k_0. The second condition is that $h(0) = 0$ and $h(u) > 0$ for all other u. Thus, the value of k_{av} is obtained as 1. Thus, (4.32) is reduced to

$$h(u) = e^{-u} + u - 1 + \frac{n_{p0}}{p_{p0}} k_0 \left(e^{u} - u - 1\right) \tag{4.34}$$

While the formulation of $h(u)$ is complete, the formulation in (4.34) causes problems of asymmetry between the source and the drain in the accumulation region ($\psi_s < 0$) [78]. Thus, an empirical adjustment is made to $h(u)$, and the final form is obtained as

$$h(u) = e^{-u} + u - 1 + \frac{n_{p0}}{p_{p0}} k_0 \left(e^{u} - u - 1 - \frac{u^2}{u^2 + 1}\right) \tag{4.35}$$

The final SPE in PSP is given as

$$V_G - V_{FB} = \psi_s + \frac{\sqrt{2\varepsilon_s p_{p0} kT}}{C_{ox}} \sqrt{h(\psi_s)} \tag{4.36}$$

where $h(\psi_s)$ is the value of (4.35) evaluated at $u = \beta\psi_s$. It can be seen that (4.36) cannot be solved analytically, and numerical methods like Levenberg-Marquardt (LM) method are used to obtain the solution.

Numerical methods are usually computation-intensive and are less preferred in compact models. It is desirable to have a closed-form solution for ψ_s as a function of the applied biases. The PSP model code uses a closed-form approximate solution of (4.36). The steps to obtain the numerical solution have been derived by the authors of PSP model [80], and have been shown here for the sake of completeness of the derivation.

The numerical solution starts with normalizing the terms in (4.36) to $1/\beta$ as

$$\left(x_{gfb}-x\right)^2 = G^2\left[x-1+\exp\left(x-x_n\right)\right] \tag{4.37}$$

where

$$x = \beta\psi_s \tag{4.38}$$

$$G = \beta\gamma \tag{4.39}$$

$$x_{gfb} = \beta\left(V_G - V_{FB}\right) \tag{4.40}$$

$$x_n = \beta\left(2\phi_B + \phi_{ns}\right) \tag{4.41}$$

A few macros can be defined as

$$x_{sub} = x_{gfb} + G^2/2 - G\sqrt{x_{gfb} - 1 + G^2/4} \tag{4.42}$$

$$s(a,b,c) = \frac{1}{2}\left[a+b-\sqrt{(a-b)^2+c}\right] \tag{4.43}$$

$$\sigma(a,c,\tau) = \frac{a\nu}{\mu + \frac{\nu}{\mu}c\left(\frac{c^2}{3}-a\right)} \tag{4.44}$$

where

$$\nu = a + c \tag{4.45}$$

$$\mu = \frac{\nu^2}{\tau} + \frac{c^2}{2} - a \tag{4.46}$$

Using (4.37)-(4.46), the value of ψ_s is calculated using the following steps:

1. Calculate η

$$\eta = s(x_{sub}, x_n + 3,5) \tag{4.47}$$

2. Calculate x_0

$$a = \left(x_{gfb} - \eta\right)^2 - G^2\eta + G^2 \tag{4.48}$$

$$c = 2\left(x_{gfb} - \eta\right) + G^2 \tag{4.49}$$

$$\tau = x_n - \eta + \ln\left(a/G^2\right) \tag{4.50}$$

$$x_0 = \eta + \sigma(a, c, \tau) \tag{4.51}$$

3. Calculate surface potential ψ_s as

$$\Delta_0 = \exp\left(x_0 - x_n\right) \tag{4.52}$$

$$p = 2\left(x_{gfb} - x_0\right) + G^2\left(1 + \Delta_0\right) \tag{4.53}$$

$$q = \left(x_{gfb} - x_0\right)^2 - G^2\left(x_0 + \Delta_0 - 1\right) \tag{4.54}$$

$$x = x_0 + \frac{2q}{p + \sqrt{p^2 - 2\left(2 - G^2\Delta_0\right)q}} \tag{4.55}$$

$$\psi_s = x/\beta \tag{4.56}$$

4.1.3 Interface Traps in SiC

The biggest problem currently faced by SiC MOSFETs is the poor quality of the SiC/SiO_2 interface which leads to a large density of interface states [81]-[83]. Yano et al. and Chung et al have shown

that the growth of SiO_2 on SiC using dry O_2 results in a large density of interface traps [84], [85]. Yano et al. have shown that low inversion mobility in SiC MOSFETs is due to the presence of large density of interface states [84]. Afanas'ev et al. [86] reported two types of interface traps at the SiC/SiO_2 interface: (a) Slow traps that can be passivated by NO annealing and (b) fast traps that can be passivated by N_2O based oxide . The Sodium-Enhanced Oxidation (SEO) technique to grow gate-oxides has shown to have lower density of interface traps near the conduction band edge as measured by thermal dielectric measurements [87]-[61].

Sheppard et al. have shown a C-V measurement based method to estimate the density of interface states in 6H-SiC MOS structures [59]. Saks et al. have shown a Hall-effect based technique to determine the density of interface states [60]. Arnold et al. have shown that Coulumbic scattering of electrons in the channel due to immobile charges in the interface states is the dominant scattering mechanism responsible for lowering the surface mobility in lightly doped p-type SiC substrates [89]. Tilak et al. [90] have reported that the contribution of Coulumbic scattering and surface roughness on the inversion layer mobility is significant for SiC MOSFETs

It can be seen that the presence of interface states is a very important physical mechanism that governs the channel mobility in SiC MOSFETs. A compact model for SiC MOSFETs must provide an efficient and accurate formulation to account for the presence of interface states in the MOSFET. In addition, in the derivation of the approximate closed-form solution for surface potential ψ_s in the PSP model [80], the effects of a density of state distribution has not been taken into account. In this work, a new formulation to describe the density of interface states in the PSP model has been proposed. The formulation offers a numerical form of the surface potential equation in the presence of interface states in SiC. The formulation can be extended into an analytical solution of the surface potential variable, and then can be easily implemented in a compact model.

4.2 Modeling Interface Traps

Saks et al. [81] have provided a formulation of the distribution of the density of interface states, based on characterization of SiC MOSFETs as

$$D_{it}(E) = D_{it,mid} + D_{it,edge}\, e^{\left(\frac{E-E_C}{\sigma_{it}}\right)} \tag{4.57}$$

where $D_{it,mid}$ is the constant interface state density near the middle of the band-gap, $D_{it,edge}$ is the interface state density in the band-gap near the conduction band edge and sig_{it} models the tail of the exponential interface state description. The variation of density of interface states inside the band-gap as described by (4.57) for $D_{it,mid} = 1 \times 10^{11}$ cm^{-2} eV^{-1}, $D_{it,edge} = 1 \times 10^{14}$ cm^{-2} eV^{-1} and $\sigma_{it} = 0.075$ eV is shown in Fig. 4.3.

The density of interface traps can be integrated within the band-gap to obtain the trapped charge per unit area as

$$Q_{it}(\psi_s) = q \int_{E_i}^{E_F} D_{it} dE = q \left\{ D_{it,mid}\, \psi_s + D_{it,edge}\, \sigma_{it}\, \mathrm{e}^{\frac{(E_i-E_C)}{\sigma_{it}}} \left[\mathrm{e}^{\frac{\psi_s}{\sigma_{it}}} - 1 \right] \right\} \tag{4.58}$$

The assumption under which the interface trapped charge density Q_{it} is derived is that the trapped charge is an infinitesimally thin sheet of charge next to the interface in the oxide that varies with the Fermi-level or ψ_s. This assumption is physically reasonable, because studies on the properties of the interface traps have shown experimentally that the traps are spatially located within a few monolayers of Si-O-C on the interface [37]. Thus, the interface trapped charge is similar in its effect to the fixed oxide charges, in that both charges are located next to the interface in the oxide.

The main difference between Q_{it} and Q_{ot} is that Q_{it} depends on the ψ_s and thus varies with the applied bias. However, its effect can be included in the SPE similar to Q_{ot}. One can re-write (4.19) to include the effects of Q_{it} as

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_{ox}} - \frac{Q_{it}(\psi_s)}{C_{ox}} \tag{4.59}$$

Using V_{FB0} for the bias-independent part of V_{FB} and using (4.58), we get

$$V_{FB} = V_{FB0} - \frac{q}{C_{ox}} \left\{ D_{it,mid}\, \psi_s + D_{it,edge}\, \sigma_{it}\, e^{\frac{(E_i - E_C)}{\sigma_{it}}} \left[e^{\frac{\psi_s}{\sigma_{it}}} - 1 \right] \right\} \tag{4.60}$$

Substituting the new value of V_{FB} in (4.36), we get the final SPE of the form

$$V_G - V_{FB0} = Q_{it}(\psi_s) + \psi_s + \frac{\sqrt{2\varepsilon_s p_{p0} kT}}{C_{ox}} \sqrt{h(\psi_s)} \tag{4.61}$$

where $Q_{it}(\psi_s)$ is defined in (4.58). Since the term $Q_{it}(\psi_s)$ monotonically increases with ψ_s, it can be seen from (4.61) that the introduction of trapped charge effectively decreases the value of ψ_s for any given applied gate-voltage. Physically, it can be explained as follows.

The applied gate voltage V_G is divided between the voltage drop in the oxide ϕ_{ox} and the potential drop in the semiconductor ψ_s as (4.15)

$$V_G = \phi_{ox} + \psi_s$$

Since the interface trapped charge Q_{it} is assumed to reside next to the interface in the oxide, it does not directly affect ψ_s. However, by a direct consequence of Gauss's theorem, Q_{it} increases

the surface electric field and thus increase ϕ_{ox}. For the same applied gate voltage, an increase in ϕ_{ox} results in a decrease of ψ_s which reduces the inversion charge Q_i and depletion charge Q_{dep} in the semiconductor. The trapped charges become detrimental to the formation of the channel by resulting in a reduction of Q_i for any applied V_G, and also acting as Coulumbic scattering centers for Q_i. As V_G increases, the inversion charge Q_i also increases, and the top layer of electrons in the channel screen the other electrons from the trapped charges. As a result, the influence of Coulumbic scattering due to Q_{it} is reduced, and surface roughness becomes the dominant limiting mechanism for mobility.

4.2.1 Implementation

The final SPE (4.61), taking into account Q_{it} cannot be solved analytically, and Levenberg-Marquadt method has been used. The new SPE has been implemented in a numerical form in Matlab along with other PSP equations described in the previous section. This allows an analysis of all the internal variables in the PSP model with the new SPE implementation. The native PSP model calculates the surface potential using an approximate analytical solution [80]. Instead of using PSP's approximate solution for ψ_s, the new SPE has been used to solve for ψ_s with bias, and rest of the calculations obtained from ψ_s like Q_i, I_D etc., have been done using PSP equations.

Fig. 4.4 shows the calculated values of surface potential using (4.61), for the condition of no interface states ($D_{it,mid} = 0$, $D_{it,edge} = 0$) and with interface states ($D_{it,mid} = 10^{11}$ cm^{-3}, $\sigma_{it} =$ 0.085 eV and varying $D_{it,edge}$). Flat-band voltage is assumed to be 0 for simplicity without lack of generalization. It can be seen that the surface potential in weak and moderate inversion reduces due to the built-up of interface trapped charge, and is calculated by the new SPE. Also, the transition from weak inversion to saturation is characterized by the gradual transition of the surface potential

from the linear increase to a saturated value, due to the build-up of trapped charge.

Fig. 4.5 shows the build-up of the inversion and trapped charges for $D_{it,edge} = 10^{13}$ cm^{-3}. Naturally, for the zero trap condition, $Q_{it} = 0$. It can be seen that the main effect of including Q_{it} in the SPE is the reduction in Q_i for any given gate-bias. This effect causes the gradual transition from weak inversion to strong inversion, as seen in the input characteristics of the enhancement MOSFETs (Fig. 3.45). The gradual transition can also be achieved by the native PSP model using the Coulumbic scattering parameter **CS**. However, **CS** only affects the current calculation inside the model, and ignores the reduction of Q_i, which is not physical.

Fig. 4.6 shows the comparison between the calculated drain current using the original and new SPE, along-with measured input characteristics of the $16\mu m \times 8\mu m$ enhancement MOSFET. The effect of the trapped charge is seen during the region between weak inversion and the onset of strong inversion. Using the Coulumbic scattering parameter **CS** in the native PSP model, it is not possible to get a good description of the build-up of trapped charge in the channel, and the model deviates from measurement in that region. With the new SPE, the calculated drain current matches the measured drain current in weak inversion region well.

While it is clear that the trapped charge must be properly accounted by any model to accurately describe the operation of SiC MOSFETs, especially in the weak/moderate inversion region, implementation of the new SPE in a geometry and temperature scaled compact model is a non-trivial task. One of the limitation of the new SPE formulation is that it is prone to non-convergence for some bias values, and the solution for the surface potential relies on the initial values used in the numerical algorithm. Moreover, the initial value guess also depends on the bias and thus is a limitation of using the new SPE in a compact formulation. When the model convergence problems are overcome, simulation times have been seen to increase by a factor of three. Despite the challenges

of implementing the new SPE in a compact formulation, the work presented in this section is a complete mathematical description of the effect of interface charges, and can serve as a foundation for development of compact model equations.

Due to the challenges of convergence and simulation times with the new SPE, for the purpose of large-scale circuit design, the native PSP model with changes in the code for SiC specific material properties like intrinsic carrier concentration, band-gap with temperature scaling and surface mobility has been used. The main reason for this approach is because the PSP model has a closed-form analytical solution for the surface potential in its native code. Also, the partial effect of mobility reduction due to the presence of interface traps can be modeled by the native PSP model using the Coulumbic scattering paramter **CS**. The results for parameter extraction and model performance for the SiC PSP model have been presented in the next few sections of this chapter.

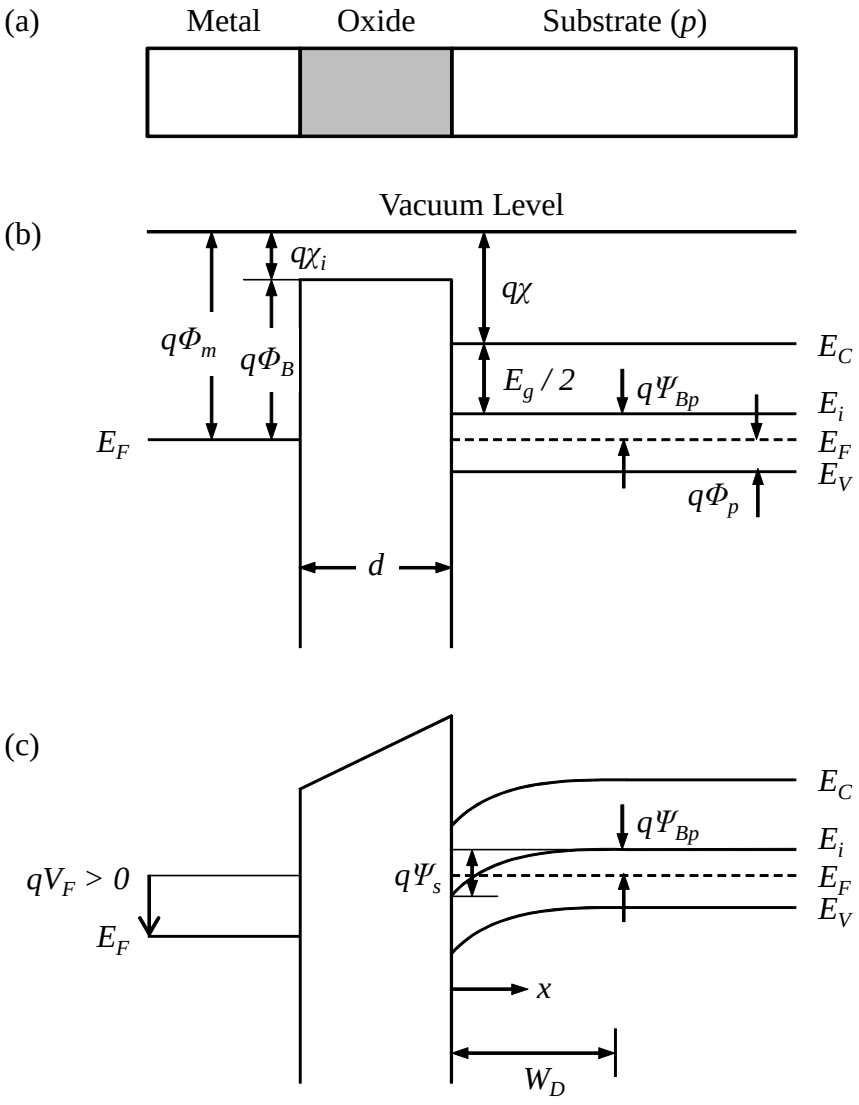


Fig. 4.1: Ideal MOS-CAP with (a) 2-D structure. (b) Energy band diagram at flat-band. (c) Energy band diagram with positive gate-voltage

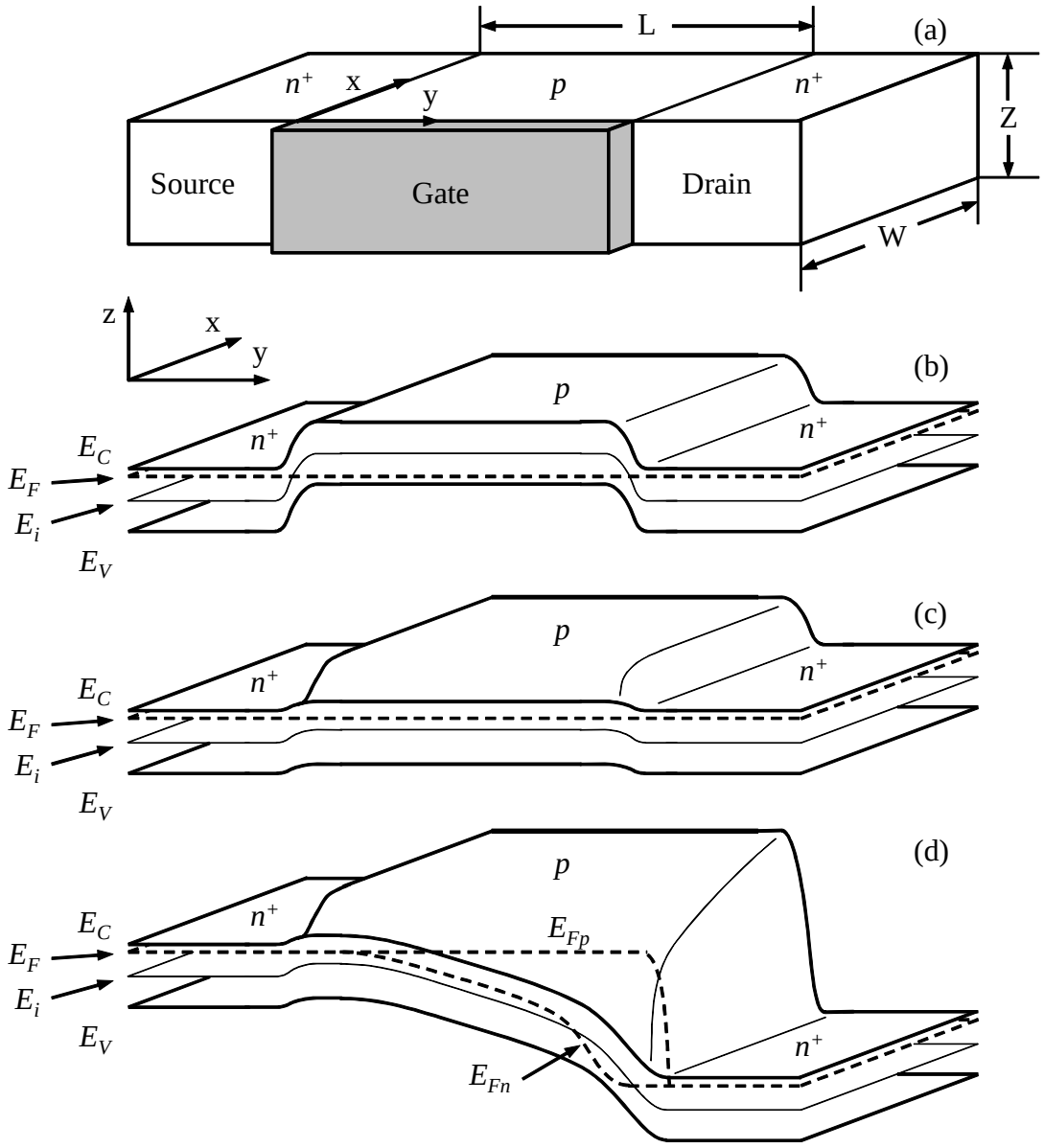


Fig. 4.2: 2-D energy band diagram of a MOSFET with (a) Device structure. (b) Band diagram for zero gate bias equilibrium condition ($V_{DS} = 0$). (c) Band diagram for positive gate bias at equilibrium condition ($V_{DS} = 0$). (d) Band diagram for positive gate bias at non-equilibrium ($V_{DS} > 0$).

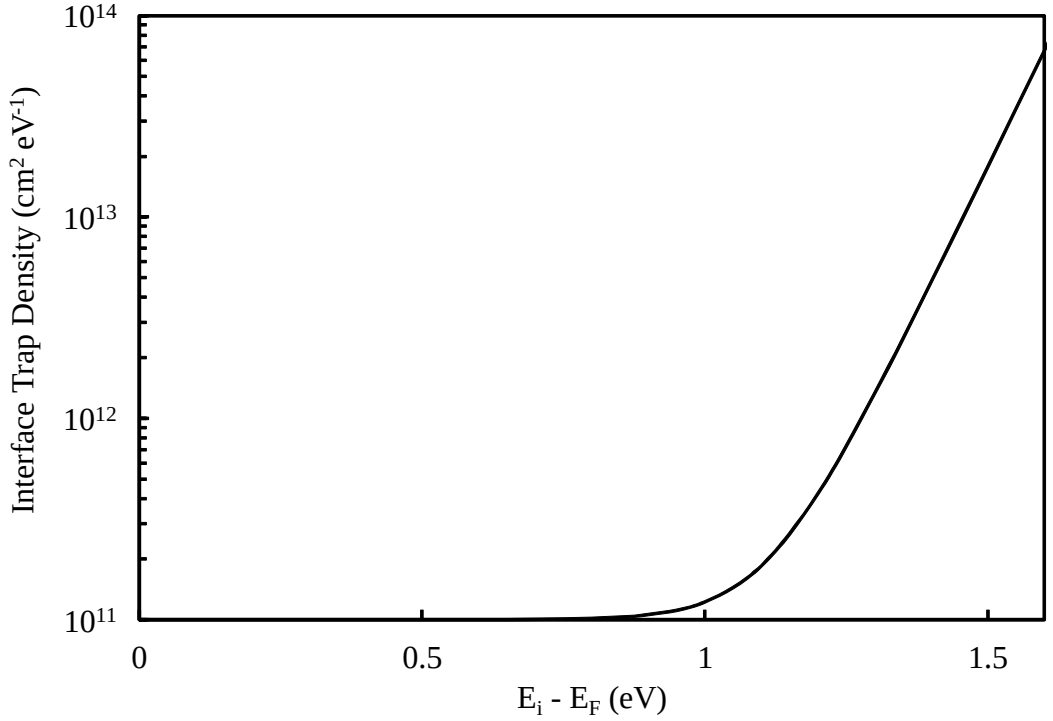


Fig. 4.3: Interface state density distribution within the band-gap

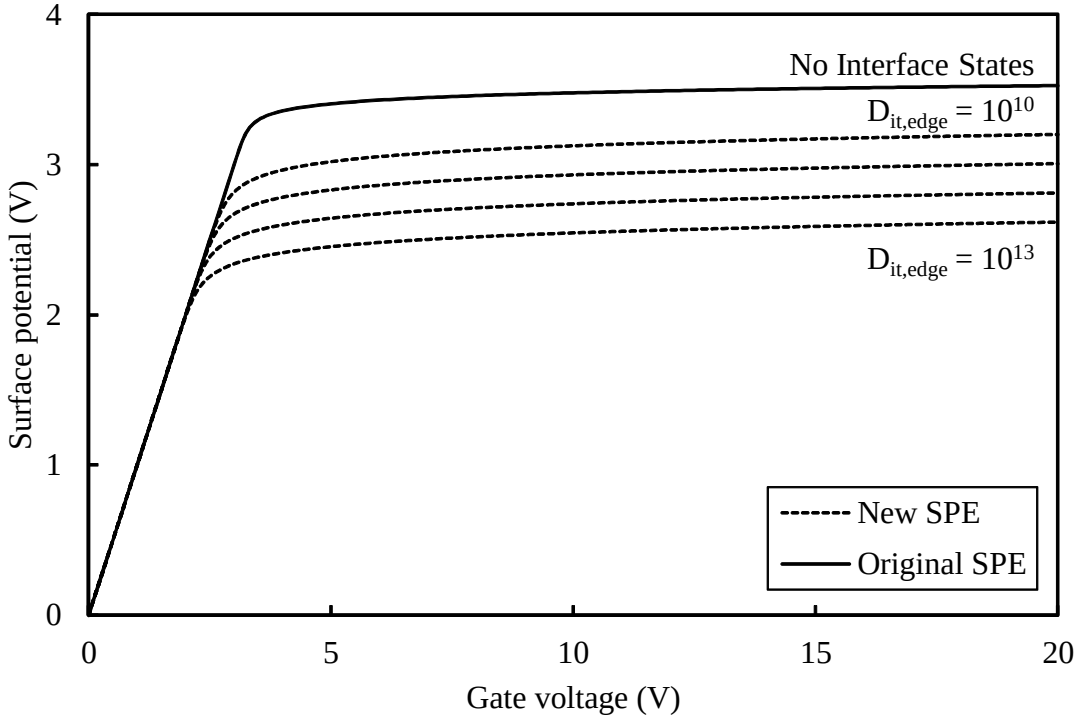


Fig. 4.4: Calculated surface potential using the original (4.36) and new surface potential equations (4.61)

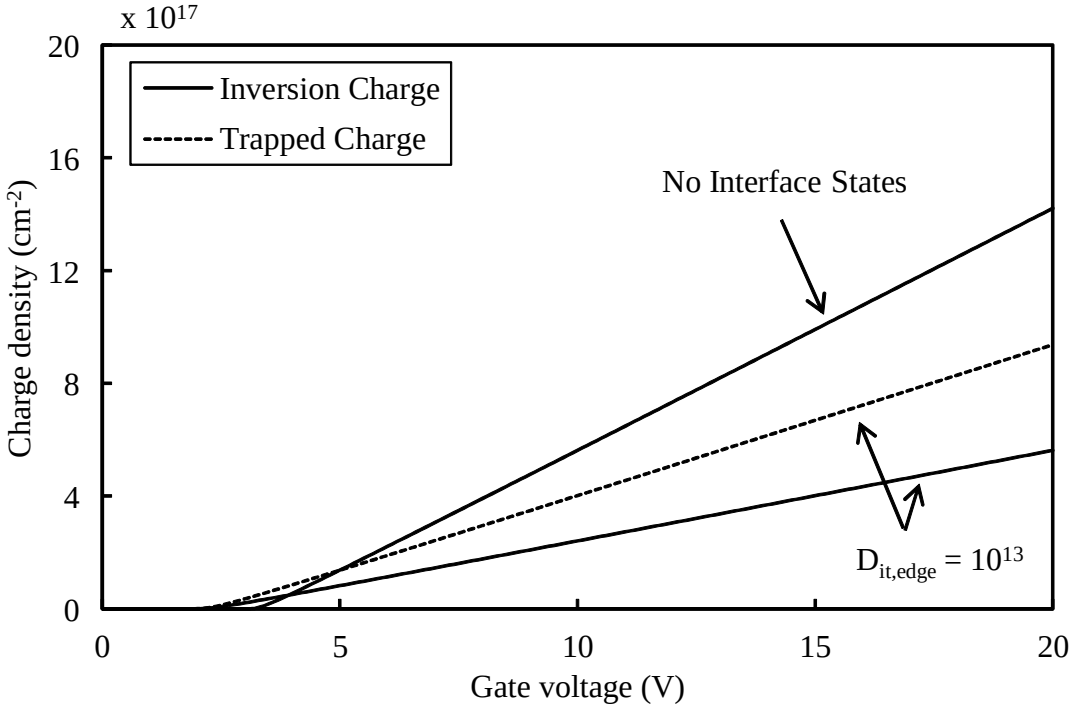


Fig. 4.5: Calculated inversion charge using the original (4.36) and new surface potential equations (4.61)

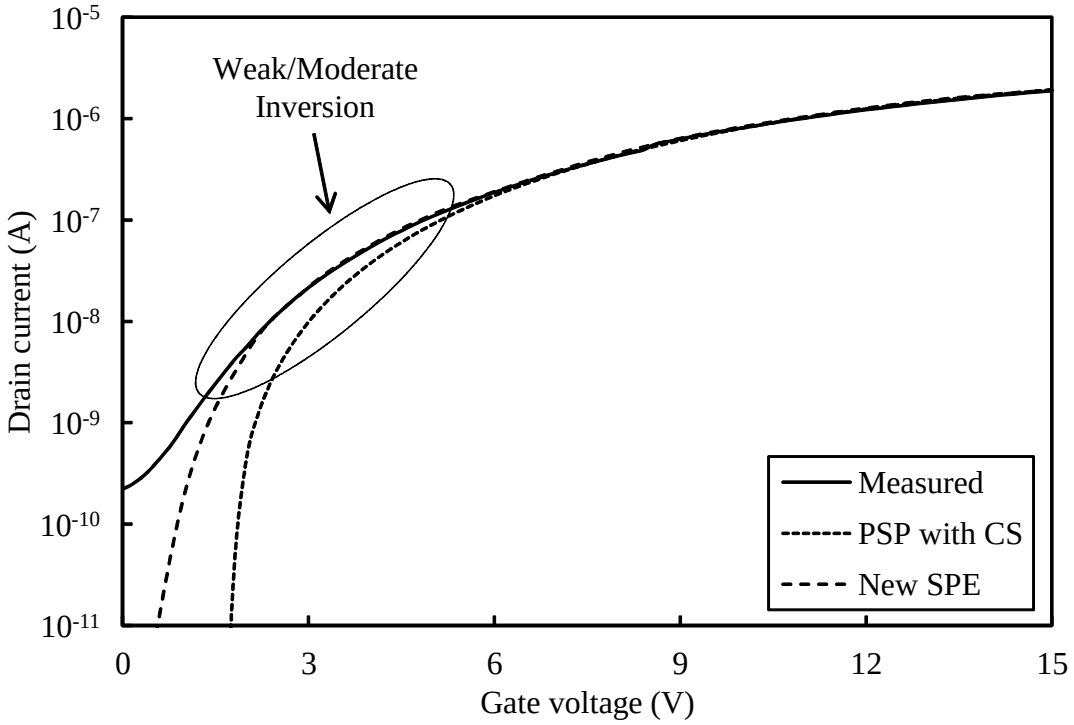


Fig. 4.6: Measured (solid) and Calculated (dashed) drain currents using the native PSP model with **CS** and the new SPE (4.61)

4.3 Parameter Extraction

A detailed parameter extraction strategy is outlined in the official PSP model documentation [1]. The extraction of a global parameter set for all the devices over temperature was broken into several smaller steps. A global parameter set is scaled for a given device size using geometry scaling rules and geometry scaled parameters. In addition, the global parameter set is also modified over temperature using temperature scaling rules and temperature scaling parameters. The final values of global parameters for a particular device size and simulation temperature are called *local parameters*. Local parameters are parameter values used inside the model after the geometry and temperature scaling calculations have been made.

The measurements required for parameter extraction have been outlined in sections 3.4 and 3.5. The parameter extraction strategy began with the extraction of local parameters for the long channel large device ($32\mu m \times 8\mu m$). This was done so that starting values for all the parameters were obtained without any short-channel or narrow-width effects.

AC parameters were extracted first using the $C_{GG} - V_G$ characteristics. The value of **TOX** was determined by process information, and fixed in the beginning of the parameter extraction process, because a lot of other parameters depend on the value of **TOX**. For the current process, the value of **TOX** was fixed at 40 nm. The various AC parameter extracted after fixing the value of **TOX** are shown in table 4.2. Their values were extracted by optimizing the simulated and measured $C_{GG} - V_G$ characteristics. The extracted values of **TOX**, **NP** were fixed after AC extraction. The values of **NEFF** and **DPHIB** served as initial values and were re-optimized later.

Before extraction of DC parameters, the AC parameters were optimized properly and fixed to their extracted values. Local DC parameters for the wide long channel MOSFET were ex-

Table 4.2: AC parameter extraction

Step	Parameters	Fitted To	Abs./Rel.
1	**VFB**, **NEFF**, **DPHIB**, **NP**, **COX**	$C_{GG} - V_G$	Relative
2	Re-optimize step 1		

tracted next. Since parameters were being extracted for SiC devices, all the initial parameter values were calculated for SiC. The long-channel device allowed proper extraction of mobility parameters **THEMU** and **MUE**.

The shape of the simulated $I_D - V_{GS}$ curve was roughly set by extracting **NEFF**, **BETN**, **MUE** and **THEMU** from the wide long-channel device. Then, **NEFF**, **DPHIB**, **CT** and **GFACNUD** were extracted using the sub-threshold region of the $I_D - V_{GS}$ characteristics. Mobility parameters **MUE**, **THEMU**, **CS**, **XCOR** and **BETN** were then re-optimized using the $I_D - VGS$ and $g_m - V_{GS}$ characteristics. Coulumbic scattering parameter **CS** is very important in describing the effect of interface states in the SiC enhancement MOSFETs, and proper extraction of **CS** is important. The value of velocity saturation parameter **THESAT** was then be estimated using the $I_D - V_{DS}$ measurement. The conductance parameters **ALP**, **ALP1**, **ALP2**, **VP** and **AX** were extracted using the $g_{DS} - V_{DS}$ measurement. **THESAT** was re-extracted using $I_D - V_{DS}$ measurement and the two steps were re-optimized until satisfactory fits were obtained. All the steps of parameter extraction for the wide long-channel MOSFET are outlined in table 4.3.

After the extraction of parameters for the wide long-channel MOSFET, parameters were extracted for the wide short-channel MOSFET ($32\mu m \times 2\mu m$). Doing so allowed the extraction of short-channel effect parameters like DIBL without including the effects of narrow-width. Mobility reduction parameters **MUE** and **THEMU** were taken from the long-channel MOSFET. First,

Table 4.3: DC wide long channel parameter extraction

Step	Parameters	Fitted To	Abs./Rel.
1	**NEFF**, **BETN**, **MUE**, **THEMU**	$I_D - V_{GS}$	Absolute
2	**NEFF**, **DPHIB**, **CT**, **GFACNUD**	$I_D - V_{GS}$	Relative
3	**MUE**, **THEMU**, **CS**, **XCOR**, **BETN**	$g_m - V_{GS}$	Absolute
4	**THESAT**	$I_D - V_{DS}$	Absolute
5	**ALP**, **ALP1**, **ALP2**, **VP**, **AX**	$g_{DS} - V_{DS}$	Relative
6	**THESAT**	$I_D - V_{DS}$	Absolute

parameters **NEFF**, **DPHIB**, **BETN** and **RS** were extracted using the $I_D - V_{GS}$ characteristics. The extracted value of **RS** from the short-channel MOSFET was copied back into the long-channel MOSFET parameter set, and steps 1-6 for the long-channel MOSFET was re-optimized. The rest of the parameters extracted for the short channel length are shown in table 4.4. Parameters **GFACNUD**, **VSBNUD** and **DVSBNUD** were only extracted if non-uniform doping effects in the substrate are needed. The NUD effect can be turned on by setting **SWNUD** to 1.

Table 4.4: DC wide short channel parameter extraction

Step	Parameters	Fitted To	Abs./Rel.
1	**NEFF**, **BETN**, **DPHIB**, **RS**	$I_D - V_{GS}$	Absolute
2	**NEFF**, **DPHIB**, **CT**, **GFACNUD**, **VSBNUD**, **DVSBNUD**	$I_D - V_{GS}$	Relative
3	**BETN**, **RS**, **XCOR**	$g_m - V_{GS}$	Absolute
4	**THESAT**	$I_D - V_{DS}$	Absolute
5	**CFB**	$g_{DS} - V_{DS}$	Absolute

Once satisfactory parameters were obtained for both the wide-long and wide-short channel MOSFETs, the extraction procedure described in tables 4.3 and 4.4 was be performed on all intermediate channel lengths and widths to obtain a set of local parameters for every intermediate device

size. In development of a global parameter set, the effects of temperature scaling and geometry scaling were treated separately as described in the next sub-sections.

4.3.1 Temperature Scaling Parameter Extraction

The temperature scaling parameters of any device can be extracted by using the room temperature local parameters determined for that device as a starting point. Next, the corresponding temperature scaling parameters are extracted using measured data at various temperature points. For example, instead of using **THEMU** in the parameter extraction procedure at elevated temperature, the corresponding temperature scaling parameter **STTHEMU** was extracted instead. The reference temperature **TR** was always set to room temperature, such that the local parameters obtained at room temperature were not affected by temperature scaling equations. For the SiC process, characterization for all devices was done at three temperature points of 25 °C, 125 °C and 225 °C. Tables 4.5 and 4.6 show the temperature scaling parameters extracted using over-T measurements from the long and short-channel MOSFETs.

Table 4.5: Temperature scaling parameters extracted using long-channel MOSFET

Step	**Parameters**	**Fitted To**	**Abs./Rel.**
1	**STVFB**	$I_D - V_{GS}$ over T	Relative
2	**STBETN**, **STMUE**, **STTHEMU**, **STCS**, **STXCOR**	$I_D - V_{GS}$ over T	Absolute
3	**STTHESAT**	$I_D - V_{DS}$	Absolute

Another approach to extracting temperature scaling parameters is to set the reference temperature **TR** to the corresponding temperature, e.g. 125 °C. Then all the local parameters are extracted for all the devices as described in the previous section, and local parameter sets are obtained at each temperature. Finally, the temperature scaling parameters can be extracted by the variation of each

Table 4.6: Temperature scaling parameters extracted using short-channel MOSFET

Step	Parameters	Fitted To	Abs./Rel.
1	**STVFB**	$I_D - V_{GS}$ over T	Relative
2	**STBETN**, **STRS**	$I_D - V_{GS}$ over T	Absolute
3	**STTHESAT**	$I_D - V_{DS}$	Absolute

local parameter over temperature. This approach is more time-consuming as it involves dealing with a very large number of parameters. However, if the native temperature scaling equations do not sufficiently described the variation of a particular parameter over the entire temperature range, such an approach is needed in order to determine the new temperature scaling for a particular parameter. For the purpose of the low voltage SiC MOSFETs, since the chosen temperature range was 25 °C to 225 °C, PSP's native temperature scaling equations proved sufficient and thus the first approach was used.

4.3.2 Geometry Scaling Parameter Extraction

Before the extraction of geometry scaling parameters, it is important to distinguish between mask dimensions and actual dimensions. Fig. 4.7 shows a schematic of a MOSFET with the difference between physical and layout L and W shown. The difference between actual layout length and physical length due to lateral source and drain diffusion is denoted by ΔL and the difference between layout width and physical width is denoted by ΔW. The value of ΔL can be extracted from the extrapolated zero-crossing of **1/BETN** versus mask length L, and the value of ΔW can be extracted from the extrapolated zero-crossing of **BETN** versus mask width W [91]. The details of the extracted values of ΔL and ΔW are given in Sections 4.4.4 and 4.5.4.

Once local parameters for all device sizes were extracted, corresponding geometry scaling

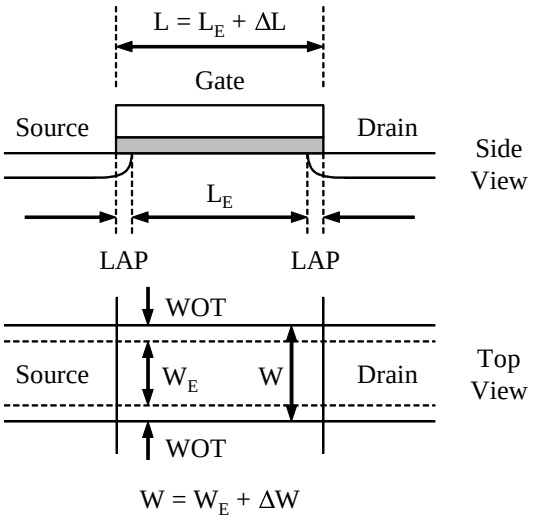


Fig. 4.7: Layout and physical dimensions in a MOSFET structure

parameters for each scalable parameter were extracted using the local parameters as a function of W and L. For example, the flat-band voltage parameter **VFB** has a geometry scaling rule given as [1]

$$V_{FB} = V_{FBO} + V_{FBL}\frac{L_{EN}}{L_E} + V_{FBW}\frac{W_{EN}}{W_E} + V_{FBLW}\frac{W_{EN}\,.\,L_{EN}}{W_E\,.\,L_E} \tag{4.62}$$

where V_{FB} is the local parameter value, V_{FBO} is the geometry independent part, V_{FBL} is the length dependent part, V_{FBW} is the width dependent part and V_{FBLW} is the area dependent part of the flat-band voltage. L_{EN} and W_{EN} were the electrical lengths and widths of the device, while L_E and W_E were reference values, and were kept at $1\mu m$ each inside the model. Each geometry scaled parameter has a similar equation as shown in (4.62), and thus an accurate scaling for each parameter over the entire geometry was obtained.

4.3.3 Final Optimization

Once both temperature scaling and geometry scaling parameters were extracted, a global parameter set was obtained which would describe the characteristics of all device sizes over temperature. It is often the case that the global parameter set does not fit *all* the devices equally well, and an optimization is obtained, where the global parameters fit all the device sizes well, but may not fit some individual devices. If more accuracy is needed for some particular device or temperature, the local parameters for that condition can be calculated from the global set using the scaling rules, and then rest of the parameters can be re-extracted to improve the fit for the particular condition. The other alternative is to use binned parameter sets, where each bin has a global parameter set of its own, and the parameters are switched when moving from one bin to the other, with each bin having its separate global and scaling parameters. For the low voltage SiC process, a single global parameter set was extracted and the next two sections show the model performance for the depletion and enhancement SiC MOSFETs.

4.4 Depletion MOSFET Model Performance

Parameters for depletion MOSFETs were extracted using characterization data over temperature as shown in section 3.4. This section has been sub-divided into several sections. First, the performance of the SiC PSP model for the wide-long ($32\mu m \times 8\mu m$), wide-short ($32\mu m \times 2\mu m$) and narrow-long ($8\mu m \times 8\mu m$) depletion MOSFETs at room temperature has been presented. Next, the geometry scaling of the various model parameters have been shown. Finally, the performance of the three corner devices has been shown at 125 °C and 225 °C. Agilent's IC-CAP software was used with ADS simulator for the parameter extraction and optimization [92]. The modified

Verilog-A code for PSP 103.1.1 was used with SiC specific constants and mobility changes.

4.4.1 Gate Capacitance

The characterization setup for gate capacitance $C_{GG} - V_G$ measurement has been described in section 3.4.1. Fig. 4.8 shows the simulated SiC PSP model for the $32\mu m \times 8\mu m$ depletion MOSFET. Parameter **TOX** was set to 40 nm. Initial values for **VFB**, **NEFF**, **DPHIB**, **NP** and **COX** were extracted. Good agreement was observed between the simulation and measurements. The measured $C_{GG} - V_G$ characteristic was seen to reduce in the accumulation region, and is likely due to the resistance of the accumulation layer.

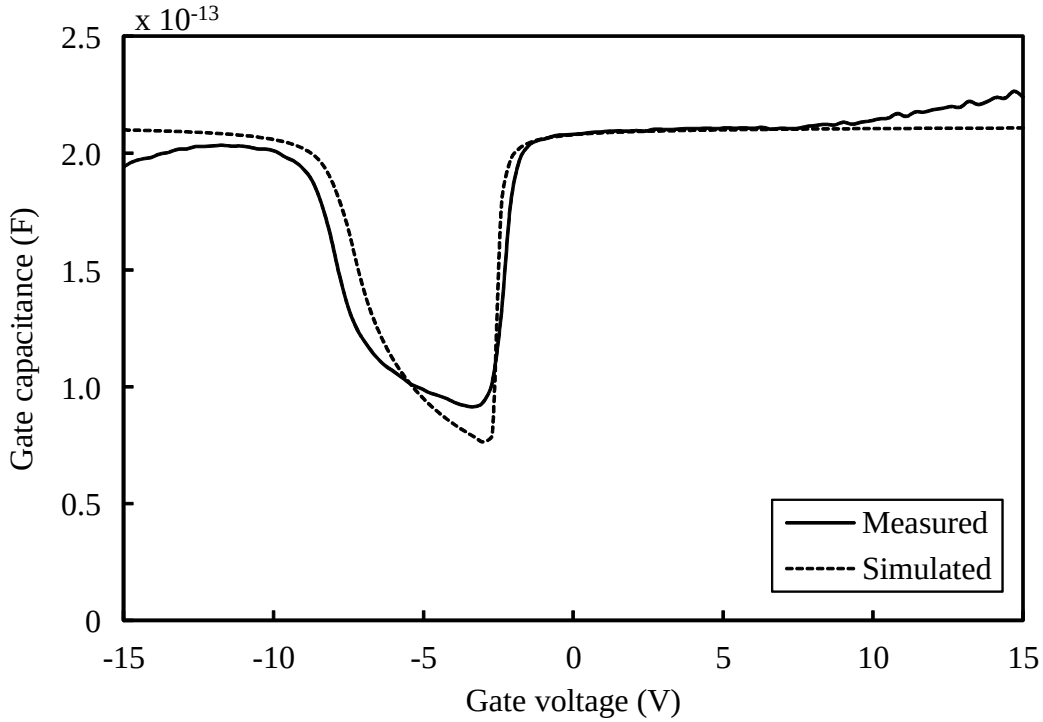


Fig. 4.8: Measured (solid) and simulated (dash) $C_{GG} - V_G$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET at 25 °C

4.4.2 Input Characteristics

The comparison between measurement and simulation of the input characteristics at room temperature of ($32\mu m \times 8\mu m$), ($32\mu m \times 2\mu m$) and ($8\mu m \times 8\mu m$) depletion MOSFETs is shown in Figs. 4.9 - 4.11 respectively. The back-bias dependence seen in the devices was not captured completely by the model at large back biases of $V_{SB} > 9\,V$. This was attributed to strong non-uniform doping in the substrate. However, most of the depletion MOSFETs are connected as active loads with their gates and sources tied together ($V_{GS} = 0$). **NEFF** and **DPHIB** were re-optimized using the $I_D - V_{GS}$ characteristics. Values for **BETN**, **MUE**, **THEMU**, **CT**, **CS**, **XCOR** were also extracted. It can be seen that the performance of the depletion MOSFETs was well matched by the model.

The derived transconductance ($g_m - V_{GS}$) characteristics for the three devices are shown in Figs. 4.12 - 4.14 respectively. The $g_m - V_{GS}$ characteristics show a mis-match between the model and simulation. The reason for the mis-match is that the depletion MOSFETs show a non-linear mobility reduction at higher gate biases due to non-uniform substrate doping, and the model parameters have been extracted to do a best-fit to the characteristics over the entire bias range. As a result, the peaks in the $g_m - V_{GS}$ characteristics are not fitted by the model, as the non-linear mobility reduction is not captured.

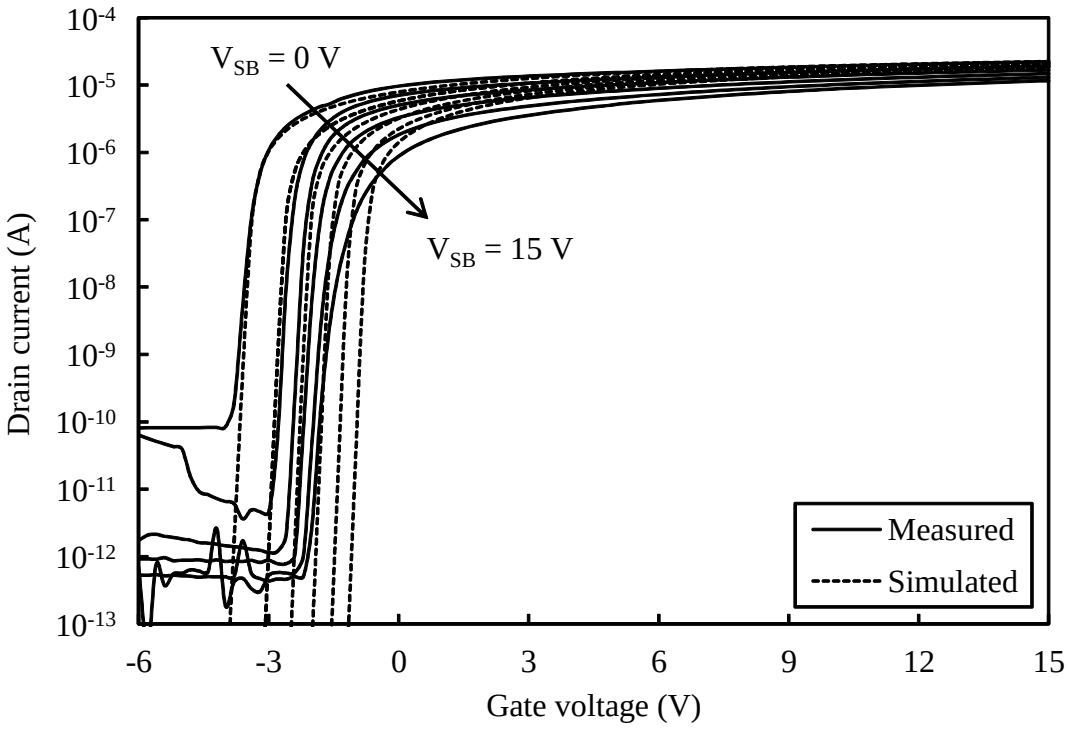


Fig. 4.9: Measured (solid) and simulated (dash) $I_D - V_{GS}$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET at 25 °C

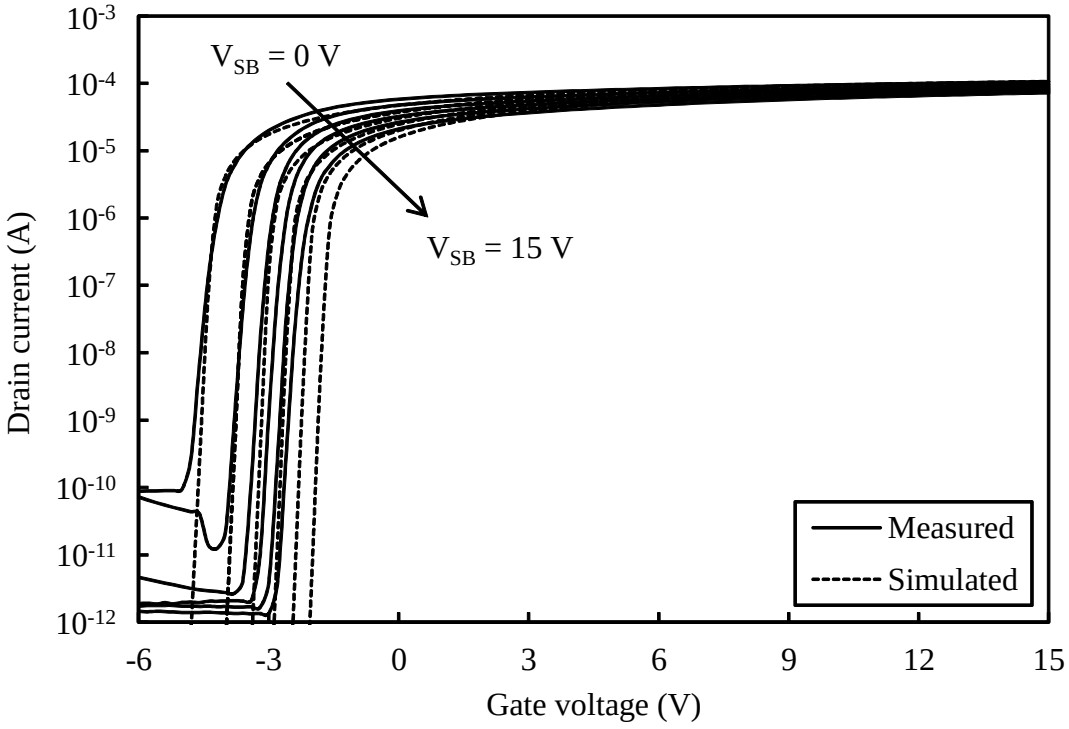


Fig. 4.10: Measured (solid) and simulated (dash) $I_D - V_{GS}$ characteristics of $32\mu m \times 2\mu m$ depletion MOSFET at 25 °C

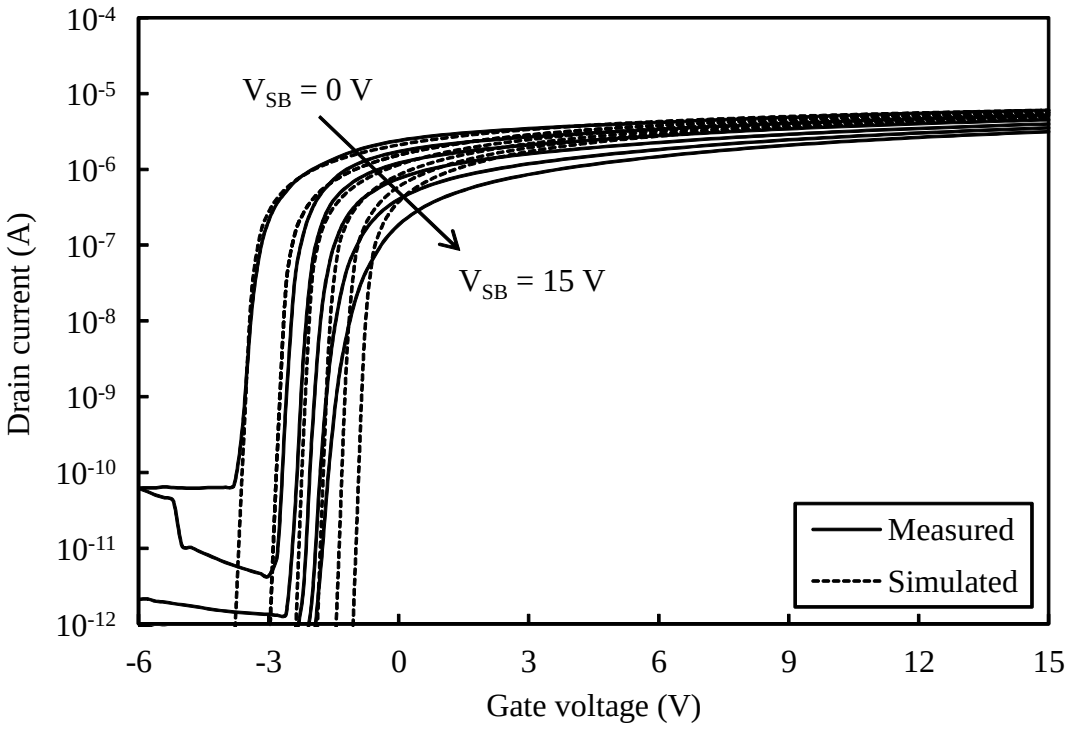


Fig. 4.11: Measured (solid) and simulated (dash) $I_D - V_{GS}$ characteristics of $8\mu m \times 8\mu m$ depletion MOSFET at 25 °C

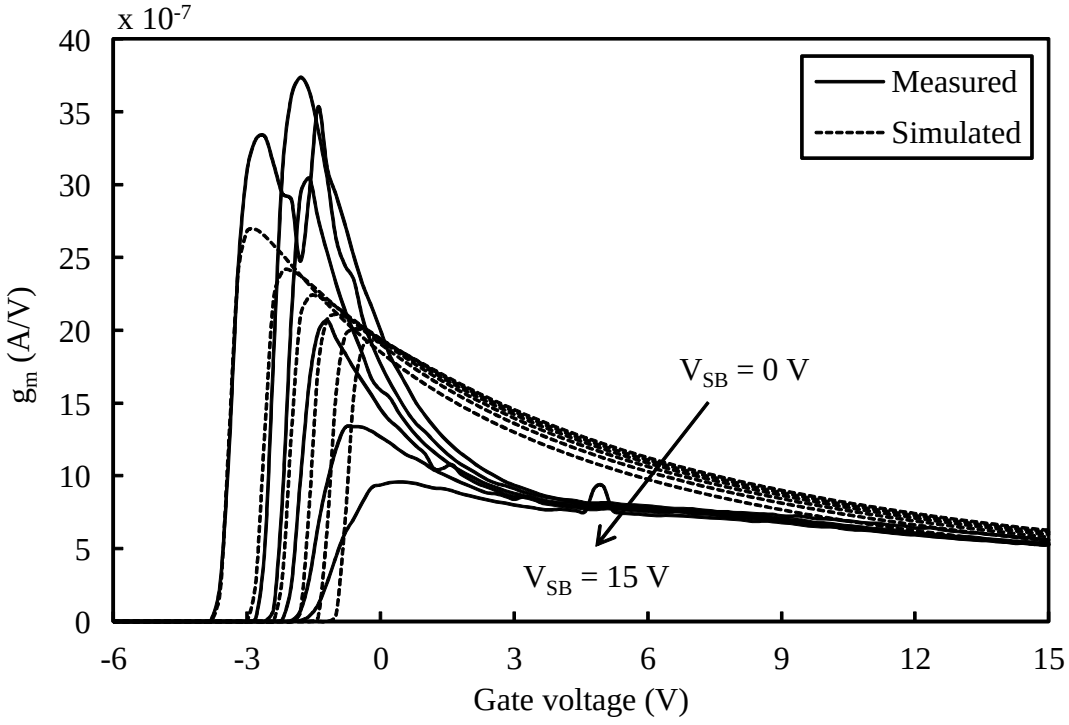


Fig. 4.12: Measured (solid) and simulated (dash) $g_m - V_{GS}$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET at 25 °C

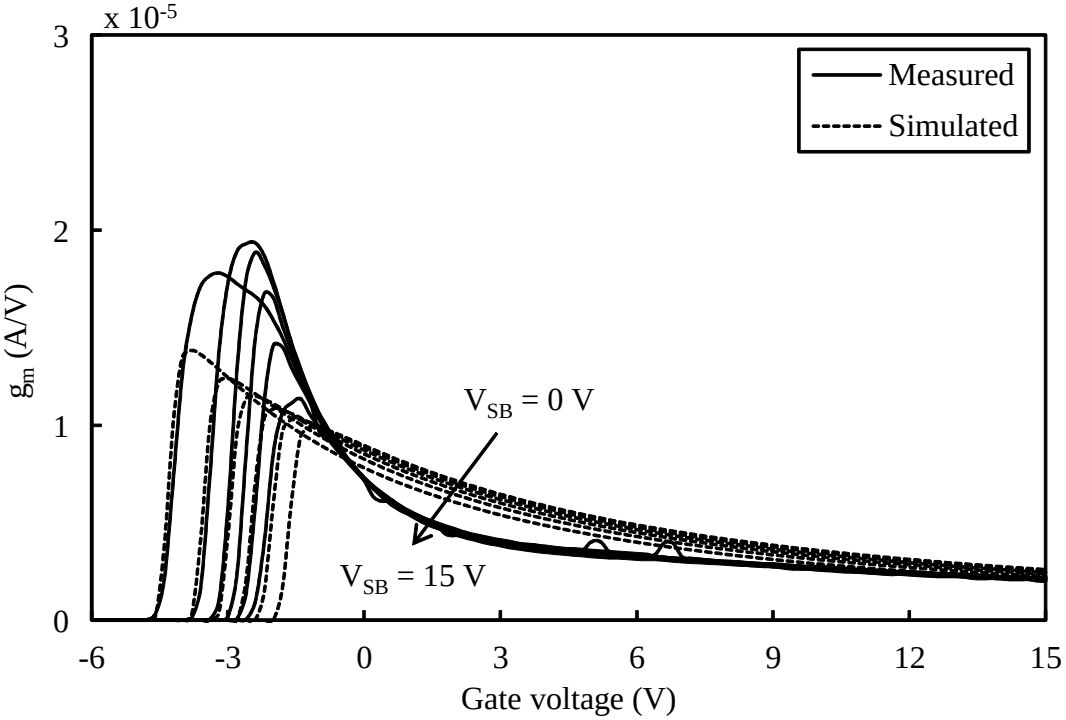


Fig. 4.13: Measured (solid) and simulated (dash) $g_m - V_{GS}$ characteristics of $32\mu m \times 2\mu m$ depletion MOSFET at 25 °C

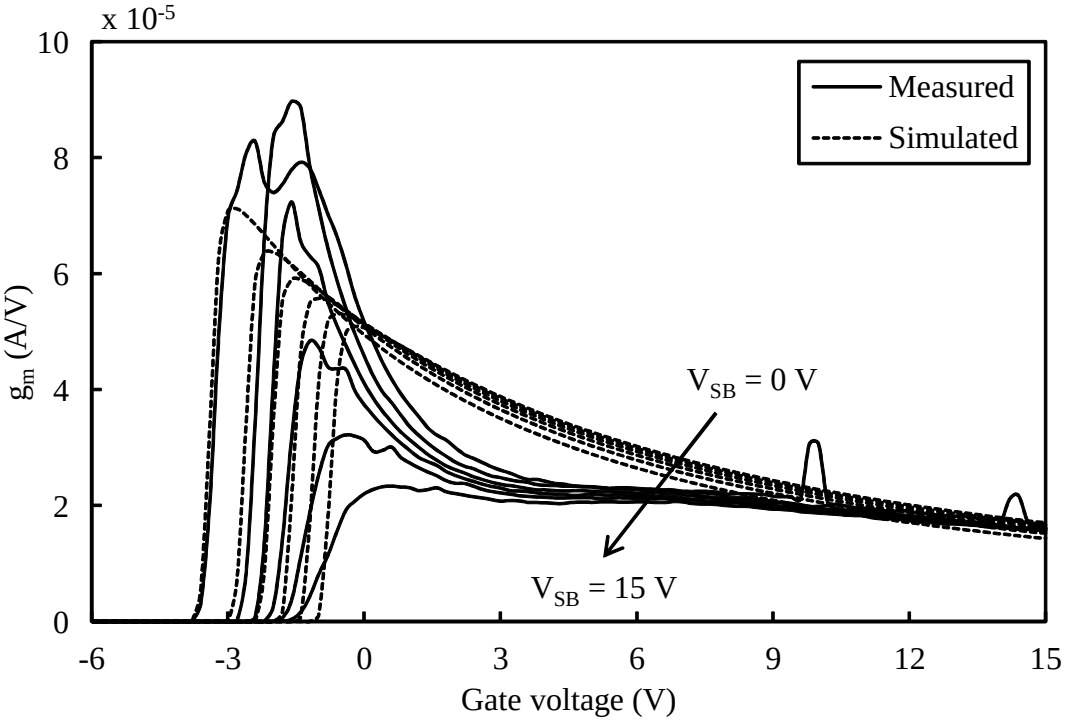


Fig. 4.14: Measured (solid) and simulated (dash) $g_m - V_{GS}$ characteristics of $8\mu m \times 8\mu m$ depletion MOSFET at 25 °C

4.4.3 Output Characteristics

The comparison between measurement and simulation of the output characteristics at room temperature of ($32\mu m \times 8\mu m$), ($32\mu m \times 2\mu m$) and ($8\mu m \times 8\mu m$) depletion MOSFETs is shown in Figs. 4.15 - 4.17 respectively. Mobility parameters **THEMU** and **MUE** were extracted using the output characteristics of the wide-long channel MOSFET. The short-channel MOSFET characteristics were used to extract **RS**. Simulated and measured output conductance for the three device sizes is shown in Figs. 4.18 - 4.20 respectively. Velocity saturation parameter **THESAT** was extracted using the $g_{DS} - V_{DS}$ characteristics. It can be seen that the longer channel lengths have a low g_{DS} and a relatively flat output characteristics at $V_{GS} = 0V$, where most of the depletion MOSFETs are operated. Thus, the long depletion MOSFETs are good current sources. The presence of channel length modulation (CLM) is seen in the output characteristics of the $32\mu m \times 2\mu m$ device, and is included in the model.

4.4.4 Geometry Scaling

Most of the parameters in the PSP model scale with length L and width W, and there are separate scaling parameters for length-scaling and width-scaling. When geometry scaling is ON in the model, the local parameter values are calculated using global parameters and the corresponding device length and width. Local values for all parameters are calculated using one form of a geometry scaling equation and geometry scaling parameters.

For the SiC process, in order to analyze the length scaling of the parameters, W was kept constant at $32\mu m$ and L was varied from $8\mu m$ to $2\mu m$. For width scaling, L was kept constant at $8\mu m$ and W was varied from $32\mu m$ to $8\mu m$.

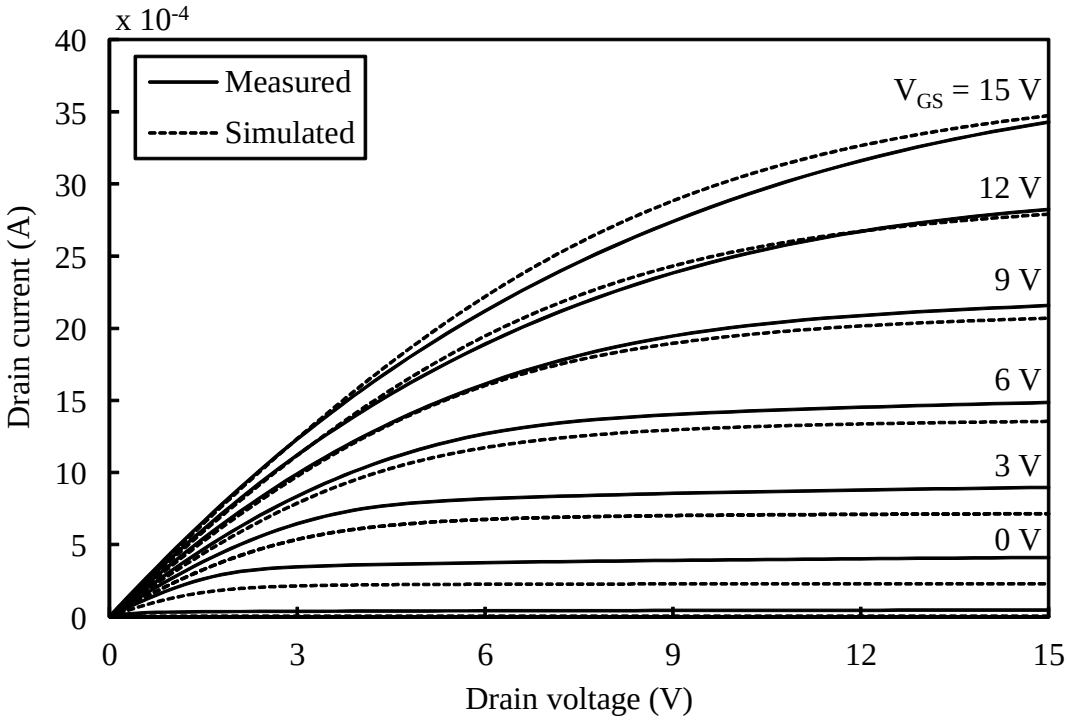


Fig. 4.15: Measured (solid) and simulated (dash) $I_D - V_{DS}$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET at 25 °C

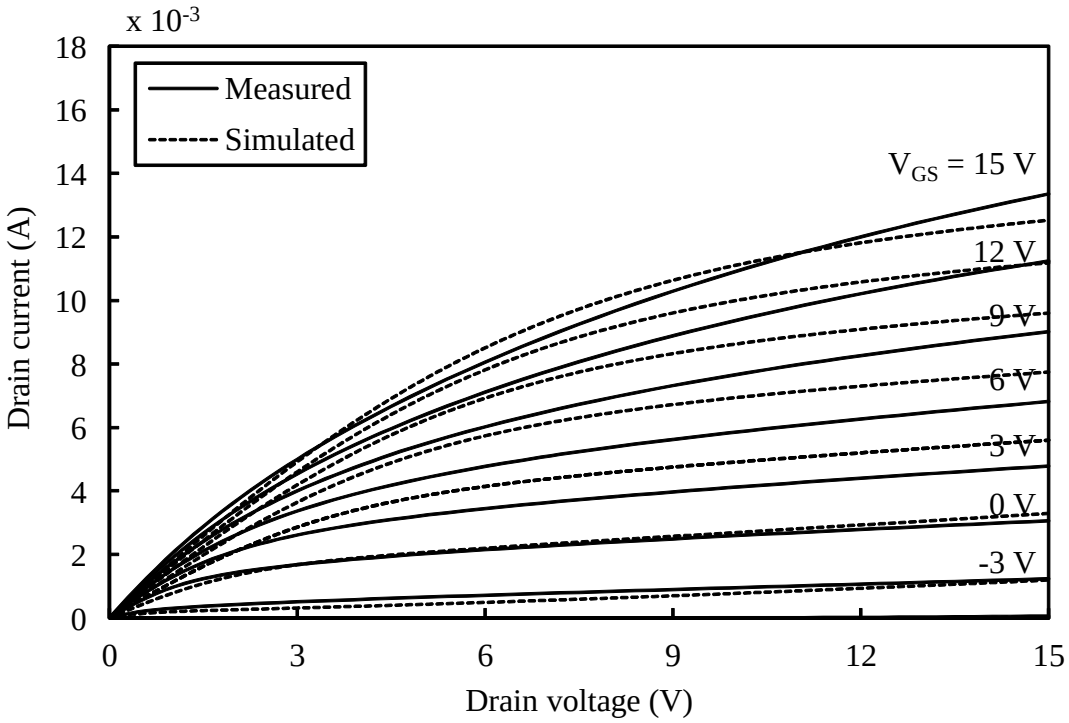


Fig. 4.16: Measured (solid) and simulated (dash) $I_D - V_{DS}$ characteristics of $32\mu m \times 2\mu m$ depletion MOSFET at 25 °C

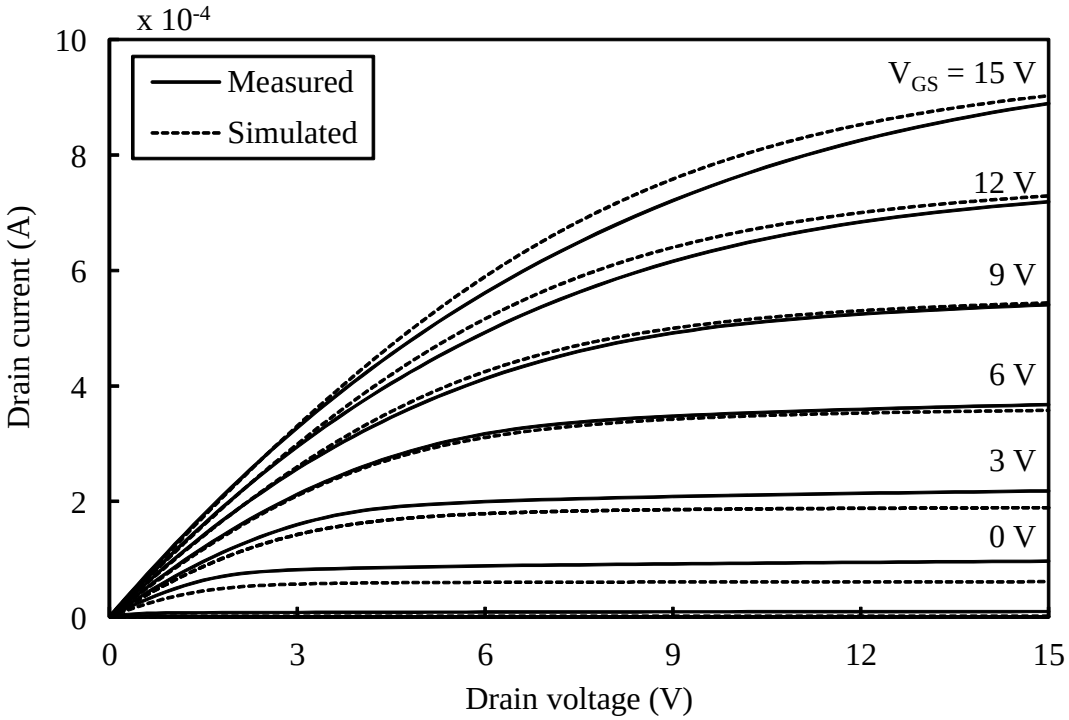


Fig. 4.17: Measured (solid) and simulated (dash) $I_D - V_{DS}$ characteristics of $8\mu m \times 8\mu m$ depletion MOSFET at 25 °C

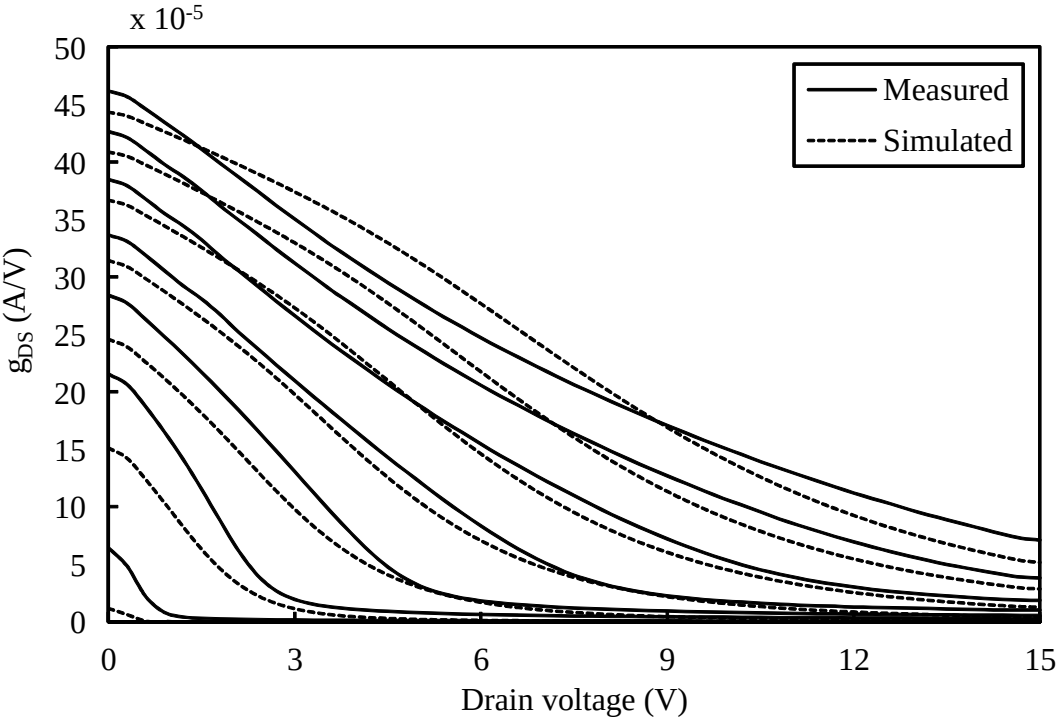


Fig. 4.18: Measured (solid) and simulated (dash) $g_{DS} - V_{GS}$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET at 25 °C

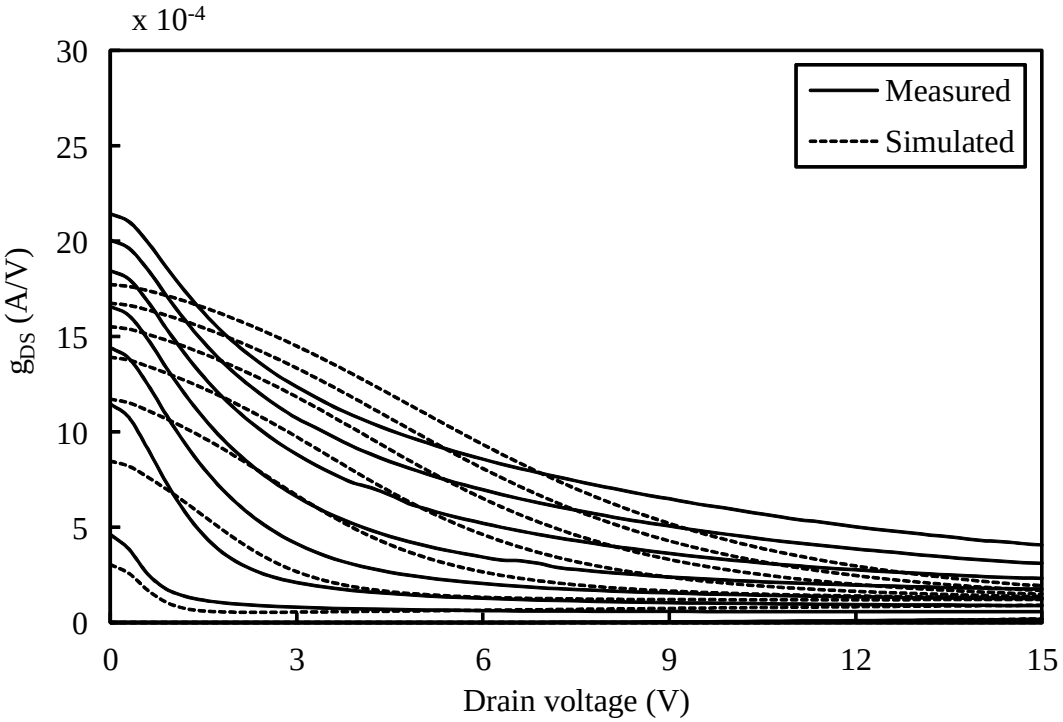


Fig. 4.19: Measured (solid) and simulated (dash) $g_{DS} - V_{GS}$ characteristics of $32\mu m \times 2\mu m$ depletion MOSFET at 25 °C

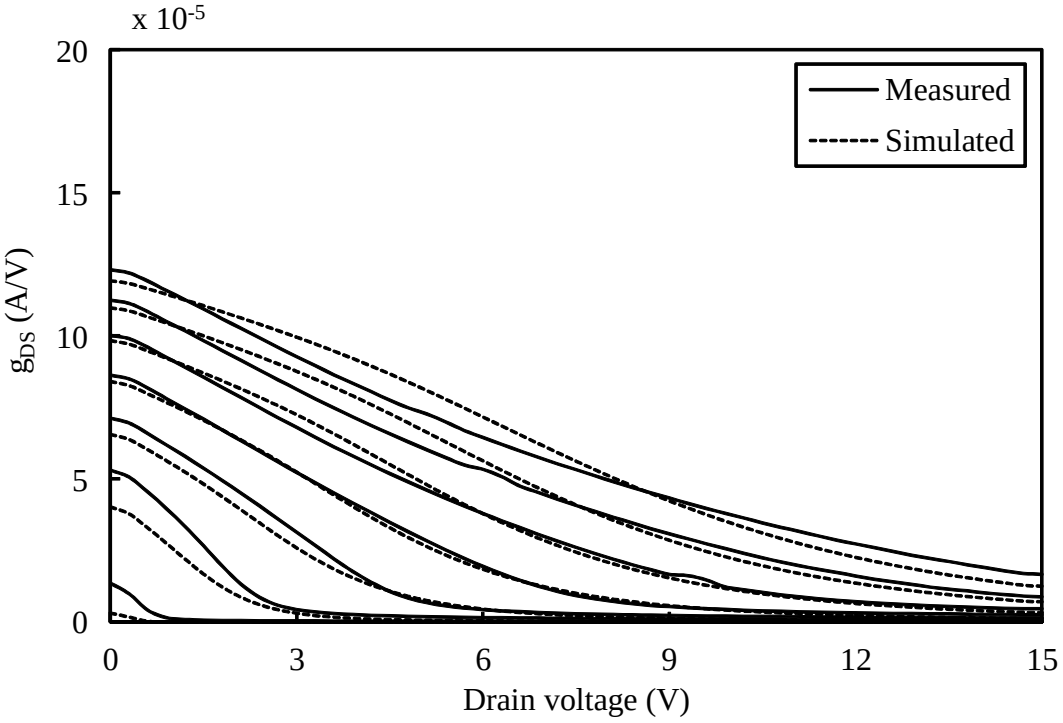


Fig. 4.20: Measured (solid) and simulated (dash) $g_{DS} - V_{GS}$ characteristics of $8\mu m \times 8\mu m$ depletion MOSFET at 25 °C

Before the extraction of geometry scaling parameters, values of ΔL and ΔW were extracted using the geometry scaling of **BETN** [91]. Fig. 4.21 shows the variation of **BETN** with L and W. ΔL was calculated to be $0.23\mu m$ from the extrapolated zero-crossing of 1/**BETN** versus L and ΔW was calculated to be $0.0013\mu m$ from the extrapolated zero-crossing of **BETN** versus W. The calculated values of ΔL and ΔW were used to calculate internal values for L_E and W_E according to

$$L_E = L - \Delta L \tag{4.63}$$

$$W_E = W - \Delta W \tag{4.64}$$

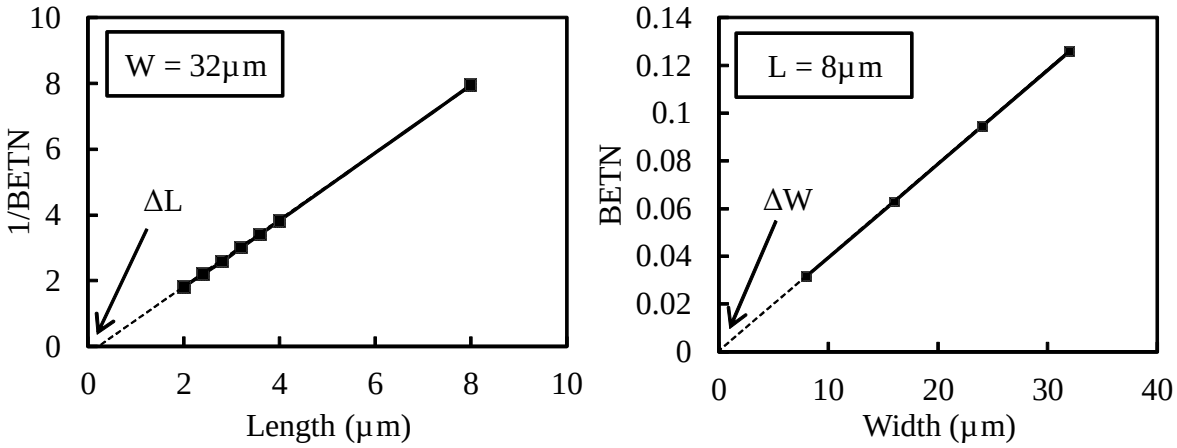


Fig. 4.21: Extraction of ΔL and ΔW from **BETN**

Using the local parameters extracted for various values of W and L as described in section 3.1.1, the variation of the parameters was seen with W and L. Using the same data, the geometry scaling parameters for **BETN** were extracted. **BETN** scales with geometry as

$$\mathbf{BETN} = \frac{\mathbf{UO}}{G_{P,E}} \cdot \frac{W_E}{L_E} \cdot G_{W,E} \tag{4.65}$$

where **UO** is the zero-field mobility, $G_{P,E}$ and $G_{P,E}$ are set to 1. A single value of **UO** satisfies both the width and length scaling for **BETN** if the values of ΔL and ΔW were accurately extracted in the last step. The value of **UO** was calculated to be 0.0305.

Fig. 4.22 shows the length scaling of **VFB**. The geometry scaling parameters for **VFB** were extracted according to the following scaling rule

$$\mathbf{VFB} = \mathbf{VFBO} + \mathbf{VFBL}\,\frac{L_{EN}}{L_E} + \mathbf{VFBW}\,\frac{W_{EN}}{W_E} + \mathbf{VFBLW}\,\frac{W_{EN}\,L_{EN}}{W_E\,L_E} \tag{4.66}$$

where L_{EN} and W_{EN} are reference lengths and widths and equal to $1\mu m$, **VFB** is the local parameter value, **VFBO** is the geometry independent global value, **VFBL** is the length-scaling global value, **VFBW** is the width-scaling global value and **VFBLW** is the length and width scaling global value. The extracted value of **VFBO** was -9 and that of **VFBL** was -2.2. No variation of **VFB** was observed with width, and **VFBW** and **VFBLW** were set to 0.

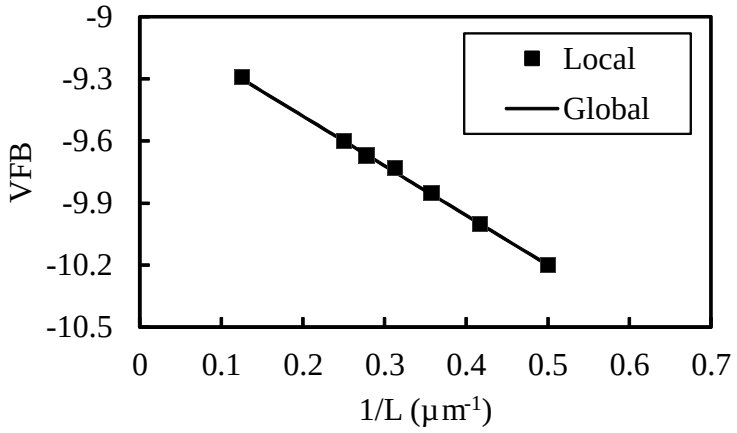


Fig. 4.22: Variation of **VFB** with 1/L

The variation of saturation velocity parameter **THESAT** with L is shown in Fig. 4.23. The

geometry scaling for **THESAT** is given as

$$\mathbf{THESAT} = \left(\mathbf{THESATO} + \mathbf{THESATL}.\frac{G_{W,E}}{G_{P,E}}.\left[\frac{L_{EN}}{L_E}\right]^{\mathbf{THESATLEXP}} \right) . \left(1 + \mathbf{THESATW}.\frac{W_{EN}}{W_E}\right) . \left(1 + \mathbf{THESATLW}.\frac{W_{EN}.L_{EN}}{W_E.L_E}\right) \tag{4.67}$$

where the parameter naming convention is the same as in the case of **VFB**. The calculated value of **THESATO** was -0.604, value of **THESATL** was 0.7 and the value of **THESATLEXP** was 0.055. The variation of **THESAT** with width was negligible, and was not used by setting **THESATW** and **THESATLW** to 0. The length scaling of DIBL parameter **CF** is shown in Fig. 4.24. The length

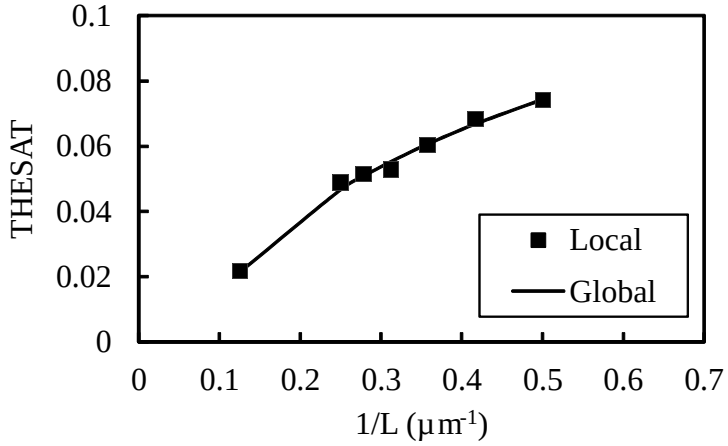


Fig. 4.23: Variation of **THESAT** with 1/L

variation for **CF** is given by

$$\mathbf{CF} = \mathbf{CFL}.\left[\frac{L_{EN}}{L_E}\right]^{\mathbf{CFLEXP}} . \left(1 + \mathbf{CFW}.\frac{W_{EN}}{W_E}\right) \tag{4.68}$$

It can be seen that the DIBL parameter increased with 1/L as expected. Due to a large drain-source voltage of 20 V in the SiC MOSFETs, the DIBL effect was seen at channel lengths of $2\mu m$. The

calculated values of **CFL**, **CFLEXP** and **CFW** were 0.25, 0.9 and 0 respectively.

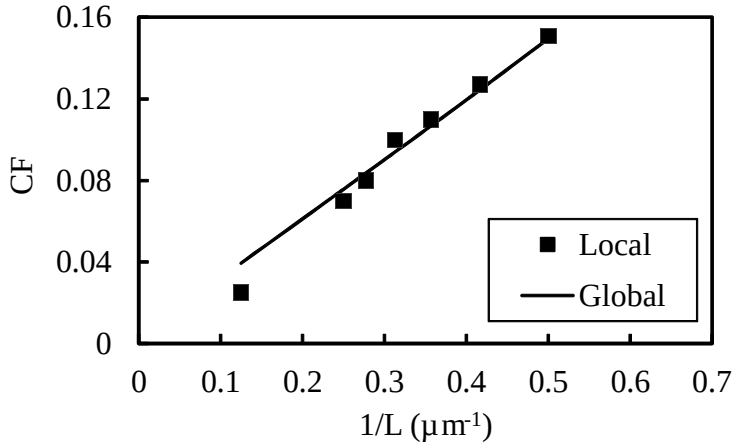


Fig. 4.24: Variation of **CF** with 1/L

4.4.5 Temperature Scaling

Temperature scaling rules affect the calculation of the local parameters in the same way as geometry scaling rules. Temperature scaling rules are calculated based on the difference between simulation temperature and reference temperature (which is in most cases 25 °C). A thorough approach to extract a full geometry and temperature scaled model is to perform geometry scaling at several temperature points, and then derive temperature scaling parameters for every global parameter *and* their geometry scaling parameters as well. For example, for the flat-band voltage parameter **VFB**, one would need to extract values for every device size at each temperature point. Then, the temperature scaling parameters for **VFB** and its scaling parameters **VFBL**, **VFBW** and **VFBLW** must be extracted using the temperature data. While this procedure is thorough, it involves a 2-dimensional scaling problem (with geometry and temperature). As a result, this approach has not been used for temperature scaling in this process.

Instead, the temperature and geometry scaling aspects have been partitioned and assumed in-

dependent of each other. In other words, geometry scaling parameters have been extracted in the usual way at room temperature, and then temperature scaling parameters for the large device has been extracted, assuming the geometry scaling holds over temperature. While this assumption is incorrect, it introduces error within tolerable limits and lessens the burden of a thorough parameter extraction which is time consuming, and outside the scope of this dissertation. Once the temperature scaling parameters have been extracted, the resultant temperature and geometry scaled model has been tested for the narrow-long and wide-short devices, and it has been shown that the error introduced by the simplification of parameter extraction is within tolerance.

Temperature scaling was done using three temperature points of 25°C, 125°C and 225°C. This section presents the temperature scaling of the large $32\mu m \times 8\mu m$ depletion MOSFET. Fig. 4.25 shows the comparison between measurement and simulation of the input characteristics over temperature. The threshold voltage can be seen to decrease with increasing temperature as expected, and the on-state resistance increases. Figs. 4.26 and 4.27 show the output characteristics for the same device at 125 °C and 225 °C respectively.

Temperature scaling for **BETN** is given as

$$BETN_T = \mathbf{BETN} \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{\mathbf{STBET}} \tag{4.69}$$

where $BETN_T$ is the temperature scaled local value of **BETN** for a given temperature, **STBET** is the temperature scaling parameter for **BETN**, T_{KR} is the reference temperature in Kelvin scale and T_{KD} is the ambient temperature in Kelvin scale. Using the extracted local values for **BETN** over temperature, the value of **STBET** was calculated to be 2.6. The temperature scaling of **BETN** is shown in Fig. 4.28.

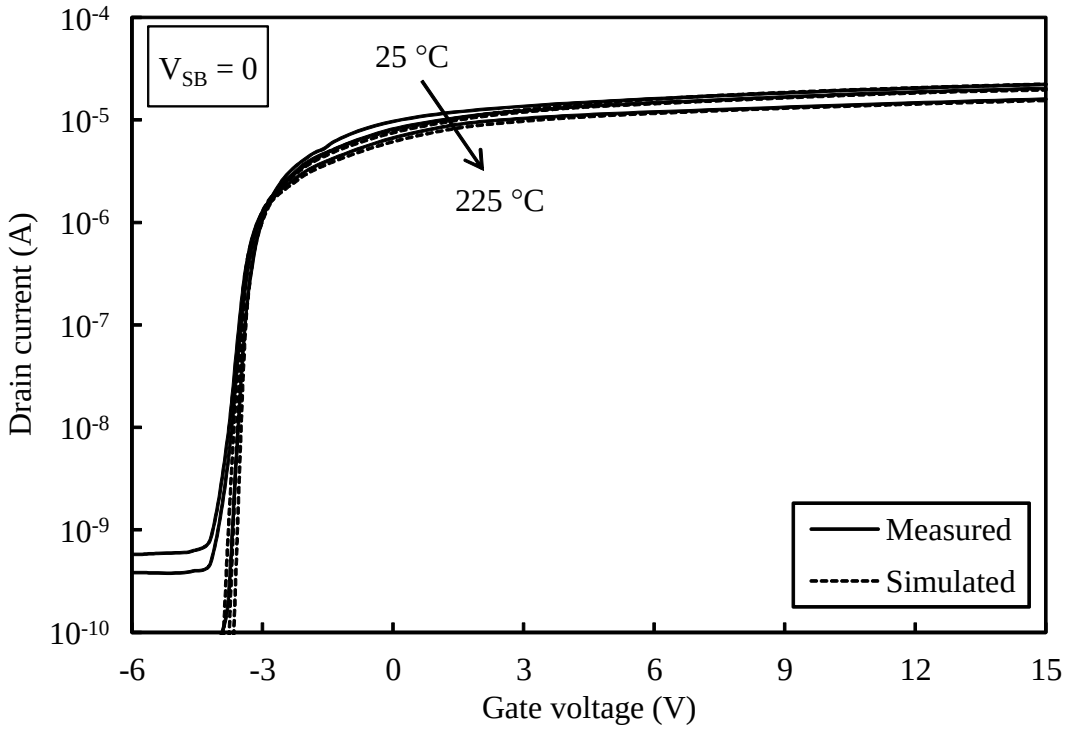


Fig. 4.25: Measured (solid) and simulated (dash) $I_D - V_{GS}$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET over temperature

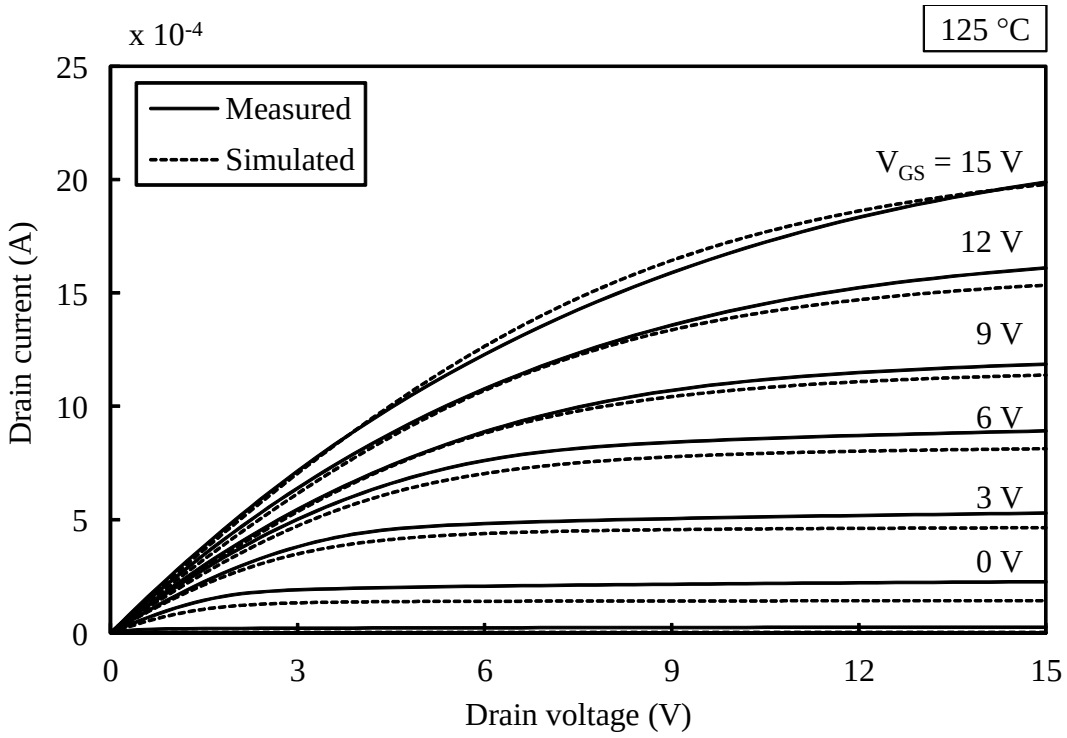


Fig. 4.26: Measured (solid) and simulated (dash) $I_D - V_{DS}$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET at 125 °C

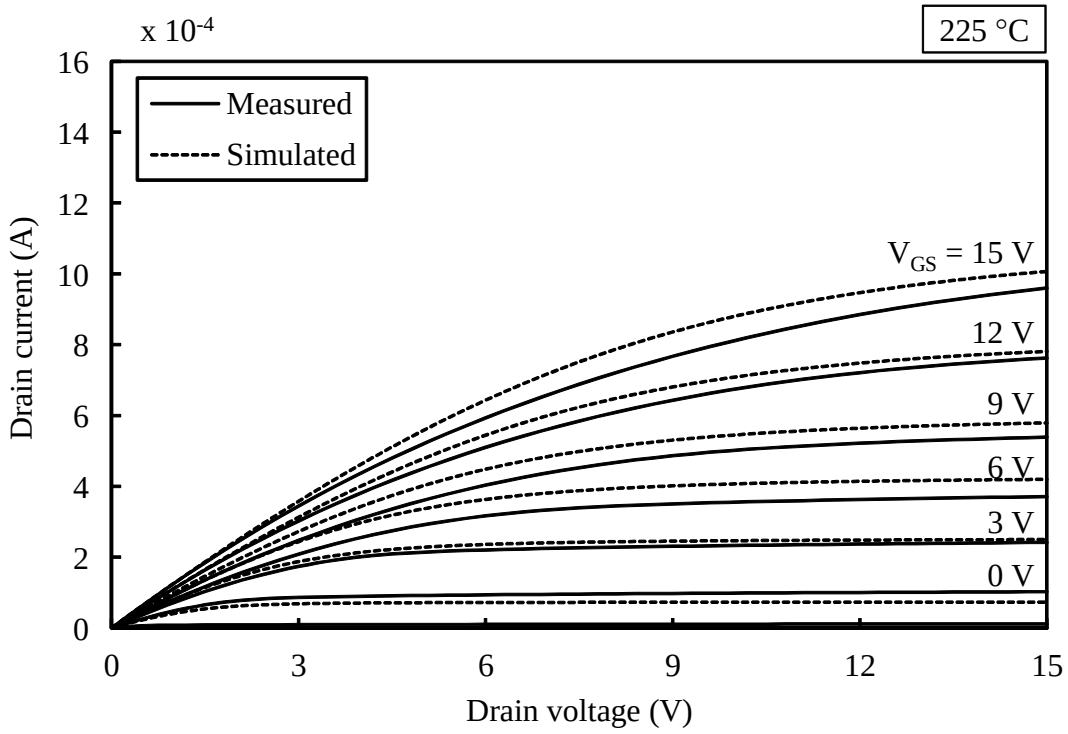


Fig. 4.27: Measured (solid) and simulated (dash) $I_D - V_{DS}$ characteristics of $32\mu m \times 8\mu m$ depletion MOSFET at 225 °C

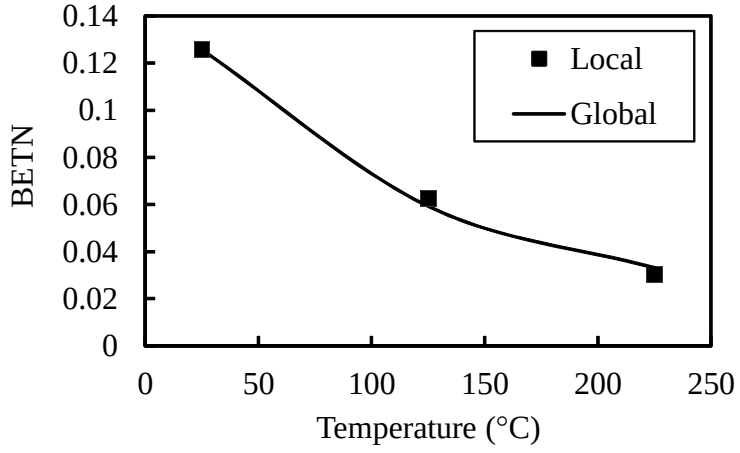


Fig. 4.28: Temperature scaling of **BETN** for the $32\mu m \times 8\mu m$ depletion MOSFET

VFB is scaled with temperature as

$$VFB_T = \mathbf{VFB} + (T_{KD} - T_{KR}) \ . \ \mathbf{STBET} \tag{4.70}$$

The variation of **VFB** with temperature is shown in Fig. 4.29. The extracted value of **STVFB** from temperature variation of **VFB** was -1.95×10^{-3}.

The temperature scaling of **THEMU** is given as

$$THEMU_T = \mathbf{THEMU} \ . \ \left(\frac{T_{KR}}{T_{KD}}\right)^{\mathbf{STTHEMU}} \tag{4.71}$$

where **STTHEMU** is the temperature scaling parameter for **THEMU**. The variation of **THEMU** with temperature is shown in Fig. 4.30. The calculated value of **STTHEMU** was 1.9.

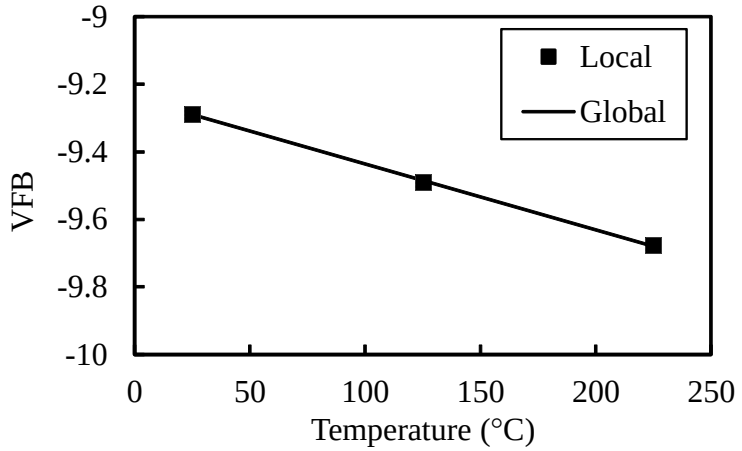


Fig. 4.29: Temperature scaling of **VFB** for the $32\mu m \times 8\mu m$ depletion MOSFET

Once the temperature scaling parameters were extracted for the $32\mu m \times 8\mu m$ depletion MOSFET, using the temperature and geometry scaling equations, performance for other device sizes can be predicted. A complete extracted parameter list is given in Table 4.7 at the end of this chapter.

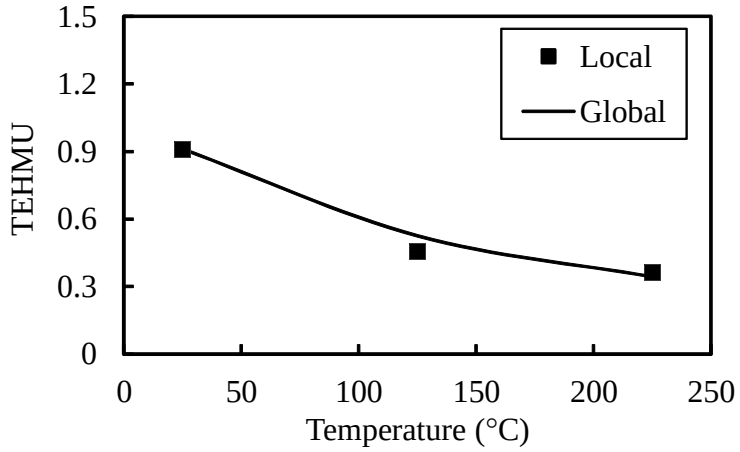


Fig. 4.30: Temperature scaling of **THEMU** for the $32\mu m \times 8\mu m$ depletion MOSFET

4.5 Enhancement MOSFET Model Performance

The performance of the SiC PSP model for enhancement MOSFETs has been presented in the same way as for depletion MOSFETs. Parameters for enhancement MOSFETs were extracted using characterization data over temperature as shown in section 3.5. During characterization, it was found that the $32\mu m \times 8\mu m$ enhancement MOSFET had a damaged gate-oxide. Since the characterization was done for several devices in with scripted macros, the problem of gate-oxide leakage was discovered after all the device data was taken. As a result, the $16\mu m \times 8\mu m$ enhancement MOSFET has been used instead of the $32\mu m \times 8\mu m$ as the large device in parameter extraction.

First, the performance of the SiC PSP model for the wide-long ($16\mu m \times 8\mu m$), wide-short ($32\mu m \times 2\mu m$) and narrow-long ($8\mu m \times 8\mu m$) depletion MOSFETs at room temperature has been presented. Next, the geometry scaling of the various model parameters have been shown. Finally, the performance of the 3 corner devices has been shown at 125 °C and 225 °C.

4.5.1 Gate Capacitance

The characterization setup for gate capacitance $C_{GG} - V_G$ measurement has been described in section 3.5.1. Fig. 4.31 shows the simulated SiC PSP model for the $32\mu m \times 8\mu m$ enhancement MOSFET. Parameter **TOX** was set to 40 nm. Initial values for **VFB**, **NEFF**, **DPHIB**, **NP** and **COX** were extracted. Good agreement was observed between the simulation and measurements.

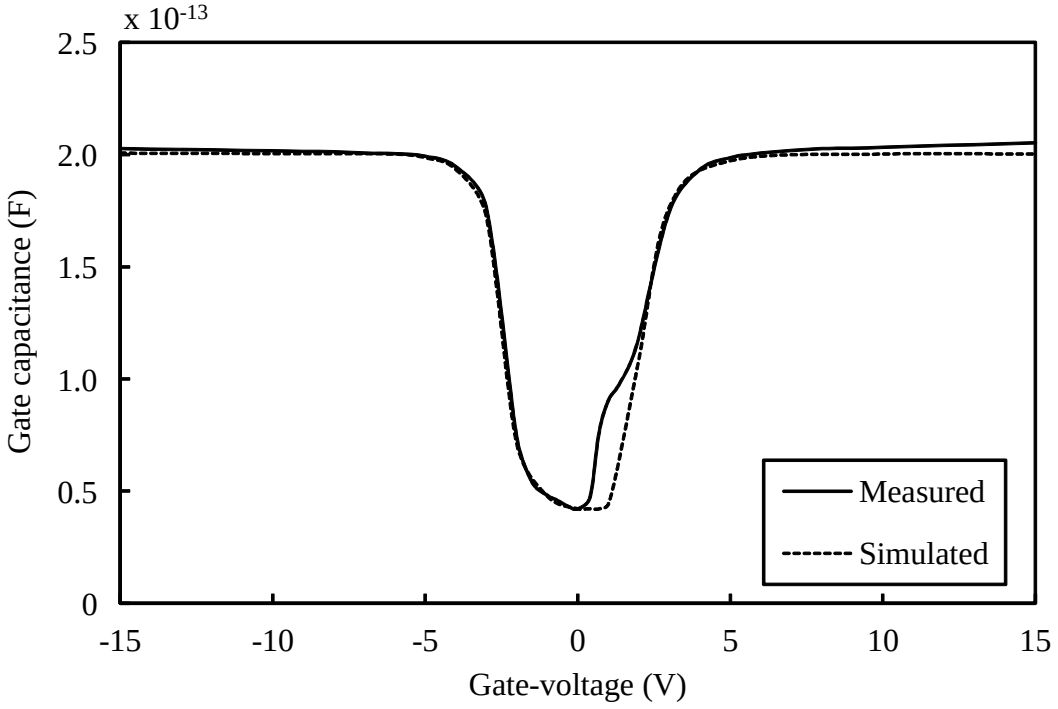


Fig. 4.31: Measured (solid) and simulated (dash) $C_{GG} - V_G$ characteristics of $32\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

4.5.2 Input Characteristics

The comparison between measurement and simulation of the input characteristics at room temperature of ($16\mu m \times 8\mu m$), ($32\mu m \times 2\mu m$) and ($8\mu m \times 8\mu m$) enhancement MOSFETs is shown in Figs. 4.32 - 4.34 respectively. **NEFF** and **DPHIB** were re-optimized using the $I_D - V_{GS}$ characteristics. Values for **BETN**, **MUE**, **THEMU**, **CT**, **XCOR** were also extracted. The input char-

acteristics were modeled well by accurately extracting the Coulumbic scattering parameter **CS**, which describes the gradual transition from weak inversion to strong inversion due to scattering from trapped electrons in interface states. The derived transconductance ($g_m - V_{GS}$) characteristics for the three devices are shown in Figs. 4.35 - 4.37 respectively.

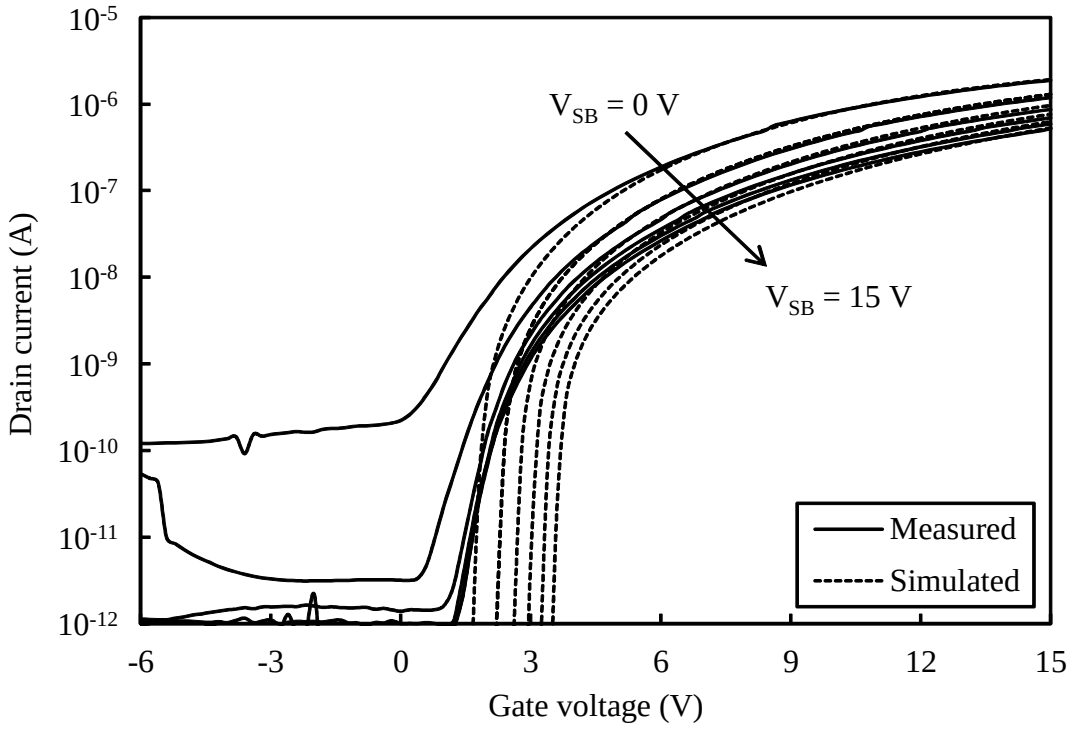


Fig. 4.32: Measured (solid) and simulated (dash) $I_D - V_{GS}$ characteristics of $16\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

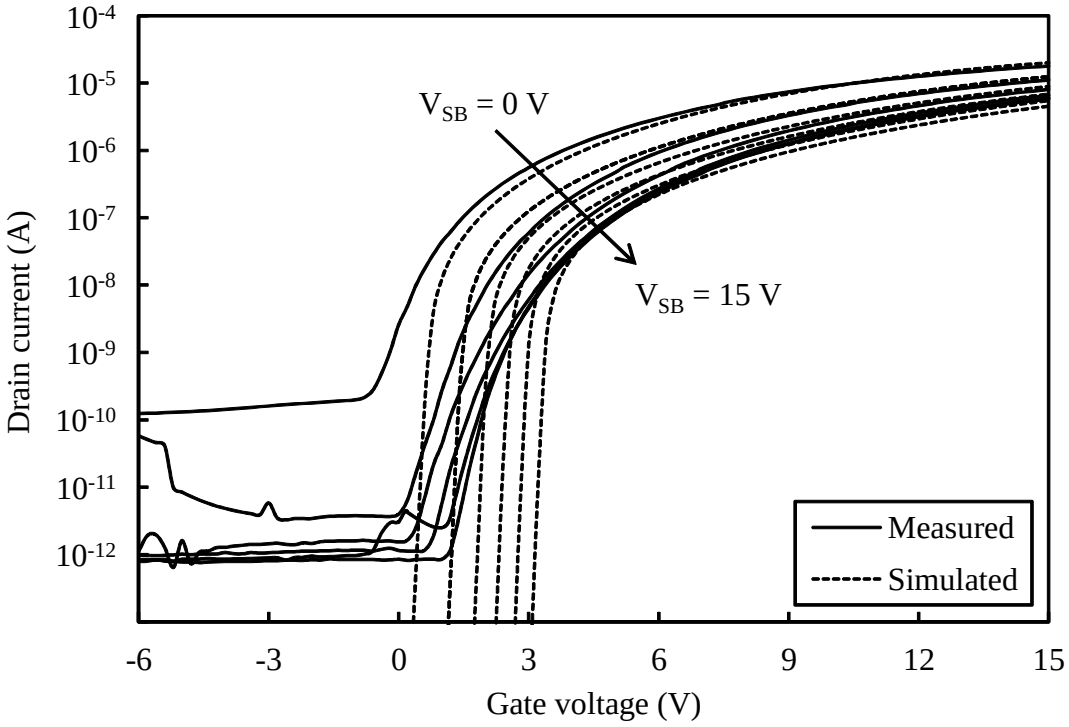


Fig. 4.33: Measured (solid) and simulated (dash) $I_D - V_{GS}$ characteristics of $32\mu m \times 2\mu m$ enhancement MOSFET at 25 °C

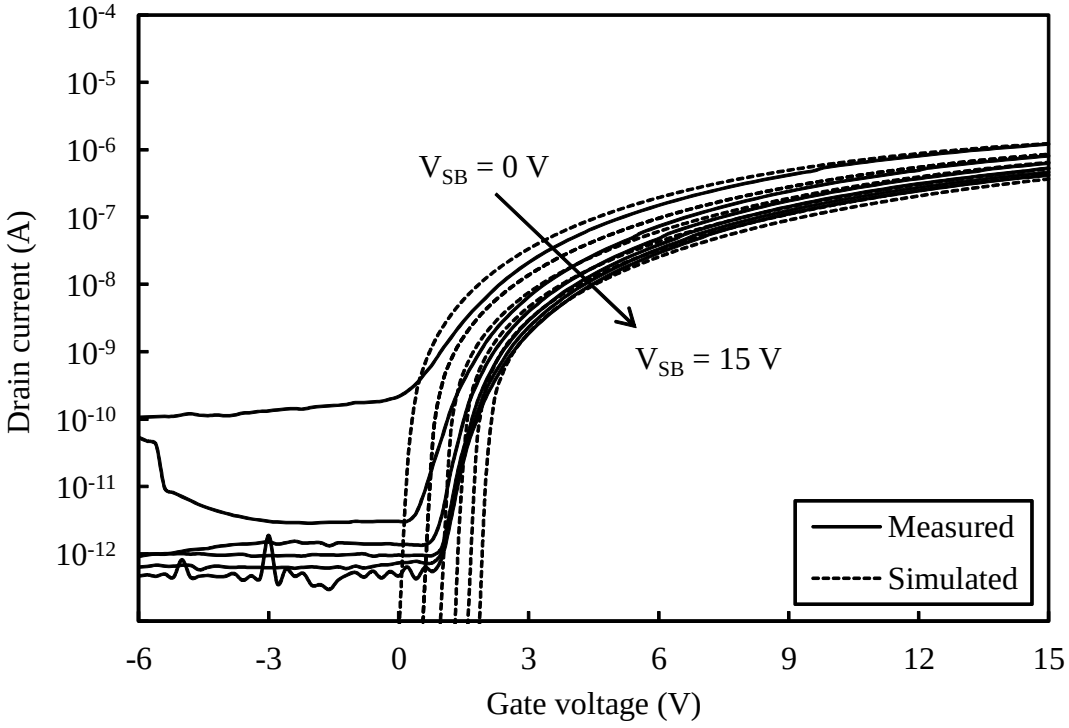


Fig. 4.34: Measured (solid) and simulated (dash) $I_D - V_{GS}$ characteristics of $8\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

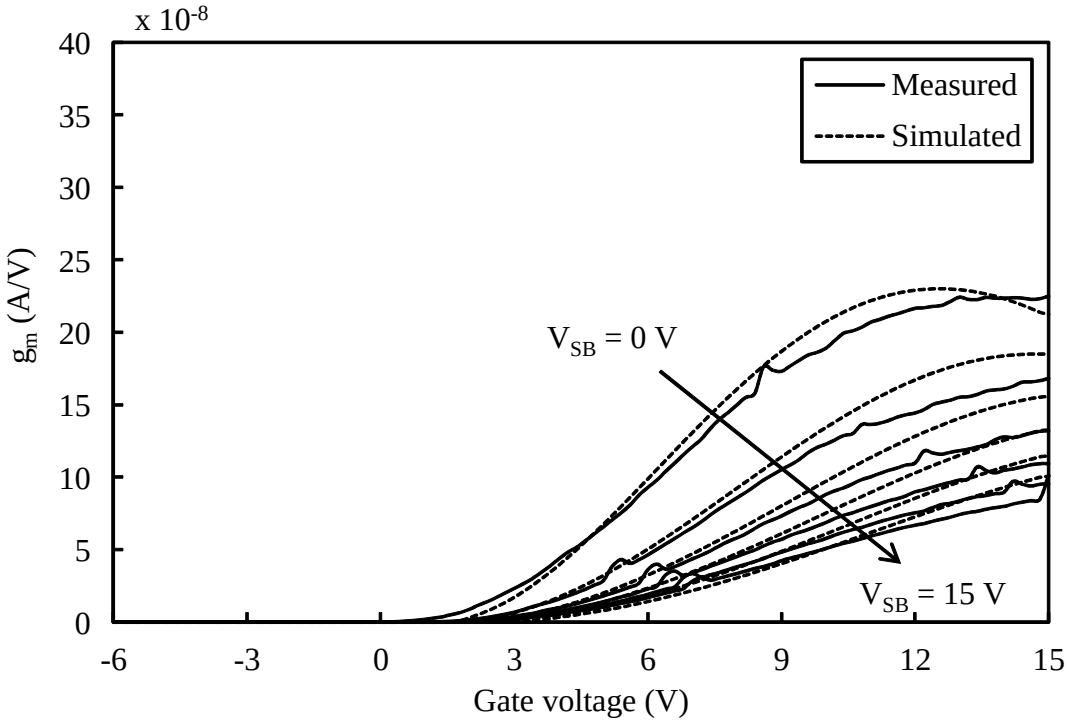


Fig. 4.35: Measured (solid) and simulated (dash) $g_m - V_{GS}$ characteristics of $16\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

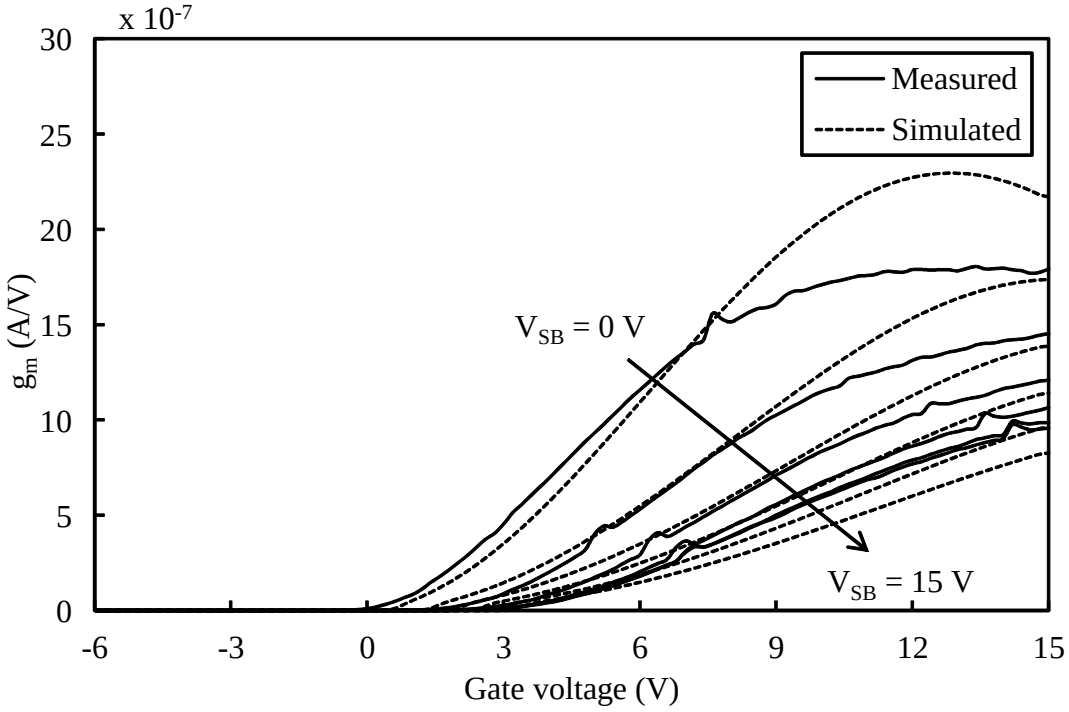


Fig. 4.36: Measured (solid) and simulated (dash) $g_m - V_{GS}$ characteristics of $32\mu m \times 2\mu m$ enhancement MOSFET at 25 °C

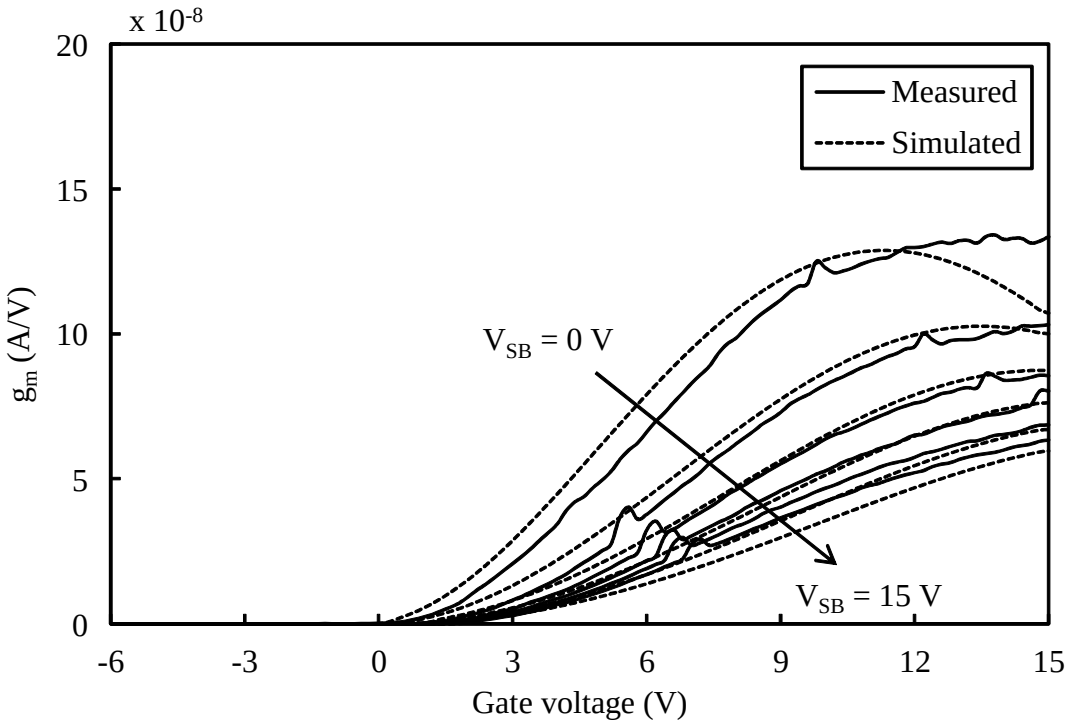


Fig. 4.37: Measured (solid) and simulated (dash) $g_m - V_{GS}$ characteristics of $8\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

4.5.3 Output Characteristics

The comparison between measurement and simulation of the output characteristics at room temperature of $16\mu m \times 8\mu m$, $32\mu m \times 2\mu m$ and $8\mu m \times 8\mu m$ enhancement MOSFETs is shown in Figs. 4.38 - 4.40 respectively. Mobility parameters **THEMU** and **MUE** were extracted using the output characteristics of the wide-long channel MOSFET. The short-channel MOSFET characteristics were used to extract **RS**. Simulated and measured output conductance for the three device sizes is shown in Figs. 4.41 - 4.43 respectively. Velocity saturation parameter **THESAT** was extracted using the $g_{DS} - V_{DS}$ characteristics. Long-channel enhancement MOSFETs exhibited a high value of R_{ON}, and made them suitable in current matching applications. The presence of channel length modulation (CLM) is seen in the output characteristics of the $32\mu m \times 2\mu m$ device, and is included in the model.

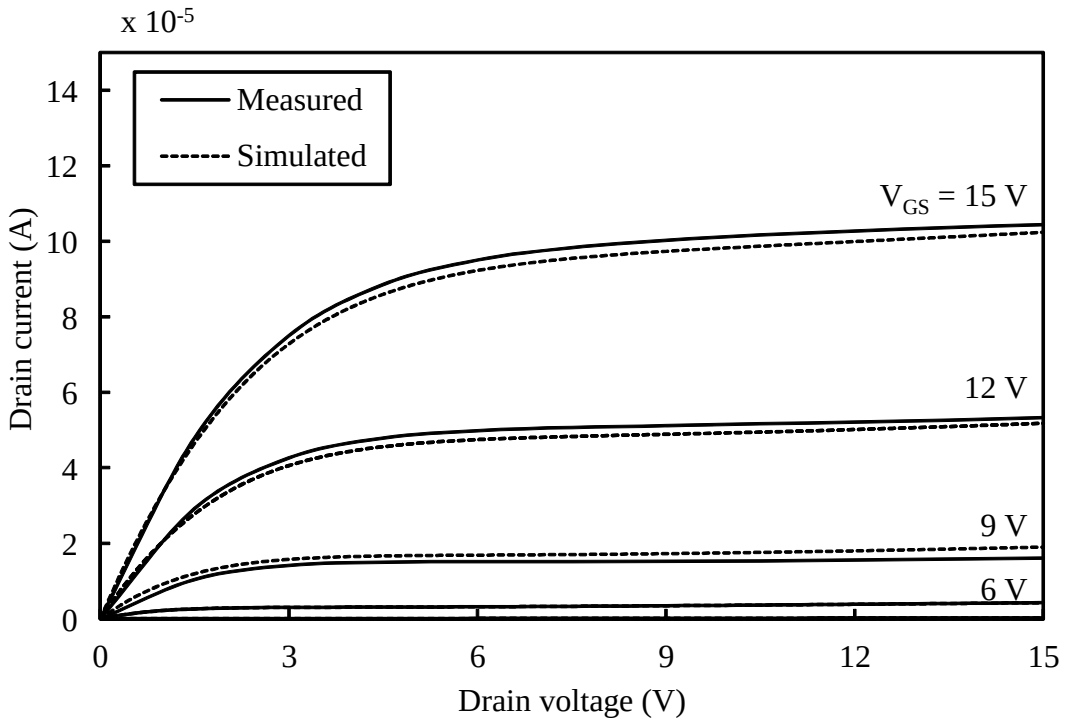


Fig. 4.38: Measured (solid) and simulated (dash) $I_D - V_{DS}$ characteristics of $16\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

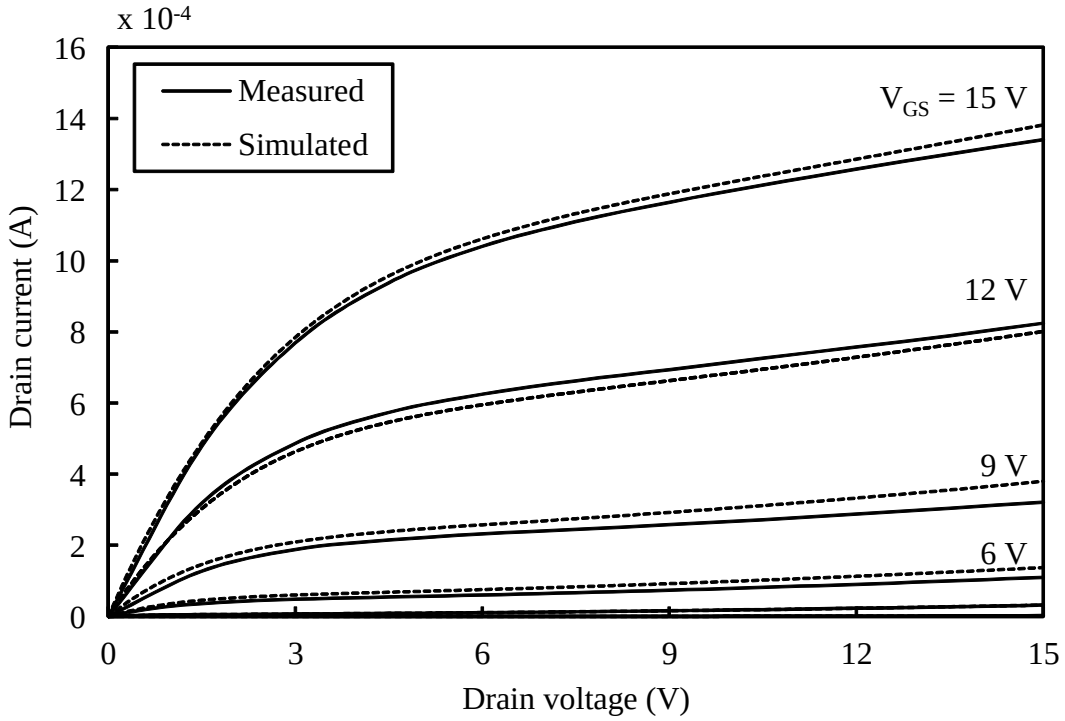


Fig. 4.39: Measured (solid) and simulated (dash) $I_D - V_{DS}$ characteristics of $32\mu m \times 2\mu m$ enhancement MOSFET at 25 °C

4.5.4 Geometry Scaling

For sake of brevity, only the results of geometry scaling for enhancement MOSFETs has been presented in this section. The detailed derivation and procedure of determining geometry scaling has been described in section 4.4.4. Since the largest device size available for enhancement MOSFETs was $16\mu m \times 8\mu m$, in order to determine length scaling of the parameters, devices with width $32\mu m$ and lengths 2, 2.4, 2.8, 3.2, 3.6 and $4\mu m$ were used. For width scaling, three device widths of $24\mu m$, $16\mu m$ and $8\mu m$ were used. The quality of model fits to the measurement lend confidence in the geometry scaling performance of the global model.

The geometry scaling parameter extraction began with the extraction of ΔL and ΔW using **BETN**. The variation of **BETN** with L and W for enhancement MOSFETs is shown in Fig. 4.44.

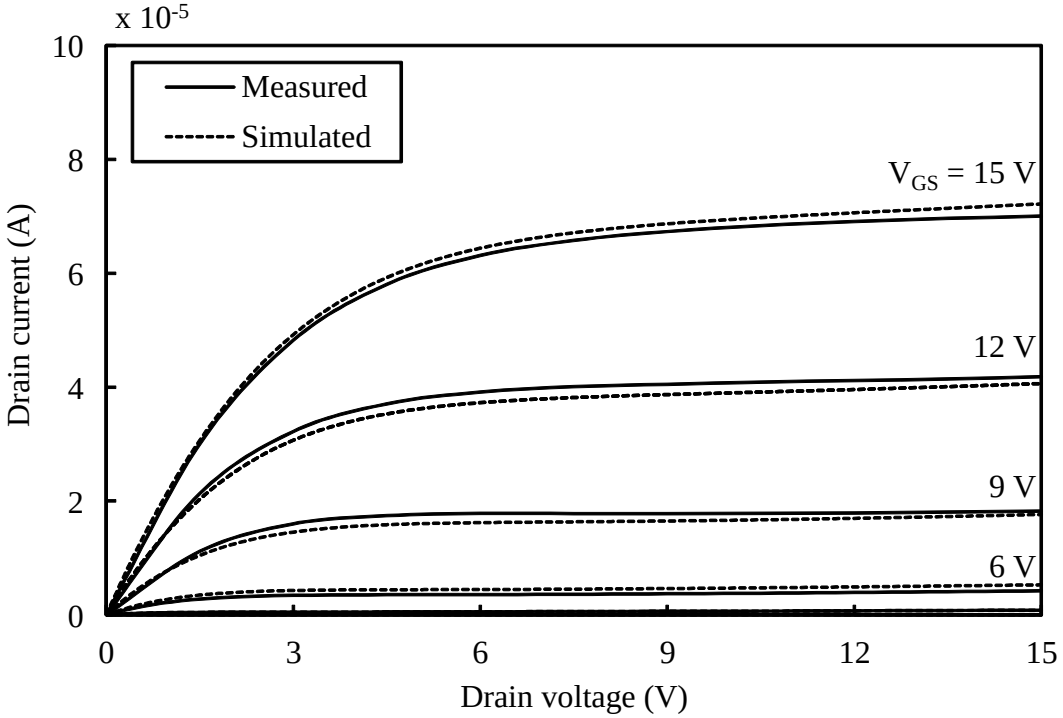


Fig. 4.40: Measured (solid) and simulated (dash) $I_D - V_{DS}$ characteristics of $8\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

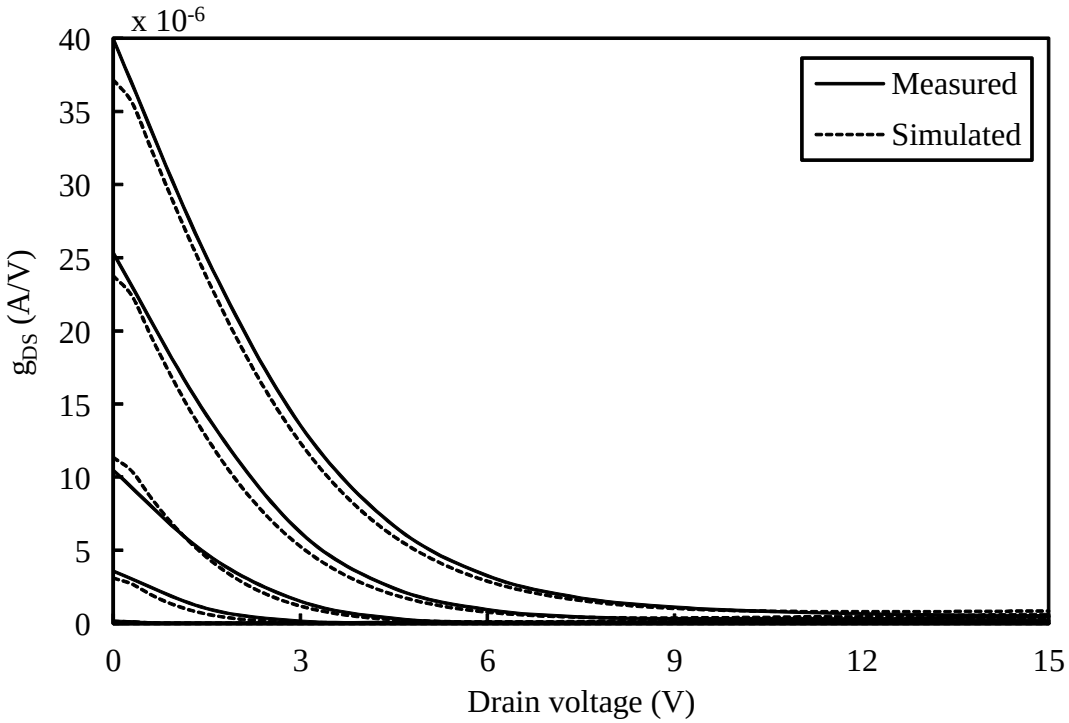


Fig. 4.41: Measured (solid) and simulated (dash) $g_{DS} - V_{GS}$ characteristics of $16\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

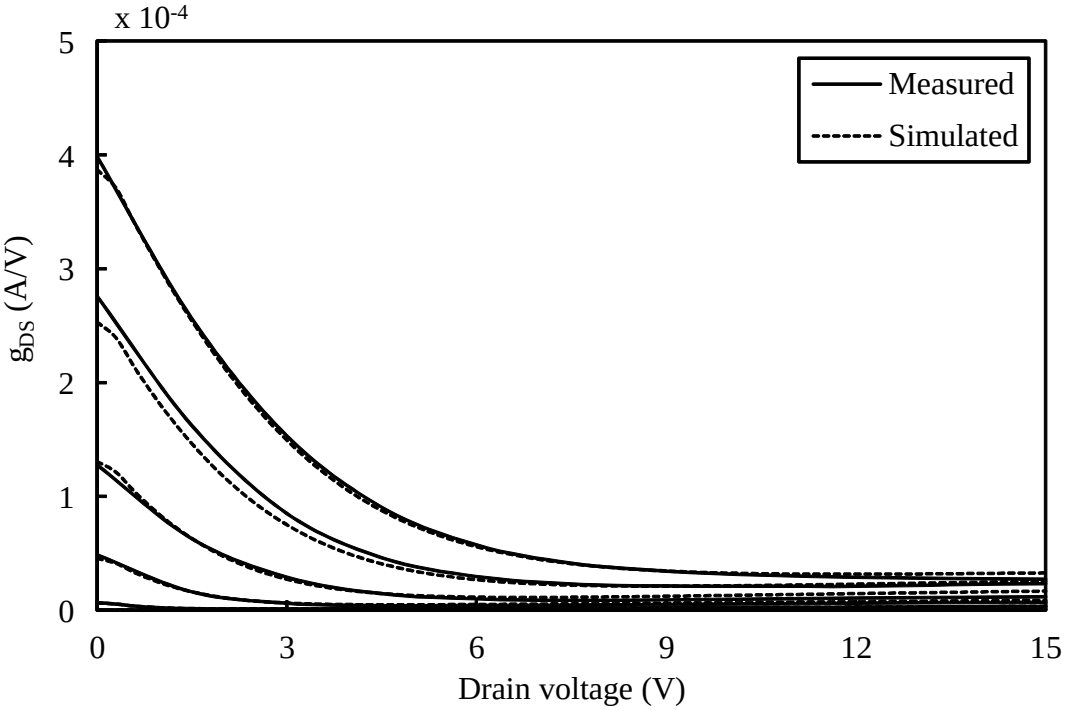


Fig. 4.42: Measured (solid) and simulated (dash) $g_{DS} - V_{GS}$ characteristics of $32\mu m \times 2\mu m$ enhancement MOSFET at 25 °C

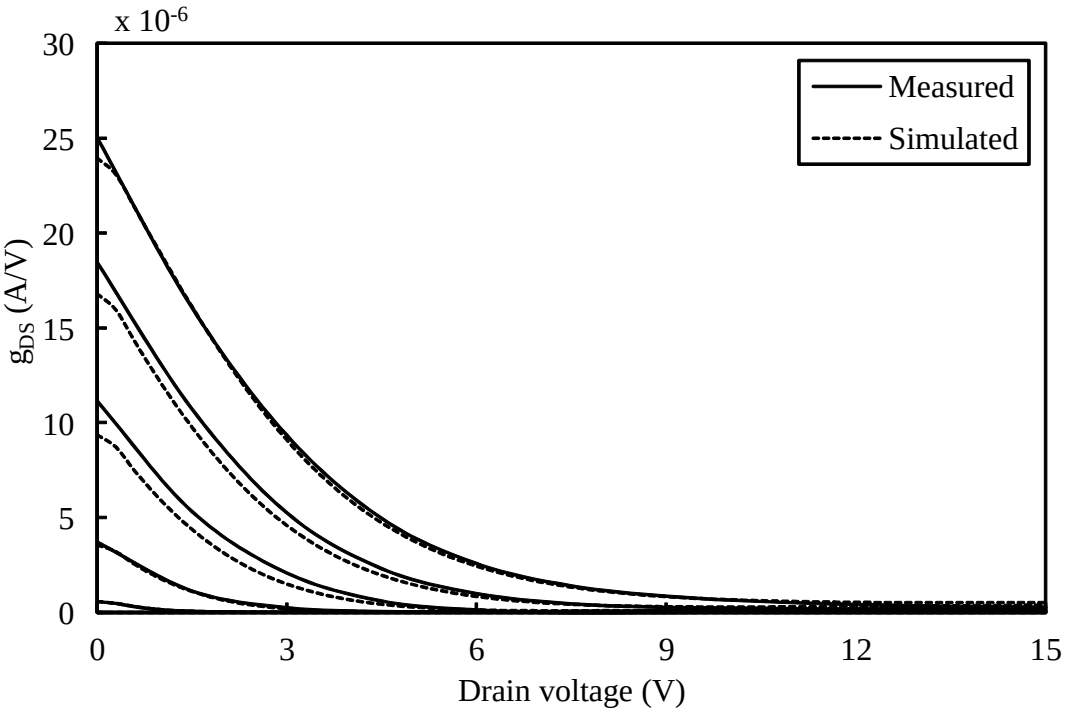


Fig. 4.43: Measured (solid) and simulated (dash) $g_{DS} - V_{GS}$ characteristics of $8\mu m \times 8\mu m$ enhancement MOSFET at 25 °C

The calculated values of ΔL and ΔW were $0.21\mu m$ and $0.08\mu m$ respectively and were used in the geometry scaling procedure. Using the variation of **BETN** with device geometry, value of **UO** was set to 0.0042.

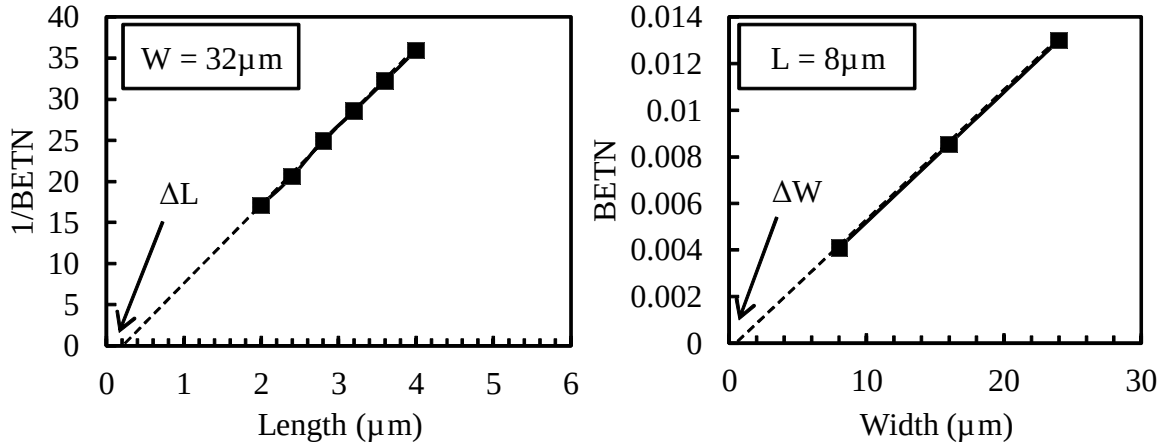


Fig. 4.44: Extraction of ΔL and ΔW from **BETN**

Fig. 4.45 shows the length scaling of **VFB**. The extracted value of **VFBO** was -0.5 and that of **VFBL** was -5.9. No variation of **VFB** was observed with width, and **VFBW** and **VFBLW** were set to 0.

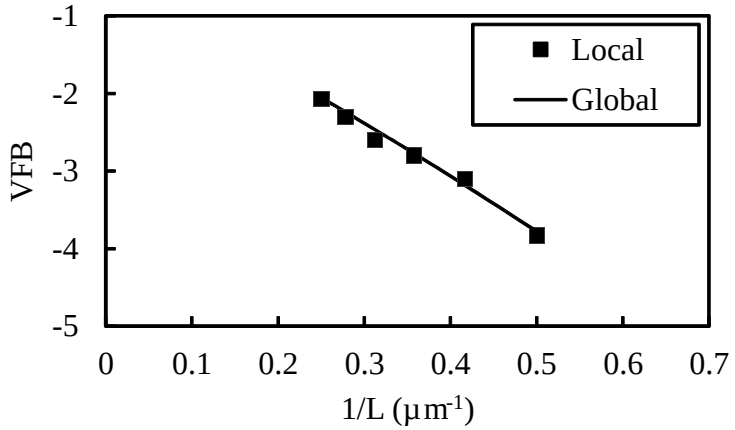


Fig. 4.45: Variation of **VFB** with 1/L

The variation of saturation velocity parameter **THESAT** with L is shown in Fig. 4.46. The

calculated value of **THESATO** was -0.385, value of **THESATL** was 0.7 and the value of **THESATLEXP** was 0.055. The variation of **THESAT** with width was negligible, and was not used by setting **THESATW** and **THESATLW** to 0.

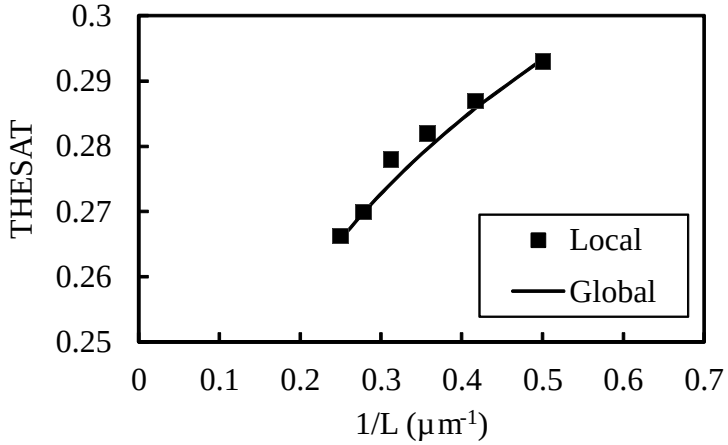


Fig. 4.46: Variation of **THESAT** with 1/L

The length scaling of DIBL parameter **CF** is shown in Fig. 4.47. The DIBL parameter was seen to increase with 1/L as expected. Due to a large drain-source voltage of 20 V in the SiC MOSFETs, the DIBL effect was seen at channel length of 2μm. The calculated values of **CFL**, **CFLEXP** and **CFW** were 0.25, 1.05 and 0 respectively.

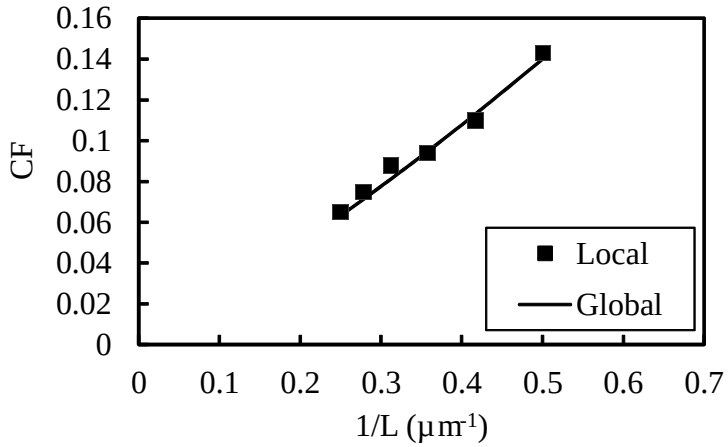


Fig. 4.47: Variation of **CF** with 1/L

4.5.5 Temperature Scaling

Temperature scaling has been discussed in detail in section 4.4.5, and will not be discussed again. Instead, results of the performance of the model for the $16\mu m \times 8\mu m$ enhancement MOSFET have been presented. A list of all the extracted enhancement model parameters have been listed in Table 4.7.

Fig. 4.48 shows the comparison between measurement and simulation of the input characteristics over temperature. The threshold voltage can be seen to decrease with increasing temperature as expected. Figs. 4.49 and 4.50 show the measured and simulated output characteristics for the same device at 125 °C and 225 °C respectively. It is seen that the on-state resistance of the enhancement MOSFET *decreases* with temperature, which is opposite to the expected behavior. This behavior is attributed to the behavior of interface trap occupancy, which reduces with increasing temperature and has been described in detail in section 3.5.4. This effect has been modeled by using the proper values for the temperature scaling parameters **STBETN**, **STVFB** and **STTHEMU**.

The temperature scaling of **BETN** is shown in Fig. 4.51. Using the extracted local values for **BETN** over temperature, the value of **STBET** was calculated to be -0.41. The variation of **VFB** with temperature is shown in Fig. 4.52. The extracted value of **STVFB** from temperature variation of **VFB** was -2.3×10^{-3}. The variation of **THEMU** with temperature is shown in Fig. 4.53. The calculated value of **STTHEMU** was 1.5.

In order to account for the reduction of trapped charge as temperature increases, the Coulumbic scattering parameter **CS** was also scaled with temperature. The temperature scaling for **CS** is given by

$$CS_T = \mathbf{CS} \,.\, \left(\frac{T_{KD}}{T_{KR}}\right)^{\mathbf{STCS}} \tag{4.72}$$

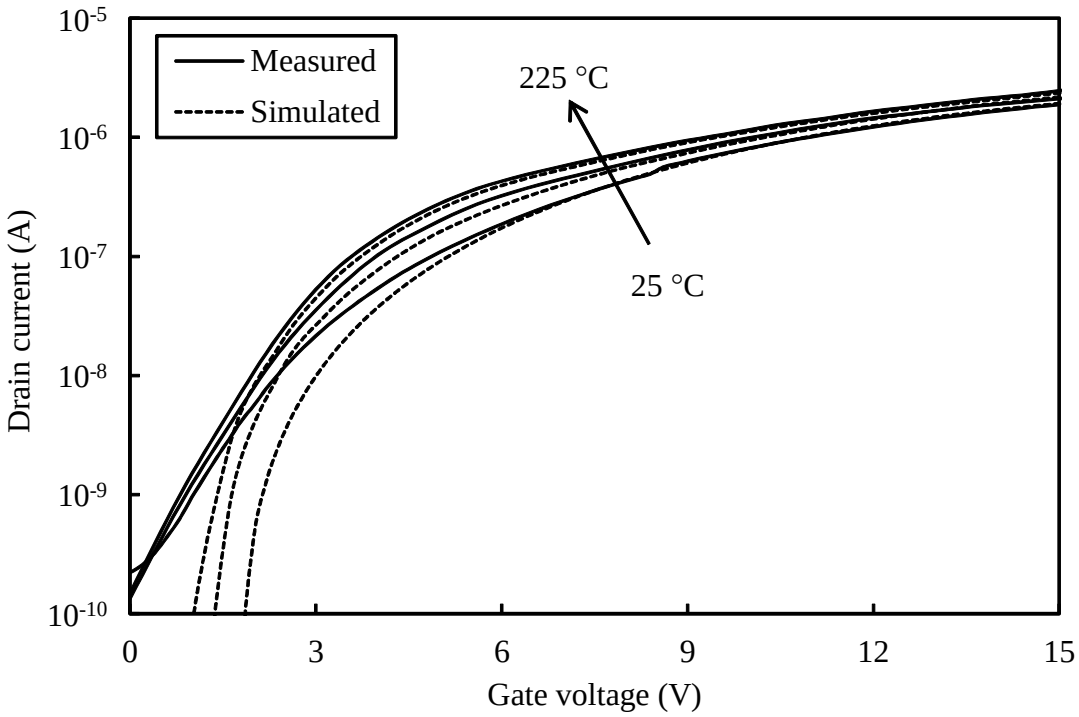


Fig. 4.48: Measured (solid) and simulated (dash) $I_D - V_{GS}$ characteristics of $16\mu m \times 8\mu m$ enhancement MOSFET over temperature

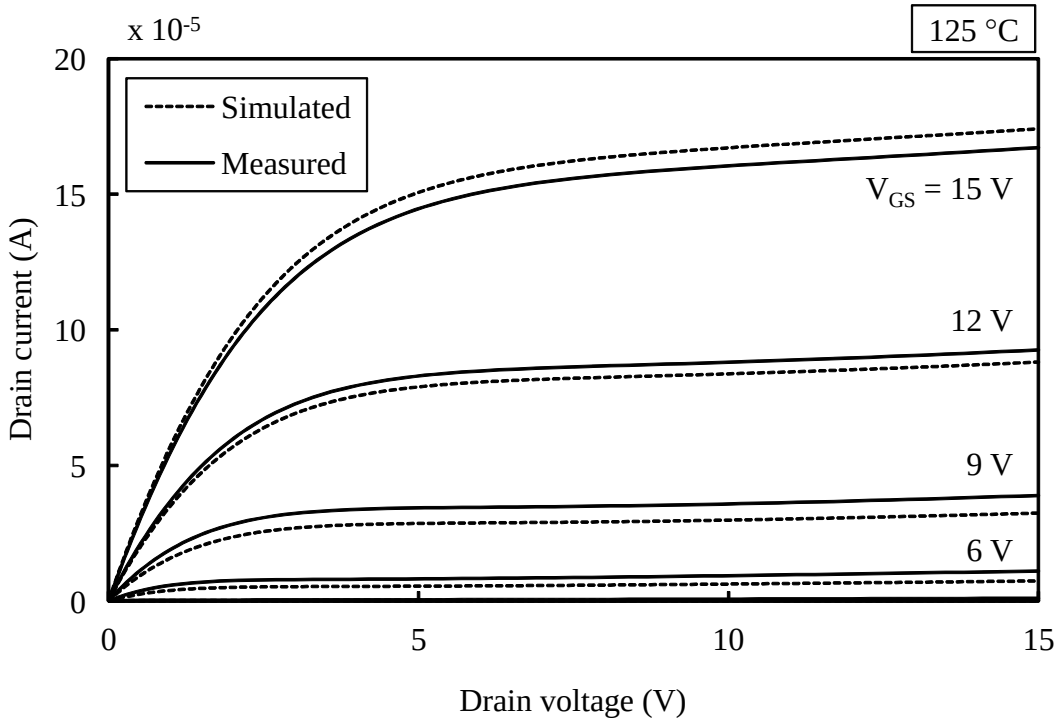


Fig. 4.49: Measured (solid) and simulated (dash) $I_D - V_{DS}$ characteristics of $16\mu m \times 8\mu m$ enhancement MOSFET at 125 °C

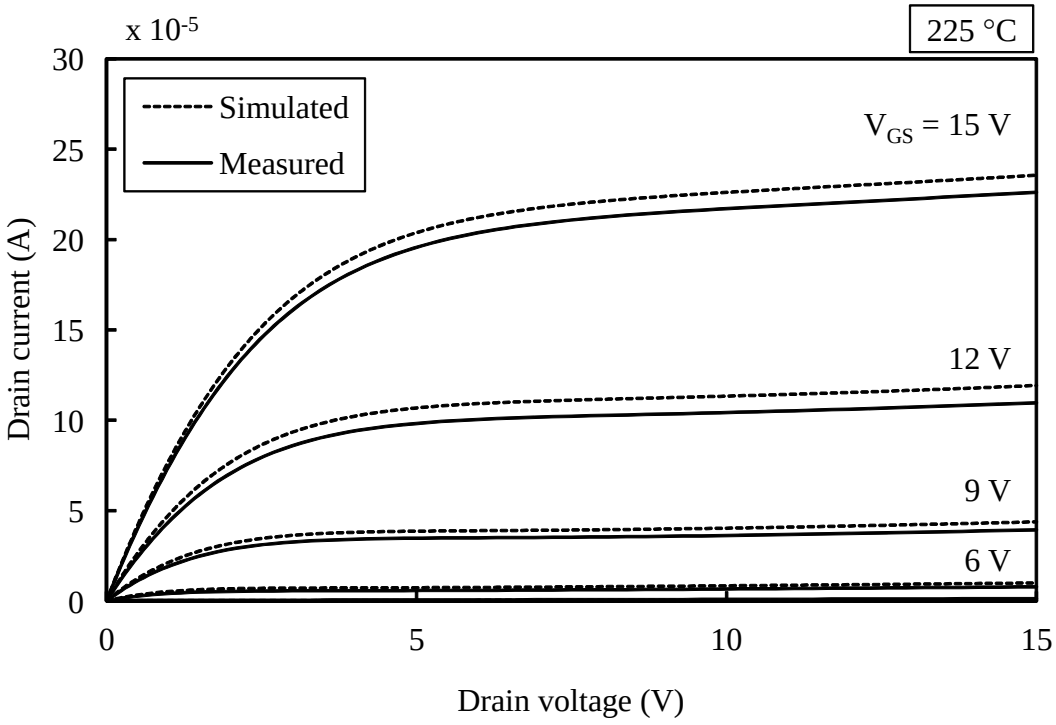


Fig. 4.50: Measured (solid) and simulated (dash) $I_D - V_{DS}$ characteristics of $16\mu m \times 8\mu m$ enhancement MOSFET at 225 °C

Fig. 4.54 shows the temperature scaling of **CS**. The calculated value of **STCS** was -2.2. As expected, as the temperature increases, the effect of **CS** reduces because the electrons in the channel get more energy to overcome the trapped charge scattering. In addition to this effect, the trap occupancy also decreases with temperature [67] which further reduces the Coulumbic scattering component in the channel. The complete parameter set for the enhancement MOSFET is given in Table 4.7.

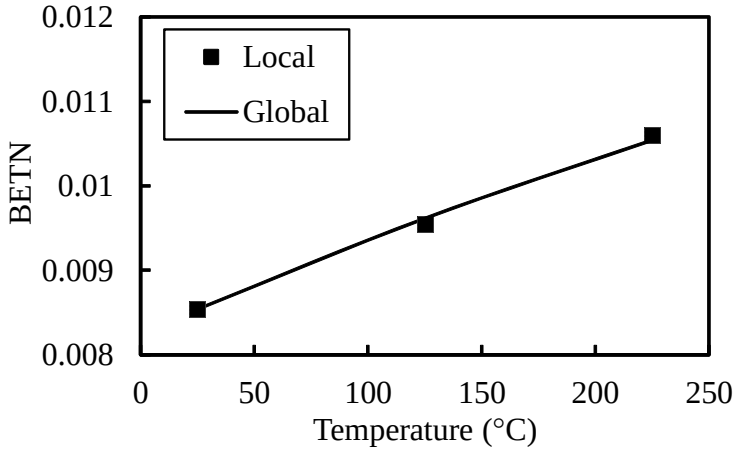


Fig. 4.51: Temperature scaling of **BETN** for the $16\mu m \times 8\mu m$ enhancement MOSFET

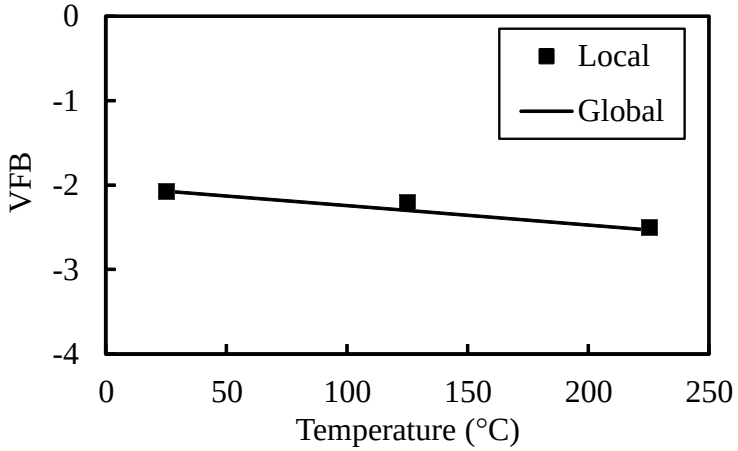


Fig. 4.52: Temperature scaling of **VFB** for the $16\mu m \times 8\mu m$ enhancement MOSFET

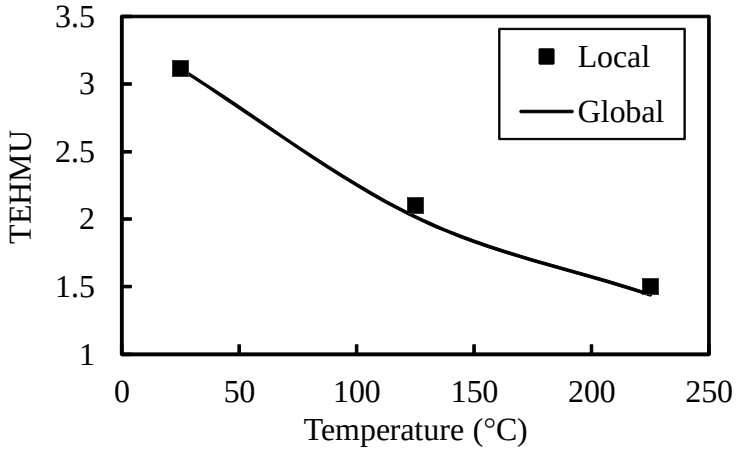


Fig. 4.53: Temperature scaling of **THEMU** for the $16\mu m \times 8\mu m$ enhancement MOSFET

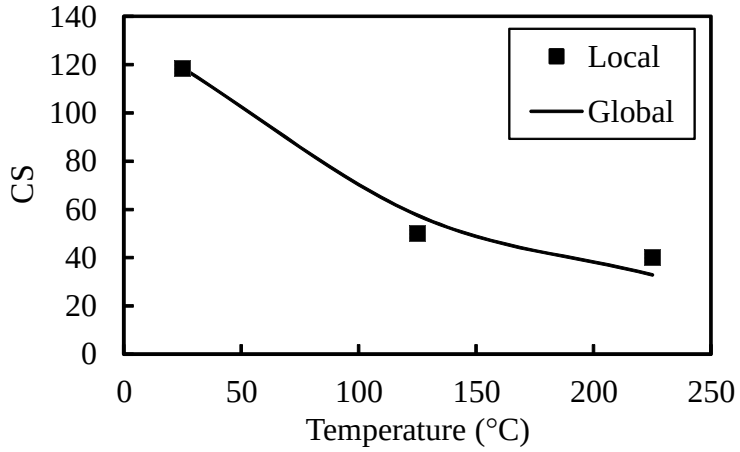


Fig. 4.54: Temperature scaling of **CS** for the $16\mu m \times 8\mu m$ enhancement MOSFET

Table 4.7: Extracted parameters of the PSP model

Parameter	Description	Depletion	Enhancement
TYPE	N-type: 1, P-type: -1	1	1
LEVEL	Model selection	103	103
TR	Reference temperature	25	25
DTA	Temperature offset	0	0
SWGEO	Geometry scaling switch	1	1
SWDELVTAC	Separate charge calculation flag	1	1
QMC	Quantum-mechanical correction	1	1
VFB	Flat-band voltage local value	-	-
VFBO	Geometry independent part	-9	-0.5
VFBL	L-scaling	-2.2	-5.9
STVFB	Temperature scaling	-1.95×10^{-3}	-2.3×10^{-3}
TOX	Oxide Thickness local value	-	-
TOXO	Geometry independent part	4.1×10^{-8}	4.1×10^{-8}
NEFF	Substrate doping local value	-	-
NSUBO	Geometry independent part	2.06×10^{22}	1.05×10^{22}
FACNEFFAC	Effect substrate doping factor	-	-
FACNEFFACO	Geometry independent part	2.694	2.512
DPHIB	Offset of bulk potential	-	-
DPHIBO	Geometry independent part	1.913	1.878
CF	DIBL parameter	-	-
CFL	L-scaling	0.25	0.255
CFLEXP	L-scaling exponent	0.9	1.05
BETN	Zero-field mobility X Aspect ratio	-	-
UO	Zero-field mobility	0.05	0.0042
STBET	Temperature scaling	2.6	-0.41
MUE	Mobility reduction coefficient local value	-	-
MUEO	Geometry independent part	4.077	1
THEMU	Mobility reduction exponent local value	-	-
THEMUO	Geometry independent part	0.911	3.112
STTHEMU	Temperature scaling	1.9	1.5

Parameter	Description	Depletion	Enhancement
CS	Coulumbic scattering local value	-	-
CSO	Geometry independent part	0	118.6
STCS	Temperature scaling	0	-2.5
THESAT	Velocity saturation parameter local value	-	-
THESATO	Geometry independent part	-0.604	-0.385
THESATL	L-scaling	0.7	0.7
THESATEXP	L-scaling exponent	0.055	0.055
AX	Linear/saturation transition factor local value	-	-
AXO	Geometry independent part	3	0.6
COX	Intrinsic channel oxide capacitance local value	-	-
COXO	Geometry independent part	2.11×10^{-13}	2.11×10^{-13}

Chapter 5

Power MOSFET Model

5.1 Introduction

Compact model development for SiC power MOSFETs is currently an active area of research. With the rapid development of SiC power MOSFETs by various research groups, the development of good compact models for power MOSFETs must follow. Several device manufacturers ship SPICE sub-circuit models with their devices, which have numerous problems. Sub-circuit models generally suffer from empirical formulation and do not always provide physically relevant parameters. In addition, the overall complexity of sub-circuit models often causes convergence problems. There are several sub-circuit based power MOSFET models in the published literature that contain discrete models to simulate the DMOSFET structure [93] – [99]. Compact models have a clear advantage over sub-circuit models because of improved convergence, physical description of equations and parameters and a reduction in the total number of parameters. Designers are now feeling the need for accurate compact models to be able to simulate the new breed of SiC power MOSFETs.

A physical model based on the charge sheet approach has been proposed by Brews *et al.* [73] that provides an accurate description of the device performance [100]. However, the model relies heavily on the description of the device structure and internal doping profiles, and cannot be used for off-the shelf devices. Budihardjo *et al.* proposed a lumped-charge model [101] which is based on the lumped charge modeling approach [102], [103]. The lumped charge (LC) modeling approach, as the name suggests consists of lumping the charges in the device in the various regions,

and the charges vary with the applied biases. LC models have a good physical description of the various regions of operation, but their parameters are difficult to extract. McNutt *et al.* presented a compact model for SiC power MOSFETs with a good description of the gradual transition from linear to saturation region of operation. The model's parameter extraction procedure has been implemented in a proprietary software that is not available. Phankong *et al.* developed a model with a good description of the internal capacitances [104]. However, the model has a simple description of the channel current and does not accurately reproduce the gradual transition from linear to saturation seen in SiC power MOSFETs. Göhler *et al.* proposed a compact model in VHDL with a good description of the switching behavior and the reverse diode of the power MOSFET [105]. However, the model has a simplified formulation of the on-state characteristics and does not accurately model the transition from linear to saturation region.

A new compact model has been developed in this work for SiC power MOSFETs, with a datasheet driven parameter extraction methodology [45]. The parameter extraction procedure would allow the user to extract all relevant model parameters using the data that is available from most device vendors. The model features an accurate description of the MOS channel, drift region, non-linear capacitances, and the internal charges. Parameters have been extracted for the commercially available 1200 V, 20 A SiC power MOSFET from 25°C to 200°C. The model's on-state and switching behavior has been verified by comparing simulation with characterized data from bare-die and packaged devices.

For modeling low voltage MOSFETs, the PSP model was used as the base model with SiC relevant modifications. The low voltage MOSFETs are used in a large variety of applications, including digital, analog and RF applications. For the present work, the SiC MOSFETs were intended to develop digital and low frequency analog circuits for the gate driver. A compact model

needed to design such circuits must have all the necessary effects included in them that would be sufficient for the application. At the same time, several effects that are irrelevant for the intended application can be omitted to lessen the burden of simulation complexity and parameter extraction. In short, a compact model must be sufficiently able to model a device for *an intended application space*. The PSP model contains all physical effects that are important to consider when designing digital and low frequency analog circuits and was suited for modeling the low voltage MOSFETs. Additionally, several geometries of the low voltage devices were available, and the PSP model offers geometry and temperature scaling frameworks which enabled the use of a single global parameter set for all the device sizes.

The emphasis on the intended application is important, and it justifies the use of the PSP model for the low voltage MOSFETs. The power MOSFET on the other hand is used in switch-mode type application, where large-signal DC and transient characteristics of the device are of interest. A compact model for the power MOSFET model needs to address different requirements of the application space. Since power MOSFETs are not geometry scaled devices, geometry scaling is not needed in a power MOSFET model. Similarly, more focus must be given to the switching characteristics of the device, and the large signal C-V characteristics of the model must accurately fit the device. Thus, the formulation of the power MOSFET is different and less extensive than the PSP model, because it is sufficient and accurate to describe the power MOSFET characteristics in power system simulations.

5.2 Model Description

The power MOSFET model developed in this work has been written in MAST and Verilog-A modeling languages and is supported by a wide variety of simulators. For sake of brevity, the term "model" from now on throughout this chapter refers to the new power MOSFET model, unless specified otherwise. The basic structure of the model is shown Fig. 5.1. The model has 3 external pins – gate (G), drain (D) and the source (S) and an internal pin (DI) to represent the partitioning of the drift region from the channel region of the DMOSFET. In the description of the model, the calculated variables have been written using a normal font style with the name of the variable like $I_{channel}$ and q_{gd}. The model parameters have been written in all-capital bold letters like **VT1** and **KP1**, and temperature scaled parameters have been written with a sub-script **T** like $\mathbf{VT1_T}$ and $\mathbf{KP1_T}$ to ease the distinction between internal variables, model parameters and their temperature scaled values. In order to improve readability, the equations discussed in this section do not include the temperature scaled representation for the parameters. However, temperature scaling will be discussed in detail in Section 5.3.4.

5.2.1 On-state Characteristics

When the bias on the gate exceeds the threshold voltage, current in the device flows from the drain to the source and comprises the main channel current. In order to provide additional flexibility in controlling the transition from linear to saturation region, the main channel current has been divided into two parallel components as

$$I_{channel} = I_1 + I_2 \tag{5.1}$$

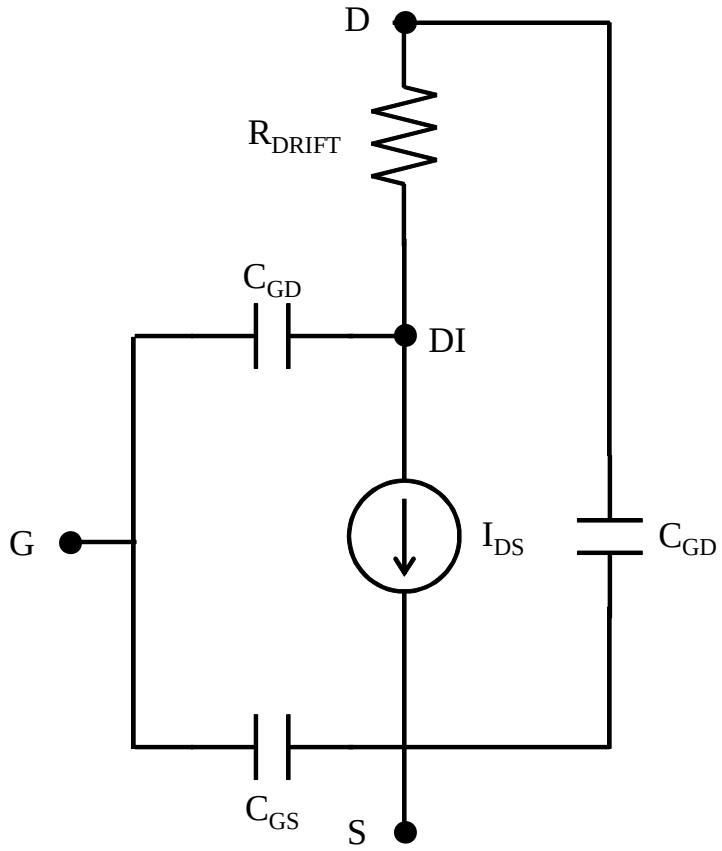


Fig. 5.1: Topology of the power MOSFET model

where $I_{channel}$ is the total channel current of the device, I_1 and I_2 are the two channel components. The Hefner IGBT model [106] has described this partition and provided a formulation that allows the smooth transition from linear to saturation region of the device. The formulation has been modified to de-couple the extraction of the model parameters and redefined in this model. Each component of the channel current is treated independently and provides additional fidelity during the parameter extraction process. For both current components, the different regions of operation are defined as

$$\text{Channel State} \begin{cases} \text{Off} & \text{if } V_{GS} < \mathbf{VTX} \\ \text{Linear} & \text{if } V_{GS} \geq \mathbf{VTX} \text{ and } V_{DIS} \leq \dfrac{V_{GS} - \mathbf{VTX}}{\mathbf{PVF}} \\ \text{Saturation} & \text{if } V_{GS} \geq \mathbf{VTX} \text{ and } V_{DIS} > \dfrac{V_{GS} - \mathbf{VTX}}{\mathbf{PVF}} \end{cases} \tag{5.2}$$

where **X** in all the equations is replaced by **1** and **2** to describe I_1 and I_2 components, **VTX** is the threshold voltage, **PVF** is the pinch-off parameter, V_{GS} is the applied gate-source voltage and V_{DIS} is the voltage between the internal drain node and the source. The channel current in each of the operating regions is given as:

Linear Region

$$I_X = \mathbf{KFX} \cdot \mathbf{KPX} \left\{ (V_{GS} - \mathbf{VTX}) V_{DIS} - \left(\mathbf{PVF}^{(yx-1)} {V_{DIS}}^{yx} (V_{GS} - \mathbf{VTX})^{\left(\frac{2-yx}{yx}\right)} \right) \right\} \left(1 + \frac{V_{DIS}}{\mathbf{VA}} \right) \tag{5.3}$$

Saturation Region

$$I_X = \mathbf{KPX} \frac{(V_{GS} - \mathbf{VTX})^2}{1 + \mathbf{THETAX}(V_{GS} - \mathbf{VTX})} \left(1 + \frac{V_{DIS}}{\mathbf{VA}} \right) \tag{5.4}$$

$$yx = \frac{\mathbf{KFX}}{\mathbf{KFX} - PVF/2} \tag{5.5}$$

Threshold voltage of the power MOSFET is defined by **VTX**. The parameter **PVF** controls the transition region from linear to saturation of the power MOSFET. Fig. 5.2 shows the variation of

the output characteristics for an output characteristic sweep at $V_{GS} = 10\,V$ for different values of **PVF**. The current gain parameters **KFX** and **KPX** are joined continuously by the variable *yx* given by (5.5). At higher gate voltages, the reduction in current due to transverse electric fields is given by the term containing **THETAX** in (5.4). The formulation of the channel current is continuous in the second order in order to allow proper convergence of the simulator and a continuous transition from saturation to linear region.

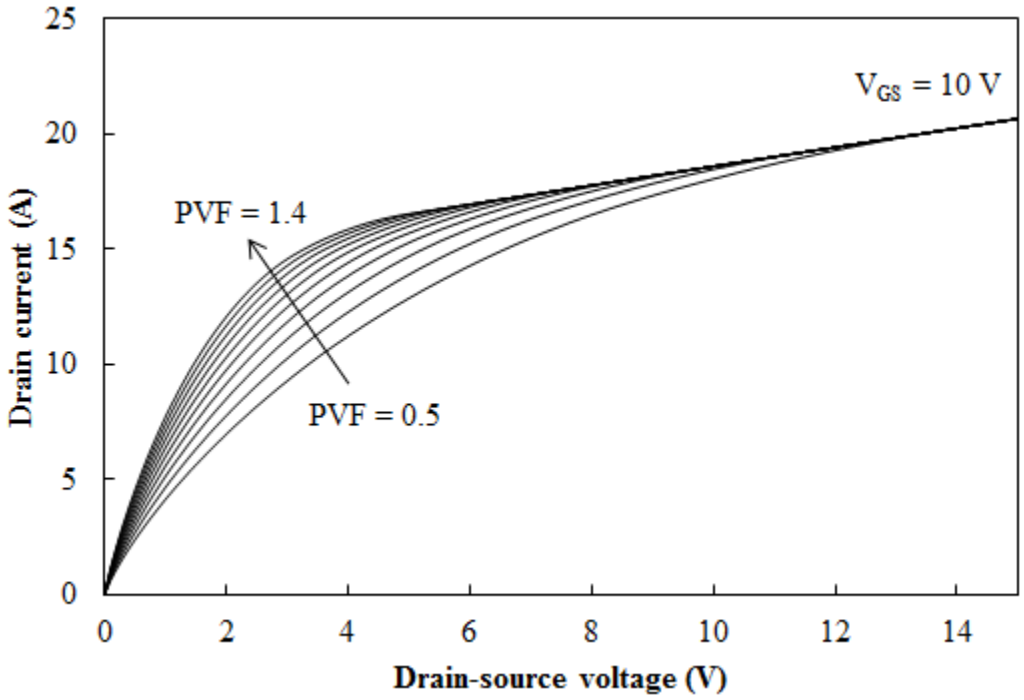


Fig. 5.2: Controlling transition from linear to saturation using **PVF**

The on-state voltage drop across the power MOSFET is shared between the source contact resistance, the channel and the drift layer resistance as

$$V_{DS} = I_D(R_{drift} + \mathbf{RS}) + V_{DIS} \tag{5.6}$$

Typically, the contact resistance is small as compared to the channel and the drift region resistance. As a result, the source resistance can be approximated to be combined with the drift layer resistance on the drain side as in (5.6) to reduce the number of internal nodes needed in the model to improve simulation speed. The contribution of the drift layer resistance must be calculated accurately for proper modeling of the device. The drift region resistance is given as

$$R_{drift} = \frac{w}{qA\mathbf{NA}\mu_n} \tag{5.7}$$

where w is the width between the depletion layers, and is given by

$$w = \mathbf{WB} - 2w_{dep} \tag{5.8}$$

$$w_{dep} = \sqrt{\frac{2\varepsilon_{SiC}\left(V_{DIS} - V_{bi}\right)}{q\mathbf{NA}}} \tag{5.9}$$

$$V_{bi} = \phi_T ln\left(\frac{\mathbf{NA}N_D}{{n_i}^2}\right) \tag{5.10}$$

where N_D is the doping of the drift region, ϕ_T is the thermal voltage, V_{bi} is the built-in voltage across the P-substrate/N-drift region and n_i is the intrinsic carrier concentration of SiC. The doping of the lightly doped drift layer (N_D) is assumed to be $10^{16}\,\mathrm{cm}^{-3}$, which is the typical value for SiC power MOSFETs. The intrinsic carrier concentration and mobility in the lightly doped drift region as a function of temperature are given in (2.2) and (2.7)

The current through the drift region is calculated as

$$I_{Drift} = \frac{V_{DDI}}{\left(\mathbf{RS} + R_{drift}\right)} \tag{5.11}$$

Since the drift region is in series with the channel region, the current in the two must be the same. Thus, (5.1) and (5.11) are equated to iteratively solve for the voltage at the internal node DI. Using the approximation of combining the source series resistance in the drift region, the number of internal nodes reduces to 1, which greatly increases the simulation speed and improves model convergence.

5.2.2 Transient Characteristics

A structure of the power MOSFET with internal capacitances is shown in Fig. 2.5. The main capacitances in the structure are: (a) gate-source overlap and metallization capacitance, (b) source-drain depletion capacitance and (c) gate-drain two phase overlap capacitance.

Typically, the source contact region is heavily doped in order to provide a good ohmic contact between the metal and the source. The capacitor between the gate and the source is formed at the gate-source metalization and the gate-source overlap region. The gate-source metalization component is a constant parallel plate capacitor. The gate-source overlap component can also be approximated as a parallel plate capacitor due to the high doping in the N^+ region, which causes very little variation in the depletion width in the N^+ region during inversion. Since both the capacitance components are constants, they have been combined into a single parameter, the gate-source capacitance parameter **CGSO**. Thus, the gate-source capacitance and charge stored in the capacitor are given as

$$cgs = \mathbf{CGSO} \tag{5.12}$$

$$qgs = cgs \cdot V_{GS} \tag{5.13}$$

The drain-source junction forms a P/N^- junction, since the P-substrate region is always shorted to

the source through the P^+ contact. The resulting capacitor that forms between the drain and the source regions is the depletion region capacitance of a P-N junction, which can be modeled as

$$cds = \mathbf{CDSO}\left(\frac{1}{1+V_{DIS}/V_{bi}}\right)^{\mathbf{M}} \tag{5.14}$$

and the stored charge in the depletion region is given as

$$qds = \int_0^{V_{DIS}} cds.dV \tag{5.15}$$

$$qds = \frac{\mathbf{CDSO}.{V_{bi}}^{\mathbf{M}}}{1-\mathbf{M}}\left[(V_{bi}+V_{DIS})^{(1-\mathbf{M})} - {V_{bi}}^{(1-\mathbf{M})}\right] \tag{5.16}$$

The gate-drain junction is a series combination of the oxide capacitor under the gate and the depletion region in the lightly doped drift region. The gate-oxide capacitance is constant and depends on the active area and the oxide thickness. The depletion width under the gate-oxide varies with the applied biases on the gate and the drain. The depletion region under the gate-oxide disappears when the gate-oxide-drain structure reaches flat-band condition. The flat-band voltage is defined by the parameter **VFB**. The gate-drain overlap capacitance is given as

$$cgd = \frac{\varepsilon_{SiC}\cdot\mathbf{AGD}}{t_{gd}} \tag{5.17}$$

$$t_{gd} = t_{ox} + w_{gd} \tag{5.18}$$

$$t_{ox} = \frac{\varepsilon_{SiC}\cdot\mathbf{AGD}}{\mathbf{COXO}} \tag{5.19}$$

$$w_{gd} = \begin{cases} 0 & \text{if } V_{DIG} \leq -\mathbf{VFB} \\ \sqrt{\dfrac{2\varepsilon_{SiC}\left(V_{DIG}+\mathbf{VFB}\right)}{(q\mathbf{NA})}} & \text{if } V_{DIG} > -\mathbf{VFB} \end{cases} \tag{5.20}$$

where, **AGD** is the active gate-drain overlap area, t_{gd} is the total charge thickness under the gate, t_{ox} is the physical oxide thickness, w_{gd} is the gate-drain depletion layer thickness, **VFB** is the flat-band voltage, **COXO** is the gate-oxide capacitance per unit area and V_{DIG} is the voltage between internal node DI and gate node G. The gate-drain capacitor formulation results in a two-phase capacitance, the value of which varies with the drain and gate voltage until the gate-drain voltage reaches flat-band condition.

5.3 Parameter Extraction

The new power MOSFET compact model has been developed with a parameter extraction strategy in mind that allows the user to extract the parameters using data available in datasheets. The model contains 20 room temperature parameters and 10 temperature parameters that control the temperature scaling of the room temperature parameters. Table 5.1 lists all the model parameters with a brief description and classification as DC, CV or temperature parameter. For brevity, the room temperature parameters are called nominal parameters.

The parameter extraction procedure consists of the following three main steps:

- Measurements
- Extraction of nominal parameters at room temperature
- Extraction of temperature scaling parameters

5.3.1 Measurements

While the parameter extraction strategy can be followed by using data from device datasheets, the data presented in the datasheet is often a mean-value data-set, with some variation in the data going from one device to another. As a result, it is a good practice to verify the device data through physical measurements to gain more insight into the device characteristics.

For the validation of the model in this dissertation, actual characterization data has been used from the commercially available 1200 V, 20 A SiC power MOSFETs. The characterization has been done using an Agilent B1505A Power Device Analyzer [107]. The power MOSFETs were available in a TO-247 package for characterization. In addition, bare dies for the same device were also available from Cree.

In order to characterize the bare-dies, they were mounted on a hot chuck in a Signatone High Power Probe Station. A power MOSFET is a vertical device, with the gate and source on top and the drain at the bottom. Since the chuck is electrically grounded, the dies cannot be directly placed on the chuck. A probe-card was been developed in-house that allows the back-side contact of the die with electrical isolation from the chuck. The gate and source terminals were probed from the top surface of the die, while the drain terminal was probed from under the die using the copper-plate of the spring-loaded probe-card. Thus, the drain terminal was electrically isolated from the chuck. In order to characterize the power MOSFET over the entire temperature range, packaged parts have been used, with the bare-die data used to validate the packaged device data.

The model requires the following measurements at room temperature in order to extract the nominal parameters:

- Measurement 1: Input characteristics (I_D - V_{GS})

V_{GS} swept from 0 V to 20 V in 0.1 V step

V_{DS} constant at 10 V

- Measurement 2: Output characteristics (I_D - V_{DS})

  V_{DS} swept from 0 V to 15 V in 0.1 V step (limit I_D to 20 A)

  V_{GS} stepped from 0 V to 20 V in 2 V step

- Measurement 3: Transfer capacitances (C_{ISS}, C_{OSS} and C_{RSS})

  C_{ISS} – Measure C_{GD} and C_{GS} between source and gate, and connect drain to shield/guard cable, sweep V_{DS}

  C_{OSS} – Measure C_{GD} and C_{DS} between the drain and the gate, and short the source to the gate, sweep V_{DS}

  C_{RSS} – Measure C_{GD} between drain and gate, and connect source to shield/guard cable, sweep V_{DS}

In addition, measurements 1 and 2 should be performed on at least 2 more temperature points (mid-temperature and max-temperature) in order to extract the temperature scaling parameters.

5.3.2 Initialization of Parameters

Before starting the parameter extraction, some parameters were calculated and fixed for the rest of the extraction process. **TEMPC** is the simulation reference temperature, and was set to 25. **A** is the active device area and **AGD** is the gate-drain overlap area. If any information about the device structure is not available, one should scale the value of **A** according to the current rating of the device. For example, the value of **A** is 0.02 for a 20 A device, and can be changed to **A** 0.01 for a 10 A device. The adjustments in the current and capacitance of the device are absorbed by other

parameters, which are optimized using the measured data. However, it must be noted that **AGD** must always be less than **A**. One can start with a value of **AGD** as 0.75.**A**, and then optimize it in later steps.

5.3.3 Extraction of Nominal Parameters

The general strategy while extracting model parameters is to extract the parameters in small groups. Each group of parameters, once extracted serve as initial conditions for the sub-sequent extraction steps. As a result, the sequence of extraction of the parameters becomes important and should be followed. Some steps require a re-optimization of the previously extracted parameter values along-with the new parameters. In those cases, the two steps are re-optimized until satisfactory fits are obtained for both the extraction steps.

In the model, DC and capacitance parameters have been separated and are de-coupled from each other. The parameter extraction process began with the extraction of all DC parameters. First, parameters related to the input characteristics were extracted using measurement 1. Since the drain voltage was kept at 10 V, and the gate-source voltage is swept from 0 V to 20 V, it was ensured that the device went into saturation. During saturation, the current in the device is given by (5.4), re-written here

$$I_X = \mathbf{KPX}\frac{(V_{GS}-\mathbf{VTX})^2}{1+\mathbf{THETAX}(V_{GS}-\mathbf{VTX})}\left(1+\frac{V_{DIS}}{\mathbf{VA}}\right)$$

In the input characteristics, the low current region as shown in Fig. 5.3 was used to extract **VT1** and **KP1**. **VT1** is defined as the voltage around which the power MOSFET starts turning on, and

KP1 controls the slope of turn-on. Then, the high current region was used to extract **VT2** and **KP2**. **VT2** is defined as extrapolated threshold voltage of the power MOSFET, while **KP2** controls the slope of the high current region. During the measurement, the current in the device was limited to the rated value to avoid damaging the device. The result of optimization can be seen in Fig. 5.4.

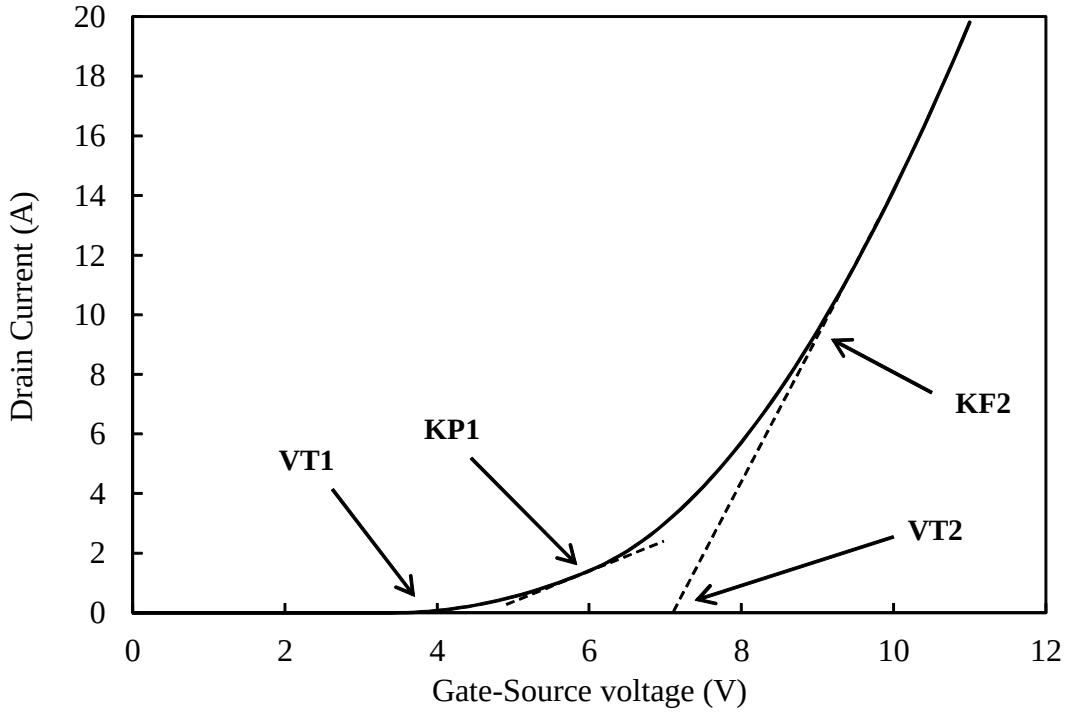


Fig. 5.3: Extraction of **VT1**, **VT2**, **KP1** and **KP2**

Parameters related to the output characteristics were extracted next using measurement 2. The channel current in the on-state is given by a combination of (5.4) and (5.3), where the linear region current is given as

$$I_X = \mathbf{KFX} \cdot \mathbf{KPX} \left\{ (V_{GS} - \mathbf{VTX}) V_{DIS} - \left(\mathbf{PVF}^{(yx-1)} {V_{DIS}}^{yx} (V_{GS} - \mathbf{VTX})^{\left(\frac{2-yx}{yx}\right)} \right) \right\} \left(1 + \frac{V_{DIS}}{\mathbf{VA}} \right)$$

In the output characteristics, the low current region as shown in Fig. 5.5 was used to extract the

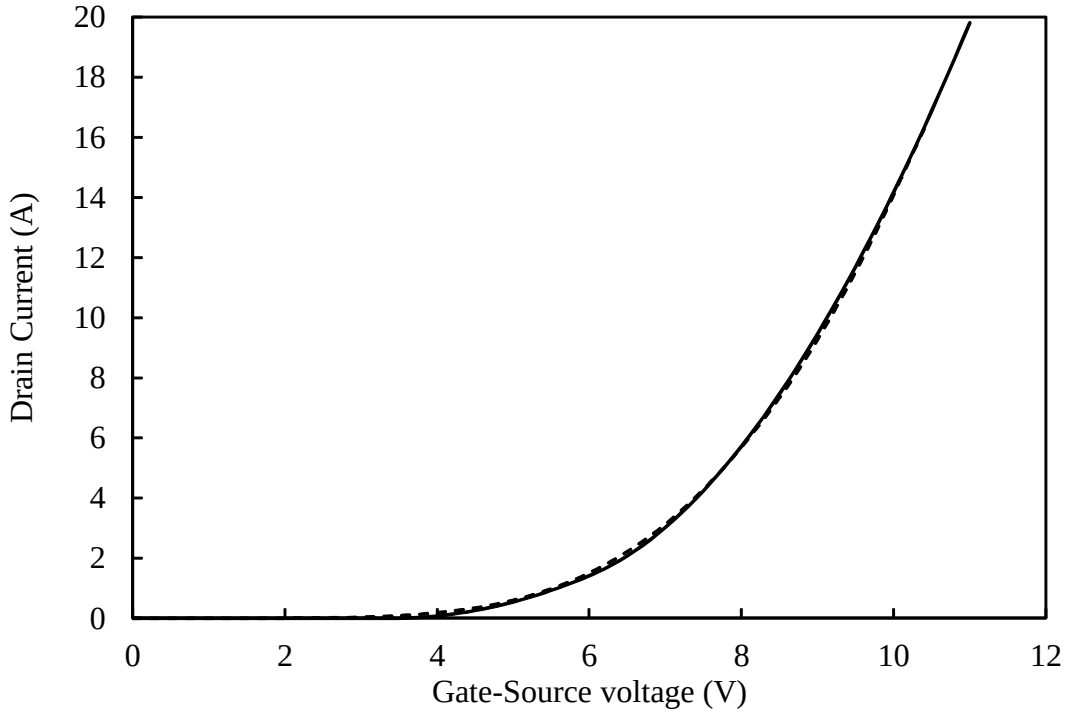


Fig. 5.4: Measured (dash) and simulated (solid) input characteristics at room temperature

low current gain **KF1**, and the high current region was used to extract the high current gain **KF2**. The transition from linear to saturation region was controlled by the transition parameter **PVF**. The variation of the output characteristics with **PVF** has been shown in detail in Fig. 5.2. The slope of the saturation region at low gate voltage values gave the value of Channel Length Modulation parameter **VA**. The result of extraction of parameters from the output characteristics is shown in Fig. 5.6.

After extracting all the DC parameters, the DC extraction steps were repeated in order to get more fine tuned parameter values for the output and the input characteristics. There are two ways to perform the parameter extraction. The first method is to do the extraction manually, using the different data regions described in this section, and tuning the parameter values by hand to get a good fit between the measured and simulation data. The second method is to create a series

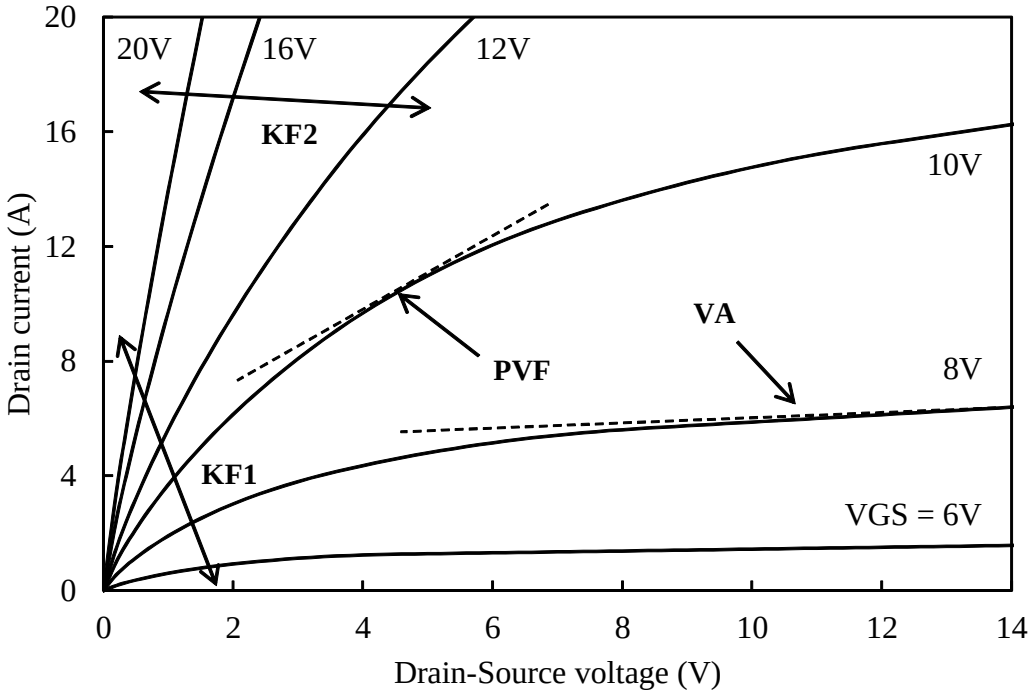


Fig. 5.5: Extraction of **KF1**, **KF2**, **PVF** and **VA**

of automated extraction steps, along-with an optimizer that can optimize the parameter values in specified regions of the measured data. The second method requires additional setup time, but once the setup for the parameter extraction recipe is completed, extracting multiple parameter sets for different devices can be done very efficiently, and saves time in the long run.

In this dissertation, both methods were used. For manual extraction, the Saber simulator environment from Synopsys [38] was used, because Saber allows the tuning of parameters on-the-fly, and also allows the user to import Comma-Seperated-Value files (.csv), which store the measured data. As a result, Saber simulation environment helps with the manual extraction process. For automated extraction, the ICCAP software from Agilent [92] was used. ICCAP is a model parameter extraction tool, and it can interface with several commercial simulators like HSPICE, Saber and Spectre. ICCAP also has several built-in optimizers that can be used with the interfaced simulator

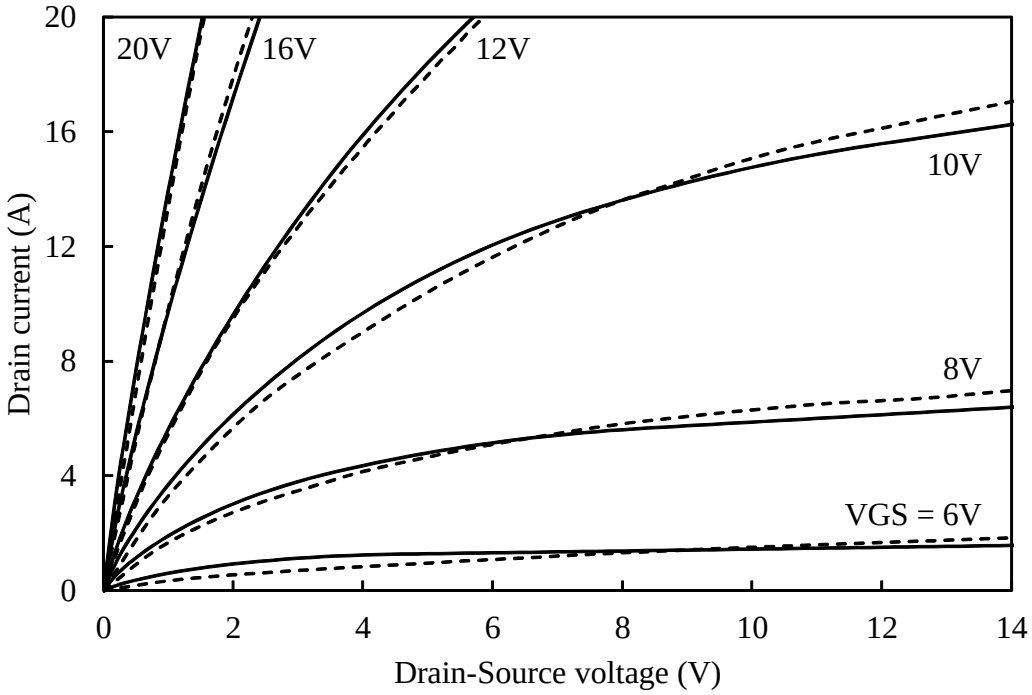


Fig. 5.6: Measured (dash) and simulated (solid) output characteristics at room temperature

to optimize the parameter values. The optimizer also features window definition, that allows the optimization to be done on a specific region of the data. In addition, ICCAP offers the creation of macros which are sequential steps of optimization for a given model. As a result, with the combination of optimization regions and macro-creation, fully-automated extraction routines can be implemented which allow the user to extract all the model parameters with a single macro.

After the extraction of DC parameters was completed, capacitance parameters were extracted. Datasheets generally give values for the input, transfer and reverse capacitances, which relate to the internal model capacitances as

$$C_{ISS} = cgd + cgs \tag{5.21}$$

$$C_{OSS} = cgd + cds \tag{5.22}$$

$$C_{RSS} = cgd \tag{5.23}$$

Parameters related to *cgd* were extracted first because *cgd* is directly calculated from C_{RSS} as shown in Fig. 5.7. If the thickness of the oxide is known from process information, **COXO** can be calculated directly using (5.19), and the initial value of **AGD**. If thickness of the oxide is not available, then parameters **COXO** and **AGD** can be adjusted to control the value of C_{RSS}. The variation of C_{RSS} with V_{DS} is due to the movement of the depletion boundary under the gate in the drift region, which depends on the doping density parameter **NA** of the drift region. Thus, using the C_{RSS}-V_{DS} data, the value for **NA** was extracted.

After extracting parameters related to *cgd*, the value of **CGSO** was extracted which controlled the value of *cds*. **CGSO** is simply the difference in the value of C_{ISS} and C_{RSS} as seen from (5.21) and (5.23). Finally, parameters **CDSO** and **M** related to *cds* were optimized using C_{OSS} - V_{DS} data. The various steps of extraction of capacitance parameters are shown in Fig. 5.7. The result of extracting capacitance parameters is shown in Fig. 5.8.

5.3.4 Temperature Scaling

Once the nominal parameters are extracted, the model is complete and ready to be used for room temperature simulations. However, if device performance over temperature is needed, the model parameters need to scale with temperature. Several nominal parameters have temperature scaling parameters associated with them that scale their values for a given temperature. There are two approaches to extract the temperature scaling parameters.

The first approach is to extract the temperature scaling parameter for the corresponding nominal parameter at the elevated temperature directly using the steps described in Section 5.3.2. In the

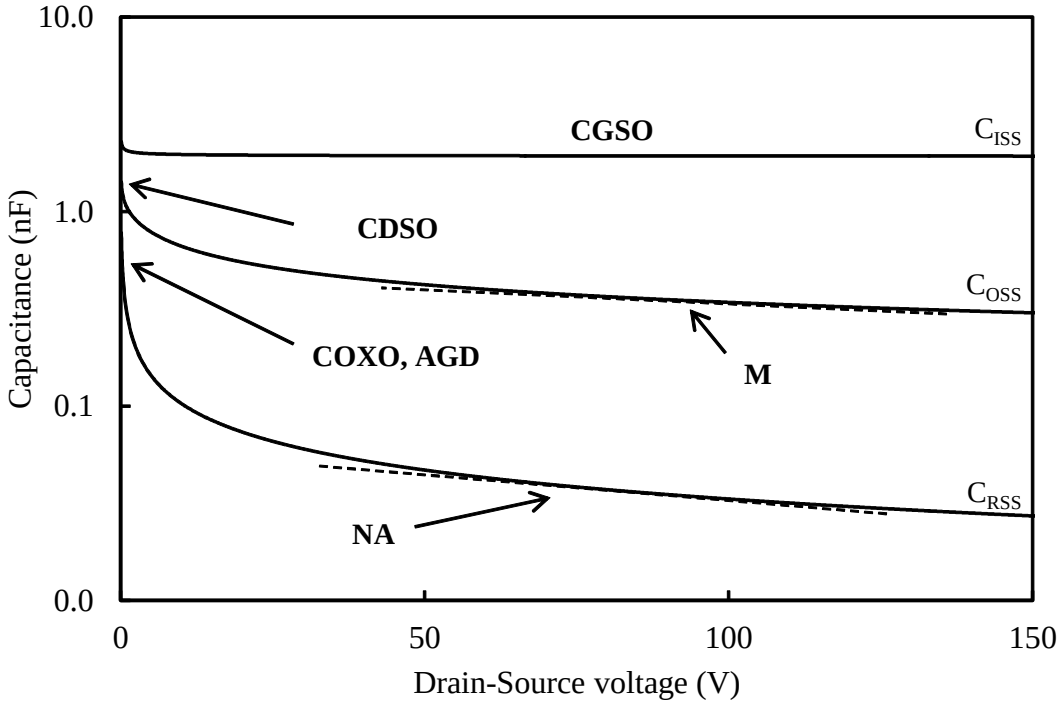


Fig. 5.7: Extraction of capacitance parameters

extraction procedure, the temperature scaling parameter is used instead of the nominal parameter. For example, in order to extract the temperature scaling for **VT1**, the model is simulated at the elevated temperature (225 °C), and the corresponding temperature scaling parameter **VT1TEXP** is extracted at 225 °C. The extract temperature scaling parameters are then verified at a middle temperature point (125 °C e.g.,) to ensure that the temperature scaling is valid throughout the temperature range and not just at the end-points. This approach is simpler and less time consuming and is recommended in the course of normal model usage.

The second approach is suggested if the built-in temperature scaling equations cannot sufficiently predict the device performance over the entire temperature range. This happens if the devices are from a new process, with a different temperature variation trend, or if the model is being used outside of the intended temperature range. For example, if the model is used for a

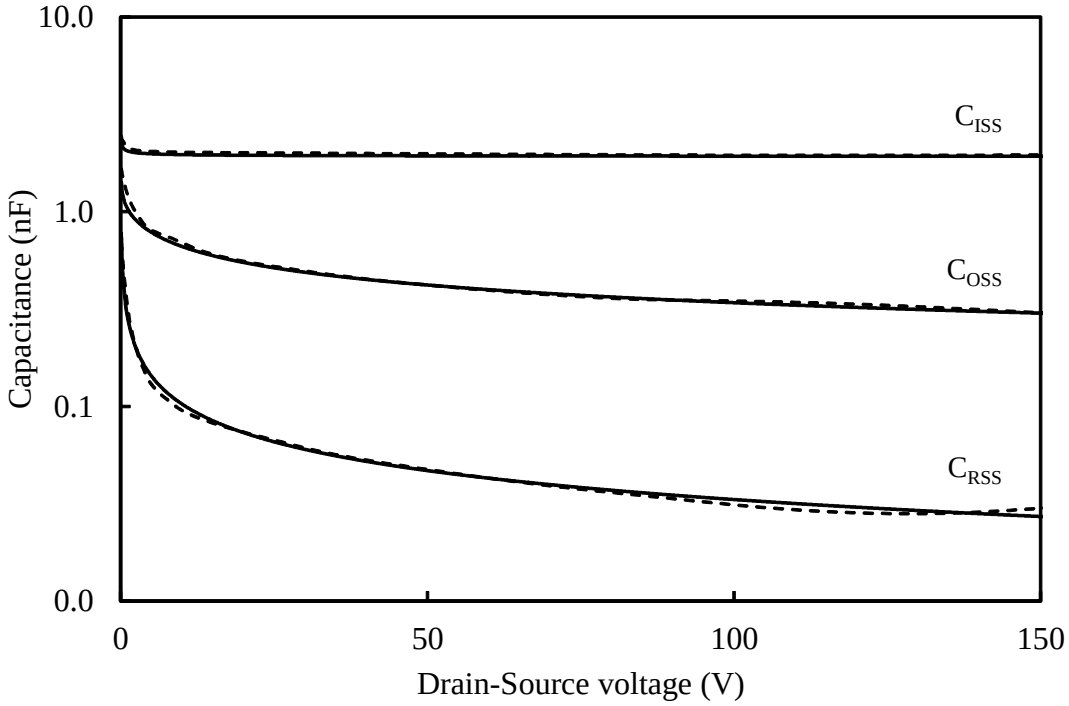


Fig. 5.8: Measured (dash) and simulated (solid) C-V characteristics at room temperature

hypothetical device that can withstand 350 °C, the temperature scaling of the model may not be sufficient to describe the effects beyond 225 °C. The second approach enables the user to derive the temperature scaling behavior of the model, and change the underlying scaling equations in the model to meet their needs.

The second approach, also known as isothermal extraction procedure starts with the extraction of all nominal parameters at *each temperature*. The temperature scaling in the model is turned off by setting the model reference temperature **TEMPC** equal to the simulator temperature T_{Ref} (set inside the simulator options) equal to each of the elevated temperature points. When $\mathbf{TEMPC} = T_{Ref}$, all the temperature scaling equations inside the model are off, as all the temperature scaling equations are a function of either $\mathbf{TEMPC}/T_{Ref}$ or $\mathbf{TEMPC} - T_{Ref}$. Once the parameter extraction procedure is used at different temperature points, a set of nominal parameters as a function of

temperature is obtained. Using these functions, new temperature scaling equations can be defined, which effectively scale the model parameters with temperature. The second approach was used to develop the temperature scaling equations in the model. However, the first approach was also used to re-extract and verify the temperature scaling parameters. Temperature scaling equations for all the nominal parameters are given as

$$KPX_T = \mathbf{KPX}\left(\frac{\mathbf{TEMPC}}{T_{Ref}}\right)^{\mathbf{KPXTEXP}} \tag{5.24}$$

$$KFX_T = \mathbf{KFX}\left(\frac{\mathbf{TEMPC}}{T_{Ref}}\right)^{\mathbf{KFXTEXP}} \tag{5.25}$$

$$THETAX_T = \mathbf{THETAX}\left(\frac{\mathbf{TEMPC}}{T_{Ref}}\right)^{\mathbf{THETAXTEXP}} \tag{5.26}$$

$$VTX_T = \mathbf{VTX} - \mathbf{VTXEXP}\left(T_{Ref} - \mathbf{TEMPC}\right) \tag{5.27}$$

$$VA_T = \mathbf{VA} - \mathbf{VATEXP}\left(T_{Ref} - \mathbf{TEMPC}\right) \tag{5.28}$$

In addition to the temperature scaling equations, the material constants are also scaled with temperature. *Note that the scaling of material constants depend on absolute simulation temperature, and not the reference temperature of the model.* This is the main reason for performing the isothermal extractions at each elevated temperature and turning off the model's temperature scaling and not just extracting model parameters at room temperature for different temperature data-sets. The temperature scaling of intrinsic carrier concentration and mobility in the model is given in (2.2) and (2.7), respectively. A list of all the extracted values of the parameters for the power MOSFET model are given in Table 5.1

5.4 Model Performance

Parameters for the commercially available 1200 V, 20 A SiC power MOSFET from CREE [32] were extracted for a temperature range of 25 °C to 225 °C. In order for a model to be validated, it must reproduce a good match between the measured device and simulated characteristics in DC, CV, and transient characteristics. In the following sections, the performance of the model has been presented for the DC, CV and switching characteristics of the device.

5.4.1 DC Performance

The simulated and measured input characteristics of the power MOSFET at 25 °C, 125 °C and 225 °C are shown in Fig. 5.9. Good agreement is observed between the model and the simulation lending confidence in the model. The simulated and measured output characteristics at the three temperatures are shown in Figs. 5.10 – 5.12. Good match between the simulation and measurement verified the extracted DC parameters over temperature.

It can be seen from the output characteristics that SiC power MOSFETs have a gradual transition from linear to saturation region. In these devices, the resistance of the drift region is low due to high doping in the drift region. In addition, due to low surface mobility of SiC, the channel resistance is high and the channel has a high transconductance. As a result, the enhanced transconductance coupled with low drift region resistance causes the device to transition smoothly from linear to saturation. A good description of the transition by the model is essential in properly reproducing the device characteristics in the transition region.

Another important point to be seen from the output characteristics is the opposite behavior of on-state resistance of the drift region and the threshold voltage. As temperature increases,

the threshold voltage decreases as seen in Fig. 5.9. With increasing temperature, the on-state resistance of the drift region increases due to increased lattice scattering of the electrons. The two mechanisms oppose each other, and their effects can be seen by observing the drain current at gate-source voltage of 20 V and 6 V in Figs. 5.10 – 5.12. Due to the reduction in threshold voltage, the 6 V gate-source voltage drain current actually increases with temperature going, while the 20 V gate-source voltage drain current decreases with increasing temperature due to increase in the on-state resistance of the drift region which becomes predominant at higher current levels. Accurate modeling of this effect is important to properly model the device over temperature. A schematic for DC characterization of the power MOSFET is shown in Fig. 5.13

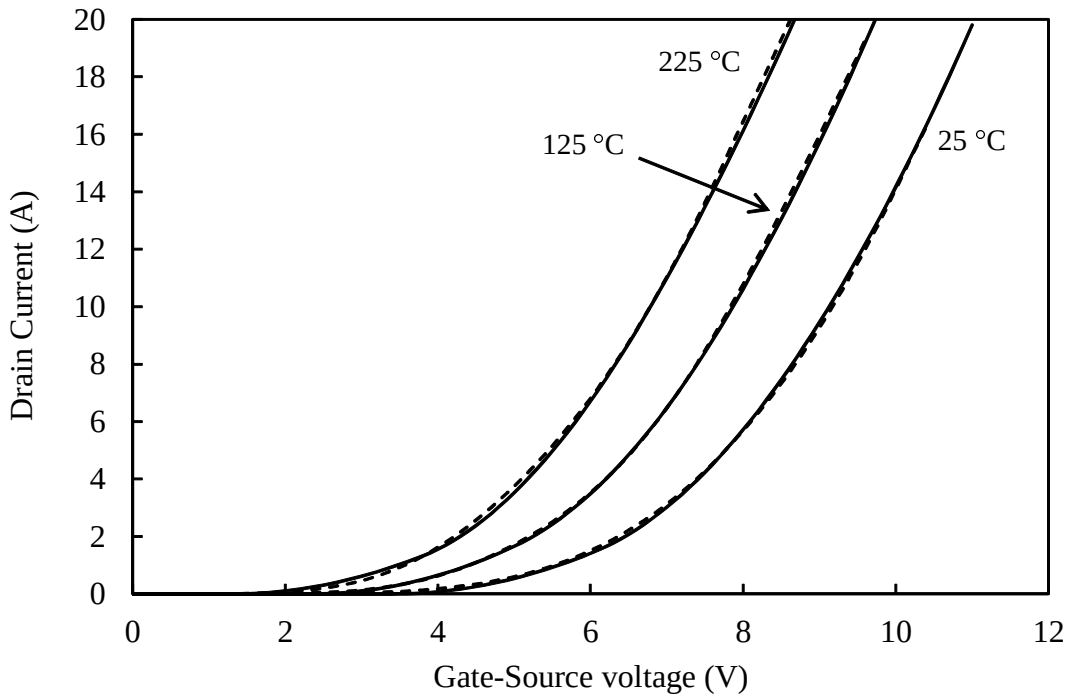


Fig. 5.9: Measured (dashed) and simulated (solid) input characteristics over temperature

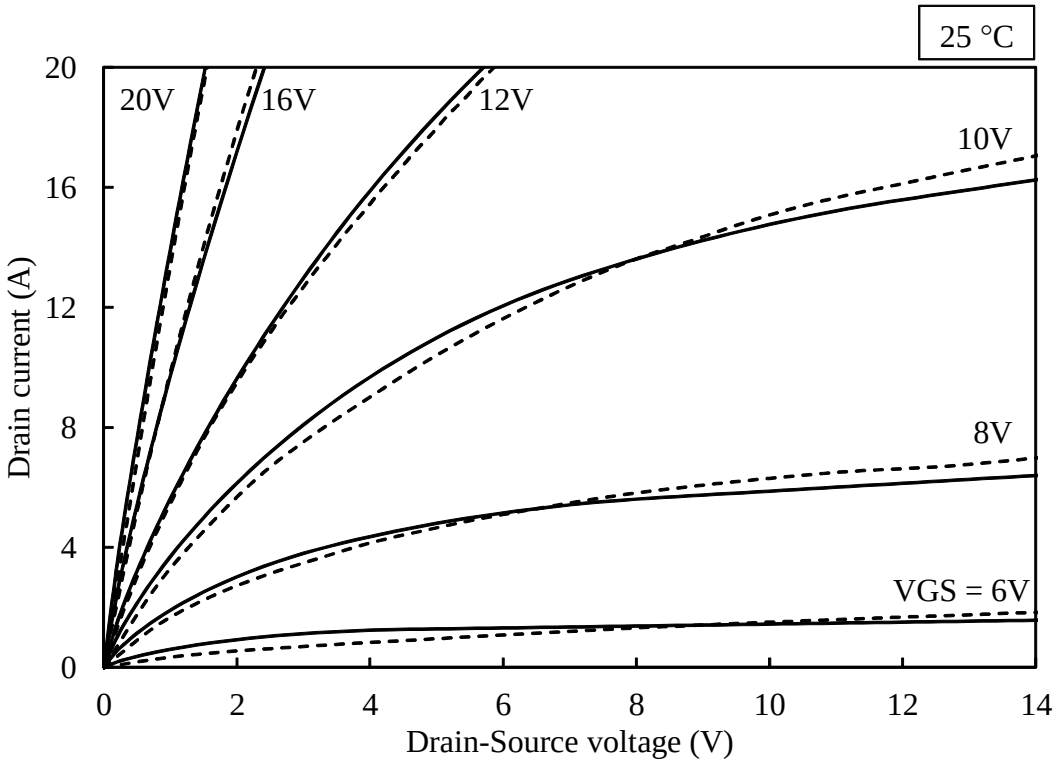


Fig. 5.10: Measured (dashed) and simulated (solid) output characteristics at 25 °C

5.4.2 Transient Performance

During the parameter extraction procedure (Section 5.3.3), the CV characteristics of the device were used to extract the transient capacitance parameters. However, in order to verify that the extracted capacitance parameters simulate the switching behavior of the device well, it was important to verify the performance of the model with device data from a transient test, like a resistive load switching test.

The switching performance of the the device was tested using a single pulse resistive load test as shown in Fig. 5.14. The pulse voltage signal was provided by an external gate-driver switching between 15 V and -8 V. A 41.7 Ω load was used which was characterized to have a 200 nH parasitic inductance. A 1200 V, 20 A Schottky diode from Semisouth (SDP20S120D) [108] was used as a

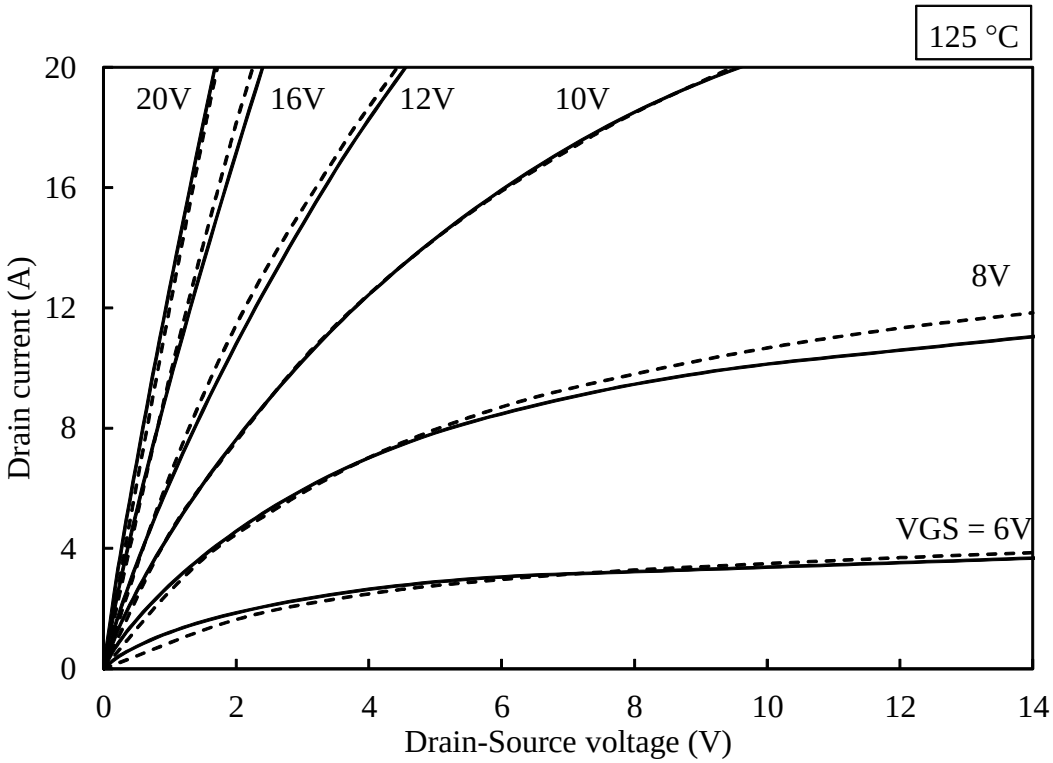


Fig. 5.11: Measured (dashed) and simulated (solid) output characteristics at 125 °C

free-wheeling diode in parallel to the load resistor. A 10 Ω resistor was connected to the gate of the power MOSFET to control the turn-on and turn-off times of the device. The DC bus voltage used for the setup was 200 V.

The measured and simulated drain voltage and current waveforms during turn-on are shown in Fig. 5.15 and 5.16. The gate-voltage during turn-on is shown in Fig. 5.17. The effect of the Miller effect through the non-linear gate-drain capacitance can be seen in the gate-voltage waveform. It is accurately modeled by the formulation of the gate-drain capacitance as described in Section 5.2.2. Good agreement is observed between the measurements and simulation, which lends confidence in the developed model. With the verification of the DC performance over temperature, C-V performance and the transient performance of the model with characterization data from the real device, the model validation is complete. The developed power MOSFET model has been

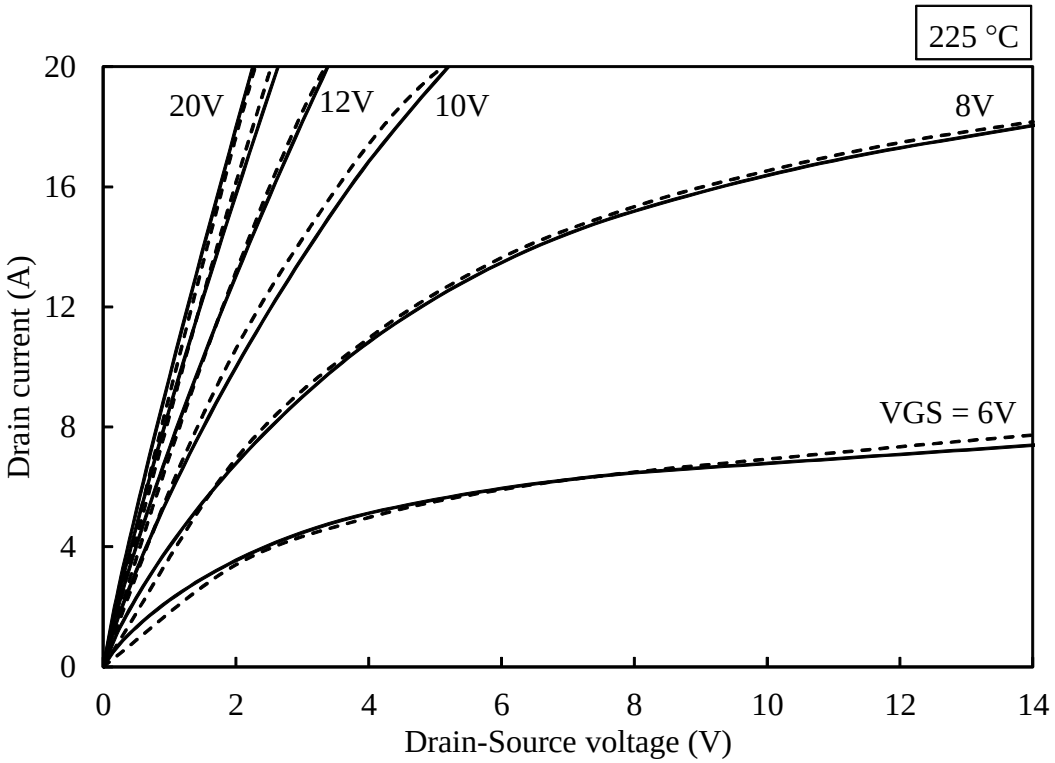


Fig. 5.12: Measured (dashed) and simulated (solid) output characteristics at 225 °C

used extensively in a number of different system-level simulations, and has also been validated for convergence and simulation performance.

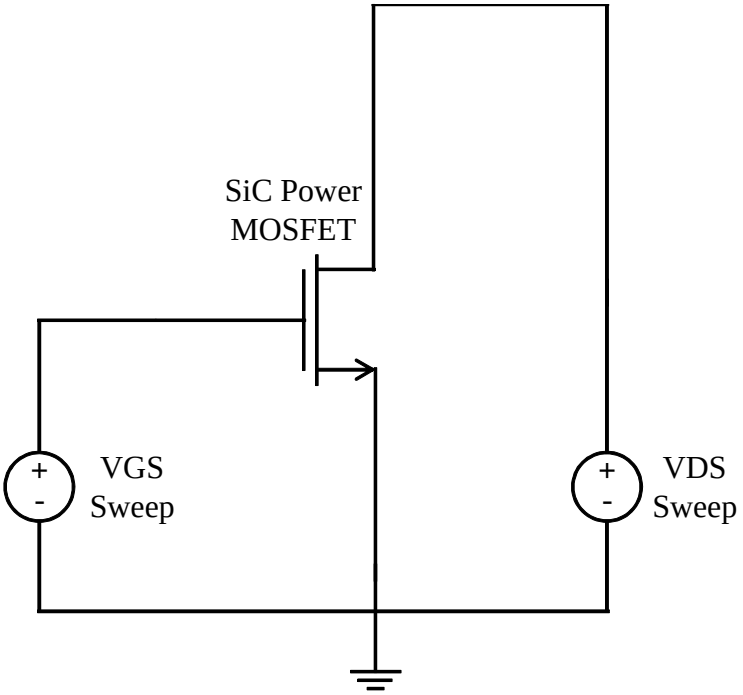


Fig. 5.13: Schematic for DC characterization

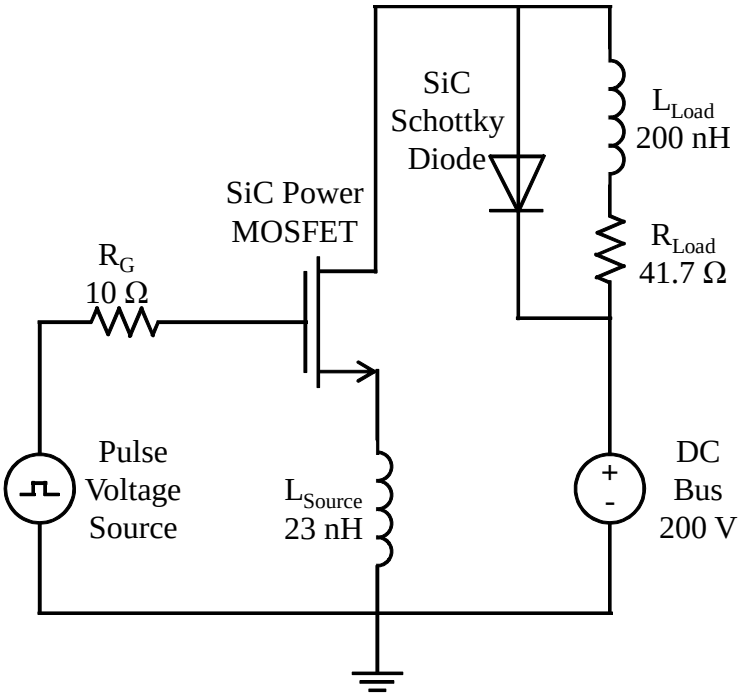


Fig. 5.14: Schematic for the resistive load switching test

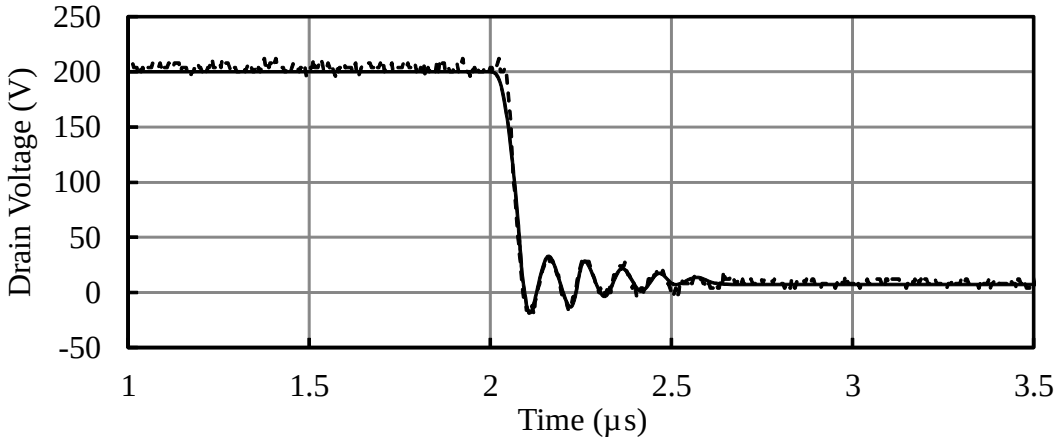


Fig. 5.15: Measured (dash) and simulated (solid) drain voltage waveform during turn-on

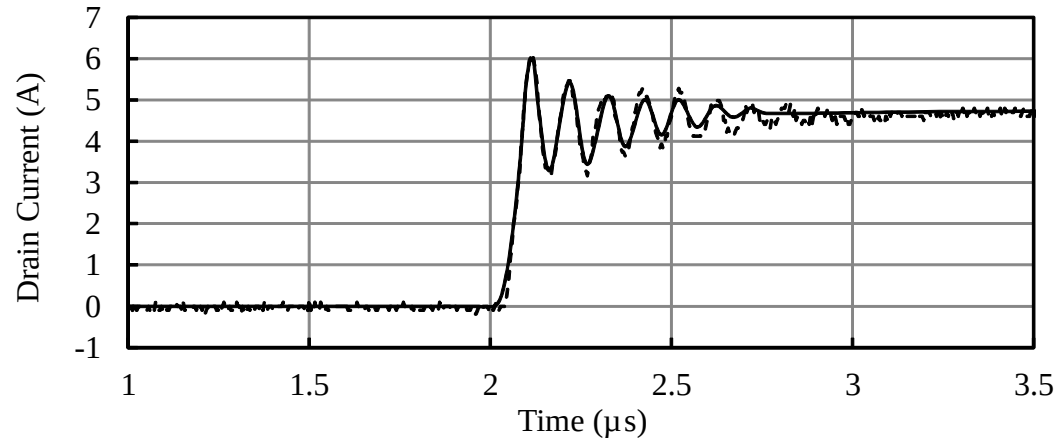


Fig. 5.16: Measured (dash) and simulated (solid) drain current waveform during turn-on

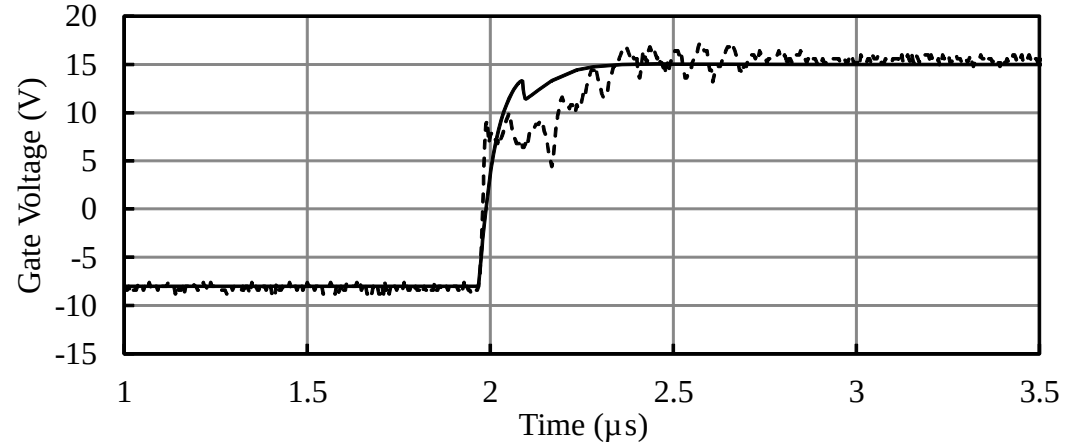


Fig. 5.17: Measured (dash) and simulated (solid) gate voltage waveform during turn-on

Table 5.1: Parameters in the Power MOSFET Model

Parameter	**Description**	**Classification**	**Value**
TEMPC	Reference Temperature (°C)	Initialization	25
A	Device active area (cm^{-2})	Initialization	0.02
AGD	Gate-drain active area (cm^{-2})	Initialization	0.013
CDSO	Drain-source zero-bias capacitance (F)	CV	5.5×10^{-10}
M	Drain-source depletion capacitance parameter	CV	0.3
COXO	Gate-oxide capacitance (F)	CV	2.6×10^{-12}
VFB	Effective Flat-band voltage (V)	CV	0.1
NA	P-Substrate doping (cm^{-3})	CV	3.1×10^{15}
CGSO	Gate-source overlap capacitance (F)	CV	1.6×10^{-9}
PVF	Transition parameter	DC	0.54
VT1	Channel 1 threshold voltage (V)	DC	3.5
VT2	Channel 2 threshold voltage (V)	DC	6.15
THETA1	Channel 1 transverse field reduction parameter (V^{-1})	DC	1.2×10^{-3}
THETA2	Channel 2 transverse field reduction parameter (V^{-1})	DC	1.2×10^{-3}
KP1	Channel 1 current gain parameter (A/V^2)	DC	0.36
KP2	Channel 2 current gain parameter (A/V^2)	DC	0.54
KF1	Channel 1 saturation gain factor	DC	3
KF2	Channel 2 saturation gain factor	DC	5
VA	Early voltage parameter (V)	DC	35
RS	Source resistance (Ω)	DC	0.02
VT1TEXP	VT1 Temperature Slope (V/T)	Temperature	-1.1×10^{-2}
VT2TEXP	VT2 Temperature Slope (V/T)	Temperature	-1.2×10^{-2}
KP1TEXP	KP1 Temperature Exponent	Temperature	0
KP2TEXP	KP2 Temperature Exponent	Temperature	-0.7
KF1TEXP	KF1 Temperature Exponent	Temperature	0
KF2TEXP	KF2 Temperature Exponent	Temperature	0
THETA1TEXP	THETA1 Temperature Exponent	Temperature	4.8
THETA2TEXP	THETA2 Temperature Exponent	Temperature	4.8
VATEXP	VA Temperature Slope (V/T)	Temperature	0

Chapter 6

Model Simulation Verification

This chapter is where the rubber meets the road, and the models described in previous chapters are put to test in large system level simulations. The first step in model verification is model validation with real device data. This has been presented in Chapters 4 and 5 in conjunction with the model development. While single instances of a compact model may follow the measured data well and converge for different bias conditions, when more than one device is introduced in a system with other components like other devices, resistors, capacitors etc., the compact model has to be mathematically well-formulated so that it converges for all simulation conditions. Model simulation verification is done to check the model for convergence problems, inconsistencies in large simulations, satisfactory simulation times and other metrics that are important when using the models.

The low voltage SiC MOSFET model was used to simulate and design a complete gate-driver chip in SiC. The gate-driver chip design contains over 20,000 instances of the low voltage SiC PSP model including paralleled MOSFETs to increase multiplicity M. The whole simulation system consisted of the gate driver circuit driving the power stage consisting of six power MOSFET model instances, each being hard-switched independently. In addition, parasitic elements were also been extracted from layout and used in the circuit. The entire system posed a very rigorous and rugged test-bench for the developed models. While a discussion of the complete gate-driver chip simulation is outside the scope of this document, results from the simulation of the voltage reference circuit, used in the gate driver chip have been presented here for validation of the models.

6.1 1.5 V Reference Circuit

Mayorga et al. have designed a 1.5 V reference circuit was designed using the developed models for the gate-driver chip. The gate driver chip operates with 0 V and 20 V available as inputs. It is desirable to be able to provide a negative V_{GS} to the power MOSFET during operation to be able to fully turn it off, especially at elevated temperatures. The negative V_{GS} is also important to provide a noise margin to the system. In order to obtain a negative V_{GS} for the power MOSFET using a 0 V to 20 V power supply, the 1.5 reference circuit was connected to the source of the power MOSFET, and the 0 V of the gate driver was connected to the gate of the power MOSFET. This enabled a V_{GS} swing of 20 V, with -1.5 V on the low side and 18.5 V on the high side, and provided the necessary negative V_{GS}.

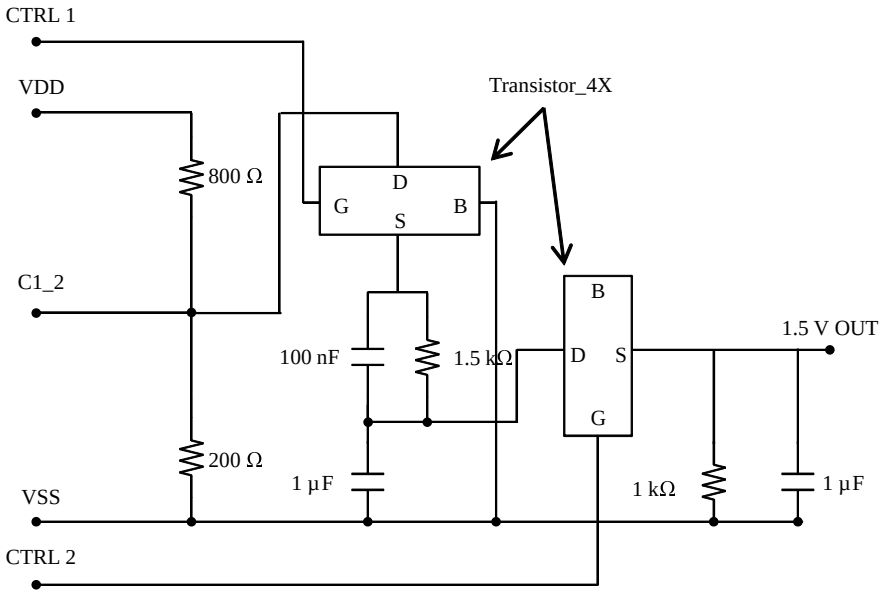


Fig. 6.1: Schematic of the 1.5 V reference circuit

The schematic of the 1.5 V reference circuit is shown in Fig. 6.1. It consisted of a voltage divider circuit, followed by a step-down capacitor circuit to switch the voltage down. The output

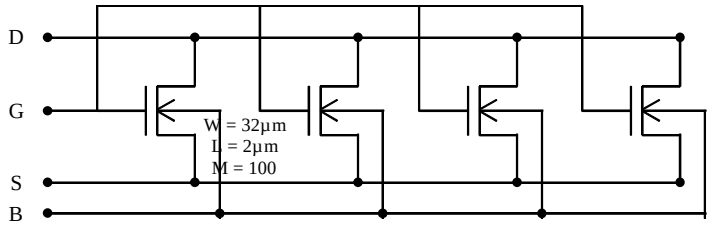


Fig. 6.2: Schematic of Transistor_4X block

of the circuit consisted of a capacitor that could provide the transient current required by the power MOSFET during turn-on and turn off (estimated to be ~1.5 A). The Transistor_4X block in the circuit comprised of four MOSFETs in parallel, each with 100 fingers as shown in Fig. 6.2. The transistors were controlled by complementary control signals CTRL1 and CTRL2, which were generated using ring-oscillator circuits on chip, which will not be discussed. The switched capacitor network was used to step the voltage down using the 1.5 kΩ and 1 kΩ resistors. The second Transistor_4X block allowed voltage sharing between the two large 1 μF capacitors and the 1 kΩ resistor provided a current path to ground.

The voltage reference circuit was connected to the source of the power MOSFET model in a clamped inductive test circuit to evaluate hard-switching losses. The schematic of the clamped inductive circuit is shown in in Fig. 6.3. The circuit was evaluated at a 50% PWM duty cycle. In a transient simulation, the current in the inductor ramps up with time, so the circuit cannot be operated indefinitely. Given the value of the inductor and the initial conditions, the final value of the current after any given number of cycles can be calculated by theory. If the system simulates correctly, the output of the 1.5 V reference circuit is not expected to change and maintain a steady value of 1.5 V.

The transient simulation of the clamped inductive circuit was performed as follows. The circuit was powered up by applying values of VDD and VSS at t = 0. At t = 4 μs, the output of the gate-

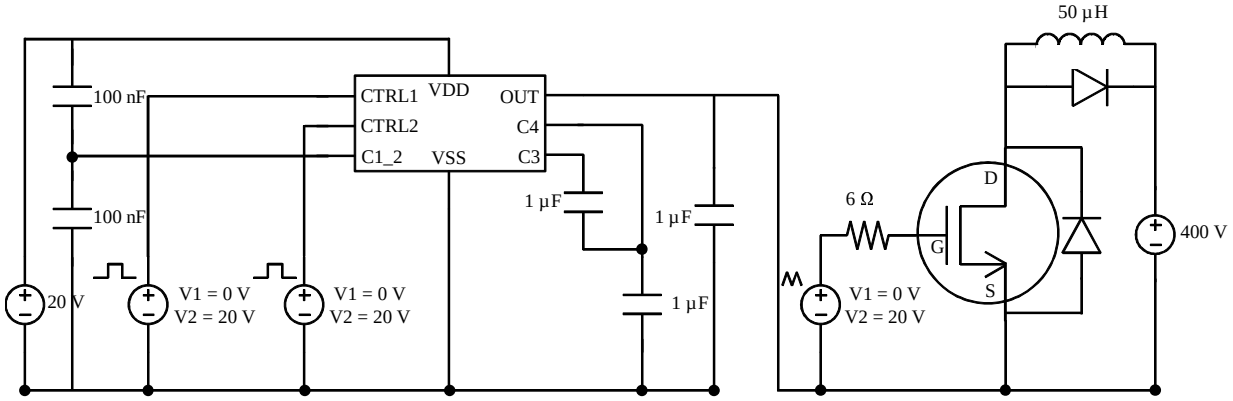


Fig. 6.3: Schematic of the clamped inductive circuit

driver was applied to the power MOSFET, and the gate-driver generated a gate-signal with a 50% duty cycle, 1 μs period and 2 ns rise and fall times. The gate driver became active at t = 4 μs to allow the voltage reference circuit ouput to stabilize at the 1.5 V value. The load inductance was set to 50 μH and the initial current in the inductor was 0 A. The DC link across the power MOSFET was 400 V. With the circuit setup, the inductor current was expected to ramp up at a rate of 8 A / μs. The final current in the inductor was determined by the on-time of the PWM signal, which was set to 1 μs.

Fig. 6.4 shows the power-up of the 1.5 V reference circuit from t = 0 s. The gate-signal to the power MOSFET was applied at t = 4 μs. Fig. 6.5 shows the simulated gate-voltage and gate-current of the power MOSFET, the load current in the inductor, and the output of the 1.5 V reference circuit during hard-switching of the power MOSFET. The inductor current was seen to increase as expected at a rate of 8 A / μs. The gate current in the power MOSFET was seen to peak at 1.5 A during turn on and turn off cycles. The shape of the waveforms and peak values verified the correct operation of the circuit.

The clamped inductive circuit validated the low voltage and power MOSFET models for the fol-

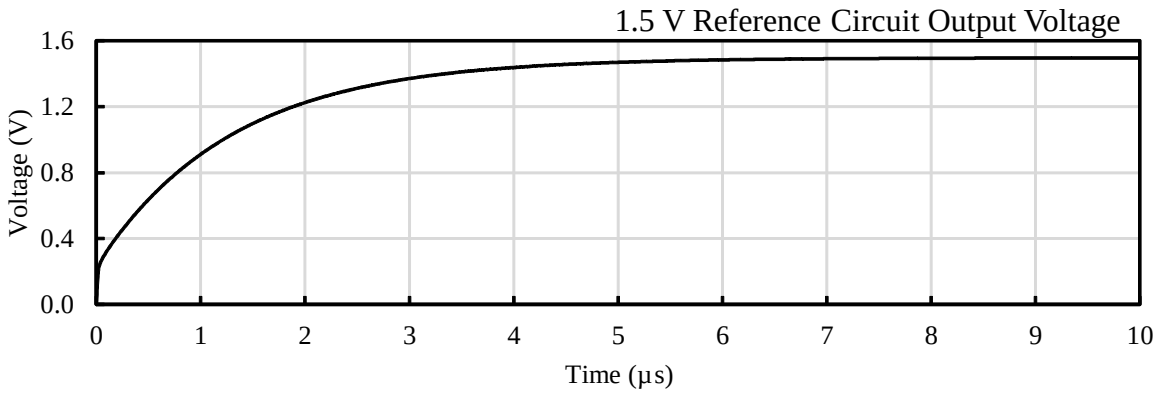


Fig. 6.4: Simulated output voltage of the 1.5 V reference circuit from turn-on to steady state

lowing criteria:

- **Hard switching**: In the clamped inductive circuit, the power MOSFET was driven hard by the low voltage gate-driver circuit. Thus, the proper operation of the circuit verified proper switching action of the power MOSFET model and the transient performance of the low voltage MOSFET model.

- **Digital simulation**: The control signals CTRL1 and CTRL2 were generated using ring oscillator circuits on-chip. Since ring-oscillators comprise of several stages of back-to-back inverters, the proper generation of control signals verified the proper transient operation of the low voltage MOSFET models.

- **Analog simulation**: The 1.5 V reference circuit generated an analog signal of 1.5 V irregardless of the output load conditions. The simulation results showed that the output of the 1.5 V reference circuit stayed constant at 1.5 V, and verified the analog behavior of the low voltage MOSFETs. Moreover, several other analog circuits were also designed on the chip including under-voltage lockout protection (UVLO), current sense amplifier and Schmitt trigger circuits using the low voltage MOSFET models.

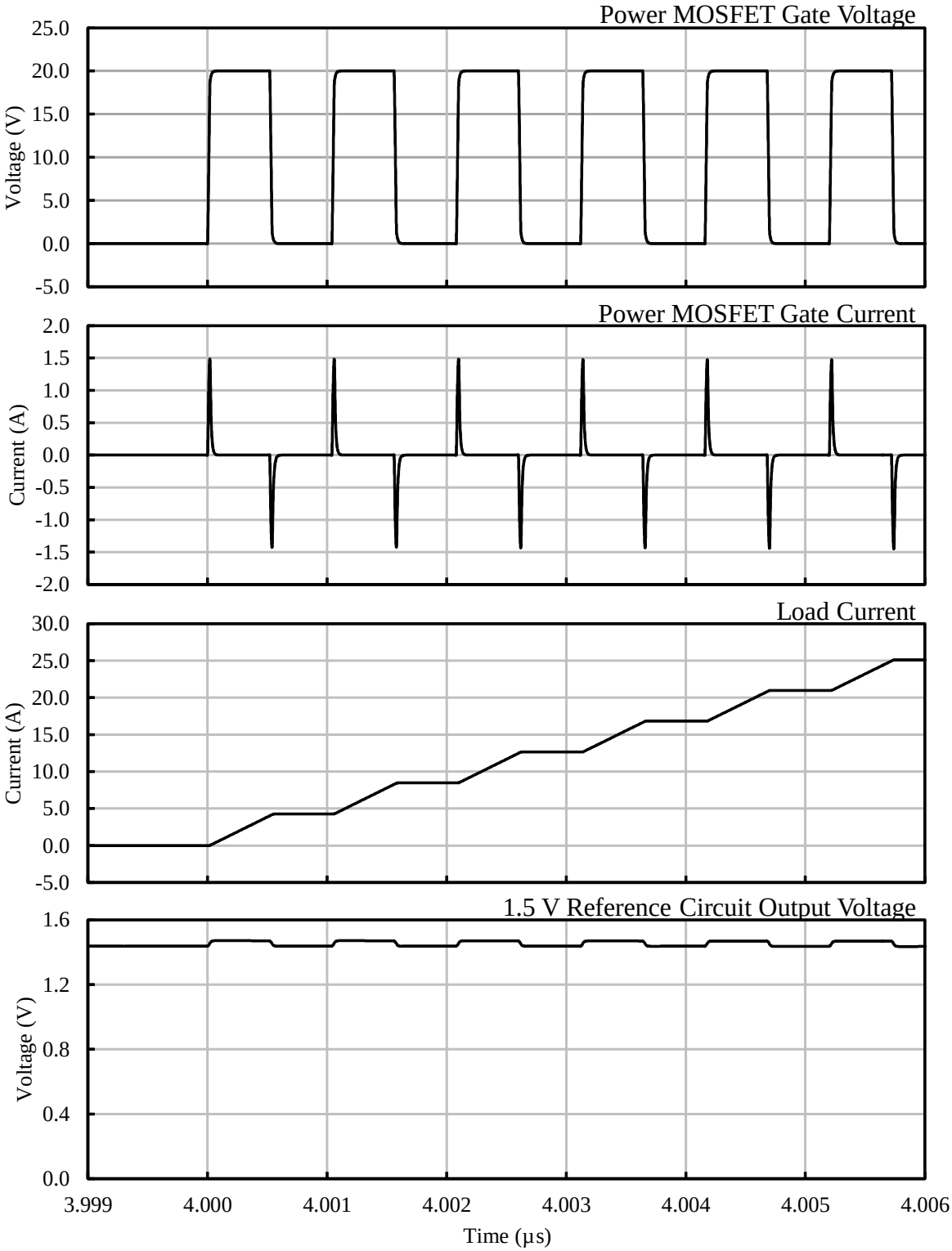


Fig. 6.5: Simulated waveforms of the clamped inductive circuit

- **Convergence**: Perhaps the most important result of the circuit simulation was that the models simulated without any convergence problems over the entire temperature range. In order to ensure convergence under all conditions, parasitic elements for the entire layout were extracted and fed back into the netlist of the clamped inductive circuit. The entire system with parasitics simulated successfully, verifying the absence of any convergence issues with the models

Chapter 7

Conclusion And Future Work

7.1 Summary

The objective of the work presented in this dissertation was to develop compact models for SiC low voltage and power MOSFETs, which would aid the design of integrated systems in SiC. Using the developed models, an integrated gate-driver chip (IGDC) in SiC was developed and is currently in fabrication. The IGDC will enable on-chip control of SiC power MOSFETs, which would result in operation at elevated temperatures and high frequency operation than what is currently possible with state of the art Si technology. The 2 μm SiC process from Cree has been characterized to show promising performance up to 225 °C for the development of low voltage SiC MOSFETs. Some fabrication problems like mobile ion contamination in the threshold adjust enhancement MOSFETs were discovered while characterizing the new process, and were relayed back to Cree to improve the process flow. A test chip was designed to characterize the new process, and it will serve as a template for future iterations of the process.

Using the test-chip, extensive characterization of low voltage SiC MOSFETs was done over a wide range of geometries and temperatures. Due to larger operating voltages in the SiC MOSFETs, short channel effects were seen at channel lengths of less than 4 μm. Moreover, the impact of interface states on the temperature behavior of SiC MOSFETs was also been characterized for a wide-range of geometries. Using the characterization data, a SiC version of the PSP compact model was developed with new equations for mobility, band-gap and intrinsic carrier concentration of 4H-SiC over temperature. In addition, the new PSP model was scaled over temperature and geometry

to better reflect the behavior of the SiC MOSFETs over temperature. For example, the on-state resistance of the enhancement MOSFETs decreases with temperature, contrary to what is found for Si devices. The main reason for this behavior is the reduced occupancy of interface states at elevated temperatures, which results in more electrons available for conduction in the channel region for any given gate voltage. This effect was captured by using the appropriate temperature scaling parameters in the enhancement MOSFET model.

Another important impact of this work is that a solid foundation has been provided for the development of a closed form analytical compact model with a mathematical description of the large density of interface states found in SiC low voltage MOSFET surfaces. The biggest challenge currently faced by SiC MOSFETs is the presence of a large density of interface states, and it is important to account for the effect of the interface state occupancy to yield physically accurate device characteristics. This work presents a numerical representation of the fundamental surface potential equation in the presence of the interface states distribution, found in 4H-SiC.

A temperature scaled compact model for the commercially available 1200 V, 20 A SiC power MOSFET was also developed. The model shows excellent agreement with measured device characteristics over temperature. In addition, the model was tested for convergence behavior in several power system applications. The power MOSFET model also features a charge-conserving capacitance equation formulation that is continuous across the entire bias range. The power MOSFET model is available in the Verilog-A and MAST modeling languages.

7.2 Primary Contributions

The primary contributions of this work are:

- Design, layout and fabrication of a test-chip to characterize new 2 μm process in SiC
- Characterization of low voltage enhancement and depletion SiC MOSFETs of different geometries over wide temperature
- Development of modified geometry and temperature scaled PSP low voltage compact model for SiC MOSFETs
- Formulation of the numerical equation for the surface potential equation in the presence of an interface state distribution found in 4H-SiC surfaces
- Development of the power MOSFET model, and optimization of the model for the commercially available 1200 V, 20 A power MOSFET
- Validation of the developed models by enabling the design of a complete integrated gate-driver chip on SiC

7.3 Future Work

The focus of this work has been to deliver compact models for SiC low voltage MOSFETs and the commercially available 1200 V, 20 A SiC power MOSFET. During characterization of the low voltage MOSFETs, the main focus has been on the DC and CV characteristics of the devices over temperature. The low voltage MOSFETs can also be used for high frequency operation. A thorough study of the low voltage MOSFETs for their high frequency small-signal performance over

temperature would be of interest to the industrial and academic community. Another important performance metric that should be analyzed is the noise performance of the devices. The noise behavior of the low voltage MOSFETs over temperature is important when designing amplifiers and RF-circuits.

An area of extension of the low voltage model is the extraction of temperature scaling parameters for the geometry scaling parameters. In the current version of the model, the temperature scaling and geometry scaling performance of the devices have been assumed to be independent of each other and extracted independently. A more accurate parameter set would also include the temperature scaling of the geometry scaling parameters, and could be developed in future iterations of the model.

The study of interface states in SiC metal-oxide surfaces has been a perennial topic of interest in the SiC community. Currently, the large density of interface states in SiC MOSFETs heavily influences the performance of these devices. Accurate modeling of interface states is vital while designing circuits with these devices. The numerical model developed in this work for including the effect of interface states in the surface potential equation provides a solid foundation for the development of a new analytical approximate solution for the surface potential equation in the presence of interface states. Such a solution can be directly implemented in the native PSP model, to allow a geometry and temperature scaled compact formulation for SiC low voltage MOSFETs in the presence of interface states.

7.4 Conclusion

With rapid advancements in SiC processing technology, full-scale development of integrated circuits in SiC is not a distant dream. Designing integrated circuits in SiC would result in highly integrated systems, which can operate at high power densities in harsh environments with high efficiency. The characterization data presented in this work provides valuable information to the device manufacturers, who can improve their existing processes to get a better overall process. Better process result in higher circuit yields and lower costs, which is one major factor that will govern the adoption of SiC in the near future.

It is often the case that circuits are only as good as the models used to design them with. Having accurate and robust compact models for a new process is a tremendous asset, and provide the most basic building blocks to design circuits with. This work aims to fill the void of low voltage SiC compact models, and pave the way for designers to work their magic with SiC. The integration of low voltage and high voltage SiC components on the same chip will revolutionize the face of power systems of the future.

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