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A METHODOLOGY FOR IMPLEMENTING RF BISTS IN PRODUCTION TESTING TO REPLACE RF CONVENTIONAL TESTS

A METHODOLOGY FOR IMPLEMENTING RF BISTS IN PRODUCTION TESTING TO REPLACE RF CONVENTIONAL TESTS

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Microelectronics-Photonics

By

Deepa Mannath University of Pune Bachelor of Engineering, 2000 Texas Tech University Master of Science in Electrical Engineering, 2002

> December 2010 University of Arkansas

ABSTRACT

Production testing of Radio Frequency (RF) devices is challenging due to the complex nature of the tests that have to be performed to verify functionality. In this dissertation a methodology to replace the complex and expensive RF functional tests with defect-oriented Built-in Self Tests (BiSTs) is detailed. If a design has sufficient margin to RF specifications then RF tests can be replaced with structural tests using a new data analysis technique called quadrant analysis, which is presented. Data from the analysis of over one million production units of said System on Chip (SoC) is presented along with the results of the analysis. The BiST techniques that have been used are discussed and a Texas Instruments 65 nm RF SoC with a Bluetooth and a FM core was used as a case study. The defect models that were used to develop the BiSTs are discussed as well. The scenario in which a design does not have sufficient margin to specification is also discussed. The data analysis method required in such a case is a regression analysis and the data from such an analysis is shown.

The results prove that it is possible to replace expensive RF conventional tests with structural tests and that modern RFCMOS process technology and advances in design like the Digital Radio Processor (DRPTM) technology enable this. The Defective Parts Per Million (DPPM) impact of making this replacement is 27 units and is acceptable for RFCMOS high volume products. Finally, data showing test cost reduction of about 38% that resulted from the elimination of RF conventional tests is presented.

This thesis is approved for recommendation to the Graduate Council

Thesis Director:

Dr. Simon S. Ang

Thesis Committee:

Dr. Randy Brown

Dr. Jia Di

Ricky D. Hudgens (ex-officio)

Prof. Kenneth Vickers

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CHAPTER 1: INTRODUCTION

1.1 A Brief History of Telecommunications and the Cellular Landscape

Hedy Lamarr (born Hedy Kiesler Markey) was an unlikely inventor. A Germanborn beauty trained in acting, she moved to Hollywood in the 1930s and applied for a patent on a "Secret Communication System" on June 10 1941 [1], with George Antheil. They devised a radio-control mechanism in which the transmitted carrier frequency would jump around via pre-arranged, randomized and non-repeating frequency hopping code. The mechanism had "slotted paper rolls like player-piano rolls that synchronized the frequency changes in transmitter and receiver. It also used exactly eighty-eight frequencies, the number of keys on a piano". The duo tried unsuccessfully to sell the idea to the US Navy at the time to implement radio control mechanisms for torpedoes using frequency hopping so that the radio signals could not be "jammed" by the enemy.

This invention, even after the patent expired, was the basis of modern digital communications systems. Advances in Communications Theory made by pioneers like Shannon[2], Nyquist[3] and Hartley[4] followed by advances in electronics technology have played a major role in developing the system which cellular phone systems worldwide use today.

Mobile devices are now ubiquitous and an integral part of our daily lives. The first official mobile phone is said to have been used in 1946 by the police in Sweden, but the phone was connected to the telephone network and the police car battery was drained after only 6 phone calls. Modern cell phones rely on hexagonal cells and cell phone towers which were devised by Bell Labs' engineers in the late 1940s; the electronics and

other required technologies, however took decades to mature. In 1983 Motorola brought to the market a truly portable cellular phone called the DynaTAC 8000X, which used the purely analog Advanced Mobile Phone System (AMPS) mobile technology, weighed about 28 ounces and was known as "brick" due to its shape. The second generation (2G) phones that followed, were able to operate on mobile systems like Group Speciale Mobile (GSM) and Code Division Multiple Access (CDMA), weighed a few hundred grams and were truly portable because smaller batteries became available. Today we can text, call, navigate, email and watch television using cell phones. Figure 1.1 shows Motorola's DYNATAC 8000X [5] and the Apple iPhone [6] for comparison.



Figure 1.1: The DYNATAC 8000X and iPhone

Cellular phones have also become great enablers of socio-economic change in various parts of the world. The International Telecommunications Union (ITU), which is a United Nations agency that deals with information and communication technology issues, reports that in 2009 there were approximately 4.1 billion cell phone subscribers worldwide [7]. The cell phone today is a commodity and is available both as a basic,

bare-bones device that can be used only for making calls and as a high-end gadget that is virtually a laptop on the go.

The main radio chip, which is actually used to transmit and receive voice information as well as the peripheral devices that support Frequency Modulation (FM), Wireless Local Area Network (WLAN), Global Positioning System (GPS) and Bluetooth (BT) functionality on a cell phone are commoditized. Average Unit Price (AUP) of these peripherals in particular, is very low and companies like Texas Instruments (TI) that design, manufacture and supply these, are under immense pressure to provide the least expensive device with the most functionality.

The device that was chosen for this research and analysis is one such commodity part, called Orca, which provides BT and FM functionality as a single–chip solution.

1.2 Objectives of this dissertation

In this dissertation the details of a new methodology for implementing BiSTs in RF circuits along with some novel test methods will be presented. The goal of this research is to demonstrate that RF circuits can be tested with defect-oriented tests instead of functional or specification-based tests, leading to test time reduction, and how this would enable meeting test cost targets on the Orca device.

1.3 Organization of the dissertation

The chapters are organized such that the background material like the architecture of the device and the issues seen in production testing of such devices along with the reasons for BiST are covered in Chapters 2, 3 and 4. Chapter 5 is a short summary of digital DFT, its origins, the fault models used therein and the connection between digital DFT and RF BiST. Chapter 6 covers the fault models observed in RF devices while Chapter 7 contains descriptions of the BiSTs implemented to detect those faults.

The methodology for implementing these BiSTs in a new design is detailed in Chapter 8, while Chapters 9 and 10 cover the novel data analysis method used and the results of this analysis. Finally, conclusions are stated and future work outlined in Chapter 11.

CHAPTER 2: THE DEVICE AND ITS ARCHITECTURE

2.1 Introduction

Orca, Texas Instruments' BT+FM SoC in the 65 nm CMOS technology node uses the DRPTM technology, which enables low size, power and cost. It can support Bluetooth specification v2.1 and the Enhanced Data Rate (EDR) standard and includes a fully embedded FM core and Radio Data System (RDS) receiver and transmitter [8]. Figure 2.1 [8] is a block diagram showing the main functional blocks within the Orca device.

2.1 Device Architecture

The blocks labeled Bluetooth Radio and FM Radio in Figure 2.1 are the two cores containing the RF circuits that require the RF Conventional (RFC) tests.

Bluetooth is a global wireless standard operating in the unlicensed ISM band at 2.4 GHz. BT devices must be robust in order to combat the noisy and crowded environment in this band that is also occupied by WLAN devices, Microwave ovens, etc. These devices are made robust mainly by using 3 techniques: Frequency-Hopping Spread Spectrum (FHSS) modulation, short data packets, and adaptive power control [9].



Figure 2.1: Orca Functional Block Diagram

Incidentally, Bluetooth is named after the Danish King Harald Blåtand (meaning Bluetooth). He is said to have united the Scandinavian people in the 10th century. In the same way, the main goal of Bluetooth technology is to unite personal computing devices in a wireless fashion.

The first known radio news program is said to have been broadcast on August 31, 1920 by a station called 8MK in Detroit, Michigan [10]. Amplitude Modulation (AM) was used, but FM was soon found to be superior since it was not affected by static and interference like AM.

2.2 The BT Core

Figure 2.2 shows the block diagram of the BT core. The transmitter path consists of the digital blocks that support transmission (TX digital), the amplitude modulation circuitry, the oscillator (OSC), and the Pre-Power Amplifier (PPA).



Figure 2.2: BT core block diagram

The receiver path consists of the Low Noise Amplifier (LNA), the Transconductance Amplifiers for I and Q paths (TA_I and TA_Q), I and Q mixers, Feedback Digital to Analog Converter (FBDAC), Intermediate Frequency Amplifiers for I and Q paths (IFA_I and IFA_Q), Analog to Digital Convertors (ADC) for I and Q paths (ADC_I and ADC_Q), Cascaded integrator-comb (CIC) filters for I and Q paths (CIC_I and CIC_Q) and Goertzel energy estimation hardware followed by digital blocks that support reception (not shown).

The BT transceiver architecture comprises of both a very low IF (I/Q) receiver and a direct (polar) modulation transmitter. It has a single digitally controlled oscillator (DCO) core which produces a dual frequency band output: 4.8 GHz & 6.4 GHz. The ISM band frequency of 2.4 GHz is created by either dividing the 1st frequency by 2 or by mixing two divisions of the 2nd frequency (achieving a 3/8 product). This special mode allows the DCO to oscillate without experiencing any interference or RF pulling from the 2nd harmonic of the transmitted signal at the PA output. The original 2nd multiple of the ISM frequency is used for the receiver local oscillator. A block diagram of the RF/Analog section of the Bluetooth core is shown in Figure 2.2.

Very Low Intermediate Frequency (VLIF)

The BT receiver includes 3 gain stages, one before down conversion to IF and two after. The LNA located before the down converting mixer is common to both I & Q chains, while the rest of the blocks are duplicated for each chain. The DC level for each of the chains, originating mainly from self mixing of input RF signal at the mixer ports, is separately corrected for the I and Q paths and for each of the IF gain stages. Correction is implemented as open loop control over the Feedback DAC which cancels imbalance between the two differential lines of the IF signal. The Local Oscillator port of each mixer is supplied with a dual phase (0° & 90°) 2.4 GHz signal originating from the DCO core 4.8 GHz output. The different phases are created in the analog RF dividers inside the core, and then buffered into the two mixer inputs. Phase noise properties of this LO input are extremely crucial for performance as they are the main limiting factor when operating in the region out of sensitivity signal strength (ultimate SNR). This is due to the fact that LO phase noise properties will appear directly on the down converted IF signal sampled by ADC.

Polar Modulation Transmitter Architecture

In direct (or polar) modulation, the variable frequency and/or amplitude information to be applied on the transmitter is not created by a combination of orthogonal data traces (i.e., I & Q), but rather it is introduced directly to the transmitting hardware. In the Orca device, these modulation inputs are referred to as Frequency Control Word (FCW) and Amplitude Control Word (ACW), respectively. The All Digital PLL (ADPLL) [11] block in this device has the unique capability to not only lock the LO or RF carrier signal in place but also to modulate its phase and frequency according to digital data input. In a similar manner, there is a power amplifier which is structured as an array of power transistors, capable of switching in and out of the actual operation. In this way, amplitude modulation may be applied and controlled via translation of the requested amplitude into a number of devices transmitting RF power into the antenna or device RF port. In spite of having a lot of advantages, this architecture also has its share of challenges, like ensuring extreme accuracy and control over the DCO gain (KDCO),

phase noise performance of the output RF signal required to shift during locked state, and the linearity of the PA response to ACW input variation.

2.3 The FM core

The FM core block diagram in Figure 2.3 shows the RX path, the TX path, and the Audio block. The TX path consists of the ADCs (ADCL and ADCR) which digitize the analog Audio data, the TX digital block which consists of the RDS encoder and the Stereo encoder, the oscillator, the triangular wave generator (TRIGEN), the PPA, and PA. These are followed by a tunable capacitor (CTUNE) which is used for impedance matching so that the maximum power transfer can be achieved.



Figure 2.3: FM core block diagram

The envelope detector block can be switched in so that transmitted signal power can be digitized with the RX ADC. This is used both in the functional mode and for several of the BiSTs which will be described later on. The RX path consists of LNAs for the I and Q paths (LNAM and LNAP) followed by mixers, filters, TAs, and ADCs dedicated to these two paths. The RX digital block consists of the RDS decoder and the Stereo decoder and it also produces digital audio data which gets converted to analog format and can be picked up at the left and right output pins (FMLOUT and FMROUT) at a 1 kHz rate.

3.1 Why Test?

Figure 3.1 depicts on a very high level the steps that are followed during the creation of a VLSI device.



Figure 3.1: Product Development Flow

The marketing team solicits requirements and needs from the customer. This is translated into product requirements documents, and eventually gets converted to system and block level specifications by system and block designers. This is followed by the design of the device which includes logic design and layout and is followed by fabrication. After fabrication the device goes through production test which may be divided into wafer level probe and final test after packaging for Ball Grid Array (BGA) devices or wafer-level test for Wafers Scale Package (WSP) devices. If a device fails production testing, the failure could be due to one or more of the following:

- The device had a defect which was introduced during fabrication
- The design was faulty
- The device did not meet specifications
- The test was faulty

Testing must detect all of the above four conditions and diagnosis can be used to determine which of these caused the test to fail. Hence, testing must be correct and effective to maintain the quality of the devices shipped to customers. Testing done at various points in the fabrication line can detect the cause of defects before they have done much damage and before additional resources have been spent manufacturing a potentially bad device. A good test strategy thus enables economical production of devices. Thus, quality and economy are the two main benefits of testing, making it a crucial part of the product development flow.

3.2 Test Complexity

Moore's law dictates that the number of transistors on an integrated circuit doubles every 18 to 24 months [12]. In addition to this, modern wireless devices have reached new levels of integration in recent years with multiple radio platforms and complex digital logic appearing on a single silicon die. This has led to smaller, faster devices capable of multiple RF modulation standards such as WLAN, FM, GPS and BT simultaneously. These Systems on Chip (SoCs) are sold for around \$1 to \$3 to service a market that requires these to be manufactured in the billions. Hence, their test cost budget is very low and this poses new challenges to test design and implementation.

The increases in transistor density and integration have also raised test complexity. Equation 3.1, first proposed by E. F. Rent at IBM [13] relates the number of device pins N_p to the number of transistors N_t .

$$N_p = k\sqrt{N_t}$$
 Equation 3.1

Increases in device pins leads to increased demands on the test equipment; the tester now must be capable of providing more power supplies, handling more digital pins, and processing more analog and RF signals. This limits the number of devices that can be tested simultaneously on any one tester, because the tester resources must be divided among device pins.

3.3 Types of Testing

3.3.1 Characterization Testing

This type of testing verifies that a new design is correct and that all the functional specifications are met. It determines the limits of device operation by running functional tests, probing internal nodes of the device, and making AC and DC type measurements.

One "lot" of silicon wafers normally has 25 wafers and the cost of processing a single wafer depends on the wafer size, the number of mask levels, and the technology node. For example, it costs several thousands of dollars to process a 300mm wafer with 25 mask levels using the 65 nm technology. So, when a new design is in the works, the process, design and product engineers together create a Design of Experiments (DOE). One or more wafers are processed according to the parameters defined in the DOE.

Normally PMOS and NMOS transistor drive currents, metal line widths, nwell resistor strength and other parameters that may affect device functionality are selected to be varied in the DOE. These devices are then tested across different temperatures and voltages so that device operation at various Process Voltage and Temperature (PVT) corners can be studied. It is desirable to test for the worst case because the device passing the worst case tests should work for average conditions.

Characterization data is used to diagnose design issues, to determine the device's characteristics to specifications, and also to develop a production program which is a subset of the characterization program.

Typically characterization is performed on a characterization "bench" using specialized tools like Spectrum Analyzers, FM Analyzers, and Communication Bluetooth Testers, etc. Increasingly, characterization is performed on Automated Test Equipment (ATE) whenever possible so that more devices can be tested, yielding more data for statistical calculations.

3.3.2 Production Testing

The tests performed in production are not as comprehensive as those performed during characterization, but they also must ensure that quality requirements are met by preventing shipment of defective devices. Production test time is very important since it translates into a recurring cost on every device that is tested. Hence every effort is made to keep the production test time to a minimum while guaranteeing quality. Production tests verify that the part does not have a manufacturing defect that will prevent proper functionality and are go/no-go type tests that may not have enough information to help identify faults.

Every organization has their testers of choice: most use testers from vendors like Teradyne and Eagle while some have their testers built in-house. TI's in-house tester is called the Very Low Cost Tester (VLCT) and is the tester used for testing Orca devices in production. These testers maybe capable of testing several devices in parallel (multisite testing). It is important to state here that there may be several "insertions" in the production test flow, i.e., the wafer or singulated device maybe tested several times on various testers, under multiple conditions with different test programs. Let us consider a BGA device for example. Immediately after wafer fabrication, the wafer is tested as a whole on a prober. In this case, the test head which holds the Prober Interface Board (PIB) with the socket heads is stationary while the prober moves the wafer. This insertion is called "Multiprobe" and may be the first insertion for a BGA device before it is singulated and packaged or it may be the only insertion for a WSP device which may not be tested after singulation. In case of BGA devices, after the wafer is singulated and the units are packaged, they go through a second insertion called Final Test, where the Device Interface Board (DIB) with the socket is connected via POGOTM pins to the test head. A handler is used to insert packaged devices into the socket for testing. Although it is desirable to perform production test only at room temperature, there may be design issues that require testing to be conducted at hot or cold temperatures. This complicates the test setup further.

3.3.3 Burn-in Testing

This type of testing checks the reliability of devices. During burn-in test, devices are subjected to production tests at high temperature and over-voltage stress for several hours. There are two types of reliability failures in most semiconductor devices: infant mortality failures and freak failures. Infant mortality failures are caused mostly due to design sensitivities and process variations and can be screened out by a short term burn-in of around 10-30 hours, while freak failures exhibit reliability issues that can occur in normal devices and require around 100-1,000 hours of burn-in [14].

3.4 Common test categories in the production flow and their ranking

The main categories of tests in the production program are as described in the following pages.

3.4.1 Continuity Tests

During continuity testing, the presence of on-chip ESD protection circuits is detected in order to verify that each device pin can be connected to the tester without electrical shorts or opens. These circuits conduct excess ESD current to the ground or power planes when the voltage at the pin exceeds one diode drop above or below the power or ground voltage. If a device fails continuity testing, then no further tests are conducted to prevent damage to the tester pins. These tests are very important and all device pins with protection circuits are tested for continuity.

3.4.2 On-Die Parametric Tests (ODP)

The fabrication facilities monitor hundreds of process parameters inline during wafer processing to make sure all process specifications are within limits. Special test structures are included in every device to monitor process variation during production testing. These test structures are used to measure NMOS and PMOS drive currents and are excellent indicators of the process spread.

3.4.3 Digital DFT

Digital tests are created though ATPG using automated tools from Mentor, Cadence, etc. Digital DFT is a combination of mostly patterns that cover both stuck-at structural and at speed parametric type defects. Also, digital logic circuits have very high design margins, so the digital DFT is mostly catching structural type defects versus guarding a tight parametric distribution. This is the ideal scenario for obtaining a low test cost. These vectors or patterns are executed while the device voltage supplies are held at certain levels where marginality is known to exist from device characterization.

3.4.4 Trim and EFUSE

Band gaps have to be measured and calibrated to the right voltage levels because they are used as reference voltage for the LDOs in the device. The band gap voltage is trimmable by blowing fuses called Electronic Fuses (EFUSEs) and the correct setting is permanently stored. EFUSEs are also blown to store a number that is unique to every device called Die ID.

3.4.5 Memory Tests

Memory test patterns are also automatically generated and executed within the device.

3.4.6 Leakage currents

Leakage tests provide a fast and easy way to detect devices with fabrication issues. Leakage currents can be an indication of several physical defects such as particulate contaminants that can cause opens or shorts as well as bad design practices. High leakage can also indicate devices that appear to be functional early on but maybe subject to early failure known as infant mortality. When a voltage is applied to a highimpedance device pin, a finite amount of current will normally flow out of the pin. In functional mode, high leakage current leads to shorter battery life for wireless devices. Hence, most customers have leakage current specifications for digital and analog pins. This is measured by forcing a DC voltage at the input or output pin and measuring the current flowing into or out of that pin.

3.4.7 Supply Currents

Supply current measurements are another way to detect gross defects. In addition to measuring the supply currents with the entire device on, various blocks in the device can be activated using digital test patterns and supply currents can be measured to check which particular block has gross defects.

3.4.8 LDO tests

The output voltage of LDOs is tested; load regulation and line regulations tests are also performed on LDOs.

3.4.9 Pin Voltage tests

The voltages at the digital pins are measured while a current is applied.

3.4.10 RF/Analog BiSTs

BiSTs are implemented to test the various analog and RF blocks in the device.

3.4.11 RF Conventional Tests

These tests will be discussed in Section 3.5 and rank very low on this list because of their test time impact.

The most economical test solution would use the lowest cost test to remove a particular type of defect. In this dissertation a new system for ranking production tests according to the percentage of defective units they detect and the amount of time they
require to make that determination is proposed. This is one step in a process that will eventually eliminate RFC tests. This first step defines a hierarchy for redundant kills that will assign credit to the cheapest test. At the end the expensive RFC tests will only be credited for defects that they detect on their own. For example, a test that detects 2% of defective devices in 10% of the total test time will have a rank of 20 (after multiplying the quotient by 100 to eliminate too many numbers after the decimal), while a test that detects the same number of defective devices in 5% of the total test time will have a higher rank of 40. Test Rank is defined in Equation 3.2.

Test Rank =
$$\frac{\text{Defect Detection Rate }(\%)}{\text{Test Time }(\%)} *100$$
 Equation 3.2

3.5 Typical BT RFC Production Tests

RF signal levels span a wide range and RF measurements are often expressed in decibels. This wide range cannot be accommodated on a linear scale. So, the decibel compresses it by using logarithmic units. When there is a change of a factor of 10 there are equal increments on a decibel scale. Also, measurements with the decibel scale better reflect the way humans hear.

To obtain a decibel the ratio of two power measurements or the ratio of two voltages is calculated and expressed in logarithmic units. Equations 3.3 and 3.4 define the decibel for power and voltage measurements.

$$P_{dB} = 10 * \log_{10-} \frac{P_1}{P_0}$$
 Equation 3.3

$$G_{dB} = 20 * \log_{10-} \frac{V_1}{V_0}$$
 Equation 3.4

Traditionally, the tests done on BT devices check for functionality and include tests that check the transmitted spectrum, modulation characteristics, accuracy and drift of the carrier frequency and BER measurements for sensitivity, carrier-to-interferer, blocking, and intermodulation conditions on the receive side. This section covers the details of these tests to illustrate their complexity as well as to help understand the functional coverage they provide.

Information regarding Bluetooth modulation is readily available from specifications provided by the Bluetooth Special Interest Group (SIG) [15]. A Bluetooth packet is shown in Figure 3.2. The packet contains an access code, a header, and payload. The various wireless tests may or may not use portions of the packet. The tester must be able to isolate to a specific region in the packet as needed.



Figure 3.2: Bluetooth Packet

3.5.1 BT Transmit tests

The key functional tests of the transmitter (TX) chain are:

1. Transmit power measurement: In this test, the BT device is transmitting a modulated Gaussian Frequency Shift Keying (GFSK) or Enhanced Data Rate (EDR)

signal which is captured, down- converted, and measured by the tester. To be able to do this, the tester must have the ability to receive an RF signal and process it. The Class 1.5 specification for the Orca device is typically 12.5 dBm of average power using GFSK modulation and 10 dBm using EDR modulation with an internal Low Drop Out (LDO) regulator at room temperature.

2. Transmit output spectrum tests: This set of tests checks if the device complies with in-band and out-of-band spurious emissions standards. The output spectrum of the device is checked against a mask based on specifications. The adjacent channel power is the sum of measured power in a 1 MHz bandwidth channel. The transmitter transmits in channel number M, and the adjacent channel power is measured in channel number N. The device transmits a pseudo random data pattern during the test. Tables 3.1[15] and 3.2 [15] show the Bluetooth specifications.

in-Danu Spurious Emissions Mask Specification		
Frequency Offset	Transmit Power	
<i>M</i> ± 500 kHz	-20 dBc	
M - N = 2	-20 dBm	
<i>M</i> - <i>N</i> >3	-40 dBm	

Table 3.1: In-band Spurious Emissions Mask Specifications

le 3.2: Out-of-Band Spurious Emissions Mask Specifications		
Frequency Band	Operating (dBm)	Idle (dBm)
30 MHz to 1 GHz	-36	-57
1 to 12.75 GHz	-30	-47
1.8 to 1.9 GHz	-47	-47
5.15 to 5.3 GHz	-47	-47

3 2. Out-of-Band Spurio **.** . . Tabl

In order to create a spectral mask close to the ideal spectral mask, the test time would be substantial (in the order of minutes) to create a smooth curve using FFT. Since test time is at a premium and directly affects test cost, less averaging is used which leads to measurement errors and results in either false yield loss or in defective units being shipped if the device is marginal in this parameter.

3. Tests that check modulation characteristics: The tests that check the modulation characteristics are essentially testing the stability of the LO and the modulator. A drifting LO or a dysfunctional modulator can cause frequency deviation beyond the 175 kHz specification. This test requires the tester to have vector signal analyzer capabilities since both phase and symbol information are needed.

4. Initial Carrier Frequency Tolerance (ICFT) and Drift: This test measures the finite difference between the programmed channel frequency (desired) and initial frequency of the VCO. The ICFT result must be less than 75 kHz, by measuring the first preamble bits.

3.5.2 BT Receiver tests

BT Receiver (RX) tests are designed to check how well a device can receive the signal transmitted by a nearby transmitter in the presence of other unwanted signals from other transmitters. The receiver should also be able to reject in-band and out-of-band signals. The Bit Error Rate (BER) percentage is defined as:

$$BER \% = \frac{Number_of_bad_bits}{Number_of_transmitted_bits} \times 100$$
 Equation 3.5

The test equipment should be able to modulate the RF signal and control the levels of both the desired signal and the interfering signal. The device receives these signals and processes them, after which the tester compares the output digital bits with the original digital bits. Synchronizing the bits transmitted by the tester and the bits received from the device is a very important aspect of this test. The device BER is measured under each of the following conditions: **1. Carrier-to-interference (C/I) BER:** During the C/I test, the device receives two signals: the modulated desired signal at a certain power level and the modulated interferer at a different power level.

2. Sensitivity BER: The sensitivity test is used to measure the power level at which the devices cannot sense the incoming signal well enough in the absence of any interfering signals. The sensitivity requirement for the Orca device is a BER better than 0.01% at an input signal level at or below -83 dBm.

3. Blocking BER: This test checks the ability of the device to detect the desired signal in the presence of in-band and out-of-band blocking signals.

4. Intermodulation BER: In a non-linear device, intermodulation products are created when two tones interact. If these products are strong and fall in the region of the desired signal, they can inhibit the ability of the device to detect the desired signal. This test measures the BER with two unwanted signals in addition to the desired signal.

5. Maximum input level BER: This test is similar to the sensitivity test, except that it measures the ability of the device to operate when supplied with a high input level signal. BER is measured when an input signal at 20 dBm is being received by the device. The BER test is very sensitive to noise in the test environment and also to interference from signals being applied to nearby devices. So in a multisite test solution where several units are tested in parallel it is possible that not all devices can be tested for BER simultaneously. This can double or triple the effective test time.

3.6 Typical FM RFC Production Tests

Conventional tests of FM devices include measurement of the signal's level, frequency and phase. Signal-to-noise ratio (SNR) is the ratio of level measurements made

under various conditions expressed in dB. "Distortion" is a term used to quantify the amount of unwanted components in a signal. Total Harmonic Distortion (THD) is a frequently used method, in which the harmonic content of the audio output is measured at various audio and modulation levels.

3.6.1 FM tests

The key functional tests of the FM core are:

1. Sensitivity: The sensitivity is the RF input level required for 26 dB signal-to-noise ratio at the device's audio output ports.

2. Maximum SNR: This is the SNR measured with an input RF signal level of -47 dBm with an applied 1 kHz FM modulation. This test is described in detail here as it is necessary to understand how this is done so that the BiST that is used to replace it will be clear. The tester supplies a -47 dBm, 1.0078125 kHz FM modulated tone of 1 mV amplitude at the frequency of operation, fc. The offset in the input tone is chosen so that after FFT, the signal lies on one FFT bin without any spectral leakage. The FM synthesizer or Local oscillator (LO) is tuned to the desired fc to down-convert the incoming RF signal. The signal is then digitized and demodulated by the FM device. The demodulated signal is collected at the device audio output pins using the tester's waveform digitizer. A 20 kHz anti-aliasing filter is applied and some samples are discarded to stabilize the capture. Then, 8,192 samples at a rate of 192 kHz with a resolution bandwidth of 192 kHz/8, 192 = 23.4375 Hz are collected. FFT is performed on these 8,192 samples. The FFT bins from 13 to 640, which correspond to the 500 Hz to 15 KHz, are used in the calculation. Signal power is calculated from a single bin 43 which corresponds to 1.0078125 kHz. Noise is calculated by adding the noise power in the

remaining bins. The SNR is computed as a ratio of the signal and noise calculated. For stability, the measurements are averaged 3 times.

3. Adjacent Channel selectivity: During this test, the SNR is measured at the device's audio output with interfering signals at +/- 200 kHz and +/- 300 kHz offset from fc.

4. Cellular Blocking tests: This test measures the effect of cellular activity on FM sensitivity of the device.

5. Image Response SNR: This test measures the image rejection with mono and stereo signals.

6. In-band blocking: This test measures the ability of the device to operate in the presence of nearby interfering signals. The interferers are set 35 dB higher than the signal of interest and placed at 100 KHz offsets from +/-400 kHz to +/-1 MHz.

7. Mono and Stereo SNR: This test measures SNR in mono and stereo modes.

8. Audio Output Level: The Left and Right audio signal level outputs are measured with nominal modulation.

9. RF transmitted power: This test measures the maximum transmit output level into a resonated loop antenna with no modulation applied.

During characterization all of these parameters are tested on devices to cover expected variations in Process, Voltage and Temperature. A subset of these parameters is then agreed upon by the design, test and business groups to be the ones that are to be tested in production. This becomes the list for the RFC production tests. For the Orca device, the following parameters were identified: **1. Bluetooth Sensitivity Bit Error Rate (BER):** For an input signal with 8DPSK modulation the BER should be lower than 0.01% for a level lower than -83 dBm. The Bluetooth specification for such a signal is -70 dBm.

2. Bluetooth output power in EDR mode: The minimum output power should be 8 dBm for Class1.5 operation.

3. FM Maximum Signal to Noise Ratio (SNR): In mono mode Maximum SNR should be higher than 57 dB.

4. FM output Power: The transmitted power should be at least $117 \text{ dB}\mu\text{V}$.

TI's homegrown tester is called the VLCT for Very Low Cost Tester. This was the tester used to test Orca in production. It had the following resources:

- 1. 512 digital pins. 256 of these had source/capture capabilities, meaning they had memory associated with them and could be used to implement ATPG vectors.
- 32 high speed clock channels that had a total frequency range between 100 KHz –
 700 MHz. It also had frequency counters and time measurement capability.
- 3. Several high and low current power supplies.
- 4. V/I instruments to support analog test, voice-band mixed-signal test.
- 5. One Rhode and Schwarz SMATE200a Vector Signal Generator.
- 6. Two RF Sources that were divided into 16 RF resources and could be used to transmit and receive signals from the devices being tested. It was possible to transmit to 16 RF ports simultaneously, but it was only possible to receive and capture RF signals from 8 ports at a time.

CHAPTER 4: TEST AS A DIFFERENTIATOR

The increasing complexity of RF SoCs has resulted in an exponential increase in test complexity and integration of devices has drastically complicated the testing environment. RFC tests like Bit Error Rate (BER), Error Vector Magnitude (EVM) and RF power tests are time consuming, require specialized, periodically calibrated instrumentation, and are difficult to perform in a mass production environment. One reason for this is that conventional RF tests are intended to verify functionality and adherence to specification. The following sections detail various aspects of production testing and make the case for BiST.

4.1 The Cost of Test

There are three main aspects to the recurring costs involved in the manufacture and selling of a semiconductor device: cost of the silicon die, cost of packaging, and cost of testing the device. Overall test cost is affected by various factors such as the type of tester used, test time, and the multi-site factor or parallelism of the test solution. Equation 4.1 represents test cost as a function of these factors.

Test Cost (cents)= Test Time * Multisite Factor * Tester Cost (cents/s) Equation 4.1

The cost of the testers can vary, but it could be considered to be a non-recurring capital type cost. The time it takes to test a device in production could very well be the market differentiator for a product, as it is a recurring cost incurred on each and every device. The multi-site factor is an important knob that can be used to reduce test cost by reducing the number of testers necessary. However, the ability of a solution to port to a high multi-site solution may be limited by the type of tests performed. The higher the multi-site factor, the more devices can be tested in a single insertion. Multi-site testing brings down the test cost by a factor equivalent to the number of sites tested simultaneously. This means that tests requiring specially modulated inputs or tests which provide modulated output data to be captured and analyzed may not be feasible on a high multi-site board because of the lack of sufficient sources or capture ports. When testing WSP devices the board real estate issue is exacerbated even more, because the sockets are not as far apart as the sockets for singulated devices.

Finally, the cost of the tester itself is dictated by the types of measurements that required. For example, a VLCT that has RF measurement capabilities costs \$15/hour more than one without.

4.2 Test Cost Budget

The budget for test is the dollar amount that can be spent on testing the device while still maintaining a healthy profit margin. The budget for the device used in this research was 2.5% per dollar of the AUP. Test cost, as stated above, is a function of the type of tester used, the multisite factor, and the amount of time the device spends on the tester. So hypothetically, suppose the AUP is \$1, then the test cost budget is 2.5 cents. Suppose the charge for using the tester is \$100 per hour then the test time budget would be 0.9 seconds per device. The test time budget is defined as:

Test time budget (seconds) =
$$\frac{\text{Test Cost Budget (cents)}}{\text{Tester Cost (cents/second)}}$$
 Equation 4.2

Equation 4.2 represents the budget on a single-site solution i.e. for testing one device at a time. A multi-site solution where multiple devices can be tested simultaneously would reduce the cost of testing a single device so the test time budget could increase, but it will

not increase by the factor of the multi-site because there would be some overheads. For TI's RFCMOS devices, the multi-site factor usually is a multiple of 2 and it is very common to see multi-site factors of 4, 8 and 16.

4.3 Yield Targets

In order to maintain viable profit margins on these relatively low priced devices, the yield targets are extremely aggressive. As mentioned earlier, TI's WSP devices are tested only once after fabrication. The yield target for such devices is the defect limited yield, assuming no yield loss due to parametric issues or test-related issues. The formula used to calculate this defect limited yield is dependent on the process technology and the particular fabrication facility. For Orca it is described by Equation 4.3.

Defect Limit Yield =
$$\frac{0.95 \times 100}{(\text{Die Size} \times \text{DD} + 1)^{15}}$$
 Equation 4.3

Additional costs will be incurred for any overkill due to device parametric noncompliance issues or test issues.

4.4 DPPM targets

DPPM is defined as the number of parts returned from the customer because those devices do not pass testing in their production line or fail to perform on the field. The DPPM target is based on the business; an automotive part may have a DPPM target of 0, while a commodity part in a non-critical application could tolerate higher DPPMs. The DPPM target for the Orca is 200.

4.5 The case for BiST

A company must be able to increase its manufacturing capacity in response to customer demand, if and when the demand increases, without a large investment in capital and within a reasonable amount of time. Since test time and the equipment used have a great impact on capacity, it is useful to have tests that are designed into the chip and are relatively short. Hence, there is a great drive to replace external testing with tests that the device performs internally. The device computes results and the test program just reports pass/fail results in the datalog like any go/no-go test. These internal tests are called BiSTs and have been used extensively in digital designs since the 1980s. Tests that are done internally could be faster due to reduction in time lost in communication between the device and the tester. BiSTs require little or no external stimulus as the device performs the test and produces test results, which are then logged out, thus eliminating the need for expensive tester resources.

In order to implement RF BiSTs, the faults that cause real failures in RF devices must be understood and tests that detect those faults must be designed. In this work two fault models [16] associated with RF circuitry were identified, which will be described in detail in Chapter 6. BiSTs that covered these fault models were designed and implemented in the production program.

CHAPTER 5: THE HISTORY AND STATUS OF BIST IN DIGITAL CIRCUITRY

Testing is a broad concept that can be applied to any system and it involves applying a known stimulus to a device/system in a known state and evaluating a predictable response from the device/system. This requires that the device being tested is controllable with the ability to apply a known stimulus and the device is observable so that the predicted response can be collected and evaluated. Design For Test (DFT) in digital designs was developed in the late eighties and early nineties. In this chapter, the development of DFT techniques for digital circuits, digital fault models, digital test vector generation will be discussed. It will also be shown how concepts analogous to these can be used in the analog world.

5.1 Faults, failures and fault coverage metrics in digital circuits

When a failure occurs in the Device under Test (DUT), it could be due to a defect manifested as a fault [17]. A defect is caused by physical problems in the silicon. The following defects are commonly observed in CMOS devices:

- Shorts in the gate oxide
- Opens and shorts in metal traces
- Open or plugged vias
- Shorts to the ground and power planes
- Process errors or photo mask errors.

A fault on the other hand is the failure mode manifestation of a defect. The fault is a model of the failure mode caused by the defect and it relates the defect to the behavior of the circuit. A short in the gate oxide for instance could lead to shorting of the Source (S)

and Drain (D) of the transistor as shown in Figure 5.1 and can be represented by keeping the output of the transistor at a fixed logic value (logic 1 or 0). These faults may manifest as high current, high impedance or some intermittent state. This is the transistor level representation of the fault and it can also be translated into the gate level. For example the S to D short in Figure 5.1 could result in the output always being "stuck at 1".



Figure 5.1: S to D short causing D to always be at logic 1

The stuck-at fault is a common model used at the gate level, and opens and shorts in circuit interconnections can be identified with the stuck-at model to allow tests to be generated to isolate these faults.

Stuck-on or stuck open conditions of CMOS transistors, resistive bridging faults and partially conducting transistors can be identified with the pseudo stuck-at model. The IDDQ tests are used to catch these faults.

Another commonly used fault model is the "delay fault" which can be due to an open metal connection through which current tunneling occurs, leading to a delay in propagation. Partially conducting transistors and resistive bridges exhibit path delay or transition faults. These are caught by at-speed tests.

A third type of fault in digital circuits is called current fault and it is indicated by high leakage currents. The leakage current measurements can be made after running a stuck-at test or after "toggling" as many nets, nodes and gates as possible.

A circuit may have several defects, but a defect may not necessarily translate into a failure. For a failure to occur, the conditions of observability and controllability as mentioned earlier must exist. Criteria for the failure measurement must also be present. If the circuit is redundant so that the fault cannot be observed, controlled or the fault does not affect the output, then even though the fault exists the failure may not. These defects could be a reliability concern which must be eliminated during burn-in, but they would not cause failure.

Digital test vectors exercise and detect a certain number of faults in the design. Equation 5.1 defines the metric for fault coverage.

Fault coverage =
$$\frac{\text{Total detected faults}}{\text{Fault population}}$$
 Equation 5.1

5.2 Types of Tests

1. Functional Tests: A functional test verifies that a circuit behaves as it was intended to; it verifies whether the design is correct. For example, if a circuit is designed so that it functions as an adder, then all possible addition operations are checked and they are expected to yield the correct answer. This should be done during RTL or gate level simulation. Functionality may also need to be verified under certain timing and power consumption constraints. In most modern digital designs, functionality is not tested

during production test. If there is a gap in test coverage through structural tests that results in customer returns which cannot be filled by appropriate structural test, then a functional test may be added into the test program. But these tests can be test time intensive, and hence undesirable.

2. Structural Tests: Structural tests are used to verify if the circuit structure is intact after the manufacturing process. This can be done by applying the static stuck-at model and assuming that a defect will cause a gate or a net to always be stuck at 0 or stuck at 1. Vectors that require nodes to toggle are applied and the results are compared to expected results to detect failure. This type of testing is measured by the fault coverage metric in Equation 5.1. Similarly, the delay fault model and the current fault model can be applied to assess timing and power consumption, respectively.

5.3 Automatic Test pattern Generation (ATPG)

ATPG is the process of applying algorithm-based software to the design to create test vectors. The ATPG tool can be applied to a design after certain preparation such as creating a library of standard cells, ensuring the design description is in the right data format for the ATPG tool, and establishing test goals and constraints. The actual ATPG process involves the following main steps:

1. Establishing the fault model: All the faults that are to be tested must be listed and the first fault to be tested is picked for the ATPG tool to generate vectors.

2. A propagation path for the fault to an observe point is established: The logic that contains the fault is analyzed so that a path for the fault can be traced to a point where the fault can be observed.

3. A controllability point is established: A path is traced through the netlist from the fault location back to a point where it can be controlled in order to establish the logic values needed to excite the fault.

The order and nature of this analysis depends on the algorithms used by the ATPG tool. The vector data is then translated into the correct data format called TDL for Test Descriptive Language. This vector is then simulated and verified. The simulation is a fault simulation that verifies if the fault under consideration is detected, detects other faults that are caught by the vector, and also identifies any illegal conditions like placing different logic values on a single net. The vector is then saved and any additional faults which are detected are dropped from the list of faults, with this process then repeated with all the faults.

Observability and controllability are two very important attributes of a circuit that make it testable. Controllability is the ability to set a node in the design to a certain value, while observability is the ability to observe the value of a node. Scan insertion is the process of making a design observable and controllable by adding extra circuitry like multiplexers, clocks, etc. This does require additional resources such as clocks, die area, and sometimes adds delays in the functional path, but the "pros" far outweigh the "cons" due to the added test coverage. Figure 5.2 (A) is an example of a circuit whose input and output are not observable and controllable; it is transformed into a testable circuit by adding the multiplexer and control lines (P1, Test Mode Select and P0) as shown in Figure 5.2 (B). On average the increase in chip area due to addition of circuits to support ATPG is between 2% to 10%.



Figure 5.2: (A) Uncontrollable and unobservable circuitry (B) Testable Circuitry

The main goal is to improve the controllability and observability in a design, which reflect the two phases of test generation, namely, test sensitizing and test propagation.

5.4 Scan-based Testing

The complexity of VLSI chips is increasing in terms of gate counts, pin counts, integration and functionality. A common metric used to quantify this complexity is the gate-to-pin ratio, which for today's complex devices can be in the thousands. So, large sections of the device are inaccessible, and hence, not easily testable with a reasonable number of functional sequential patterns. A word must be said here about sequential and

combinational circuits. In combinational circuits, the output depends only on the current values of the inputs and not on the past values. A combinational circuit requires a test vector that will produce the wrong output if there is a fault in the circuit. In sequential circuits, the output depends not only on the current values of the inputs, but also on their past values. Sequential circuits have memory elements and feedback and one must apply the right inputs and set all the flip-flops in the correct states before performing the test. This exponentially increases the level of test complexity, and hence, scan-based design attempts to make sequential circuits behave like a combinational circuit, which is easier to test. To achieve this goal, sequential elements are replaced with scannable sequential elements. The best way to do this is to provide test access points within the circuits, most commonly using scan techniques. Scan is a structured methodology because it can be standardized, is repeatable and can be automated. The scan architecture employs shift registers which are placed within the chip and allows control as well as observation of the chip. Multiple scan chains allow optimization of vector depth and the scan architecture enables algorithmic tools to verify the design as well as generation of test vectors.

A scan cell is the fundamental, independently-accessible unit of scan circuitry, serving both as a control and observation point for ATPG and fault simulation. A scan cell contains at least one memory element (flip-flop or latch) that lies in the scan chain path. As shown in Figure 5.3, it can be considered as a black box composed of an input, an output and a procedure specifying how data gets from the input to the output. The most commonly used scan cell is the Multiplexed D Flip-Flop which simply involves adding a multiplexer before every flip-flop to select between scan and functional data.

There are other scan cell types like the Clocked Scan Cell and the Level Sensitive Scan Design (LSSD) system [18].



Figure 5.3: Basic Scan Cell

Figure 5.4 shows an example of inserting scan circuitry to a D flip flop. The multiplexer allows control enabling either scan data or functional data to be shifted in. When the scan enable (scan_en) clock is high, scan data is shifted in and captured. Scan testing is accomplished by changing the mode that a scan cell operates in. There are several scan architecture types like full scan, partial scan and partition scan. In full scan, all memory elements in the design are replaced with their scannable equivalents. These are then "stitched" together into scan chains. While the full scan design technique makes all storage elements scannable, it may not be acceptable for all designs because of area and timing constraints. In a design with partial only a certain percentage of the flip-flops in the design are replaced by equivalent scannable elements. The ATPG process on very large, complex designs can often be unpredictable. Large designs, which are split into a number of design blocks, benefit most from partition scan, where the design is partitioned into blocks which are scanned individually.



Figure 5.4: D flip-flop before and after adding scan circuitry

DFT techniques are also applied to other design blocks like memory and the input/output circuit structures. The BiST techniques applied to the RF/Analog blocks are similar to the structural tests applied to digital logic blocks.

5.5 Digital Design Flow with DFT

Figure 5.5 shows the high level design flow for a digital IC.



Figure 5.5: Digital Design Flow

Once the gate level netlist is generated, the scan chains are inserted followed by test pattern generation. If the patterns do not meet the fault coverage target, the RTL is modified to add more coverage. Scan vectors are generated and verified and TDLs are handed off to the Test Engineers for implementation in the test programs.

5.6 Drawing Parallels from Digital DFT

In the previous sections the basic fault models used in digital circuits, the types of tests used to detect these faults and the automated methods used to generate the vectors for these tests were described. Circuit complexity, ULSI designs, and the need to meet quality through adequate test coverage drove the development of these test methods. In the RF and Analog world, designs are geared towards functionality and meeting specification similar to those in the digital world. However, customers and System, Design and Test Engineers until very recently saw production testing of RF and Analog devices as being very much like characterization or design validation, where several (or as many as possible) device specifications were tested.

In this dissertation a structural approach to test RF and analog circuits was proposed and implemented. Fault models for RF circuits were proposed and tests were developed to detect defects identified by those fault models. Chapters 6, 7 and 8 discuss the fault models, BiSTs, and methodology of BiST implementation respectively.

CHAPTER 6: THE MAJOR FAULT MODELS IN RF CIRCUITS

6.1 Introduction

In this dissertation it is shown that a defect based test strategy could be extended to the RF sections of modern communication SoCs. Knowledge of the actual defects that occur in these devices allowed reduction of the test list, and hence test time, to a few simple BiSTs that make extremely high volume production possible. For the first time, these defects were categorized and the tests are described. In addition, a novel method of verifying the defect models is described.

6.2 Fault Models

In order to create and apply DFT techniques to the RF blocks of the design, the following fault models were first proposed based on which tests were developed.

6.2.1 Trauma in the Signal Path

Trauma defects or failures are caused due to a discontinuity or trauma in the signal path or circuit component. A manufacturing defect in any particular block or in the signal path can cause that block or that path to be dysfunctional. This type of defect may be caused by irregularities in wafer processing leading to missing or shorted metal lines, missing circuit elements due to lithography defects, undesirable capacitance changes due to insulator thinning or thickening in MOS and MIM capacitors, etc. These defects are very similar to open or short type defects modeled by the stuck-at fault in digital circuits. Test coverage for such defects is provided by "scanning or toggling" the elements of the circuit/block and measuring in some way the effect or contribution of that element. An example of trauma is a missing element in an amplifier gain chain that attenuates the

gain. Trauma also includes missing components of a major block. As a second example, consider the Digitally Controlled Oscillator (DCO) which is the unstable element used for frequency synthesis in the Orca device. The DCO has several capacitor banks.

In the Orca BT core, there are 3 banks of digitally controllable weighted binary capacitance devices [19] and the structure of the banks is as shown in Figure 6.1. The structural test for the DCO then would involve toggling each capacitor in these banks between its high capacitance mode and its low capacitance mode and measuring the frequency contribution due to each one.



Figure 6.1: Capacitor Bank

If during the manufacturing process, damage is done to any of the digital signal lines that control the capacitors or any defect is introduced that causes the capacitor itself to malfunction, the structural test will be able to detect it in the form of a wrong frequency measurement when the capacitor is exercised.

6.2.2 Loss of critical performance

Critical performance parameters can be measured internally to check if the circuit is "healthy". One such parameter which is fundamental to all oscillators is the phase noise. In case of an ideal oscillator, all its power is concentrated at its frequency of operation, *f*. In a practical oscillator, however, the spectrum will spread into frequencies around f. This spreading is called phase noise. Phase noise affects the transmitter by causing interference in adjacent bands; in a receiver the presence of phase noise can make it less sensitive. Phase noise in a device can originate from four sources:

1. Thermal noise: This noise is found in lossy elements and is also caused by physical processes in semiconductor devices. Thermal noise can be characterized by Equation 6.1.

$$P_{th} = KT\Delta f$$
 Equation 6.1

where, *K* is Boltzmann's constant; *T* is the absolute temperature in Kelvin and Δf is the bandwidth.

2. ADC quantization noise: An ADC converts the input signal from analog to digital and this is inherently a non-linear process. There is always a difference between the true value of the analog signal being converted and the quantized signal. The probability of this error is uniformly distributed across the quantization level Q. So, the probability density function of the amplitude is 1/Q and the noise power can be calculated as shown in Equation 6.2.

$$P_{Q} = \frac{1}{Q} \int_{-\frac{Q}{2}}^{\frac{Q}{2}} X^{2} dx$$
 Equation 6.2

3. DCO Phase Noise: Phase noise in the DCO can lead to reduced channel selectivity and increased BER in the receiver. For an ideal oscillator operating at ω_0 , the spectrum is in the shape of an impulse, whereas for an actual oscillator, the spectrum spreads around the center frequency. The phase noise of an oscillator depends on several of variables that can range from its atomic structure to the environment. Consider a unit bandwidth at an offset $\Delta \omega$ with respect to ω_0 . Phase Noise is derived by calculating the noise power in this bandwidth, and dividing the result by the carrier power. The presence of phase noise can cause "reciprocal mixing" in the receiver which can affect BER [20]. Figure 6.2 is a basic diagram of the ADPLL based transmitter [21] and is shown here to illustrate the complex control and feedback mechanisms employed for frequency tuning and modulation in the modern RF transmitter.



Figure 6.2: The ADPPL based transmitter

4. Power Supply Noise: Noise from power sources can be a significant contributor of phase noise in the DCO. Linear voltage regulators are used for filtering the DCO's supply voltage. In addition, precautions like providing a dedicated regulator and ground plane for the DCO are also taken.

Traditionally phase noise is measured by capturing, down-converting and digitizing the transmitted signal, and then, digitally filtering the data to calculate the phase noise [22]. This test is time-consuming and requires specialized instrumentation.

The ADPLL, however, is able to make an equivalent measurement internally. This test does not check for structural defects, but it does check for the overall health of the DCO by monitoring the phase noise, and thus, is equivalent to leakage current tests that are modeled by the current fault model in digital logic circuits.

The location of filter poles in case of the filters in the receive chain is another example of a health check.

6.3 BiST creation from a block diagram

Figure 6.3 is a generic block diagram of a RF transceiver. It consists of the basic blocks shown and test coverage for each block is defined as follows.



Figure 6.3: Block Diagram of a generic RF transceiver

6.3.1 LNA and TA

The gain stages of these blocks are switched on one by one and the gain contribution is measured. Absolute measurements of gain are not necessary to check for structural defects so gain deltas are measured and compared against limits.

6.3.2 Mixer

The mixer block is tested by default because if the mixer is not functional no subsequent block would show the right result.

6.3.3 RX Filter

The filter poles are tested to make sure that it is performing the low pass function.

6.3.4 Feedback DAC

The various settings of the DAC are measured using the ADC.

6.3.5 Local Oscillator (LO)

The LO consists of capacitor banks. Each capacitor is toggled to check for the right frequency deviation and the total frequency range is also measured. Phase noise (in terms of the equivalent phase error) of the LO is another important criterion that is checked.

6.3.6 Pre Power Amplifier (PPA) and Power Amplifier (PA)

The various stages of amplifiers are switched on and the difference between stages is measured.

6.3.7 Other blocks or circuits

1. Input/output (I/O) structures: For example, the test solution may not have the resources to contact a certain RF pin and make a continuity measurement. In such a case, even if the internal circuitry is fully tested, there may be test coverage gaps if the I/O is not tested. BiSTs must be implemented to cover I/Os in such a case.

2. LDOs and critical currents: All the LDOs must be tested to verify that they are defect-free and capable of supplying the right voltage levels to the various circuit blocks. Current consumption of the RF blocks are also measured when the device is in certain functional states like RX or TX.

3. Un-scanned digital blocks: Sometimes certain digital blocks are not scannable because they are high-speed and the ATPG timing cannot be closed at that speed. In such a case BiSTs that check the functionality of such blocks have to be created.

6.4 Method of extracting defect models from production material

In order to find the actual defects that occur in production devices, all RFC fails were shipped back and retested on a known-good test setup to verify the fail and understand the fail mechanism.

CHAPTER 7: ENABLING BISTS FOR RF CIRCUITS

In Chapter 1 the term BiST, which implies that the tests are done mostly internal to the device with little or no stimulus from the tester, was discussed. This could make the test cheaper because a tester that is not too fancy and hence inexpensive can be used. Also BiSTs can be faster than conventional tests. The only way to meet the test cost budget described in Chapter 4 for today's low cost devices is by replacing expensive RFC tests with faster internal tests. Digital DFT tools already produce tests for the digital portions of the chips in an automated fashion.

Most digital tests can be classified as "structural" because they check for the structural integrity of the transistor or circuit component under test. In this dissertation, structural tests are proposed to test RF sections of the chip in a simple manner to verify that a particular component is present and that it can meet certain performance criteria. Instead of full-chain tests that verify complex functionality like BER performance or SNR performance, defect-based production tests can be applied to a chip that is well-designed so that all the functionality is ensured with a good margin. As such, production testing should not be used to check for performance incompliance or process variation. A robust design and good digital compensation techniques should be able to produce a chip that performs well functionally as long as it is checked for defects. This brings us to the very important topic of margin.

7.1 The Margin Question: how much margin is enough?

Parameters that have a normal Gaussian distribution can be measured using a capability index. A capable process or parameter is one where almost all the measurements are within specification limits. This can be represented by the plot in Figure 7.1.



Figure 7.1: Process Capability

Several statistical functions such as Cp and Cpk, can be used to measure "capability" and they assume a normal distribution. Assume that the data is normal and that μ and σ are the mean and standard deviation, while USL and LSL are the upper and lower specification limits. The population capability indices are defined as follows by Equations 7.1 and 7.2.

$$Cp = \frac{USL - LSL}{6\sigma}$$
 Equation 7.1

$$Cpk = \min\left[\frac{USL - \mu}{3\sigma}, \frac{\mu - LSL}{3\sigma}\right]$$
 Equation 7.2

The *Cpk* of a process measures how centered the parameter is between its lower and upper specification limits and also measures its stability. Figure 7.2 shows how the *Cpk* statistic can vary for different σ . If the parameter follows a normal distribution, then the fraction of the defective parts may be determined by using Z-tables [23]. At *Cpk* = 1.33, the defect rate drops to 66 Parts Per Million (PPM). To attain less than a 0.5 PPM defect rate, a *Cpk* level of 1.67 is required. The probability of a defective part existing at a *Cpk* level of 2.0 is about 2 Parts Per Billion (PPB). In this dissertation margin is defined as the property that causes a parameter to have a *Cpk* value that predicts an acceptable DPPM level.



Figure 7.2: Varying standard deviation and *Cpk*

This is all well and good if the measurement is ideal. In reality, the distribution of a test parameter includes the variations/errors in the measurement. Let us consider an RF parameter with a Probability Density Function (PDF) described by $f_x(x)$, where each measurement is that of a unique device and the distribution of its measurement described by $f_y(y|x)$ as shown in Figure 7.3.



Figure 7.3: Statistical distributions for RF test and measurement error.

If it is assumed that this is a Noise Figure measured in dB, then the upper limit is more important. There are 2 main criteria used to judge the goodness of a device: the Upper Specification Limit (USL), which could be the number specified on the datasheet as being the highest possible value that a customer will measure on a shipped device and the Upper Test Limit (UTL) which maybe slightly lower (say 0.5 dB lower) than the USL, to

accommodate test variations. Depending on whether or not there is sufficient margin and depending on the accuracy of the measurement, several scenarios are possible:

1. Ideal Measurement: A certain number of devices will fail if the distribution is wide and there is no margin to specification. The number of devices that are expected to fail assuming that the measurement is perfect would be given by Equation 7.3.

$$P[X \ge USL] \times (\text{Population of devices}) = \int_{UL}^{\infty} f_X(x) dx \times (\text{Population of devices})$$
 Equation 7.3

Non-ideal measurement: However, no physical measurement is perfect and when considering a measurement with a certain standard deviation σ , a certain number of units above the UTL will be identified as failing units. The probability that a unit is identified as a bad unit due to measurement error is given by Equation 7.4.

$$P[B] = \int_{-\infty}^{\infty} \left[\int_{UTL}^{\infty} f_Y(y \mid x) dy \right] f_X(x) dx$$

$$= \int_{-\infty}^{\infty} \left[1 - \int_{-\infty}^{UTL} f_Y(y \mid x) dy \right] f_X(x) dx$$

$$= 1 - \int_{-\infty}^{\infty} F_Y(UTL \mid x) f_X(x) dx$$

Equation 7.4

These units will not be shipped to the customer and constitute the yield loss. The actual yield loss is given by Equation 7.5.

Yield Loss = (Population of devices)
$$\times P[B]$$
 Equation 7.5

3. False Failures: Since the USL and UTL are different and there is a certain measurement σ , there will be a population of devices that are actually good to the USL, but are identified as bad devices. These are the overkill units. The probability that a device is an overkill unit is given by Equation 7.6.

Equation 7.6

$$P[C] = \int_{-\infty}^{USL} \left[\int_{UTL}^{\infty} f_Y(y \mid x) dy \right] f_X(x) dx$$

=
$$\int_{-\infty}^{USL} \left[1 - \int_{-\infty}^{UTL} f_Y(y \mid x) dy \right] f_X(x) dx$$

=
$$F_X(USL) - \int_{-\infty}^{UTL} F_Y(UL \mid x) f_X(x) dx$$

The total number of units that are overkilled is given by Equation 7.7

$$Overkill = (Population of devices) \times P[C]$$
Equation 7.7

4. Defective units shipped: Lastly, and most importantly, if the distribution of the device for a certain parameter is too wide and/or the test σ is high, devices that measure higher than the USL may be shipped to the customer. When detected at the customer end they will be returned and counted as DPPM. The probability that a device is a DPPM is given by Equation 7.8 and the total number of devices that could be counted as DPPM is given by Equation 7.9.

$$P[D] = \int_{USL}^{\infty} \left[\int_{-\infty}^{UTL} f_{Y}(y \mid x) dy \right] f_{X}(x) dx$$
Equation 7.8
$$= \int_{USL}^{\infty} F_{Y}(UTL \mid x) f_{X}(x) dx$$

 $DPPM = (Population of devices) \times P[D]$ Equation 7.9

By using the equations described above, we can see how the DPPM, yield loss, and overkill are affected by a particular parameter's distribution, the test distribution, and limits. This information can be used first to convey to the designers what the standard deviation should be for a particular specification parameter so that yield and DPPM targets are met. It is also used to align the limits of the BiSTs to be able to detect all the
units which are identified as fails by the conventional test. This can drive improvement of the BiSTs' standard deviation if necessary.

In the characterization phase, RFC tests that show good margin are identified as candidate tests for replacement with BiSTs. For the Orca devices, the following RF tests were shown to have good margin during characterization and they were included in Phase 1 of the production test program, described in section 8.3, for full test coverage of the RF blocks:

- 1. FM Transmit power
- 2. BT Transmit Power
- 3. BT Sensitivity Bit Error Rate (BER)

The FM Maximum SNR test was also a candidate for replacement, however it did not show good margin in production, and hence, it was treated differently. All these analyses are detailed in Chapter 10.

7.2 Factors that enable BiST

1. CMOS-based radio-design: The integration of digital and RF/analog circuits on a single SoC meant that RF/analog circuit components would have to function in deep-submicron CMOS (90nm and lower geometries) just as well as they would in analog processes like SiGe and GaAs with larger geometries. Advances in CMOS process technologies like high resistivity substrate, thick metals and additional devices such as high quality MIM capacitors, varactors etc. enabled this integration of digital logic and RF/analog circuits. These advances have also enabled the scaling of geometries, making CMOS attractive for use in the manufacture of SoCs with complex digital logic and RF/Analog capabilities on the same piece of silicon [24]. CMOS processes are sturdy and

available from independent foundries like TSMC, SMIC, UMCi etc. with extremely high yields and low defect densities. CMOS-based radio design has made RF BiST possible because it requires the digital logic, digital processor, and memory available on these SoCs.

2. DRPTM **technology:** Digital Radio Processor (DRPTM) technology is used to design RF circuits in deep-submicron CMOS processes by utilizing the superior "time-domain resolution of digital signal edge transition" instead of the "voltage resolution" of analog signals which have reduced headroom due to lower supply voltages. This led to RFCMOS SoC designs with the superior RF performance required of contemporary devices which implement complex digital modulation techniques while meeting the goals of low phase noise, high switching speed, fewer spurs, low cost, smaller size, low power consumption, and wide tuning range [25]. DRPTM technology also brings with it unprecedented access to device registers that control all circuit components as is the case with Bluetooth/FM device by Texas Instruments used in this dissertation research.

3. Computational capabilities of a processor on chip: The devices under consideration have integrated Digital Baseband (DBB), Application Processors (AP), RF, memory, and power management circuitry all on a single die. The architectures of these SoCs allow for a change in test methodology with the use of BiSTs. They possess one or more APs, such as an ARM processor which allows complex math to be used to compute the results of internal tests. Internal memory (RAM) can be used while performing calculations and to store results. Complete transceivers are integrated together so that loopback can be leveraged to use the receiver to test the transmitter and vice versa.

4. Firmware-based radio design: Above all, these radios are tending towards being software defined and so there is a pre-existing software infrastructure that can be used effectively in production testing. The BiSTs proposed are firmware-intensive with very little extra hardware required. This is valuable when test cost is calculated because any extra hardware would translate to a recurring cost on every die shipped. Additionally, if the tests need to be changed or re-written, firmware can be modified after the design is frozen and masks are generated without any additional penalties. If a coverage gap is discovered after a device is released to production, new tests can be added to close that gap because it would only require a firmware change.

Hence, BiSTs have the potential to replace traditional production test methods by utilizing on-chip resources to structurally test the integrity of the device.

7.3 BiSTs for individual RF/Analog design blocks in the BT core

In this section the BiSTs implemented in the BT core of Orca are discussed to illustrate the methods and the thought process used to design them. Similar tests were implemented in the FM core as shown in the list for FM BiSTs at the end of this section for reference.

As shown in Figure 2.2, the BT core consists of the following RF blocks: PPA, LNA, TAs, DCO, Mixers, IFAs, FBDACs and ADCs. In order to provide structural coverage of all these blocks, tests were designed to check the circuit structure of each block and the health of some of the blocks by verifying performance. The following sections describe each of these tests in detail.

It should be noted here that the units of the data output from the BiSTs. Since these tests are firmware based with the detection being done by some internal circuitry, the test outputs may not always be quantifiable in real physical units like dB, Volts or Amperes; the output of the DC estimation block and the calculations in the ADPLL used to calculate Phase Error result in quantities without units. Wherever a conversion to a physical unit is possible the equation used for the conversion is shown and when it is not possible to convert the data are presented without any units.

7.3.1 Receiver Gain Test

Test Principle and Method: This test checked if the TAs and IFAs worked properly for all gain steps. The BT core had only one RF port for both transmit and receive function, and since this was a half-duplex system, the device switched between RX and TX functionality. This test was performed in the loopback mode, utilizing on-chip leakage (approximately -60 dBm level) to couple the transmitted signal into the receive path as shown in Figure 7.4. Since this was a VLIF receiver, in order to detect a signal in the loopback mode, the principle of sideband detection was used. An Amplitude Modulated (AM) signal at 1 MHz rate was transmitted through the LO buffer before the PPA. This signal showed up as a sideband in the receiver after down-conversion. The PPA was turned OFF during the test and reception through RX front end relied on leakage from PPA output. This method of using the detected side-band levels for BiST was novel and has not been found in any other literature.

The level of the sideband was detected using a hardware mechanism in the baseband called the Goertzel filter, which was an indicator of the gain contribution of the amplifiers. The various gain levels were switched in and out and their contribution was measured using the Goertzel hardware, which is discussed below.



Figure 7.4: RX Gain test path

The TA block converted the incoming voltage signal into a current signal which the mixer operates on. If the TA bock were not functional, nothing down the receive chain would work and no signal would be detected in the digital blocks of the receiver. Also, the TA did not have stages which could be switched in and out. So, the TA was inherently checked when any block past the TA was utilized to detect a signal, and hence, there was no need for a separate BiST for the TA.

The LNA block had 3 gain stages (the first 2 provided ~5 dB gain while the 3rd one provided between 15 and 20 dB gain) and could have been tested using the loopback BiST, however, during early experiments on silicon, it was found that the transmitted signal from the PPA coupled through the silicon to an LC tank at the output of the LNA. This self-mixing would then drown the effect of the gain contribution of the LNA and a wrong gain delta was detected. So, the only way to test the LNA was with an external Continuous Wave (CW) signal. With the external signal, the LNA gain stages were switched on one by one and the gain contribution was measured using the Goertzel block.

Hardware hooks needed: The BT core had a Low Power Scan (LPS) module which was used in the functional mode for power estimation in 4 adjacent bands. There were 2 reasons to estimate power: one was to control the current consumption in the scan mode when the device was scanning for nearby signals and the other was for Adaptive Frequency Hopping (AFH) which was used to reduce the effect of interference from the environment. The power estimation in the LPS module was done using hardware that implements the Goertzel algorithm. The Goertzel algorithm is more efficient than the FFT to compute an N-point DFT for less than 2*log₂N coefficients [26]. The first order Goertzel filter is given by Equation 7.10 can be drawn as shown in Figure 7.5.

$$y(n) = e^{\frac{2j\prod k}{N}} Y(n-1) + x(n)$$
 Equation 7.10



Figure 7.5: First order Goertzel

where, y(-1)=0 and N defines the center of the bins. The bins would be in the following frequencies: (Fs/N)*k for k= [0, 1 ...N-1], where k selected the bin number hence the frequency to measure. There were four Goertzel power estimators in the LPS module, working in parallel in order to achieve power estimation of 4 separate channels simultaneously.

Figures 7.6 and 7.7 show the output of the Goertzel block for all IFA1 and IFA2 settings for one nominal unit. IFA1 had 8 steps, each with a gain contribution between 336 and 400 while IFA2 had 5 steps, each contributing around 480 and 544 of gain. The output of the Goertzel block could be converted into dB using Equation 7.11.



$$Dutput in \ dB = 20* Log_{10} \frac{DC_estimator_output}{256}$$
 Equation 7.11

Figure 7.6: Output data for all IFA1 settings



Figure 7.7: Output data for all IFA2 settings

7.3.2 Feedback DAC Test

Test Principle and Method: The feedback DAC blocks were designed to compensate any differential DC offsets in the RX path, which could cause the ADCs to compress. This test verified that the feedback DACs were functional and structurally sound by checking if they were performing the DC offset compensation function correctly. The DC voltage level of the IF signal at the input of the ADCs was measured to verify that the level was below a certain maximum value. Also, the test checked if the feedback DACs were working as expected. The test path was as shown in Figure 7.8. The DC level measurement was done in the digital section by a DC estimation block. The outputs of IFA1 and IFA2 could be connected directly to the ADC so that the each DAC could be tested independently. The DAC levels were swept and the DC contribution of each level was measured and compared against limits.



Figure 7.8: Feedback DAC test schematic

Both DACs had 62 possible codes and each DAC1 code is supposed to contribute between 2 to 12 units at the output of the DC Estimation block while each DAC2 step contributes around 50 units. Figures 7.9 and 7.10 show the data for the 2 DACs for one nominal unit. The dotted red lines represent limits.



Figure 7.9: FBDAC1 codes and the output of the DC Estimator block



Figure 7.10: FBDAC2 codes and the output of the DC Estimator block

Hardware hooks needed: The DC estimation block was needed to perform this test. In addition, the switches which connect the IFAs individually to the ADC werre also needed.

7.3.3 Image Rejection Ratio (IMRR) Test

Test Principle and Method: This test was parametric in nature because it did not really check for circuit structure issues. Image frequencies are a serious problem in heterodyne receivers since the filtered product of the wanted signal and an image signal would be superimposed and the image could be much larger than the signal of interest [27]. Hence it was necessary to have the ability to reject image signals. This test measured how good

the Signal to Noise Ratio (SNR) was when an image was present in the RX path. This would emulate the effect of a mismatch in the RX front end. During this test, an external CW signal was sent to the RF input port and the power of the IF signals at +/- 0.5 MHz (wanted and image signals) was measured using the Goertzel hardware. Then, the ratio between the magnitude of the wanted and image signals was calculated and compared to expected limits. The IMRR was expected to be at least 21 dB, which when converted back to the Goertzel block output using Equation 7.11 was 2880. Figure 7.11 shows the data for this test for one wafer with the dotted red lines showing the expected range of values.

Hardware needed: This test also used the Goertzel filter hardware in the LPS module. In addition, it required a CW signal in the BT band around 2.4 GHz.



7.3.4 IF Pole Location Test

Figure 7.11: IMRR test histogram

Test Principle and Method: This test is also parametric in nature and verifies the pole location of the Low Pass IF filters. The principle used here is unique because no external signals or resources are needed to check the poles of the IF filter and it is truly a BiST. A 1 MHz square wave signal is sent to the IF Filter input which creates a tone at the fundamental and another one at the third harmonic as shown in Figure 7.12. This test is parametric in nature because it does not really check for circuit structure issues. The square wave is created by toggling the FBDAC1 control between two values. The AM output consists of at least two tones: a fundamental and a 3rd harmonic. The attenuation in the 3rd harmonic corresponds to the pole location and is required to meet predefined limits.

7.3.4 IF Pole Location Test

Test Principle and Method: This test was also parametric in nature and verified the pole location of the Low Pass IF filters. The principle used here was unique because no external signals or resources were needed to check the poles of the IF filter and it was truly a BiST. A 1 MHz square wave signal was sent to the IF Filter input which created a tone at the fundamental and another one at the third harmonic as shown in Figure 7.12. This test was parametric in nature because it did not really check for circuit structure issues. The square wave was created by toggling the FBDAC1 control between two values. The AM output consisted of at least two tones: a fundamental and a 3rd harmonic. The attenuation in the 3rd harmonic corresponded to the pole location and was required to meet predefined limits.



Figure 7.12: IF pole location test schematic

The ratio of the 3rd harmonic with the fundamental was expected to be between 2 and 7.5 dB and was measured for 8 critical Automatic Gain Control (AGC) steps. Each of these AGC settings placed the IF amplifiers in certain specific settings. The Goertzel block output was again converted to dB using Equation 7.11. Figure 7.13 shows the pole location for every AGC setting. The limits for this test are 332 and 608 and are shown by the dotted red lines.



Figure 7.13: IFA pole location for various AGC settings

Hardware needed: This test also used the Goertzel filter hardware in the LPS module. The digital controls to toggle the FBDAC inputs to create a square wave were also needed.

7.3.5 Drift Test in RX and TX modes

Test Principle and Method: This test was a parametric test which measured the frequency stability of the DCO. During the RX drift test, the device was working in open loop operation and the DCO was not locked, while during the TX drift test the DCO was locked to the lowest in-band frequency. Samples of the instantaneous frequencies were recorded at the output of the ADPLL. Then, the maximum frequency deviation was measured and compared with expected limits. No additional external or internal hardware was needed for this test. The frequency drift was expected to be below 20 kHz in both TX and RX modes.

7.3.6 DCO Capacitor Scan Test

Test Principle and Method: This test was the closest to digital structural tests because it tested each capacitor setting in the DCO. The DCO consisted of 3 capacitor banks:

- 1. The Process Voltage Temperature (PVT) bank
- 2. The Acquisition Bank
- 3. The Tracking bank

The PVT and Acquisition banks were used to set the center frequency of oscillation before the actual transmission or reception begins, while the tracking bank precisely controlled the oscillating frequency during the actual operation, including the modulation while transmitting. The PVT capacitors were divided into PVTH and PVTL banks with 5 binary encoded capacitors each lending 2^5 (32) different capacitance settings each. Each PVTH setting contributed 10 to 40 MHz while each PVTL setting contributed around 4 MHz frequency deviation. The Acquisition bank had 6 binary encoded capacitors, each lending 2^6 (64) different capacitance settings with a frequency contribution of 600 kHz each, while the Tracking Bank had 80 individually controlled capacitors which contributed about 60 kHz of frequency change. Hence, the Tracking Bank had the finest resolution among these three capacitor banks, and was therefore most challenging to test.

This test checked if all capacitors within the DCO worked properly. In order to do that, all individual capacitor settings were scanned when the ADPPL was in open loop mode. Each capacitor was toggled and its frequency contribution was measured. For the PVT and Acquisition Banks, the frequency counter within the ADPLL was used for translating the actual DCO frequency into digital words that were read using the firmware. For the Tracking Bank, since it had finer frequency steps, the digital PHase Error (PHE) signal (to be discussed in the following section) produced by the phase detector in the ADPLL was processed to determine the magnitude of the frequency perturbations created by each tested capacitance. Figure 7.14 shows a sample of the data for the PVTL bank for a nominal unit with the dotted red lines showing the limits for this test.

Hardware needed: There was an on-chip frequency counter for functional reasons. This test used that frequency counter and it required digital control of individual capacitor settings.



Figure 7.14: DCO PVTL bank settings and frequency contributions

7.3.7 PHE test in TX and RX modes

Test Principle and Method: In section 6.2 DCO phase noise was described as being one of the fault models in the Orca device, with the traditional phase noise measurement being complex and expensive. While the PHE test was a BiST, it was parametric in nature and similar to the tests for current faults in digital logic circuits. The phase noise of the DCO had been correlated [28] to the PHE measurement which will be described in this section.

The DCO Tracking bank capacitors were used to perform frequency modulation. The DCO gain was calibrated to achieve low distortion during transmission [29]. The frequency command word (FCW) is used to set the DCO to the desired frequency. As seen in Figure 7.15, the clock edges of the reference frequency and the clock edges from the DCO were compared and turned into a digital representation by the time-to-digitalconverter (TDC).



Figure 7.15: ADPLL based transmitter

The TDC output was then subtracted from the FCW and filtered through IIR filters to get the PHE signal. This signal was sampled by the on-chip processor and a variance calculation was performed in order to calculate RMS phase error as shown in Equation 7.12, where N was the number of samples and xi was the data value for the i-th sample.

$$\sigma^{2} = \frac{1}{N} \sum (xi - \overline{x})^{2}$$
 Equation 7.12

Approximately 8000 samples of PHE vector were sampled and a software-based variance calculation of the digital PHE signal in the ADPLL was performed. Figure 7.16 shows how the dividers in the TX and RX paths are independent, so the PHE test was performed in the TX mode and the RX mode respectively. It was performed in three separate BT channels (0, 39 and 79) in order to get a sampling of noise performance across the BT band and Figure 7.17 shows the TX PHE data in the 3 channels. The TX PHE value in all three channels is expected to be below 49,000.



Figure 7.16: Independent frequency dividers in TX and RX paths.



Figure 7.17: TX PHE data in 3 channels

No extra internal or external hardware was needed to perform this test.

7.3.8 PPA Scan Test

Test Principle and Method: This test verified proper functionality of all PPA's internal transistors. A damaged transistor could affect the EDR modulation in the device badly. The PPA had 73 transistors: 63 Most Significant Bits (MSB), 7 Least Significant Bits (LSB), and 3 Fractional bits. The design allowed each individual MSB transistor to be addressed and ON/OFF toggled. Toggling created AM modulation, of which the 1st sideband was tuned to the IF band of the RX chain. The MSB transistors were activated individually and the rest were activated in groups. Each MSB transistor was expected to produce at least 300 units at the output of the Goertzel block.

This test was performed in loopback mode using the scheme shown in Figure 7.4 for the RX gain test, where the receiver was utilized to measure the effect of the PPA transistors. The AM sideband detection technique described in 7.3.1 was used during this test as well. The data for this test is shown in Figure 7.19 with the dotted red lines representing minimum and maximum expected values.

Hardware needed: The Goertzel block was used for the sideband energy detection.



Figure 7.19: PPA MSB transistor test data

7.3.9 Period Inversion (PERINV) Test

Test Principle and Method: This test was parametric in nature but was a true BiST because no external resources were needed. The ADPLL module was in charge of locking the DCO frequency in place and to do so it obtained an estimate of the oscillator's instantaneous frequency. Having pure digital traits, the analog RF signal was sampled and converted into a digital word from which the phase error was calculated and fed to the correction loop. This conversion accuracy relied on a block called TDC which contained a set of serial inverters. The delay of each inverter was extremely important to

the fractional accuracy of the frequency digital measurement. The PERINV test was performed using an internal HW mechanism which was capable of counting how many inverters were activated or toggled during a single cycle of the RF clock input. From this, a simple calculation could be done to specify the delay of each inverter. In addition, to evaluate proper block functionality, this test could also be used to estimate the process and transistor strength of the design, via the linkage between the magnitude of device current and propagation delay.

7.3.10 DCO Lock test

Test Principle and Method: This BiST checked the frequency range operation of the DCO. This was done by setting lock frequency to 10 MHz below the lower Bluetooth band limit, and 10 MHz above the upper Bluetooth band limit, and reading a lock indication from the ADPLL hardware. The lock indication was to be a reference reading of the instantaneous frequency versus the required one and the average deviation from it was measured. The result for this test was a 1 or 0, depending on whether the device can lock at both specified frequencies.

7.4 BiSTs for individual RF/Analog design blocks in the FM core

A set of similar tests were implemented for the FM core in Orca. Table 7.1 is a list of the BiSTs implemented in the FM core of Orca along with a brief description of each.

FM BiST name	Brief description
TX ctune	Covers all 127 settings on the TX CTUNE capacitor
Tri-Gen Gain sweep	Covers the various gain stages of the Triangular wave generator block
PA gain sweep	Covers the various gain stages of the PA block
Tx Power (108 MHz)	Internally measures TX power at 108MHz
Synthesizer Lock Range	Checks if the synthesizer can lock across the required frequencies.
Coarse Array scan	Scans the Coarse bank capacitors in the Oscillator
Mid Array scan	Scans the Mid bank capacitors in the Oscillator
Fine Array scan	Scans the Fine bank capacitors in the Oscillator
Q divider sweep	Tests if the Oscillator Q divider block is functional
LNA and VGA gain sweep	Uses a TX signal looped back into RX to check the various gains stages of the LNA and VGA
FBDAC sweep	Scans the Feedback DACs digital words.
Audio loopback test	Uses loopback to test the amplifiers in the audio block
FM Max SNR BIST	Internally performs FFT to calculate the SNR number.

Table 7.1: FM BiSTs implemented in Orca

The next chapter deals with the methodology for implementing these tests in a new design.

CHAPTER 8: METHODOLOGY FOR IMPLEMENTING BISTS

Conventionally, the test generation process takes the following into consideration: system performance requirements, industry standards, design team inputs, process and technology considerations, trim and tuning requirements. These are used to generate a production test list with performance-based as well as defect-oriented tests. These can be complex like BER, EVM, etc., time-consuming, and requiring expensive instrumentation. A new methodology for implementing On-chip RF Built-in Tester (ORBiT) tests that have the following characteristics has been defined in this work:

- Tests that provide structural coverage of all design blocks not covered by digital tests, which ensure the absence of manufacturing defects and cover the fault models we have observed in RF/analog blocks.
- 2. Tests that include parametric tests like PHE, drift, lock, etc., which check for the health of the device in a manner similar to current based fault tests for digital logic.
- 3. Tests that are inherently BiSTs by nature, hence run mostly internally, are simpler and faster than the conventional RF tests.
- 4. Tests that are not derived directly from the datasheet.

In the following sections, the methods used for developing, specifying and implementing these tests in TIs 65 nm devices like Orca are discussed.

8.1 BiST Infrastructure

All the ORBiT tests were firmware based, i.e., some firmware code was written, which could be executed by the BT core's ARM processor. This firmware code was downloaded from the test program into the device's memory to manipulate the device's hardware registers and perform the necessary computations to arrive at the results which were also then stored in the memory. These results could then be read out from this memory and reported in the tester datalog.

The firmware infrastructure already existed for these multi-core devices with several processors, because along with the device a FW service pack was also available to customers to be run each time the device was brought up in functional mode. In order to create the BiSTs, this FW infrastructure was re-used to create the custom code required to implement each BiST. The code was usually developed in C programming language and when compiled, one of the outputs was an image file which could be downloaded into the device memory and executed.

In order for the download to be quick, the same parallel interface used for implementing the digital scan tests was used. In TI's RFCMOS devices, the IEEE P1500 standard was used to design a parallel 8-bit bus that could be used to download test code into the device memory and to transmit information from the device back to the tester. For this, functional pins were multiplexed in the test mode to act as data in/out pins. This was all defined in a detailed MS Excel sheet called the "Pin-Multiplexing Sheet". The Direct Memory Load Execute Dump (DMLED) principle was employed to run the tests using the P1500 interface.

The process of converting the FW image file into the correct format for the tester is called TDL generation. The TDL for each test was downloaded into the device memory, executed by the cortex, and then the results were again transported to the tester via the parallel interface and reported in the datalog.

Re-using the available digital infrastructure was the right thing to do to reduce overheads. However, it was important to verify early on that it was functional for the intended purpose of running the ORBiT tests as well. Digital logic and digital test TDLs are almost 100% simulated; the same is not true of the ORBiT tests, partly because of the lack of well-developed RF models that could be used for simulation and partly because of time pressure in the chip design phase. In the past, no designer would have liked to delay the design process to ensure that all the BiSTs were functioning! This mindset is changing, however, because of the demonstrated effectiveness and cost savings from these BiSTs. So, in order to ensure that the digital infrastructure would work for the ORBiT tests, "ORBiT infrastructure TDLs" were created using very basic FW code that exercised some portion of the RF blocks and was supposed to produce a predetermined result. These TDLs were generated for every core and were simulated before the design was finalized.

8.2 BiST generation Flow

TI's product development flow is interspersed with several milestones called Check Points. At Check Point 0, for example, TI solicits requirements from the customer and the Marketing team presents a Marketing Requirements Document. At Check Point 1 a high level technical analysis is presented to assess if TI can come up with a profitable solution that will satisfy the customer's requirements, and at Check Point 2, all the major players involved in producing a chip like the System, Design and Product Engineering teams present their plans to make the product a reality. At Check Point 2 the main task is to perform a test cost analysis for the prospective device. This analysis is very involved and includes considerations like test board hardware, sockets, tester platforms, test time, and a high level test list. The test cost target for the Orca device was that it be less than 2.5% of the AUP. For a device with AUP less than \$5, this was a very challenging goal to meet.

Figure 8.1 shows all the phases in the generation of the ORBiT tests. The BiST generation is broken into the following time frames:

- 1. Pre-Pattern Generation (PG): This is the phase during which design, simulation and layout of the device are carried out and it can last anywhere between nine months to two years or more. It is also defined as the time between Check point 0 and Check Point 3, which is right after PG.
- Post PG, Pre-Silicon: There is approximately a one-month gap between when the design is finalized, masks are generated and actual silicon is available for testing. This is the time when fabrication occurs.
- 3. Post-Silicon: This is the period when actual devices are available and are qualified, and characterized. Also the production test programs are created. This period can last from several weeks to months depending on the time to market pressures and the status of the device.



Figure 8.1: BiST generation flow

At Check Point 0, a requirements document is created called "The ORBiT requirements document" which includes a functional description of all the ORBiT tests. Full test coverage of the RF/analog blocks starts with a review of the block diagram of the analog areas of the chip in the early stages of the design (prior to Check Point 2). Such a block diagram enables the conceptual development of the tests leading to the creation of a high level description of the tests.

This functional test specification or requirements document is created by a System Engineer with help from a Test Engineer who has an understanding of the test environment. Design schematic reviews are the best way of ensuring that all the analog blocks are covered sufficiently. The requirements document also contains requests for any additional design hardware blocks or hooks that may be needed to enable the BiSTs.

This functional description can then be used along with device register definitions to create specifications and power-up sequences for the device that a Firmware Engineer can use to write appropriate FW to implement the test.

The time between PG and silicon arrival is used to create the FW based BiSTs, generate TDLs from the FW image files. First the infrastructure TDLs are debugged followed by the actual test TDLs once they are incorporated into the test program.

Once silicon is in hand, the ORBiT tests are first verified on the bench using an evaluation board, and then, ported to the VLCT. A Gauge Repeatability and Reproducibility (GRR) study is run, followed by qualification and characterization of the device and the device is "Released to Production" (RTP) for volume manufacturing which includes production testing. These are several phases of production testing with respect to ORBiT tests which are described in the following Section 8.3.

8.3 Phases of Production Testing

Production testing includes some stages that are in preparation for RTP and some following RTP; these are shown in Figure 8.2. The GRR study includes testing a predetermined number of devices (10 to 100) repeatedly on 2 to 4 testers with 2 to 4 boards to ensure that a particular test produces the same (or very similar) results on various setups. The GRR metric is based on mean and standard deviation and is described as follows.

Test standard deviation σ_t is given by Equation 8.1, where σ_r and σ_R are the standard deviation of repeatability and reproducibility.

$$\sigma_t = \sqrt{(\sigma_r)^2 + (\sigma_R)^2}$$
 Equation 8.1

Measurement Cp is given by Equation 8.2

$$Cp = \frac{(USL - LSL)}{6\sigma_t}$$
 Equation 8.2

and %GRR is given by Equation 8.3

$$\% \text{GRR} = \frac{100}{\text{measurement } Cp}$$
 Equation 8.3

On most parameters, GRR is expected to be lower than 10% for the parameter to be production-worthy. The GRR data, along with inputs from the Systems and Design Engineers, are used to determine limits for the ORBiT test parameters for the Characterization phase.



Figure 8.2: Phases of production testing

Characterization of some parameters that require specialized instrumentation is performed on the bench setup, while all the parameters that can be characterized on the VLCT are run there, because the VLCT is much faster and a larger number of units can be run in an automated fashion using the handler as opposed to an operator switching parts on the bench. Characterization units are chosen from the various process splits and they are run at a minimum of three temperatures (Room: 25°C; Cold: -40 °C; Hot: 85 °C) and several operating voltages depending on the Characterization Plan. The ORBiT tests are all characterized on the VLCT with the aforementioned limits. Characterization data demonstrates how the test will perform across all expected operating conditions and across all process variations expected during the fabrication process. In the Section 8.4 the method used to determine ORBiT test limits is described. Characterization is followed by the Qualification phase where a qualification plan is followed, which is designed so as to test the device under several conditions such as ESD (both Human Body Model and Charged Device Model), Latch-up, Humidity, and Temperature to study any device parametric shifts and Early Failure rate (EFR). There have been examples of ORBiT tests showing sensitivity to ESD failures even before a functional parameter registers a fail.

After qualification, the production test solution is prepared for volume production during the ramp stage and testers are brought online one after another at the production site. GRR data is collected for each tester and analyzed before that tester in included in the production line.

During Phase 1 of production test, data for both the RFC tests and the BiSTs are collected on approximately one million units in production. Devices that fail the conventional RF test, but are not detected as failing devices by the ORBiTs, are identified. The Quadrant Analysis procedure (described in Chapter 9) is used to resolve these units. During Phase 2, using the results of Quadrant Analysis, the RFC tests identified for replacement are removed and replaced entirely by the ORBiTs.

8.4 Setting limits for ORBiT tests

Since almost 80% of the ORBiT tests are structural in nature and check if a circuit component or stage is present and functional, block level design specifications are used to derive the initial limits for each of these parameters. For example, in the DCO capacitor scan test described in Section 7.3.6, the PVTL capacitors are supposed to contribute 2 to 5 MHz of frequency shift. This type of information is provided by the block level Designers and the Systems Engineers. GRR data consists of the mean and standard deviation for each parameter. This GRR data combined with the inputs from Designers and Systems Engineers is used to set what is termed as "preliminary" or "characterization" limits. These limits are set so that outliers are removed and a significant portion of the Gaussian distribution is well within the upper and lower limits. Figure 8.3 shows the characterization data for the PPA transistor scan test described in Section 7.3.8. The magenta, blue and green squares represent data for Hot, Mid-cold and Nominal process splits. It is clear that these test parameters are affected by process variations, so the production limits will have to be determined taking this fact into consideration.



Figure 8.3: PPA scan characterization data for three process splits

Hence, after characterization the limits are adjusted. The test program is then ready to RTP. Limits are calculated by using the mean (μ) and standard deviation (σ) as shown in Equation 8.4.

$$UTL = \mu + 6\sigma \qquad \text{Equation 8.4}$$
$$LTL = \mu - 6\sigma$$

In most cases engineering judgment is used when analyzing the distribution of the test to set limits so that outlier parts are excluded. For example, using Equation 8.4, the limits for the distribution shown in Figure 8.4 are marked by the red lines. However, it is clear that limits at the dotted black lines will be better to exclude outliers.



Figure 8.4: Setting limits to exclude outliers

One note here about using characterization data from Hot and Cold temperatures. Since the ORBiT tests were intended to check for structural issues and health of the circuits, room temperature data was sufficient. Hence only room temperature characterization data were used for the purpose of setting limits. If data from the other two temperatures were used, the variation would be so large that any limits set using that data would be too wide open to catch any actual limits. These limits were inserted in the characterization program and data were collected as described above.

8.5 Continue on Fail (COF) testing

In order to empirically calculate DPPM, the production data from one million units were analyzed. For the analysis, data for the RFC tests as well as the structural tests were needed. This implied a higher test time impact than that incurred when running RFC tests alone. This initial high test time was justified because once the analysis was completed the test-time intensive RFC tests were removed. For a high volume device that will run billions of units in its lifetime, the initial test time hit was negligible. Normally, during production testing, the test program was terminated as soon as the part fails a test, so that no additional tester time was wasted in testing a known bad unit. For this analysis data from all tests was required for every unit. Hence, for the one million units used for this analysis, testing continued until all the tests were executed; this is called Continue On Fail. The only exception was a continuity fail, since such a fail could cause high currents to flow through the device pin to the tester pin and actually damage the tester pin. So if a part failed continuity, no further tests were performed.

CHAPTER 9: DATA ANALYSIS METHOD

9.1 Why Quadrant Analysis?

The most common approach used to analyze data when trying to see if one test (in this case the RF conventional test) could be replaced by another one (in this case the ORBiT test) is to create a regression plot. The two parameters under consideration are plotted against each other and the R^2 is calculated. R^2 is a statistical measure of how close a regression line is to real data and is a unitless metric whose values range from 0 to 1. The closer the value is to 1, the closer the performance of the ORBiT test is to the RF conventional test. A R^2 of 1.0 (100%) indicates a perfect fit. The scatter plot of the collected RFC data (plotted on the Y axis) can be fit with the ORBiT data (plotted on the X axis) using least-squares as seen in Figure 9.1.



Figure 9.1: R² calculation

$$Y = Y_P + \varepsilon = c_1 X + c_0 + \varepsilon$$
 Equation 9.1

where, c_0 and c_1 are constant coefficients and ε is the fit (or prediction) error. It can be shown that the conventional RF test values can be optimally estimated using the following linear predictor [30].

$$Y_{P} = \left(\rho \frac{\sigma_{Y}}{\sigma_{X}}\right) X + \left(\overline{Y} - \rho \frac{\sigma_{Y}}{\sigma_{X}} \overline{X}\right)$$
Equation 9.2

where, ρ is the correlation coefficient between the measured *Y* and *X* data, σ_x is the standard deviation of *X* and \overline{X} is the mean value of *X*. The latter can be estimated by Equations 9.3 and 9.4.

$$\overline{X} = \frac{1}{N} \sum_{n=1}^{N} X_n$$
 Equation 9.3

$$\sigma_{X} = \sqrt{\frac{1}{N-1} \sum_{n=1}^{N} (X_{n} - \overline{X})^{2}}$$
 Equation 9.4

From these, the figure of merit R^2 is calculated as shown in Equation 9.5 [31].

$$R^{2} = \rho^{2} = 1 - \frac{\sum_{n=1}^{N} (Y_{n} - c_{1}X_{n} - c_{0})^{2}}{\sum_{n=1}^{N} (Y_{n} - \overline{Y})^{2}}$$
Equation 9.5

The R^2 metric can be used when making a one-to-one replacement of tests. Since most of the structural tests were not one to one replacements of the RFCs, this type of analysis could not be used. When data from two tests were plotted against each other they were naturally divided into 4 quadrants as shown in Figure 9.2, hence, the name "Quadrant" analysis. Each structural test had multiple parameters, each of which had a pass/fail
indictor or flag (1 or 0) based on limits that were used to determine them. Similarly, the RFC results could also be separated into 1 or 0 indicators using their limits. When the pass/fail flags of the structural tests were combined and plotted against the pass/fail flags of the RFC in question, the data were manageable and could be analyzed one quadrant at a time.



Figure 9.2: Four quadrants of data

9.2 Quadrant Analysis Procedure

The structural tests which included the ORBiT tests, Digital tests, trim tests, power management tests and IO tests needed to cover the test path were identified. These would be used to replace the RFC tests.

The Pass/Fail flags for the RFC tests were combined to create one Pass/Fail flag; the same was done for the structural tests. When the Pass/Fail flags were plotted against each other, 4 quadrants were obtained as seen in Figure 9.3. The units that passed both sets of tests were in the good-good quadrant and those that failed both sets were in the bad-bad quadrant, and since both sets of tests agreed on their status, no further resolution was needed for these units.



Figure 9.3: Four quadrants with pass/fail flags

The units that were good to the RFC but failed the structural tests were the "overkill" units. If the number of overkill devices was less than the expected defect density, then no action was taken for those. These units could be failing due to the added coverage provided by the structural tests. The units that fail the RFC but pass the structural tests were the "underkill" units. These underkill units were retested, failure analysis was performed and they were dispositioned. RFC tests that reached a 20 PPM underkill level were reviewed for removal. Based on this, the DPPM budget was adjusted. In this manner, the quadrant analysis procedure was used to categorize and disposition units that were detected as defective by the RFC tests, without performing R^2 analysis.

As mentioned in Chapter 3, after characterization a list of production tests was put together. For the Orca device, Table 9.1 lists all the RFC tests that were to be replaced in the left column and all the Structural Tests that would be used to replace them in the right side column.

RFC Test to be replaced	Structural tests
BT TX Power	Digital
BT Bit Error Rate (BER)	Analog BiSTs
FM Maximum SNR	IO tests
FM TX power	

Table 9.1: List of RFCs and the tests that will replace them

Chapter 10 covers the data and analysis used to replace these tests.

CHAPTER 10: DATA ANALYSIS RESULTS

This Chapter discusses the quadrant analysis results for the RX and TX paths in the BT and FM cores. In order to empirically calculate the DPPM impact of replacing the RFC tests with the structural tests, approximately one million units worth of production data were analyzed. Since the production test program had COF implemented, data for all tests were recorded for each unit. The ordering of the tests in the production program was paramount when it came to quadrant analysis. The tests were ordered by rank (using the ranking system described in Section 3.4, by Equation 3.1) so that the structural tests including the ORBiT tests were executed before the RFC tests. Figure 10.1 shows the yield loss associated with the various fail categories seen in the Orca device. In Figure 10.2, the test times of various tests are shown for comparison. It is clear that Continuity, Leakage and ODP tests had very low test time compared to the RFC Tests.



Figure 10.1: Fail percentages of various test categories



Figure 10.2: Average test time of various fail categories

When these tests were ranked using Equation 3.1, the Memory tests ranked highest followed by ODP and Continuity. The RFC tests ranked very low (at second last) because of their high test times and the LDO tests, while being fast tests, did not provide much value in terms of defect detection.

This method of ranking can be used to evaluate the effectiveness of the test, while taking into account its test time contribution. The rank of all Orca tests is shown in Figure 10.3.



Figure 10.3: Test category ranking

Figure 10.4 shows the production test flow for Orca.



Figure 10.4: Orca production test flow

The Orca production solution was a multi-site solution, meaning several units could be tested in parallel. The board had eight sockets, so at most eight devices could be tested in parallel. With this flow, it was easy to isolate units that failed only the RFC tests, because they were binned as RFC test failures, and these were now underkills. Once the underkill units were known, the wafer skeletons (the non-good bin units left on the wafer after the good bin units were shipped to customers) with the underkills were shipped back for evaluation. Figure 10.5 shows the steps after the wafer skeletons were received.



Figure 10.5: RFC fail isolation and resolution

First the units that failed only the RFCs in production were picked from the wafer skeleton, and then, they were retested on a "Golden" Tester, which was a well-calibrated known-good tester. Sometimes units that failed RFCs in production would pass when retested because the production setup probably required recalibration when those units were tested. If this happened, those units were considered good-good units and taken out of the underkill bucket. During Step 3 the retest data were analyzed to check if the underkill units were detected as fails by any other test. This could happen because the production test program that was used to test the underkills could be outdated by the time these units arrived from the production floor and updates to the program like limits changes or addition of new tests had to be considered. This could also happen if the device was damaged during handling or was a reliability problem known as a "walking wounded". Meaning, it may have failed only the RFC in production, but other performance parameters were slowly degrading and when retested that degradation was obvious because of other parameters failing. Such devices usually failed the continuity tests and several other structural tests. These were also removed from the underkill bucket. In some cases, units would continue to fail only the RFC when retested on the "Golden" tester (Step 4). In such instances, the units were retested on the bench setup because the bench boards most closely mimic the customers test environment and some units did pass when tested on the bench. This behavior was seen in case of units that failed BT Sensitivity BER and was attributed to noise on the tester. Step 5 involved retesting the underkills with the most current ORBiT tests. If the underkills were not identified as bad units, either a new test had to be designed to detect it or the units were to be added to the DPPM count.

10.1 Sensitivity BER Quadrant Analysis

BT Sensitivity BER test was the lowest ranked RFC test in the Orca production program because it was complex and required abound 3.5 s of test time. As mentioned in Section 3.5, the Sensitivity BER test is sensitive to interference from signals being received by neighboring devices on a multi-site board. So, on the Orca octal site solution, devices are tested four at a time. A checker board pattern of testing was implemented so that devices that were tested simultaneously were as spatially separate as possible. Figure 10.6 shows how the eight sites were located on the octal site board and the sites marked with the same color are tested in parallel.

Site 8	Site 6	Site 4	Site 2
Site 7	Site 5	Site 3	Site 1

Figure 10.6: Octal site solution with checkerboard pattern for Sensitivity BER test

This effectively doubled the test time of the Sensitivity BER test to about 7 s.

Figure 10.7 shows how the BER dropped down to 0 as the SNR rises. This was because the receiver's ability to distinguish between bits improves as the energy of the received signal increases.

In most RFCMOS DCOs, thermal noise was the main contributor of noise under sensitivity conditions, but for the Orca device, the DCO phase noise was the more dominant noise source.

When ~one million units were analyzed for this test, there were about 2,500 underkill units. After these units went through the fail isolation and resolution procedure

it became clear that a new test would be needed to detect the BER failures. At that point the ORBiT test list contained a PHE test in the TX mode.



Figure 10.7: BT BER versus SNR

So, it was surprising that all the BER fails were not being caught by that test. Both the test procedure and the data were analyzed with the System Engineers and a gaping hole in the test coverage was revealed. Figure 10.8 shows the block diagram of the BT core with each block colored according to the LDO (Low Drop-Out) power supply that supplied it. Two points must be noted here:

1. The RX and TX paths had separate frequency divider circuits. This meant that a PHE test done in the TX mode might not reflect the phase noise properties of the device in RX mode. Hence it was necessary to perform the PHE test in RX mode.

2. The DCO and its dividers were supplied by the same LDO. The design team theorized that the RX divider had problems that caused it to draw more current from the DCO LDO while operating which translated to noise affecting the DCO performance.

Due to these reasons, a RX PHE test was implemented and it was found that almost 32% of BER fails in production were caught by RX PHE.



Figure 10.8: BT core block diagram with LDOs.

Figure 10.9 shows the Pareto analysis for the Sensitivity BER test. The second largest category of tests that caught the Sensitivity BER fails was Digital DFT. This was expected since any defects in the digital sections of the design could affect the RF blocks because they were controlled by the digital blocks. The digital blocks covered around 70% of the design and they were tested using ATPG techniques.



Figure 10.9: Categories of structural tests that detect Sensitivity BER fails

It can be seen from Figure 10.9 that the other higher order tests that detected BER failures were Trim and EFUSE tests, ODP tests, Continuity tests, etc. These tests were relatively easy and inexpensive to perform in a production test environment, and hence, were ranked high.

While most of the sensitivity BER failures were detected by the RX PHE test, the other BiSTs that detect the remaining sensitivity BER fails were DCO Capacitor Scan test, Receiver Gain test, Pre Power Amplifier (PPA) Scan, Feedback DAC test, Image Rejection Ratio (IMRR) test, IFPOLE test, and RX drift test. Figure 10.10 shows a Pareto analysis of the categories of ORBiTs that detected BER fails.



Figure 10.10: Categories of ORBiTs that detect BER fails

18 units in the one million analyzed failed the conventional Sensitivity BER test and were not detected as fails by any structural test. These counted towards the DPPM when the Sensitivity BER test was removed.

10.2 BT TX Power Quadrant Analysis

The BT TX power conventional test had several components. The full list of parameters is shown in Figure 10.11 and these included measurement of transmitted power of the fundamental frequency in the EDR and GFSK mode as well as power in the adjacent channels to the left and right of the fundamental. It also includes measurement of current while the device was transmitting. The goal of this quadrant analysis was to replace all these parameters.

Conventional Tests
BTTX_P_G_S14_P0
BTTX_P_G_S15_N3
BTTX_P_G_S15_N2
BTTX_P_G_S15_N1
BTTX_P_G_S15_P0
BTTX_P_G_S15_P1
BTTX_P_G_S15_P2
BTTX_P_G_S15_P3
BTTX_I_G_CL15IN_S15
BTTX_I_G_MLDOIN_S15
BTTX_I_G_VIO_IN_S15
BTTX_I_G_LDOIN_S15
BTTX_I_G_LDOIN_W_IO_S15
BTTX_P_G_STEP_S15_S14BTTX_P_E3_S14_P0
BTTX_P_E3_S15_N3
BTTX_P_E3_S15_N2
BTTX_P_E3_S15_N1
BTTX_I_E3_LDOIN_S15
BTTX_I_E3_LDOIN_W_IO_S15
BTTX_P_E3_STEP_S15_S14
BTTX_P_REL_G_E3_S15 BTTX_P_E3_S15_P0
BTTX_P_E3_S15_P1
BTTX_P_E3_S15_P2
BTTX_P_E3_S15_P3
BTTX_I_E3_CL15IN_S15
BTTX_I_E3_MLDOIN_S15
BTTX_I_E3_VIO_IN_S15

Figure 10.11: BT TX Power test parameters

The BT transmit power parameter during Class 1.5 operation was specified to be greater than 8 dBm and less than 13 dBm. Figure 10.12 shows the histogram for the transmitted power with EDR3 modulation at the highest PA power setting in the 2402 MHz frequency band. It was very well centered and was not seen to be marginal in characterization. All the other parameters listed in Figure 10.11 show similar performance in terms of design margin. This test was included in the production program during Phase 1 for test coverage of the TX path of the device. So, this was the next test to be replaced by structural tests.



Figure 10.12: Histogram of BT TX Power with EDR3 modulation

The initial quadrant analysis on approximately one million units was performed by combining pass/fail flags of the RFCs and comparing them against the combined pass/fail flags of the ORBiTs in the BT TX path. Figure 10.13 shows that there were 697 underkill units which had to be resolved.

Almost 98% of these underkills were converted to the good-good bucket when they were retested, meaning they passed the RFC tests. So, they failed in production testing because of tester calibration and site offset issues. This is a common and prevalent issue with RFCs that require well-calibrated test setups and reiterate the case for replacing these tests with structural tests that are independent of setup.

PF		Good	Bad
้อ	Good	989920	697
0	Bad	3075	149
BB			
'в			
'. -			
l t			
sts			

PF_all_BT_TX_Pwr_conventional_tests

Figure 10.13: Quadrant Analysis of BT TX Power tests.

Nine of these units were detected by ORBiT tests through re-adjustment of their limits, and 6 units could not be detected by any structural tests and went towards the DPPM count as underkills. It should be noted here that the underkill due to the structural tests was quite high (~0.1%). Almost 80% of these devices came from four wafers with the signature shown in Figure 10.14. It was concluded that this was process-related and not of much concern.



Figure 10.14: Wafer with BT TX Structural overkill pattern

Figure 10.15 shows a Pareto analysis of the tests that detected the transmit power test fails. In this case, the Digital tests were able to detect most of the transmit power failures. When the underkill were retested on the bench, it was found that a majority of the units that failed the transmit power test in production retested to be good units. This was because accurate transmit power measurements were not possible in a production test environment. So, in reality, the RFC in production was "over-killing". The trim, ODP, memory BiSTs and current tests also detected a large percentage of the parts that failed transmit power.



Figure 10.15: Categories of structural tests that detect BT TX RFC fails

A defect in any digital block that supported the transmit function or in a memory block would immediately affect the transmit power measurement because it would affect the modulation. The RF BiSTs detected only around 0.02% transmit power failures. Although this seems like a very small number, it was imperative for coverage and to keep the DPPM low. Figure 10.16 shows the Pareto analysis of the RF BiSTs that detected transmit power defects.



Figure 10.16: Categories of ORBiTs that detect BT TX RFC fails

The defects in the underkill devices are being studied as part of future work so that more BiSTs can be put in place to eliminate them.

10.3 FM TX Power Quadrant Analysis

The FM TX power parameter also exhibited good margin during the characterization phase as seen in Figure 10.17. The datasheet specification is that the performance should be higher than 117 dB μ V across all FM frequencies.



Process and Temperature Splits

Figure 10.17: FM TX power at 107.9 MHz across process and temperature

The initial quadrant analysis over approximately one million units showed that 715 units were underkills. When these devices were retested on the "Golden" tester, about 96% of these retested to the good-good bucket. Again, the reason for this was the poor quality test setups at the production sites. 24 of the underkills were dispositioned by tightening the limits on some ORBiT tests. An example is shown in Figure 10.18: the solid black lines show the new tightened limits while the dashed lines show the old limits. Such limits changes were made on several parameters such as the FM PA test and the FM Trigen test to disposition the 24 units. After these changes, three units remained as underkills and counted towards DPPM.



Figure 10.18: ORBiT test limits adjustment

The FM TX power RFC was a 600 milliseconds long test, with all eight sites on the board tested simultaneously. However, the next production test solution planned for Orca is a 16 socket solution. As mentioned earlier, the VLCT has limited RF resources and it cannot make a RF power measurement on 16 sites in parallel. So, in order to enable the 16-site solution, it was paramount that the FM TX power RFC be eliminated. The ORBiT tests checked for coverage till the device pin, but there was no way of guaranteeing that the device pin (or ball) was covered, i.e., if the ball were missing or shorted it was not certain if any ORBiT test would be able to detect it. In order to prove that a missing or shorted ball could be detected, a missing ball was simulated by covering it with insulating tape and a shorted ball was simulated by actually shorting 2 neighboring balls with solder as shown in Figure 10.19.



Figure 10.19: Orca WSP package with tape and short

All the ORBiT tests were executed on these two devices and found that several test parameters in the TX path were able to detect these two conditions. Figure 10.20 shows how the TX tuning capacitor sweep test was affected. The blue and magenta lines show the behavior of the devices before the experiment, while the cyan and yellow lines show their behavior after the changes were made. The reason for this effect is believed to be the change in impedance that the device saw at the TX pin when the ball was shorted or missing, which affected this test data. This experiment successfully proved that the structural tests implemented to test the transmit path of the FM core were sufficient to detect all known fail scenarios and enabled not only test time reduction, but also a higher multi-site solution.



Figure 10.20: TX Ctune capacitor sweep data

10.4 FM Maximum SNR Quadrant Analysis

The FM Maximum SNR parameter performance of Orca's FM core was found to be marginal to the 57 dB (57.5 dB production test limit with guard band) specification during characterization. Figure 10.21 illustrates the variation over process and temperature.



Figure 10.21: FM SNR across Process and Temperature

The X-axis shows various DOE splits, where CC, HH, NN represent the Cold-Cold, Hot-Hot process corners and Nominal material at room temperature, 85°C and -40°C. Cold, Hot and Nominal refer to the NMOS and PMOS doping that affect the drive currents (Idrive.) of these transistors. The Y-axis represents the SNR values. So, it was obvious that even at room temperature there were nominal material units that did not have Cpk between 1.67 and 2 and were very marginal to the 57 dB specification.

The RFC FM maximum SNR test was described in detail in Section 3.6 and it required external instrumentation, marked by red in Figure 10.22, and had a high test time in the range of 1.2 s. Since the parameter did not have sufficient design margin, the only way to achieve reduction in test time was to perform the calculation of SNR internally. So, a BiST which used a 107.9 MHz FM modulated signal and instead of capturing the data at the Audio pins was implemented, FFT was performed internally and SNR was calculated. The setup used for the BiST was similar to the one shown in Figure 10.22, except that the data is not captured at the Audio out pins.



Figure 10.22: FM SNR test measurement setup

It was processed internally by the ARM Cortex. An external -47 dBm RF carrier source signal of frequency fc Hz was frequency modulated with a 1 kHz tone and fed into the

device. The down-converted signal was then digitized and demodulated by the FM device. The demodulated signal was sampled at 48 kHz and stored in the internal memory of the device. A total number of 768 samples were collected to be processed internally with an FFT based BiST with resolution bandwidth of 48 kHz/768 = 62.5 Hz. The selection of sampling frequency and amount of collected data resulted in the FM tone at exactly FFT bin 1 kHz/62.5 = 16.

The 768 samples were stored in three separate buffers of size 256 each. A 256 point FFT was computed on each buffer using a 3-term Blackman Harris window. This particular window was chosen to minimize the side lobe leakage that could have been caused by frequency offset in the LO. The three 256 point FFTs were combined using a radix-3 implementation to form a 768 point FFT. This was done so that the overall computation complexity of computing a 768 point FFT was reduced.

The next step was to compute the power spectrum of the samples. The power spectrum was then A-weighted. The signal power was computed by adding the power spectrum of five bins around the tone bin. The noise power was computed by adding the power spectrum of the remaining bins between 300 Hz and 15 kHz. The power in the harmonics of 1 kHz FM tone was removed from the noise power calculation as these harmonics did not contribute to the noise power.

To reduce the estimation variance of the signal power and the noise power, they were both averaged over eight bursts of 768 samples. The resulting averaged power values were used to compute the FM SNR.

The correlation between the RFC SNR and the BiST SNR was performed using the R^2 analysis method detailed in Section 9.1. The initial correlation between the FFT-

based BiST described above and the conventional FM SNR test had an R^2 value of around 0.775. In order to remove all units that measure less than 57 dB, the corresponding limit placed on the BiST had to be 60 dB (See Figure 10.23).



Figure 10.23: Conventional SNR test vs. BiST SNR (initial)

This would lead to an overkill of about 25%. The parts that failed the BiST but passed the conventional test were the overkill units. Hence, it was necessary to improve the R^2 value. In order to do this the Design Of Experiments (DOE) method was used. The main parameters identified for the DOE analysis were as follows:

- 1. The number of times the signal power and noise power are averaged before calculating the SNR value.
- 2. The delay time allowed for the RX chain to settle before data is collected to calculate SNR.

The DOE legs shown in Table 10.1 were derived from the 2 variables above. The experiment involved testing about 150 units covering various process corners, so that a good regression line could be plotted.

DOE Legs	Averages	Delay
1	4	45 ms
2	4	90 ms
3	8	45 ms
4	8	90 ms

Table 10.1: DOE Legs

The plot in Figure 10.24 shows the analysis of the data collected with the settings shown in Table 1. The Y-axis shows the R^2 of the BiST versus the conventional test normalized to the R^2 from 2 runs of the conventional test. This plot clearly shows that averaging the signal and noise power eight times and adding a 90 ms delay (Leg 4) yields a good R^2 value of greater than 0.975 (normalized). The data for this leg is shown in Figure 10.25. It was seen that there was still around 2% overkill, but that was tolerable for the test cost savings achieved by using the BiST.







Figure 10.25: Conventional SNR test vs. BiST SNR (final)

This concludes all the data analysis that was performed for ORBiT-based test time reduction on Orca. Table 10.2 shows the time it takes to test the Orca device before and after quadrant analysis was done. This has enabled about 38% test time reduction.

Test Name	Test Time in seconds		
	Before Quadrant Analysis	After Quadrant Analysis	
Continuity + ODP	0.96	0.96	
Trim	2.39	2.39	
Digital	6.23	6.23	
ORBIT FM	2.89	2.89	
ORBIT BT	2.44	2.44	
BER	7	N/A	
BT TX power	0.45	N/A	
FM SNR	1.2	N/A	
FM TX power	0.45	N/A	
Total Test Time	24.01	14.91	
Test Time Reduction	38%		

 Table 10.2: Orca test times before and after quadrant analysis

10.5 Summary

By using this methodology for implementing RF BiSTs the empirical calculation of DPPM for the Orca device has been performed. There were only 27 RFC fail units that the ORBiT tests could not detect as failures, hence these were the underkill/DPPM. This proved that the structural tests developed using the proposed fault models were valid and sufficient replacements for RFC tests. Since the DPPM i.e., the underkill was found to be much lower than the DPPM budget, this data was presented to Quality Engineers over the period of the last 18 months and the test replacements were made after their approval.

The area occupied by RF circuitry was around 30%, while in the past the test cost (in terms of test time) of RF circuitry was disproportionately high, being about 50 to 60% of the total device test time. Now with ORBiT tests the RF test time was proportional to

its area and is about 36% as seen from Table 6. Thus ORBiT enabled RF test to achieve the same entitlement as Digital Tests. This is a new paradigm in the world of RF production testing and will serve as the benchmark for future RFCMOS SoCs.

CHAPTER 11: CONCLUSIONS AND FUTURE WORK

This methodology for implementing BiSTs and the analysis that was done on actual production devices to replace RFCs are at the core this dissertation research. It is unprecedented in the area of RF production testing to replace all functional tests that guarantee specifications and replace them with BiSTs that check for structural integrity and circuit health. The implemented ORBiTs tests have successfully replaced the RFCs on the BT and FM cores of Orca enabling a 16-site solution and reducing test time in production by about 38%. This was possible because the total DPPM impact of replacing these RFCs was 27 units, which was well under the DPPM budget of 200 units. This DPPM calculation was empirical because actual production data from one million units was used and all units that failed only the RFCs were retested to arrive at this number. This validated the procedure of RFC replacement and proved that the BiSTs were sufficient replacements.

The RF defect models proposed in this dissertation are new additions to the existing body of knowledge on RFCMOS devices and have enabled the implementation of a defect-oriented test methodology. The research work done for this dissertation helped quantify the probability of occurrence of defects based on these defect models. The BiSTs that have been built using these defect models employed some novel techniques such as sideband detection, which had not been used previously for such test.

The quadrant analysis technique developed to analyze the ORBiT data was developed specifically for these datasets and represented a new method that could be used for analyzing large datasets with hundreds of parameters that did not have many inter-dependencies. To correlate two parameters which are similar such as the RFC FM SNR and the BiST FM SNR test, the regression analysis method was sufficient. The analytical equations developed for DPPM, yield and overkill estimation of a marginal parameter were new to this body of work and have very valuable applications, such as specifying mean and sigma values of a certain functional parameter to designers so that the design has good margin that will enable defect-oriented test.

The BiSTs that were designed for these cores are portable along with the core designs. They have been successfully implemented in 3 other 65 nm devices with these cores.

Several improvements can be made to this methodology. For example, the TDL generation process can be made more generic so that each core does not require separate TDL generation scripts. It will also be beneficial to continue studying the 27 underkill units to understand the root cause of failure, so that either new BiSTs can be developed to detect them or design can be improved. It would be beneficial on future designs to include more simulations on the ORBiT test itself before it is converted to TDL. Currently, each TDL is simulated to ensure that the digital control infrastructure is functional; during this simulation the actual ORBiT test itself is treated as a black box which toggles the test status pin called TEST_EXEC. This pin is driven high and low by the processor at the beginning and end of the test respectively. Better and more complete analog models will help to make the simulations more accurate and thus help with better test coverage.

To conclude, implementing this methodology has enabled higher profit margins on high volume, low AUP RFCMOS SoCs through test cost reduction.

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APPENDIX A: DESCRIPTION OF RESEARCH FOR POPULAR PUBLICATION

It is 11.00 am on a sunny Saturday in Mumbai, India and Mrs. Kumar's maid Maya has not showed up for her usual Saturday morning shift to help with lunch preparations and cleaning. So, Mrs. Kumar calls Maya on her cell phone to inquire. Cell phones are now ubiquitous the world over because they are affordable even to people like Maya who live on less than \$100 a month. This proliferation has been enabled by several factors such as the rapid development of cell phone infrastructure, advances in telecommunications technology, and the commoditization of the chips that are used in cell phones. With 60% of the world's citizens having access to cell phones, they have evolved from being a luxury item to a commodity that people take for granted.

Early radio chips were manufactured in the expensive and complex Silicon-Germanium technology, but advances in process and design techniques enabled RF devices to be made using silicon processes, enabling integration of digital and RF circuits on the same silicon chip. This was followed by the integration of multiple radios on the same piece of silicon, further driving costs down.

These radio chips are now available for under \$5 and are manufactured in volumes of several hundred million. Companies like Texas Instruments, Broadcom, Qualcomm etc. use the same foundries and technologies and are charged more or less the same price for a wafers. Test cost, however, varies from company to company and can be the market differentiator to generate larger profit margins. Deepa Mannath, a PhD student in the University of Arkansas' interdisciplinary Microelectronics-Photonics graduate program has done her PhD research at Texas Instruments in the area of test cost reduction for high volume RF devices. Ms. Mannath says, "TI's emphasis on reducing test cost

remains high because it is one of the few knobs TI can turn that will help increase profit margins on a per device basis".

Traditionally, testing of RF devices entailed checking for functionality and verifying adherence to complex specifications. Rick Hudgens, a Product Engineering Manager at Texas Instruments thinks that "RF tests that verify functionality are antiquated and need to be replaced with structural tests, just like the digital boys did in the eighties!" Such RF tests were complex and time-consuming, requiring expensive instrumentation. They actually checked whether the device was functioning the way it was intended to in the operational mode. For instance, the transmit power test would check if the device is putting out the right power level with the right data or voice information. Firstly, it is not feasible to check all possible functionalities on the complex chips in the production line, and secondly, the low test cost budgets warrant drastic measures such as reduction of test time. When customer demand increases, companies like TI should be able to crank up the volume within a short period of time without any capital investments in terms of test hardware and instruments.

Ms. Mannath's methodology presented in her dissertation enabled test cost reduction by replacing the conventional RF tests with tests that are defect-based and are run internally. It is possible to do this on today's highly integrated silicon devices because of the availability of high-end processing capability on-chip. This methodology has made RF test cost on these chips proportional to the area occupied by RF circuits, which is about 30%. Ms. Mannath's work has created a new benchmark for test cost of RFCMOS devices. Widespread application of these techniques will help companies improve profit margins while delivering affordable cell phones to a world population
with a seemingly unquenchable thirst for such technology. People like Maya will be able to continue buying cell phones and subscribing to cell phone service, thereby widening their scope for opportunities to pursue economic development for themselves and their families.

APPENDIX B: EXECUTIVE SUMMARY OF NEWLY CREATED INTELLECTUAL PROPERTY

The methodology for implementing RF BiSTs in this dissertation is newly created IP since it was pieced together using some pre-existing methods used for the implementation of Digital BiSTs and adapting them for firmware-based RF BiSTs.

The RF defect models which have been identified and verified empirically in this dissertation have been proposed for the first time with reference to RFCMOS SoCs.

The BiST technique of using sidebands to detect signal levels is novel. This technique is used in both the BT and FM cores and it has been recommended for an internal Manufacturing Incentive Award (MIA), the case for which will be reviewed in January 2011.

The quadrant analysis technique used in this dissertation is unique because it offers a simple way to analyze large volumes of structural test data without actually performing a regression analysis on each and every BiST parameter.

APPENDIX C: POTENTIAL PATENT AND COMMERCIALIZATION ASPECTS OF LISTED INTELLECTUAL PROPERTY ITEMS

C.1 Patentability of Intellectual Property (Could Each Item be Patented?)

Patent applications have been submitted internally to TI, but were not pursued as testrelated IP are not detectable by competitors and cannot be defended. The author was encouraged to submit for Manufacturing Incentive Awards (MIAs) which recognize cost savings of greater than \$1 Million.

C.2 Commercialization Prospects (Should Each Item Be Patented)

No, for the reason described above.

C.3 Possible Prior Disclosure of IP

All the material in this dissertation has been published or been submitted for publication. The publications are listed in Appendix G.

APPENDIX D: BROADER IMPACT OF RESEARCH

D.1 Applicability of Research Methods to Other Problems

This methodology cannot be applied to any other problem.

D.2 Impact of Research Results on U.S. and Global Society

No major impact.

D.3 Impact of Research Results on the Environment

No impact.

APPENDIX E: MICROSOFT PROJECT FOR PHD MICROEP DEGREE PLAN

Microsoft Project was not used to track progress on this TI project. So, the project plan was not attached.

APPENDIX F: IDENTIFICATION OF ALL SOFTWARE USED IN RESEARCH AND

THESIS/DISSERTATION GENERATION

Computer #1: LTA0866361

Model Number: D620, Serial Number: 0T7570 Location: Texas Instruments, Dallas, TX. Owner: Texas Instruments, Inc.

Software #1:

Name: Microsoft Office 2007 Purchased by: Texas Instruments

Software #2:

Name: MATLAB R2008b Purchased by: Texas Instruments

Software #3:

Name: Spotfire Purchased by: Texas Instruments

Software #4:

Name: Microsoft Visio Purchased by: Texas Instruments

Deepa Mannath

Dr. Simon S. Ang

APPENDIX G: ALL PUBLICATIONS PUBLISHED, SUBMITTED AND PLANNED

- 1. "Decoupling with Anodized Ta" L Schaper, R. Ulrich, D. Mannath, J. Morgan, K. Maner, IPC February 2004.
- 2. "Advanced Decoupling in High Performance IC Packaging" Deepa Mannath, Leonard W. Schaper, Richard K. Ulrich. ECTC 2004.
- 3. "Yield and Reliability of Tantalum Pentoxide Integrable Decoupling Capacitors" Deepa Mannath, Anurag Yadav, Leonard W. Schaper, Richard K. Ulrich, Viswas Reddy Pola, University of Arkansas. IMAPS 2004. 37th International Symposium on Microelectronics.
- 4. "Yield enhancement of VCO Inductors and Capacitors through Process and DFT" Deepa Mannath, Ali Syed. TI Yield Symposium, June 2006.
- 5. "RF BIST in DRP2: Implementation and Data" Deepa Mannath, Cui Mao, Val Besong. TI Symposium for Test, August 2007.
- "The Implementation of Built-In Self Tests in a Digital Radio Processor (DRPTM)" Cui Mao, Deepa Mannath, Val Besong, Oren Eliezer, Scott Larson. The 8th IEEE Workshop on RTL and High Level Testing, Beijing, China, October 2007.
- 7. "ORBiT implementation, data and correlation in ORCA's DRPb core" Deepa Mannath, David Cohen, Cui Mao, Victor Montano, Rohini Kesavan. TI Symposium for Test, August 2008.
- 8. "A Reduced-Cost Built-in Self Test for an FM Receiver" D. Mannath, V. Montano-Martinez, I. Syllaios, S. Bhatara, M. Attaluri, Z. Parkar and S. S. Ang. IEEE DCAS October 2010.
- 9. "Structural Approach for Built-in Tests in RF Devices Deepa Mannath, Dallas Webster, Victor Montano-Martinez, David Cohen, Shai Kush, Thiagarajan Ganesan, Adesh Sontakke. IEEE ITC 2010.
- 10. "A Statistical Approach for Design and Testing of Analog Circuitry in Low-Cost SoCs", Oren Eliezer, Bogdan Staszewski, Deepa Mannath. IEEE MWCAS 2010.
- 11. "Implementation of BiSTs to replace BER and TX Power Production Tests in Bluetooth devices" Deepa Mannath, David Cohen, Víctor Montaño Martínez, Simon Ang and Shai Kush. Submitted on 08/31/2010 to Journal of Electronic Testing: Theory and Applications for publication in Special Edition on RF test in 2011.

APPENDIX H: PLAGIARISM CHECK

This dissertation was submitted by Deepa Mannath to http://www.turnitin.com for plagiarism reviewed by the TurnItIn Company's software. I examined the report on this dissertation that was returned by that plagiarism review site and attest that in my opinion the items highlighted by the software are incidental to common usage and are not plagiarized material.

Ken Vickers Director, MicroEP Graduate Program

Dr. Simon S. Ang Dissertation Director