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Design and Control of a Bidirectional Dual Active Bridge DC-DC Converter to Interface Solar, Battery Storage, and Grid-Tied Inverters

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A thesis submitted in partial fulfillment
of the requirements for the degree of
Honors Bachelor of Science
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by

Kenny George

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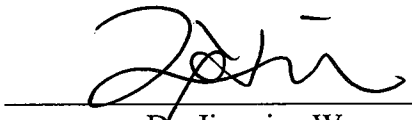

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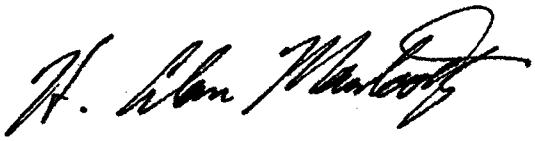

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Abstract

In order to further reduce the size of today's power converters, wide bandgap semiconductor technologies are being explored. These devices, such as silicon carbide (SiC), have been shown to outperform their silicon counterparts when used in high frequency switching, high temperature, and high voltage applications. These properties make them highly desirable in the bidirectional dual active bridge power converter. Being an isolated converter topology, the dual active bridge employs a transformer to provide step-up/step-down functionality and galvanic isolation for the converter. Transformers, as well as other passive components such as inductors and capacitors may be reduced in size when higher switching frequencies are employed. SiC devices used in this application can in turn provide a means to shrink overall system size and increase the power density of the converter, proving further the viability of power electronic systems in applications that require compactness and high efficiency. The aim of this thesis is to demonstrate the performance benefits of SiC MOSFETs in the dual active bridge topology. A justification for the choice of topology is included in this work, along with all of the appropriate design considerations and analysis, leading to the design of a 2kW dual active bridge converter. Modern modeling techniques are also explored and used to develop an enhanced digital controller, implemented in a DSP, for steady state reference tracking and load disturbance rejection. A demonstration of the designed converter verifies the analysis techniques explained therein.

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1. INTRODUCTION

1.1 Problem: Intelligently Interfacing Solar Power and Battery Storage with Grid

Demand for sustainable electric power has never been higher. In order to meet this demand, electric power systems must evolve to allow for integration of renewable energy sources, such as wind and solar, and to also provide high capacity battery backup under blackout conditions. One proposed solution is the smart green power node (SGPN), a modular intelligent power flow controller that interfaces solar panels and battery storage with the utility grid at the residential load level. Not only does the SGPN present a means for individual households to use solar power, but it also facilitates an unprecedented level of user control via its intelligent load forecasting and reporting.

1.2 Thesis Statement

At the heart of the SGPN are the power electronic systems, which enable the employment solar panels and battery storage elements. Prior research has been conducted on such power converters using silicon semiconductor devices, and found to be quite large do to their excessive losses and relatively low switching frequency. Modern wide bandgap semiconductor devices, such as silicon carbide (SiC), present many desirable dynamic characteristics that apply to medium and high power switching converter systems. This research seeks to demonstrate the size and efficiency benefits of SiC based converter systems as they are applied to the SGPN technology. This will be validated through the development of the system's bidirectional dc-dc converter, which acts as the interface between residential dc loads, a solar and battery fed low voltage bus, and a high voltage dc bus feeding a grid-tied inverter. Results will be presented that either support or refute the claim for potential of next generation SiC devices to replace pre-existing silicon based converter systems as the norm.

1.3 Approach

In developing modern power electronic converters, several design considerations come into play. System level specifications must first be identified based on power rating and bus voltages, which coincide with ancillary power electronic systems (i.e. grid-tied inverters, battery charge converters, etc.). A converter topology must then be selected and designed to meet the aforementioned requirements. Advanced modeling techniques must be applied in order to develop appropriate control schemes, which stabilize the converter and enable intelligent power flow. Finally, a working system must be constructed and tested using selected components and a digital controller.

1.4 Potential Impact

Operating switching converters at higher frequencies will reduce overall system size, which will make new applications for such converters more feasible. However, current silicon based designs are limited in their frequency of operation capabilities due to the excessive losses they incur during hard switching phases. Silicon carbide semiconductor devices exhibit material properties, which make them an optimal choice when high frequency operation is desired. When these devices are employed, higher density power converters can be realized. Applications for such converters include distributed generation in the future smart grid, plug-in electric vehicles, space exploration, and various extreme environment electronic systems.

1.5 Organization of Thesis

This thesis is organized into seven chapters. The first chapter is an introductory chapter that introduces the thesis topic and includes reasoning behind the proposed research. The second chapter briefly introduces the smart green power node system model and discusses which subsystems are at play, specifically the bidirectional dc-dc converter that will be explored in more depth. The third chapter develops the fundamental principles of operation of the dual active bridge, the selected dc-dc converter, and its related design considerations. The fourth chapter covers the controller design for the dual active bridge, which will include the construction of an optimal system model, controller type selection, load disturbance considerations, and digital implementation. Chapter Five will provide details on auxiliary electronics systems needed to operate the convert. These subsystems include feedback sensors and signal conditioning, power supplies, and signal isolators. The sixth chapter will outline testing procedures used to validate converter operation and the resulting measurements. Closing in the seventh chapter, a discussion of results will be presented as well as the impacts of this work and recommended future work.

2. PROPOSED SYSTEM LEVEL OVERVIEW

2.1 Smart Green Power Node

The proposed smart green power node (SGPN) interfaces battery storage and solar power elements with residential dc loads and the utility grid. The system consists of several interconnected power electronic converters, such as those that connect the batteries and solar panels with a low voltage bus, the isolated dc-dc converter that steps up the low voltage bus and controls power flow, and the grid-tied inverter.

The work of this thesis will be centered on the design of the isolated dc-dc converter that interconnects the low voltage and high voltage busses. The dual active bridge is selected based upon its desirable characteristics, such as its symmetry, reduced filter size, and its ability to more easily realize soft switching [1][2]. Additionally, because the DAB utilizes eight switching devices, as opposed to the 4-switch Dual-Half Bridge converter, it's effective power rating can be pushed much higher.

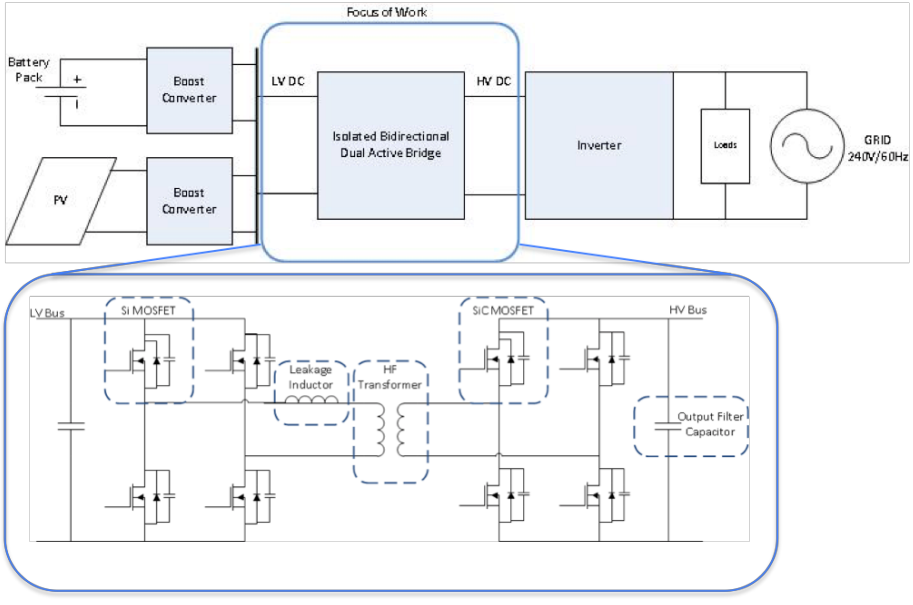

FIGURE 1: SMART GREEN POWER NODE SYSTEM

2.2 System Specifications

In order for the converter developed in this thesis work to be compatible with previous versions of SGPN, it must meet standing system specifications, but with a higher target efficiency. System specifications for this work are given in Table I below. Those parameters that specifically apply to the dual active bridge are bolded.

Table I. SMART GREEN POWER NODE SYSTEM SPECIFICATIONS

Parameter	Value
Grounding Configuration	240 V to ground
Maximum load tested	**2 kVA**
Transformer turns ratio	**1:4**
Primary side DC voltage (RMS) input	**95 V**
Secondary side DC voltage (RMS) input	**380 V**
AC voltage (RMS) output	240 +/ 1.2 V_{AC}
Inverter frequency output	60 +/ 0.3 Hz
AC current (RMS) output	8.34 A
System efficiency	> 95%
Voltage output THD+N	< 5%
Current output THD+N	< 5%

3. DUAL ACTIVE BRIDGE CONVERTER

3.1 Topology

The dual active bridge is a bidirectional, controllable, dc-dc converter that has high power capabilities comprised of eight semiconductor devices, a high frequency transformer, energy transfer inductor, and dc-link capacitors. The converter can be more simply described as a more common full-bridge with a controllable rectifier. Due to the symmetry of this converter, with identical primary and secondary bridges, it is capable of bidirectional power flow control, and the reason why it is selected for the smart green power node application.

The topology is shown in Fig. 2, where V_{in} and V_{out} are the dc-link voltages, L_k is the leakage inductance of the transformer plus any necessary external energy transfer inductance, and S_{1-8} are the controllable semiconductor switches. The dual active bridge has been studied extensively previously in similar applications [1],[2],[3]. In previous years, in order to accommodate high dc-link voltages (>300V), insulated gate bipolar transistors (IGBTs) have been commonplace [3]. As such, S_{1-8} switching cells have been traditionally implemented with anti-parallel diodes and snubber capacitors in order to direct current commutation on switching events and to allow for zero voltage switching (ZVS) through the snubber capacitor and energy transfer inductance resonance. The motivation for developing high voltage MOSFETs is because these devices host an intrinsic body diode and drain-to-source output capacitance, which take the place of these external components and reduces the part count of the converter. Wide bandgap materials, such as silicon carbide (SiC), have been topics of research in the areas of power electronics because of their higher voltage and thermal ratings, as well as their lower turn on energy, making them ideal for high frequency switching converter applications.

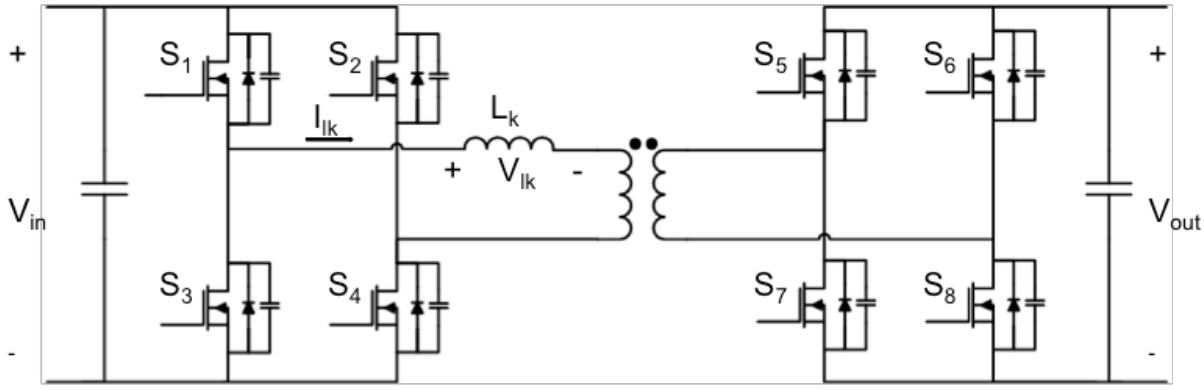

FIGURE 2: DUAL ACTIVE BRIDGE TOPOLOGY

3.2 Power Flow Analysis

Each full-bridge consists of two totem-poled switching devices, which are driven with complimentary square-wave pulses. The switching frequency of these complimentary devices is referred to as the switching frequency of the converter (f_s). In this application, in order to reduce the size of passive components and to leverage SiC's superior physical properties, high frequency switching will be employed. At high frequencies, the isolation transformer's magnetizing inductance becomes negligible and the transformer can be modeled only by its leakage inductance. Fig. 3 reflects an equivalent system, which will be used to derive the power equation for the converter. The two full bridges invert both dc bus voltages, represented as square waves V_{pri} and V_{sec}, and apply them to the terminals of the high frequency transformer (HF-XFMR).

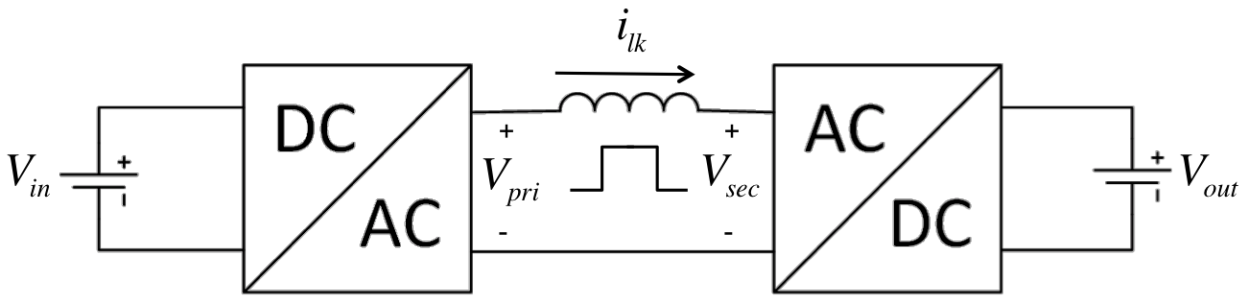

FIGURE 3: HIGH FREQUENCY EQUIVALENT DUAL ACTIVE BRIDGE

Power flow in the dual active bridge can be directed by phase-shifting the pulses of one bridge with respect to the other. This form of control, called phase shift modulation (PSM), directs power between the two dc busses such that the leading bridge delivers power to the lagging bridge [4]. This concept is illustrated in Fig. 4 in which the applied square waves create a voltage differential across the leakage inductance and direct its stored energy.

Considering the control pulses for switches $S_{1,4}$ of the primary bridge and $S_{5,8}$ of the secondary bridge, shifting the secondary bridge pulses by $+\delta$ instantiates power delivery from the

primary bridge to the secondary bridge. Similarly, shifting the secondary bridge by $-\delta$, making it the leading bridge, causes power to be delivered to the primary bridge.

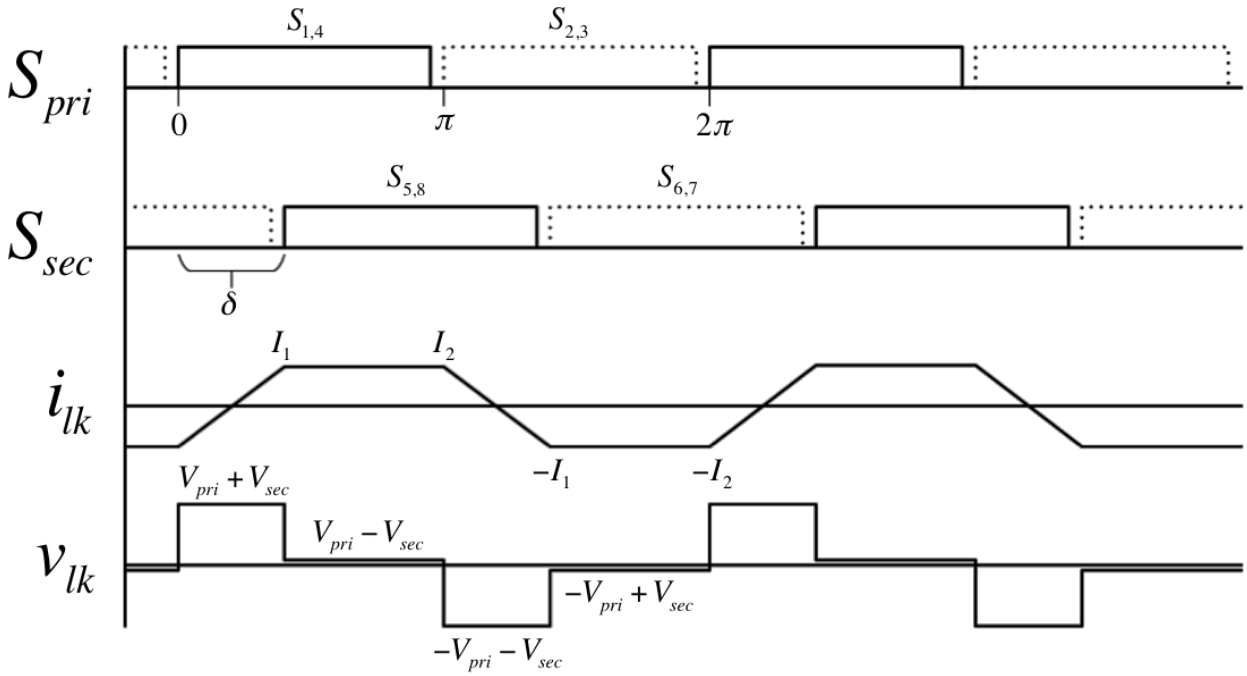

FIGURE 4: DUAL ACTIVE BRIDGE WAVEFORMS

The symmetry of the current waveform i_{lk} through the leakage inductance allows for the following power flow analysis to be developed using a half switching period. The inductor current waveform can be expressed as:

$$\frac{di_{lk}(t)}{dt} = \frac{V_{pri}(t) - V_{sec}(t)}{L_k} \tag{1}$$

Each half cycle can be divided into two intervals: Interval 1 occurs between $(0 < \theta < \delta)$ and interval 2 is defined as $(\delta < \theta < \pi)$. Considering the depiction of the current waveform in Fig. (4), solving for (1) gives the following expressions during the two time durations.

$$V_{in} + \frac{V_{out}}{n} = L_k \frac{I_1 + I_2}{dT}, \quad \text{for } 0 < t < dT \tag{2}$$

During interval 2, the inductor current is:

$$V_{in} - \frac{V_{out}}{n} = L_k \frac{I_1 + I_2}{(1-d)T}, \quad \text{for } dT < t < T \tag{3}$$

With n being the turns ratio of the transformer, T being the duration of a half-cycle of the period, I_1 and I_2 being the inductor current during switching instances, and d being the phase shift duty percentage of the two bridges, which will be referred to as the duty cycle of the converter.

Averaging (2) and (3), as shown in [5], yields an expression for the average output current of the converter:

$$I_{out} = \frac{(1 - |d|)dTV_{in}}{nL_k} \tag{4}$$

From this the average output power can be derived:

$$P = V_{out}I_{out} = \frac{(1 - |d|)dTV_{in}V_{out}}{nL_k} \tag{5}$$

This expression shows a relationship between the power delivered to the output as a function of the duty cycle (phase shift) between the two bridges, the switching frequency of the converter, and the energy transfer inductance. Additionally, (5) also indicates that a negative duty cycle (or phase shift) between bridges will cause power to be drawn from the output and delivered to the input dc bus. Fig. 5 shows the power transfer per unit vs. the duty cycle of the two bridges. These parameters must be balanced in order to design a functioning converter to suite a particular application's needs.

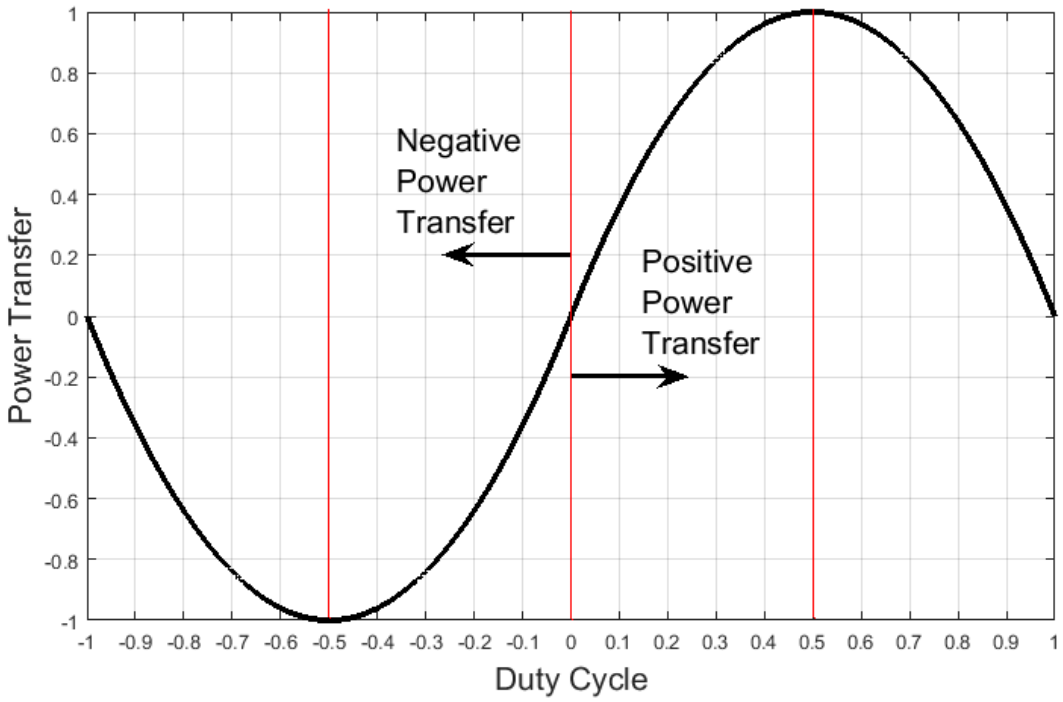

FIGURE 5: DUAL ACTIVE BRIDGE POWER TRANSFER CHARACTERISTIC

3.3 Preliminary Design Considerations

For the SGPN application, reliability across a wide power range must be met. To do so, several major converter components must be selected to withstand maximum anticipated current and voltage stresses and to facilitate desired power flow control. The critical components of the dual active bridge are the HF-XFMR, external energy transfer inductor, MOSFETs, and dc-link capacitors. Additionally, all design criteria will be met operating at switching frequencies greater than 100 kHz. It will be shown in the design process that 250 kHz operation is not only feasible, but is also necessary in order to achieve optimal system size reduction while meeting converter efficiency requirements. The following analysis will outline key system parameters that will be used for component selection.

3.4 Inductor Sizing

As a reactive component, inductor sizes are dependent on frequency. From (5) it is shown that with fixed dc bus voltages, varying either the switching frequency or energy transfer inductance will alter the power handling capabilities of the converter. Along with the switching frequency, the maximum desired power must be placed at an optimal duty cycle. [6] and [7] explore the design of high frequency dual active bridge and the optimal placement of the maximum power on the power transfer curve. Generally, maximum power of the dual active bridge should be placed between 30% and 40% duty cycle because it remains mostly linear in this region, which makes future current controller development much easier. Additionally, by designing for extra headroom at the top of the curve gives the converter extra current delivery capabilities, which will be needed to respond to load steps.

An optimal inductor value is selected by solving (5) for the energy transfer inductance and sweeping key system parameters, such as the switching frequency f_s and maximum power duty cycle d. The expression for the energy transfer inductance is:

$$L_k = \frac{(1 - |d|)dV_{in}V_{out}}{2f_s n P_{max}} \tag{6}$$

Note that the half cycle period T has been expressed in terms of the switching frequency of the converter to provide context for future discussion and graphical illustration. Fig. 6 shows the energy transfer inductance across varying switching frequencies with the maximum power placed at different duty cycles. As can be seen, increasing the switching frequency drastically reduces the size of the total inductance need to facilitate maximum power transfer. Similarly, the duty cycle affects the inductance value, but becomes less noticeable at higher frequencies. Due to diminishing returns of reduced inductor size at frequencies greater than 250 kHz, this switching frequency and a duty cycle of 35% are selected for this converter design.

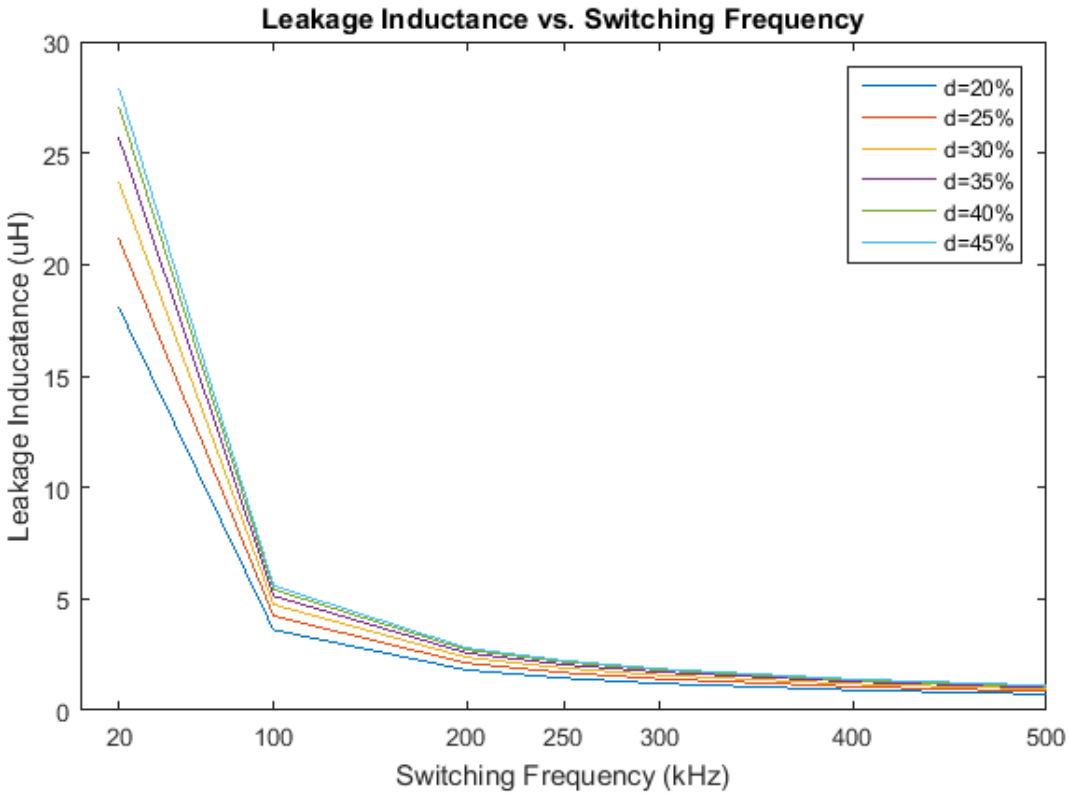

FIGURE 6: INDUCTOR SIZING

3.5 Switching Devices

A key component of the dual active bridge is the switching devices themselves. As shown in Section 3.4, operation at higher switching frequencies greatly reduce the size of the energy transfer inductor. In order to operate at such high switching frequencies with minimal switching losses, SiC MOSFETs must be employed. The SiC material and the process used to manufacture devices from it yield devices with high band gap energy, high thermal conductivity, and high critical electric field. These intrinsic device properties make them ideal for high voltage, high frequency converter applications [7]. Primarily, the relatively low turn on energy of the device gate and the lower output capacitance are what allows for these SiC devices to be switched at high speeds (>50 kHz) while remaining power efficient. Additionally, their superior thermal conductivity and small die size make them ideal for extreme environment and highly dense power converter applications, of which the dual active bridge for the SGPN must meet high power density standards.

3.6 Gate Driver

SiC gate driver design presents many unique considerations due to the high transconductance of the devices. As opposed to Si insulated gate bipolar transistor (IGBT) devices, SiC MOSFETs require tight gate regulation to keep the device in the saturation region [9]. This is made even more difficult to achieve if one is to implement these devices in high frequency switching circuits, in which parasitic inductances cause excessive ringing in the gate drive loop. Because of SiC MOSFET's larger transconductance, the defining line between the triode and saturation region is blurred, making it act more as a voltage-controlled resistance than a voltage-controlled current source. Fig. 7 depicts typical I-V curve transconductance characteristics of the SiC MOSFET and the Si IGBT. As can be seen, when the IGBT collector to emitter voltage reaches sufficiently large value, with different gate to emitter voltages, the device constricts current flow and behaves as a constant current source. Opposite of this, the SiC MOSFET never reaches a clear saturation point. This is directly due to its larger intrinsic transconductance, which makes its I-V characteristic more linear.

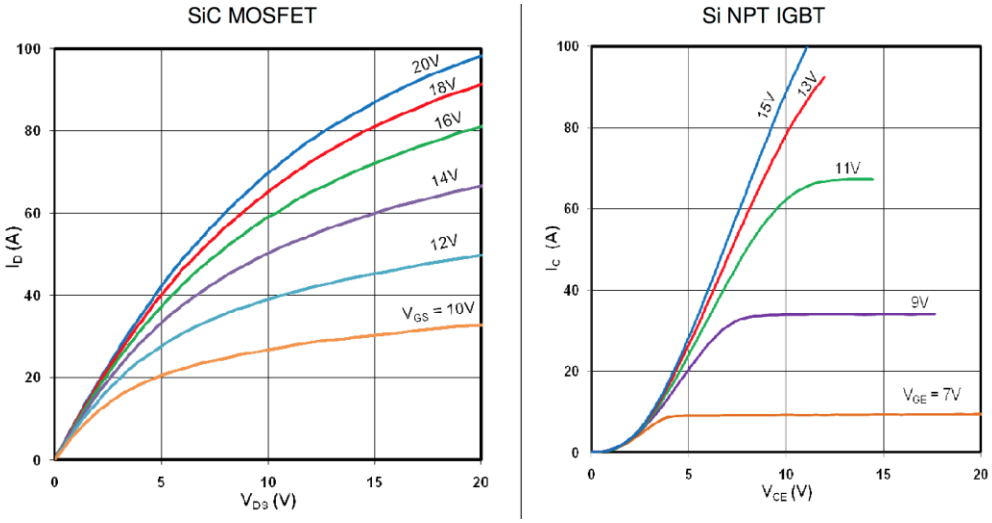

FIGURE 7: SIC MOSFET VS. SI IGBT I-V TRANSCONDUCTANCE CURVE (CREDIT: CREE [9])

Keeping this in mind, when high frequency operation is desired, SiC MOSFET gate drivers must be capable of large peak drive currents in order to push the device past the Miller plateau. Additionally, the gate driver must be capable of providing both a positive turn-on voltage and negative turn-off voltage (typically +20V/-5V for Cree's standard line of SiC MOSFETs) [10]. Finally, the gate driver must be placed as close to the device as possible in order to minimize trace inductance and excessive ringing in the circuit. These are all key in ensuring the SiC devices can be turned on and off at will with no issues.

3.7 Transformer Design

After the inductor has been sized and the converter power rating has been selected, the HF-XFMR must be designed to withstand current voltage stresses. Referring back to Fig. 4, which depicts typical DAB waveforms, the peak currents I_1 and I_2 through the transformer occur at the switching instances of each bridge. Rearranging (2) and (3):

$$I_1 = \frac{T}{2L_k}\left(2\frac{V_{out}}{n}d + V_{in} - \frac{V_{out}}{n}\right) \tag{7}$$

$$I_2 = \frac{T}{2L_k}\left(2V_{in}d - V_{in} + \frac{V_{out}}{n}\right) \tag{8}$$

In the case where the primary reflected output voltage is equal to the input voltage, (7) and (8) can be further simplified to:

$$I_1 = \frac{T}{2L_k}\left(2\frac{V_{out}}{n}d\right) \tag{9}$$

$$I_2 = \frac{T}{2L_k}(2V_{in}d) \tag{10}$$

$$\therefore I_1 = I_2 \tag{11}$$

If a zero-error controller in used, and the turns ratio of the transformer satisfies the input to output voltage conversion ratio, then this assumption is valid. Using (4), (5), (9), and (10), a compilation of the dual active bridge's power flow parameters can be calculated. Results for the current design are show in the following table. Recall that maximum power transfer of 2kW was designed to occur at a duty cycle of 35%, which is shown in red.

Table II. DUAL ACTIVE BRIDGE SYSTEM

Duty Cycle / Phase Shift	Input Current (A)	Output Current (A)	Primary Peak Current (A)	Secondary Peak Current (A)	Output Power (W)
0.05	4.40	1.10	4.63	1.16	417.58
0.10	8.33	2.08	9.25	2.31	791.20
0.15	11.80	2.95	13.88	3.47	1120.87
0.20	14.81	3.70	18.51	4.63	1406.58
0.25	17.35	4.34	23.13	5.78	1648.34
0.30	19.43	4.86	27.76	6.94	1846.14
0.35	21.05	5.26	32.39	8.10	1999.99
0.40	22.21	5.55	37.02	9.25	2109.88
0.45	22.90	5.73	41.64	10.41	2175.81
0.50	23.13	5.78	46.27	11.57	2197.79

The analysis indicates that the HF-XFMR must be capable of handling approximately 48A/12A peak primary and secondary currents, as well as being rated for at least 2.2 kW. The design of the transformer will not be covered in this work and a functioning transformer was ordered from Payton Group Magnetics. The transformer's specifications are included in Appendix A.

3.8 Zero Voltage Switching Operation

The principle of zero voltage switching (ZVS), also called soft-switching, is based upon the resonant relationship between the snubber capacitance across each device and the equivalent inductance of the circuit during different switching intervals. Essentially, during switching events, the current through one of the complimentary devices is interrupted, but due to the energy transfer inductance, current is supplied through the snubber capacitor and forced through the anti-parallel diode of the device. This is referred to as current commutation and is a fundamental component of many power electronic converters. A simple resonance relationship between the snubber capacitance and the circuit inductance is

$$f_r = \frac{1}{2\pi\sqrt{L_k C_S}} \tag{12}$$

where f_r is the resonant frequency and C_s is the snubber capacitance. The instantaneous current flow through the capacitance is given by:

$$I_{CS} = C_S \frac{dV_{CS}}{dt} \tag{13}$$

Because the equivalent capacitance seen by the inductor during switching intervals is double that of a single snubber capacitor due to the complimentary transistor pair, the total inductor current can be written as:

$$I_{Lk} = 2I_{CS} = 2C_S \frac{dV_{CS}}{dt} \tag{14}$$

Thus, the amount of energy stored in the inductor must be equal to or greater than, the total energy required to fully charge/discharge the snubber capacitors in order to realize ZVS operation.

Considering this, it is clear that the inductor current during transition periods must be both greater than zero and capable of transferring/drawing enough energy to adequately charge and

discharge the equivalent capacitances in the devices. In ideal cases, this is guaranteed when the voltage transfer ratio (M) is equal to one [5], or in other words that the voltage conversion is entirely handled by the turns ratio of the transformer.

$$M = \frac{V_{out}}{nV_{in}} \tag{15}$$

Conveniently, the expressions (7) and (8) for peak currents through each switch can be rewritten in terms of the voltage conversion ratio, which will be used for determining the ZVS boundary of each device. In this work, the transformer will be designed such that this condition is met.

$$I_1 = \frac{TV_{in}}{2L_k}(2Md + 1 - M) \tag{16}$$

$$I_2 = \frac{TV_{in}}{2L_k}(2d - 1 + M) \tag{17}$$

However, not only must the inductor current at switching instances be greater than zero, but the energy stored in the inductor must be greater than or equal to the energy stored in the equivalent output capacitances of the devices such that:

$$E_{Lk} \geq E_{Cs} \rightarrow \frac{1}{2}L_k {i_{lk}}^2 \geq 4\left(\frac{1}{2}C_s {V_{CS}}^2\right) \tag{18}$$

$$i_{Lk} \geq 2V_{CS}\sqrt{\frac{C_s}{L_k}} \tag{19}$$

Then, writing each peak current in terms of this boundary:

$$I_1 = \frac{TV_{in}}{2L_k}(2Md + 1 - M) \geq 2V_{in}\sqrt{\frac{C_s}{L_k}} \tag{20}$$

$$I_2 = \frac{TV_{in}}{2L_k}(2d - 1 + M) \geq 2V_{out}\sqrt{\frac{C_s}{L_k}} \tag{21}$$

Finally, the ZVS boundary conditions for the input and output bridges are given as a function of the voltage conversion ratio, switching frequency, inductance, and snubber capacitance.

$$d \geq \frac{M-1}{2M} + \frac{2\sqrt{L_k C_{s,i}}}{TM} \tag{22}$$

$$d \geq \frac{1-M}{2} + \frac{2Mn\sqrt{L_k C_{s,o}}}{T} \tag{23}$$

In recent years, IGBT devices have been used to create high voltage switching converters, though they have a higher equivalent output capacitance and no intrinsic body diode. Therein lies the appeal of SiC MOSFETs as they exhibit a very low equivalent output capacitance, which removes the need for external snubber capacitance and simultaneously makes ZVS transition times shorter. The equivalent output capacitance of the devices (C_{eq}) is nonlinear in nature and should be found in the devices' data sheet at the corresponding rated voltage. Additionally, SiC MOSFETs have an intrinsic body diode, which may act in place of the external anti-parallel diode. These characteristics make high frequency switching more feasible and further converter size reduction possible.

3.9 Loss Analysis

The losses of the dual active bridge are isolated in several categories: transformer/magnetic losses, switching losses, and conduction losses. The loss incurred in the transformer and inductor is not within the context of this work, but are explored extensively in several other papers [11], [12], and [13]. This leaves switching losses and conduction losses for consideration in this design work, both of which rely heavily on the selection and utilization of the semiconductor devices in the converter. As stated in section 3.8, by selecting SiC MOSFETs as the key-switching component of the high voltage bridge, and by designing the transformer turns ratio to facilitate the voltage conversion, the switching losses can be ideally omitted.

Conduction losses are the simplest to understand and predict, as they are a function of the RMS current (I_{RMS}) through each bridge of the converter and the selected device's drain-to-source on resistance (R_{ds}). As such, the conduction losses can be calculated by using Ohm's Law [14]. Using (9) and (10) to find the peak bridge currents, the RMS current through each device can be calculated beginning with the peak current.

$$I_{SPeak,LV} = \frac{T}{2L_k}\left(2\frac{V_{out}}{n}d\right) \tag{24}$$

Then, the RMS current of the primary side current can be found, followed by the losses per device.

$$I_{SRMS,LV} = \frac{I_{SPeak,LV}}{\sqrt{2}} \tag{25}$$

$$P_{cond,sw} = R_{ds}I_{SRMS,LV}^2 \tag{26}$$

More precisely, because there are four devices per bridge that conduct the RMS current per half switching cycle:

$$P_{cond,bridge} = 4P_{cond,sw} = 4R_{ds}I_{SRMS,LV}^2 \tag{27}$$

4. CONTROL & FEEDBACK

4.1 Phase Shift Control

A variety of control schemes for the dual active bridge have been studied. Most common of these is the phase shift modulation (PSM) method, which directs power flow by shifting the leading edges of each complimentary pair of devices, both high- and low-side switches. Single phase shift modulation (SPSM) is the most simple to implement and follows exactly the power flow derivation described in section 3.2. Refer to Fig. 4 again for an illustration of this method. Other methods, such as dual phase shift modulation, hybrid phase shift modulation, and triple phase shift modulation have been studied and compared [15] and [16]. These variations on the PSM method offer many benefits, but their controller design and implementation are much more sophisticated. This work will utilize the SPSM method, with measurement and control signal flow provisions made for future control method comparisons.

4.2 Converter Modeling

Modeling the dynamics of the dual active bridge have been the topic of recent research [17], through which accurate converter transfer functions are derived. A model developed around the Fourier expansion of the switching functions is of particular interest because of its demonstrated ability to accurately model the dual active bridge across a wide range of power delivery. Developed in [17], this converter model begins with defining the input and output voltages as functions of the switch states and the primary and secondary voltages.

$$V_{pri} = V_{in}\{S_1 - S_2\} \tag{28}$$

$$V_{sec} = V_{out}\{S_5 - S_6\} \tag{29}$$

A full model cannot be developed without a current based expression for the output voltage. Therefore, KCL analysis of the output node of the converter must be completed, wherein the current injected by the output bridge (i_{dc}) and the output capacitor (i_c) comprise the elements of the load current (i_{out}).

$$i_c = i_{dc} - i_{out} \tag{30}$$

Table III. SWITCHING
STATES OF OUTPUT BRIDGE

S_5	S_6	i_{dc}
0	0	0
0	1	$-i_{lk}$
1	0	i_{lk}
1	1	0

From (22) and Table III, the time domain expression for (19) can be obtained.

$$i_{dc} = i_{lk}\{S_5 - S_6\} \tag{31}$$

Now, to put combine these systems of equations, a closed KVL loop must be defined for the inner loop comprised of the inductor current, load, and respective bridge voltages.

$$V_{pri} - \frac{N_p}{N_s}V_{sec} - R_L i_{lk} - L_k \frac{di_{lk}}{dt} = 0 \tag{32}$$

Now, substituting (28) and (29) into (32), a final expression of the voltage characteristic as a function of the selected energy transfer inductance and switching states is complete.

$$R_L i_{lk} + L_k \frac{di_{lk}}{dt} = V_{in}\{S_1 - S_2\} - \frac{N_p}{N_s}V_{out}\{S_5 - S_6\} \tag{33}$$

The switching functions S_1, S_2, S_5, and S_6 may be expanded using the Fourier transform in order to convert them to time-domain expressions. Being that they are all square waveforms, their Fourier series expansion can be expressed as:

$$S_k = \frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{N} \frac{\sin([2n+1]\{\omega_s - \alpha_k\})}{[2n+1]}, N \geq 0, k = 1,2,3 \ldots \tag{34}$$

where N is the number of considered decomposed harmonics of the switching functions. The series summation of these harmonics yields a representation of the original square waveform, where the higher number of harmonics included yields increasingly better representations of the original switching waveform.

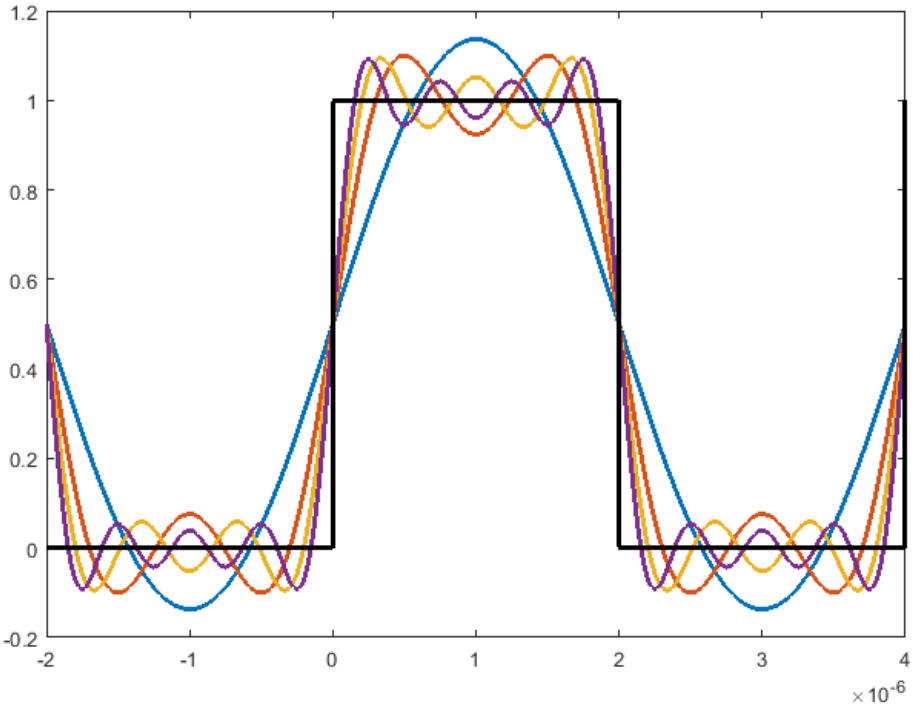

FIGURE 6: FOURIER EXPANSION OF SWITCHING WAVEFORM

Applying this expression of the switching function to MOSFETs of importance yields the following:

$$S_1 = \frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{N}\left[\frac{\sin([2n+1]\{\omega_s t\})}{[2n+1]}\right], N \geq 0, k = 1,2,3 \ldots \quad (35.a)$$

$$S_2 = \frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{N}\left[\frac{\sin([2n+1]\{\omega_s - \pi\})}{[2n+1]}\right], N \geq 0, k = 1,2,3 \ldots \quad (35.b)$$

$$S_5 = \frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{N}\left[\frac{\sin([2n+1]\{\omega_s - \delta\})}{[2n+1]}\right], N \geq 0, k = 1,2,3 \ldots \quad (35.c)$$

$$S_6 = \frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{N}\left[\frac{\sin([2n+1]\{\omega_s - \delta - \pi\})}{[2n+1]}\right], N \geq 0, k = 1,2,3 \ldots \quad (35.d)$$

The foundational analysis outlined above is applied in [17] to define a standard expression of the transfer function. Recombining equations and rearranging obtain the following nonlinear model:

$$\frac{dV_{out}}{dt} = f(V_{out}, \delta) = -i_{load} + \frac{8}{C_{out}\pi^2}\frac{N_p}{N_s}\sum_{n=0}^{N}\left[\frac{1}{[2n+1]^2} \times \left\{\frac{V_{in}}{|Z[n]|}\cos([2n+1]\delta - \varphi_z[n]) - \frac{N_p}{N_s}\frac{V_{out}}{|Z[n]|}\cos(\varphi_z[n])\right\}\right] \quad (36)$$

Where $Z[n] = \sqrt{{R_L}^2 + (2\pi f_s[2n+1]L_k)}$ and $\varphi_z[n] = \tan^{-1}\left(\frac{2\pi f_s[2n+1]L_k}{R_L}\right)$. A standard linearization technique based on the small-signal analysis is then applied to derive a linearized model.

$$\frac{d(V_{out} + \Delta V_{out})}{dt} \approx f(V_{out0}, \delta_0, i_{load0}) + \frac{\partial f}{\partial V_{out}}\bigg|_0 \Delta V_{out} + \frac{\partial f}{\partial i_{load}}\bigg|_0 \Delta i_{load} + \frac{\partial f}{\partial \delta}\bigg|_0 \Delta\delta \quad (37)$$

Finally, combining like terms and putting into the standard 1st order format, the fully linearized expression for the rate of change in the output voltage is:

$$\frac{d\Delta V_{out}}{dt} = A\Delta V_{out} + B_\delta \Delta\delta + B_I \Delta i_{load} \quad (38.a)$$

$$A = \frac{-8}{C_{out}\pi^2}\left(\frac{N_p}{N_s}\right)^2 \sum_{n=0}^{N}\frac{\cos(\varphi_z[n])}{[2n+1]^2|Z[n]|} \quad (38.b)$$

$$B_\delta = \frac{-8}{C_{out}\pi^2}\frac{N_p}{N_s}\sum_{n=0}^{N}\left[\frac{\sin(\varphi_z[n] - [2n+1]\delta_0)}{[2n+1]|Z[n]|}\right] \quad (38.c)$$

$$B_I = -\frac{1}{C_{out}} \quad (38.d)$$

4.3 Controller Design

Switching converter control methods range in capabilities and sophistication. Of these, the most common are those that monitor and regulate a single input/output or variable via a negative feedback loop, and are referred to as single-input single-output (SISO) systems. In the case of the dual active bridge feeding a grid-tied inverter, the output voltage must be regulated in order to ensure compatibility with other electronic devices, downstream dc loads, and to avoid backward power flow through the converter when it is undesired. Additionally, because of the symmetry of the converter and its bidirectional power flow capabilities, a control system may be developed for one side of the converter and simply mirrored to the other side when the power flow direction is reversed during battery charging intervals.

The standard feedback control loop of a power converter is shown in Fig. 9, where $G(s)$ is the plant function, or converter model, $C(s)$ is the controller, V_{out} is the measured output voltage, and V_{ref} is a reference signal that commands the controller to track. In this case, the output voltage is the controlled system variable. In the closed loop form, the output is sampled and compared to the reference signal, which generates an error signal. The controller function forcibly applies control signals to the plant function and is often times designed to eliminate the error between the sampled output and reference input, effectively realizing zero steady-state error.

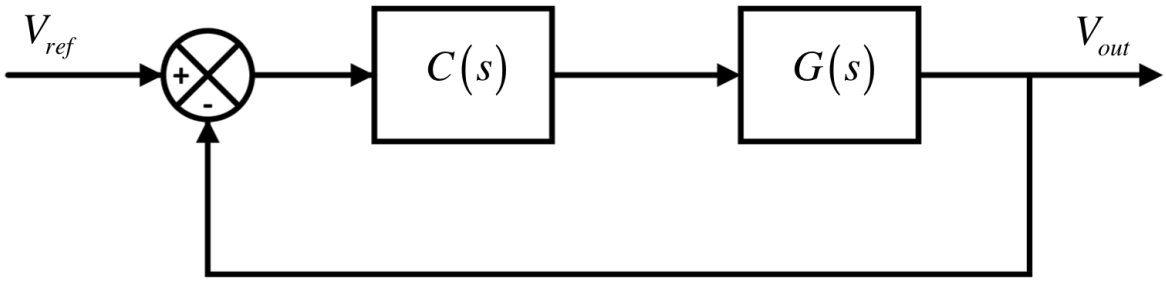

FIGURE 7: CLOSED LOOP FEEDBACK CONTROLLER

From the system model developed in section 4.2, a plant function can be obtained. This is accomplished by deriving the s-domain expression using the Laplace transform. Initially, the load current disturbance will be ignored. This will greatly simplify the design of a steady-state tracking controller. Applying the Laplace transform to (38) and rearranging gives:

$$G(s) = \frac{B_\delta}{s - A} \tag{39}$$

Since the plant function is 1st order, a proportional-integral (PI) controller would be an ideal controller to implement, as it produces zero steady-state tracking error [18] and [19]. The transfer function of the PI controller is:

$$G(s) = K_p + \frac{K_i}{s} \tag{40}$$

where K_p is the proportional term gain and K_i is the integral term gain.

Now, with the plant and controller transfer functions defined, the final input-to-output characteristic can be written as:

$$F(s) = C(s)G(s) = \left(K_p + \frac{K_i}{s}\right)\left(\frac{B_\delta}{s - A}\right) \tag{41}$$

4.4 Digital Controller

Modern power converter control systems are implemented using digital signal processors (DSP). This poses a challenge for controller design, as a continuous time controller, such as the PI controller explained in section 4.3, cannot be implemented in this format. They must be converted to a discrete-time representation of their continuous-time counterparts in order to be implemented in DSP controllers.

Though the conversion of continuous-time controllers into discrete-time controllers produces a mathematical expression that is considerably different, it is still possible to construct the controller using the continuous-time variables such as the PI controller gains K_p and K_i. This makes it possible to design the controller using continuous time models. However, at least one new controller variable must be introduced in order to accurately model the continuous-time expression, and that is the sampling delay time T_s. The sampling time variable first appears when the continuous-time controller function is transformed into the discrete domain by way of the Z-transform. For illustration purposes, the following conversion will be performed on the proportional-integral-derivative (PID) controller transfer function and later boiled down to the PI controller from [20].

$$PID(s) = K_p + \frac{K_i}{s} + K_d s \leftrightarrow PID(z) = K_p + \frac{K_i T_s z}{z-1} + \frac{K_d N(z-1)}{(1+NT_s)z-1} \tag{42}$$

Though (38) is now in a discrete format, it still needs to be reduced to a difference equation so that it may be implemented in the DSP source code. Difference equation formats (43) are a version of discrete-time system representation that is constructed solely from the summation of gain-weighted sampled measurements. In this format, $x(k)$ is the output control variable, which is the sum of gain-weighted past values of itself and another sampled measurement $y(k)$.

$$x(k) = \sum_{n=1}^{N} A_k x[k-n] + B_0 y[k] + \sum_{n=1}^{N} B_k y[k-n] \tag{43}$$

The controller's transfer function is essentially an error-to-control variable function, so translation of the discrete-time controller to its respective difference equation will begin with this observation. First, (42) is rewritten into a standard form (44).

$$PID(z) = \frac{\delta(z)}{e(z)} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \tag{44.a}$$

$$b_0 = K_p(1 + NT_s) + K_i T_s(1 + NT_s) + K_D N \tag{44.b}$$

$$b_1 = -\left(K_p(2 + NT_s) + K_i T_s + 2K_d N\right) \tag{44.c}$$

$$b_2 = K_p + K_d N \tag{44.d}$$

$$a_0 = (1 + NT_s) \tag{44.e}$$

$$a_1 = -(2 + NT_s) \tag{44.f}$$

$$a_2 = 1 \tag{44.g}$$

Which can then be expressed in its difference equation form:

$$\delta[k] = \frac{-a_1}{a_0}\delta[k-1] - \frac{a_1}{a_0}\delta[k-2] + \frac{b_0}{a_0}e[k] + \frac{b_1}{a_0}e[k-1] + \frac{b_2}{a_0}e[k-2] \tag{45}$$

This form, as shown in (41), is simple to implement in the DSP source code, which controls the converter.

4.5 Load Disturbance Mitigation

In the case of switching converters, especially those operating at high frequencies, the response of the PID controller is slow with respect to the bandwidth of the converter. This makes the converter susceptible to load disturbances. Referring back to (34), the converter model explicitly demonstrates a direct relationship between changes in load current to the output voltage, such that load steps would cause a voltage sag or spike at the output of the converter. This may be handled in one of two ways: either the output capacitor must be made sufficiently large to supply the instantaneous current required to drive a load transition, or the controller must be equip to responded to load steps quickly.

As mentioned, the PID controller offers many benefits, namely it's zero steady-state tracking error, but can only be made to respond so fast while minimizing overshoot oscillations. This fact makes it alone unsuitable for responding to load disturbances. Instead, a feed-forward path may be added to the controller, which gives an instantaneous estimate of the control variable based on input and output samples. Solving (46), which is a rewrite of the power transfer equation in terms of the input voltage and output current, for the phase shift between the bridges is the best way to give this immediate response.

$$\frac{i_{load}}{V_{in}} = \frac{8}{\pi^2}\frac{N_p}{N_s}\sum_{n=0}^{N}\left(\frac{1}{[2n+1]^3}\frac{sin([2n+1]\delta)}{2\pi f_s L_k}\right) \tag{46}$$

However, due to the complexity of this equation, solving for the phase shift in real-time is impossible. Therefore, a lookup table must be used in order to provide the approximation, as shown in Fig. 10. When this approximation is summed with the output of the controller, it reduces the stress on the controller to compensate for load current disturbances.

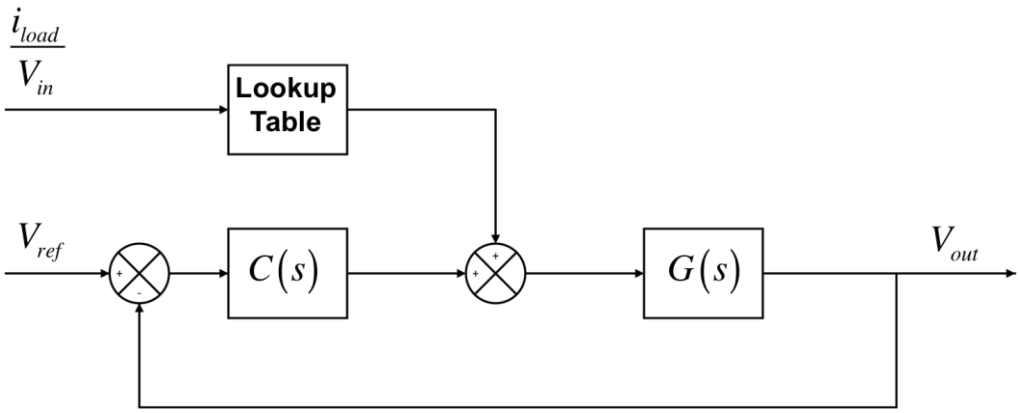

FIGURE 8: CONTROLLER WITH FEED-FORWARD PATH

5. CONVERTER DESIGN & PCB

5.1 Dual Active Bridge

Following the analysis outlined in chapter 3, and to meet the converter specifications in Table I, critical converter parameters/components may be selected. Referring to Fig. 6, it is shown that the primary reflected energy transfer inductance needed to facilitate a minimum 2 kW power capacity shrinks drastically in size at frequencies greater than 100 kHz. However, the inductance vs. frequency plot is logarithmic in nature and diminishing returns in size reduction are seen at frequencies greater than 250 kHz. Therefore, 250 kHz is tentatively selected as the converter switching frequency, keeping in mind that the design process is an iterative one. Furthermore, recognizing the importance of leaving the converter a fair amount of headroom so that the controller may respond to load disturbances, the optimal phase shift duty percentage is defined at 35%. According to Fig. 6, this would require a total energy transfer inductance less than 2.053 μH (primary reflected).

Selecting the switching devices is less straightforward, in that they require no mathematical analysis to select, but rather best judgment must be applied. Contributing factors to switching device include MOSFET's on resistance, peak voltage and current ratings, and the stresses they must withstand. Table II holds values for peak primary and secondary currents with the selected energy transfer inductor, which puts constraints on the both the current carrying capabilities of the selected devices and the on resistance that they must have in order to minimize losses. Naturally, the low voltage side of the converter conducts higher peak currents and will therefore exhibit higher conduction losses through each device. Unfortunately, available discrete packaged SiC MOSFETs do not have a low enough on resistance to conduct these high currents without sustaining losses that would greatly inhibit the efficiency of the converter. Therefore, a high power

Si MOSFET must be selected, taking care to select a device with the lowest possible turn-on energy and output capacitance so that it may closely match the performance of the SiC devices.

As a key component in the dual active bridge, the transformer must also be selected carefully. The design of the transformer is beyond the scope of this work, so its specifications must be determined for a professional manufacturer to produce. Again, referring to Table II, the peak primary and secondary currents are approximately 48 A and 12 A, respectively. Additionally, its equivalent primary leakage inductance must not be greater than 2.053 μH, or else the converter will not be able to operate at 2 kW power. It is also important that it have a turns ratio of 1:4 so that the voltage conversion ratio is equal to one and ZVS is easier to achieve.

Finally, a gate driver for the switching devices must be selected. The Texas Instruments UCC27531 is chosen based on its ability to source and sink gate current through two separate IC pins, which allows for separate tuning of turn-on and turn-off characteristics. Essentially, two separate gate resistances may be applied; one for turn-on and one for turn-off, allowing the gate driver to source/sink different peak currents for driving the device. This is desirable for the SiC MOSFETs because of their high transconductance, which makes their turn-off transition critical to ensuring that gate jitter does not occur.

Table IV. DUAL ACTIVE BRIDGE COMPONENTS AND PARAMETERS

Component/Parameter	Value/Part
HV Side MOSFET	Cree C3M0065090D SiC MOSFET
LV Side MOSFET	International Rectifier IRFP4668PBF Si MOSFET
Transformer	Payton Planar Transformers Model 58913
Energy Transfer Inductor (Secondary Reflected)	24.3 μH EC96 ER31/6/25 Ferrite Core
DC-link capacitors	Kemet C4AEJBW5300A3LJ 30 μF Film
Gate Driver IC	Texas Instruments UCC27531 2.5A/5A Gate Driver

The design of the dual active bridge and its performance across varying load conditions is verified through LTspice simulations.

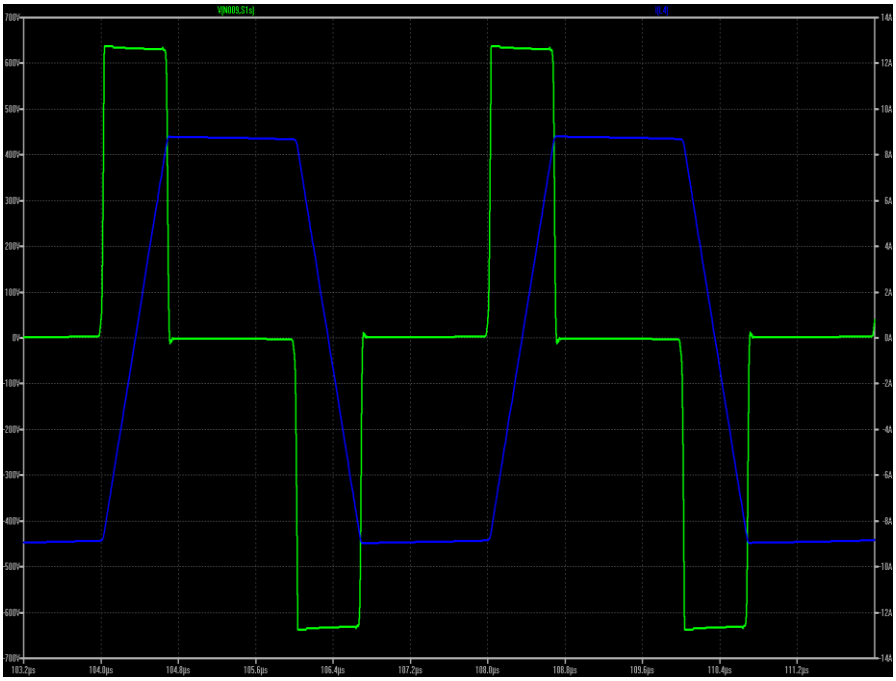

FIGURE 9: INDUCTOR CURRENT (BLUE) & VOLTAGE (GREEN): 2 KW LOAD, D= 0.35

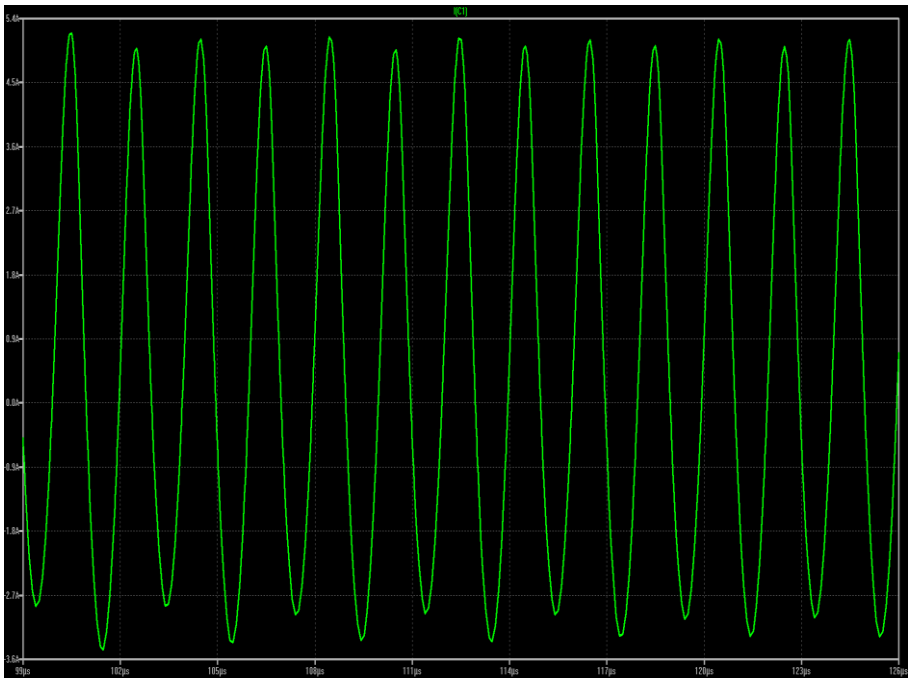

FIGURE 10: CAPACITOR CURRENT: 2 KW LOAD, D = 0.35

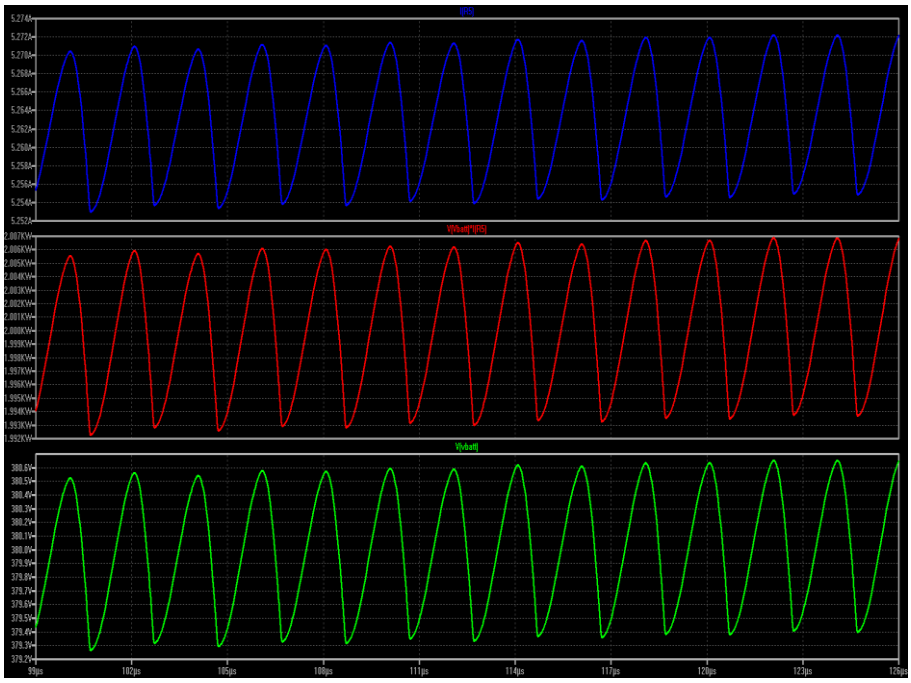

FIGURE 11: OUTPUT CURRENT (BLUE), POWER (RED), & VOLTAGE (GREEN): 2 KW LOAD, D = 0.35

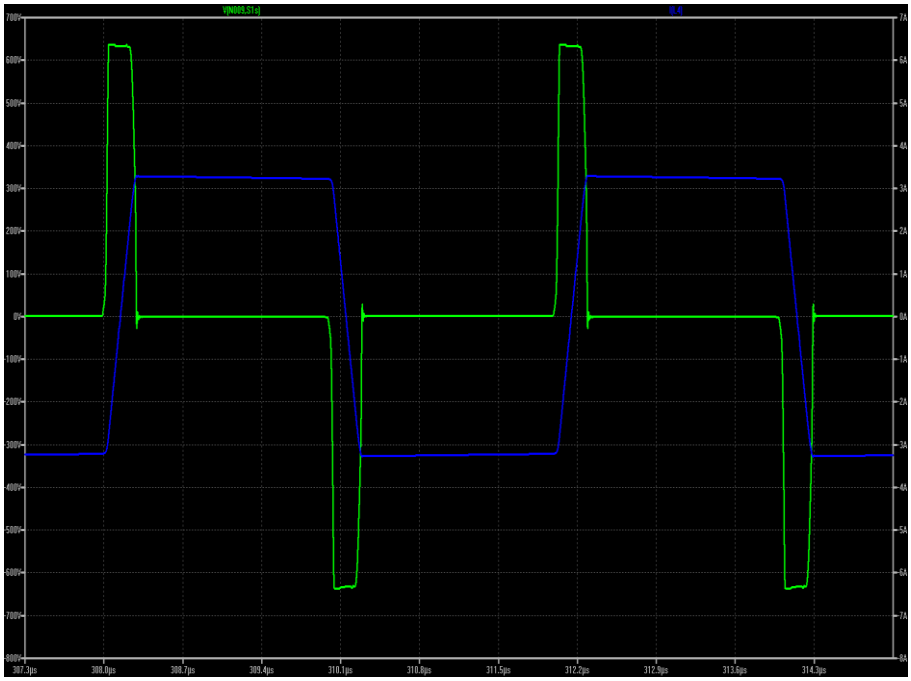

FIGURE 12: INDUCTOR CURRENT (BLUE) & VOLTAGE (GREEN): 1 KW LOAD, D =0.131

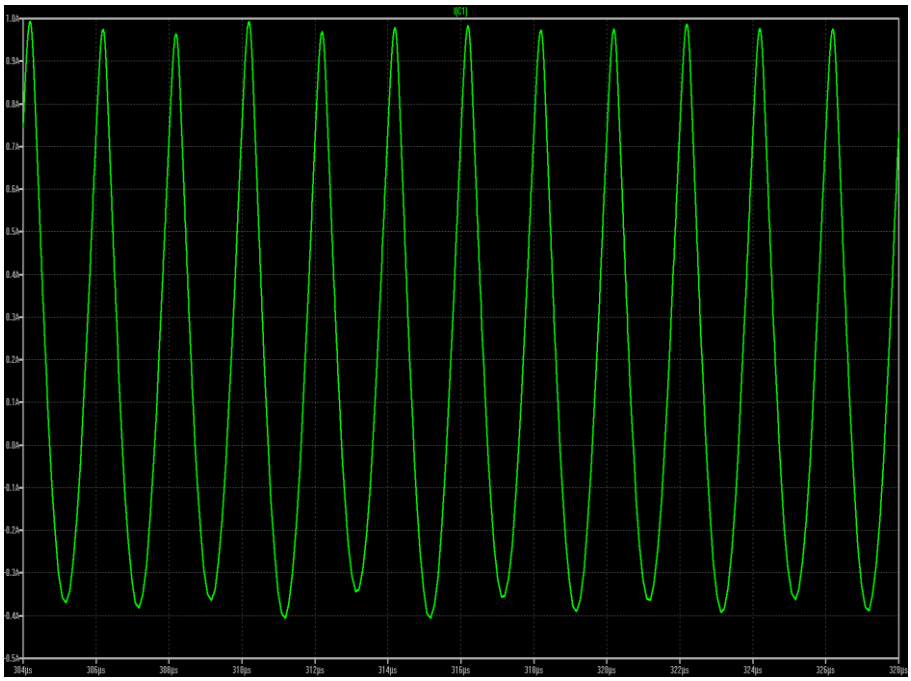

FIGURE 13: CAPACITOR CURRENT: 1 KW LOAD, D = 0.131

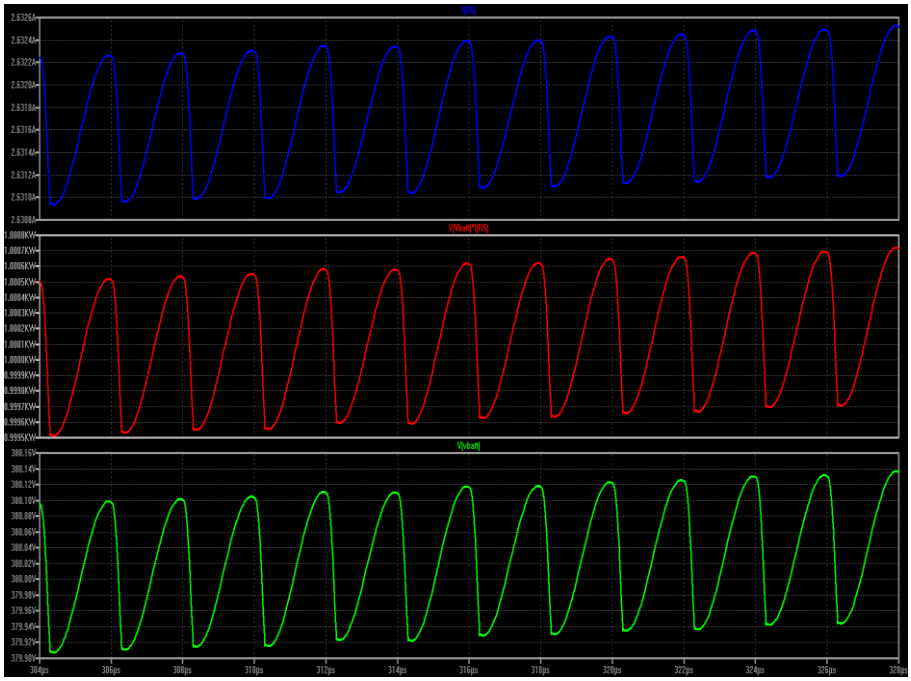

FIGURE 14: OUTPUT CURRENT (BLUE), POWER (RED), & VOLTAGE (GREEN): 1 KW LOAD, D = 0.131

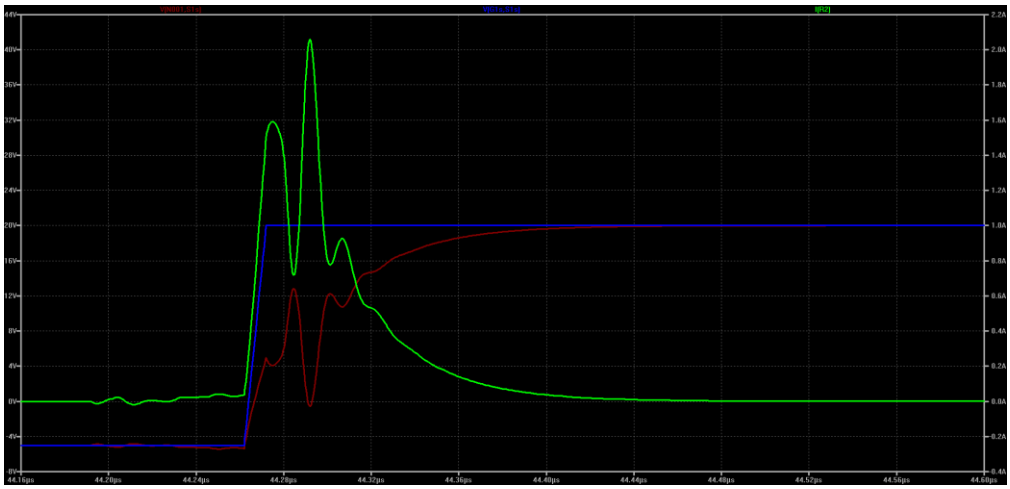

FIGURE 15: SIC MOSFET TURN-ON GATE CURRENT (GREEN), GATE-TO-SOURCE (RED), & DRIVE VOLTAGE (BLUE): $R_{G,ON}$ = 10 Ω

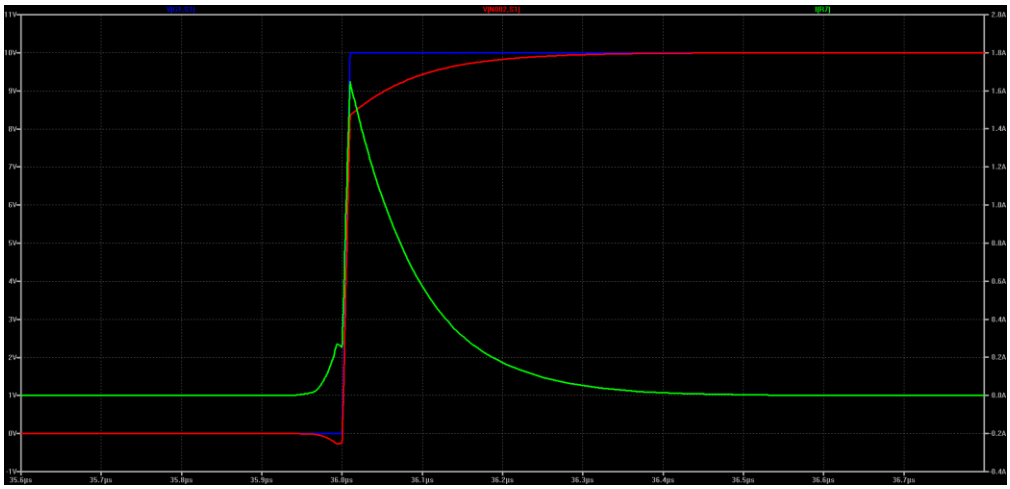

FIGURE 16: SI MOSFET TURN-ON GATE CURRENT (GREEN), GATE-TO-SOURCE (RED), & DRIVE VOLTAGE (BLUE): $R_{G,ON}$ = 5 Ω

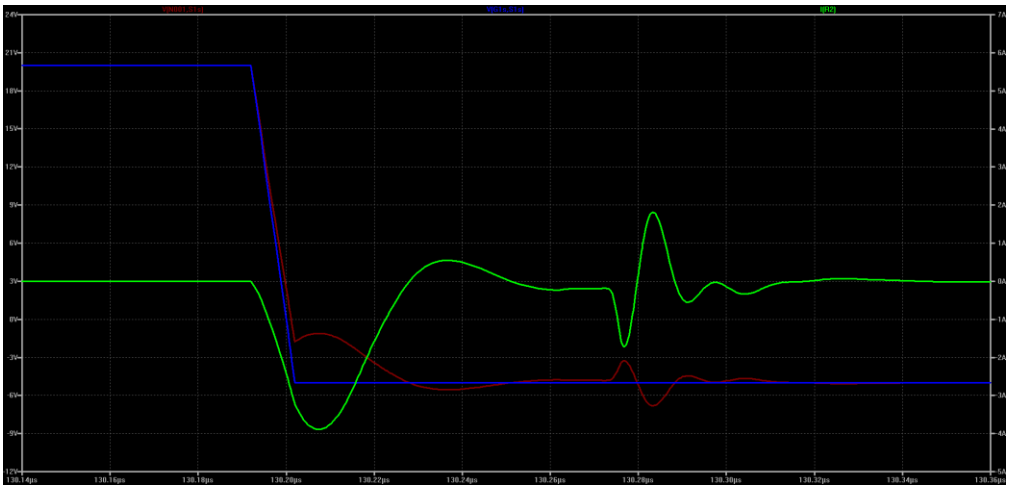

FIGURE 17: SIC MOSFET TURN-OFF GATE CURRENT (GREEN), GATE-TO-SOURCE (RED), & DRIVE VOLTAGE (BLUE): $R_{G,OFF}$ = 1 Ω

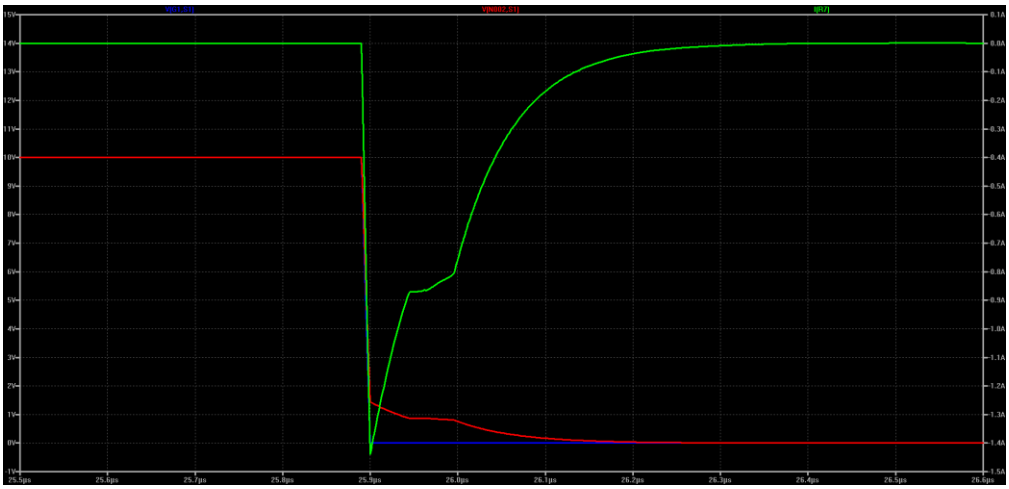

FIGURE 18: SI MOSFET TURN-OFF GATE CURRENT (GREEN), GATE-TO-SOURCE (RED), & DRIVE VOLTAGE (BLUE): $R_{G,OFF}$ = 5 Ω

Fig. 11-20 demonstrate the converter's steady-state operation under 1 kW and 2 kW loads with matched phase shift. In simulation, peak current and voltage values match those calculated from the analysis techniques developed in Chapter 3. The gate driver currents also do not eclipse the peak drive current capabilities of the TI UCC27531 device, thus verifying the design process.

5.2 Digital Controller

Using the component values listed in Table IV and applying the control scheme developed in Chapter 4, analysis of the converter operation in closed-loop may be completed. Matlab/Simulink is utilized to simulate the converter with its appropriate controller. Additionally, because the optimal selection of controller gains is beyond the scope of this work, the SISO tool in Matlab is employed to derive the desired controller gains. Beginning with only the PI controller, Fig. 21 depicts the converter simulation schematic under test with the digital PI controller. Fig. 22 shows the converter response upon start-up to a voltage reference of 380 V, while Fig. 23 shows the controller's calculated control variable. The results show that the converter reaches a steady-state voltage of 380 V within 50 ms and the control variable does not saturate.

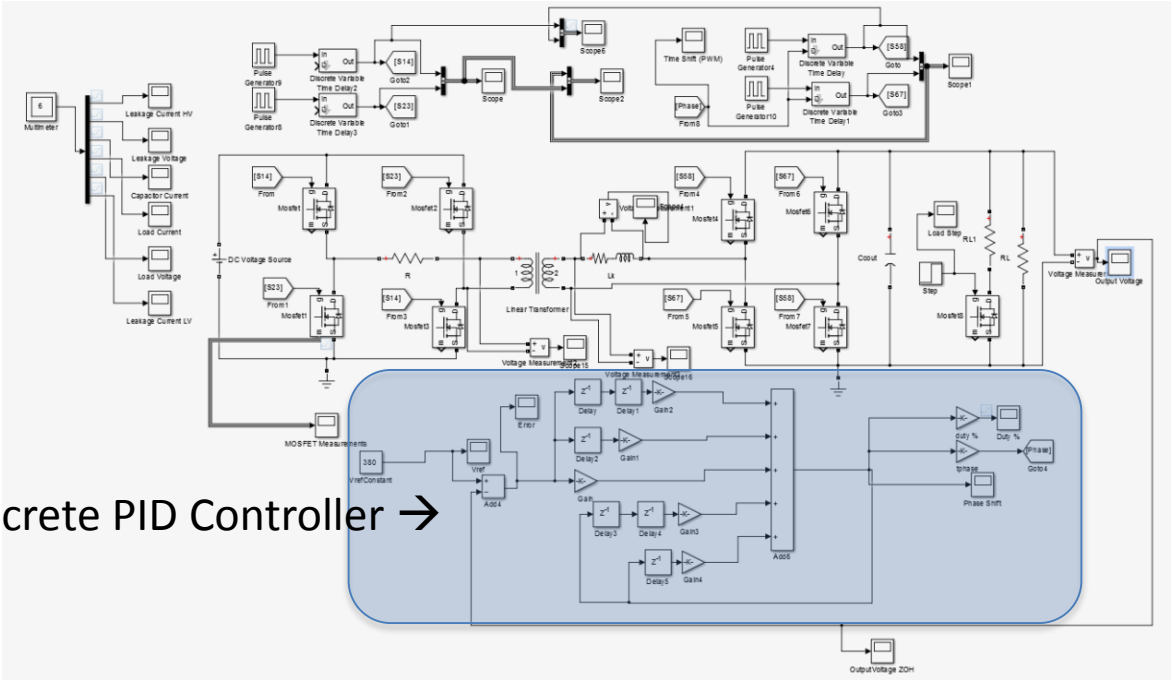

FIGURE 19: SIMULINK CONTROLLER SIMULATION: DIGITAL PI CONTROLLER

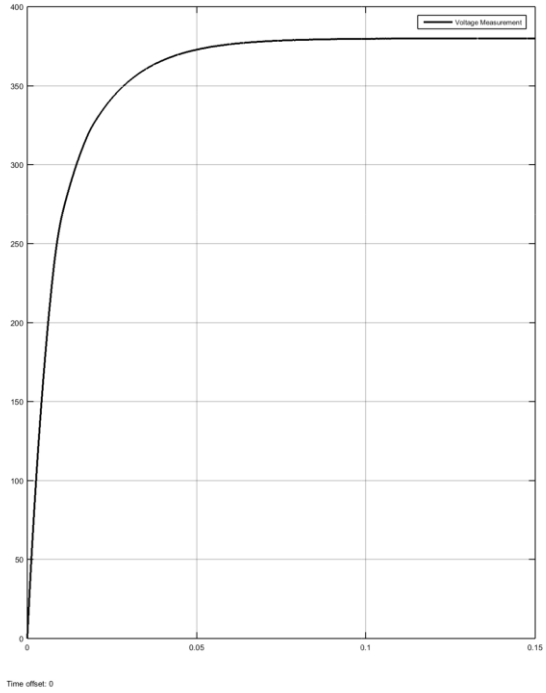

FIGURE 20: CONVERTER OUTPUT VOLTAGE RESPONSE: DIGITAL PI CONTROLLER

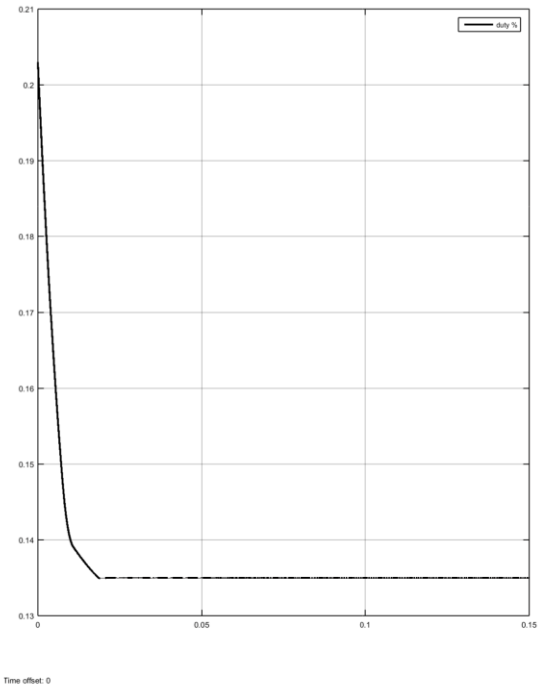

FIGURE 21: CONTROLLER RESPONSE: DIGITAL PI CONTROLLER

Next, the PI controller is tested against a load step (50%-100% and 100%-50% respectively). Fig. 24 shows the converter reaching steady state under the PI control at 1 kW load. When the load is stepped up from 1 kW to 2 kW (50%-100%), the voltage at the output sags 100V for 250ms due to the rapid discharge of the capacitor to supply the increase load current demand.

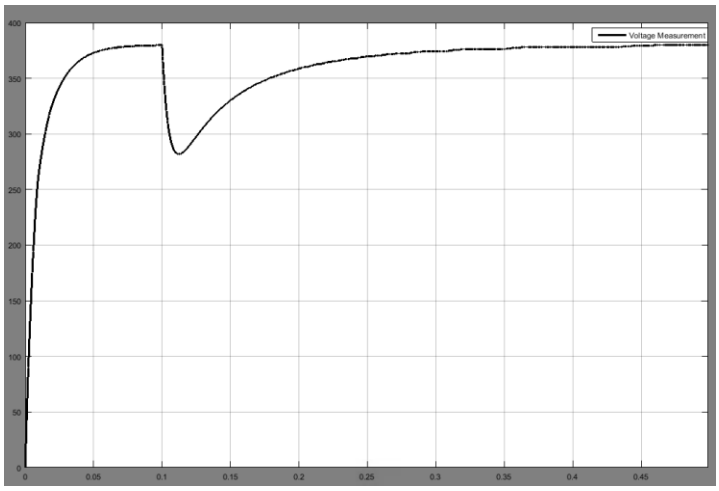

FIGURE 22: CONVERTER OUTPUT VOLTAGE - 50%-100% LOAD STEP: DIGITAL PI CONTROLLER

Fig. 25 shows the converter reaching steady state under the PI control under 2 kW load. When the load is stepped down from 2 kW to 1 kW (100%-50%), the voltage at the output spikes 150 V for 100 ms.

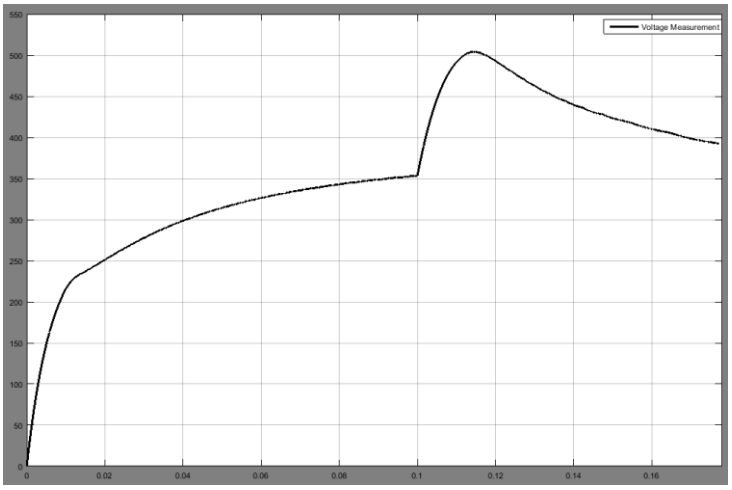

FIGURE 23: CONVERTER OUTPUT VOLTAGE - 100%-50% LOAD STEP: DIGITAL PI CONTROLLER

As described in section 4.5, the effects of load disturbances may be mitigated by implementing a feed-forward path in the control scheme, which estimates the control variable based on output current and input voltage measurements. This, again, allows for near instantaneous response to such disturbances. The feed forward path is implemented in the same Simulink model shown in Fig. 21 using a lookup table as described in section 4.5, as shown in Fig. 26. This forward path is summed with the controller calculation and then applied to the dual active bridge phase shift register. Fig. 27 and 28 show the controller's response to the same load steps as Figs. 24 and 25 with a 100 µF capacitor dc-link capacitor.

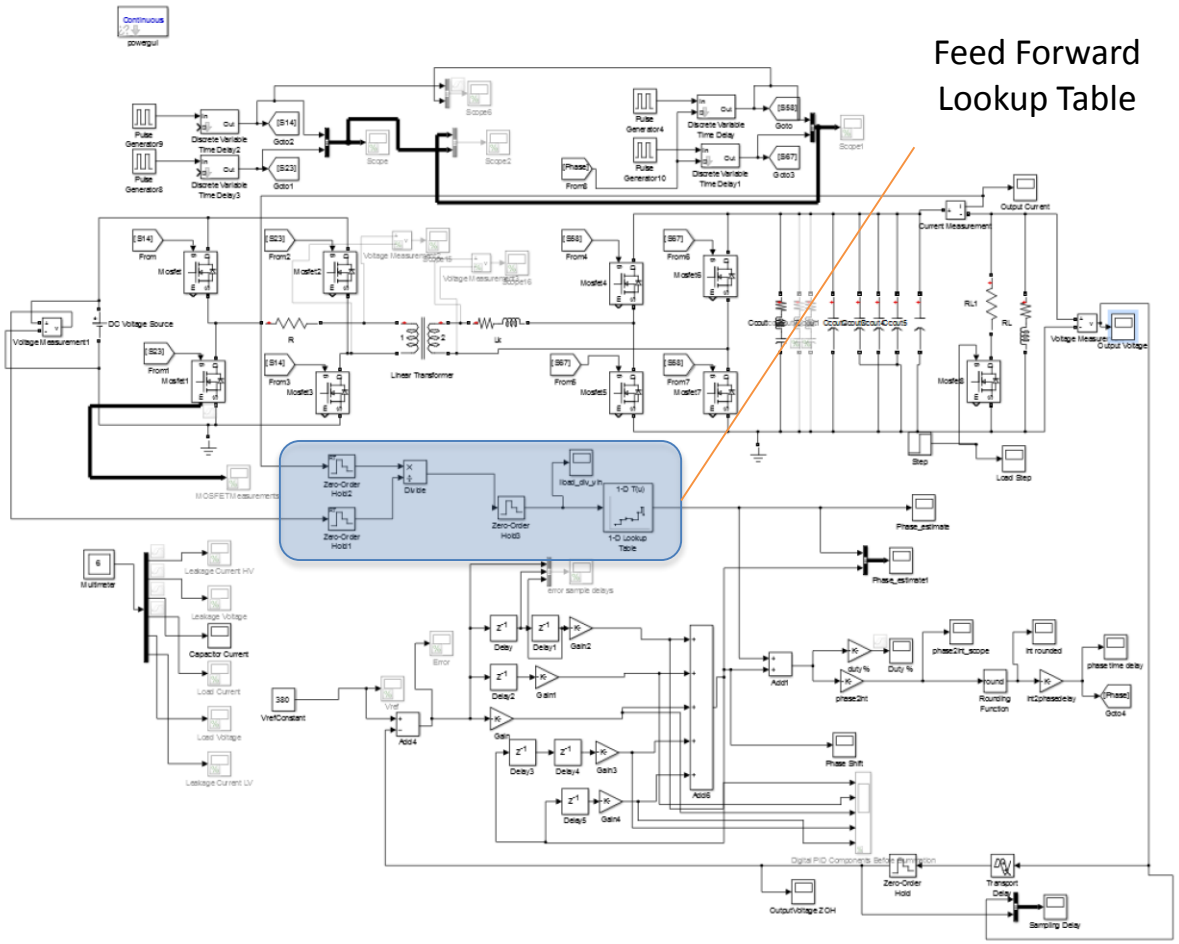

FIGURE 24: SIMULINK CONTROLLER SIMULATION: DIGITAL PI CONTROLLER PLUS FEED FORWARD

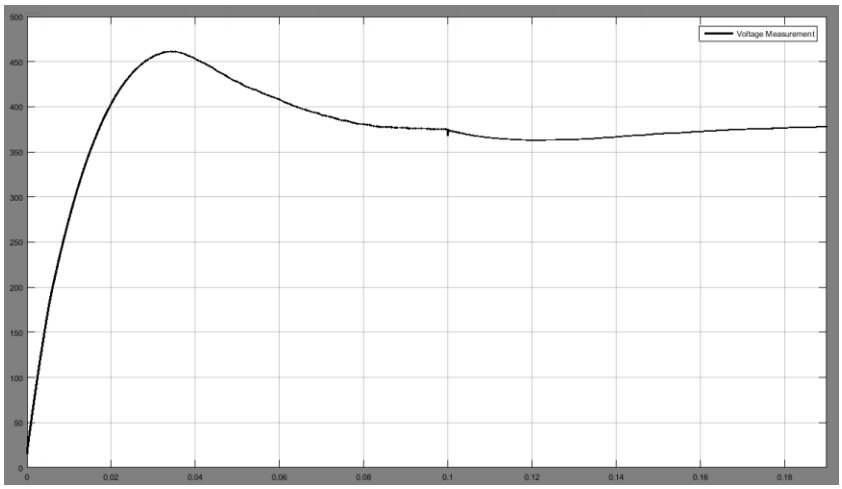

FIGURE 25: CONVERTER OUTPUT VOLTAGE - 50%-100% LOAD STEP: DIGITAL PI CONTROLLER PLUS FEED FORWARD – 100 µF DC-LINK CAPACITOR

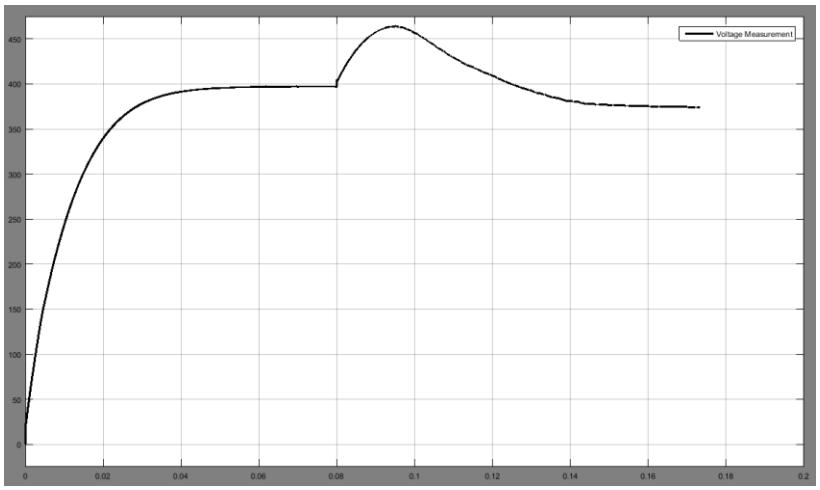

FIGURE 26: CONVERTER OUTPUT VOLTAGE - 100%-50% LOAD STEP: DIGITAL PI CONTROLLER PLUS FEED FORWARD – 100 µF DC-LINK CAPACITOR

Though the effects of the load disturbances are not completely nullified, they are less severe than the effects without the feed forward path; only sagging 20 V for 100 ms and spiking 80 V for 100 ms, respectively.

Further simulations with different output capacitances shows that the lower the dc-link capacitance, the faster the response time of the controller. Figs. 29 and 30 show the response of the controller under the same load step conditions as presented before, but with a 25 µF dc-link capacitance. The results show a 20 V sag for 50 ms and 50 V spike for 30 ms and suggest that

selecting a dc-link capacitor close to this value will yield optimal steady state tracking and allow the controller to respond quickly to load disturbances.

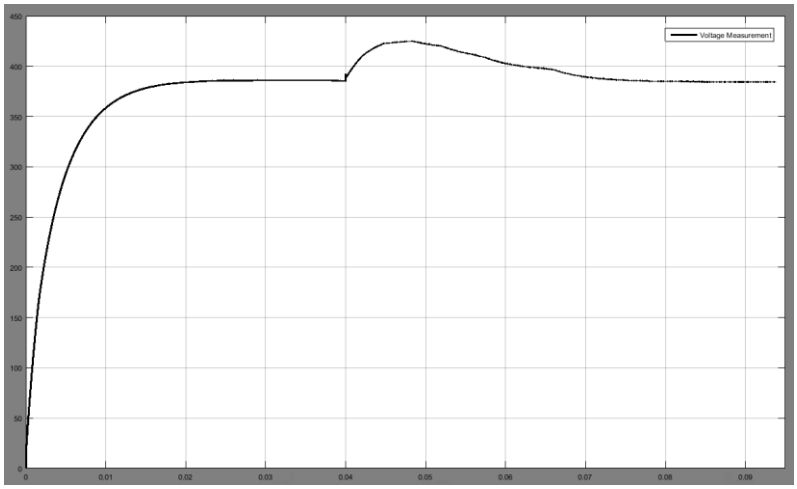

FIGURE 27: CONVERTER OUTPUT VOLTAGE - 50%-100% LOAD STEP: DIGITAL PI CONTROLLER PLUS FEED FORWARD – 25 µF DC-LINK CAPACITOR

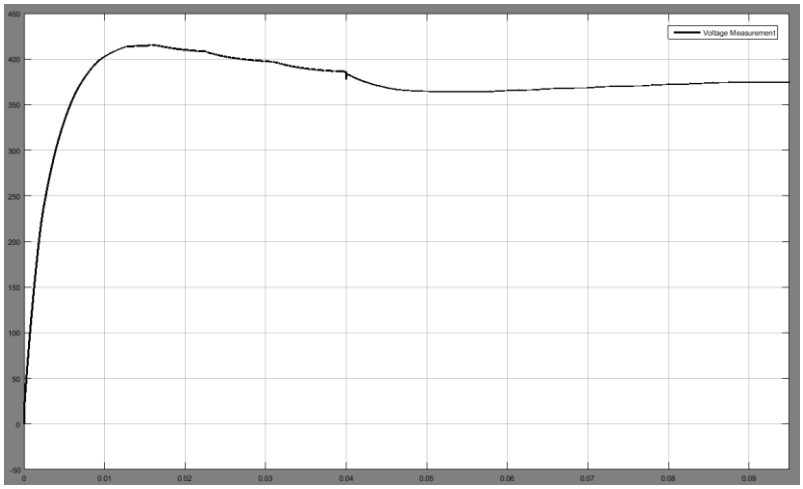

FIGURE 28: CONVERTER OUTPUT VOLTAGE - 100%-50% LOAD STEP: DIGITAL PI CONTROLLER PLUS FEED FORWARD – 25 µF DC-LINK CAPACITOR

5.3 DSP and Sensors

Control of the converter is accomplished through the use of a DSP with appropriate sensing and feedback circuitry. The DSP used is a Texas Instruments TMS320F28335, which boasts a 150 MHz clock, 32-bit floating-point processor with six individually controllable ePWM channels and a 16 channel, 12-bit ADC. For the developed prototype, the control card version of the DSP is chosen. The selected controller as described in section 5.2, requires several converter parameters to be sensed and fed back to the DSP. The PI controller requires the output voltage to be sensed, while the feed-forward path requires that the input voltage and output current be sensed.

A differential, high-impedance resistor divider circuit is employed to sense the dc-link voltages at the input and output of the converter. This configuration isolates the sampled voltage from the converter ground node and references it to the analog ground reference of the DSP and other signal conditioning circuitry. It also scales down the sensed voltage to a 0-3 V range to be sampled by the analog-to-digital converter (ADC) of the DSP. After scaling the voltage, it must be filtered to remove all high-frequency content in the signal so that only the dc component is measured. A Sallen-Key filter with an instrumentation amplifier buffer front-end is selected to perform this function for all sensed signals in this converter because of its second order cutoff characteristic and ease of use.

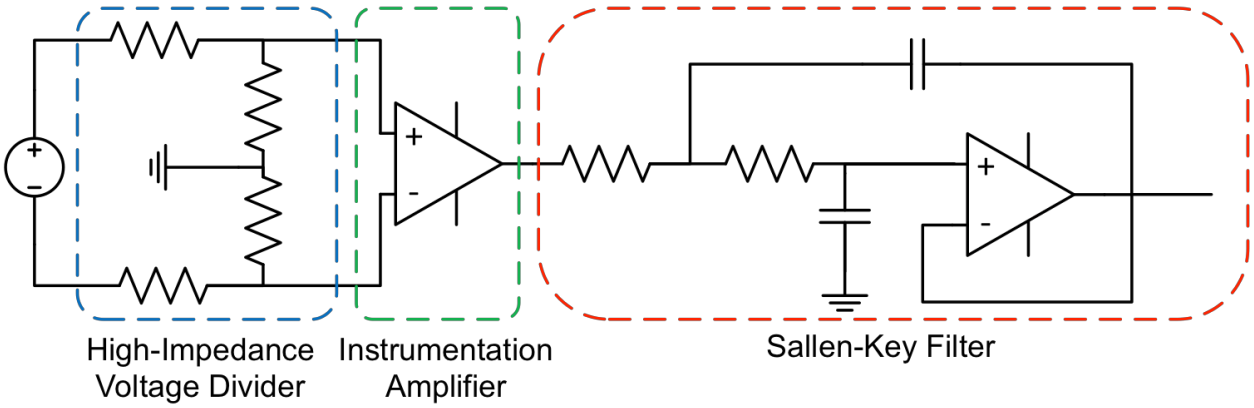

FIGURE 29: VOLTAGE SENSING NETWORK

This sensing network is applied to the LV and HV dc busses and will need to be designed for each application. Selecting voltage divider resistors is contingent upon the bus voltage, while a single Sallen-Key filter design works for both busses. Simulating the above network as it is applied to each respective bus verifies the design.

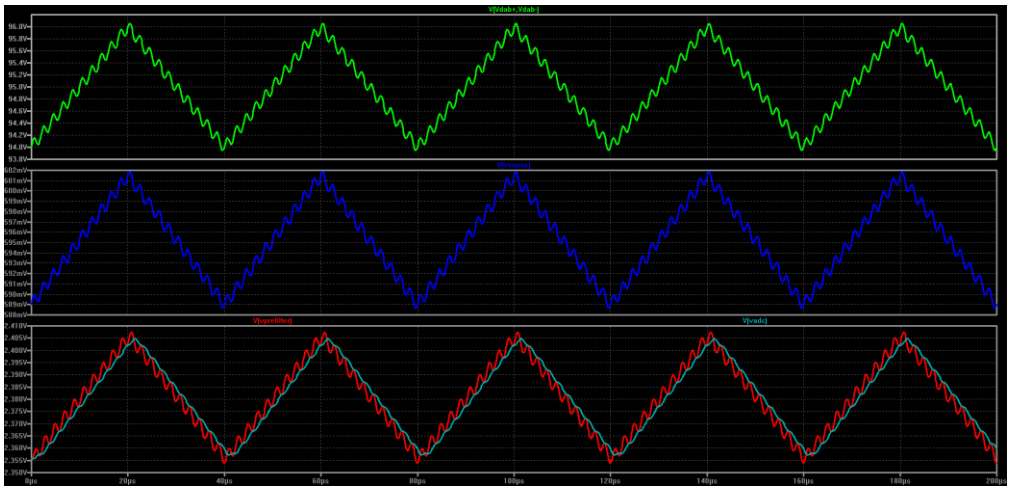

FIGURE 30: LOW VOLTAGE SENSING NETWORK: LV BUS (GREEN), RESISTOR DIVIDER (BLUE), PRE-FILTER (RED), ADC (LIGHT BLUE)

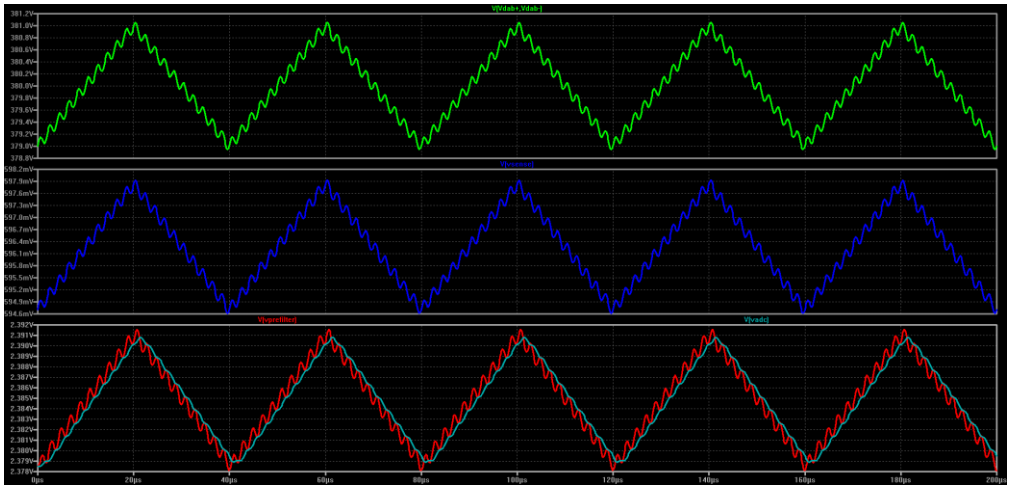

FIGURE 31: HIGH VOLTAGE SENSING NETWORK: HV BUS (GREEN), RESISTOR DIVIDER (BLUE), PRE-FILTER (RED), ADC (LIGHT BLUE)

Sampling the input and output current is more involved and has many possible solutions. For ease of implementation, the Allegro ACS712ELC-30 A Linear Hall-Effect IC is selected to measure these currents. It is capable of sensing +/-30 A with a ratiometric output from 0-5 V

centered at 2.5 V. Again, this voltage is incompatible with the ADC and must be scaled using a resistor divider. As an extra measure against noise pollution on the sensing line, a Sallen-Key filter is used to remove any harmonic content from the sensed signal. This configuration is shown in Fig. 34 and simulation/verification of the design is shown in Fig. 35 and Fig. 36.

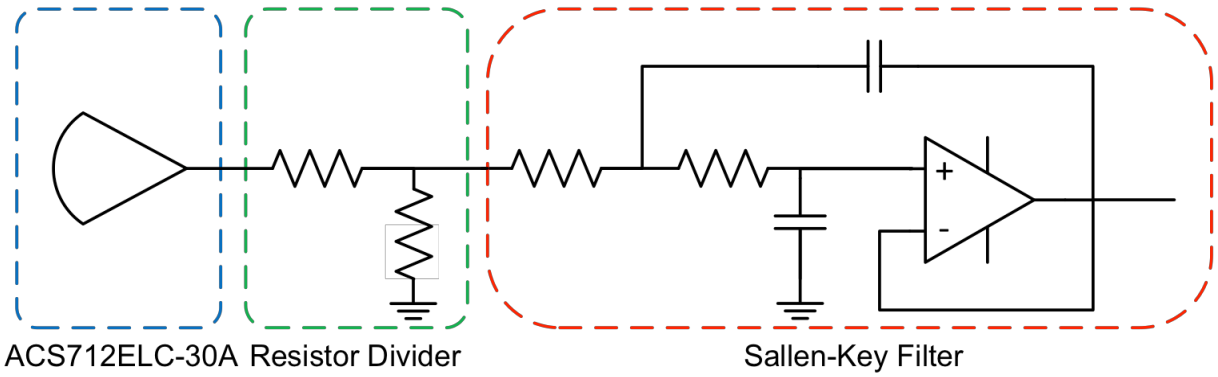

FIGURE 32: CURRENT SENSING NETWORK

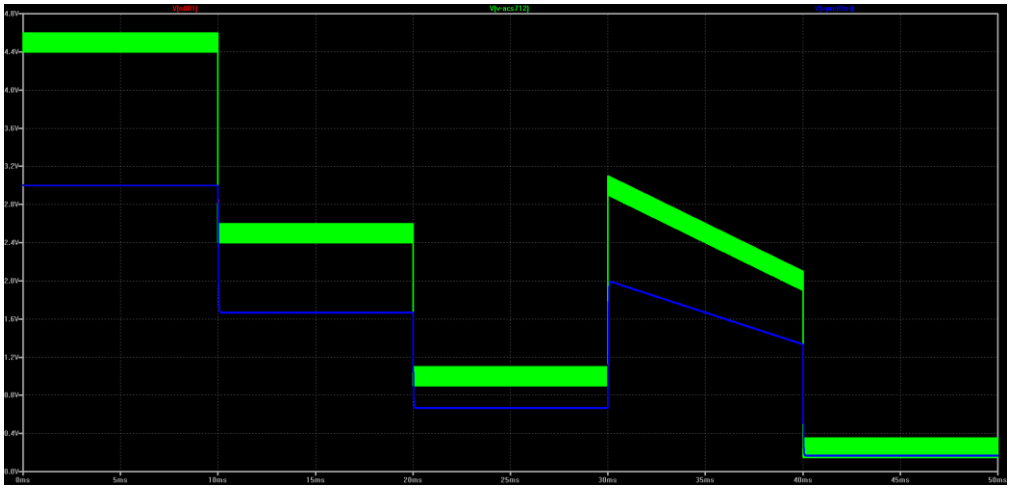

FIGURE 33: CURRENT SENSING NETWORK: ACS712ELC-30A (GREEN), PRE-FILTER (BLUE), ADC (RED)

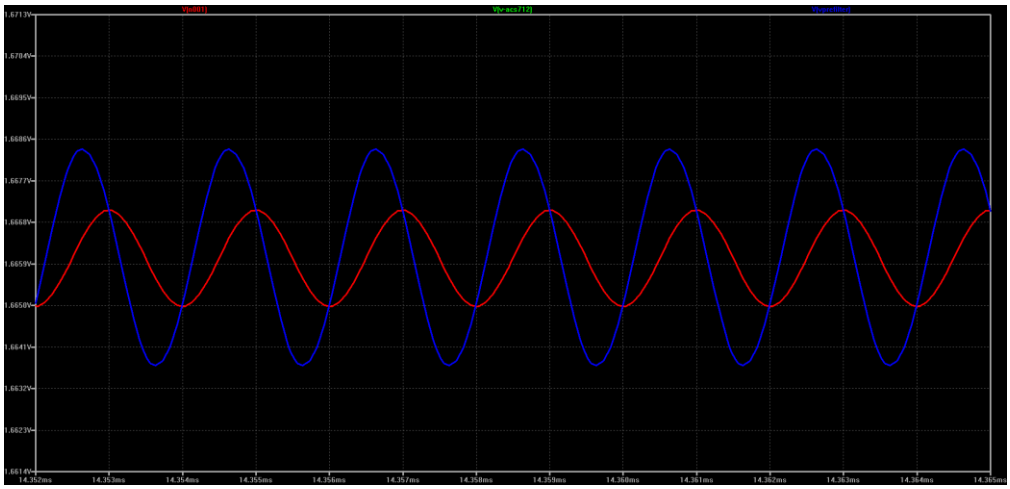

FIGURE 34: CURRENT RIPPLE REDUCTION AFTER FILTER: PRE-FILTER (BLUE), ADC (RED)

5.4 PCB Layout and Stack-up

Multi-layer printed circuit boards (PCB) are expensive and can quickly blow a budget when prototyping. However, it is possible to create a stack-up of a system, in which different components or subsystems are placed on different PCBs and stacked on top of one another. This technique allows for smaller boards to be fabricated, which are often cheaper. This method also holds the additional benefit of increasing system compactness and power density, though it comes with its own set of challenges.

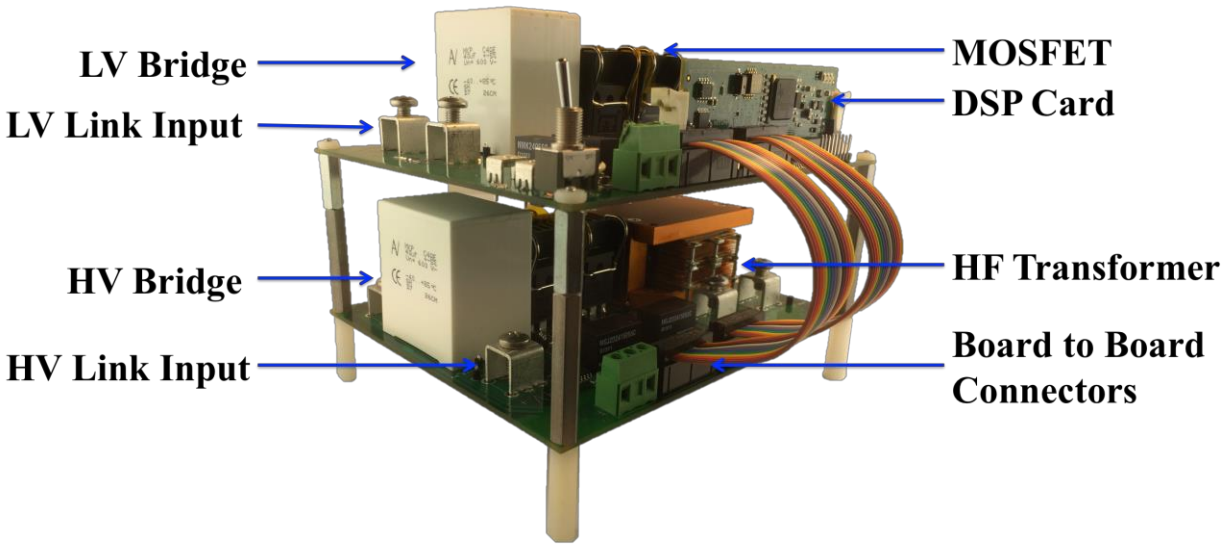

FIGURE 35: DUAL ACTIVE BRIDGE STACK-UP

High frequency operation of switching converters can lead to increased parasitic interference along high frequency signal carrying traces. In the case of this design, high frequency switching signals generated by the DSP must travel relatively long distances before they reach their respective switching devices. In order to mitigate the effects of trace inductance, differential line drivers and receivers are employed to reject any common-mode noise that is generated along the signal path. This upholds control signal integrity and reduces the chance of false switching on

any one device. In any switching bridge topology, this is very important, as shoot-through conditions will short out whole dc busses.

Another challenge of the using a stack-up design comes with the actual PCB layouts and where components and connectors are placed. Stack-ups, as opposed to single board solutions, are three-dimensional and this third dimension becomes another layout consideration. There is no right or wrong way to design the third dimension, but extra care must be taken in ensuring that any board-to-board connectors are aligned and can be easily connected. Additionally, standoff posts must be used and the alignment of these postholes must be taken into account as well.

For this stack-up the LV and HV bridges are placed on two separate PCBs, with the LV board also hosting the DSP and the HV board hosting the high frequency transformer and energy transfer inductor. Standard 4-layer PCBs are used in order to accommodate the large number of control signals and to add extra copper layers for high current carrying capacity in the LV bridge. Figs. 38-43 show the final layout and layers of the HV bridge PCB and Figs. 44-49 show the final layout and layers of the LV bridge PCB.

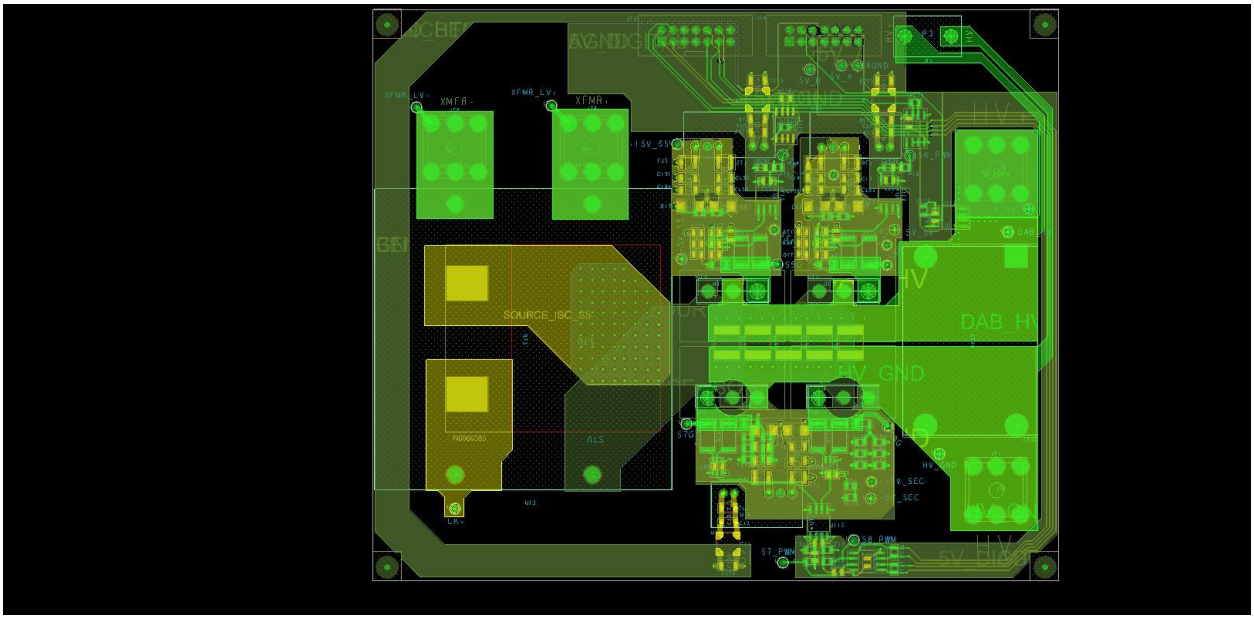

FIGURE 36: HV PCB - FULL LAYOUT

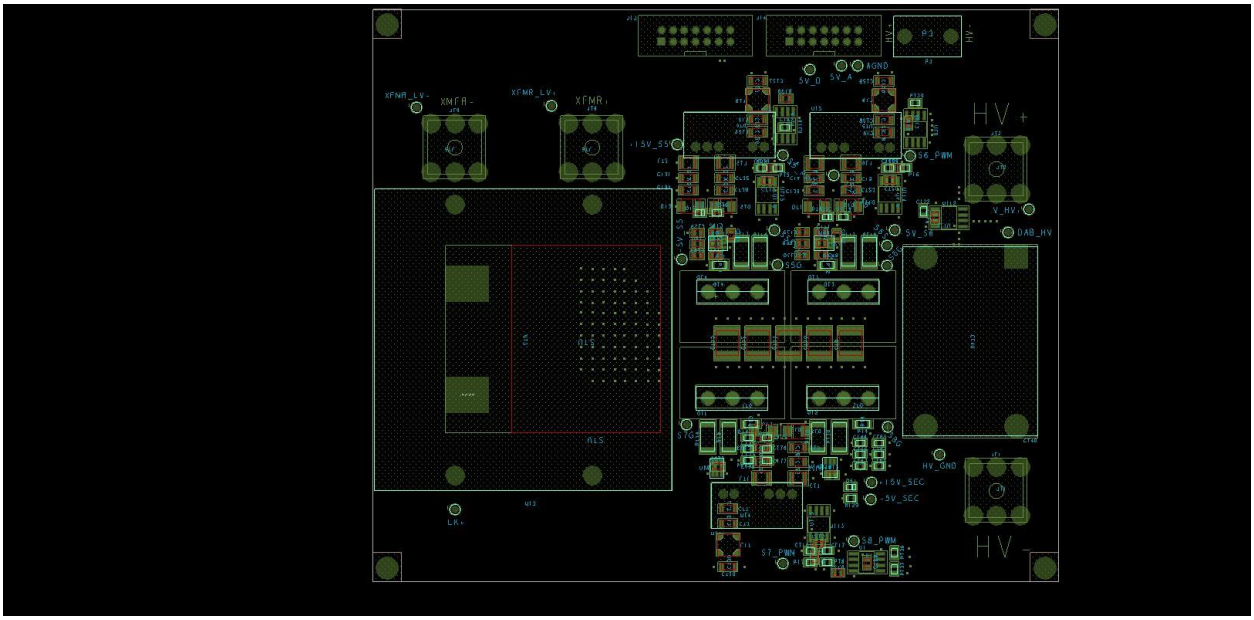

FIGURE 37: LV PCB - COMPONENT PLACEMENT/SILKSCREEN

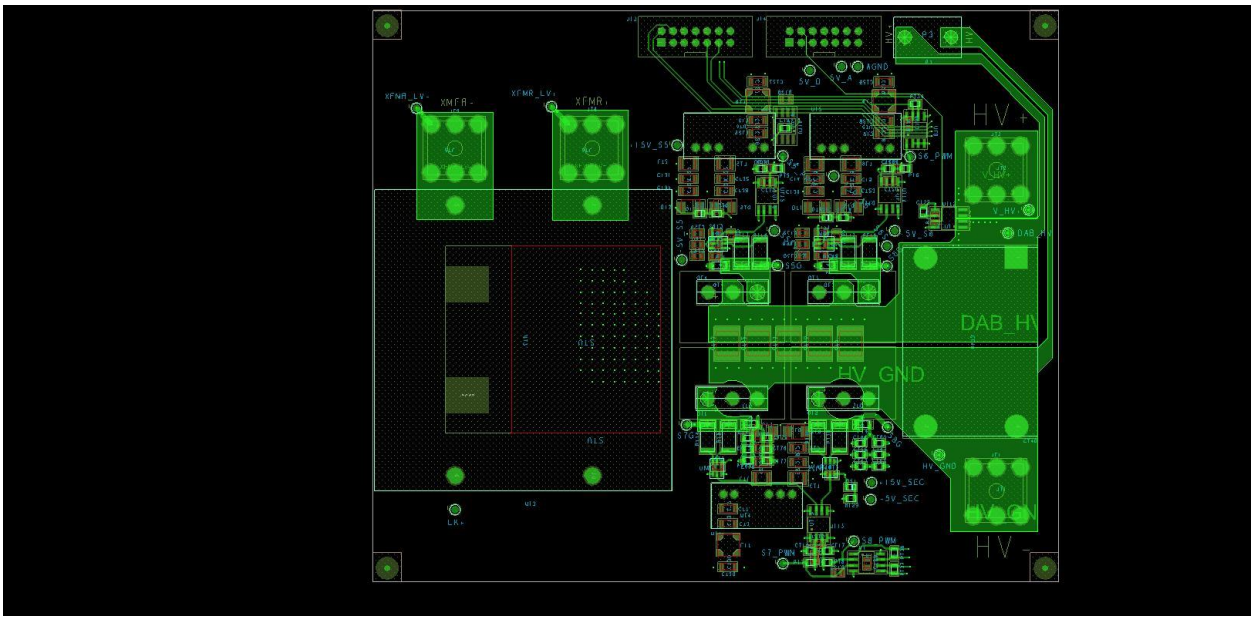

FIGURE 38: LV PCB - TOP LAYER

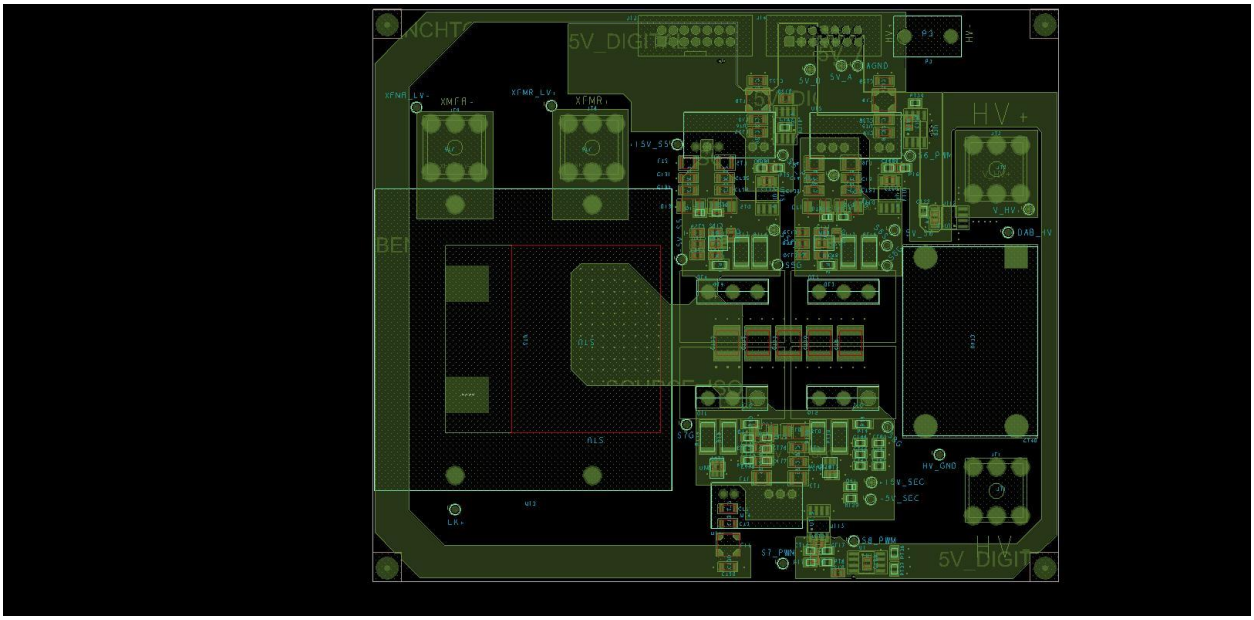

FIGURE 39: LV PCB - LAYER 2

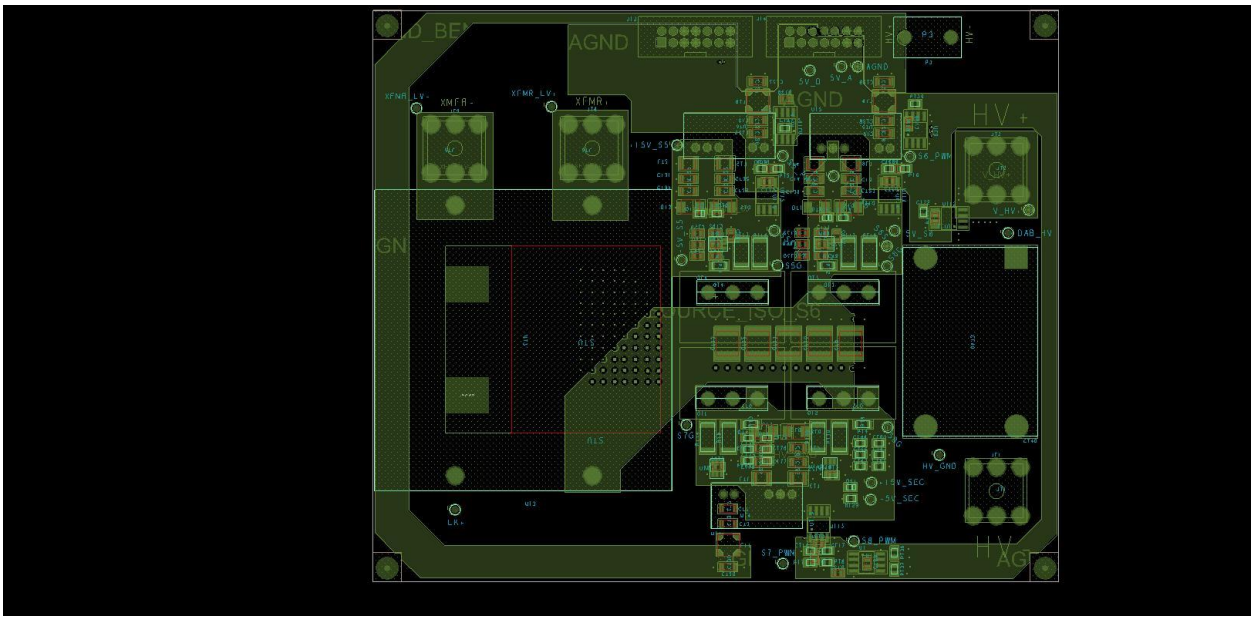

FIGURE 40: LV PCB - LAYER 3

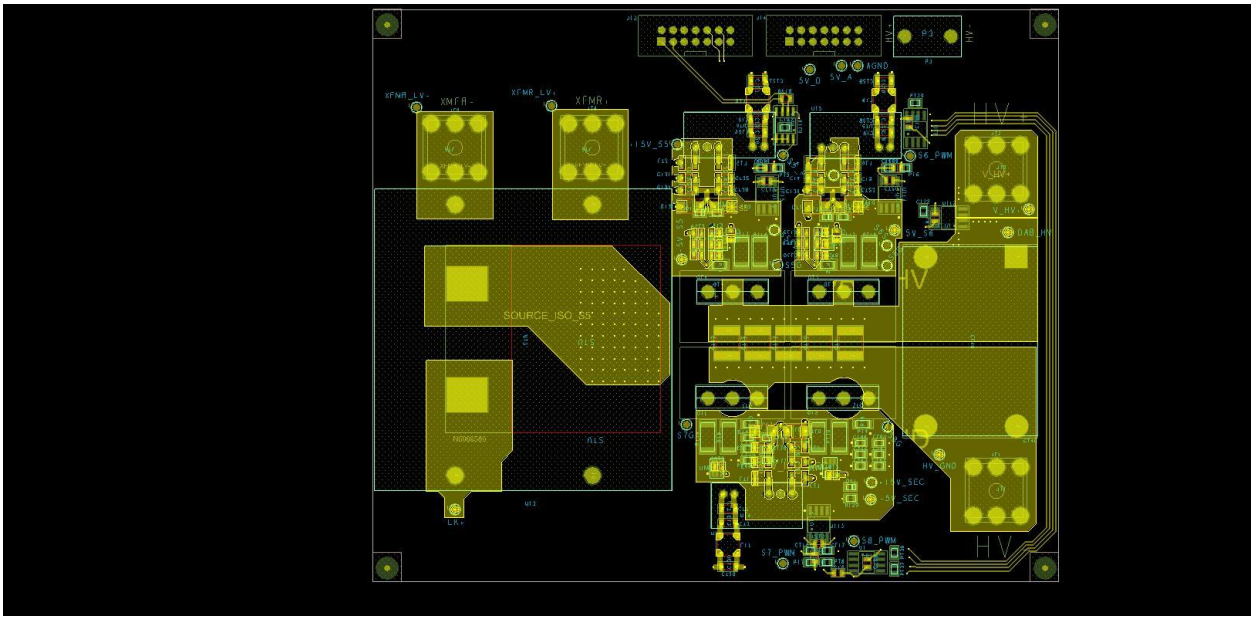

FIGURE 41: LV PCB - BOTTOM LAYER

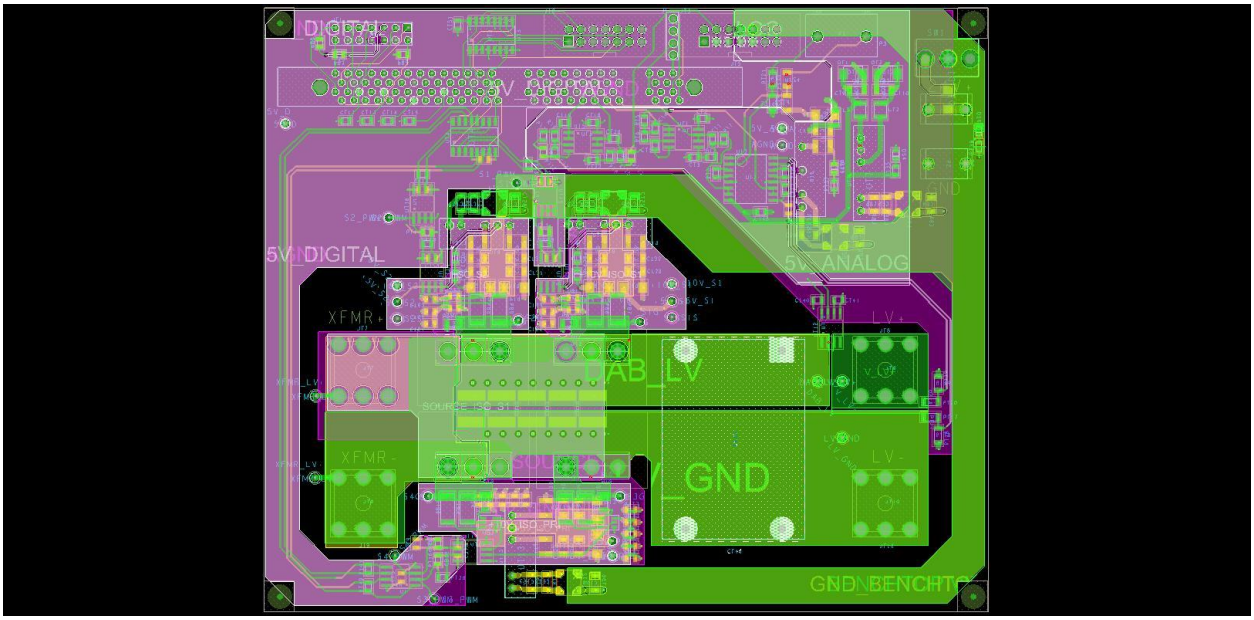

FIGURE 42: HV PCB - FULL LAYOUT

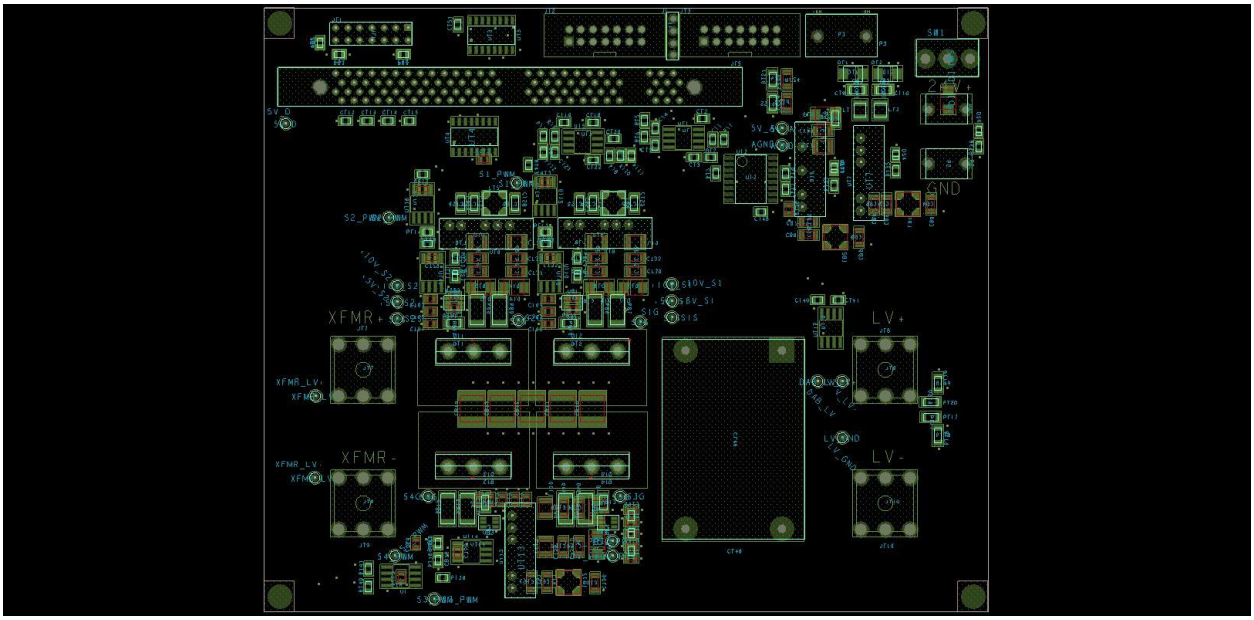

FIGURE 43: HV PCB - COMPONENT PLACEMENT/SILKSCREEN

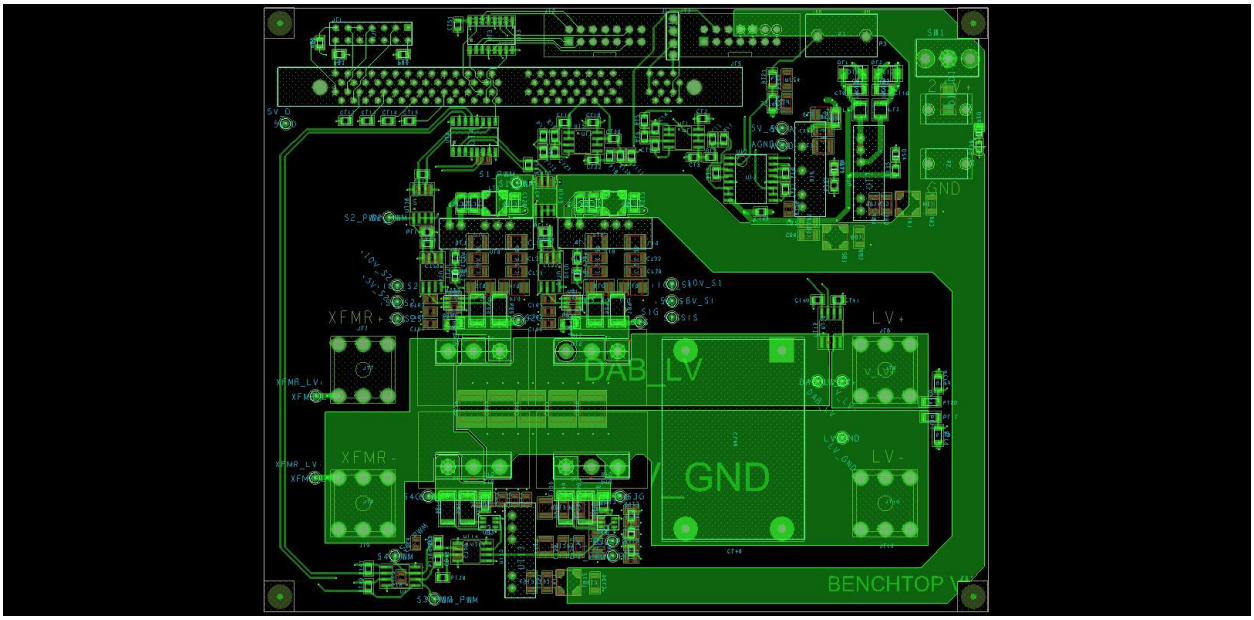

FIGURE 44: HV PCB - TOP LAYER

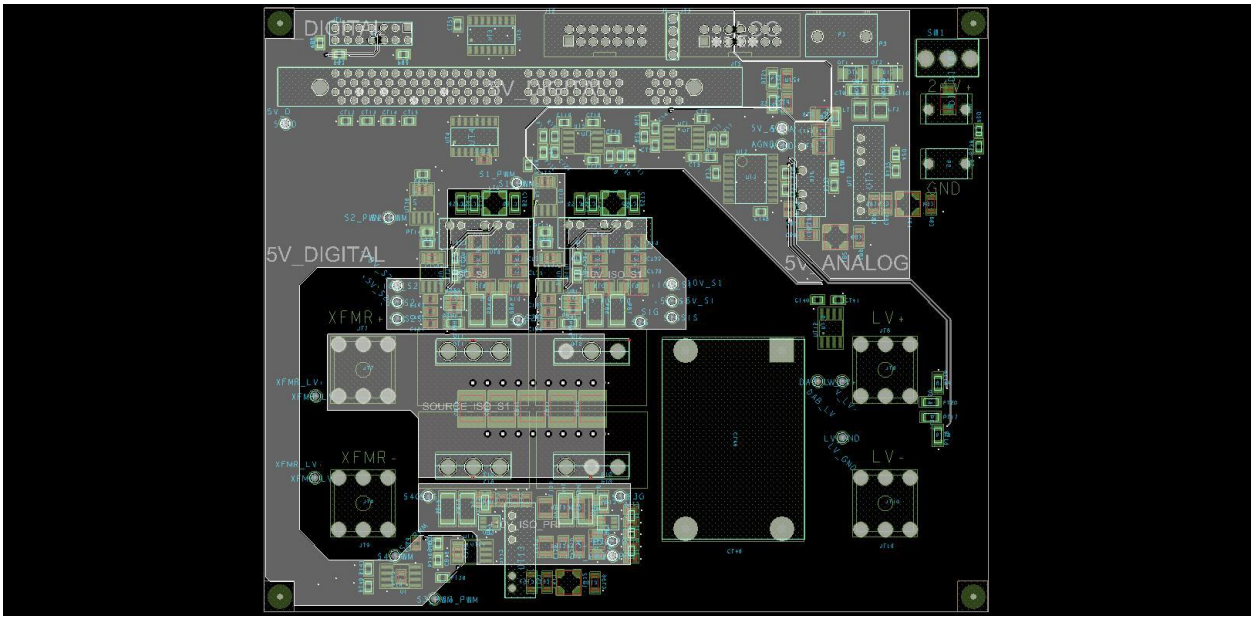

FIGURE 45: HV PCB - LAYER 2

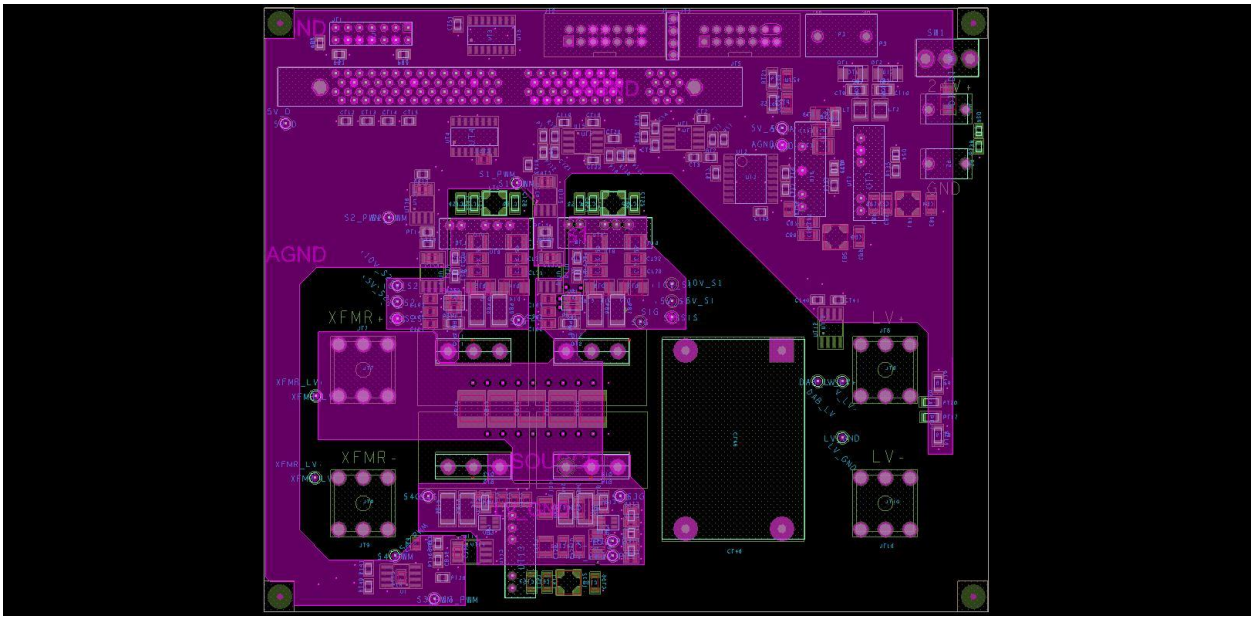

FIGURE 46: HV PCB - LAYER 3

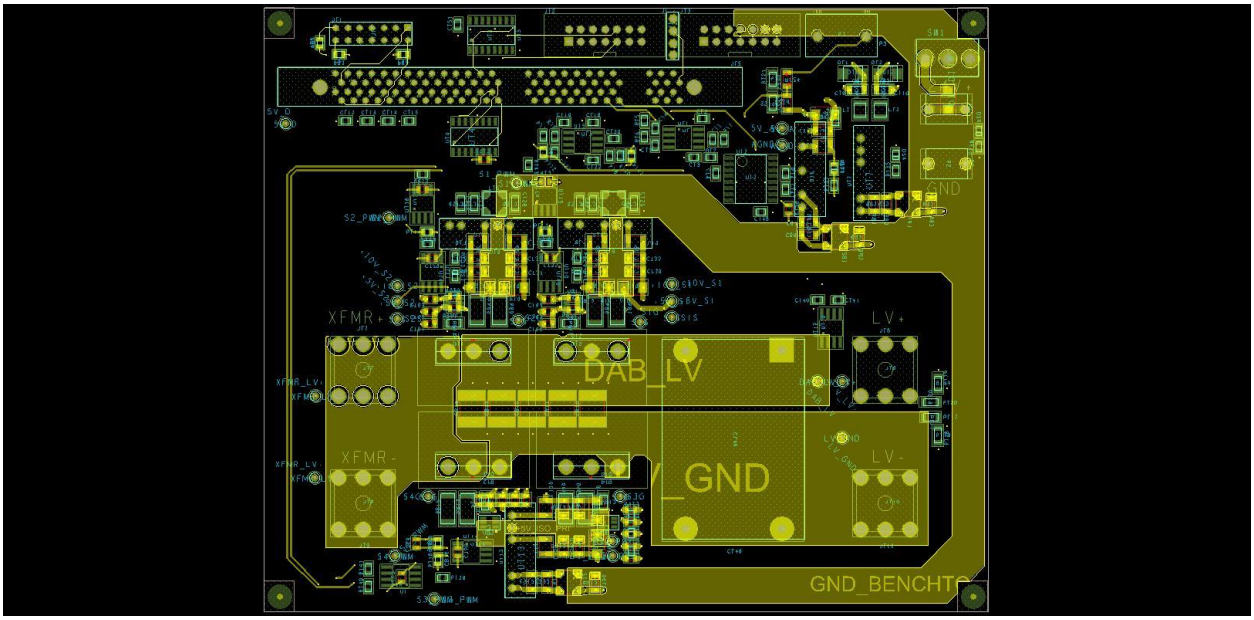

FIGURE 47: HV PCB - BOTTOM LAYER

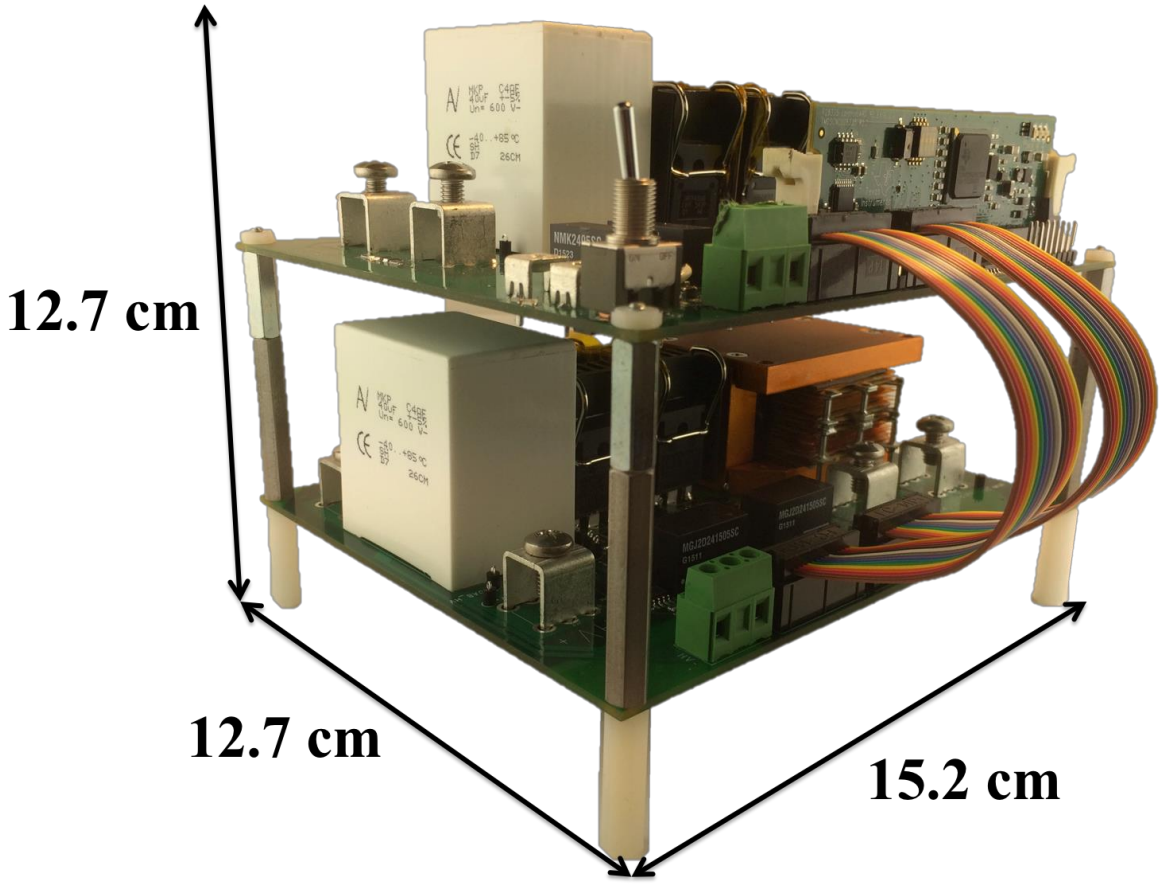

FIGURE 48: DUAL ACTIVE BRIDGE STACK-UP DIMENSIONS

6. TESTING AND RESULTS

In order to test the dual active bridge's functionality and to gauge its performance, several key pieces of equipment must be used. For one, the on board electronics must be powered via a 24 V bus. In the full SGPN system, this will be provided via a regulated bus that is pulled from the four 12 V batteries by tapping across two of the cells. However, for initial testing, a standalone Agilent E3620A dc supply is used. Another dc supply is used to emulate the low voltage dc bus at the input of the dual active bridge. To accommodate a wide power range, a 600V/20A DHP Sorensen dc power supply is selected. Measurement equipment includes a Tektronix MDO3024 Mixed Domain Oscilloscope with isolated voltage and current probes for waveform capture and a Hioki 3193 power analyzer for input/output and efficiency measurements. Finally, for variable load control, a switched matrix resistive load bank is utilized. All of the above mentioned testing equipment, except the load bank, is housed inside a large server rack with blast shields for safety purposes. Additionally, all testing above 50 V or 20 W is conducted with a safety observer.

FIGURE 49: SORENSEN DHP SERIES 600V/20A DC SUPPLY

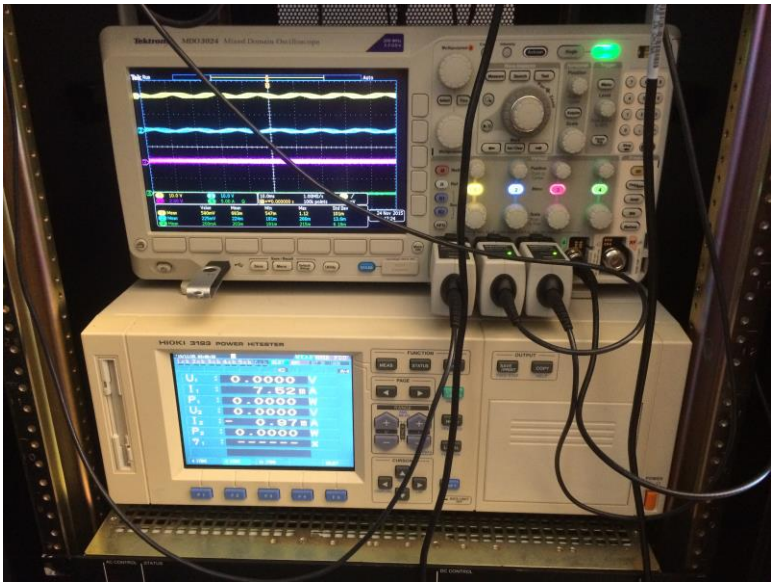

FIGURE 50: TEKTRONIX MDO3024 OSCILLOSCOPE (TOP) AND HIOKI 3193 POWER ANALYZER

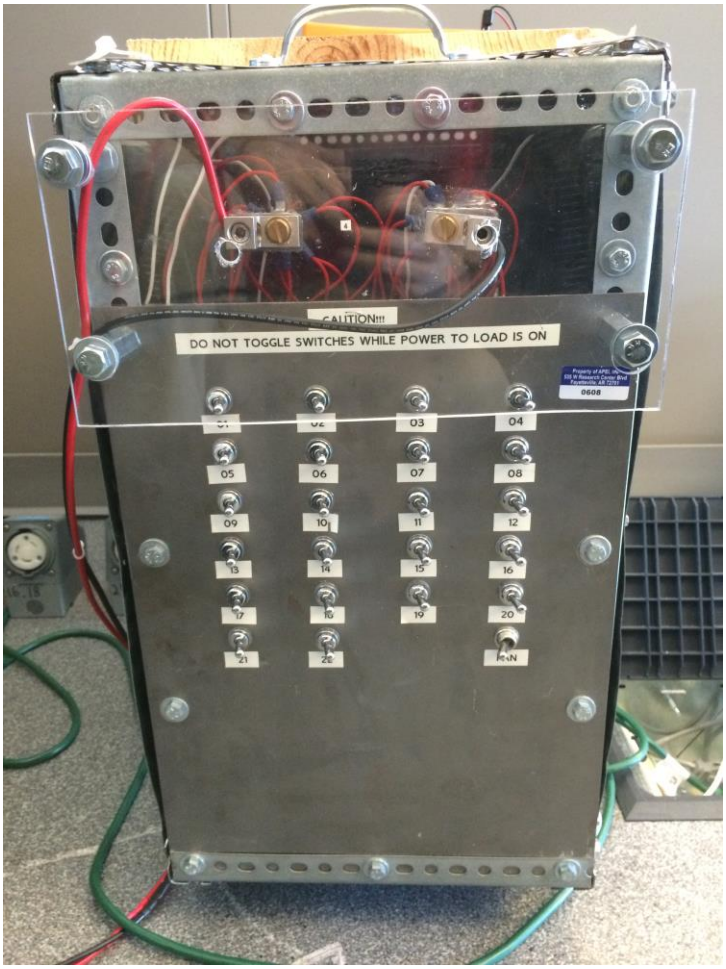

FIGURE 51: SWITCHED MATRIX RESISTIVE LOAD BANK

FIGURE 52: TEST BED HOUSED IN SERVER RACK

Key measurements include the energy transfer inductor voltage (v_{lk}) and current (i_{lk}), along with the gate signals of the leading high-side switches of each bridge (S_1 and S_5) as they are shown ideally in Fig. 2. Observing these waveforms will demonstrate the dynamic characteristics of the dual active bridge. The digital display of the Hioki power analyzer will feedback real time input/output voltages, currents, and efficiency, making it unnecessary to measure these values with the oscilloscope.

Testing across a wide range of voltages and power levels is necessary in order to maintain safety and to give an accurate measurement of performance. In conjunction with this, open loop testing of the converter is completed first before applying a closed-loop control. It should be stated at this time that a closed loop control method as described in Chapter 4 is not subjected to testing

in this work, but is recommended as the next step in future works and continued development of the SGPN system.

Beginning with low voltage levels (~10 V), the converter is first tested to ensure energy transfer from one bridge to the next. After the functionality of the converter is confirmed, a steady step increase of the input voltage up to the ideal 95 V input is completed in order to avoid a catastrophic failure at higher voltages. Again, this is done for safety reasons. All throughout this process, load changes are made in order to keep the power levels in line with the voltage increases, and this includes calculating open loop duty percentages for each test in order to guarantee the load is matched to the power delivery. Additionally, a parameter of the switching waveforms, the space between gate pulses (dead time), is varied to show its effects on converter efficiency and to accommodate the nonlinear effects of the input capacitance of the Si MOSFET devices. Tabulated results of 10 tests with varied system parameters are shown in Table V.

Waveforms captured during testing show the inductor current and voltage as similar to those outlined in section 3.2, though with excessive ringing. This is because of the non-ideal nature of implemented power converters, especially those operating at high frequencies. In addition to the intangibles associated with real world high frequency power converters, planar transformers are known to be exceptionally noisy compared to their wound transformer counterparts [21]. There is indeed a tradeoff between compactness and dynamic performance when considering transformers for these applications. Taking note of the excessive ringing, and to offer an argument for the differences between planar and wound transformers, a low power test was performed with a ferrite 3C96 magnetic core hand wound transformer in place of the planar transformer. Waveforms associated with all 10 tests using the planar transformer are shown in Figs. 55-64,

while the one low power test using the hand wound transformer is shown in Fig. 65. In all waveforms: yellow - S_1, blue - S_5, purple - v_{lk}, and green - i_{lk}, unless otherwise stated.

TABLE V: TESTING RESULTS

	Designed Test Parameters						Measured Values						
	Input Voltage	*Ideal Power*	*Load Resistance*	*Duty Percentage*	*Switching Frequency*	*Dead Time*	*Input Voltage*	*Input Current*	*Output Voltage*	*Output Current*	*Input Power*	*Output Power*	*Efficiency*
Test 1	10 V	20 W	80 Ω	0.27	250 kHz	333 ns	10.2 V	1.38 A	32.14 V	0.386 A	14.1 W	12.4 W	88.30%
Test 2	20 V	80 W	80 Ω	0.27	250 kHz	666 ns	20.4 V	2.65 A	62.55 V	0.753 A	53.8 W	47.2 W	87.50%
Test 3	30 V	120 W	120 Ω	0.155	250 kHz	666 ns	30.3 V	3.08 A	101.4 V	0.818 A	93.4 W	83 W	88.80%
Test 4	50 V	333 W	120 Ω	0.155	250 kHz	666 ns	50.4 V	4.97 A	165.1 V	1.33 A	251 W	220 W	87.80%
Test 5	75 V	750 W	120 Ω	0.155	250 kHz	666 ns	75.6 V	7.31 A	243.4 V	1.96 A	553.8 W	477.92 W	86.30%
Test 6	95 V	1200 W	120 Ω	0.155	250 kHz	666 ns	95.8 V	9.13 A	304.4 V	2.46 A	875.5 W	749.5 W	85.60%
Test 7	95 V	1800 W	80 Ω	0.27	250 kHz	666 ns	95.7 V	11.5 A	278.6 V	3.36 A	1105.3 W	936.8 W	84.76%
Test 8	95 V	1800 W	80 Ω	0.27	250 kHz	333 ns	95.8 V	11.6 A	279.65 V	3.37 A	1110.8 W	945.5 W	85.11%
Test 9	95 V	2050 W	70 Ω	0.34	250 kHz	333 ns	94.9 V	13.4 A	276 V	3.82 A	1277.2 W	1054.4 W	82.56%
Test 10	10 V	22.3 W	70 Ω	0.34	250 kHz	333 ns	19.2 V	2.57 A	41 V	0.567 A	26.4 W	23.3 W	88.60%

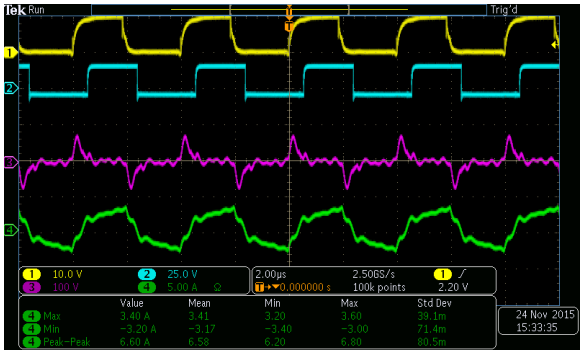

FIGURE 53: DUAL ACTIVE BRIDGE TEST #1

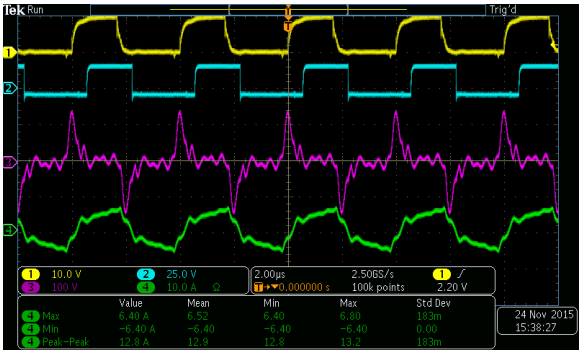

FIGURE 54: DUAL ACTIVE BRIDGE TEST #2

FIGURE 55: DUAL ACTIVE BRIDGE TEST #3

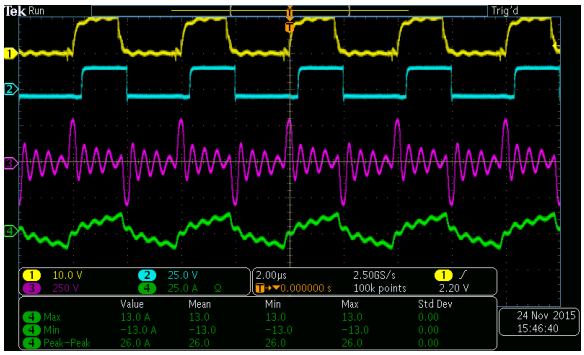

FIGURE 56: DUAL ACTIVE BRIDGE TEST #4

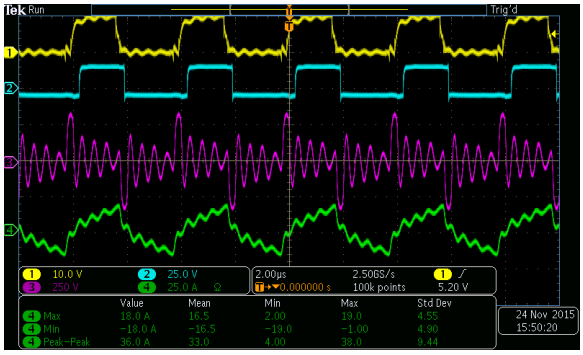

FIGURE 57: DUAL ACTIVE BRIDGE TEST #5

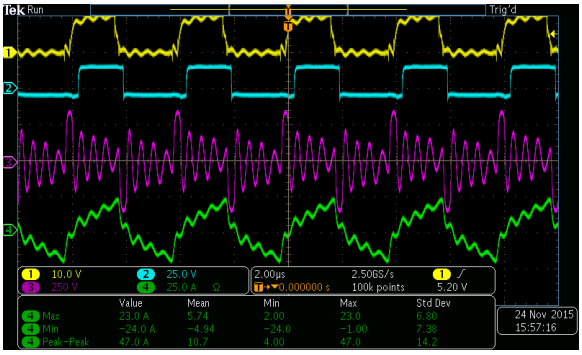

FIGURE 58: DUAL ACTIVE BRIDGE TEST #6

FIGURE 59: DUAL ACTIVE BRIDGE TEST #7

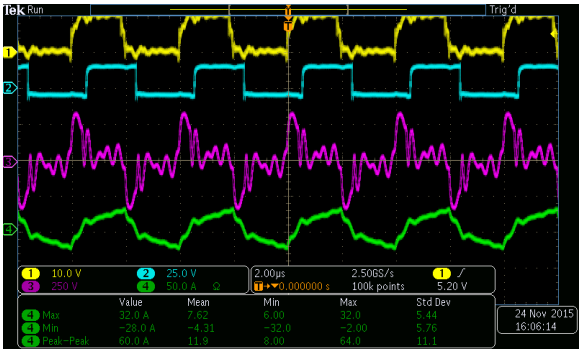

FIGURE 60: DUAL ACTIVE BRIDGE TEST #8

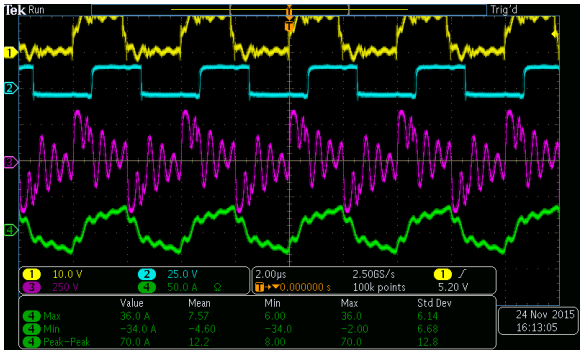

FIGURE 61: DUAL ACTIVE BRIDGE TEST #9

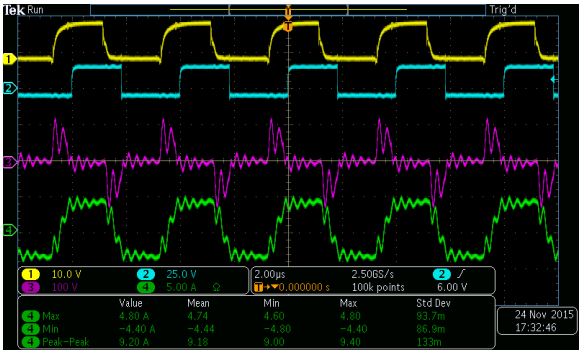

FIGURE 62: DUAL ACTIVE BRIDGE TEST #10

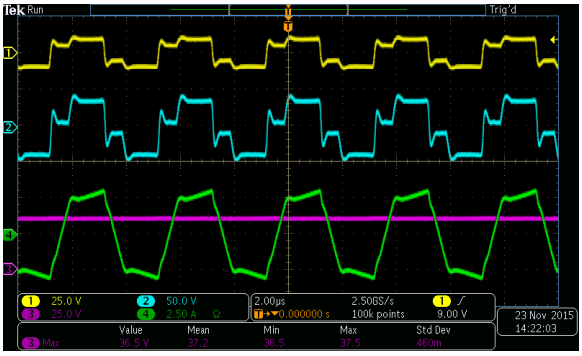

FIGURE 63: DUAL ACTIVE BRIDGE TEST - WOUND TRANSFORMER – Transformer Primary (Yellow), Transformer Secondary (Blue), Voltage Output (Purple), Inductor Current (Green)

These tests reveal that the dual active bridge does indeed transfer power from one bridge to the other and is capable of handling power capacities up to 1.75kW. However, the efficiency is below specification, with peak efficiencies of ~88%, not including the power required to operate the gate drivers and ancillary circuitry. Reevaluating the test bench using a thermal camera to search for heat losses revealed that the pair of board to board connectors that connect the inverted LV signal to the input of the transformer on the HV board was heating to temperatures in excess of 100 °C. The contact points where not of sufficient size to handle the larger currents on the LV side of the converter and were replaced with larger circle connectors. For direct comparison, test 10 is repeated at the calculated ideal 2050 W in order to observe the results of replacing the connector. Fig. 66 shows the waveforms resulting from this test. As can be seen, the ringing in the inductor voltage is greatly reduced and more closely matches the ideal case shape of the inductor voltage. Additionally, the efficiency is increased from ~84% to ~88%, as calculated by the Hioki

power analyzer (Fig. 67), along with a substantial increase in the observed output voltage. It is truly amazing how much the tiniest of details in converter design and builds can have the largest of impacts in overall system performance.

It is also worth noting that the output voltage of each measurement does not match directly with the 1:4 turns ratio of the transformer. This is because of the large dead times used in these preliminary tests in order to observe certain safety precautions and potential hazards with shoot through currents.

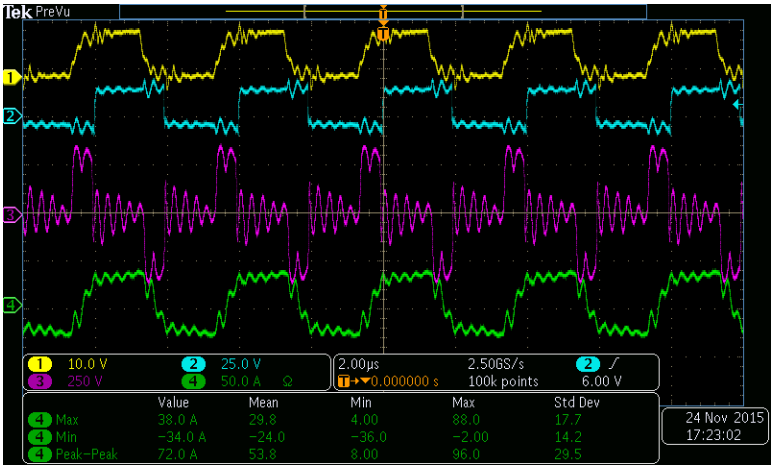

Figure 64: DUAL ACTIVE BRIDGE TEST (WAVEFORMS) - REPLACED CONNECTOR

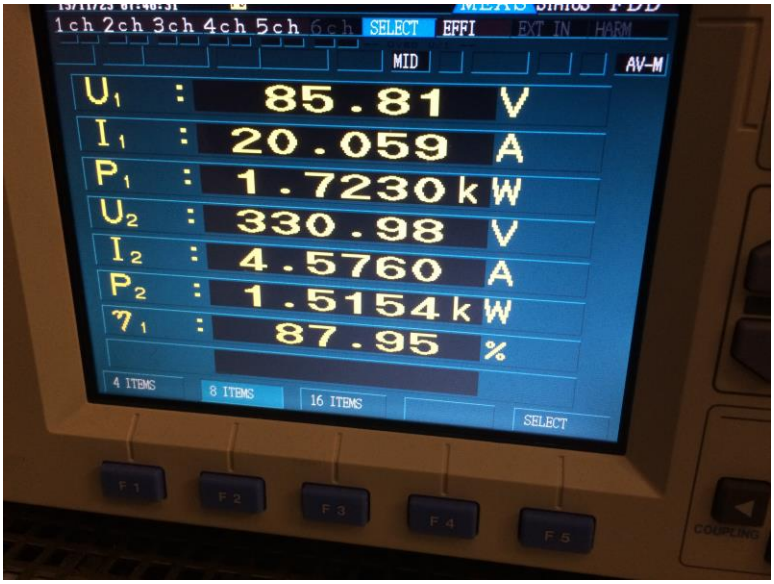

Figure 65: DUAL ACTIVE BRIDGE TEST (HIOKI) - REPLACED CONNECTOR

7. CONCLUSIONS

In this work, a dual active bridge is identified as a preferred power converter for interfacing the low voltage and high voltage dc busses of the Smart Green Power Node system due to its potential high power capacity and bidirectional power flow capabilities. An overview of the dual active bridge converter principle of operation, bidirectional power flow capability, and dynamic characteristics were discussed in Chapter 3. Converter modeling and control methods are developed in Chapter 4 based upon an enhanced Fourier series based model of the switching actions of the converter. Chapter 4 also demonstrates the feasibility and desirable results of applying a PI controller for matched steady state tracking of a reference output voltage. In conjunction with the feed forward control path, this control scheme facilitates optimal converter operation and performance, even accounting for load disturbances. Matlab/Simulink simulations verify this control scheme's quality. Chapter 5 discusses more in depth the design of a 2 kW, 95V/380V, bidirectional dual active bridge converter. Sizing of the energy transfer inductor, peak specifications of the high frequency transformer, selection of controller parameters, design of adequate feedback signal conditioning networks, and converter stack-up are all covered. Finally, chapter 6 presents results from preliminary testing of the converter up to 1.75 kW with peak efficiencies of ~88%.

The resulting converter from this work will require further work in order to meet all desired specification of the SGPN system. This future work will include further investigation of losses in the converter and testing of the digital controller under load disturbance scenarios. Tuning of the dead time could lead to increased efficiency, but will certainly lead to a better voltage conversion ratio as the dead time reduces the effective pulse width of each gate signal and reduces the average voltage delivered to the primary of the transformer.

Overall, the design and demonstration of this converter yielded a power electronic interface capable of operating up to 1.75 kW, with a power capacity of 0.814 W/cm^3 with an incredibly low mass of 1 kg. By increasing the switching frequency of the dual active bridge converter and utilizing advanced wide bandgap SiC semiconductor devices, many external passive components were greatly reduced in size compared to previous versions of the SGPN. One point of comparison lies within the size of the planar transformer, in which the one used in this build is 66% smaller than transformer used in previous builds. It was found that planar transformers are noisier at high frequency than their wound counterparts, as can be seen when comparing the switching waveforms of Fig. 65 and any of the 10 tests conducted using the planar transformer. Another size reduction opportunity was shown through the simulations of the digital controller, in which lower output capacitances allowed the controller to respond more quickly to load disturbances.

The knowledge and experience acquired in this work will be further developed in future work, both academic and professional. Implementing a full power converter system requires attention to more details than presented in the classroom. Subsystems within the converter, including feedback networks, controller design and digital implementation, gate driver circuitry, PCB layout and system stack-up, and safe testing best practices were all developed further in the student who completed this work. It is the student's desire to continue to build upon the successes of this thesis work and to push the boundaries of high-density high frequency power converter design through continued study of wide bandgap semiconductor devices and their benefits in systems like the smart green power node.

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APPENDIX A - DSP CODE

```
/*
 * main.c
 */

// ===========================================================================
// =================                          ====================
// =================      Global Definitions      ====================
// =================                          ====================
// ===========================================================================

// Include header files
#include "DSP28x_Project.h"     // Device Headerfile and Examples Include File
#include <stdio.h>
#include <math.h>

// Interrupt Definition
__interrupt void adc_isr(void);

// Function Definitions
void SystemStart(void);
void PID(void);

// Timer/ePWM Variables
#define PI 3.141592654
#define PWMCARRIER 250E3 /*PWM FREQ = 250kHz*/
#define SYSCLK 150E6 /* 150MHz */
#define TBCLK 150E6 /* 150MHz */
#define ADC_MODCLK 0x3 // HSPCLK = SYSCLKOUT/2*ADC_MODCLK2 = 150/(2*3)   = 25.0 MHz
Uint16 EPwm_TBPRD = (TBCLK/PWMCARRIER)/2;
float PI_INV = 1/PI;
float phase = 0;
float duty = 0;

// PID Variables
float reference = 380; // reference voltage
#define Kp  0.11173*0.015 // proportional gain
#define Ki  0.11173 // integral gain
#define Kd  0 // derivative gain
#define N  0 // derivative filter coefficient (equal to 0 when using PI control vs. PID control)
#define cycledelay  2 // number of pwm cycles per sample


// PID Variables
float Ts = 0;// Ts = cycledelay/PWMCARRIER (example: cycledelay = 5, PWMCARRIER = 250kHz --> Ts
= 5/250000 = 20us)
float b0 = 0;
float b1 = 0;
float b2 = 0;
float a0 = 0;
float a1 = 0;
float a2 = 0;
float A1 = 0;
float A2 = 0;
```

```
float B0 = 0;
float B1 = 0;
float B2 = 0;

float x = 0; // computational variable
float delta0 = 0; // delta[k]
float delta1 = 0; // delta[k-1]
float delta2 = 0; // delta[k-2]
float error0 = 0; // error[k]
float error1 = 0; // error[k-1]
float error2 = 0; // error[k-2]



// ADC Variables
float ADC2Bit = 1/1365; // 3V/4095bit = 732.6uV
float V_HV = 0;
float V_LV = 0;
float I_HV = 0;
float I_LV = 0;
float test0 = 0;
float test1 = 0;
float test2 = 0;
float a = 0;
float b = 0;
float c = 0;
float d = 0;

// Control Variables

int main(void)
{


        // Initialize System Control:
            InitSysCtrl();

        // Clock Setting
            EALLOW;
            SysCtrlRegs.HISPCP.all = ADC_MODCLK;     // HSPCLK = SYSCLKOUT/ADC_MODCLK
            EDIS;

        // Define GPIO for use as EPWM and ADC SOC
            InitEPwm1Gpio();
            InitEPwm2Gpio();
            InitEPwm3Gpio();
            InitEPwm4Gpio();
            InitEPwm6Gpio();


        // Clear all interrupts and initialize PIE vector table:
        // Disable CPU interrupts
            DINT;

        // Initialize the PIE control registers to their default state.
```

```
        InitPieCtrl();

    // Disable CPU interrupts and clear all CPU interrupt flags:
        IER = 0x0000;
        IFR = 0x0000;

    // Initialize the PIE vector table with pointers to the shell Interrupt
    // Service Routines (ISR).
        InitPieVectTable();

    // Interrupts that are used are re-mapped to
    // ISR functions found within this file.
        EALLOW;  // This is needed to write to EALLOW protected register
        PieVectTable.ADCINT = &adc_isr;
        EDIS;    // This is needed to disable write to EALLOW protected registers

//###########################################################################
//                      GPIO Setup
    // Testing Pin
        EALLOW;
        GpioCtrlRegs.GPAPUD.bit.GPIO8 = 0;   // Enable pullup on GPIO2
        GpioDataRegs.GPASET.bit.GPIO8 = 1;   // Load output latch
        GpioCtrlRegs.GPAMUX1.bit.GPIO8 = 0;  // GPIO2 = GPIO
        GpioCtrlRegs.GPADIR.bit.GPIO8 = 1;   // GPIO2 = output
        GpioDataRegs.GPACLEAR.bit.GPIO8 = 1; // Initalize LOW
        EDIS;


  // Initialize all the Device Peripherals:
        InitAdc();  // For this example, init the ADC


    // Enable ADCINT in PIE
        PieCtrlRegs.PIEIER1.bit.INTx6 = 1;
        IER |= M_INT1; // Enable CPU Interrupt 1
        EINT;         // Enable Global interrupt INTM
        ERTM;         // Enable Global realtime interrupt DBGM

  // Configure ADC
        AdcRegs.ADCMAXCONV.all = 0x0001;      // Setup 2 conv's on SEQ1
        AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x0; // Setup ADCINA0 as 1st SEQ1 conv.
        AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0x1; // Setup ADCINA1 as 1st SEQ1 conv.
        AdcRegs.ADCCHSELSEQ1.bit.CONV02 = 0x2; // Setup ADCINA2 as 1st SEQ1 conv.
        AdcRegs.ADCCHSELSEQ1.bit.CONV03 = 0x3; // Setup ADCINA3 as 1st SEQ1 conv.
        AdcRegs.ADCTRL2.bit.EPWM_SOCA_SEQ1 = 1;// Enable SOCA from ePWM to start SEQ1
        AdcRegs.ADCTRL2.bit.INT_ENA_SEQ1 = 1;  // Enable SEQ1 interrupt (every EOS)
  //AdcRegs.ADCTRL3.bit.SMODE_SEL = 1;       // Simultaneous sample mode

        EALLOW;
        SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;
        EDIS;


  // EPWM Module 1 config
        EPwm1Regs.TBPRD = EPwm_TBPRD; // Period = 900 TBCLK counts
        EPwm1Regs.TBPHS.half.TBPHS = 0; // Set Phase register to zero
```

```
        EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Symmetrical mode
        EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE; // Master module
        EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;      // Clock ratio to SYSCLKOUT  //
HSPCLKDIV = (1 -- 0b000)
        EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;        // CLKDIV = (1 -- 0b000)
        EPwm1Regs.TBCTL.bit.PRDLD = TB_SHADOW;
        EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO; // Sync down-stream module
        EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
        EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
        EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
        EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
        EPwm1Regs.AQCTLA.bit.CAU = AQ_SET; // set actions for EPWM1A
        EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;
        EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
        EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active Hi complementary
        EPwm1Regs.DBFED = 100; // FED = 20 TBCLKs
        EPwm1Regs.DBRED = 100; // RED = 20 TBCLKs
  // EPWM Module 2 config
        EPwm2Regs.TBPRD = EPwm_TBPRD; // Period = 900 TBCLK counts
        EPwm2Regs.TBPHS.half.TBPHS = EPwm_TBPRD; //
        EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Symmetrical mode
        EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Slave module
        EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;      // Clock ratio to SYSCLKOUT  //
HSPCLKDIV = (1 -- 0b000)
        EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;        // CLKDIV = (1 -- 0b000)
        EPwm2Regs.TBCTL.bit.PHSDIR = TB_DOWN; // Count DOWN on sync (=120 deg)
        EPwm2Regs.TBCTL.bit.PRDLD = TB_SHADOW;
        EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
        EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
        EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
        EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
        EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
        EPwm2Regs.AQCTLA.bit.CAU = AQ_SET; // set actions for EPWM2A
        EPwm2Regs.AQCTLA.bit.CAD = AQ_CLEAR;
        EPwm2Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
        EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active Hi Complementary
        EPwm2Regs.DBFED = 100; // FED = 20 TBCLKs
        EPwm2Regs.DBRED = 100; // RED = 20 TBCLKs
// EPWM Module 3 config
        EPwm3Regs.TBPRD = EPwm_TBPRD; // Period = 900 TBCLK counts
        EPwm3Regs.TBPHS.half.TBPHS = EPwm_TBPRD*0.5; // Set Phase register to zero
        EPwm3Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Symmetrical mode
        EPwm3Regs.TBCTL.bit.PHSEN = TB_ENABLE; // SLAVE module
        EPwm3Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;      // Clock ratio to SYSCLKOUT  //
HSPCLKDIV = (1 -- 0b000)
        EPwm3Regs.TBCTL.bit.CLKDIV = TB_DIV1;        // CLKDIV = (1 -- 0b000)
        EPwm3Regs.TBCTL.bit.PRDLD = TB_SHADOW;
        EPwm3Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
        EPwm3Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
        EPwm3Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
        EPwm3Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
        EPwm3Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
        EPwm3Regs.AQCTLA.bit.CAU = AQ_SET; // set actions for EPWM1A
        EPwm3Regs.AQCTLA.bit.CAD = AQ_CLEAR;
        EPwm3Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
        EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active Hi complementary
```

```
            EPwm3Regs.DBFED = 100; // FED = 20 TBCLKs
            EPwm3Regs.DBRED = 100; // RED = 20 TBCLKs
// EPWM Module 4 config
            EPwm4Regs.TBPRD = EPwm_TBPRD; // Period = 900 TBCLK counts
            EPwm4Regs.TBPHS.half.TBPHS = EPwm_TBPRD*0.5 + EPwm_TBPRD - 1; //
            EPwm4Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Symmetrical mode
            EPwm4Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Slave module
            EPwm4Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;       // Clock ratio to SYSCLKOUT  //
HSPCLKDIV = (1 -- 0b000)
            EPwm4Regs.TBCTL.bit.CLKDIV = TB_DIV1;         // CLKDIV = (1 -- 0b000)
            EPwm4Regs.TBCTL.bit.PHSDIR = TB_DOWN; // Count DOWN on sync (=120 deg)
            EPwm4Regs.TBCTL.bit.PRDLD = TB_SHADOW;
            EPwm4Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
            EPwm4Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
            EPwm4Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
            EPwm4Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
            EPwm4Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
            EPwm4Regs.AQCTLA.bit.CAU = AQ_SET; // set actions for EPWM2A
            EPwm4Regs.AQCTLA.bit.CAD = AQ_CLEAR;
            EPwm4Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
            EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active Hi Complementary
            EPwm4Regs.DBFED = 100; // FED = 20 TBCLKs
            EPwm4Regs.DBRED = 100; // RED = 20 TBCLKs

            EPwm1Regs.CMPA.half.CMPA = EPwm_TBPRD/2; // adjust duty for output EPWM1A
            EPwm2Regs.CMPA.half.CMPA = EPwm_TBPRD/2; // adjust duty for output EPWM2A
            EPwm3Regs.CMPA.half.CMPA = EPwm_TBPRD/2; // adjust duty for output EPWM1A
            EPwm4Regs.CMPA.half.CMPA = EPwm_TBPRD/2; // adjust duty for output EPWM2A
//=====================================================================
  //                  ePWM Setup (ADC SOC Trigger)
  // Triggers ADC at 250kHz

  // Configure ePWM6 for ADC SOC
            EPwm6Regs.ETSEL.bit.SOCAEN = 1;       // Enable SOC on A group
            EPwm6Regs.ETSEL.bit.SOCASEL = 4;      // Select SOC from time-based counter equal to
zero
            EPwm6Regs.ETPS.bit.SOCAPRD = 1;       // Generate pulse on 1st event

  // EPWM Module 6 config
            EPwm6Regs.TBPRD = EPwm_TBPRD*cycledelay; // Period = 900 TBCLK counts
            EPwm6Regs.CMPA.half.CMPA = 30;    // Set compare A value
            EPwm6Regs.TBPHS.half.TBPHS = (EPwm_TBPRD*cycledelay*0.5); //
            EPwm6Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Symmetrical mode
            EPwm6Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Slave module
            EPwm6Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;       // Clock ratio to SYSCLKOUT  //
HSPCLKDIV = (1 -- 0b000)
            EPwm6Regs.TBCTL.bit.CLKDIV = TB_DIV1;         // CLKDIV = (1 -- 0b000)
            EPwm6Regs.TBCTL.bit.PHSDIR = TB_DOWN; // Count DOWN on sync (=120 deg)
            EPwm6Regs.TBCTL.bit.PRDLD = TB_SHADOW;
            EPwm6Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
            EPwm6Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
            EPwm6Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
            EPwm6Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
            EPwm6Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
            EPwm6Regs.AQCTLA.bit.CAU = AQ_SET; // set actions for EPWM2A
            EPwm6Regs.AQCTLA.bit.CAD = AQ_CLEAR;
```

```
  // Action Qualifiers
            //EPwm6Regs.AQCTLA.bit.PRD = AQ_SET;
            EPwm6Regs.AQCTLA.bit.CAU = AQ_SET;
            EPwm6Regs.AQCTLA.bit.CAD = AQ_CLEAR;
            EPwm6Regs.TBCTL.bit.CTRMODE = 2;                    // count up mode

  // PID Constants
            Ts = cycledelay/PWMCARRIER;
            b0 = Kp*(1+N*Ts) + Ki*Ts*(1+N*Ts) + Kd*N;
            b1 = -(Kp*(2+N*Ts) + Ki*Ts + 2*Kd*N);
            b2 = Kp + Kd*N;
            a0 = 1+N*Ts;
            a1 = -(2+N*Ts);
            a2 = 1;
            A1 = -(a1/a0);
            A2 = -(a2/a0);
            B0 = b0/a0;
            B1 = b1/a0;
            B2 = b2/a0;


            EALLOW;
            SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
            EDIS;


       // Wait for ADC interrupt
            for(;;)
            {}

}


__interrupt void adc_isr(void)
{


//  GpioDataRegs.GPASET.bit.GPIO8 = 1;

  // Take ADC Measurements
  V_HV = (a = AdcRegs.ADCRESULT0>>4 , a = a * 0.1172161172);
  V_LV = (b = AdcRegs.ADCRESULT1>>4 , b = b * 0.0293);
  I_HV = (c = AdcRegs.ADCRESULT2>>4 , c = c - 2275 , c * 0.0164835165);
  I_LV = (d = AdcRegs.ADCRESULT3>>4 , d = d - 2275 , d * 0.0164835165);

  // Call PID controller
  //GpioDataRegs.GPASET.bit.GPIO8 = 1;
  PID();
  //duty = delta0 * PI_INV;
  //GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;



  // Load new phase values
  EPwm3Regs.TBPHS.half.TBPHS = delta0*PI_INV*EPwm_TBPRD; //
```

```
  EPwm4Regs.TBPHS.half.TBPHS = delta0*PI_INV*EPwm_TBPRD + EPwm_TBPRD - 1; //
  EPwm6Regs.TBPHS.half.TBPHS = (EPwm_TBPRD*cycledelay*0.5 + delta0*PI_INV*EPwm_TBPRD); //

  GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;


  //phase = delta0 * PI_INV * EPwm_TBPRD;
  // Reinitialize for next ADC sequence
  AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;         // Reset SEQ1
  AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;       // Clear INT SEQ1 bit
  PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;   // Acknowledge interrupt to PIE

  return;
}


void SystemStart()
{}

void PID()
{
        error0 = reference - V_HV;
        delta0 = A1*delta1 + A2*delta2 + B0*error0 + B1*error1 + B2*error2;
        if (delta0 >= PI*0.5)
        {
           delta0 = PI*0.5;
        }
        if (delta0 <= 0)
        {
           delta0 = 0;
        }
        error1 = error0;
        error2 = error1;
        delta1 = delta0;
        delta2 = delta1;
}
```

APPENDIX B – PLANAR TRANSFORMER SPECIFICATIONS

Functional specs

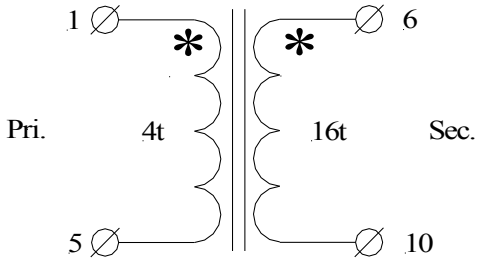
1. Generic Type	: T250-4-16.
2. Total output power range	: 2000W (380Vdc /5.5Adc). 4560W (380Vdc/12Adc - 95Vdc/48Adc)
3. Operating frequency of transformer	: 250 kHz.
4. Output ripple frequency	: 500 kHz
5. Input voltage of power stage	: 90 ÷ 100Vdc link.
6. Input voltage of transformer	: 95Vpeak, Bipolar Square waveform.
7. Topology	: Full Bridge, ZVT.
8. Operating duty cycle, max.	: 1.0
9. Volt-second product, max.	: 380V-μsec
10. Pri. Sec. ratio	: 4 : 16
11. Primary current, max (for 92% power supply effic.)	: 23Arms. – nominal output; 48Arms – overload.
12. Secondary current, max	: 5.5Arms. – nominal output; 12Arms – overload.
13. Dielectric strength	
(Pri. to Sec.)	: 1500Vdc.
(Pri., Sec. to Core)	: 1000Vdc.
14. Ambient temperature range	: -5 ÷ 45°C.
15. Estimated power losses	: 16W – nominal output; 40W – overload, continuous.
16. Estimated hot spot temperature **(with 60°C heat sink)**	: 90°C – nominal output; 130°C – overload, continuous.
17. Mechanical dimensions (for reference only)	: Length - 67 mm. : Width - 65 mm. : Height – 36 mm.

PAYTON 2000 W SMPS TRANSFORMER

Functional specs

Date : 10/08/15

Electrical diagram.



Terminals layout sketch (preliminary; side & top view; not to scale).