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Design of Integrated Current Reference Circuits for a 180-nanometer BICMOS Silicon Process

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DESIGN OF INTEGRATED CURRENT REFERENCE CIRCUITS FOR A 180-NANOMETER BICMOS SILICON PROCESS

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Distinguished Professor of Electrical Engineer

ABSTRACT

The goal of this thesis is to provide design analysis, simulation results, and physical layout structure for three current references that are to be physically fabricated in a 180-nanometer BICMOS silicon process. The report briefly discusses the need for voltage and current references in analog circuit applications, before zooming in to examine three topologies being tailored to the needs of an integrated solar micro-inverter system. These topologies are: proportional to absolute temperature (PTAT), complementary to absolute temperature (CTAT), and constant across temperature (Constant) bias circuits. First, each topology is designed schematically to meet the needs of the micro-inverter system. Those schematics are then taken in turn through simulations in Cadence Virtuoso. These simulations return successful results showing functionality throughout temperature and power supply variation, as well as system startup. Finally, the circuits are laid out in Virtuoso's layout package, utilizing common-centroid layout schemes and process parasitic simulations. The circuits are fully prepared for fabrication.

ACKNOWLEDGEMENTS

First, I would like to acknowledge Dr. Mantooth, my thesis advisor, for his pivotal aid in my honors research experience, my classroom education, and the preparation of this honors thesis. I must also thank Ashfaqur Rahman. He has been an exceptional mentor during this project, both in direction and in patience.

Next, I could not complete this work without acknowledging my parents, Tony and Misty Megee, for their prayer, encouragement, and counsel throughout my honors undergraduate career.

Finally, I give highest acknowledgement and praise to my Lord and Savior Jesus Christ. He is my King of glory.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

I. INTRODUCTION

A. Problem: Integrated Circuit Solar Micro-inverter

Many electronic circuits and devices, from individual transistors to operational amplifiers, rely upon a DC operating point in order to function properly. This operating point is often established and maintained through the use of a reference circuit. Such reference circuits provide either a voltage profile, a current profile, or both that fulfill the requirements of the other circuit or device. Such manipulation of voltage and current profiles for references in other circuits is called DC biasing. DC biasing is an important component to both individual block design, and system level design within integrated circuits, since it contributes to the overall power consumption of the system.

The system being examined in this thesis is an integrated micro-inverter. Three main circuit blocks make up the micro-inverter: Power Supply, Gate Driver, and Mixed Signal. Within these blocks, many individual circuits depend upon proper current biasing.

B. Thesis Statement

The goal of this applied project is to design robust current reference circuits for a 180-nanometer Dongbu BiCMOS process in silicon. Three current-temperature profiles are designed in order to provide proper current biasing to other blocks within a multi-chip integrated solar micro-inverter system. These reference circuits are simulated using Cadence Virtuoso design tools. Experimental results will be aquired at a later date.

C. Organization of Thesis

Five headings divide the body of this thesis report. First, the Introduction provides the project definition and thesis statement. Second, the Schematic Design section identifies the circuit topologies and their designs in order to meet project's goal. Next, the paragraphs under the Circuit Simulations heading describe the schematic simulation results of the reference topologies. The penultimate heading, Cadence Layout and Parasitic Simulations, gives similar simulation procedures and results for the physical layout stage of the project. Finally, the Conclusion section summarizes the thesis report and highlights the future work needed to bring the project to full completion.

II. SCHEMATIC DESIGN

The following section provides the design theory behind the three types of current references designed. First, the circuit specifications are given. Next, each topology providing a unique current reference profile is discussed in its basic form. Finally, practical additions to the basic topologies that are tailored to the needs of the project are discussed.

A. Circuit Specifications

Each current reference is designed to output less than 50 μA. This specification exists in order to limit power consumption, and a small current can later be mirrored to other blocks in the system. Furthermore, the Constant current reference must not fluctuate by more than 2% across a supply voltage variation of ±10%. This is the target PSRR range for the other topologies as well.

B. Circuit Topologies

Two circuit topologies are employed to meet the current biasing requirements of the system. Each topology offers a unique current profile for use as reference. These profiles are: proportional to absolute temperature (PTAT), complementary to absolute temperature (CTAT). These two topologies are then combined for the constant to temperature current reference. All current references are designed to operate functionally across temperatures from -40° to 125 °C. Also, each reference should ideally output less than 20 to 30 μA of current before being mirrored to other blocks in the micro-inverter system. Finally, the topologies being presented in this thesis report are non-isolated: they require no isolation layer in silicon.

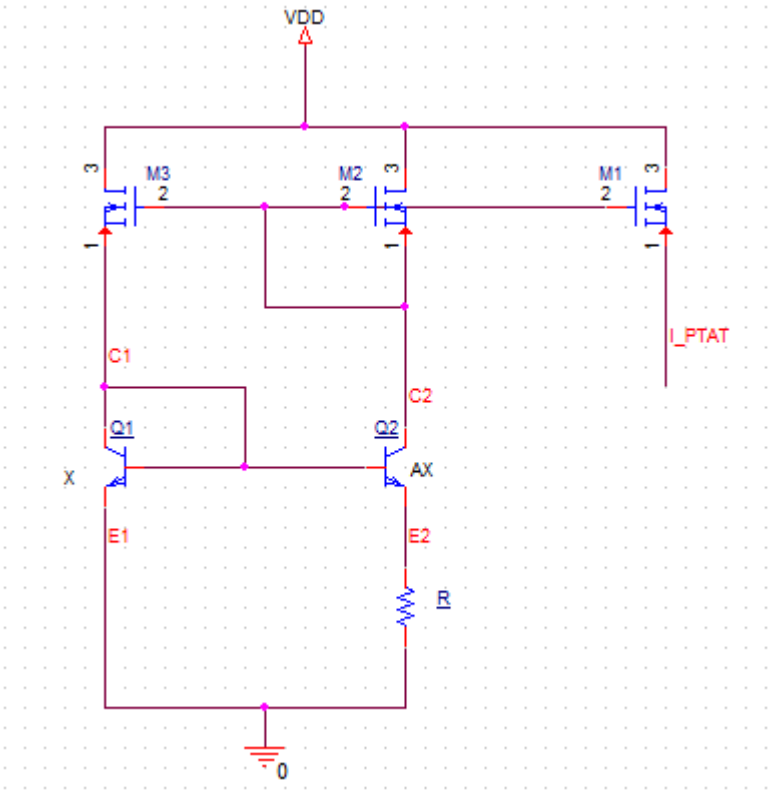


Figure 1: Basic PTAT Cell

1. Proportional to Absolute Temperature (PTAT)

Figure 1 shows the basic PTAT cell. As shown, the PTAT output results from a difference of base-emitter voltages in two Bipolar Junction Transistors (BJTs). The following analysis of the basic PTAT cell is cited from Rincon-Mora's text on Voltage References (Rincon-Mora, 2001). Applying Kirchhoff's Voltage law to Q1, Q2, and resistor R of Figure 1,

$$I_{C2}R + V_{BE2} = V_{BE1} \tag{1}$$

The base-emitter voltage of any BJT follows a logarithmic relationship, as seen in Equation 2:

$$V_{BE} = V_T \ln\left(\frac{I_C}{J_S * Area}\right), \tag{2}$$

where V_T is the thermal voltage and J_s is a BJT P-N junction constant. Substituting for V_{BE} in Equation 1 gives,

$$I_{C2} = \frac{1}{R}(V_{BE1} - V_{BE2}) = \frac{V_T}{R}\ln(\frac{I_{C1}Ax}{I_{C2}x}), \quad (3)$$

where x and Ax are the areas of *Q1* and *Q2*, respectively. Since the two BJTs are connected with the MOSFETs as a current mirror, then Equation 3 subsequently yields,

$$\frac{kT}{qR}\ln(A) = \frac{\Delta V_{BE}}{R} \equiv I_{PTAT}, \quad (4)$$

where k and q are fundamental constants, and T is absolute temperature in Kelvin. Thus, the output current is shown to be directly and linearly proportional to absolute temperature.

2. Complementary to Absolute Temperature (CTAT)

The basic CTAT cell being used for the project is shown in Figure 2. Once again, Rincon-Mora states, "The output current (ICTAT) is described as

$$I_{out} = \frac{V_{BE}}{R} \equiv I_{CTAT}, \quad (5)$$

where V_{BE} is the base-emitter (diode) voltage across transistor *qn*. Sink current I_x can be designed to be any value as long as it is greater in magnitude than I_{CTAT} throughout the whole operating temperature range" [2]. Thus the CTAT cell provides current that is indirectly and linearly proportional to absolute temperature.

For the references used in the project, I_x is a PTAT cell. It provides proper biasing to the CTAT reference. This further illustrates the need for DC biasing in electronic circuits. In this case, one reference circuit is used to provide DC biasing to another reference circuit.

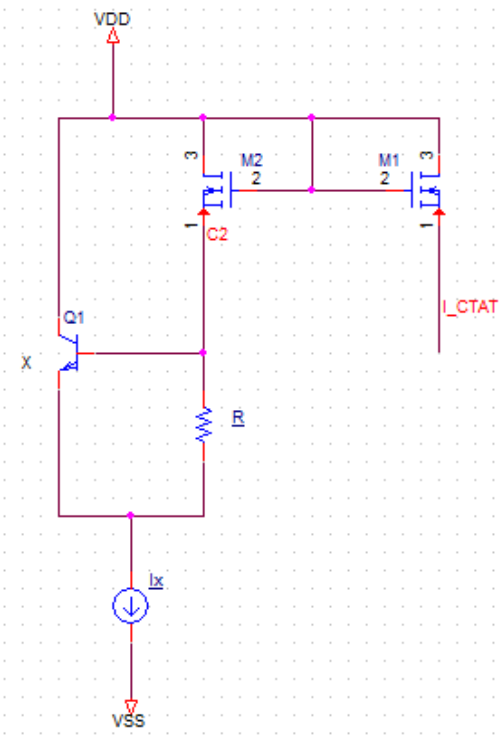


Figure 2: Basic CTAT Cell

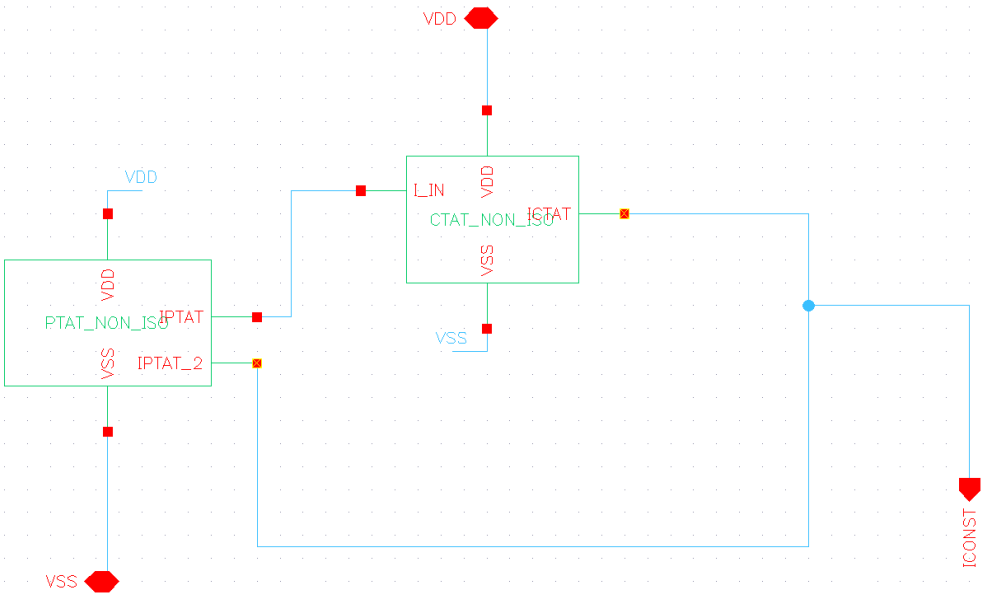


Figure 3: Basic Constant Cell

3. Constant Current Reference

The constant current reference, in this application, is constructed simply by adding the PTAT and CTAT branch currents together. Schematic level simulations are done to find a proper balance between the branch currents. Figure 3 on the previous page displays the basic Constant reference cell.

C. Additions to Basic Cells

Three major additions to the basic cells are described below. Each addition addresses common system level issues with the reference circuits. Since the basic PTAT cell is used throughout all three topologies, each addition is made solely to the PTAT cell. Each subsequent topology is then affected by the presence of the update PTAT reference.

1. Startup

The first system level issue with reference circuits is startup. The differential equations governing the operation of the PTAT cell have two particular solutions, one of which is zero. As Rancon-Mora states, "The current generators […] have an additional stable operating point, which is when I_{PTAT} is zero. A startup circuit (not shown) is required to prevent them from settling in this undesired state" [2]. Without this circuit, the PTAT reference can simply settle into this zero state when the system is first powered up.

The startup circuit implemented for this project adds MOSFETs to draw a small amount of current constantly off of the collector of Q1. Thus the circuit is never allowed to operate in a zero state.

2. Power Supply Rejection Ratio (PSRR)

The second system level issue involves PSRR. Generally, the basic cells described above possess low PSRR, and therefore their outputs overly fluctuate with a small change in V_{DD}. Since these reference circuits are to be the baseline for other blocks of the system, they need to be less susceptible to changes in power supply. In order to mitigate this issue, a differential amplifier was added to the PTAT basic cell. This diff-amp provides voltage bias to the mirrors of the base voltage of the BJTs, and significantly increases the PSRR of each reference circuit.

3. Power Consumption

Power consumption is always an issue in integrated circuits. Current and thus power consumption is kept below 50 μA per reference to meet the power consumption requirements of the power supply and regulators on chip. An additional branch of cascoded MOSFETs and series resistors is added draw current away from the reference and reduce the overall power consumption of the unit.

The final schematic for the PTAT is shown in Figure 4. The branch for the diff-amp, the diff-amp for PSRR, and the startup branch are shown from right to left across the figure. The basic cell and two mirrored outputs are displayed on the far right.

4. Putting It All Together

Aside from the system level additions, some practical changes are also made to the basic cell. As shown in Figure 4 below, each current mirror is a cascode current mirror. This increases the output resistance of each mirror, and contributes somewhat to the PSRR [1]. Since

the voltage supply is 5 V, there exists enough room in the circuit for the reduction in voltage swing brought by the cascode mirrors.

Second, each reference current is produced from a voltage across a resistor. This resistor is ideally temperature independent. This task can be difficult to accomplish with real process resistors, however. In order to tackle this issue, two process resistors were matched for their temperature coefficients in such a way that their series combination would produce an equivalent, nearly temperature independent resistor. Therefore, Figure 4 shows two matched process resistors in place of the one resistor for the basic PTAT cell.

Schematic design for the project is complete. The following section describes the simulation process in Cadence Virtuoso and its results.

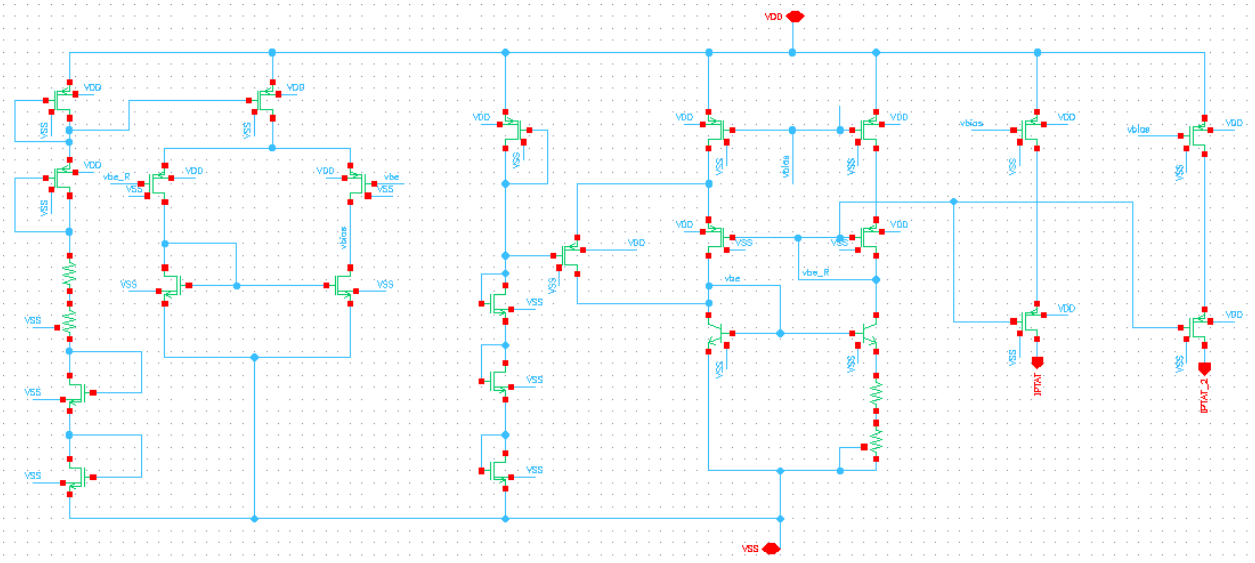


Figure 4: PTAT Non-Isolated Schematic

III. CIRCUIT SIMULATIONS

Each circuit schematic described above is taken in turn through cadence simulations. Each is subjected to a temperature sweep from -39° to 125 °C. Each circuit is also tested for PSRR by sweeping the power supply across a ±10% range (from 4.5 V to 5.5 V). Finally, startup simulation results are included for the PTAT and CTAT topologies.

Although the Dongbu 180 nm allows for isolated devices and circuits, the circuits describes here use an npn transistor that cannot be used in an isolated well. Hence these circuits must be built on the silicon substrate and cannot be isolated for higher voltage applications.

A. PTAT Non-isolated

Figure 4 from the previous section displays the final virtuoso schematic for the non-isolated PTAT generator. This circuit mirrors its output to provide two output currents. Figure 5 delivers simulation results for this circuit for DC response across operating temperature (-39° to 125 °C). As shown, each output branch supplies a current profile that is linearly and directly proportional to temperature. One output produces 13.6 μA of current at 25 °C, and the other output produces 5 μA of current at 25 °C.

Each current-temperature curve exhibits an R^2 value greater than .999. Also, currents produced at the extremes (-39° and 125° C) differ by less than 1% from currents predicted by an extrapolated linear regression generated from normal operating temperatures.

As shown in Figure 6, a PSRR simulation of the non-isolated PTAT generator results in a robust response for both outputs. Across temperature, the reference circuit's maximum PSRR is 2.9% for both outputs.

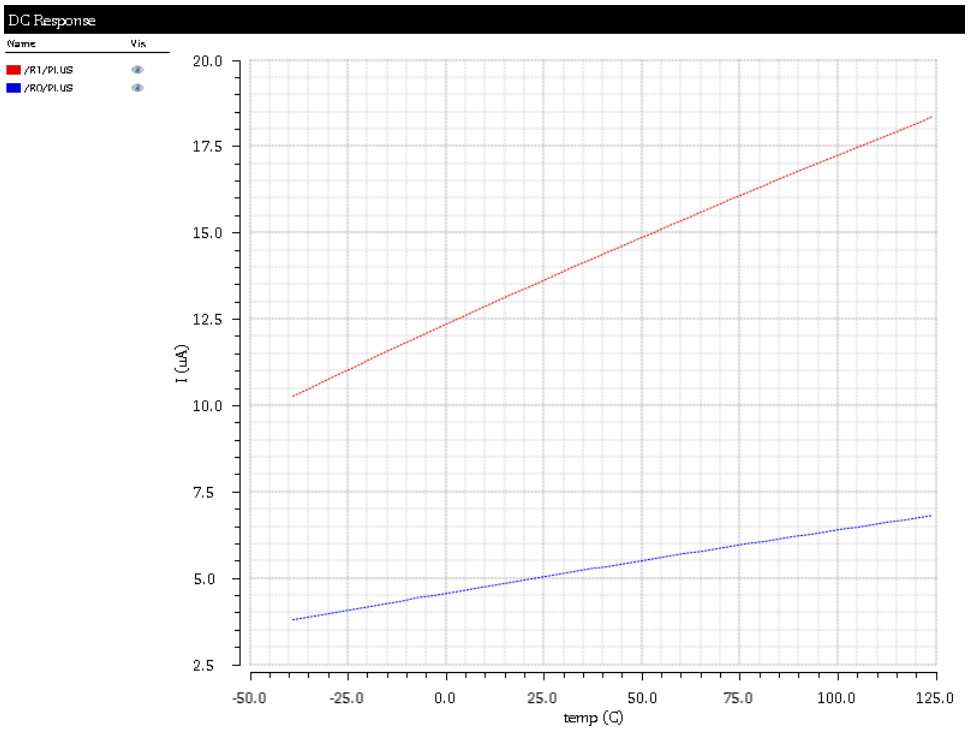


Figure 5: PTAT Non-Isolated Temperature Sweep

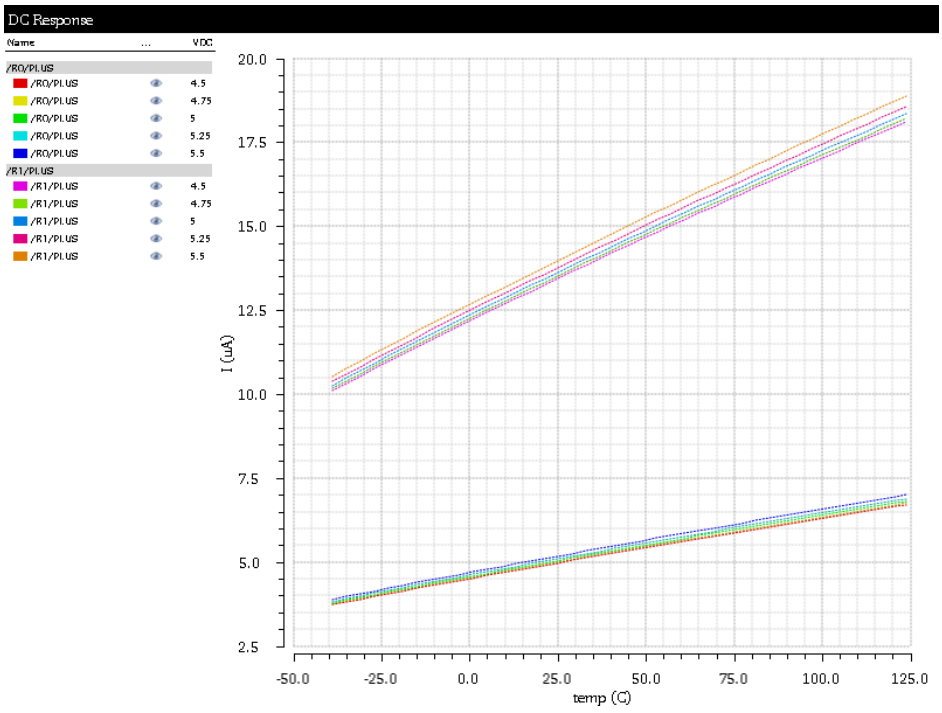


Figure 6: PTAT Non-Isolated VDD Sweep

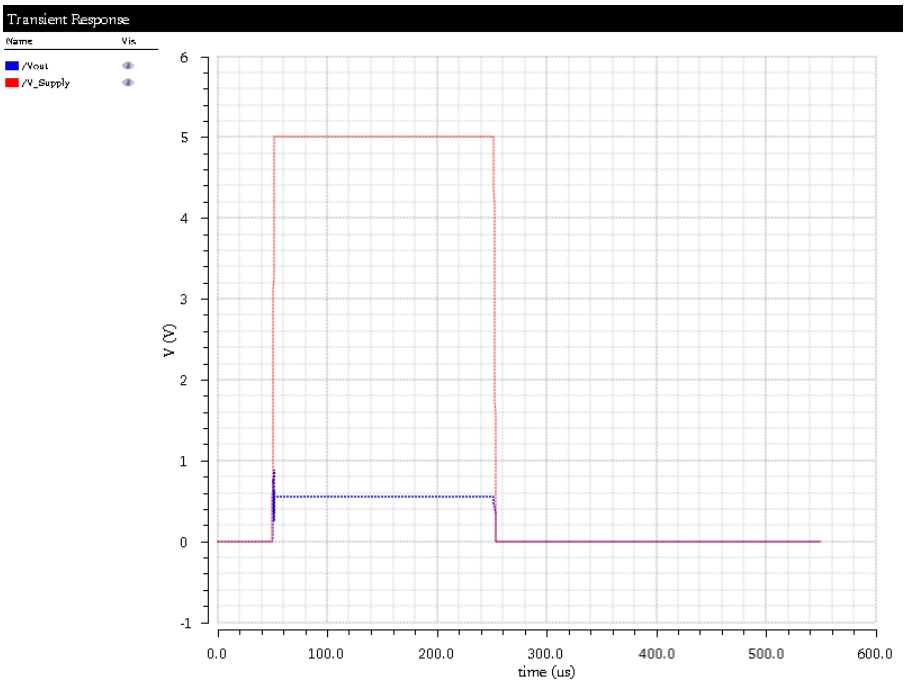


Figure 7: PTAT Non-Isolated Startup

The final simulation for startup is shown in Figure 7. It indicates successful startup for the PTAT non-isolated reference.

B. CTAT Non-isolated

The CTAT schematic designed as a non-isolated reference is shown in Figure 8. Figure 9 and Figure 10 give the DC simulation results. The temperature sweep indicates that the reference circuit functions properly. It adequately provides an inversely linear relationship between current and temperature, with a room temperature (25 °C) output of 7.5 µA. After analysis of the simulation results, the circuit's current-temperature curve possesses an R^2 value of 0.998, and it has a maximum error of 2.5% at temperature extremes when compared against extrapolated regression.

The VDD sweep also contributes robust results. The maximum change in output current over a 20% supply voltage swing is 1.9%. Finally, the startup simulation, shown in Figure 11, indicates a successful steady station condition for the CTAT reference.

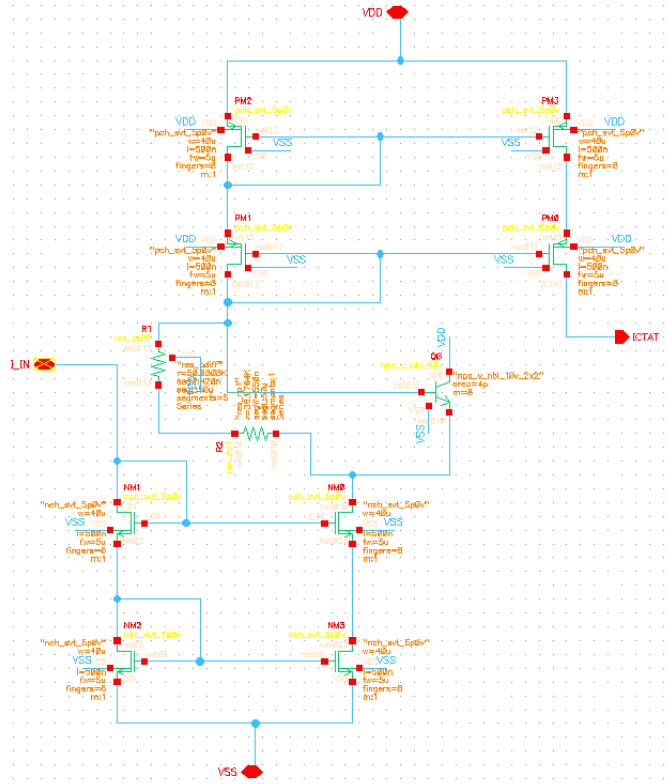


Figure 8: CTAT Non-Isolated Schematic

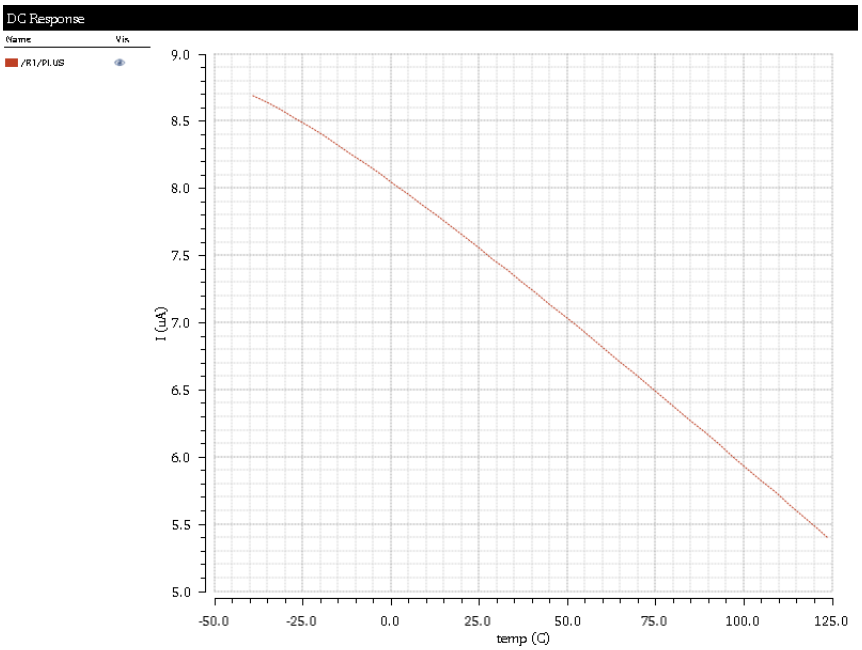


Figure 9: CTAT Non-Isolated Temperature Sweep

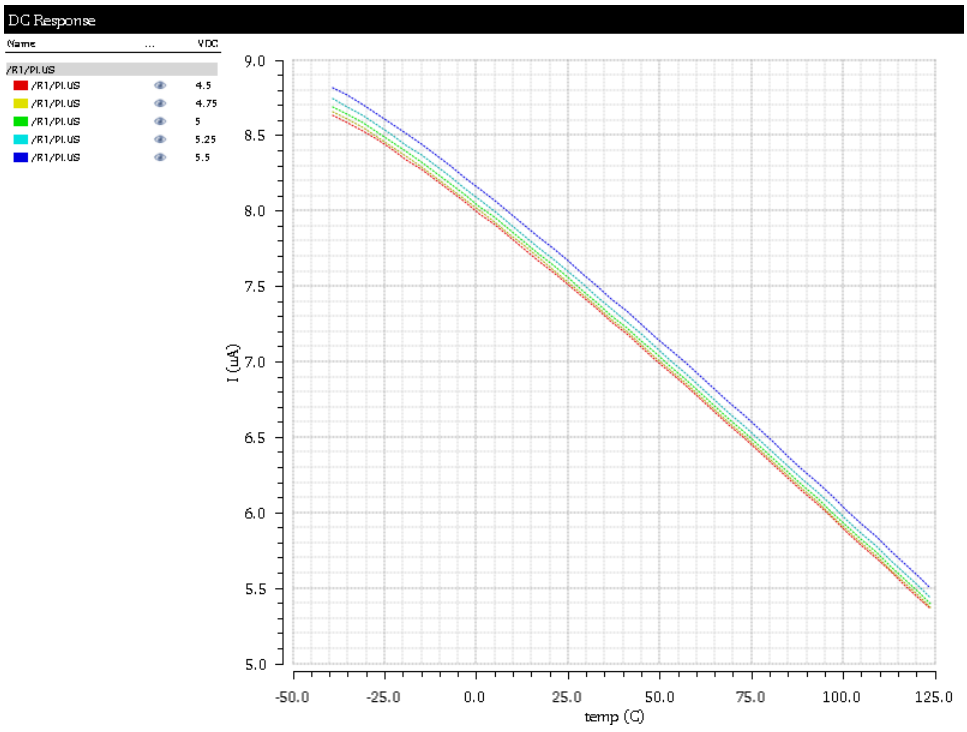


Figure 10: CTAT Non-Isolated VDD Sweep

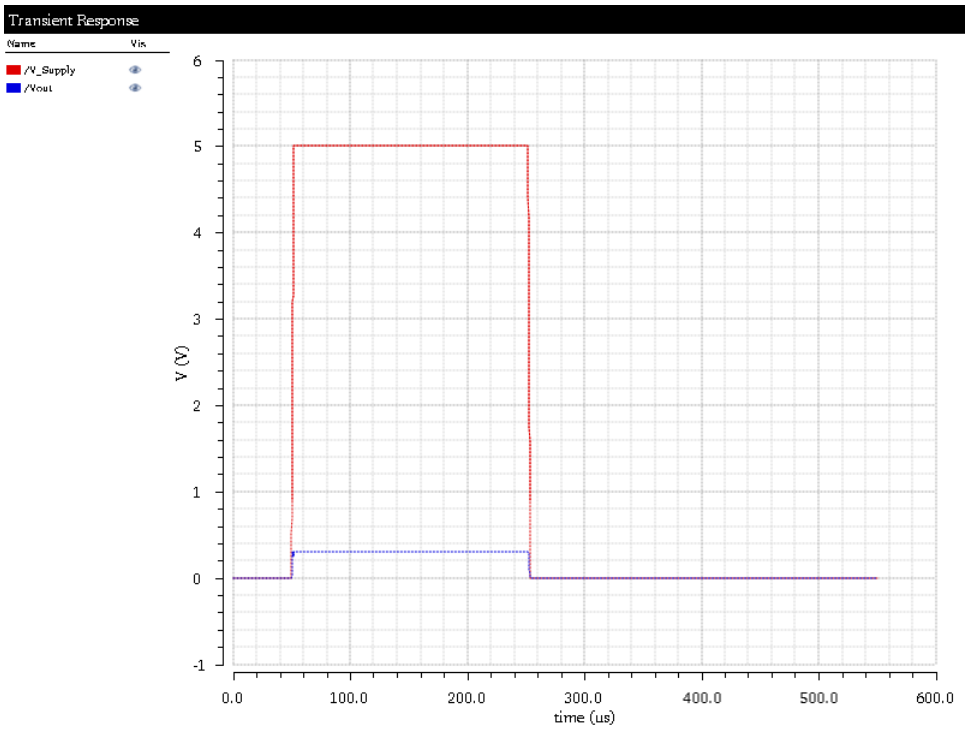


Figure 11: CTAT Non-Isolated Startup

C. Constant Non-isolated

The constant current reference shown in Figure 12 is the last schematic needed for the system's requirements. As shown, the reference circuit supplies constant current via combination of PTAT and CTAT currents. A mirroring stage, designed by Ashfaqur Rahman, is added between PTAT and CTAT blocks to correctly bias the CTAT block and to output extra PTAT currents as needed. The constant output is simply the addition of PTAT and CTAT output branches.

Figure 13 displays the temperature sweep results for the non-isolated constant current reference. Across the entire temperature range, the reference varies its output current by only 0.44 μA. This is less than ±2% variation.

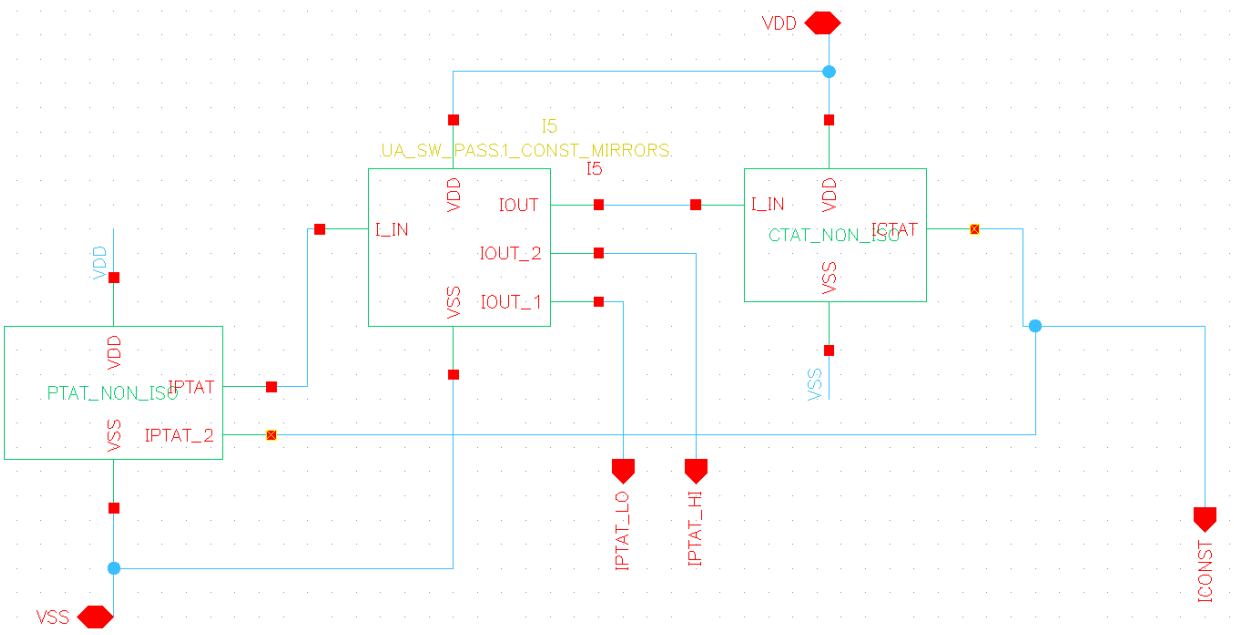


Figure 12: Constant Non-Isolated Schematic

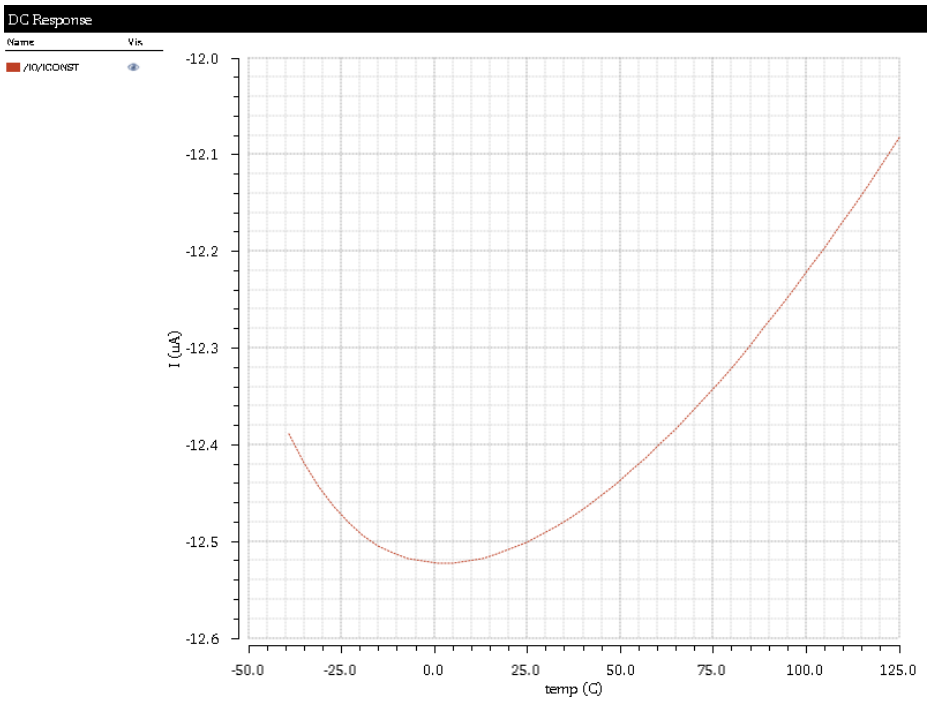


Figure 13: Constant Non-Isolated Temperature Sweep

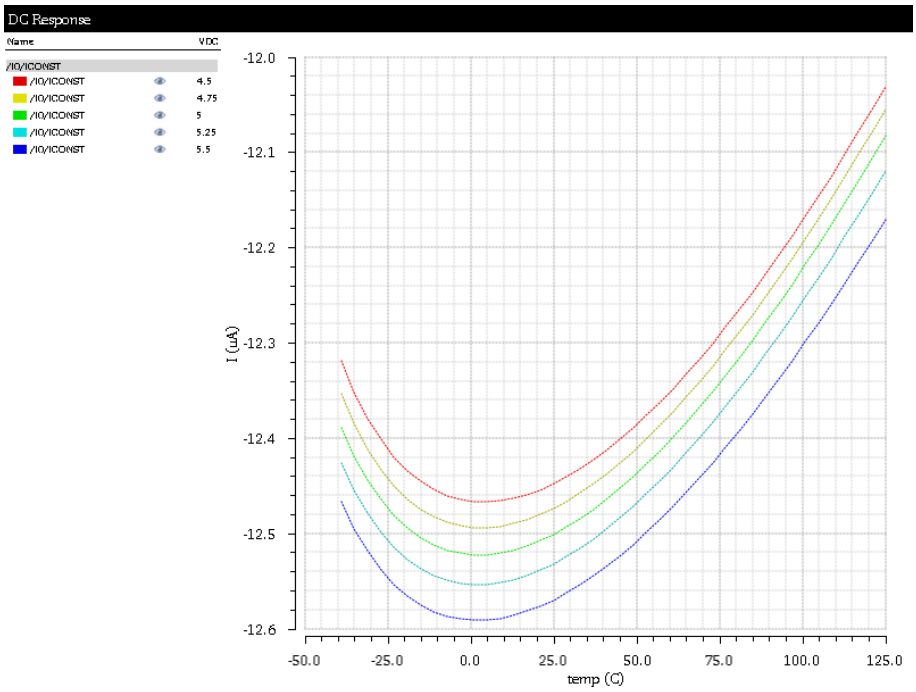


Figure 14: Constant Non-Isolated VDD Sweep

The power supply sweep in Figure 14 also returns positive results for the constant current reference. At -10% supply voltage, or 4.5 V, the output only drops at the lowest by 0.6%. At the +10%, or 5.5 V, the output only rises by 0.7%.

The simulation results show that the PTAT and CTAT current reference circuits slightly missed their target of less than 2% variation across V_{DD} sweep. However, when they are combined into the Constant reference, the specification is met perfectly. All current references also operate at currents less than 50 µA, meeting the power consumption spec.

IV. CADENCE LAYOUT AND PARASITIC SIMULATIONS

The following section provides the cadence layout results for the current references. First, it describes the layout process, including some layout design considerations as well as simulations and checks run on each reference topology. Then, it gives the final layout for each circuit that is sent to fabrication. As stated earlier in the introductory section, this is the most recent stage of the project, and physical testing is to be provided at a later date.

A. Design Considerations for Layout

Layout of integrated circuits is a process usually constrained by space, speed, and power. For the reference circuits under scrutiny, the speed of the circuit becomes a nonissue as long as steady state is reach. The space constraint of the entire project is also quite generous, so latitude is available in the layout to allow extra space for the circuit to perform well at the desired power level. Thus the layouts are designed with extra wire width and extra vias throughout the layout.

Second, in order to increase the matching of the mirroring transistors, and to decrease the process variation in their fabrication, common-centroid layout is implemented for the cascode current mirrors and the diff-amps. Common-centroid layout uses inter-digitation of MOS fingers and array symmetry of devices in order to minimize the space between the centroids of the matched devices [3]. In this way, the reference circuits are built in Cadence using two layers of metal for interconnecting wires.

B. Layout Checks and Simulations

Four process checks and simulations are run on a typical layout in Cadence. First, a design rule check (DRC) is run. This check compares the layout against the design rules for the Dongbu fabrication process. If any rules or recommendations are broken, the DRC returns an error or a warning, respectively, and highlights the mistake in the layout. Figure 15 below shows a return report from a DRC for the PTAT non-isolated reference.

Second, a layout-versus-schematic (LVS) comparison is run. This check simply compares and contrasts what is built in the schematic window to what is built in the layout window. It checks wire connections, labels, external pins, and device sizes to make sure that the physical fabrication will return the desired circuit. Again, this check returns a report. An example of a successful LVS report is shown in Figure 16 on the next page.

Third, a parasitic extraction (PEX) simulation is run. PEX takes a look at the parasitics intrinsic to any physical layout, and then adds these extra parameters to the schematic simulations previously completed, and runs them again. The layouts used in this project are subjected to a PEX including parasitic resistances and capacitances. Parasitic inductance is ignored for now. An example of a successful PEX report for the PTAT is included in Figure 17.

All reference layouts possess successful DRC, LVS, PEX, and corner simulations. The next subsection provides the final layouts for the project.

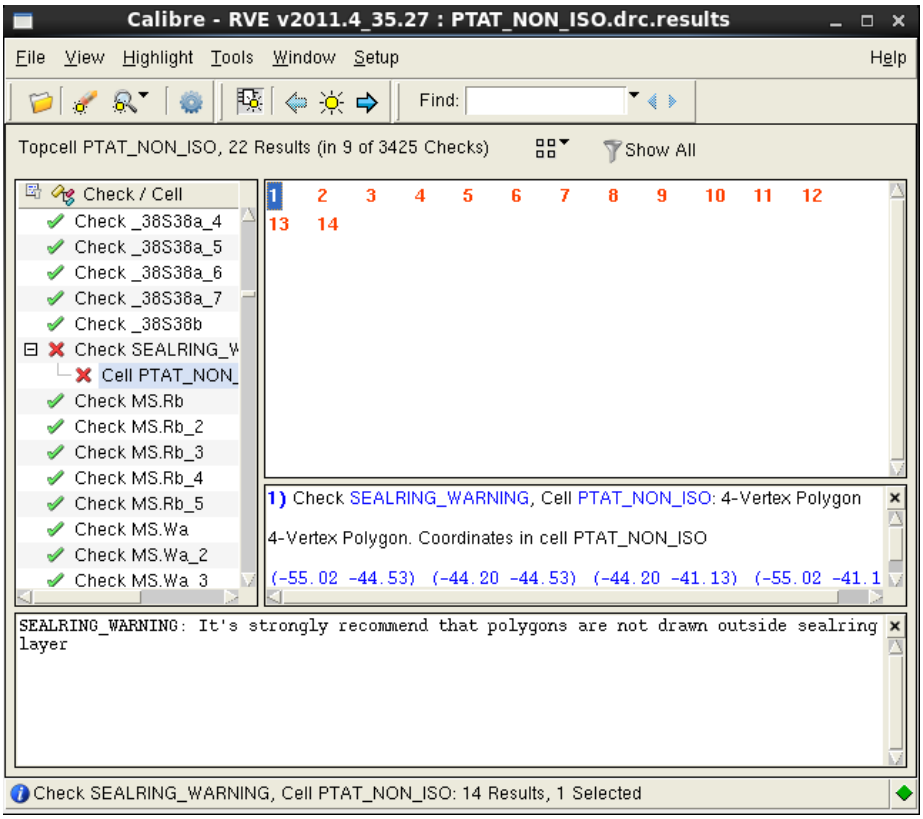


Figure 15: DRC Example For PTAT

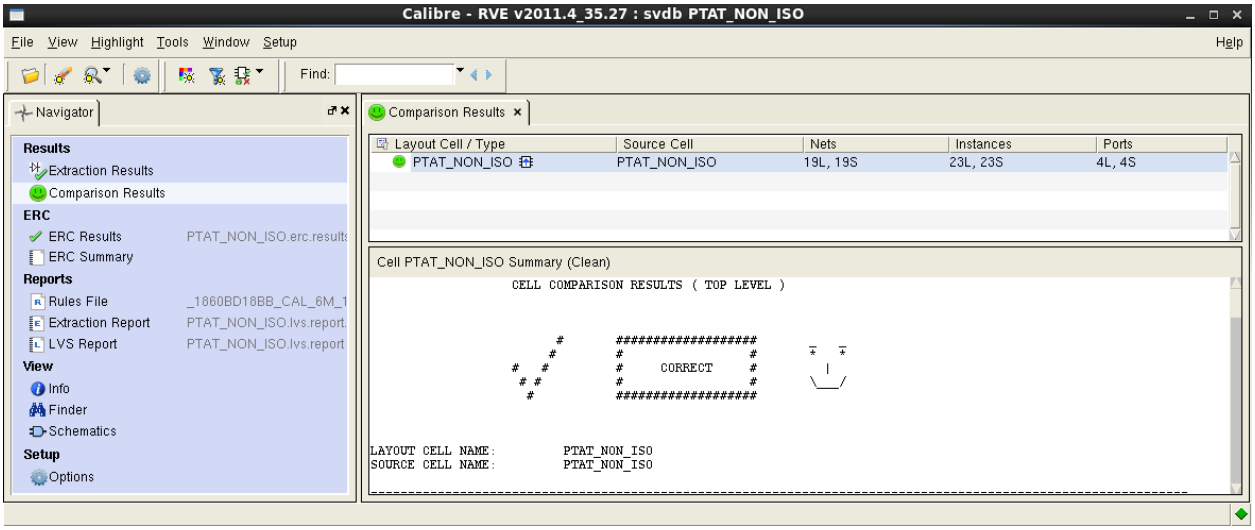
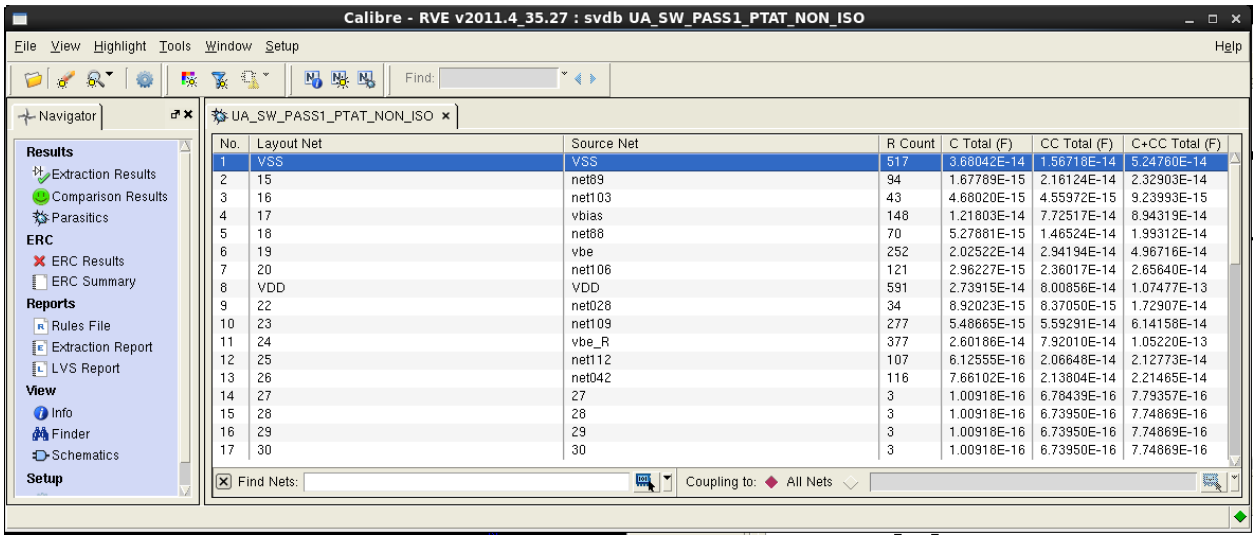


Figure 16: LVS Example For PTAT



No.	Layout Net	Source Net	R Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	VSS	VSS	517	3.68042E-14	1.56718E-14	5.24760E-14
2	15	net89	94	1.67789E-15	2.16124E-14	2.32903E-14
3	16	net103	43	4.68020E-15	4.55972E-15	9.23993E-15
4	17	vbias	148	1.21803E-14	7.72517E-14	8.94319E-14
5	18	net88	70	5.27881E-15	1.46524E-14	1.99312E-14
6	19	vbe	252	2.02522E-14	2.94194E-14	4.96716E-14
7	20	net106	121	2.96227E-15	2.36017E-14	2.65640E-14
8	VDD	VDD	591	2.73915E-14	8.00856E-14	1.07477E-13
9	22	net028	34	8.92023E-15	8.37050E-15	1.72907E-14
10	23	net109	277	5.48665E-15	5.59291E-14	6.14158E-14
11	24	vbe_R	377	2.60186E-14	7.92010E-14	1.05220E-13
12	25	net112	107	6.12555E-16	2.06648E-14	2.12773E-14
13	26	net042	116	7.66102E-16	2.13804E-14	2.21465E-14
14	27	27	3	1.00918E-16	6.78439E-16	7.79357E-16
15	28	28	3	1.00918E-16	6.73950E-16	7.74869E-16
16	29	29	3	1.00918E-16	6.73950E-16	7.74869E-16
17	30	30	3	1.00918E-16	6.73950E-16	7.74869E-16

Figure 17: PEX Example for PTAT

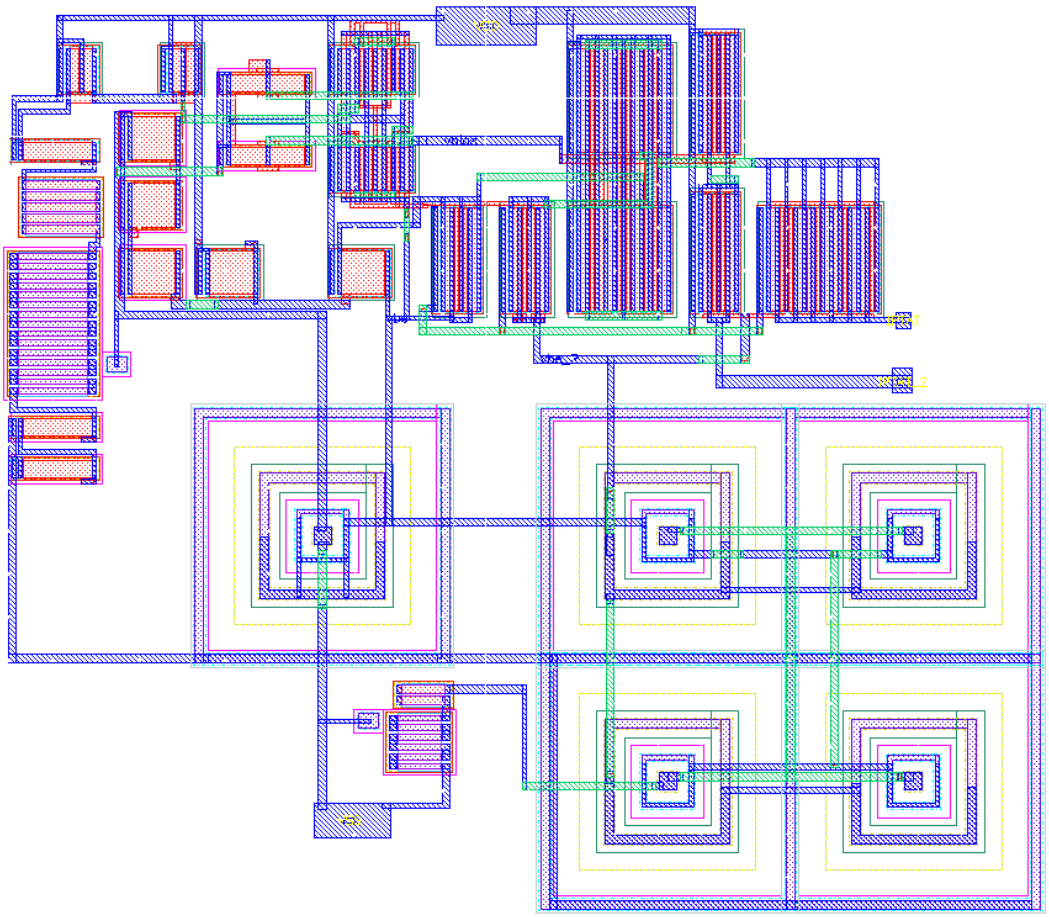


Figure 18: PTAT Non-Isolated Layout

C. Final Cadence Layouts

Figures 18-20 give the final layouts for the PTAT, CTAT, and Constant current references. As can be seen the BJTs take up the most space in each circuit. Each current mirror and differential amplifier is compiled using common-centroid layout as described above. Having thoroughly examined the schematics and their simulations, the final step before fabrication is complete for this block of the micro-inverter chip.

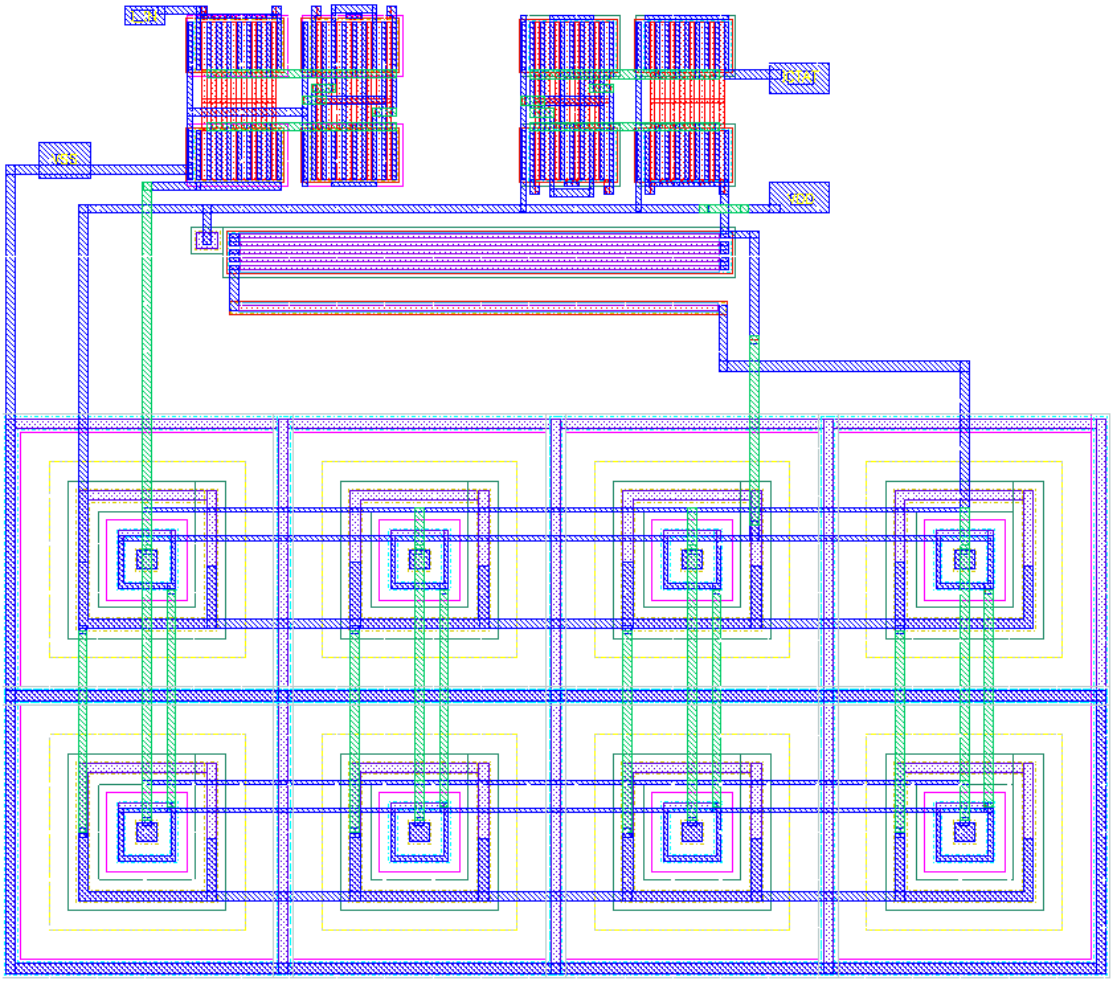


Figure 19: CTAT Non-Isolated Layout

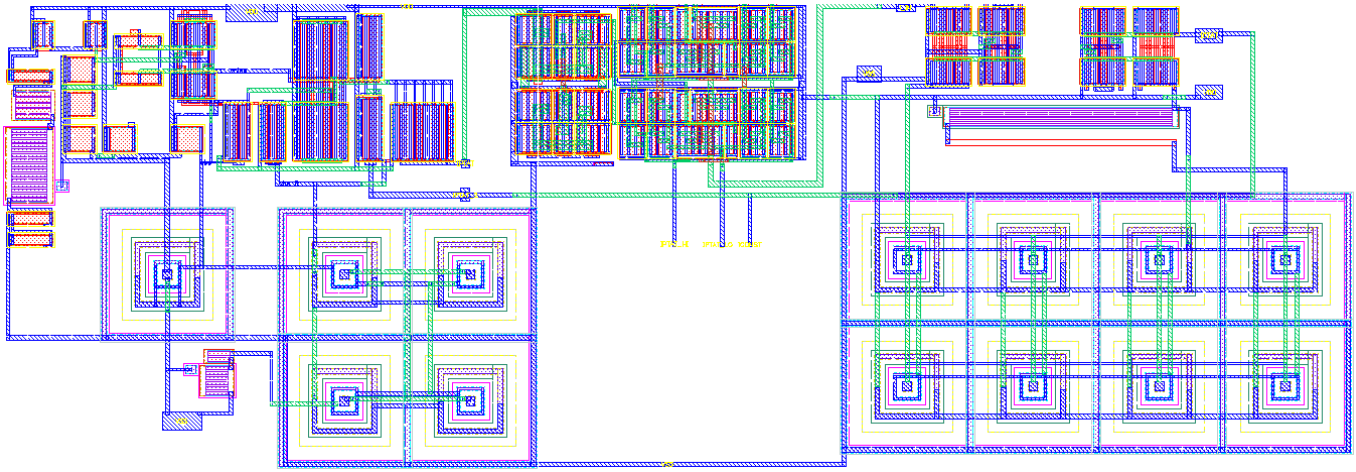


Figure 20: Constant Non-Isolated Layout

V. CONCLUSION

The current references presented in this thesis are fully developed from design to schematic to layout. In the design stage, the basic circuit cells have been described, along with their practical adaptations and additions to conform to the requirements of the micro-inverter system. At the simulation stage, these schematics were analyzed for functionality across temperature, power supply, and system startup. Finally, in the circuit layout phase, the physical images of the circuits took shape through common-centroid layout and parasitic simulations. Thus, the goals of this thesis project have been successfully met. The designs are shown to meet specifications through post-layout simulations. The final stage for these current references is fabrication in a 180-nanometer silicon process. At the date of submission of this thesis, fabrication has been accomplished, but time constraints disallowed the inclusion of experimental test data into the thesis report.

VI. APPENDIX A: REFERENCES

[1] Smith Sedra, *Microelectronic Circuits*, 6th ed. New York, United States of America: Oxford University Press, 2006.

[2] Rincon-Mora, *Voltage References: From Diodes to Precision High-Order Bandgap Circuits*.: Wiley-IEEE Press, 2001.

[3] Alan Hastings, *The Art of Analog Layout*, Marcia Horton, Ed. Upper Saddle River, New Jersey, United States of America: Prentice Hall, 2001.

VII. APPENDIX B: SIMULATED TABULAR DATA

Table 1: PTAT Raw Temperature Sweep Data

temp (°C)	R0:1 (µA)	R1:1 (µA)
-39	3.78	10.3
-35	3.86	10.5
-31	3.95	10.7
-27	4.03	10.9
-23	4.11	11.1
-19	4.19	11.4
-15	4.27	11.6
-11	4.35	11.8
-7	4.42	12.0
-3	4.50	12.2
1	4.58	12.4
5	4.66	12.6
9	4.73	12.8
13	4.81	13.0
17	4.89	13.2
21	4.96	13.4
25	5.04	13.6
29	5.11	13.8
33	5.19	14.0
37	5.26	14.2
41	5.33	14.4

temp (°C)	R0:1 (µA)	R1:1 (µA)
45	5.41	14.6
49	5.48	14.8
53	5.55	15.0
57	5.63	15.2
61	5.70	15.4
65	5.77	15.6
69	5.84	15.8
73	5.92	16.0
77	5.99	16.2
81	6.06	16.4
85	6.13	16.5
89	6.20	16.7
93	6.27	16.9
97	6.34	17.1
101	6.41	17.3
105	6.48	17.5
109	6.55	17.7
113	6.61	17.8
117	6.68	18.0
121	6.75	18.2
124	6.80	18.3

Table 2: CTAT Raw Temperature Sweep Data

temp (°C)	R1:1 (μA)
-39	8.69
-35	8.64
-31	8.58
-27	8.52
-23	8.46
-19	8.39
-15	8.32
-11	8.25
-7	8.18
-3	8.10
1	8.03
5	7.95
9	7.87
13	7.80
17	7.72
21	7.63
25	7.55
29	7.47
33	7.39
37	7.31
41	7.22

temp (°C)	R1:1 (μA)
45	7.14
49	7.05
53	6.97
57	6.88
61	6.79
65	6.71
69	6.62
73	6.53
77	6.45
81	6.36
85	6.27
89	6.18
93	6.09
97	6.00
101	5.91
105	5.82
109	5.73
113	5.64
117	5.55
121	5.46
124	5.40

Table 3: Constant Raw Temperature Sweep Data

temp (°C)	I0:1 (µA)
-39	-12.4
-35	-12.4
-31	-12.4
-27	-12.5
-23	-12.5
-19	-12.5
-15	-12.5
-11	-12.5
-7	-12.5
-3	-12.5
1	-12.5
5	-12.5
9	-12.5
13	-12.5
17	-12.5
21	-12.5
25	-12.5
29	-12.5
33	-12.5
37	-12.5
41	-12.5

temp (°C)	I0:1 (µA)
45	-12.5
49	-12.4
53	-12.4
57	-12.4
61	-12.4
65	-12.4
69	-12.4
73	-12.4
77	-12.3
81	-12.3
85	-12.3
89	-12.3
93	-12.3
97	-12.2
101	-12.2
105	-12.2
109	-12.2
113	-12.2
117	-12.1
121	-12.1
125	-12.1