5-2014

Characterization and Model Verification of SiC CMOS Transmisison Gates

Andrew H. Taylor
University of Arkansas, Fayetteville

Characterization and Model Verification of SiC CMOS Transmission Gates

An Undergraduate Honors College Thesis

in the

Department of Electrical Engineering
College of Engineering
University of Arkansas
Fayetteville, AR

by

Andrew H. Taylor

April 25, 2014

Andrew Taylor

This thesis is approved.

Thesis Advisor:

_____

Thesis Committee:

_____

_____

ABSTRACT

The aim of this thesis is to present and explore the results of a method for characterizing CMOS transmission gates in an IC design process, as well as to describe their importance in circuit design. The method applies to any fabrication process, but the work for this thesis was conducted in a silicon-carbide process, in the first round of fabrication. The first section covers basic information regarding transmission gates, as well as showing their value in circuit design. Secondly, the design, simulation, and implementation of the characterizing test structures is detailed. The third section delineates the test setup and procedures for evaluating physical device performance, and analyzes the results obtained. Finally, the function of characterization is reviewed, and the results are related to the project at hand. The results show that the characterization, in this instance, is valuable, as the simulations varied considerably from actual performance.

ACKNOWLEDGEMENTS

I thank Dr. Alan Mantooth, my thesis advisor, and my committee member, Dr. Jingxian Wu, as well as Dr. Matthew Francis, Paul Shepherd, Matthew Barlow, and Ashfaqur Ramman for all their help and guidance with this work.

I also thank my family and friends, for supporting me when I needed it during this process, and for helping make sure I stayed on the reservation while writing.

TABLE OF CONTENTS

LIST OF FIGURES

I. INTRODUCTION

A. Overview

The CMOS transmission gate, in and of itself, is not a complex device. It consists of an NFET and a PFET that are connected at the source and drain, with their body connections made to the lowest potential in the circuit and the highest potential in the circuit, respectively, as shown in Fig. 1. The gate of each transistor is connected to a digital (optimally) control signal, with the lowest and highest values, respectively, being the turn-on conditions for the PFET and NFET. This arrangement may, at first glance, seem slightly trivial, but for a certain type of circuit, it is essential.

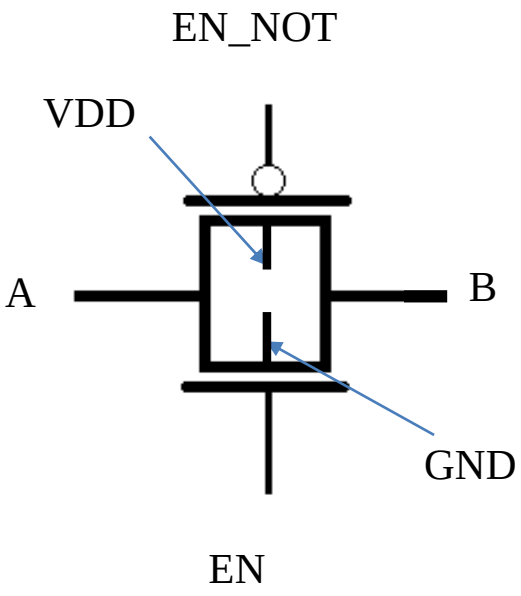

Fig. 1. Typical CMOS transmission gate schematic with terminal excitations labeled

B. Importance and Background

CMOS transmission gates, also referred to as switches, are most often employed in a particular type of circuit called a switched-capacitor circuit. Switched capacitor (SC) circuits are most generally amplifiers or signal processors of some sort, but are circuits that do not operate continuously. These types of non-continuous circuits are referred to as discrete-time circuits, and one such circuit that makes heavy use of transmission gates is the D Flip-Flop. In fact, one of the most common methods of constructing a DFF utilizes CMOS transmission gates, and the topology is shown in Fig. 2. The DFF shown is extremely small and is configured to be a stable edge-triggered FF, making it a core component in digital IC design. Another example of an SC circuit is the CMOS image sensor technology used in many of today's digital cameras. When the camera shutter is opened to take a picture, light will hit the sensor. Each of the sensor's thousands (or millions) of photocells will then produce a voltage corresponding to the light that hit it while the shutter was open, which has been passed through a color filter (most likely of the Bayer type). Capacitors attached to each of the photocells store that voltage briefly, which allows the camera itself to process the image captured even after the sensor closes, as well as on a pixel-by-pixel basis (as compared to other sensor technologies, which process the image in larger chunks, such as by row or by corner area). This, coupled with other elements of CMOS image sensor deign, allows for low power consumption compared to continuous-time sensor technologies, which is a benefit that extends itself to other SC topologies as well.

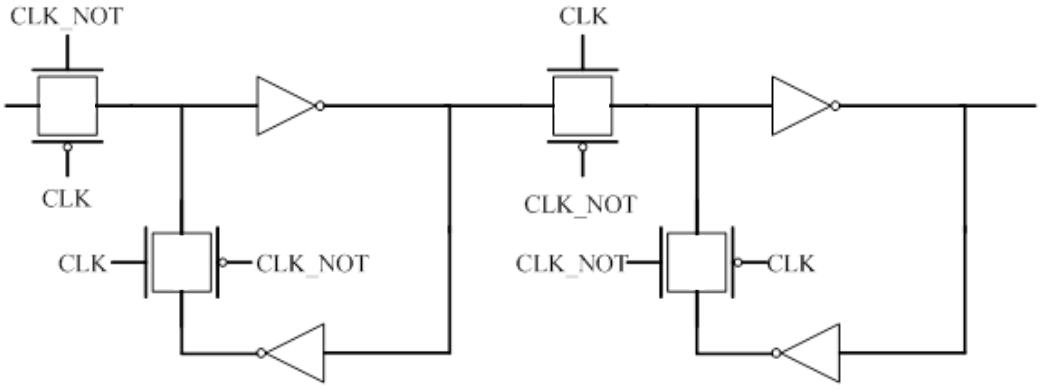

Fig. 2. D Flip-Flop using CMOS transmission gates as the switches.

The most basic of SC circuits consists of a switch and a capacitor, as depicted in Fig. 3. The switch is turned on and off, typically in response to a clock signal, to store an input voltage on a capacitor. When the switch is on, the input is connected to the capacitor, and the capacitor will follow its instantaneous value. When the switch is off, the capacitor will store the value of the input voltage at the time of turn-off. As previously mentioned in the CMOS image sensor example, SC circuits typically have lower power consumption than their continuous-time counterparts. This is simply due to the fact that sensing occurs in steps (typically to the time of a clock signal), rather than at every possible sensing interval. Especially in the case of circuits which have relatively slow or inefficient amplifying stages, the "downtime" seen when the input

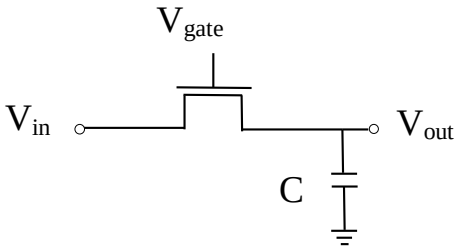

Fig. 3. Schematic showing the simplest form of switched capacitor circuit, with a MOSFET and a sampling capacitor. While the FET is on, V_C and V_{out} track V_{in}. While the FET is off, V_{out} tracks V_C.

is disconnected from the rest of the circuit can allow those slower stages to reach a more stable, and thus more useful and accurate, value faster.

The CMOS transmission gate's greatest strengths in comparison to NMOS or PMOS alone are its on-state characteristics. To elaborate, when a FET conducts, a channel is induced between the source and drain terminals. This channel allows electrons to flow, but is by no means an optimal path for them compared to a length of wire. The induced channel does, in fact, have a measurable resistance. This resistance can be quantified with Eq. 1 below, and is a key characteristic of transistors when considering them for implementation in an SC circuit.

$$r_{DSON} = {(v_D - v_s)}/{i_{DS}} \tag{1}$$

The reason why the on-state resistance becomes such an important quantity in SC circuits is because of the fact that the switches are used to connect and disconnect sections of a circuit that typically have a capacitance in them. Capacitors cannot handle instantaneous changes in voltage, and so the time constant that results from the capacitance and equivalent on-state resistance of the switch becomes important. In all cases, it is desirable to limit this time constant as much as possible to prevent transient errors from showing up in the measured output or from disrupting the operation of the rest of the circuit. Thus it becomes necessary to select a switch with the lowest on-state resistance possible, and that is where the CMOS switches become desirable over NMOS or PMOS alone.

When either an NFET or a PFET is used alone as a switch, the effective resistance in the path of the signal will end up being either r_{onN} or r_{onP}, respectively. However, when paired up into a CMOS switch, the effective resistance becomes r_{onN} in parallel with r_{onP}. The true advantage of this arrangement comes to light upon closer examination of the behavior of an

NFET and a PFET when used as a switch. As depicted in Fig. 4, the on-state resistance of an NFET will remain fairly low until V_{in} starts getting close to $V_{DD} - V_{TH}$, where it approaches infinity (a). Likewise, the resistance of a PFET drops once V_{in} has risen above the threshold voltage (b). Thus, if the two resistances are put in parallel, the resultant curve generally looks like the one in (c). This way, when one of the transistors is very close to turning off, the other transistor's resistance will dominate the term and still allow the signal to pass through. The only change to the gate circuitry is that the CMOS pair must have complimentary gate signals, so that they are both as electrically on as possible at the same time.

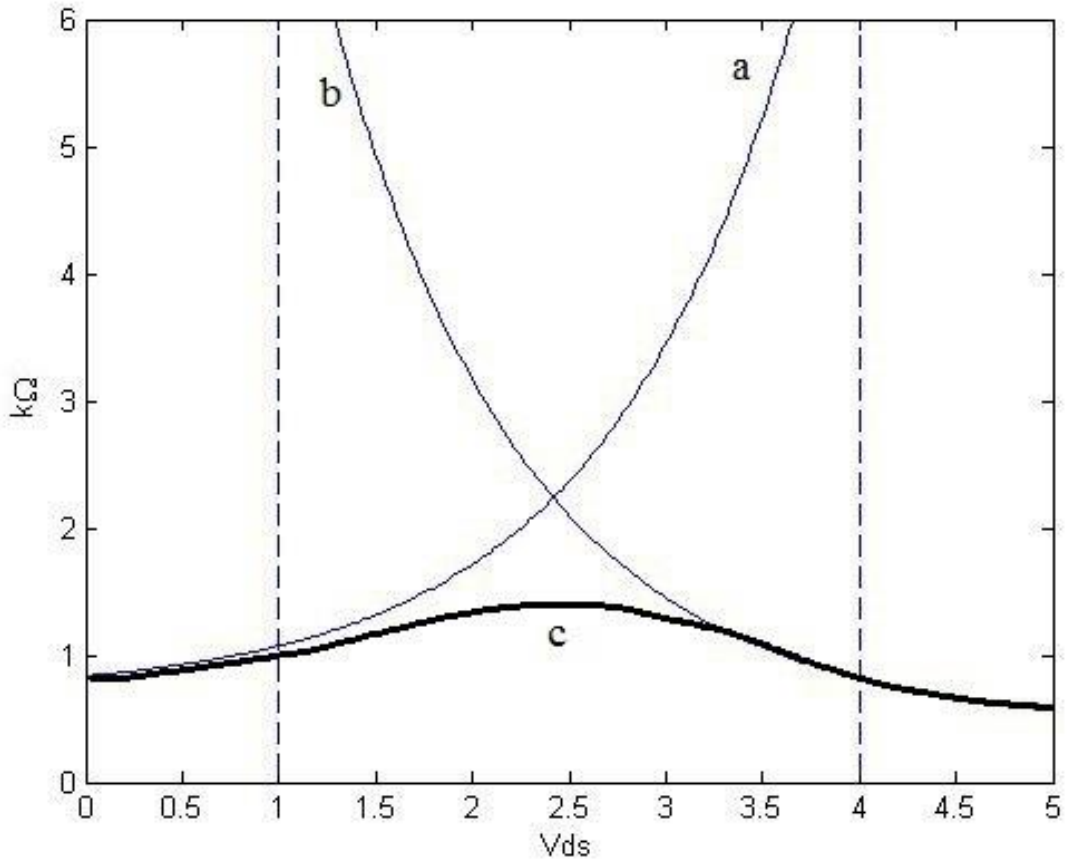

Fig. 4. Plot showing the generalized on-state resistance curves for a transmission gate comprised of an NFET (a), a PFET (a), and a CMOS pair (c).

In addition to the problems caused by the on-state resistance of a switch, there are a couple of other non-idealities that can make switched-capacitor circuit operation unstable. One is channel charge injection, and the other is clock feedthrough. Charge injection occurs at the time of turn off, and is caused by the induced channel between the source and drain terminals closing. When the channel shuts down, the charge in it at that point in time cannot simply disappear, and ends up being dumped on the source and drain terminals of the FET. This causes an unpredictable voltage offset on those terminals, which can lead to inaccuracies in the circuit. The other primary non-ideality is clock feedthrough, which is caused by the physical structure of the switches. Clock feedthrough is caused by the parasitic overlap capacitance seen between the gate terminal and the source and drain terminals. As a result, when the clock signal goes high, a small portion of it gets put on the source and drain terminals, which can be calculated using Eq. 2. The clock feedthrough is denoted by ΔV, where W is the width of the transistor, V_{CK} is the clock voltage level applied to the gate, C_{ov} is the parasitic overlap capacitance on the output terminal of the transistor, and C_H is the effective capacitance of the section of circuit on the output terminal. Clock feedthrough, like channel charge injection (CCI), causes a slight voltage offset at both terminals of the device. This effect becomes a problem when using devices to conduct signals that are close to the power supply voltages, as even a small voltage offset can push the drain or source voltage up above $V_{DD} - V_{THn}$ or $|V_{THp}|$ and make the device impossible to turn on.

$$\Delta V = V_{CK} \frac{WC_{ov}}{WC_{ov} + C_H} \tag{2}$$

However, there are ways to combat the voltage offsets introduced by clock feedthrough and CCI. One way is to introduce what are referred to as dummy transistors on the output side of

the switches. These transistors have their source and drain terminals connected together as shown on the right side of Fig. 5. They also have gate signals complimentary to those used on the switch itself so that the source/drain capacitance is driven out of phase with respect to the switch. Because the drain and source of the dummy transistors are connected and thus have no potential gradient across them, the dummy transistor's channel will not be induced just by the gate signal going high. But, when the channel charge injected by the switching transistor hits the dummy's source and drain, that energy can be enough to induce the channel (if the dummy transistors are sized appropriately), and will be absorbed by the dummy transistor in doing so. This way, the injected charge is dissipated instead of causing a voltage offset on the sampling capacitor. The dummy transistors are typically sized to be half the width of the switch transistors, based on the assumption that half of the channel charge will be injected on both terminals of the switch, and that C_{ov} is equal from gate to source and gate to drain. Unfortunately, these assumptions generally prove to be invalid, making dummy transistors limiting their ability to counteract channel charge injection.

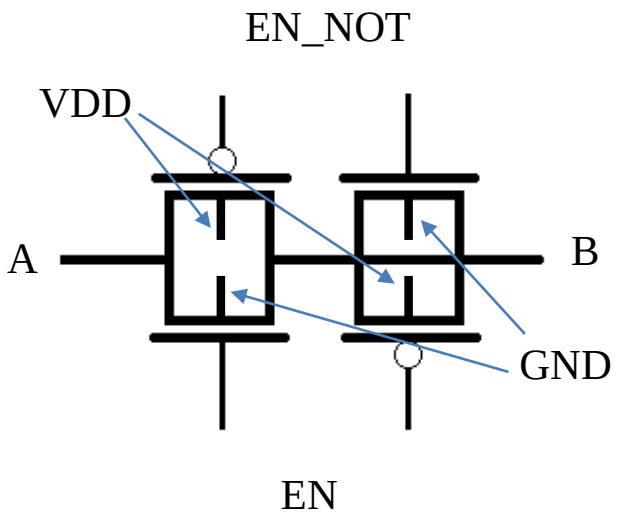

Fig. 5. CMOS transmission gate from Fig. 1 with a pair of dummy transistors on the output terminal.

Clock feedthrough, on the other hand, can be nearly eliminated with the use of dummy transistors. The switching transistor has one parasitic capacitance, C_{ovS}, from the gate to the output. The dummy transistor has two parallel capacitances between the output and its own gate, one for the source, $C_{ovD,s}$ and one for the drain, $C_{ovD,d}$. The clock feedthrough caused by the switching transistor can be completely absorbed if the dummy transistor's W is ½ of the switching transistor's W, making the total C_{ovD} equal to C_{ovS}.

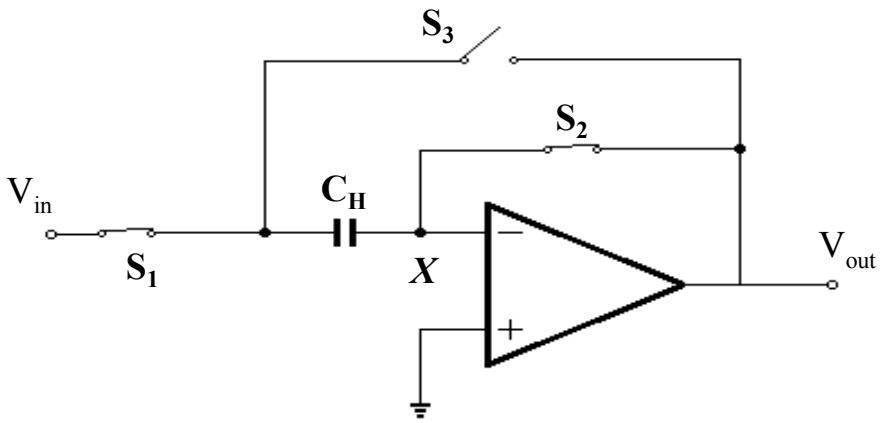

Fig. 6. Schematic showing a unity gain amplifier with switches and capacitor in place to separate the sampling and amplification modes.

Another way to counteract these voltage offsets is to introduce a time offset into the circuit. For example, consider the circuit in Fig. 6. Three switches, S_1, S_2, and S_3, have been placed around an operational amplifier to change it from a continuous-time amplifier into a discrete-time amplifier. Normal operation of the circuit would start with S_1 and S_2 closed, which would pass V_{in} to V_{out} across the sampling capacitor, thus allowing it to sample and store the value of V_{in}. Next, both S_1 and S_2 would open and S_3 would close, allowing the voltage stored on C_H to be processed by the amplifier and sent to the output. With this switching pattern, the channel charge of both S_1 and S_2 would be injected onto C_H, likely causing a sizeable voltage

offset. To compensate for the CCI, all that needs to be done to this circuit is to turn S_2 off just before S_1 does. The time interval needs to be at least S_2's fall time, and if this is done properly, node *X* will be floating when S_1 turns off. Since there is no resistive path to allow for S_1's channel charge to land on C_H, the charge instead all gets injected on the V_{in} terminal and does not affect the circuit. However, it is not always possible to implement this time offset, depending on the topology and its intended use.

C. Objective

To summarize, CMOS transmission gates have the benefit of a lower on-state resistance than an NFET or a PFET alone, which makes them highly useful in switched-capacitor circuits. However, even with that benefit, they are still susceptible to the main drawbacks of transistor-based switches, which are channel charge injection and clock feedthrough. The aim of this work is to simulate and assemble test structures for the purpose of characterizing the on-state resistance of CMOS transmission gates, as well as describe test procedures that will allow for direct comparison with the modeled behavior. The test structures examine the effects of varying the size of the transistors used, and they, along with the test setup and procedures described in the Measurements section, can be used in any fabrication process. For any given project with multiple fabrication runs, these test structures would be useful in the initial run for determining how to size transmission gates for use in any switched-capacitor circuits being designed.

II. APPROACH

A. Design

The design of the transmission gate test structures was straightforward. Using the Cadence Virtuoso Design Environment (version IC6.1.4-64b.500.10), a transmission gate was assembled for each size requiring characterization. The design was finalized by connecting the input and output terminals of each of the switches, separating the gate signals, and using the same V_{DD} and GND connections for each switch. The various terminals were connected to input, output, and input/output pins as appropriate, and the resulting schematics are displayed in Figs. 7 and 8.

For the purpose of this thesis, test structures were implemented based on the types of switches being used by the other members of the team assigned to the project, and the sizes implemented are listed below in Table 1. Due to some quirks in the manufacturing process, the size ratios were preserved while doubling the number of fingers in each transistor. This was done to counteract any performance inconsistencies caused by differences in overlap capacitance in the gate material.

TABLE 1. TEST STRUCTURES IMPLEMENTED

NFET size and NFET to PFET size ratio	Without dummy pairs	With dummy pairs
20 µm x 2 µm 2:1	✓	✓
20 µm x 2 µm 4:1	✓	✓
20 µm x 2 µm 6:1	✓	✓
4 µm x 2 µm N and 24 µm x 2 µm P	✓	✗

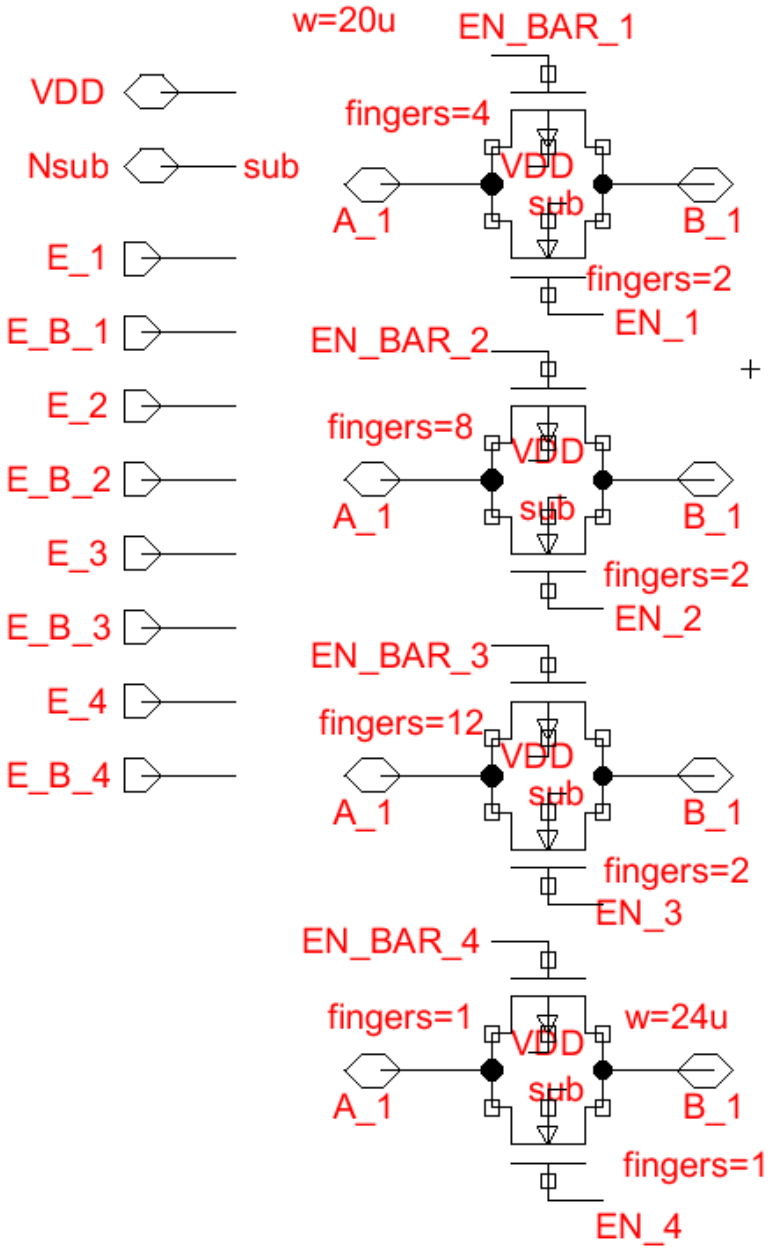

Fig. 7. Test structure schematic showing the transmission gates without dummy transistors. The switches are all designed to be probed from the same terminals, A_1 and B_1, and are activated by the complimentary gate signals EN_[x] and EN_BAR_[x]. The body connections for each transistor are connected via net name to the VDD and Nsub terminals.

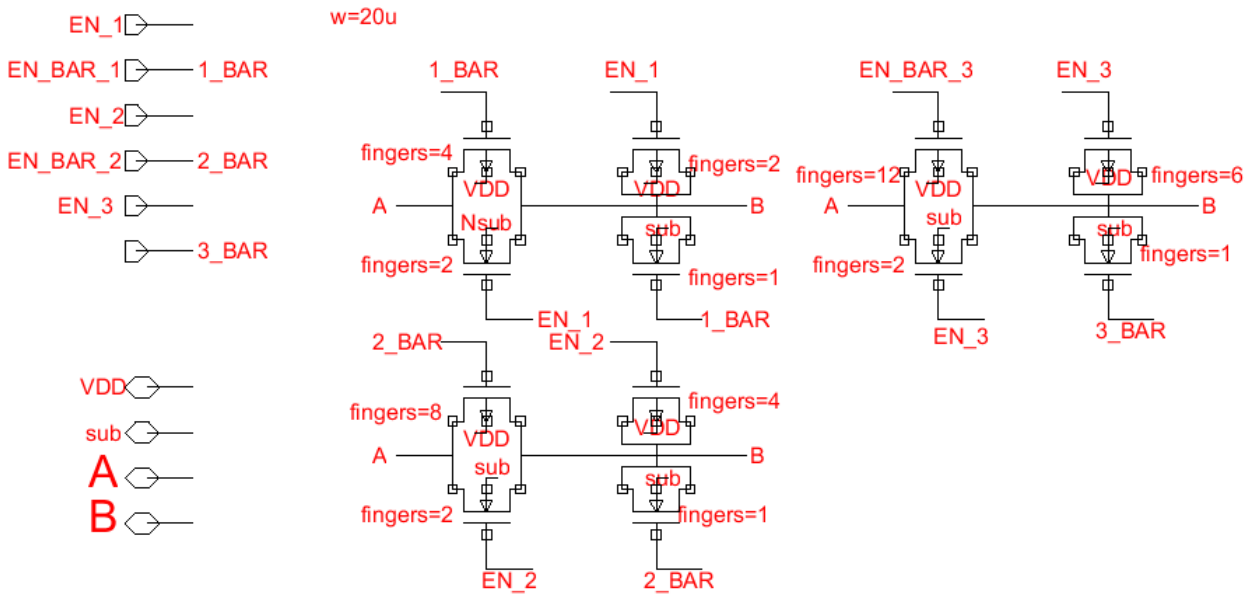

Fig. 8. Test structure schematic showing the transmission gates with dummy transistors. Terminals are connected similarly to the previous schematic, with the dummy transistors being connected drain-to-source and placed on the output side.

B. Simulation

Simulations of the transmission gates' on-state resistance were conducted using two similar test benches assembled in Cadence. Shown in Figs. 9 and 10, the test benches were designed around a circuit block created from the test structure schematics, and were designed so as to apply 15 V, which was the V_{DD} value in the fabrication process used, to the active NFET gate, all PFET body connections, and the inactive PFET gates, as well as apply 0 V to the active PFET gate, all NFET body connections, and the inactive NFET gates. The A terminal was swept from 0 V to 15 V linearly with 100 point accuracy, while the B terminal was stepped from 0 V to 15 V in increments of 1 V. Using Eq. 3, which is Eq. 1 adapted to use the signal names supplied by Cadence's Analog Design Environment (ADE L), the on-state resistance for each voltage combination was obtained and plotted to generate a family of curves like the one shown in Fig.

11. These simulations were conducted on each switch at temperatures of 25 °C, 100 °C, 200 °C, and 275 °C. The simulation setup windows are shown in Figs. 12 and13 to illustrate how the voltage sweeps and steps are established in Cadence.

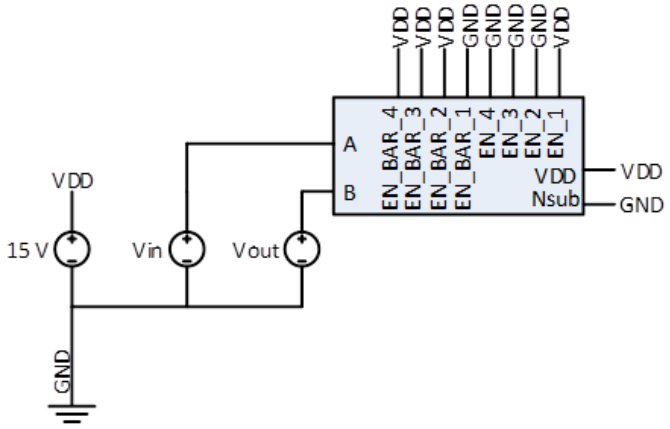

Fig. 9. Schematic showing the test bench used to simulate for on-state resistance of the test structures without dummy transistors. Voltages are applied as described above, with Switch 1 being simulated.

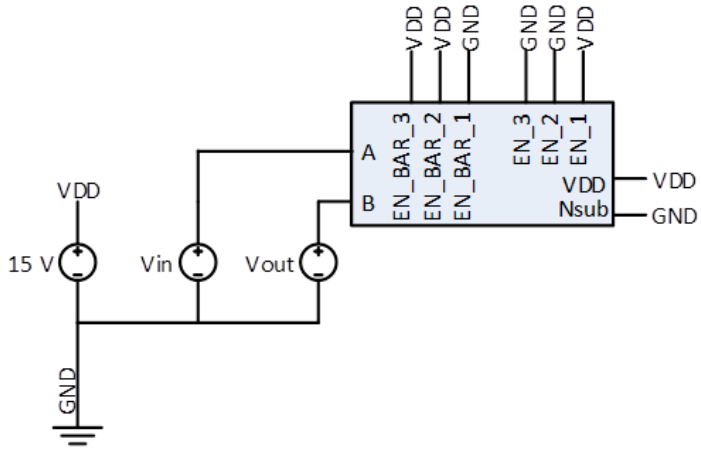

Fig. 10. Schematic showing the test bench used to simulate for on-state resistance of the test structures with dummy transistors. Voltages and device under test are the same as in the previous figure.

$$R_{ON} = {(V_A - V_B)}/{I_A} \tag{3}$$

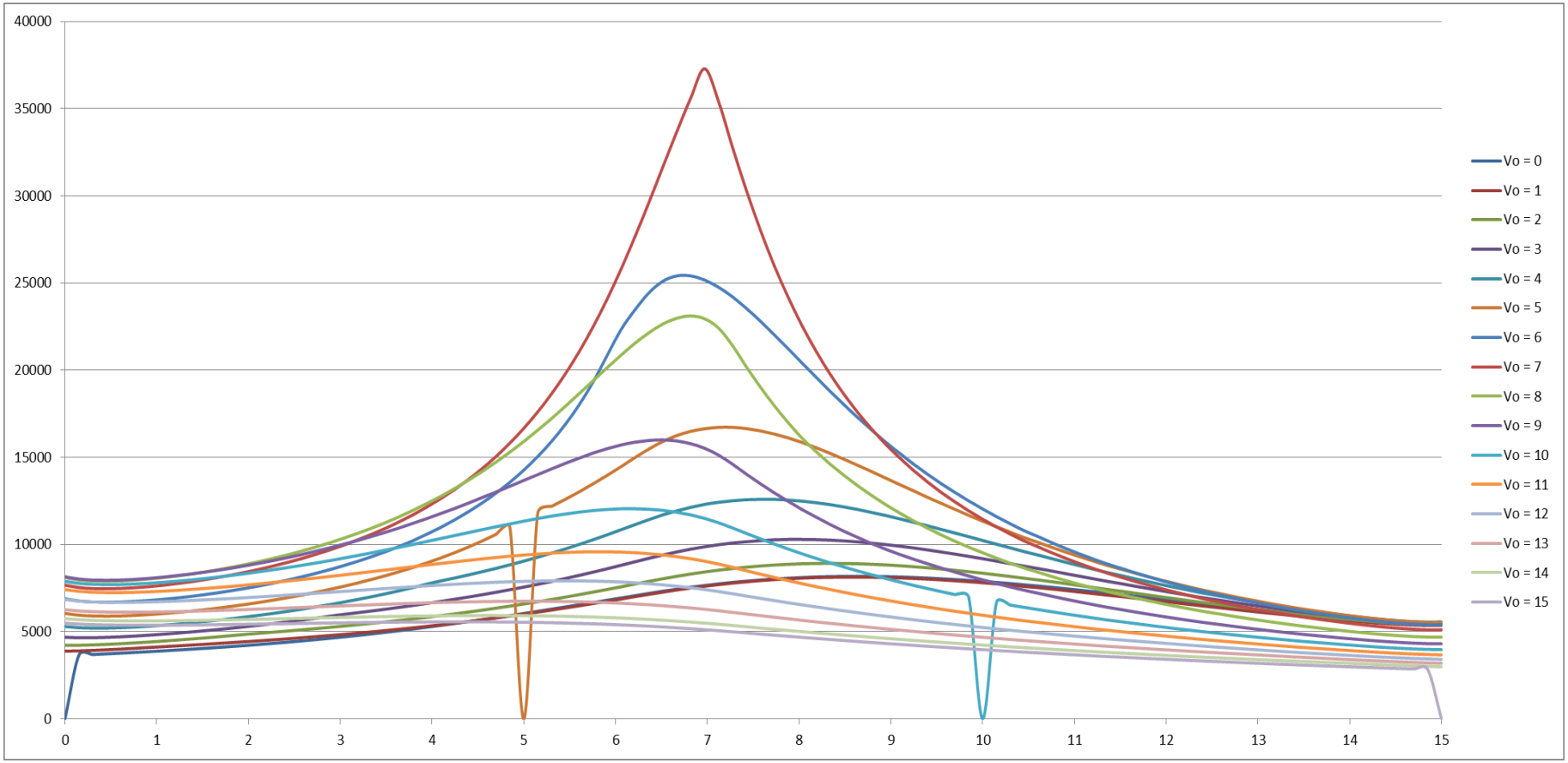

Fig. 11. Family of curves generated by an ADE L simulation setup like the one described below, detailing on-state resistance (y) versus input terminal voltage (x). The above curves are for the 4:1 size ratio switch without dummy transistors at 200 °C. Note that as the voltages on the A and B terminals close in on the same value, the resistance peaks, in keeping with basic circuit theory. The dropouts at multiples of 5 are caused by the voltage on both sides of the switch being equal, for which the resistance equation fed into the simulator went to zero.

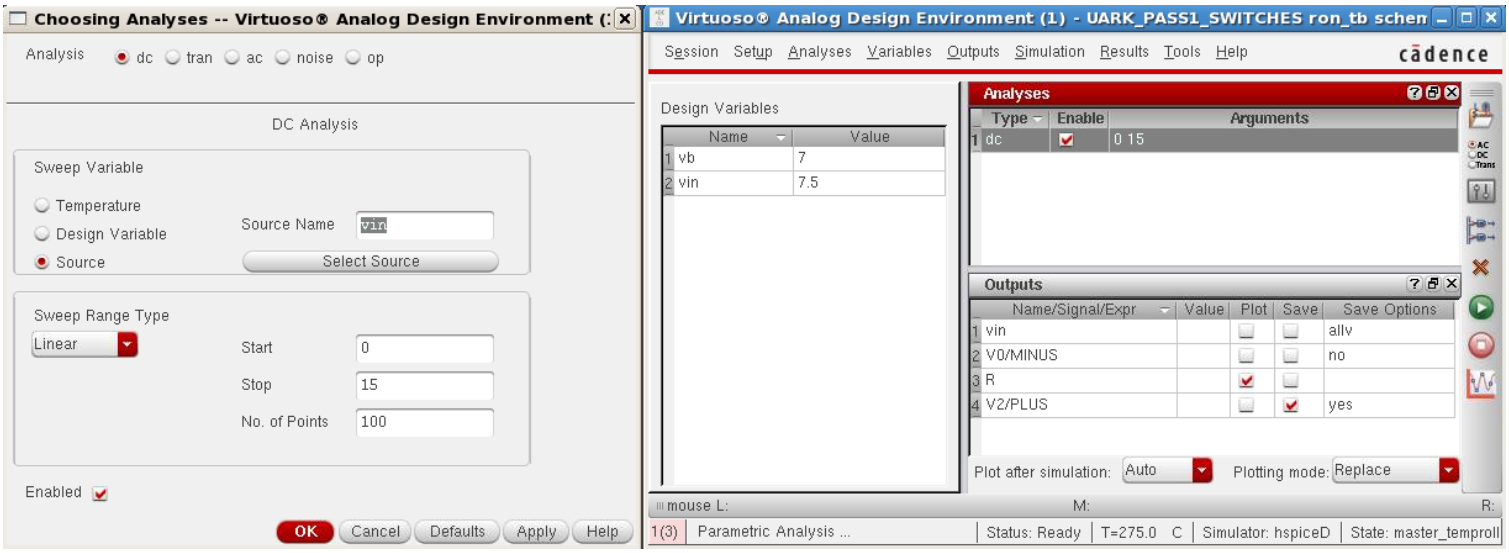

Fig. 12. ADE L configuration windows showing the setup for the primary voltage sweep of V_{in}, being a 100 point resolution linear sweep from 0 V to 15 V.

Fig. 13. ADE L Parametric Analysis window showing the setup for the voltage step of V_{out} = vb, setup to be from 0 V to 15 V in increments of 1 V.

C. Layout

To prepare the layouts, the Cadence Layout Editor tool was used. The layouts were built to match the schematics, with a few extra considerations. As mentioned earlier, the size of each primary switching transistor was doubled (by doubling the number of fingers) in order to counteract differences in the overlap capacitance seen from the gate to the source and drain. Another consideration was to not use any metal1 to poly jumpers when laying the traces for the A and B signals. These jumpers, shown in the indicated area of Figs. 14 and 15, were used to safely get one signal's trace around another signal without inadvertently merging the two. The issue with doing so is that the poly material, while capable of carrying the signal, has a much higher resistance per unit area than the metal1 material. This technique can be compared to using another layer in a printed circuit board. By creating a via from one layer of the board to another, one can wire a signal underneath another signal on the upper layer without fear of mixing them due to the insulator material between layers. It can be noted from the layouts that some signals appear to have more extensive use of jumpers than others, and that is true. The A and B signals did not have any jumpers because these were the main signals to be measured, in terms of both voltage and current. Thus, a path of minimal resistance should be laid for them, and so only one material is used, without interruption by a jumper. The power, ground, and gate signals, however, are all low current signals with no expected voltage drop, and so it is less important to maintain millivolt accuracy on them. Additionally, the dummy switches, indicated in Fig. 14, were flipped vertically to make it simpler to rout the signals; rather than having to cross EN and EN_BAR over each other in the middle of the device, the same gate signal was routed to both devices on the top and bottom.

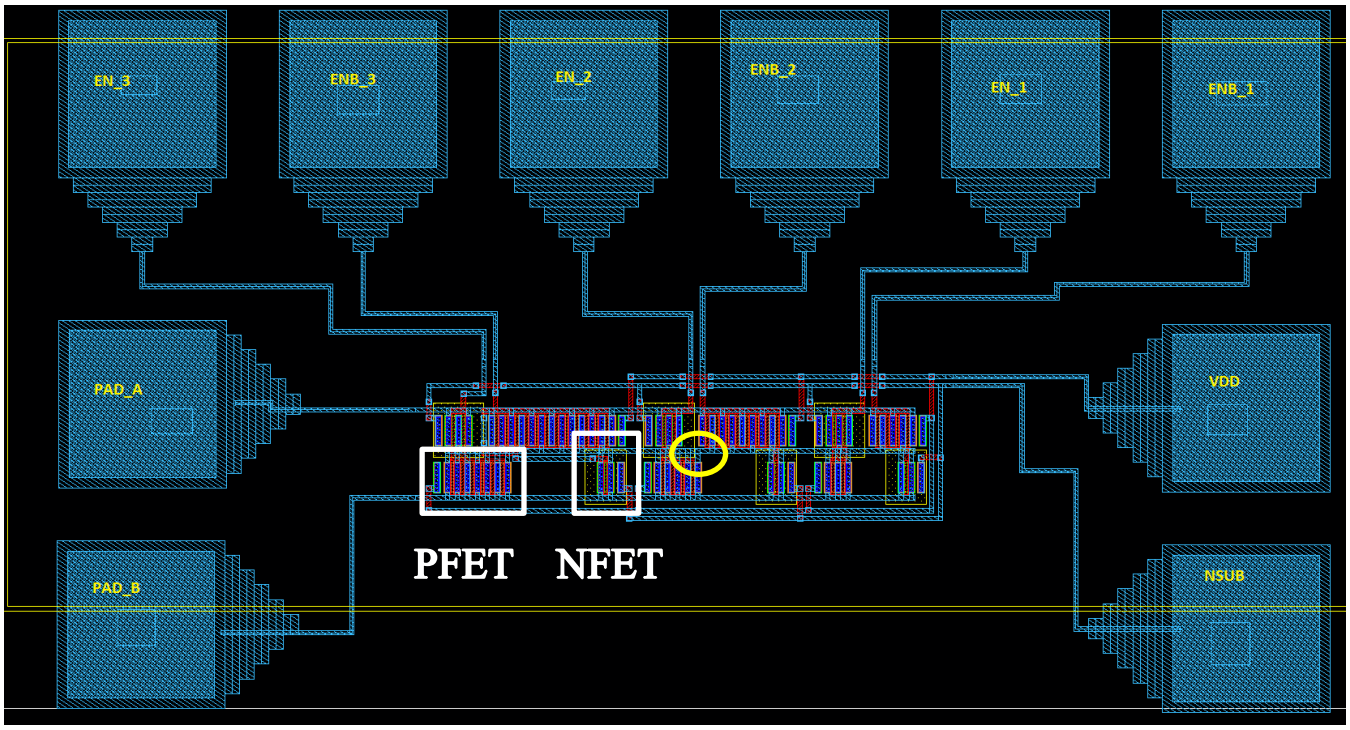

Fig. 14. Layout of the test array with dummy transistors, complete with probe pads. The jumpers are indicated by the yellow circle, and one pair of dummy transistors is indicated by white rectangles.

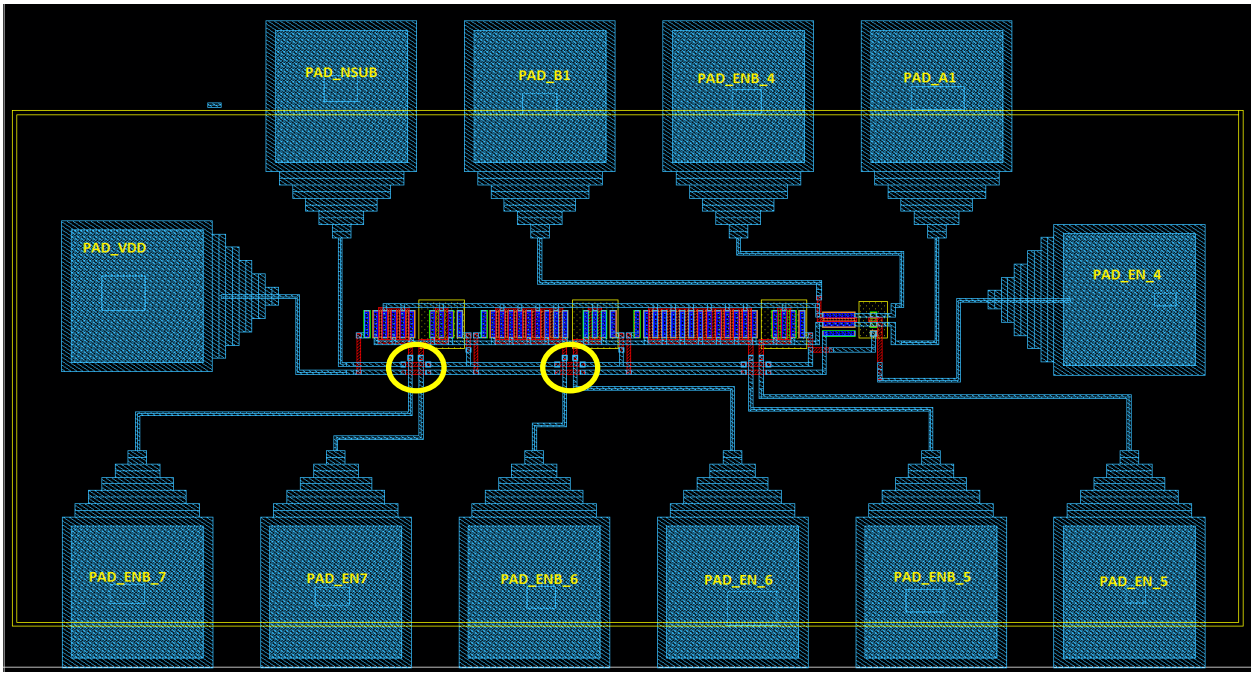

Fig. 15. Layout of the test array without dummy transistors, complete with probe pads. The jumpers are again indicated in yellow.

III. MEASUREMENTS

A. Methodology

Testing of the fabricated transmission gates was conducted in much the same way as the simulations were, once the material was prepared. For this work, the transmission gate structures were integrated into a larger circuit floor plan, which organizes circuits in the reticle on the wafer. The wafer is then cut apart to form separate die, which, if packaged, are commonly called chips. The chips were arranged in a grid-like reticle on each wafer for fabrication, with the grid arrangement being made along dicing lanes. Once the wafers were received from the fabrication facility, they were diced to separate the individual die for testing, and grouped by reticle. For clarity, Fig. 16 shows the whole wafer with several die highlighted and Fig. 17 shows the diced wafer, grouped as a reticle and placed into a custom-made die pack, again with several die highlighted.

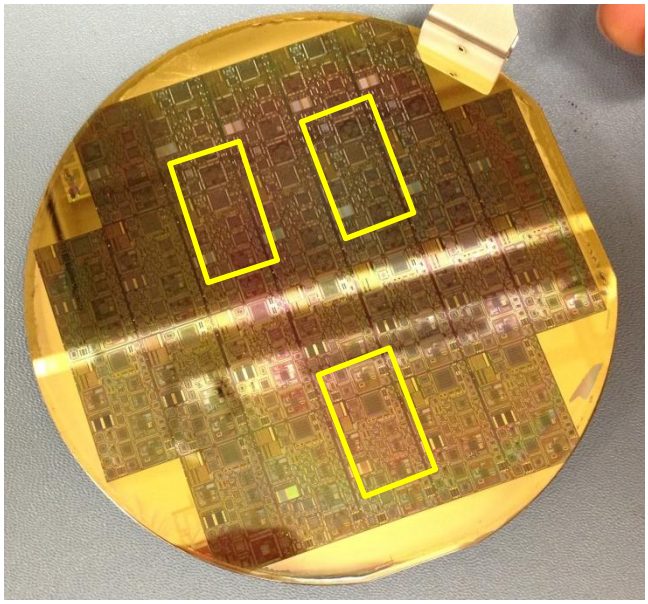

Fig. 16. A wafer of material. This is what was received from the fabrication facility, which was then divided up with a dicing saw to produce Fig. 17 below. Individual die are highlighted in yellow.

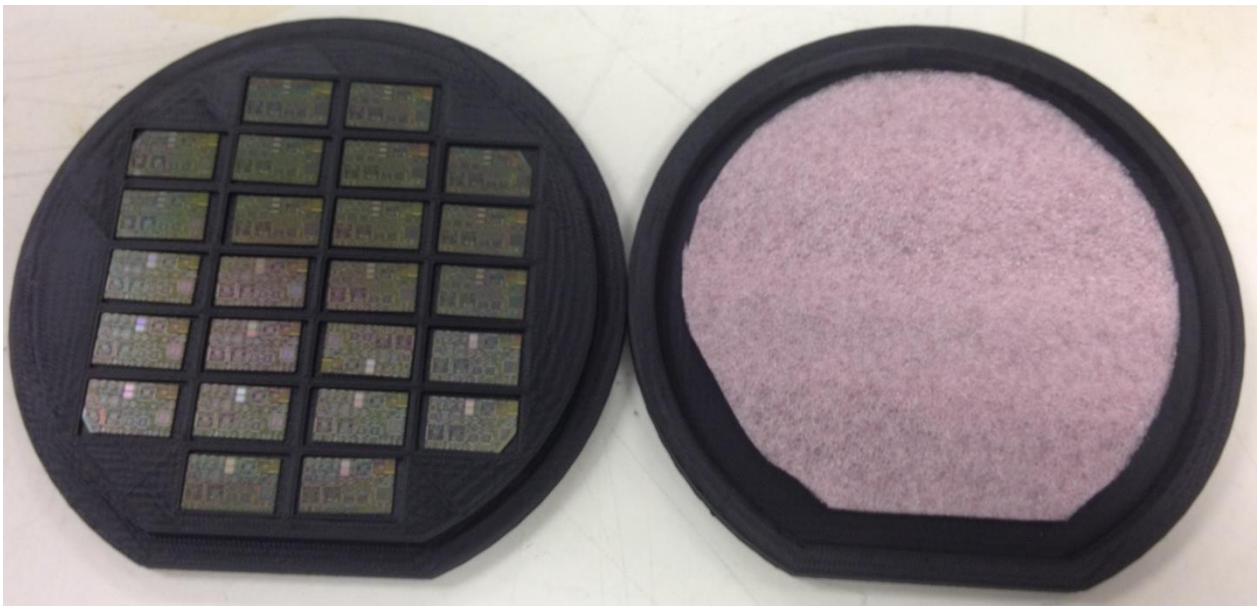

Fig. 17. A full reticle housed in a die pack. The die on the wafer in the previous image, having been fully diced, were placed in these 3D printed custom die packs for storage. The arrangement of the die was preserved in order to observe performance variations dependent on a die's position on the wafer.

The measurements were obtained using a Keithley 4200 Semiconductor Characterization System and a custom Semiprobe microscope-based probe station, shown below in Fig. 18. An Interactive Test Module (ITM) for the Keithley Integrated Test Environment (KITE) was assembled to mimic the simulation setup detailed in Figs. 12 and 13 above, which produced families of curves in much the same way as the simulator. Some extra steps were taken during setup to account for certain non-idealities in the physical components and in the testing equipment; one such precaution was the use of triaxial cable connectors to reduce signal noise due to leakage and preserve accuracy. The chuck, which is where the device being tested rests on the probe station, was also electrically grounded during testing, as well as any possible sources of electro-static discharge, so as to prevent from accidentally shocking (and likely destroying) the device under test. Testing was performed at the same temperature points as the simulations, and this was enabled by the heating elements in the chuck of the Semiprobe. Thanks to a

recently installed liquid cooling system, the temperature was maintained within 1 degree at each level. Once testing was complete, the data was moved from the Keithley into Microsoft Excel, where it was sorted and rearranged to prepare it for interpretation by a MATLAB script written specifically for this purpose. The script was written to provide the plots shown below in Figs. 19, 20, 21, and 22, which make interpreting the data a slightly more straightforward exercise compared to the family of plots in Fig. 11.

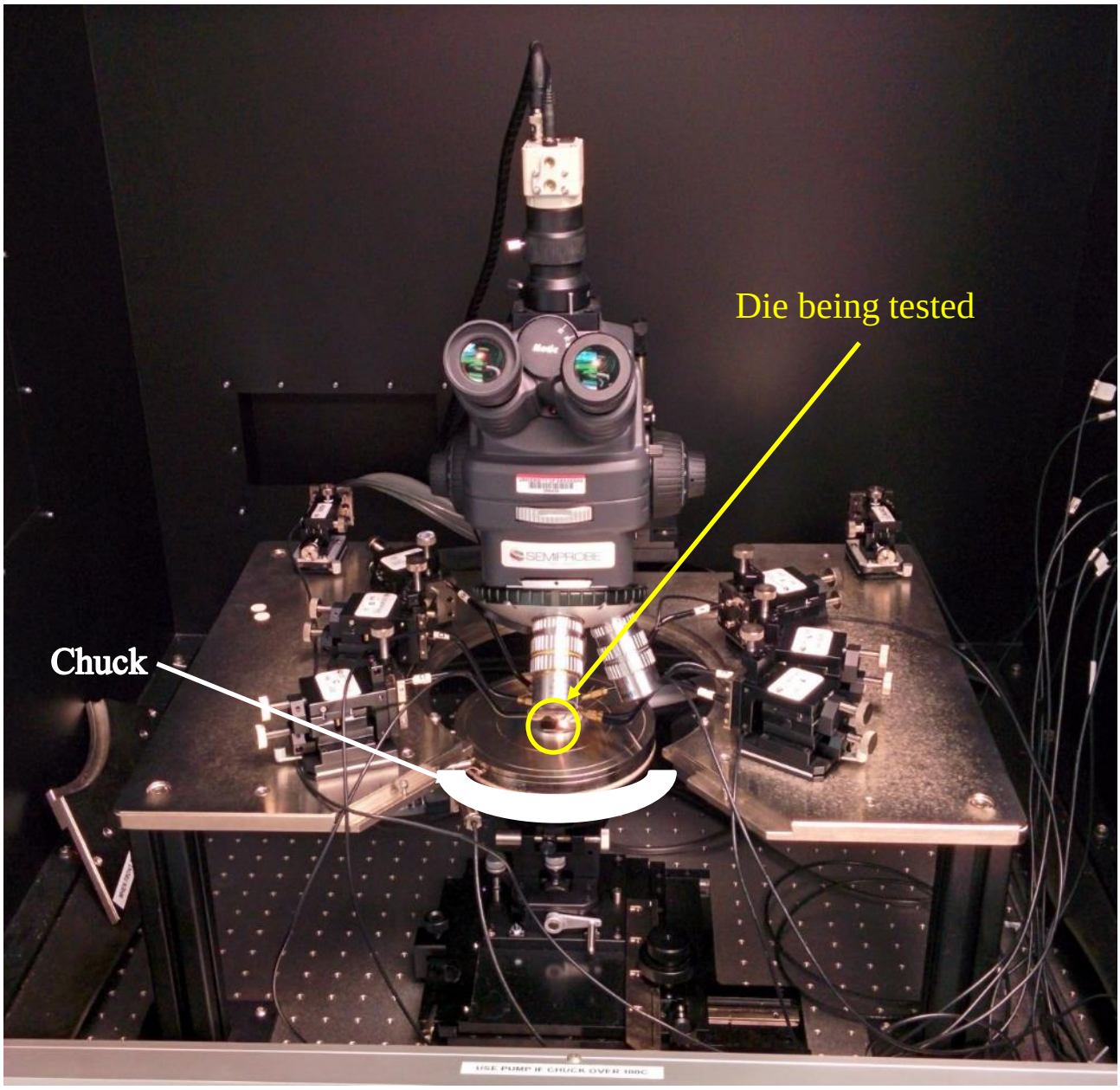

Fig. 18. Semiprobe probing station, with a die loaded onto the chuck (center) and all six probes in place.

B. Results

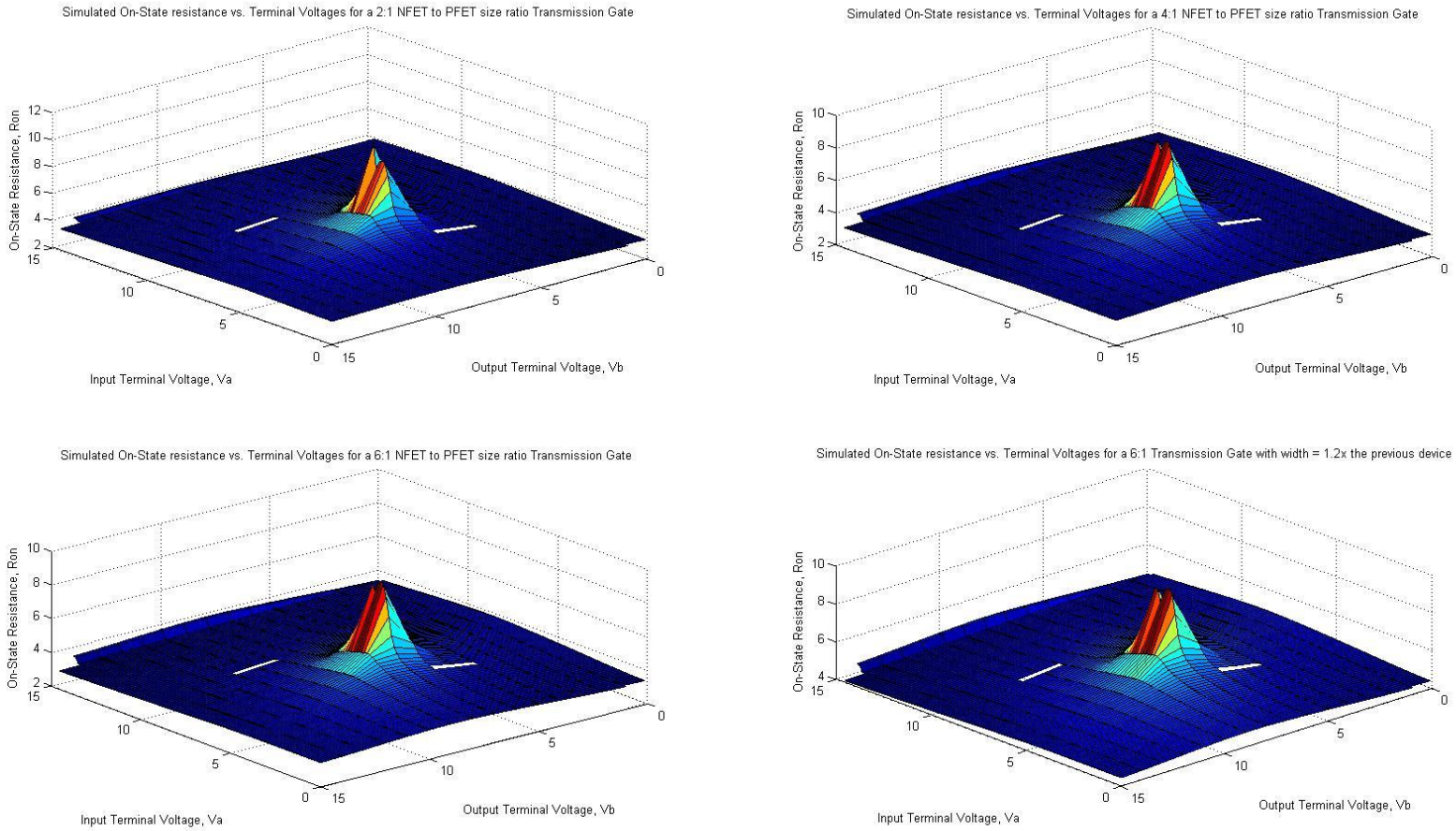

Fig. 19. Surface plots showing the SIMULATED effective on-state resistance as a function of the terminal voltages at 25 °C. These plots show how the simulator predicted the resistance would change with changes in device size, from 2:1 NFET:PFET (top left) to 4:1 (top right), 6:1 (bottom left), and a modified 6:1 with a 1.2x width compared to the regular 6:1. The z (Resistance) axis is plotted on a logarithmic scale.

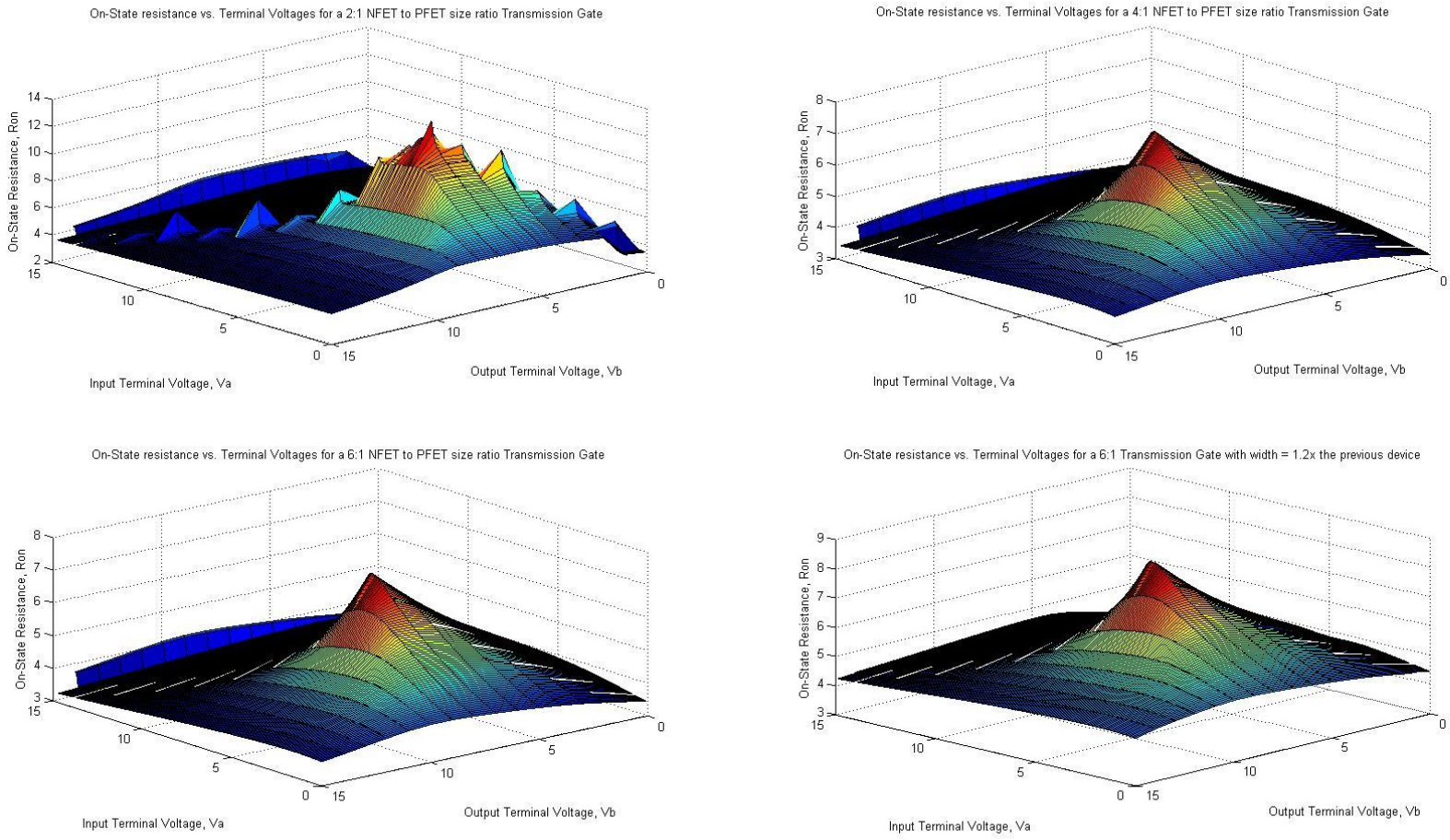

Fig. 20. Surface plots showing the room-temperature MEASURED effective on-state resistance as a function of the terminal voltages, comparing the same device geometries. The key difference is how far up the average resistance moved, as indicated by the much wider base of the peak. Furthermore, the 2:1 device behaved somewhat unstably compared to the simulations. Order is the same as the previous figure.

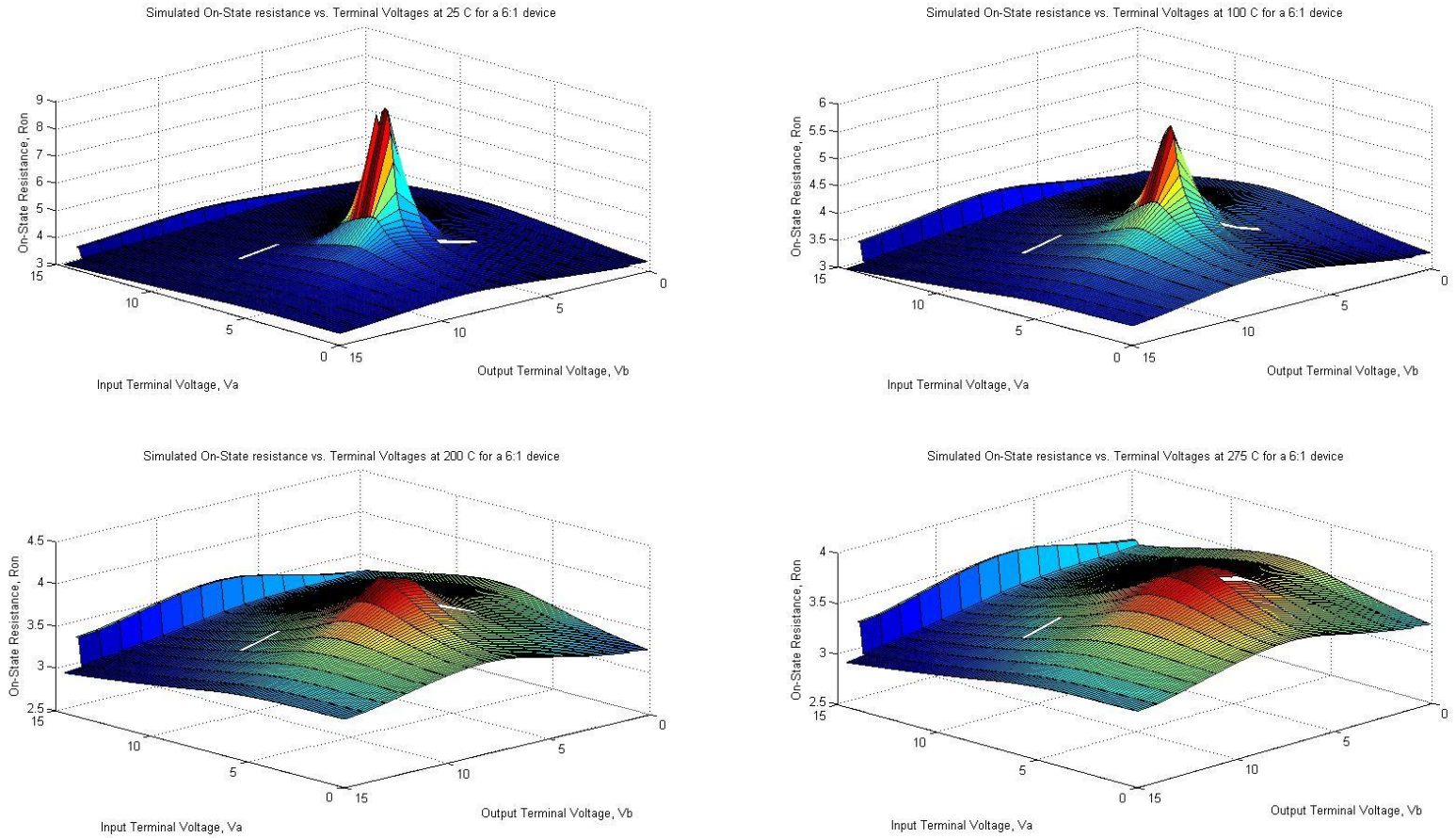

Fig. 21. Surface plots of the simulated on-state resistance, simulated over temperature for the normal 6:1 device. Note how much smoother the distribution is at higher temperatures; this could be useful for extreme environment devices. The plots are at 25 °C on the top left, 100 °C on the top right, 200 °C on the bottom left, and 275 °C on the bottom right.

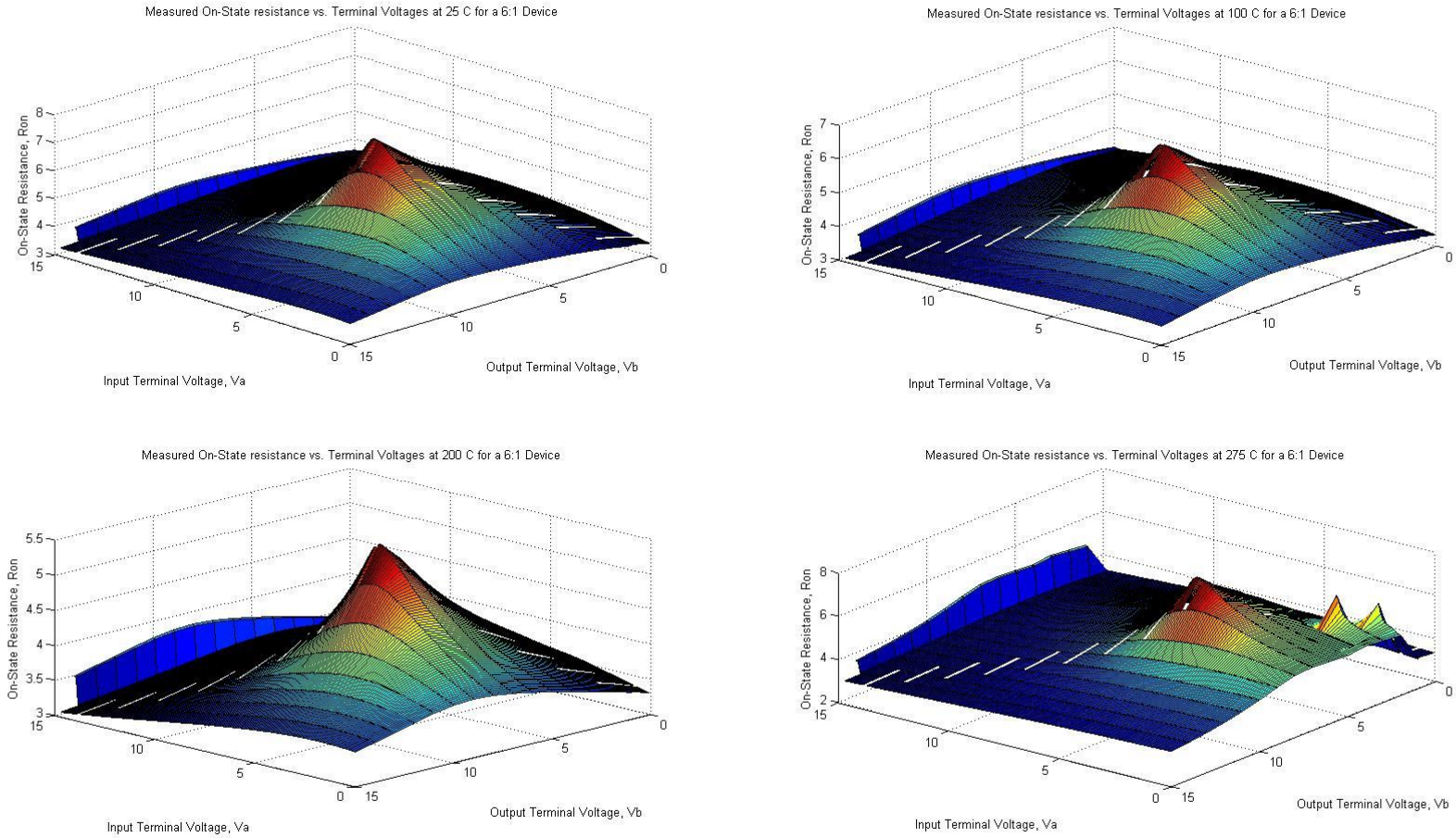

Fig. 22. Plots showing the measured on-state resistance over temperature for the 6:1 device. Plots are ordered like the previous figure. Again, performance does increase with temperature, but not quite with the same uniformity as the simulations.

C. Analysis

TABLE II. PERTINENT VALUES – GEOMETRY COMPARISON

	Average Resistance (Simulated)	Max. Resistance (Simulated)	Terminal Voltages (Simulated) (V_A V, V_B V)	Average Resistance (Measured)	Max. Resistance (Measured)	Terminal Voltages (Measured) (V_A V, V_B V)
2:1	7.500 MΩ	1.402 GΩ	6.4, 7	5.548 GΩ	20.10 TΩ	4.8, 6
4:1	2.662 MΩ	1.150 GΩ	6.4, 7	194.4 kΩ	16.57 MΩ	6.9, 7
6:1	2.088 MΩ	0.975 GΩ	6.4, 7	173.7 kΩ	14.62 MΩ	6.9, 7
6:1 modified	4.186 MΩ	2.170 GΩ	6.2, 7	1.810 MΩ	165 MΩ	7.1, 7

The key values to be taken from these resistance plots are presented in Tables 2 and 3. Upon examining the average resistance and maximum resistance for each device, conclusions may be drawn about both the need for model refinement and about how to design the switches in the future. From the standpoint of model refinement, the geometry comparison is the most telling. The fact that both average and maximum resistances are off by an order of magnitude in most cases indicates that the models need to have the current magnitude values recalibrated. However, in terms of how the resistance changes with device size ratio, the simulations tracked the measured results consistently, indicating a significant decrease in resistance from the 2:1 device to the 4:1 device, but not as much of a decrease when moving from the 4:1 top the 6:1.

With regard to how this information will impact future design, the geometry clearly indicates that to lower on-state resistance, a device of size ratio larger than 2:1 should be used, with the exception of the modified 6:1 device. That device, since it falls between the 2:1 and 4:1 in terms of performance but is larger than the unmodified 6:1, should not be considered further for design.

TABLE III. PERTINENT VALUES – TEMPERATURE COMPARISON

6:1 device	Average Resistance (Simulated)	Max. Resistance (Simulated)	Terminal Voltages (Simulated) (V_A V, V_B V)	Average Resistance (Measured)	Max. Resistance (Measured)	Terminal Voltages (Measured) (V_A V, V_B V)
25 °C	2.088 MΩ	0.975 GΩ	6.4, 7	173.7 kΩ	14.62 MΩ	6.9, 7
100 °C	5.638 kΩ	486.0 kΩ	6.2, 7	38.15 kΩ	1.780 MΩ	6.7, 7
200 °C	3.186 kΩ	135.3 kΩ	6.7, 7	13.30 kΩ	284.6 kΩ	6.6, 7
275 °C	2.619 kΩ	7.759 kΩ	5.6, 6	148.3 kΩ	16.59 MΩ	6, 6

Looking at Table 3, it becomes apparent that the models also require refinement from the perspective of behavior over temperature. The fact that the measured resistances, with the exception of the room temperature measurement, were all higher than the models indicates that the current flowing through the devices does not increase as much as was expected from the simulations. These results are even more telling due to the fact that the on-state resistance should be approximately half of that of a single transistor, since r_{onN} is in parallel with r_{onP}. Looking at the room temperature measurement however, the simulations did not predict as much

current to be flowing through the device, which may bear re-evaluation of how the effects of combining the NFET and PFET in this way affect performance at low temperatures.

Having gone through the tabulated results and looking at the plots above, it is apparent that the simulation models used will definitely benefit from the creation and testing of these test structures. While the general behavioral trends were well described in simulation, the physical devices behaved with somewhat differently across both temperature and geometric variation. Thus, these test structures would definitely be worth implementing on an initial fabrication run, so as to have the models updated and refined for use in subsequent runs.

IV. CONCLUSIONS

A. Summary

To summarize, the value of CMOS transmission gates was discussed, and a general method was described for implementing test structures of those devices for characterization purposes. The method is applicable to any fabrication process, and an equally general testing procedure was outlined to perform characterization of the physical devices. Some measured and simulated data was visualized and presented to verify the functionality of these methods. After presenting and analyzing that data, it was determined that, at least in this process and on this fabrication run, the effort of building, fabricating, and testing the structures was not wasted as there was significant variation between the simulated and measured results (with some general trends still holding, however). The models will need to be redone to incorporate this data, and re-evaluation of circuit designs will be necessary.

B. Potential Impact

If the transistor models for a particular fabrication process are not well developed, the characterization method presented in this thesis and the data obtained from using it could make or break circuit designs. The discrepancies between the simulated maximum on-state resistance and the measured on-state resistance within certain voltage ranges could easily push a sensitive circuit, such as an operational transconductance amplifier or a comparator, out of operation.

C. Future Work

Full characterization of the material received from the fabrication facility is desirable, but can be prohibitive in terms of probing time. The structures could be redone to prepare them for

packaging and thus larger scale testing, but size would be an issue. Of course, the characterization data obtained can be fed back into the models and used to refine them for the next fabrication run. If unique process variations are observed during testing, further structure development may be warranted to investigate these variations.

REFERENCES

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st Edition, McGraw Hill Higher Education, New York, NY, 2001.

[2] A. S. Sedra, K. C. Smith, *Microelectronic Circuits*, 6th Edition, Oxford University Press, New York, NY, 2010.

[3] "Transmission Gate based D Flip Flop", allthingsvlsi, [online] 2013, https://allthingsvlsi.wordpress.com/tag/transmission-gate-based-d-flip-flop/ (Accessed: 24 April 2014)