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Low voltage, low power, bulk-driven amplifier

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ABSTRACT

The importance of low voltage and low powered electronics is increasing with advances in medical electronics. This branch of electronics specifically requires low voltage and low power to make efficient innovative medical equipment. Low power electronics are also desirable because it conserves energy and power. This paper proposes a design of a differential in – differential our amplifier that uses a bulk-driven differential pair for the input pair. In addition, it also used bulk-driven current mirrors for the tail current sink and the active loads. The bulk-driven technique helps to achieve the low voltage design.

90nm CMOS technology was considered for the design but at the end SIGE 5AM process was chosen as it has low threshold voltage values maintaining good current – voltage characteristics. The software Cadence was used to simulate the design. A layout of the amplifier is out of the scope of this paper.

A gain of 14 dB was achieved using a rail-to-rail voltage of 1V (0.5V to -0.5). The power dissipation was 102uW using 5pF capacitive loads. The values of the calculations match the values of the simulations quite well. Some of the differences can be explained by the lack of accurate knowledge of the some of the process parameters for the SIGE 5AM process. Overall, the design achieved its goals and a successful low voltage and low power fully differential amplifier was created with respectable gain. This amplifier can be used as an input stage for an operational amplifier.

INTRODUCTION

Low voltage and low power operation has become popular because of the various low power medical applications. This paper proposes a design of a fully differential amplifier that will operate under supply voltages 0.5V to -0.5Vand have a power consumption of about 100uW. The very low voltages and power dissipation posed challenges when regular design techniques were used. Thus bulk-driven MOSFETS were used to achieve results with low voltages.

The design consists of an input pair and current mirrors that are bulk-driven. This paper includes a background of the theory of how the bulk-driven MOSFET operation. In addition, the calculations for the amplifier to achieve desired results are shown. Simulations for the design were done in the MSCAD lab, using the software Cadence. SIGE5AM process was used because of the 0.5 threshold voltage that was important to the design.

The paper then compares the simulated and calculated values and discusses the similarities and differences in the design. Finally, a conclusion is made about the success of the design.

THEORETICAL BACKGROUND

BULK-DRIVEN MOSFET:

The challenge behind this design was to build an amplifier that operates at a very low voltage. The threshold voltage is a limitation to design analog circuits at low voltages. The MOSFET is required to be turned on to perform any sort of signal processing. Thus the power supplies must satisfy the following requirement

$$V_{DD} + |V_{SS}| \geq V_{GS} = V_{DS} + |V_T|$$

for strong inversion operation. In addition, when the MOSFET is gate-driven, the supply voltage requirement becomes

$$V_{DD} + |V_{SS}| \geq V_{GS} = V_{DS} + |V_T| + V_{SIGNAL}$$

To avoid this problem, the design in this paper uses a bulk driven MOSFET, which removes the voltage overhead associated with the threshold voltage from the signal path.

A bulk driven MOSFET works like a JFET as a depletion device. Figure 1 shows the cross section of an n-channel MOSFET.

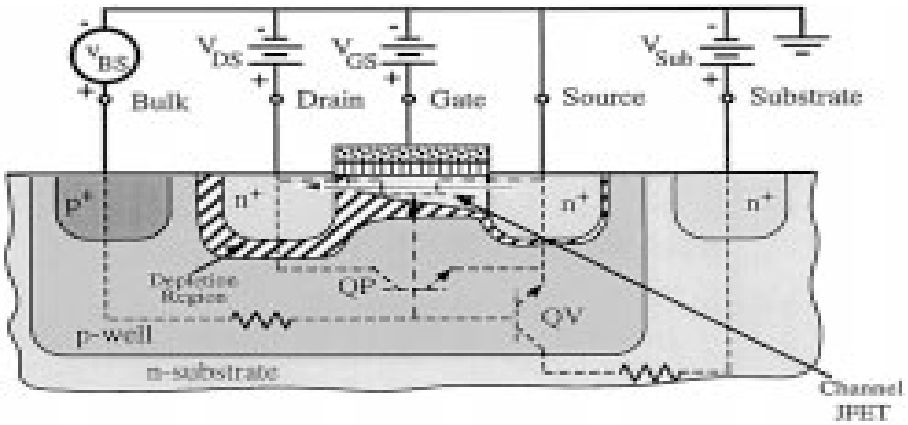

Figure 1: Cross section of n-channel MOSFET

An appropriate dc voltage is applied to the gate-source potential to turn on the MOSFET. The drain is connected in the usual way and the signal is applied between the bulk and the source. The reverse bias on the bulk-channel junction is used to modulate the current flowing from source to drain. This results in a JFET with the bulk as a signal input.

Advantages:

The depletion characteristics allow negative, zero and small positive bias voltages to achieve desired dc currents. This leads to a larger input common mode range that could not be achieved otherwise at low supply voltages.

Equations:

The large signal equation for the MOSFET is

$$i_D = \frac{1}{2} K_N' \frac{W}{L} \left[V_{GS} - V_{TO} - \gamma \sqrt{2|\phi_F| - v_{BS}} + \sqrt{2|\phi_F|} \right]^2$$

The small signal transconductance for a bulk driven MOSFET is as follows

$$g_{mbs} = \frac{\gamma \sqrt{2K_N' W/L I_D}}{2\sqrt{2|\phi_F| - V_{BS}}}$$

When V_{BS} is slightly forward biased, g_{mbs} increases and can be greater than the gate transconductance.

BULK-DRIVEN DIFFERENTIAL PAIR

An example of a bulk driven input differential pair is shown in Figure 2. A similar model will be used for the design proposed in this paper.

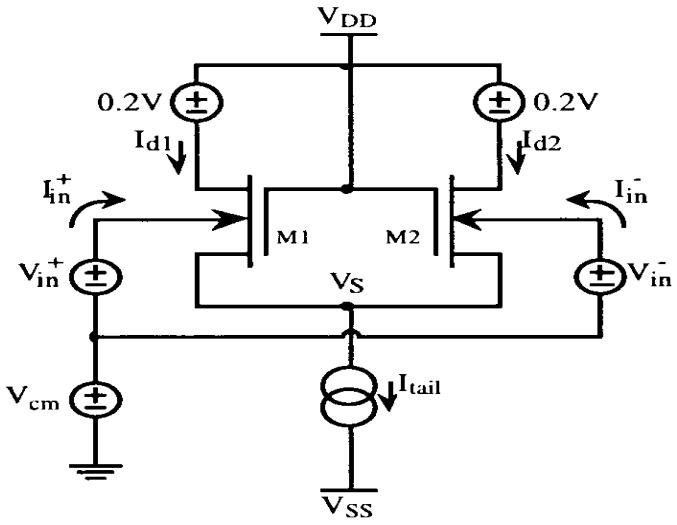

Figure 2: NMOS bulk driven differential pair

The diagram indicates that the gates of both MOSFETS are tied to the positive power supply to confirm that an inversion layer is formed. A differential voltage signal is applied between the bulk terminals of transistors M1 and M2. The differential input pair causes the currents between M1 and M2 to act as follows

$$i_1 - i_2 = G_{mbs} v_{in}$$

G_{mb} is the differential transconductance when the bulk terminal is used as the input.

$$G_{mb} = \frac{\gamma g_m}{2\sqrt{2\phi_F - V_{cm} - V_S}}$$

V_{cm} is the common mode voltage and V_S is the source coupled node voltage. Since the bulk source junction can be both reverse or forward biased, the V_{cm} can move rail to rail. For forward biasing, the threshold voltage reduces, causing V_S to follow V_{CM}. For a NMOS pair, as V_{CM} moves beyond mid-supply towards V_{DD}, V_S also moves toward V_{DD}.

BULK-DRIVEN CURRENT MIRRORS

NMOS

The differential amplifier designed in this paper uses a very similar current mirror as the one shown in the Figure 3. It is an NMOS bulk input current mirror and is used for the bias current. Instead of a gate-drain connection, the mirror has a bulk-drain connection. The bulk of the two transistors are tied together and the gates of the MOSFETS are tied to the fixed voltage V_{DD}. The latter is done to make sure the voltage between the gate and source is higher than or equal to V_T in order to form an inversion layer beneath the gate.

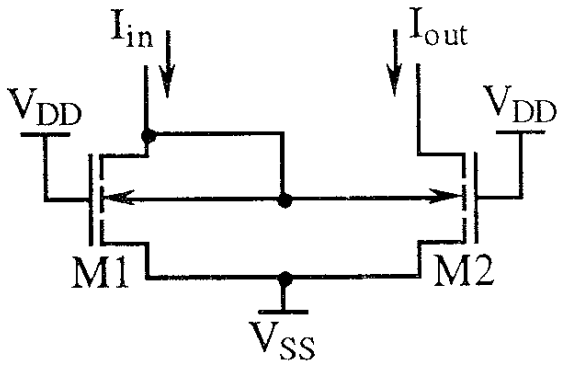

Figure 3: Bulk-driven NMOS current mirror

The operation of the mirror is as follows. With a slightly forward biased V_{BS}, the threshold voltage is decreased.

$$V_T = V_{TO} + \lambda(\sqrt{2|\phi|_F + v_{SB}} - \sqrt{2|\phi|_F}) \qquad [1]$$

Consequently,

$$i_D = \frac{K_N' W}{L}(V_{GS} - V_{TO} - \lambda(\sqrt{2|\phi|_F - v_{BS}} + \sqrt{2|\phi|_F} - \frac{1}{2}v_{DS})v_{DS}, v_{DS} < v_{DS}(sat) \qquad [2]$$

and

$$i_D = \frac{K_N' W}{2L}(V_{GS} - V_{TO} - \lambda(\sqrt{2|\phi|_F - v_{BS}} + \sqrt{2|\phi|_F})^2(1 + \lambda v_{DS}), v_{DS} \geq v_{DS}(sat) \quad [3]$$

The small signal saturation is

$$g_{mbs} = \frac{\gamma\sqrt{2K_N' W/L I_D}}{2\sqrt{2|\phi_F| - V_{BS}}} \quad [4]$$

The relationship between I_{in} and I_{out} is different for a bulk input mirror compared to a gate input mirror. For this current mirror, M1 is operating in the linear region. This condition is imposed by M1s bulk drain connection and $V_{DS1} = V_{DS2}$. Since the bulk of M1 and M2 are tied, $V_{BS1} = V_{BS2}$. M1 operates linearly since V_{DS1} is less than $V_{DS, sat}$. M2's drain-source voltage has no such restriction and can exceed $V_{DS, sat}$. Since $V_{BS1} = V_{BS2}$, $V_{GS1} - V_T = V_{GS2} - V_T$.

By solving equation [2] for V_{GS1}-V_T, and substituting in equation [3] the following expression for Iout is obtained. Unlike the gate mirror, the currents are not identical.

$$I_{OUT} = \frac{K_{N2}' W_2}{2L_2}\left(\frac{I_{IN}^2}{(K_{N1}' W_1/L_1)^2 V_{DS1}^2} + \frac{I_{IN}}{(K_{N2}' W_2/L_2)} + \frac{V_{DS1}^2}{4}\right)(1 + \lambda V_{DS2})$$

PMOS

A PMOS bulk driven current mirror works in the same it was described for an NMOS mirror. A schematic of PMOS current mirror is shown below. The PMOS current mirror is used for the PMOS active loads in the design proposed in this paper.

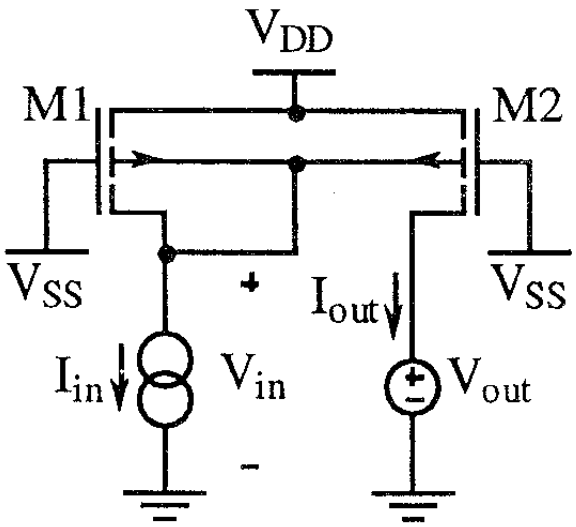

Figure 4: Bulk-driven PMOS current mirror

DESIGN

A design of a low voltage differential input, differential output amplifier has been proposed in this paper. The design uses the application of bulk-driven MOSFETS to turn on MOSFETS with rail-to-rail voltage as low as 0.5V to -0.5V. A block diagram of the amplifier is shown in Figure 5.

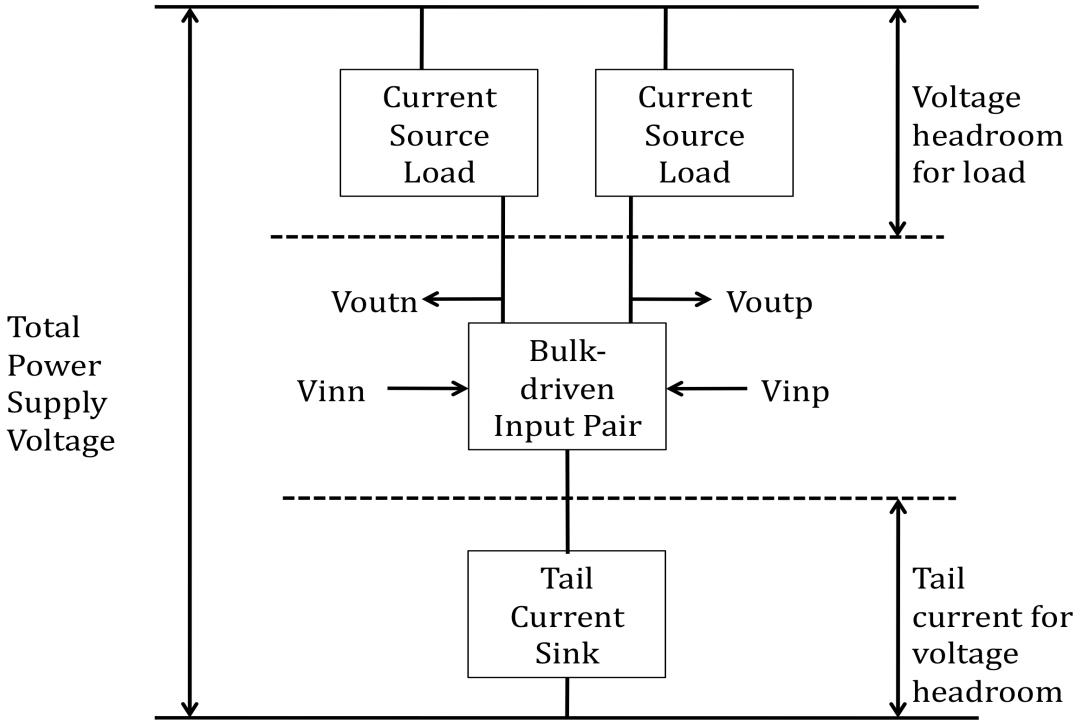

Figure 5: Block diagram for amplifier

From the diagram it can be seen that it is a popular topology for a differential amplifier has been used. However, the challenge lies in achieving an acceptable gain for the low supply voltage. A detailed schematic of the actual amplifier designed can be seen in Figure 6. A NMOS bulk-driven differential pair has been used for the differential input. A bulk-driven NMOS current mirror has been used to provide the bias current for the amplifier. Two PMOS active loads are used which are bulk connected to a bulk-driven PMOS current mirror.

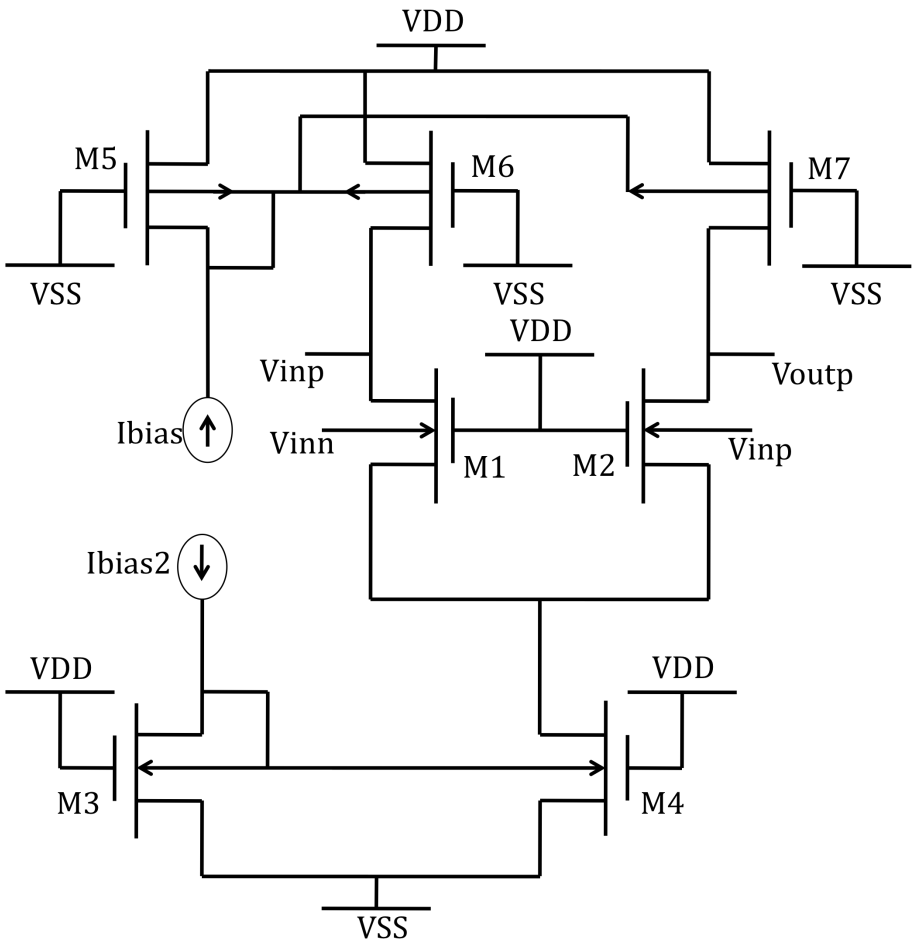

Figure 6: Schematic of the differential in – differential out amplifier

The gates of the NMOS transistors are tied to V_{DD} and the gates of the PMOS transistors are tied to V_{SS} to ensure the formation of an inversion layer beneath the gate. The bulk-driven current mirrors were used to reduce the voltage headroom required for the tail current and load. Two different bias currents were used – one for the NMOS current mirror and the other for the PMOS current mirror.

CALCULATIONS

The design needs to meet the following specifications:

$V_{DD} = 0.5V$

$V_{SS} = -0.5V$

$I_{TAIL} = 90uA$

$C_L = 5pF$

$Gain = 14dB = 5V/V$

The following are process parameters that are approximated using variables from other similar processes and experiments. The values used below for K_N, K_P, V_{TON}, V_{TOP} and lambda, were experimentally found by MSCAD lab students. The values of Gamma and Phi were approximated using the values for 0.8um CMOS Bulk Process.

$K'_N = 171u\,A/V^2$

$K'_N = 47u\,A/V^2$

$V_{TON} = 0.5V$

$V_{TOP} = -0.5V$

$\lambda_N = 0.1436V^{-1}$

$\lambda_P = 0.3998V^{-1}$

$\gamma_N = 0.4V^{1/2}$

$\gamma_P = 0.5V^{1/2}$

$2\phi_F = 0.6V$

For the following calculations, V_{DS} for each MOSFET was chosen by the designer to be in the linear or saturated region based on the MOSFET. It was also chosen with respect to the voltage headroom that was required for the design. From Figure 6,

M3 and M4

For M3, I_{BIAS2} = 60uA

Since M3 is in triode region and M4 is in saturation, the following equation can be used to calculate W/L to get an output of 90uA

$$I_{OUT} = \frac{K'_{N2}W_2}{2L_2}\left(\frac{I_{IN}^2}{(K'_{N1}W_1/L_1)^2 V_{DS1}^2} + \frac{I_{IN}}{(K'_{N2}W_2/L_2)} + \frac{V_{DS1}^2}{4}\right)(1+\lambda V_{DS2})$$

$$K'_{N1} = K'_{N2} = K'_N$$

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W}{L}$$

$$90u = 171u \times \frac{W}{2L}\left[\frac{60u^2}{(171u \times \frac{W}{L})^2 \times V_{DS1}^2} + \frac{60u}{(171u \times \frac{W}{L})} + \frac{V_{DS1}^2}{4}\right](1+0.04V_{DS2})$$

Now, $V_{BS3} = V_{DS3} = V_{BS4}$. Since M3 is operating in the linear region,

V_{DS3} can be less that V_{GS3}-V_T

Let V_{DS3}= 0.11V

$\frac{W}{L} = 15$ when $V_{DS3} = 0.11V$ and $V_{DS4} = 0.21V$

M5, M6, M7

Similarly for the PMOS mirror and load

When for M6, I_{BIAS} = 30uA and I_{OUT} needs to be 45uA

$\frac{W}{L} = 10.98$ when $V_{SD5} = 0.18V$ and $V_{SD5,SD6} = 0.45V$

M1 and M2

Since V_{DS4} of M4 of the NMOSFET current mirror is 0.21V, then

For both M1 and M2

$V_{S1,S2} = V_{SS} + V_{DS4}$

$V_{S1,S4} = -0.5 + 0.21 = -0.29V$

$V_{CM\,(\text{mid-supply})} = V_B = 0V$

$V_{BS} = -0.5 - (-0.29) = 0.21V$

$$g_{mbs} = \frac{\gamma\sqrt{2K_N' W/L I_D}}{2\sqrt{2|\phi_F| - V_{BS}}}$$

The design aims for a gain of 12dB, which is approximately 5V/V

$Gain = g_{mbs} \times R_{out}$

$$R_{out} = \frac{1}{(\lambda_2 + \lambda_7)I_{D2}} = \frac{1}{(0.143 + 0.3998)(45 \times 10^{-6})}$$

$R_{out} = 40.9k\Omega$

$$g_{mbs} = \frac{Gain}{R_{out}} = \frac{5}{40940} = 122uS$$

$$g_{mbs} = \frac{0.4\sqrt{2 \times 171u \times W/L \times 45u}}{2\sqrt{0.6 - (-0.21)}}$$

Therefore,

$\frac{W_2}{L_2} = 19.58$

$$f_{-3dB} = \frac{1}{2\pi R_{out} C_L} = \frac{1}{2 \times \pi \times 40.9K \times 5p}$$
$$f_{-3dB} = 778kHz$$

POWER DISSIPATION

Power dissipation for rail-to-rail operation of M1, M2, M4, M6, M7

$$P_{DISS} = (V_{DD} + |V_{SS}|)I_D = (0.5 + 0.5)(90uA)$$
$$P_{DISS} = 90uW$$

Power dissipation of current mirrors

For M3

$$P_{DISS,M3} = Ibias2 \times V_{DS3} = 60uA \times 0.11V$$
$$P_{DISS,M3} = 6.6uW$$

For M4

$$P_{DISS,M3} = Ibias2 \times V_{DS3} = 30uA \times 0.18V$$
$$P_{DISS,M3} = 5.4uW$$

Total Power Dissipation:

$$P_{DISS,TOTAL} = 90uW + 5.4uW + 6.6uW = 102uW$$

SLEW RATE

$$SL = \frac{I_4}{C_L} = \frac{90uA}{5pF} = 18V/us$$

SIMULATIONS

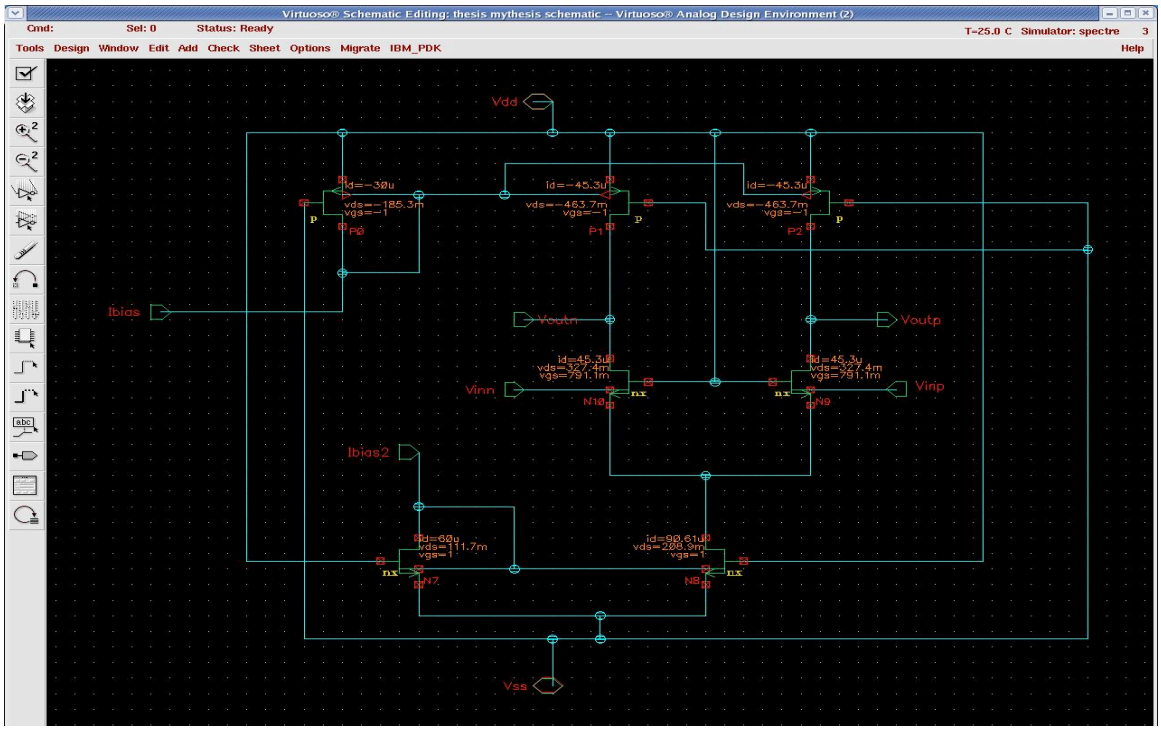

Figure 7: Bias Point Analysis of Circuit

The following results were obtained from the bias point analysis

V_{DS} for transistors:

M1& M2: 0.327V

M4: 0.206V

M6 & M7: 0.463V

M3: 0.11V

M5: 0.183V

Power dissipated in M1, M2, M3, M4, M5, M6 and M7

(2)(45.3uA)(0.327V) + (2)(45.3uA)(0.463V) + (90.6uA)(0.206V) + (60uA)(0.183) +

(30uA)(0.11V) = 104.5uW

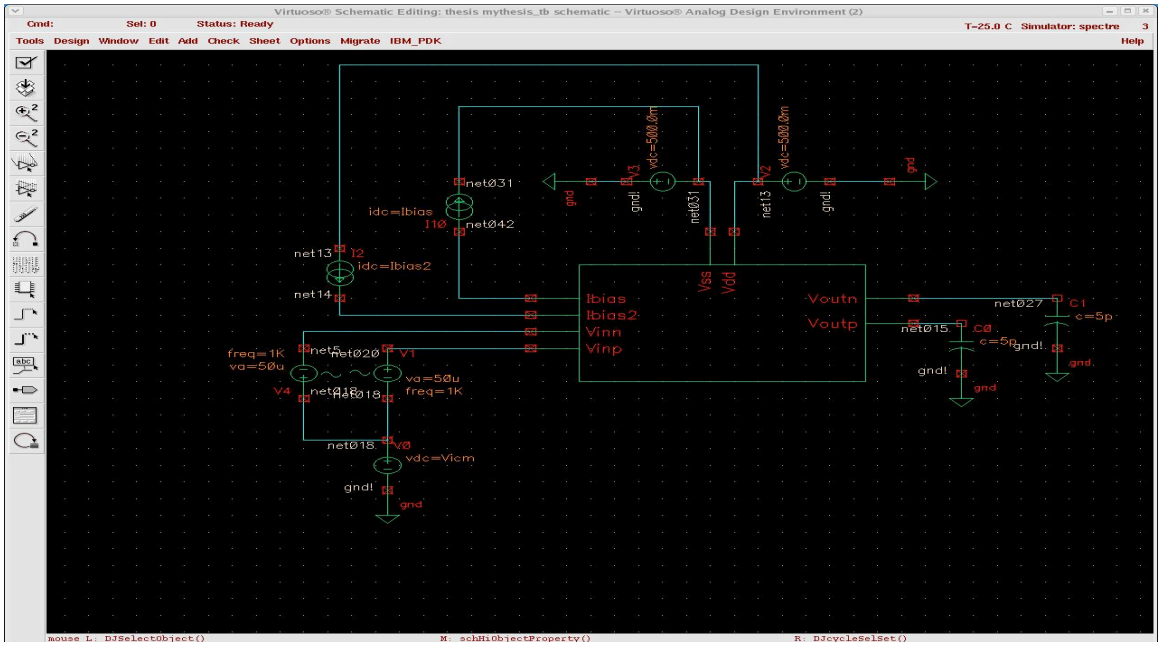

Figure 8: Schematic of the symbol

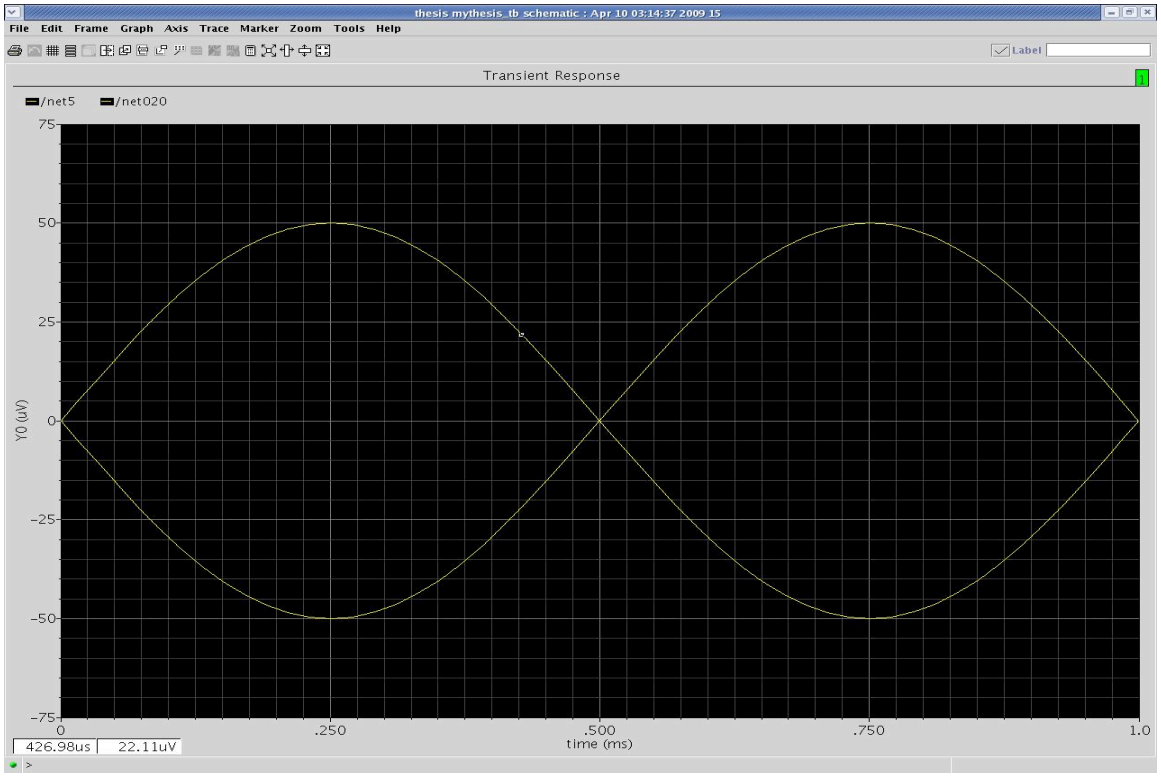

Figure 9: Transient analysis of Vinn and Vinp

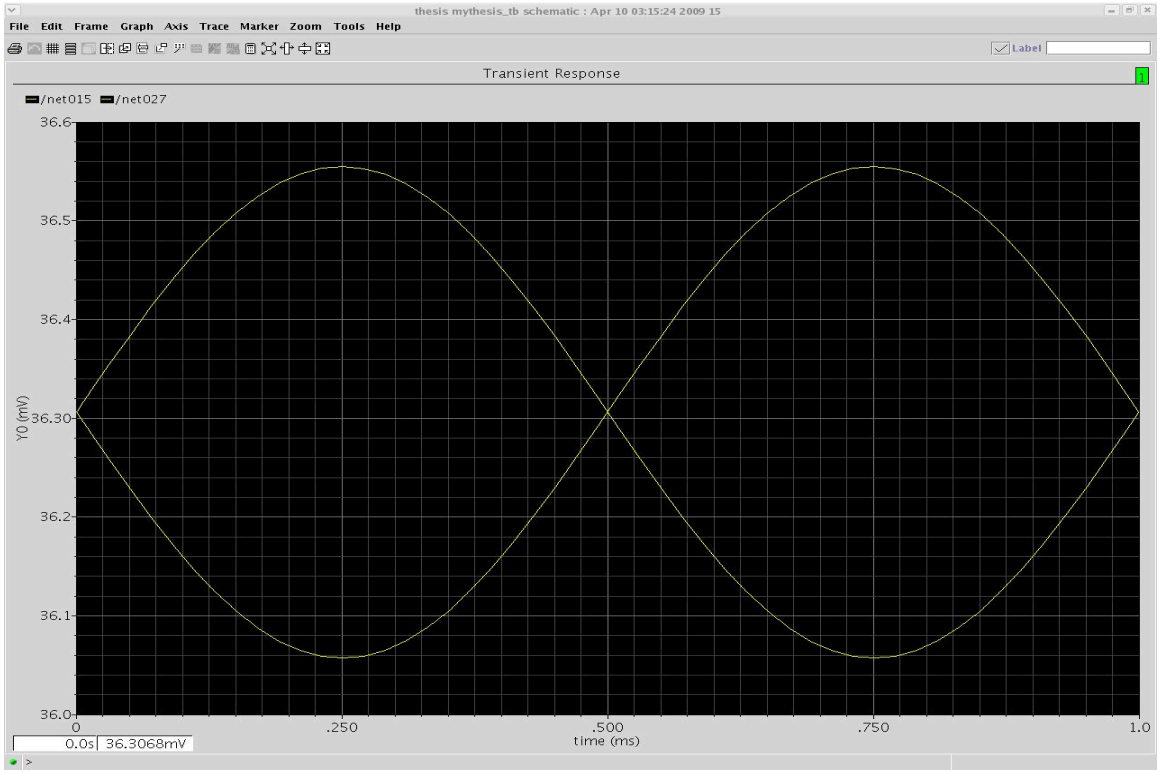

Figure 10: Transient analysis of Voutp Voutn (36.56m-36.14m =420uV, Gain=5.2V/V

Calculating gain from Figures 9 and 10

Vinp = 50uV

Vinn = -50uV

Vinp – Vinn = 100uV

Voutp = 36.56mV

Voutn = 36.14mV

Voutp – Voutn = 420uV

Gain = 260uV/100uV = 4.2

Gain in Decibels = 12.46dB

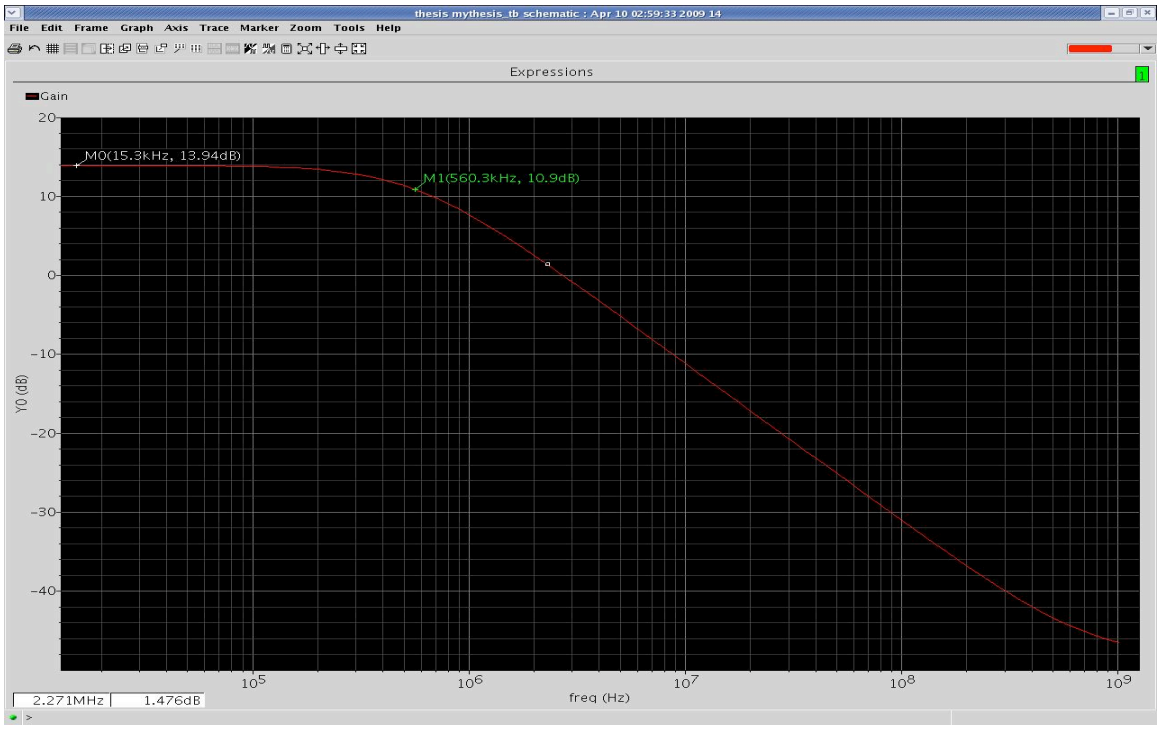

Figure 11: Bode Plot of Gain

Gain = 13.95dB

-3dB frequency = 560.3kHz

Unity Gain Bandwidth = 2.8MHz

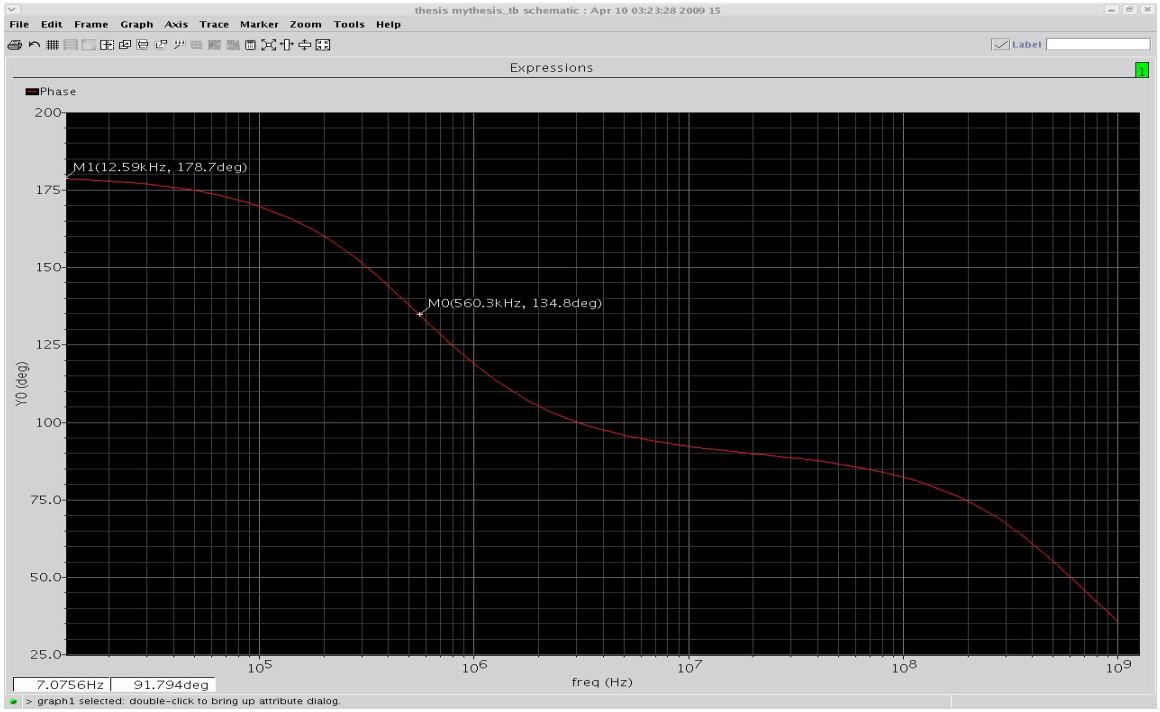

Figure 12: Bode plot of Phase

Phase margin = 100 degrees

TABULATED RESULTS

TABLE 1: Tabulation of Simulated and Calculated Results		
	Calculated	Simulated
Gain (dB)	14	13.94
Frequency, -3dB	778kHz	560kHz
W/L for M1 and M2	19.5	15u/1u
W/L for M3 and M4	16.35	10u/1u
W/L for M5, M6. M7	14.6	10u/1u
Total Power Dissipated	102W	104.5uW
Slew Rate	18V/us	-
Phase Margin	-	100°
Unity Gain Bandwidth	-	2.7MHz

DISCUSSION OF RESULTS

Gain: The gain obtained for both results were almost matched accurately

-3dB frequency: These values were also very similar. The differences can again be attributed to the inaccurate process parameters.

W/L of transistor: The results obtained by calculation and simulation for these values were slightly off from each other. One possible reason for this to occur could have been the inaccurate values of process parameters while calculating the results. Instead of keeping the W/L for simulation the same as the W/L in the calculations, The W/L of the simulations were modified to get the gain that was required.

Total Power Dissipated: The results obtained for the total power dissipated for simulation and calculation were almost exact.

Slew Rate: The slew rate that was calculated was a good value.

Phase Margin and Unity Gain Bandwidth: The simulated value obtained for the phase margin was very good. Anything above 60 degrees is good and this result produced 100 degrees. The unity gain bandwidth was a little low. The design can be modified to produce a unity gain bandwidth of 5Mhz instead of 2.8MHz.

CONCLUSION

A fully differential amplifier was designed using bulk-driven MOSFET operation. A bulk-driven differential pair was used as the differential input of the amplifier. Bulk-driven current mirrors were used for the bias current and the loads. The aim of the design was to achieve desired gain using ultra low voltage and very low power dissipation. A gain of 14dB was achieved using 1 V rail-to-rail voltage. The power dissipation was 104uW. The results obtained are very good. The design was successful in achieving its goal of operation at very low voltages with low power dissipation. However, there is always room for improvement. The design can be modified to increase the gain and the unity gain bandwidth. The differential amplifier presented can be used as an input stage for an operational amplifier.

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REFERENCES

1. Allen, P.W.; Blalock, B.J.; Rincon, G.A., "A 1 V CMOS op amp using bulk-driven MOSFETs," Solid-State Circuits Conference, 1995. Digest of Technical Papers. 42nd ISSCC, 1995 IEEE International , vol., no., pp.192-193, 15-17 Feb 1995

2. Blalock, B.J.; Allen, P.E., "A low-voltage, bulk-driven MOSFET current mirror for CMOS technology," Circuits and Systems, 1995. ISCAS '95., 1995 IEEE International Symposium on , vol.3, no., pp.1972-1975 vol.3, 30 Apr-3 May 1995

3. Blalock, B.J.; Allen, P.E., "A one-volt, 120-µW, 1-MHz OTA for standard CMOS technology," Circuits and Systems, 1996. ISCAS '96., 'Connecting the World'., 1996 IEEE International Symposium on , vol.1, no., pp.305-307 vol.1, 12-15 May 1996
URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=539890&isnumber=11195

4. Blalock, B.J.; Allen, P.E., Rincon, G.A., " Designing 1-V Op Amps Using Standard Digital CMOS Technology," Circuits and Systems, 1998. Analog and Digital Signal Processing., IEEE International Transactions on , vol.45, no. 7, July1995

5. Chatterjee, S.; Tsividis, Y.; Kinget, P., "A 0.5-V bulk-input fully differential operational transconductance amplifier," Solid-State Circuits Conference, 2004. ESSCIRC 2004. Proceeding of the 30th European , vol., no., pp. 147-150, 21-23 Sept. 2004

6. Chatterjee, S.; Tsividis, Y.; Kinget, P., "0.5-V analog circuit techniques and their application in OTA and filter design," Solid-State Circuits, IEEE Journal of , vol.40, no.12, pp. 2373-2387, Dec. 2005
URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=1546214&isnumber=33000

7. Kinget, P.; Chatterjee, S.; Tsividis, Y., "Ultra-Low Voltage Analog Design Techniques for Nanoscale CMOS Technologies," Electron Devices and Solid-State Circuits, 2005 IEEE Conference on , vol., no., pp. 9-14, 19-21 Dec. 2005
URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=1635192&isnumber=34293

8. Allen, Phillip and Holberg Douglas. “CMOS Analog Circuit Design,” New York, 2002.