Simulation and Implementation of FPGA Based Hybrid Asymmetric Multilevel Inverter

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***Abstract*—** This work focuses on proposing a new structure for asymmetric multilevel inverter. In the proposed topology, a switched capacitor (SC) and conventional series inverter are combined and connected in cascade. The proposed multilevel inverter finds its application in photovoltaic inverters which has numerous advantages. Firstly, it converts power for AC requirements from comparatively low DC voltage sources and with lower number of switching devices. Second, with the removal of transformers normally used for stepping up the voltage of each inverter stage the weight, volume and size of the whole system is reduced as the proposed topology can double the input voltage without a transformer. Symmetrical step control method (SSCM) and fundamental switching frequency method (FSFM) are applied to this proposed topology to actuate the power electronic switches for effective control and monitoring of voltage levels generated at the output. The simulation is executed using MATLAB/SIMULINK software. It was found that FSFM modulation technique results in a lower value of Total Harmonic Distortion (THD). The switching strategy is implemented with an FPGA device for the experimental prototype. The simulation and experimental result of single-phase 25- level inverter is given to demonstrate the precise operation of the suggested topology.

Keywords—switched capacitor, series-parallel connection, asymmetric multilevel Inverter, THD

I. INTRODUCTION

A multilevel inverter is a power electronic system that synthesizes a desired AC voltage from several levels of DC voltages as inputs. The ever-increasing energy consumption and the diminishing trend of using raw material resources due to its exhaustible nature and high cost have lead to the development of inexhaustible energy sources like photovoltaic (PV) more and more. The multilevel inverters have been considered as the main unit in such grid-connected systems. The challenging issues in such systems are producing an acceptable sinusoidal voltage waveform and boosting the output voltage [4]. Due to the bulky inductors, the use of a transformer in the boost multilevel inverter increases the size and cost and decreases the efficiency [1].

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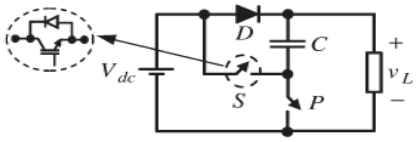


Fig. 1 Basic unit

The switched capacitor multilevel works by proper charging and discharging of capacitors in parallel and in series to produce the desired output [2]. In order to alleviate the inherent voltage unbalancing problem, the hybrid source switched capacitor topologies can be used. By using this kind of inverter structure with simpler control techniques and fewer switching devices, it is possible to achieve a higher number of voltage steps at the output [3]. This switched capacitor topologies can be used in standalone applications like PV systems and electric vehicle application [4].

This paper proposes a new topology using switched capacitor units. Symmetrical step control method and the fundamental switching method are used in this investigation. The paper is structured as follows- in the next section the basic unit of the proposed topology is explained followed by the suggested topology. Section III presents the simulation results and section IV describes the experimental results. Lastly section V provides the conclusion for this work.

II. PROPOSED ASYMMETRIC MULTILEVEL INVERTER

The suggested elementary unit for the asymmetric multilevel inverter is shown in Fig. 1. In this basic network, the capacitor is connected in series and parallel with the dc voltage source by the switches S and P. The switching on of switch P makes the capacitor to get charged to the voltage V_{dc}, and when the switch S is switched on, the capacitor starts to discharge. When the switch S is on, the diode D is off as it is reverse biased and prevents capacitor discharging to the dc voltage source. It is coherent that both switches S and P cannot be on concurrently because a short circuit across the dc voltage source V_{dc} would be created. Table I specifies the values of V_L for states of switches P and S. The elementary unit shown in Fig. 1 can be extended as shown in Fig. 2.

TABLE I
V_L VALUES FOR STATES OF SWITCHES P AND S

State	Switching states		V_L
	S	P	
1	0	1	V_{dc}
2	1	0	$2V_{dc}$

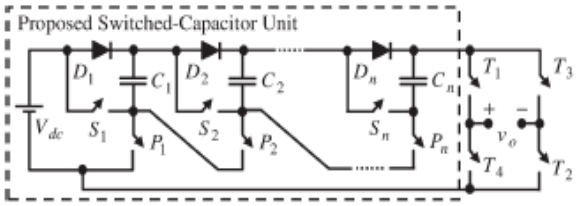


Fig. 2. Extended basic unit

In Fig. 2, the switches P_i (i=1,2,3…,n) connect the capacitors in parallel and the switches S_i (i=1,2,3…,n) connect the capacitors in series with the dc voltage sources. For producing the zero and negative output voltages, an H-bridge has been used at the output.

A. Suggested Topology

Fig. 3 shows the proposed multilevel Inverter. In this topology, two switched capacitor units have been connected in series by using H-bridges. The negative and zero voltage levels are produced by H-bridge as the basic unit can produce only the positive voltage levels.

The magnitude of the dc voltage sources can be determined in numerous ways. For this circuit, the magnitude of the dc voltage sources in the k^{th} unit follows the below relation:

$$V_k = (5^{k-1})\ V_1 . \quad (1)$$

Here, we have 2 DC sources. According to equation (1), we have

$$V_2 = 5V_1$$

This structure is called asymmetric multi-level inverter because of the dissimilarity in the magnitudes of the dc voltage sources.

There are 25 modes of operation for this proposed topology depending upon the on state of the switches for providing each level in the output voltage. Table III and IV gives the values of output voltages V_L for different states of switches S1, S2, P1, P2, T1, T2, T3, T4, T5, T6, T7 and T8 respectively. Note that there are various distinct switching sequences for producing the zero level and only one of them is shown in table III. In the tables III and IV the state conditions 1 means that the particular switch is ON and state condition 0 means that particular switch is OFF.

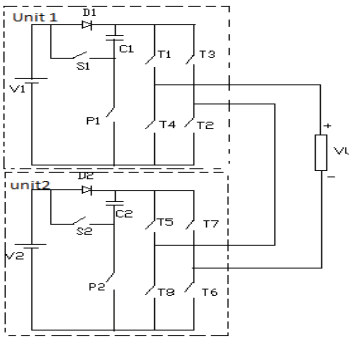


Fig. 3. Proposed topology

TABLE II
CALCULATION OF DIFFERENT PARAMETERS OF THE PROPOSED TOPOLOGY

Parameter	Formula	Value
N_{step}	5^k	5^2=25
N_{IGBT}	6k	6x2=12
N_{diode}	k	2
$N_{capacitor}$	k	2
N_{dc}	k	2
$(V_o)_{max}$	$2\sum_{i=1}^{k} V_1$	$2(V_1+V_2)$

TABLE III
SWITCHING TABLE FOR THE SUGGESTED HYBRID 25 LEVEL INVERTER FOR POSITIVE HALF CYCLE

Vl	S1	S2	P1	P2	T1	T2	T3	T4	T5	T6	T7	T8
0	0	0	1	1	0	0	0	0	0	0	0	0
V1	0	0	1	0	1	1	0	0	0	1	0	1
2v1	1	0	0	0	1	1	0	0	0	1	0	1
V2-2v1	1	0	0	1	0	0	1	1	1	1	0	0
V2-v1	0	0	1	1	0	0	1	1	1	1	0	0
V2	0	0	0	1	0	1	0	1	1	1	0	0
V2+v1	0	0	1	1	1	1	0	0	1	1	0	0
V2+2v1	1	0	0	1	1	1	0	0	1	1	0	0
2v2-2v1	1	1	0	0	0	0	1	1	1	1	0	0
2v2-v1	0	1	1	0	0	0	1	1	1	1	0	0
2v2	0	1	0	0	0	1	0	1	1	1	0	0
2v2+v1	0	1	1	0	1	1	0	0	1	1	0	0
2v2+2v1	1	1	0	0	1	1	0	0	1	1	0	0

TABLE IV
SWITCHING TABLE FOR THE SUGGESTED HYBRID 25 LEVEL INVERTER FOR NEGATIVE HALF CYCLE

0	0	0	1	1	0	0	0	0	0	0	0	0
-V1	0	0	1	0	0	0	1	1	0	1	0	1
-2v1	1	0	0	0	0	0	1	1	0	1	0	1
-V2+2v1	1	0	0	1	1	1	0	0	0	0	1	1
-V2+v1	0	0	1	1	1	1	0	0	0	0	1	1
-V2	0	0	0	1	0	1	0	1	0	0	1	1
-V2-v1	0	0	1	1	0	0	1	1	0	0	1	1
-V2-2v1	1	0	0	1	0	0	1	1	0	0	1	1
-2v2+2v1	1	1	0	0	1	1	0	0	0	0	1	1
-2v2+v1	0	1	1	0	1	1	0	0	0	0	1	1
-2v2	0	1	0	0	0	1	0	1	0	0	1	1
-2v2-v1	0	1	1	0	0	0	1	1	0	0	1	1
-2v2-2v1	1	1	0	0	0	0	1	1	0	0	1	1

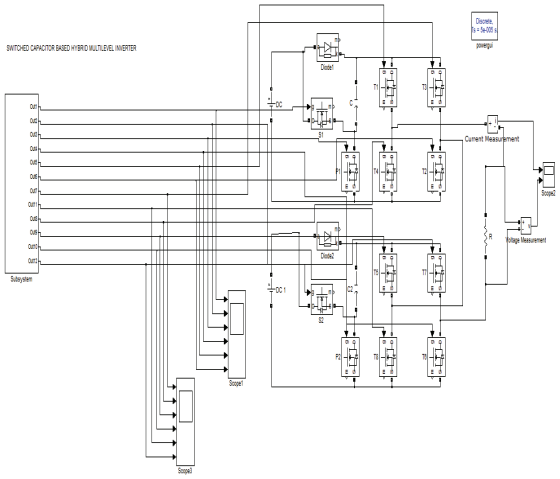


Fig. 4. Matlab/ Simulink model of Proposed Topology

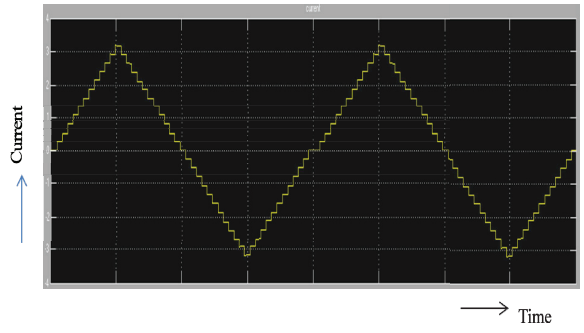
III. SOFTWARE IMPLEMENTATION AND RESULTS

Fig. 4 shows the simulation model of the proposed circuit. It is done using MATLAB/SIMULINK software for the single phase 25-level inverter to produce 50 Hz sinusoidal voltage waveform with load voltage V_L (rms) = 230V for resistive load. The magnitudes of dc voltage sources used are 27V and 135V respectively using the equation (1).

A. Symmetrical step control method

For switching to the bridge switches in MATLAB/SIMULINK pulse generators are used. According to the switching table, the Pulse Width (% of period) = n*(100/49) and Phase delay (sec) = m/50/49, where n and m are number of times the switch is ON and OFF respectively. It is given such that every level has equal duration. In terms of switching angle, each angle will be 7.5 degree which is $90^0/12$. Fig.5 shows the load voltage and current for R load of 100Ω respectively. The total harmonic distortion (THD) of the simulated 25-level load voltage is 14.57% using symmetrical step control method is shown in Fig. 6.

It can be noticed from fig. 5 that the output waveform has quarter wave symmetry. Also, the steps are symmetrical and the waveform is more like triangular rather than sinusoidal.



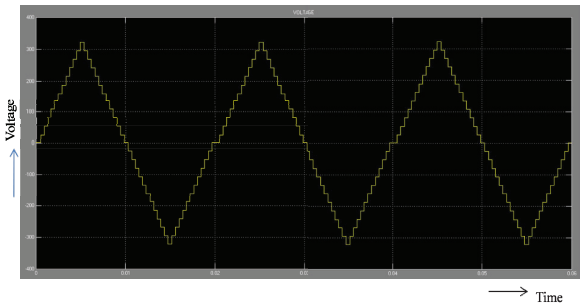


Fig. 5. Output current and voltage waveform for resistive load using SSCM

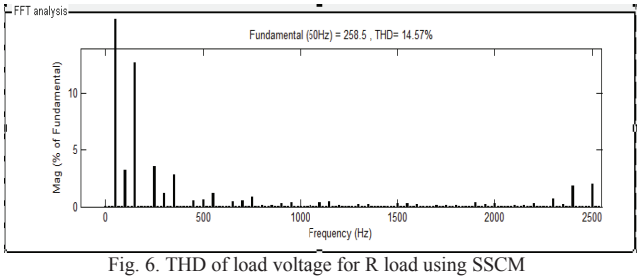


Fig. 6. THD of load voltage for R load using SSCM

B. Fundamental switching frequency method

In this method, a sinusoidal reference waveform is created and it is compared with the desired voltage levels (1 to 12pu). In MATLAB/SIMULINK, this is done by comparing a sinusoidal wave with constant lines of the required dc level. Fig. 7 shows the output voltage steps and the sinusoidal reference signal in this switching methodology. In this figure, V_{ref} and f_{ref} represents the magnitude and frequency of sinusoidal signal, respectively.

A sinusoidal reference waveform is created and it is compared with the desired voltage levels (1 to 12pu) and then the look –up table is created by programming it in MATLAB editor. This look up table is given to the appropriate switches in the switching table depending upon the modes of operation. Fig. 9 shows the load voltage and current for R load of 100Ω respectively. The total harmonic distortion (THD) of the simulated 25-level load voltage is 4.38% using fundamental switching frequency method is shown in Fig. 10.

From Fig. 10 it can be noticed that, by using fundamental switching frequency technique, all the steps in the output waveform are not symmetrical i.e., they don't have equal duration. Instead, the steps are in such a way that the resulting staircase output waveform is near to the reference sinusoidal waveform. Since the resulting output waveform is a near sinusoidal waveform, the THD obtained by using fundamental switching technique will be less as compared to symmetrical step control method.

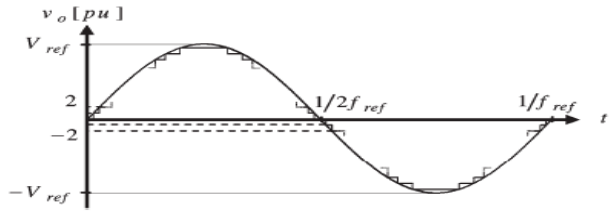


Fig. 7. Output Voltage level and Sinusoidal reference signal

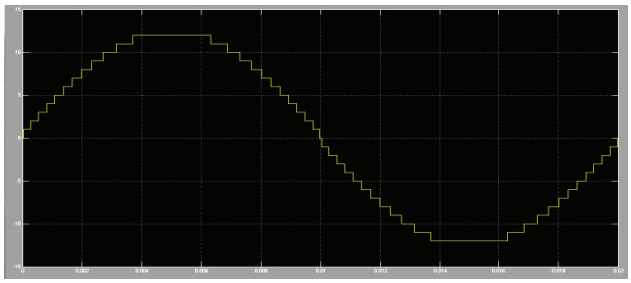


Fig. 8. Generated reference sinusoidal signal

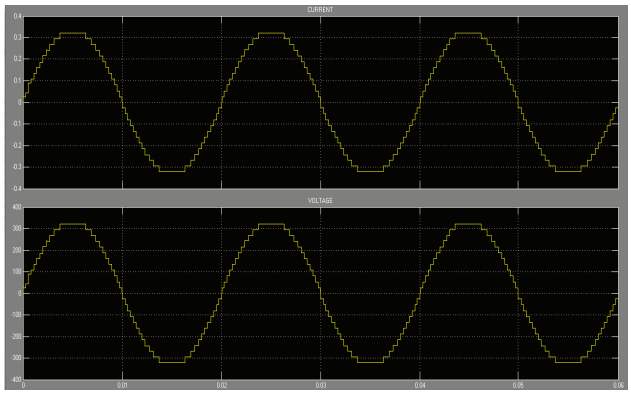


Fig. 9. Output current and voltage waveform for resistive load using FSFM

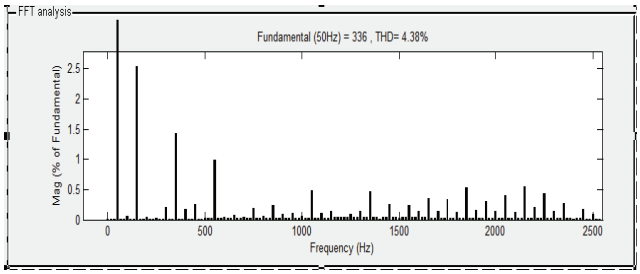


Fig. 10. THD of load voltage for R load using FSFM

Table V indicate that the THD changes from **14.21%** at no load to **15.36%** at full load in case of Symmetrical step control method and from **4.35%** to **4.50%** in case of fundamental switching frequency method. Hence the increase in THD due to loading effect is only **1.15%** in case of SSCM and **0.15%** in case of FSFM which is an advantage.

TABLE V

THD COMPARISON BETWEEN SSCM AND FSFM FOR DIFFERENT RESISTIVE LOADS WITHOUT FILTER CIRCUIT

Power output(W)	**THD**	
	Symmetrical step control method(SSCM)	Fundamental switching frequency method(FSFM)
500	15.36%	4.50%
250	15.03%	4.42%
100	14.57%	4.38%
50	14.49%	4.36%
No load	14.21%	4.35%

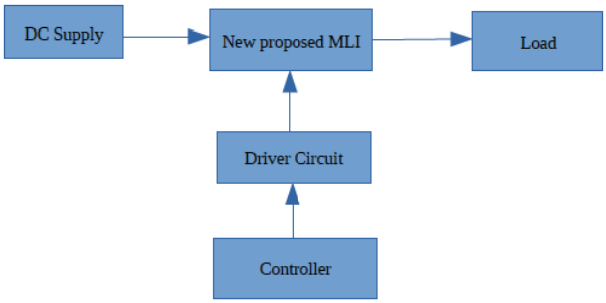


Fig. 11. Block diagram of hardware Implementation model

IV. EXPERIMENTAL VERIFICATION

Fig. 11 represents the block diagram for implementation of experimental prototype.

An isolated driver circuit is provided for each switch. The optocouplers provide the required isolation to protect the control circuit. The FPGA provides the gating signals for the driver circuits which in turn drive the switches.

The IGBT's utilized in the prototype are G4PH50UD. The FPGA Spartan 3E board is used to generate gate switching signals.

XILINX 14.5 is the software used to design the system. The process for implementing a design on FPGA is basically divided into five steps:

- Design entry
- Behavioral Simulation
- Design synthesis
- Implementation
- Device programming

This is the process through which we write the code in VERILOG for creation of gating signals. The next step is behavioral simulation which verifies whether the design entered is functionally correct or not. The result of simulated wave using inbuilt ISE simulator is shown in Fig. 12. Finally device programming is done to program the FPGA.

Fig. 13 shows the photograph of the experimental prototype and Fig. 14 shows the approximated sine-wave produced by inverter across load as recorded in oscilloscope.

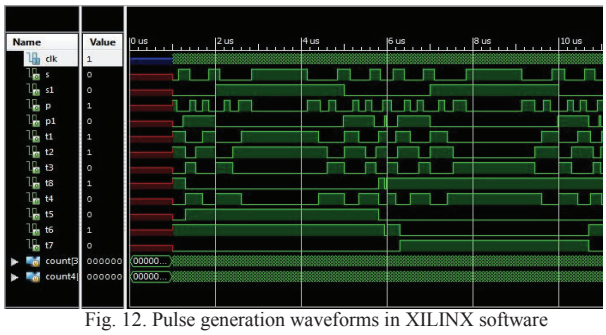


Fig. 12. Pulse generation waveforms in XILINX software

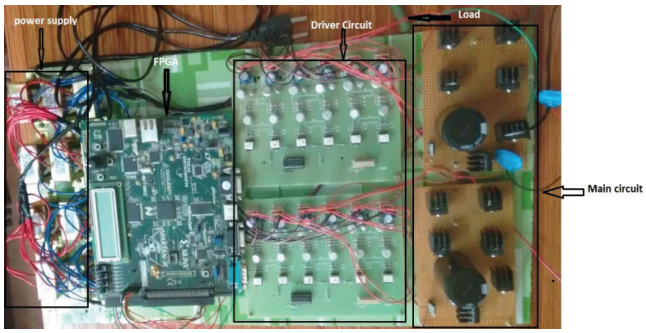


Fig. 13. Photo of Hardware

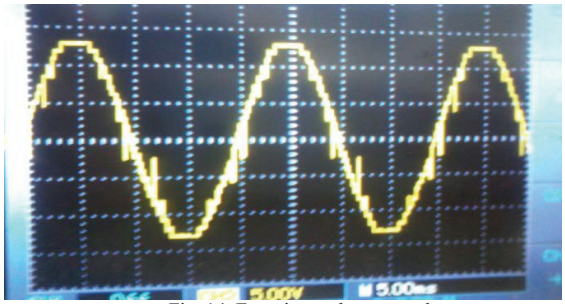


Fig. 14. Experimental output voltage

V. CONCLUSION

A new asymmetric multilevel inverter topology has been proposed through this work. It was shown that the proposed topology generates a 25-level voltage by using 12 IGBT's, 2 diodes, and 2 isolated dc input voltage sources. Thus it reduces the input dc voltage sources, utilizes fewer switching devices and also lessens the size and cost of the system in comparison with conventional topologies. In addition, the proposed topology can boost the input voltage without any transformer. Two types of switching technique i.e. Symmetrical Step Control Method and Fundamental Switching Frequency Method were used as the switching techniques for the asymmetric multilevel Inverter. And it is seen that Fundamental switching method was found to have lower THD values as compared to symmetrical step control method. Since, the THD obtained by fundamental switching scheme is less than 5%; the resulting load current and voltage can be considered as almost "clean" sinusoids. The simulations performed were validated with experimental tests and the results thus obtained from this 25-level inverter showed close proximity to each other and are very acceptable.

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