

2011 41st IEEE International Symposium on Multiple-Valued Logic

## Design of high performance Quaternary adders

Vasundara Patel K S  
 Dept of ECE, BMSCE  
 BMS College of Engg, VTU  
 Bangalore, India  
 e-mail: [vasundara.rs@gmail.com](mailto:vasundara.rs@gmail.com)

K S Gurumurthy  
 Dept of E&C, UVCE  
 University Vishweshraiya College of Engg,  
 Bangalore, India  
 e-mail: [drksgurumurthy@gmail.com](mailto:drksgurumurthy@gmail.com)

**Abstract**—Design of the binary logic circuits is limited by the requirement of the interconnections. A possible solution could be arrived at by using a larger set of signals over the same chip area. Multiple-valued logic (MVL) designs are gaining importance from that perspective. This paper presents two types of multiple-valued full adder circuits, implemented in Multiple-Valued voltage-Mode Logic (MV-VML). First type is designed using one hot encoding and barrel shifter. Second full adder circuit is designed by converting the quaternary logic in to unique code, which enables to implement circuit with reduced hard ware. Sum and carry are processed in two separate blocks, controlled by code generator unit. The design is targeted for the 0.18  $\mu\text{m}$  CMOS technology and verification of the design is done through Synopsis HSPICE and COSMOSCOPE Tools. Area of the designed circuits is less than the corresponding binary circuits and quaternary adders because number of transistors used are less.

**Keywords**- Down literal circuit, multi-level logic, quaternary full adder, One hot encoding.

### I. INTRODUCTION

Current digital electronics technologies are mainly based upon binary systems. Multi-valued systems are usually proposed to provide advantages by decreasing the number of data interconnect lines and processing elements [1]. Such logic circuits can represent numbers with fewer bits than binary, e.g. the decimal number 255 is represented as 1111 1111 in binary and 3333 in quaternary. As the circuits become less complicated, the data processing may be fast and reliable [2, 3]. However, multi-valued logic designs may be challenging due to difficulties in implementation [4]. The idea of the multiple-valued logic, or fuzzy logic opened a vast research area. In 1920, Jan Lukasiewicz begins to create a system of many-valued logic [5]. Later Jan Lukasiewicz and Alfred Tarski together formulated logic on  $n$  truth values where  $n$  was equal to or more than two [6]. In 1973, Lotifi A Zadeh proposed his theory of fuzzy logic [7]

Power reduction has been a research goal for several years and there have been many important results achieved [8]. The reduction of system noise, however, is still a lower research priority at the architectural level. Power dissipation in most integrated systems is mainly dynamic and dependent upon the voltage swing magnitude and frequency across load capacitances [9,10].

Two types of full adders are demonstrated in this paper. In the first type, Quaternary signals are converted to hot codes and after addition, output is available in quaternary

logic only, where as in the second type quaternary input is converted to unique code. After addition operation, output is obtained in quaternary, For both the cases radix converters are not required at the output side.

This paper is organized as follows. In section two, full adder using one hot encoding is demonstrated. In section three, full adder using unique encoding for quaternary inputs is explained. Section four explains the conclusion part of the paper.

### II. FULL ADDER USING ONE HOT ENCODING (TYPE I)

Proposed block diagram of the quaternary full adder is shown in figure 1, which uses barrel shifter for sum calculation. This is a novel circuit with one hot encoder. Barrel Shifter is controlled by two inputs A and B. The carry block consists of simple selection and enabling of carry output depending on the inputs A, B and Carry in. Carry input will be pre-added to the one hot encoder. Logic levels of quaternary inputs 0, 1, 2 and 3 are represented by the voltage levels of 0V, 1V, 2V and 3V respectively. A and B are the two quaternary inputs to the full adder. Table 1 shows all possible combinations of inputs when carry input is zero and Table 2 shows the all possible combinations of inputs when carry input is one.

TABLE I: TRUTH TABLE OF QUATERNARY FULL ADDITION WHEN CARRY IN IS 0

		Sum				Carry					
		B				B					
A		0	1	2	3		0	1	2	3	
	0	0	1	2	3	0	0	0	0	0	0
	1	1	2	3	0	1	0	0	0	1	1
	2	2	3	0	1	2	0	0	1	1	1
	3	3	0	1	2	3	0	1	1	1	1

TABLE 2: TRUTH TABLES OF QUATERNARY FULL ADDITION, WHEN CARRY IN IS 1.

		Sum				Carry					
		B				B					
A		0	1	2	3		0	1	2	3	
	0	1	2	3	0	1	0	0	0	1	1
	1	2	3	0	1	2	1	0	1	1	1
	2	3	0	1	2	3	2	0	1	1	1
	3	0	1	2	3	3	3	1	1	1	1

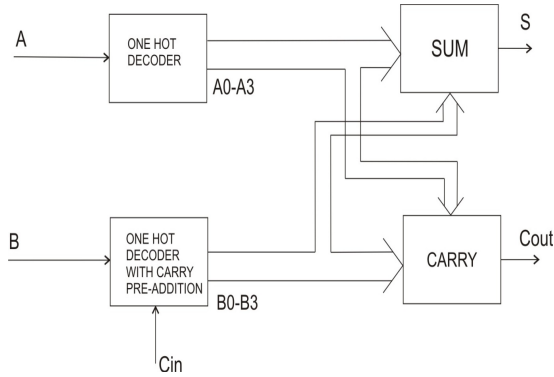


Figure 1: Block diagram of Proposed Quaternary Full Adder.

**A. One hot encoder block**

One hot encoder is shown in figure 2 for some input X. Input X will generate four hot codes Hx0, Hx1, Hx3 and Hx4 using DLC1, DLC2, DLC3, 2 XOR gates and one inverter. Hot signals generated in the one hot encoder are used to switch the corresponding voltage levels to output. These hot codes are shown in table 3. Since full adder uses two inputs A and B, it requires two one hot encoders and hot codes will be similar to table 3.

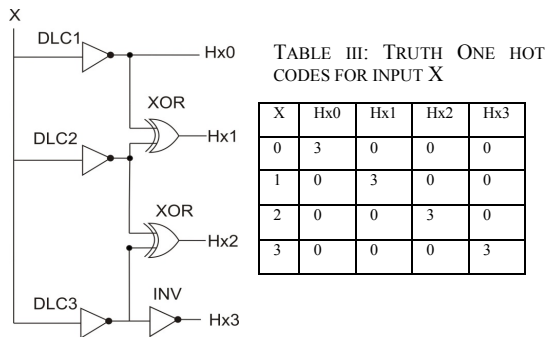


Figure 2: Common Encoding circuit for some input X

TABLE IV: ONE HOT CODE FOR INPUT B WHEN (A) CARRY IN = 0

(B) CARRY IN = 1

B	B0	B1	B2	B3
0	3	0	0	0
1	0	3	0	0
2	0	0	3	0
3	0	0	0	3

B	B0	B1	B2	B3
0	0	3	0	0
1	0	0	3	0
2	0	0	0	3
3	3	0	0	0

(a)

(b)

**B. Encoding for the input B with carry Pre-addition**

The encoding part shown in figure 3 consists of a one hot decoder with carry pre-addition. Based on the inputs one of the output lines will be high and all others will be low. The detailed circuitry includes down literal circuits, binary XOR gates along with binary inverters to get a proper one hot output. Since the adder to be designed is a full adder we should also take care of the carry input. Hence carry pre addition is done to the input B before the output is shared between Sum and Carry generators. The truth tables are shown in table 4.

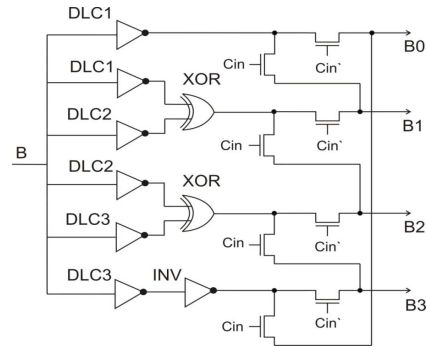


Figure 3: Circuit diagram of one hot encoding for carry pre addition

**C. Summer Block**

From the truth table of a full adder it is clear that the sum part of the adder is nothing but a shift of one input depending on the other. So a barrel shifter is used to minimize the circuitry where continuous quaternary voltage levels 0V, 1V, 2V and 3V are provided, which are directly switched to the outputs depending on the encoded values of the inputs. Hence the barrel shifter here uses a wired AND logic to drive the output line. Figure 4 shows the circuit diagram of sum generator where A0-A3, B0-B3 are the outputs from the one hot encoder block, and Sum is the output of the sum block.

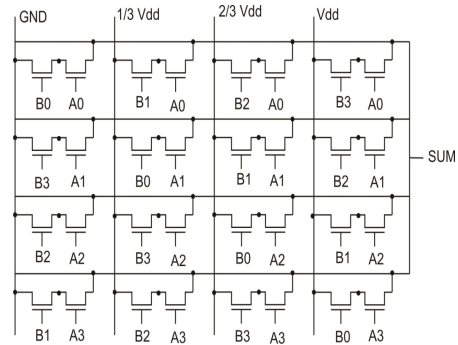


Figure 4: Logic circuit of Sum block

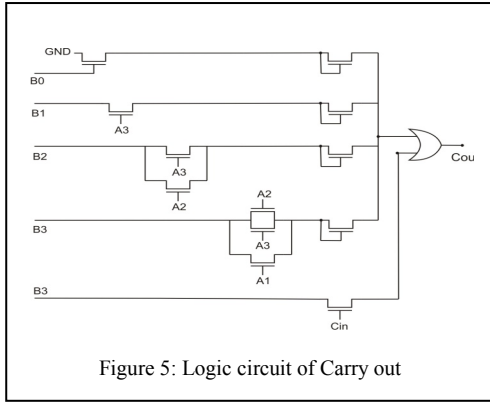


Figure 5: Logic circuit of Carry out

The carry generation block used is just a combination of inputs where one input line acts as select line and selects or rejects another line based on whether the combination of input is meeting the requirements of generating carry output. The carry pre-addition action which takes place in the first part of the adder, eliminates the carry part if input B is 3V and carry in is high hence an OR gate is used to save that carry and drive it to carry out in the carry generation circuit. Figure 5 shows the circuit diagram of carry generator.

### III. FULL ADDER USING UNIQUE ENCODING (TYPE II)

Proposed full adder circuit is based on Encoder, code generator, sum block and carry block. Encoder is required for the conversion shown in table 5, consists of DLC1 and DLC3 (Down literal circuit) [12]. Output codes of the Code generator are used to generate sum and carry of the full adder circuit. Block diagram of the full adder circuit is shown in figure 6. Logic levels of quaternary inputs 0, 1, 2 and 3 are represented by the voltage levels of 0V, 1V, 2V and 3V respectively. X and Y are the two quaternary inputs to the full adder. Table 1 shows sum and carry for all possible combinations of inputs when carry input is zero. Table 2 shows sum and carry for all possible combinations of inputs when carry input is one.

#### A. Encoder block

Proposed full adder circuit consists of encoder block which converts quaternary numbers X and Y into binary representation as shown in table 5. Output of the encoder is fed to the code generator unit. This code generator unit generates codes which are utilized for the sum and carry block to generate final value of sum and carry. Encoder block consists of DLC1, DLC3, binary X-OR gate and two inverters. Logic diagrams of encoder circuits are shown in figure 7.

#### B. Code generator block

Block diagram of the Code generator for X and Y is shown in figure 8. As seen in the previous section Quaternary input X is split up in to two equivalent binary numbers Xp and Xq. These two signals are used to generate Hx0, Hx1, Hx2, and Hx3. Quaternary input Y is split up in to two equivalent binary numbers Yp and Yq. These two

signals are used to generate Hy0, Hy1, Hy2, and Hy3. Figure 9 shows the circuit diagram of the code generator. It consists of four AND gates.

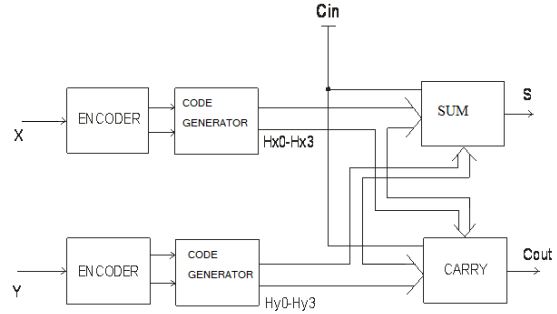


Figure 6: Block diagram of the full adder using unique encoding

TABLE V: REPRESENTATION OF QUATERNARY TO BINARY CONVERSION

X(Y)	Xp(Yp)	Xq(Yq)
0	0	0
1	1	0
2	1	1
3	0	1

#### C. Sum and carry block.

Sum and carry blocks are built with pass transistors. Pass transistors can be replaced by transmission gates for proper logic levels. Quaternary voltage levels are switched towards output according to the levels of the input. The codes generated by the code generator blocks Hx0, Hx1, Hx2, Hx3, Hy0, Hy1, Hy2 and Hy3 are used to control these pass transistors. Circuit diagrams for sum and carry are shown in figure 10 and figure 11 respectively.

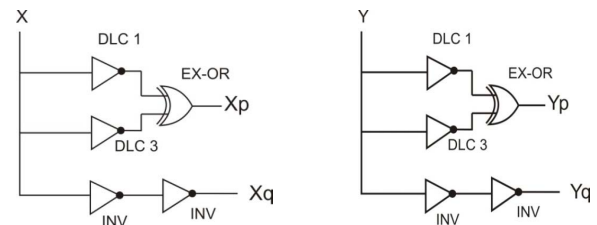


Figure 7: Logic diagrams of encoder circuits

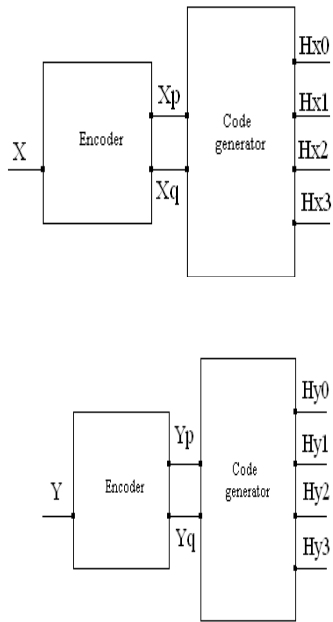


Figure 8: Block diagram of Code generator for quaternary input X and Y

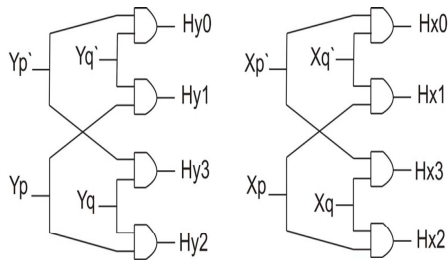


Figure 9: Code generator circuit for quaternary input X and Y

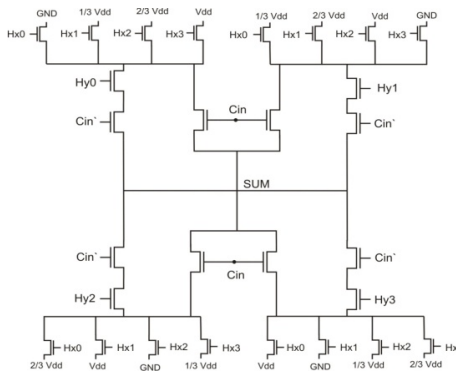


Figure 10: Circuit diagram for sum block for quaternary adder

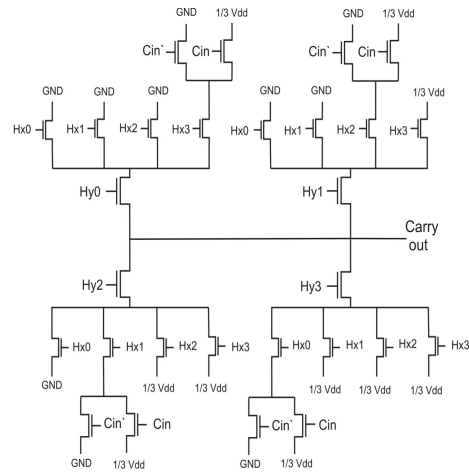


Figure 11: Circuit diagram of carry block for quaternary full adder

#### IV. CONCLUSION

In this paper we have discussed and demonstrated a design technique for two types of quaternary full adders. quaternary full adder (Type I) is designed with down literal circuit, code generators, Sum and Carry blocks. This circuit requires 148 transistors and dissipates 84 $\mu$ W at 250MHz. In Type II full adder, unique encoding for the quaternary input has reduced the requirement of the complex hardware which enables to implement high performance quaternary full adder. This circuit requires 113 transistors and dissipates 91.25  $\mu$ W. Simulation of the proposed circuits is carried out targeted for 180nm technology using Synopsis HSPICE and COSMOS tools. These circuits consume less number of transistors and shows high performance compare to the other circuits.

TABLE VI: TABLE OF COMPARISON

Author	Technology	Propagation delay	Transistor count	Dynamic power dissipation
RecardoCuna et.al [11] 2006	180nm 3V	2.24ns	332	181 $\mu$ W(250MHz)
	180nm 3V	2.66ns	276	762 $\mu$ W(250MHz)
Hirokatsu Shirahama et.al[13]2008	90nm, 1.2V	113ps	252	55 $\mu$ W(1G Hz)
Hirokatsu Shirahama et.al[14]2007	180nm 1.8V	1.4ns	194	194 $\mu$ W( 300MHz )
Type I fulladder	180nm 3V	783.3pS	113	91.25 $\mu$ W(250MHz)
Type II full adder	180 nm, V	2.02ns	148	84 $\mu$ W(250MHz)

## REFERENCES

- [1] Mahsa Dornajafi et al. "Performance of a quaternary logic design", IEEE Region 5 Conference, pp.1-6, April 2008.
- [2] K. C. Smith, "Multiple-valued logic: a tutorial and appreciation," IEEE *Computer*, vol.21, no.4, pp. 17-27, Apr. 1988.
- [3] John K Buttler, "Multiple-valued logic – Examining its use in Ultra high speed Computation", IEEE Potentials, vol.14, no. 2, pp.11-14, 1995
- [4] Shanthanu Mahapatra and Adrian Mihai Ionescu, "Realization of Multiple-valued logic and memory by Hybrid SETMOS Architecture", IEEE transaction on Nanotechnology, vol.4, no.6, pp.705-714, 2005.
- [5] Jan Lukasiewicz, "Selected works", editor L. Bokowski and translator O. Wojtasiewicz (North Holland Publishing Co.), Amsterdam, 1970.
- [6] S.Feferman. "Tarski's Influence on computer Science", 20<sup>th</sup> annual symposium on Logic in Computer Science, Chicago, Illinois, 20-29 June 2005.
- [7] Lofti A Za.Zadeh, "Fuzzy Sets, fuzzy Logic, and Fuzzy Systems, Selected paper by Lofti A Za.Zadeh", Advances in Fuzzy systems Application and theory Vol. 6 (World Scientific Publishing Co) Singapore 1996.
- [8] A.P. Chandrakasan, S. Sheng, and R.W. Broderson, "Low-Power CMOS Digital Design", IEEE J. Solid-State Circuits, vol. 27, pp. 473-483, 1992.
- [9] Aryan Sae' d, Member, IEEE et.al, "A Number System with Continuous Valued Digits and Modulo Arithmetic", IEEE Transaction on computers VOI 51, No 11, November 2002.
- [10] Douglas A. Pucknell, Kamran Eshraghian, "Basic VLSI Design" third Edition, PHI (Prentice Hall India), 2005.
- [11] Ricardo Cunha G. da Silva, "A novel voltage mode CMOS quaternarylogic design", IEEE Transactions on Electron devices, vol.53, no 6, June 2006.
- [12] Vasundara Patel K.S, K.S. Gurumurthy, "Multi-valued Logic Addition and Multiplication in Galois Field", IEEE, International Conference on Advances in Computing, Control and Telecommunication Technologies, ACT 2009, pp.752-755, 28<sup>th</sup>-29<sup>th</sup> December 2009.
- [13] Hirokatsu Shirahama and Takahiro Hanyu et.al, "Design of a Processing Element Based on Quaternary Differential Logic for a Multi-Core SIMD Processor", ISMVL, Proceedings of the 37th International Symposium on Multiple-Valued Logic, 43, 2007.
- [14] Hirokatsu Shirahama and Takahiro Hanyu, "Design of High-Performance Quaternary Adders Based on Output-Generator Sharing", Proceedings of the IEEE, 38th International Symposium on Multiple Valued Logic, pp.8-13, 2008.