CORE
Metadata, citation and similar papers at core.ac.uk
Provided by ePrints@Bangalore University

IMPACT OF DEVICE PARAMETERS OF TRIPLE GATE SOI-FINFET ON THE PERFORMANCE OF CMOS INVERTER AT 22NM

Prathima. A[1], Kiran Bailey [2], K.S.Gurumurthy [3]

[1, 2] Department of Electronics and Communication Engineering, BMSCE, Bangalore
[1]prathima.prathi@gmail.com
[2]kiranbailey@gmail.com
[3]Department of ECE, UVCE, Bangalore University, Bangalore
[3]drksgurumurthy@gmail.com

ABSTRACT

A simulation based design evaluation is reported for SOI FinFETs at 22nm gate length. The impact of device parameters on the static power dissipation and delay of a CMOS inverter is presented. Fin dimensions such as Fin width and height are varied. For a given gate oxide thickness increasing the fin height and fin width degrades the SCEs, while improves the performance. It was found that reducing the fin thickness was beneficial in reducing the off state leakage current (I_{OFF}), while reducing the fin height was beneficial in reducing the gate leakage current (I_{GATE}). It was found that Static power dissipation of the inverter increases with fin height due to the increase in leakage current, whereas delay decreased with increase fin width due to higher on current. The performance of the inverter decreased with the downscaling of the gate oxide thickness due to higher gate leakage current and gate capacitance.

KEYWORDS

DIBL, Process and Device simulation, SCEs, SOI FinFETs, Sub threshold Slope, TCAD

1. INTRODUCTION

Following the International Technology Roadmap of Semiconductors (ITRS), various non-classical silicon on insulator (SOI) device structures having thin silicon bodies promise increased transistor speed, reduced power consumption and enhanced device scalability. Several innovative multiple gates SOI structures such as Double Gate (DG) MOSFET [1], fully depleted lean channel transistor (DELTA) [2] "Gate All Around"(GAA) MOSFET [3], Pi-gate MOSFET [4] and FinFET [5-8], have been proposed by various researchers. It is expected that sustained scaling during the next decade will see the complete evolution from the single gate (SG) conventional device to the above mentioned multiple gate MOSFETs (MuGFETs)[9]. One of the main advantages of MuGFETs is that they offer superior scalability with manufacturability of conventional planar transistors. The self-aligned gates wrapping around both sides of the fin can be fabricated with a single lithography and etch step. On the other hand, the fabrication process of MuGFETs suffers from some process challenges such as the precise control of the fin width and fin height and non-uniformity of the gate oxide on the etched sidewall of the fin, which is difficult to achieve. Similarly, the channel–oxide interface condition is determined by the sidewall roughness of the fin and large parasitic resistance between the channel and source/drain is another challenge to the performance of MuGFET devices. Since real devices go through many processing steps, reliable evaluation or design optimization of final devices depend on the optimized unit process development.

DOI : 10.5121/vlsic.2012.3507

Technology Computer Aided Design or TCAD process simulation is therefore a prerequisite to device optimization or device design through device simulation. Due to the inherent link between process simulation and device simulation enabling the full optimization loop from unit process to device characteristics, one can correlate the electrical behavior of the device with small changes in the unit processes (e.g.time, temperature, doses, and energies). Since the process simulation enables virtual processing and in this way explores parameter space of processing options, a necessary prerequisite is that the processes to be modeled have adequately been implemented in the modeling software and that the required parameters have been calibrated.

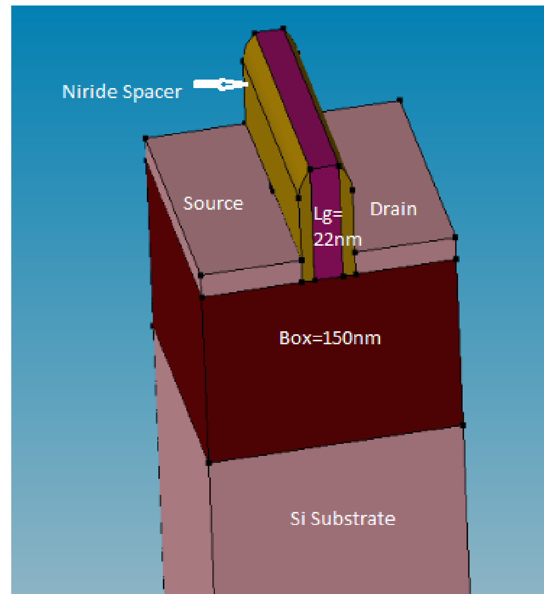


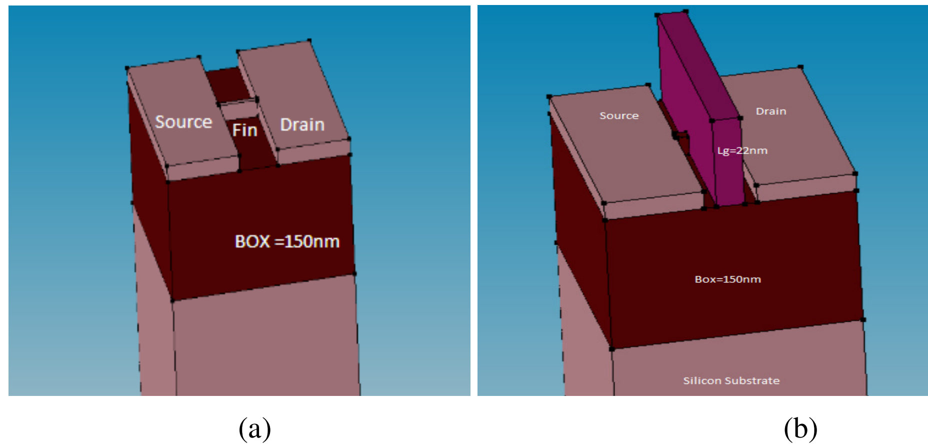
Figure 1: 3D Cross sectional view of a 22nm triple gate SOI FinFET device.

Double gate and Triple gate FinFETs are promising candidates because of their quasi-planar structure, excellent roll-off characteristics, drive current and they are close to their root, the conventional MOSFET in terms of layout and fabrication. FinFET devices are explicitly mentioned in the ITRS roadmap and have a good potential for scaling CMOS to 22 nm and below**.** Such devices include double gate FinFETs, Triple gate or Multigate FinFETs and allow the scaling down to sub-50nm gate length. Both logic and SRAM FinFET technologies have been previously demonstrated [10]. Previous work have shown the performance and power advantage of FinFET circuits over bulk CMOS [11-13]. FinFET technology has been used to improve the performance, standby power consumption, and variability in nanoscale-CMOS digital ICs, which find its application in SRAM Cells extensively [14].

Pei et al. [15] have presented design consideration based on 3D analytical modeling using Laplace equation. Short-channel effects (SCEs) and subthreshold behaviour of FinFETs were studied with different fin height, fin thickness and channel length. Muhammad Nawaz et [16] has evaluated the performance of 30nm SOI FinFET for different device parameters within the context of assessing the device design and underlying fabrication process. He has compared the performance of SOI FinFETs with the Bulk FinFETS for their usage in DRAM, SRAM and I/O applications [17]. Muhammad Nawaz has demonstrated SRAM cells and ring oscillators with inverter delay of 13.9 pS using metal gate SOI FinFETs [18].

To bring more functionality to a chip, the number of transistors is increased, resulting in increased power density and total power consumption. Total power consumption is dominated by active

power during switching of a transistor. However, in deep submicrometer technology nodes, the contribution of leakage power dissipation (due to sub threshold and gate leakage) to the total power is increasing. Increased power results in high die temperatures and hence necessitates efficient cooling solutions. Aditya Bansal and Kaushik Roy have analysed FinFET based circuits for leakage and static power dissipation for thermal runaway [19,20].



(a) (b)

Figure 2: Internal view of (a) SOI FinFET showing the Fin and (b) Poly gate wrapping around the Fin

This work focuses on the implementation of a complete process flow of 22nm triple gate SOI FinFET into a commercially available numerical 3D process and device simulation environment. Modelling, Analysis and Device Characterization of the device is carried out by implementing a full process flow using a commercial three-dimensional technology CAD (TCAD) tool. The device parameters are varied and the impact of the device parameters on the performance of CMOS inverter has been presented by evaluating the inverter for static power dissipation and delay.

2. Process And Device Simulation

The Device targeted here is 22nm triple gate SOI based FinFET. This section describes the complete modeling and simulation of the device. We also discuss the circuit performance of the device in a CMOS inverter.

2.1. Process simulation

Commercially available TCAD Sentaurus-process and Sentaurus-device simulators from Synopsys [21] have been used in this work. Semiconductor process simulation is the modeling of the fabrication of semiconductor devices. The ultimate goal of process simulation is an accurate prediction of the active dopant, stress distribution and the device geometry. The critical process steps for FinFETs on standard SOI involve fin formation, gate oxide growth, gate formation (100nm polysilicon), spacer formation (silicon nitride) and source-drain formation. No halo implants were used for setting threshold voltage in the nominal process flow. Figure 1 shows 3D cross sectional view of the triple gate SOI FinFET device with all regions. Figure 2 shows the internal view of the device showing the thin fin formed between source and drain in a NSOI FinFET. Figure also shows the patterned fin wrapped under the poly gate.

Table 1 summarizes the device parameters and their dimensions for a nominal device. Process Simulation is carried out by meshing the device and generating the mesh for the further device simulation.

Table 1: Nominal Device Dimensions

DEVICE PARAMETERS	VALUE (nm)
Gate length	22
Fin Width	5
Fin Height	20
Gate Oxide	1.5
Spacer Width	10
BOX Thickness	150

2.2. Device Simulation

Device simulation starts from the output of process simulation. Device simulation tools simulate the electrical characteristics of semiconductor devices, as a response to external electrical, thermal or optical boundary conditions imposed on the structure. Device simulations have been performed using Hydrodynamic carrier transport model, which solves the carrier temperature and heat flow equations in addition to the Poisson and carrier continuity equations. This model is useful in simulating devices ranging from deep submicron MOSFETs beyond the 0.18µm generation and heterostructure devices. I_{OFF} was defined at V_{GS}=0V, and V_{DS}=1V. Similarly, I_{ON} was defined at V_{GS}=V_{DS}=1V.

2.3. CMOS Inverter Realization

The performance of the SOI FinFET devices has been evaluated by implementing the devices in the basic inverter circuit comprising of a PSOI FinFET and a NSOI FinFET device with 22nm gate length. The width ratio of PMOS to NMOS is 2:1 to obtain symmetrical characteristics.

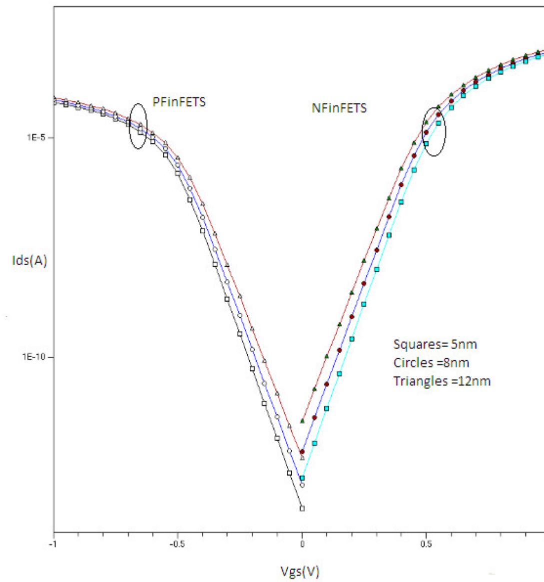
The dual fin architecture provides for the necessary area factor. Mixed mode simulations are carried out to realize the inverter circuit. The Noise margins and delays are calculated from the inverter's voltage transfer characteristics and transient response curves respectively. The total gate capacitance of the device is obtained by simulating the device for AC analysis and obtaining the CV (capacitance- voltage) sweep. The main aim is to control the off state leakage current and direct gate tunnelling current thereby minimizing the total static power dissipation of the circuit. The power and delays for other dimension variations are calculated analytically and analysed.

3. RESULTS AND DISCUSSION

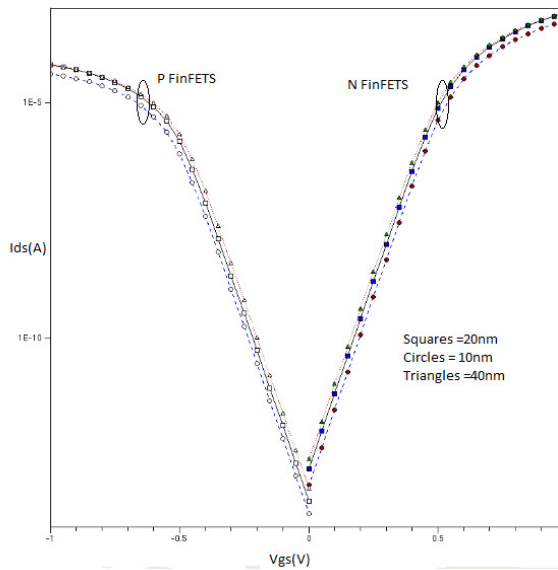
Following the process flow, the 22nm gate length SOI FinFET is simulated for various device parameter variations and the transfer characteristics are obtained. Also the SCEs are noted for each case and analysed in this section. Figure 3 shows the transfer characteristics of the device with varying fin width for a fixed fin height and also for varying fin height for fixed fin width. As the fin widths are varied for 5, 8, 12nm and fin heights through 10, 20 and 40nm the on current and transconductance increases. On current increases linearly for thicker and higher fin devices.

For example on current increases from 0.824mA to 1.08mA (31%) for a fin width increase from 5nm to 12nm for a fixed fin height of 20nm whereas increases from 0.558mA to 0.837mA (50%) for a fin height increase from 10nm to 40nm for a fixed fin width of 5nm.That is, the transconductance increases by 27.3% and 44% for fin width and fin height variations respectively. Both I_{ON} and I_{OFF} increase with the increase in fin width. With increasing fin width, I_{OFF} increases from 0.171pA to 3.42pA, which is because of increased short channel effects, while I_{ON} increases due to decreased external resistance and threshold voltage. The on/off-current

behavior extracted from fin height variation shows that the on current increases quasi-linearly with fin height, while off current remains approximately unaffected at fixed fin width. For a given gate length, the simulation results show that on current is higher for taller fin devices.



(a)



(b)

Figure 3: Transfer characteristics of SOI FinFET for different (a) Fin Widths and (b) Fin heights

It is found that fin width is the dominant factor that controls the short channel effects. Figures 4 and 5 show the SCE behavior for fin width and fin height variations. Figures show off state leakage current (I_{OFF}), threshold voltage (V_{TH}), drain induced barrier lowering (DIBL), sub threshold voltage slope (SS) and gate leakage current (I_{GATE}) behavior for varying fin widths and fin heights. We observe that the subthreshold slope, drain induced barrier leakage and I_{OFF} are quite sensitive to the variation in fin width. For example DIBL and SS change from 33 to 59mV/V (69%) and 63.7 to 69.8 mV/dec (8.2%) respectively, with fin width variation from 5 to

12nm at 20nm fin height. The threshold voltage decreases from 0.707V to 0.689V (2.6%), when fin width is increased from 5nm to 12nm for an NSOI FinFET.

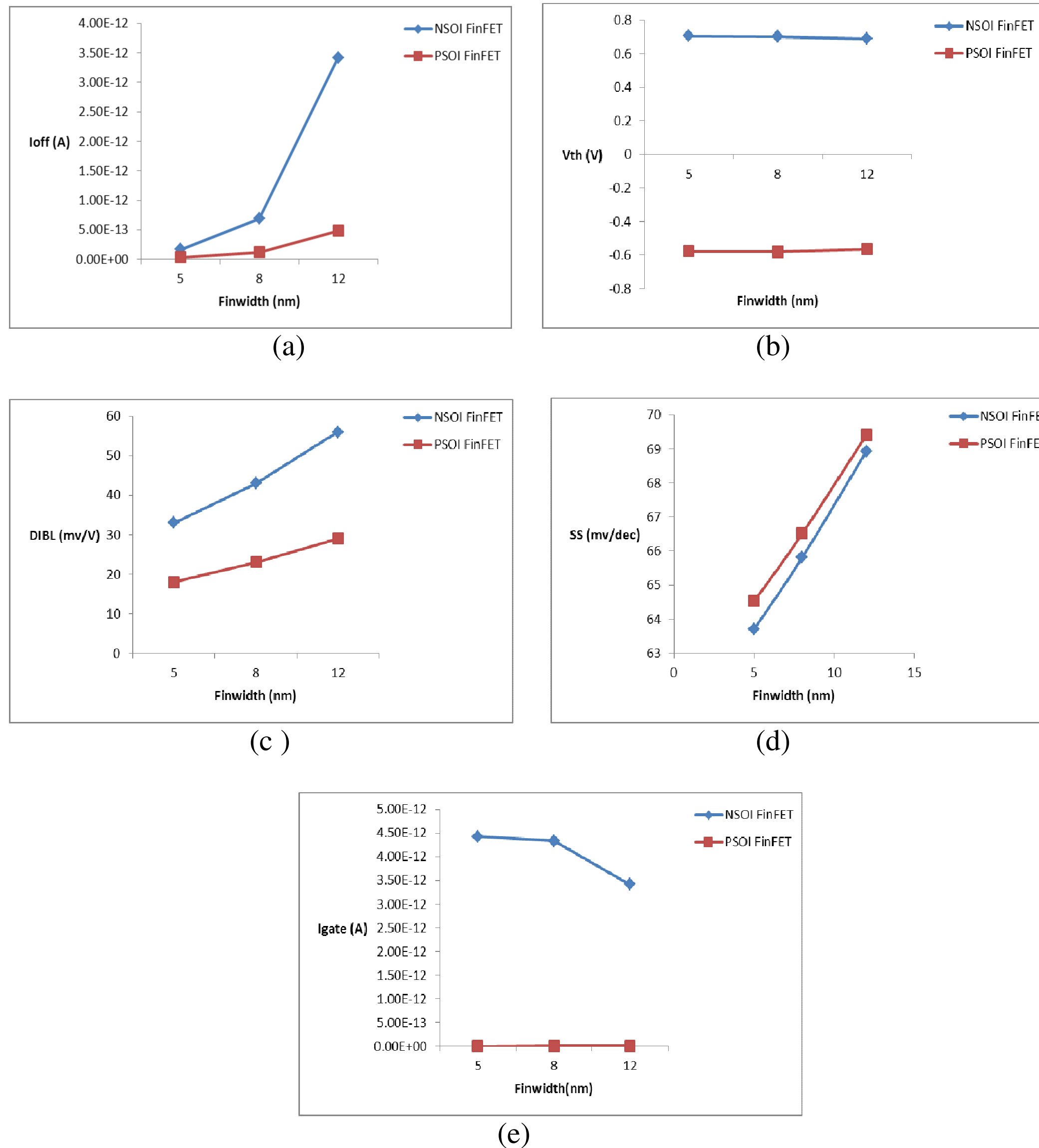


Figure 4: Impact of Fin width on (a) I_{OFF} behavior, (b) Threshold Voltage, (c) DIBL, (d) Subthreshold Slope and (e) Gate leakage current.

As ultra thin oxide is needed for scaled sub-50nm MOSFETs, direct tunneling current results in exponential increase in the gate leakage current, increased power consumption and hence deterioration in the device performance. The SCE behaviour of the devices for different oxide thickness of 1,1.5 and 1.8 nm at fixed fin width and fin height, are reported in Figure 6.

As the gate dielectric gets thinner, the gate voltage controls the channel more effectively. The effect of DIBL and SS also reduces with thinner gate oxide.A quasi-linear decrease in DIBL and SS was observed with varying gate oxide from 1.8 to 1 nm. DIBL and SS change from 36 to 28mV/V(28.5%) and 64.3 to 62.7 mV/dec(2.5%), respectively, with gate oxide thickness

reducing from 1.8 nm to 1nm at fixed fin width and fin height for a N type FinFET.The threshold voltage decreases by 1.6% i.e 0.1V decrease for approximately 1nm reduction in gate

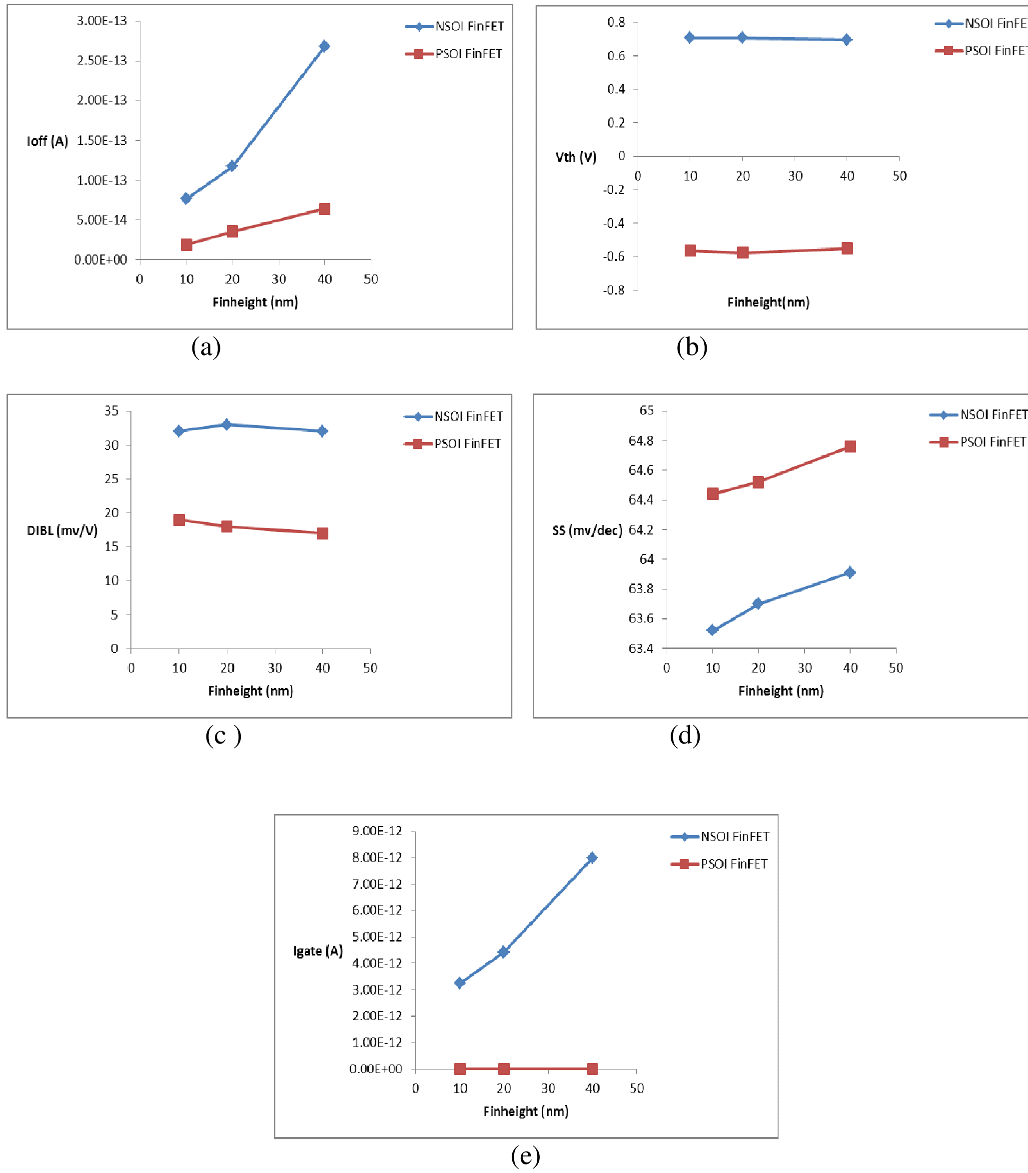
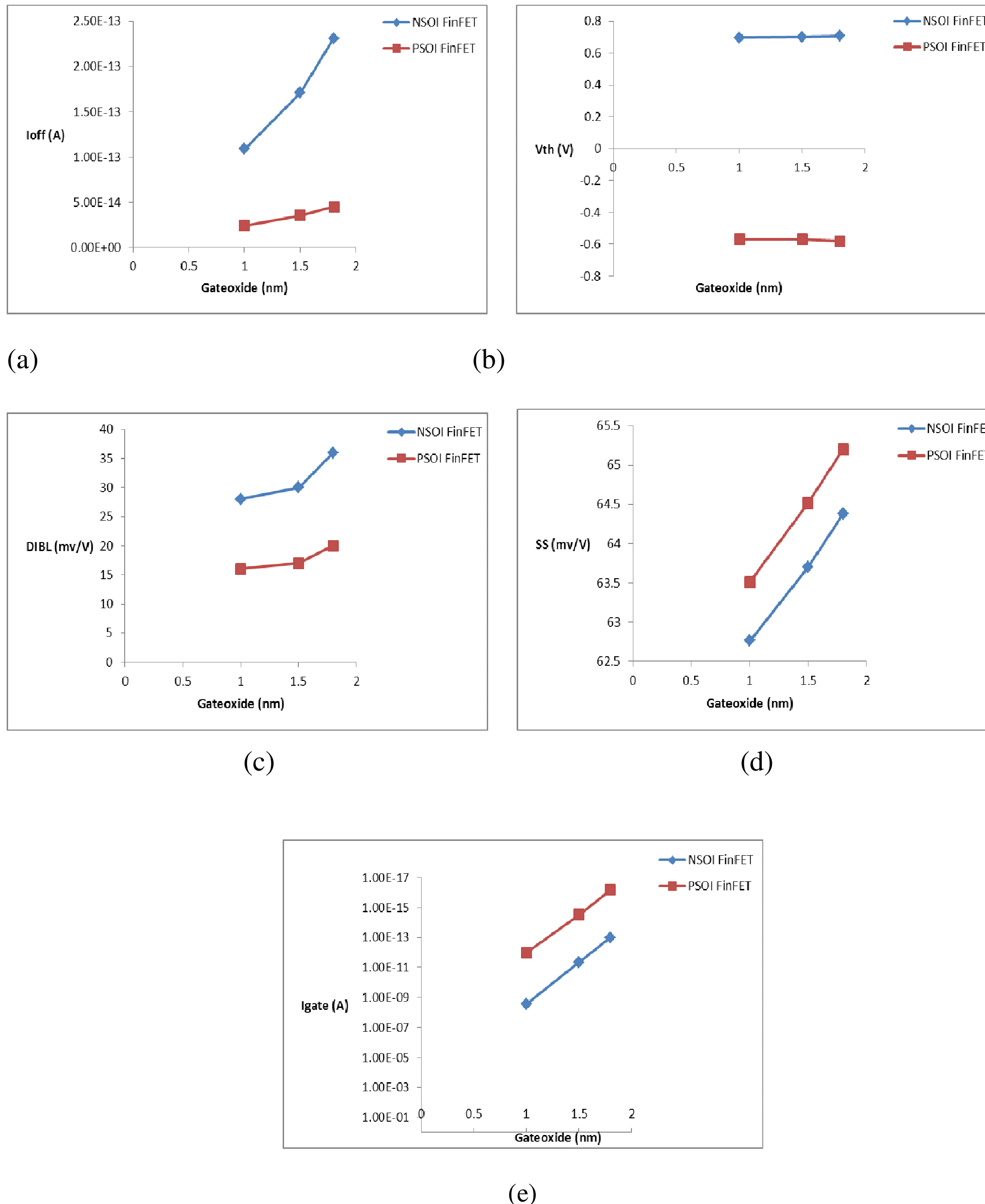


Figure 5: Impact of Fin height on (a) I_{OFF} behavior, (b) Threshold Voltage, (c) DIBL, (d) Subthreshold Slope and (e) Gate leakage current.

oxide thickness.On current and transconductance increases with decrease in gate oxide. On current increases from 742µA to 928µA (25%) for reduction of gate oxide thickness from 1.8 to 1nm.The most important factor being the direct gate tunneling current, increases from 0.1pA to 2.68 nA i.e by 3 orders of magnitude ($2.6*10^3$) when the gate oxide is reduced from 1.8nm to 1nm for a NSOI FinFET. The off current reduces with decrease in oxide thickness.Though the other SCEs reduce, the leakage factor is the dominant factor which limits the continuous scaling of the gate oxide thickness ,which leads to high static power dissipation.



(a) (b)

(c) (d)

(e)

Figure 6: Impact of Gate oxide thickness on (a) I_{OFF} behavior, (b) Threshold Voltage, (c) DIBL, (d) Sub threshold Slope and (e) Gate leakage current.

We have studied the impact of the device parameter variations on the performance of CMOS inverter (Static power dissipation and Delay). We evaluated the delay (T_d) and the static power dissipation (P_{static}) for an inverter with nominal values and also for other parameter variations. Delay is better figure of merit, since it takes into account the capacitance associated with the structure as well as the current drivability. [22, 23] The delay associated with inverter, T_d is given by the equation $T_d = C_{gg} * V_{DD} / I_{ON}$, where C_{gg} is the total gate capacitance which can be obtained by the CV sweep of the devices and V_{DD} is the supply voltage (1 volt). We have calculated the rise time delay (T_{rd}) with respect to on current of the P-device and fall time delay (T_{fd}) with respect to the on current of the N-device in each case of variation.

Power dissipation of any logic gate can be expressed as: $P_{total} = P_{dyn} + P_{static}$, where P_{dyn} represents dynamic power dissipation due to charging, discharging of capacitances when the output signal of a logic gate makes a transition. P_{static} is the static power consumption due to the leakage current whose major components are the subthreshold leakage (I_{OFF}), gate direct tunneling leakage (I_{GATE}), and junction band-to-band tunneling leakage (I_{btbt}) [24]. Hence Static power dissipation of the inverter is given by: $P_{static} = V_{DD} * I_{static} = V_{DD} * (I_{GATE} + I_{OFF} + I_{btbt})$. In double gate and triple gate SOI devices such as FinFETs, static power consumption is dominated by the subthreshold leakage and gate tunneling leakage. [25] In our FinFET devices, the body is left undoped, and the band-to-band tunneling leakage (I_{btbt}) becomes negligible. Static power consumption is a strong function of temperature, while dynamic power consumption is weakly coupled with temperature variation, hence we do not consider these components (P_{dyn} and I_{btbt}) of leakage in this paper.

Figure 7 shows the Voltage Transfer characteristics (VTC) and Transient response of a Basic Inverter with nominal device dimensions. The noise margins for the inverter were calculated from the graphical method. The high level noise margin (N_{MH}) and low level noise margin (N_{ML}) was found to be 0.509Volts and 0.492 volts respectively. AC analysis was performed for a PSOI FinFET to obtain the total gate capacitance. The gate capacitance of the NSOI FinFET device is half of its counter part and hence total gate capacitance of the inverter is calculated. The gate capacitances for the other variations are calculated analytically, which is given by the equation, $C_{gg} = \varepsilon_{ox}/t_{ox}$*Gate Area, where ε_{ox} is the permittivity of the gate oxide and t_{ox} is thickness of the gate oxide. As gate area or oxide thickness varies, capacitance also varies.

Table 2: Static power dissipation and Delay in an Inverter varying with Fin width for

V_{DD} = 1volt

Finwidth (nm)	Static power						Delay		
	Input = 0			Input =1					
	I_{GATE} (PMOS)	I_{OFF} (NMOS)	P_{Static} (pW)	I_{GATE} (NMOS)	I_{OFF} (PMOS)	P_{Static} (pW)	C_{gg} (fF)	T_{fd} (pS)	T_{rd} (pS)
Nominal=5	0.0030pA	0.17pA	0.174	4.42pA	0.035pA	4.46	0.035	0.042	0.55
8	0.0040pA	0.68pA	0.690	4.33pA	0.118pA	4.44	0.037	0.039	0.50
12	0.0046pA	3.42pA	3.420	3.42pA	0.484pA	3.90	0.040	0.037	0.48

Table 2 summarizes the static power dissipation and delay of inverters for nominal fin width and for inverters whose fin widths are varied. We observe that though the total gate capacitance (C_{gg}) increases with increase in fin width, the rise time and fall time delays reduce which is due to higher on currents for thicker fins. The rise time and fall time delays reduce by 13.5% and 14.5% respectively, as the Fin width is increased from 5 to 12nm. There is marginal variation in static power dissipation (Input=1) as the fin widths are varied by a smaller factor.

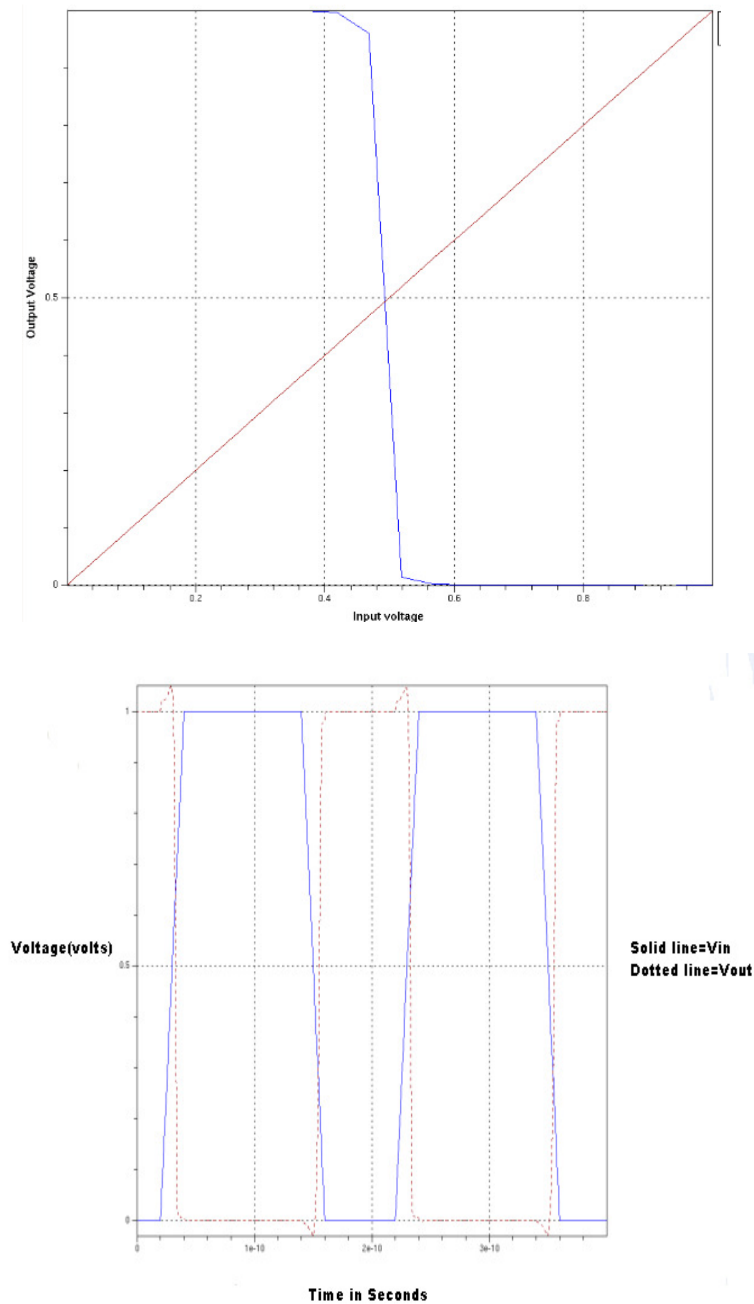


Figure 7: Voltage transfer characteristics of a static CMOS Inverter (top) and Transient response of the Inverter (bottom)

Similarly Table 3 summarizes the static power dissipation and delay of inverters for different fin heights. The static power dissipation increases by 2.5 times (77%) and delays increase by 3.6 times when the Fin height is increased from 10nm to 40nm. Increase in power dissipation is due to increasing leakage currents (Gate leakage and I_{OFF}) with Fin height, whereas increase in delay is due to increasing gate capacitance with gate area.

Table 3: Static power dissipation and Delay in an Inverter varying with Fin height for V_{DD} = 1volt

Finheight(nm)	Static power						Delay		
	Input = 0			Input =1					
	I_{GATE} (PMOS)	I_{OFF} (NMOS)	P_{static} (pW)	I_{GATE} (NMOS)	I_{OFF} (PMOS)	P_{Static} (pW)	C_{gg} (fF)	T_{fd} (pS)	T_{rd} (pS)
10	0.0025pA	0.12pA	0.078	5.93pA	0.028pA	3.25	0.0097	0.017	0.23
20	0.0030pA	0.17pA	0.174	4.42pA	0.035pA	4.46	0.035	0.042	0.55
40	0.0021pA	0.27pA	0.270	4.35pA	0.067pA	8.05	0.051	0.061	0.83

The static power dissipation and delay of inverters for different gate oxide thickness are tabulated in Table 4. The Static power dissipation increases exponentially from 0.15pW to 2.68nW ($18*10^3$ times) for approximately 1nm reduction in gate oxide thickness. This is primarily due to large gate leakage current in ultra thin oxides. We also observe that gate delay increases by 46% with reduction in gate oxide thickness from 1.8nm to 1nm. This is due to the large gate capacitances associated with thinner oxides. Hence the overall performance of the inverter is not improved with the scaling of the gate oxide thickness.

Table 4: Static power dissipation and Delay in an Inverter varying with gate oxide thickness for V_{DD} = 1volt

Gateoxide (nm)	Static power						Delay		
	Input = 0			Input =1					
	I_{GATE} (PMOS)	I_{OFF} (NMOS)	P_{Static} (pW)	I_{GATE} (NMOS)	I_{OFF} (PMOS)	P_{Static}	C_{gg} (fF)	T_{fd} (pS)	T_{rd} (pS)
1	1.027pA	0.10pA	1.130	2.68nA	0.024pA	2.68nW	0.050	0.053	0.70
1.5	0.003pA	0.17pA	0.174	4.42pA	0.035pA	4.46pW	0.035	0.042	0.55
1.8	0.00006pA	0.23pA	0.230	0.10pA	0.045pA	0.15pW	0.028	0.037	0.48

3. CONCLUSIONS

A full process flow for a 22nm triple gate SOI FinFET has been implemented in this work. Various device parameters such as Finwidth, Fin height and Gate oxide thickness have been varied and the impact of these device parameters on the static power dissipation and delay of a CMOS inverter are presented. For a given fin thickness and increasing fin height, the threshold voltage, off-current, delay and SCEs remain approximately insensitive, while the on-current and transconductance increases approximately linearly with the increase in fin height. On the other hand DIBL, SS and off-current (I_{OFF}) are quite sensitive to the variations in fin width at fixed fin height. We found out that gate leakage increased exponentially with decrease in gate oxide thickness. The rise time and fall time delays of the CMOS inverter reduced by 13.5% and 14.5% respectively, as the Fin width is increased from 5nm to 12nm, showing improved performance in terms of delay. When the fin height is increased from 10nm to 40nm, the static power dissipation increased by 2.5 times (77%) and delays increased by 3.6 times. We observed increase in the Static power dissipation from 0.15pW to 2.68nW ($18*10^3$ times for Vin =1) for approximately 1nm reduction in gate oxide thickness and increase in gate delay by 43.2% and 45.8%(Fall time delay and Rise time delay) with reduction in gate oxide thickness from 1.8nm to 1nm.Hence performance of the inverter degrades by increasing the Fin Height and with reduction in gate oxide thickness. Better Figure of merit in terms of delay is obtained with increase in Fin width.
Keeping device scalability in mind, simulated device parameters like Static power dissipation, delay and capacitances based on realistic process flow provide a useful guide to the circuit

designer for low power, analog, RF and digital applications. Further scope of work may include improving the performance of inverter for other device design considerations.

ACKNOWLEDGEMENTS

This research is supported by the BMS College of Engineering, Bangalore.The authors wish to thank BMS college of Engineering for supporting this work by encouraging and supplying the necessary tools.

REFERENCES

[1] T. Sekigawa and Y. Hayashi, "Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate", Solid-State Electronics 27, 827 (1984).

[2] D. Hisamoto, T. Kaga, Y. Kawamoto, E. Takeda, "A fully depleted lean channel transistor (DELTA)-a novel vertical ultra-thin SOI MOSFET ", Technical Digest of IEDM, 833 (1989).

[3] J.P. Colinge, M.H. Gao, A. Romano, H. Maes, C. Claeys, "Silicon-on insulator 'gate-all-around' MOS device," Technical Digest of IEDM, 595, 1990.

[4] J.T. Park, J.P.Colinge and C.H. Diaz, "Pi-Gate SOI MOSFET", IEEE Electron Device Letters, vol. 22, pp. 405-406, Aug. 2001.

[5] Xuejue Huang, Wen-Chin Lee, C. Kuo, D. Hisamoto, Leland Chang, J.Kedzierski, E. Anderson, H.Takeuchi, Yang-Kyu Choi, K. Asano, V.Subramanian, Tsu-Jae King, J. Bokor, Chenming Hu,"Sub 50-nm FinFET: PMOS", Technical Digest of IEDM, 67 (1999).

[6] D.Hisamoto, W.C. Lee, J.Keidzerski, H.Takeuchi, K.Asano, C.Kuo. T.J.King, J.Bokor and C.Hu, "FinFET-a self-aligned double-gate MOSFET scalable beyond 20 nm", IEEE Trans.Electron Devices, vol.47, pp. 2320-2325, Dec. 2000.

[7] Bin Yu, Leland Chang, S. Ahmed, Haihong Wang, S. Bell, Chih-Yuh Yang, C. Tabery, Chau Ho, Qi Xiang, Tsu-Jae King, J. Bokor, Chenming Hu, Ming-Ren Lin, D. Kyser, "FinFET scaling to 10 nm gate-length," Technical Digest of IEDM, 251 (2002).

[8] Yang-Kyu Choi, "FinFET for Terabit era", Journal of Semiconductor Technology and Science 4-1, 1 (2004). 22, pp. 405-406, Aug. 2001.

[9] J.P. Colinge, "Multi-gate SOI MOSFETs", Microelectronic Engineering, vol.84, issues 9-10, pp.2071-2076, Sept-Oct, 2007.

[10] R.V. Joshi, R.Q. Williams, E. Nowak, K. Kim, J.Beintner, T. Ludwig, I. Aller, and C. Chuang,"FinFET SRAM for high-performance low-power applications", Proceeding of the 34th European Solid-State Device Research conference, pp. 69 – 72, 2004

[11] B. A. Rainey, D. M. Fried, M. Ieong, J. Kedzierski, E. J. Nowak, "Demonstration of FinFET CMOS circuits", Device Research Conference, pp. 47-48,2002."

[12] Z. Guo, S. Balasubramanian, R. Zlatanovici, T. -J.King, B. Nikolic, " FinFET-Based SRAM Design", International Symposium on Low Power Electronicsand Design, pp. 2-7, 2005.

[13] H. Ananthan, A. Bansal, and K. Roy, " FinFET SRAM - device and circuit design considerations" Proceedings of the Sixth International Symposium on Quality Electronic Design (ISQED 2004), pp. 511-516, 2004.

[14] Tsu-Jae King, "FinFETs for Nanoscale CMOS Digital Integrated Circuits" Advanced Technology Group, Synopsys, Inc., Mountain View, California, USA.

[15] G. Pei, J. Kedzierski, P. Oldiges, M. Ieong, E.C.C. Kan, "FinFET design considerations based on 3-D simulation and analytical modeling", IEEE Trans. Electron Devices 49 (8) (2002) 1411–1419.

[16] Muhammad Nawaz, Wolfgang Molzer, Stefan Decker, Luis-Felipe Giles, Thomas Schulz, "On the device design assessment of multigate FETs (MuGFETs) using full process and device simulation with 3D TCAD", Microelectronics Journal 38 (2007) 1238–1251.

[17] Muhammad Nawaz, Wolfgang Molzer, Stefan Decker, Luis-Felipe Giles, Thomas Schulz" "Evaluation of process parameter space of bulk FinFETs using 3D TCAD"- Microelectronic Engineering 85 (2008) 1529–1539.

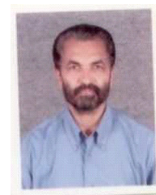
[18] M.Nawaz, Re: K. Von Armin, E. Augendre, C. Pacha, T. Schulz, K.T. San, F. Bauer, A. Nackaerts, R. Rooyackers, T. Vandeweyer, B. Degroote, N. Collaert, A. Dixit, R.Singanamalla, W. Xiong, A. Marshall, C.R. Cleavelin, K. Schrüfer, J. Jurczak,VLSI 2007, pp. 106–107.

[19] Aditya Bansal, Kaushik Roy, “Asymmetric Halo CMOSFET to Reduce Static Power Dissipation With Improved Performance”, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 52, NO. 3 MARCH 2005.
[20] Aditya Bansal, Jung Hwan Choi, Mesut Meterelliyoz, Jayathi Murthy, and Kaushik Roy, “Self-Consistent Approach to Leakage Power and Temperature Estimation to Predict Thermal Runaway in FinFET Circuits”- IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 26, NO. 11, NOVEMBER 2007
[21] Sentaurus-Process, Sentaurus-Device Simulator, Version V-2008.09, Synopsys
[22] J.W. Yang, J.G. Fossum, "On the feasibility of nanoscale triple-gate CMOS transistors", IEEE Trans. Electron Devices 52 (6) (2005) 1159–1164.
[23] J.G. Fossum, J.W. Yang, V.P. Trivedi, "Suppression of corner effects in triple gate MOSFETs", IEEE Electron Device Lett. 24 (12) (2003) 745–747.
[24] K. Roy et al., “Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits,” Proc. IEEE, vol. 91, no. 2, pp. 305–327, Feb. 2003.
[25] S. Mukhopadhyay et al., “Modeling and analysis of leakage currents in double-gate technologies”, IEEE Trans. Comput. -Aided Design Integr.Circuits Syst., vol. 25, no. 10, pp. 2052–2061, Oct. 2006.

Authors

Prathima. A received her B.E degree from BMS College of Engineering of Visvesvaraya Technological University, Belgaum 2004.Her areas of interest are VLSI design and VLSI circuits. She is presently a post graduate student(M.Tech-Electronics) from B.M.S. college of Engineering of Visvesvaraya Technological University.

Kiran Bailey received her B.E degree from Dayananda College of Engineering of Bangalore University, Bangalore in the year 1997. She got her M.Tech degree from B.M.S. college of Engineering of Visvesvaraya Technological University, Bangalore in 2001. She joined BMSCE in 1998 and has since been teaching Electronics related subjects. Her areas of interest are solid state devices, VLSI design, Low power VLSI circuits. Presently she is an Assistant professor in the dept. of E&C, BMSCE, Bangalore



Dr. K.S. Gurumurthy (M’2000) obtained his B.E degree from M.C.E – Hassan of Mysore University in the year 1973. He got his M.E Degree from University of Roorkee (now IIT-Roorkee) in 1982. He joined UVCE in 1982 and he has since been teaching Electronics related subjects. He obtained his PhD degree in 1990 from IISc Bangalore. He is a “University gold medal” winner from University of Roorkee and a recipient of the “Khosla award” for the best technical paper published in 1 982. His interests are Low power VLSI, Multi valued logic circuits, Deep submicron Devices. Presently he is a professor in the DOS in E & CE Dept., UVCE, Bangalore University, Bangalore