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Contactless Test Access Mechanism for 3D IC

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Contactless Test Access Mechanism for 3D IC

By

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DECLARATION OF CO-AUTHORSHIP / PREVIOUS PUBLICATION

I. Co-Authorship Declaration

I hereby declare that this dissertation incorporates material that is the result of research conducted under the supervision of my supervisors, Dr. Rashid Rashidzadeh and Dr. Esam Abdel-Raheem. Results related to this research are reported in Chapters 2 through 4.

I am aware of the University of Windsor's Senate Policy on Authorship and I certify that I have properly acknowledged the contributions of the other researchers to my dissertation, and I have obtained written permission from my co-author to include the aforementioned materials in my dissertation.

I certify that this dissertation, and the research results to which it refers, is the product of my own work.

II. Declaration of Previous Publication

This dissertation includes three original papers that have been previously published for publication in peer reviewed transactions and conferences, as follows:

Chapter Number	**Title of the Publication**	**Publication Status**
Chapter 2	Iftekhar Ibne Basith, Rashid Rashidzadeh, "Contactless Test Access Mechanism via Capacitive Coupling for TSV Based 3D ICs", in the proceedings of IEEE Transactions on Instrumentation and Measurement (TIM), August 26, 2015.	Published
Chapter 3	Iftekhar Ibne Basith, Rashid Rashidzadeh, and Esam Abdel-Raheem, "Contactless Detection of Faulty TSV in 3D IC via Capacitive Coupling" in proceedings of the IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS) 2015, Colorado State University, Fort Collins, Colorado, Aug 2-5, 2015.	Published
Chapter 4	R. Rashizadeh, I.I. Basith, "A Test Probe for TSV using	Published

	Resonant Inductive Coupling" in IEEE International Test Conference (ITC), Publication Year: 2013.	
	Iftekhar Ibne Basith and Rashid Rashidzadeh, "A Contactless Test Probe for TSV Based 3D ICs using resonant inductive coupling".	Submitted to IEEE TCAS I

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ABSTRACT

3D IC integration presents many advantages over the current 2D IC integration. It has the potential to reduce the power consumption and the physical size while supporting higher bandwidth and processing speed. Through Silicon Via's (TSVs) are vertical interconnects between different layers of 3D ICs with a typical 5μm diameter and 50μm length. To test a 3D IC, an access mechanism is needed to apply test vectors to TSVs and observe their responses. However, TSVs are too small for access by current wafer probes and direct TSV probing may affect their physical integrity. In addition, the probe needles for direct TSV probing must be cleaned or replaced frequently. Contactless probing method resolves most of the TSV probing problems and can be employed for small-pitch TSVs.

In this dissertation, contactless test access mechanisms for 3D IC have been explored using capacitive and inductive coupling techniques. Circuit models for capacitive and inductive communication links are extracted using 3D full-wave simulations and then circuit level simulations are carried out using Advanced Design System (ADS) design environment to verify the results. The effects of cross-talk and misalignment on the communication link have been investigated.

A contactless TSV probing method using capacitive coupling is proposed and simulated. A prototype was fabricated using TSMC 65nm CMOS technology to verify the proposed method. The measurement results on the fabricated prototype show that this TSV probing scheme presents -55dB insertion loss at 1GHz frequency and maintains higher than 35dB signal-to-noise ratio within 5μm distance.

A microscale contactless probe based on the principle of resonant inductive coupling has also been designed and simulated. Experimental measurements on a prototype fabricated in TSMC 65nm CMOS technology indicate that the data signal on the TSV can be reconstructed when the distance between the TSV and the probe remains less than 15μm.

DEDICATION

To my wonderful family – my parents, my wife and my beautiful daughters.

Indeed my success and achievements are nothing but an outcome of their unconditional love, endless support and tremendous patience.

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Next, I would like to take this chance to thank my colleagues and friends. I would like to thank Tareq Muhammad Supon and Nabeeh Kandalaft for always being there with all kinds of help when I got stuck with something. I want to thank Andria Ballo, our graduate secretary for her prayers and support throughout my stay at this department.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.I MOTIVATION OF THIS WORK

The performance of digital systems is affected by the delay of transistors and interconnects. Technology scaling reduces the size of transistors and results in faster circuits; the voltage required and the power consumed is also reduced, thus allowing for more components on a single integrated circuit. According to Moore's law [1], the transistor count per unit area in an integrated circuit should double every two years. Even though device size is getting smaller, chip size needs to increase to accommodate the ever growing demand for functionality and higher performance [2] which causes a different issue since global interconnects do not scale down aggressively enough [3]. Repeaters can be used to address this issue in exchange for more power and area. The relative delay for metal and global wiring is plotted in Figure 1.1 [4].

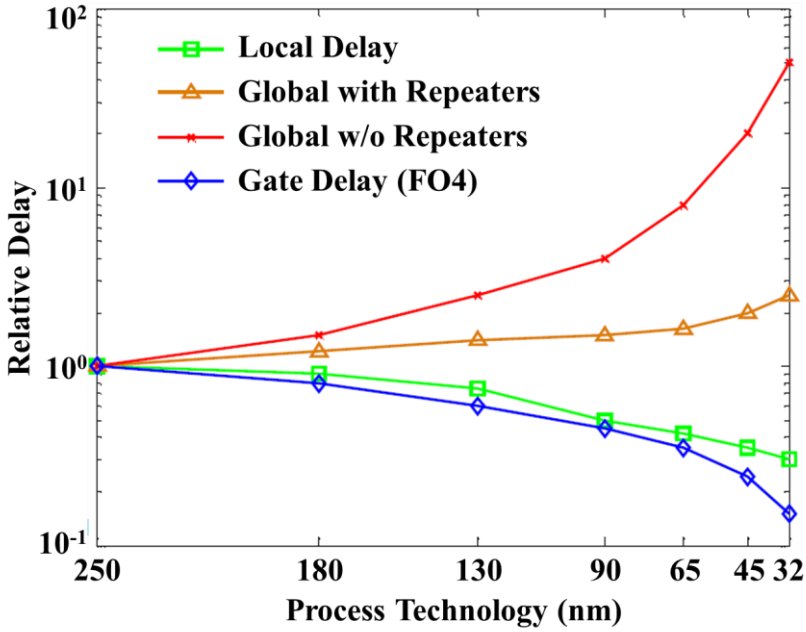

Figure 1.1: Delay for Metal 1 and Global Wiring versus feature size according to the ITRS Roadmap [4].

The overall power in modern integrated circuits is dominated by the interconnect delay which is a bottleneck [5, 6, 7] limiting the processing speed.

Three-dimensional (3D) integration is an innovative new technology that offers functional benefits and substantial interconnect performance enhancements as compared to traditional two-dimensional (2D) ICs. 3D comes with advantages like improved inter-connectivity, greater device density, lesser and shorter global wires, and the potential for heterogeneous integration [3, 8, 9]. 3D ICs combine the advantages of technology scaling with improved packaging.

1.II 3D TECHNOLOGY AND CHALLENGES

Different implementations of 3D technology are available based on the method used to realize vertical connections between the layers in the stack, such as wire-bonding [3], using contactless links [10, 11] etc. A 3D IC can be implemented using microbumps. In this process, dies are mechanically thinned down and the exposed surfaces are connected using solder bumps. However, the connections can only be made at the top layer or surface. Hence microbumps can be utilized for face-to-face bonding and thus restricting the maximum layer to two in 3D stacking. Microbumps can be quite large (50μm to 500μm) limiting the interconnect density.

A common and popular approach for 3D IC realization is the use of Through Silicon Vias (TSVs). TSVs are vertical connections created during the 3D IC assembly to connect the top and bottom sides of a die in a 3D stack. To create a TSV, a tiny hole is etched through the substrate which is covered with an insulation layer and filled with a metal. TSVs allow face-to-face or face-to-back integration and provide direct communication between active devices from different layers. Thus, TSVs allow for a high density of vertical interconnects between multiple layers and can be placed anywhere on the IC. In addition, TSV enables high speed and low power consumption for 3D integration through a smaller parasitic capacitance, inductance, and resistance.

There are many challenges for 3D IC integration as well. The design process is complex and expensive using available technologies. One of the main challenges is the increasing power density and the associated thermal issues. In a 3D IC, the tier that is stacked

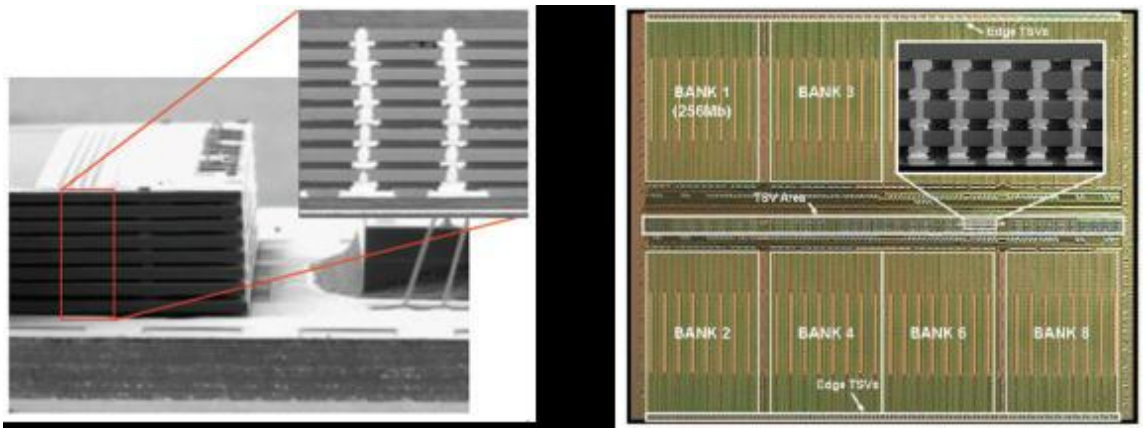

Figure 1.2: Multiple stacked die with nail shape TSVs shown in left; a DRAM die with TSVs in right [Samsung]

farthest from the heat sink will require greater time to dissipate the heat due to a high thermal resistivity, thus limiting the stack size of a 3D IC [12]. The temperature increases by 17K for a 2 die stack and 33K for a 4 die stack as shown in [13].

Another concerning factor is the yield. The access to non-bottom die is limited and functionality of the chip can only be tested once the stacking is formed which can negatively impact the yield. Despite being an excellent electrical conductor, a single faulty TSV can cause a number of known good dies to be discarded.

Testing for stacked 3D ICs is a major challenge. Techniques that are used for 2D ICs cannot be readily applied to 3D ICs. Both pre-bond and post-bond testing methods must be taken into consideration and new design-for-testability (DfT) techniques should be developed.

1.III ADVANTAGES OF 3D ICs

Through Silicon Via (TSV) is a copper nail that directly passes through the substrate to connect different dies in the 3D IC, thus reducing the average interconnect length significantly. Hence 3D stacking of ICs and vertical interconnect TSVs provides substantial benefits, however there are still a lot of challenges. The following summarizes the benefits of 3-D ICs.

1.III.A Heterogeneous Integration

Contemporary IC's demand a number of heterogeneous functions like data processing, sensing, memory, data transmission, etc. Thus, they require several fabrication processes to be integrated in one. 3D ICs offer the potential to merge these processes into a vertically stacked system. Dies with specific circuitry type such as RF, analog, MEMS/ NEMS, or different process technologies like 65nm, 45nm, and 32nm, as well as optics or graphene technologies can be fabricated separately and then stacked into 3D integration.

1.III.B Shorter Inter-connect

TSVs are usually 10-100μm in height [14]. 3D ICs reduce global wiring length by a factor of the square root of the number of layers used [15]. This reduction offers latency improvement and power saving.

1.III.C Smaller Form Factor and Cost Reduction

By decomposing a complex and large IC into smaller multiple partitions, 3D ICs help creates smaller footprints and surfaces suitable for mobile devices and military technologies. The heterogeneous integration alongside with smaller form factor helps reduce the cost required to manufacture 3D ICs.

1.III.D Higher Bandwidth

TSV's reduce the parasitic capacitance of interconnects compared to interconnects in 2D integrations; hence 3D IC integration offers higher bandwidth. An Intel Pentium-4 processor was folded onto 2-layer implementation and a performance improvement of approximately 15% was reported [16].

1.III.E Power Improvement

Effective power management techniques and strategies are essential to counter the on-chip temperatures that pose a risk to circuit reliability. Interconnect power consumption is the core portion of the total power consumed. In 3D designs, the interconnect lengths are reduced, which can be translated as power saving. In [17], approximately 7% to 46% of power reduction is reported for 3D arithmetic units.

1.IV CONTACTLESS TESTING

Different testing methods can be combined in various ways to test a chip and ensure its functionality. Recent advances in IC technology have paved the way for increased IC complexity and device density which increase the test costs [4]. Automatic Testing Equipment (ATE) is widely used to test integrated circuits. An ATE is commonly equipped with probe cards and multiple probe tips alongside the interface circuits between I/O pads on the Device Under Test (DUT) and the ATE, as shown in Figure 1.3. Probe tips are designed with adequate elasticity, so they do not deform the DUT while making direct contact [18, 19].

There are several limitations in using conventional probe cards. The size and pitch of the probe needles must get smaller as the number of I/O pads increases which may cause complications in the wafer-level testing [20]. In addition, probe deformation may be caused even with minor contacts. The accumulated debris on the probe tips also increases the resistance between the probe and the DUT which may affect the test results, thus requiring regular probe cleaning. Conventional probe cards do not support the flexible location of contact points and are not suitable for parallel testing of multiple dies [21]. Finally, the size and the pitch constraint of through-silicon vias and micro-bumps for 3D ICs make it more difficult to test with conventional probe cards [22]. TSVs are too small to be contacted by the current probes. A direct probe contact can affect the physical integrity of the TSV under test.

Contactless probing alleviates many problems associated with the direct contact method. However, it requires additional circuitry on the DUT without affecting the overall functionality of the chip. A contactless link can be implemented through radiative, inductive, or capacitive coupling.

1.IV.A Radiative Coupling

Radio Frequency (RF) plays a significant role in today's wireless communication [24-29]. Radiative coupling offers the highest communication range in comparison to other wireless methods. However, implementation of RF coupling needs large size antennas in

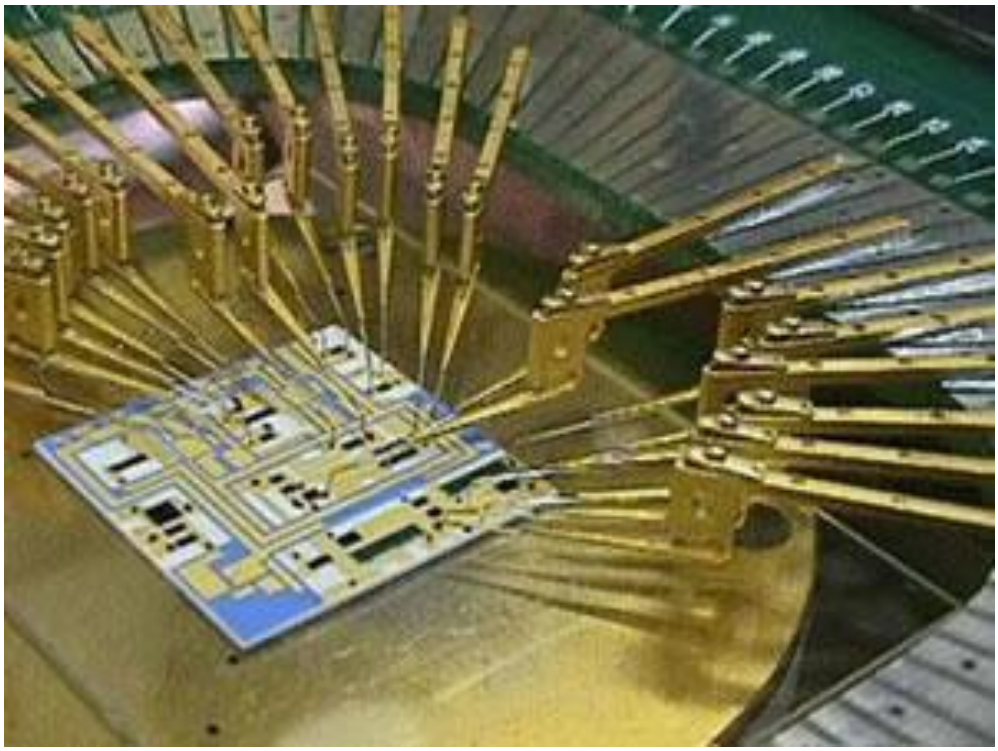

Figure 1.3: IC Probe Card with multiple probe tips [58]

both the transmitter and receiver sides. In this work, we are not pursuing radiative coupling due to the considerable area and power overhead for 3D ICs.

1.IV.B Inductive Coupling

Inductive coupling [11], [30-40] offers the midway between RF and capacitive coupling in terms of performance even though the design and characterization of on-chip inductors may get complicated. The communication range is modest, larger than capacitive but smaller than RF coupling. Inductive coupling is not affected significantly by the technology shrinking or limited supply voltage since it is current driven and can be used with external current generating circuits. Since high permeability materials are not used, the eddy current effect on the magnetic field is insignificant. In addition, by increasing the number of turns in the inductor, the coupling coefficient can be increased greatly to support the communication range needed for 3D IC testing.

1.IV.C Capacitive Coupling

Capacitive coupling is the simplest of all in terms of implementation and provides a cost effective option for contactless testing. The TSV pad and the probe tip form a small capacitor that can be used as a contactless communication channel [41-51]. The capacitor coupling allows for the high data rate needed for 3D IC testing. Even though the area overhead is small, the communication range is generally low which may limit the application.

1.V CONTRIBUTIONS OF THIS WORK

The main focus of this work was to devise a contactless test access mechanism (TAM) for TSV based 3D ICs. For this we explored all three coupling options and concluded that the radiative coupling is not feasible due to area constraint. However, both capacitive and inductive coupling provided viable options for contactless probing. We characterized a TSV using High Frequency Structure Simulator (HFSS) environment, and extracted lumped models for both inductive and capacitive coupling. The extracted spice models were used in Advanced Design System (ADS) environment for circuit level simulation. Simulations were performed to characterize the wireless communication links and the bond wires. The effect of different data rates on the reconstructed data was analyzed. Cross-talk, probe size, and misalignment between the probe and TSVs were characterized through simulations. A prototype was fabricated and tested to verify the performance of wireless links. Experimental measurements on the fabricated prototype indicate that the proposed contactless solutions can be used for TSV probing. The results of this research project have been published in one IEEE transaction article and two conference papers. A journal article covering the proposed inductive link has been submitted to the IEEE Transactions on Instrumentation and Measurement (TIM) for review.

1.VI DOCUMENT OUTLINE

The rest of this dissertation is organized as below:

- Chapter 2 presents a paper on contactless testing for TSV using capacitive coupling. This work has been published in IEEE Transactions on Instrumentation and Measurement.

- Chapter 3 is another paper on TSV fault detection using capacitive coupling which has been published in the IEEE International Midwest Symposium on Circuits and Systems 2015 held in Colorado, USA.

- Chapter 4 presents on the proposed contactless probe using resonant inductive coupling which is published in the IEEE International Test Conference 2013.

- Chapter 5 provides the summary of this work and recommendations for future work.

- Appendix A shows the list of accepted IEEE transactions and conference papers during my tenure as a PhD student, but not related to the dissertation topic.

- Appendix B shows the list of submitted IEEE transactions and conference papers both related and not related to the dissertation topic.

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CHAPTER 2

CONTACTLESS TEST ACCESS MECHANISM FOR TSV BASED 3D ICS UTILIZING CAPACITIVE COUPLING

2.I INTRODUCTION

Very Large Scale Integration (VLSI) circuits are scaled down to increase device functionality and performance. Three-dimensional (3-D) IC design has shown the potential to support the requirements for new generation of integrated circuits by heterogeneous integration of multi-disciplinary technologies. Among possible solutions for interconnects between 3D stacked IC, Through Silicon Via (TSV) technology has emerged as a viable and efficient solution due to its short interconnect length, high density, and small footprint. However, TSV technology presents new challenges and testing TSV interconnects require development of new Design-For-Test (DFT) techniques and test access mechanisms [1-3].

Various test methods have been proposed in the literature to address the challenges of testing pre-bond and post-bond TSVs. Pre-bond TSV tests detect faulty dies prior to stacking and post-bond tests cover defects due to misalignment and imperfect bonding [4, 5]. A die-level wrapper based on IEEE 1500 has been proposed in [6] to support TSV testing. Dedicated probe pads on non-bottom dies and intra die interconnects called "test-elevators" between stacked dies are introduced in this method. A sense amplifier is used in [7] to detect pre-bond TSV defects due to resistive shorts. This method requires an accurate tuning and calibration of on-chip circuitry for fault detection. Highly sensitive amplifiers have also been used in [8] for blind TSVs to detect pre-bond capacitive defects. TSV pinholes and voids are detected through a resistance measurement method using a leakage-current sensor and a capacitive bridge in [9]. A DFT based method for pre-bond testing is presented in [10] where a group of TSVs are touched simultaneously by a probe needle to form a network of TSVs. This scheme requires a direct access to TSVs through contact probes. A socket based solution using micro-scale contactor is presented in [11] to test TSVs and micro-bump arrays. The contactor can be fabricated with small pitch and relies on good electrical connection between the contact points. An

all-digital pre-bond test solution using ring oscillator is presented in [12] to detect resistive open and leakage faults based on the variation of oscillation frequency. TSVs are used as capacitive loads to affect the propagation delay of a ring oscillator in [13] to perform pre-bond testing. To detect post-bond TSV defects, a scan chain based genetic algorithm is proposed in [14].

Current wafer probe technologies based on cantilever or vertical probes require large contact pads to ensure the connectivity and cannot readily meet the pitch requirements for TSV probing. Direct TSV probing using available wafer probes can potentially lead to irreversible defects. The height variation of microbumps due to fabrication process can impede direct connection with the probe tips [15]. Moreover, conventional wafer probes have the limitation of regular maintenance and cleaning, which increases the test time and the costs of manufacturing. MEMS technology has also been utilized for TSV probing [16]. Although, the new generation of MEMS based test probes supports the pitch requirement, but they do not entirely rule out the possibility of scrub marks and physical integrity degradation due to probing. Contactless probing resolves many of the constraints of direct TSV probing. They do not require routine cleaning or maintenance as they are not subjected to physical force. They also present better mechanical performance and durability than the conventional probes.

The feasibility of contactless communication via inductive [17-19], radiative [20] and capacitive coupling [21, 22] techniques have been investigated in the literature. Inductive based interconnections are current driven and work based on the principle of magnetic induction. As a result they consume more power as compared to capacitive coupling.

To increase the coupling efficiency, a resonant inductive coupling [19] has been introduced. This method as compared to the conventional coupling supports a longer communication range. In [23], the authors have proposed three possible wireless communication methods in form of RF, near-field and optical - inductive and capacitive coupling illustrating the near-field technologies. The electrical characterization of TSV made of tungsten and hybrid Cu-adhesive wafer bonding is reported in [24] in which different techniques are utilized to determine TSV parameters.

TABLE 2.I

COMPARISON BETWEEN CAPACITIVE AND INDUCTIVE COUPLING

Criteria	Inductive	Capacitive
Driver	Current	Voltage
Communication Distance	Long	Short
Area	Large	Small
Power Consumption	High	Low

Table 2.I summarizes the comparison between the inductive and the capacitive coupling techniques. Radiative coupling is widely used for UHF RFID applications; however, the need for an on-chip antenna in this method limits its application for testing TSVs. At 1GHz, an efficient antenna has to be about 8.25cm long. Such an antenna cannot be implemented in practice due to its significant area overhead.

In this work capacitive coupling is utilized in a novel way to meet both the tight-pitch and the high-density requirements of 3D IC testing. A small probe is placed at a few micrometer distances above a TSV to form a capacitance in the range of a few femto-farads. Such a small capacitance is enough to observe TSV data activities using a sensing circuit with small size transistors and low parasitic capacitances. Measurement results using a fabricated prototype show that the implemented contactless probe can be used to observe TSV data. The rest of the paper is organized as follows. In section 2.II current capacitive coupling solutions are described. Section 2.III presents the implemented probe and interface circuit alongside the circuit level simulation results. The measurement results are discussed in section 2.IV and finally conclusions are summarized in section 2.V.

2.II CURRENT CAPACITIVE SOLUTIONS

Capacitive and magnetic coupling techniques have been used for contactless sensing in many applications. In [25-26] seat occupancy is detected using capacitive and combined inductive-capacitive coupling sensors. Similar method is reported in [27] for human proximity and safety applications. In [28] capacitive coupling is utilized for robot grasping objects. Cylindrical capacitive sensing is also used to measure displacements of active magnetic bearing spindles in [29]. In [30] authors have proposed a wireless

communication scheme for 3D IC assembly using capacitive coupling. In this approach instead of TSV, capacitively coupled interconnects are utilized for communication between stacked dies. A clock signal is used to synchronize receivers and transmitters and the clock propagation delay is compensated by a separate clock tree. The circuits are implemented using 0.13µm CMOS technology. A data rate of 1.23Gbps and total power consumption of 0.14mW/Gb/s are reported. In [31], receiver and transmitter are stacked face-to-face to communicate through capacitive coupling. This method reduces the power consumption and improves the bit rate. However, the proposed methods in [30] and [31] suffer from relatively large area overhead. In [32], a sensitive capacitive-coupling interface is presented for wireless wafer testing. This method requires dedicated receivers and transmitters with complex circuits to optimize the threshold logic level. An improved data rate of 2Gbps with an increased communication distance of about ≈4µm is reported. Capacitive coupling methods using ultra-wide band interconnect (UII) and radio frequency Interconnect (RFI) are reported in [33] to improve power and bandwidth in 3D IC. A capacitive-coupling transceiver is presented for wireless wafer-level testing in [34] with low power and high speed.

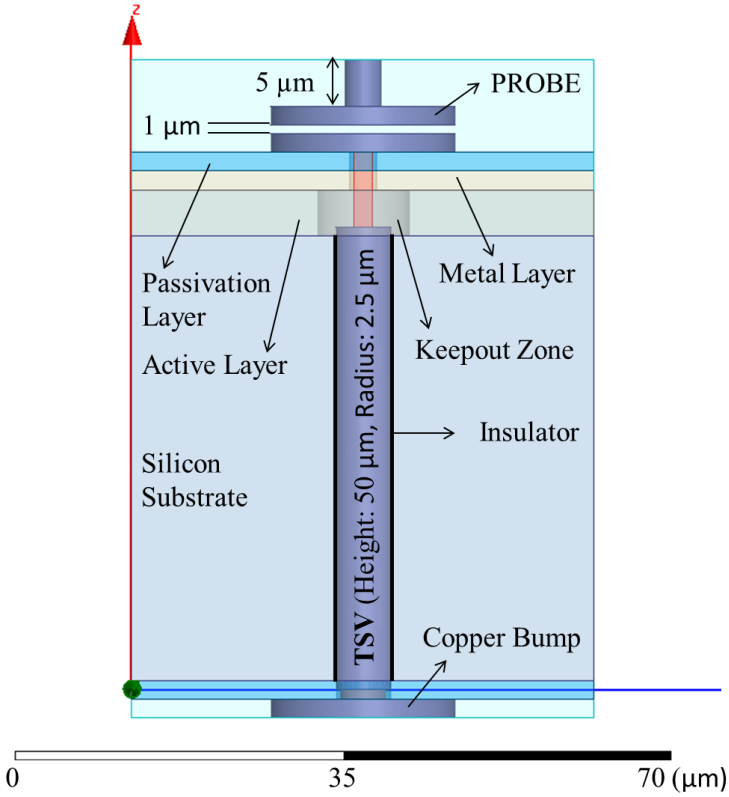
2.III SIMULATION RESULTS

Fine-pitch and high-density are the main requirements for TSV probing. To meet these requirements, the size of a contactless probe should not exceed the size of a TSV bump. As a result, the electric flux passing from the TSV to the contactless probe will be severely limited. A high resolution sensing circuit is needed to reconstruct the TSV data from the induced signal in the probe.

A. Implemented Structure

A contactless probe and a TSV were designed using High Frequency Structure Simulator (HFSS) to verify the proposed contactless probing method. HFSS is a 3D full-wave electromagnetic field simulation CAD tool that can be used to determine the electromagnetic fields within a structure and allows the extraction of a passive Spice model from S-parameters. Fig. 2.1(a) shows the implemented TSV and probe structure. The TSV is realized by a circular 50µm long copper with 2.5µm radius covered by a

(a)



(b)

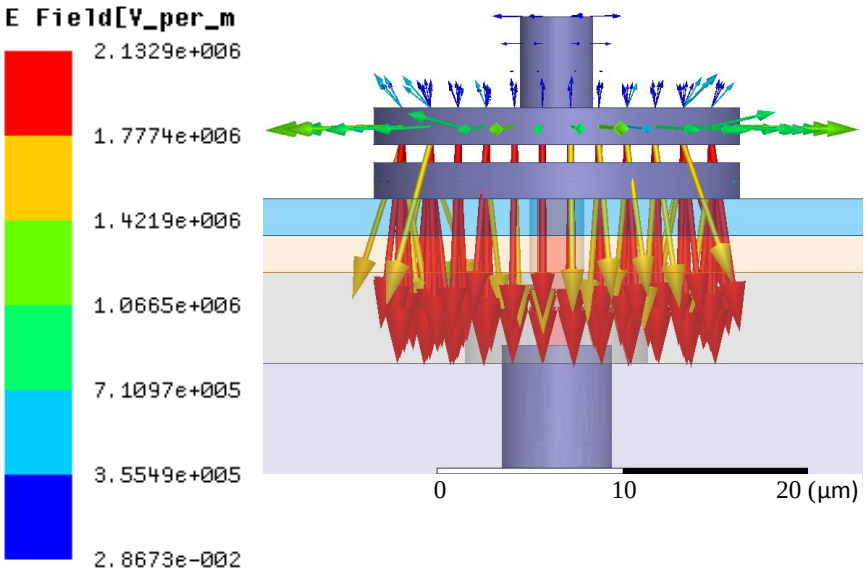
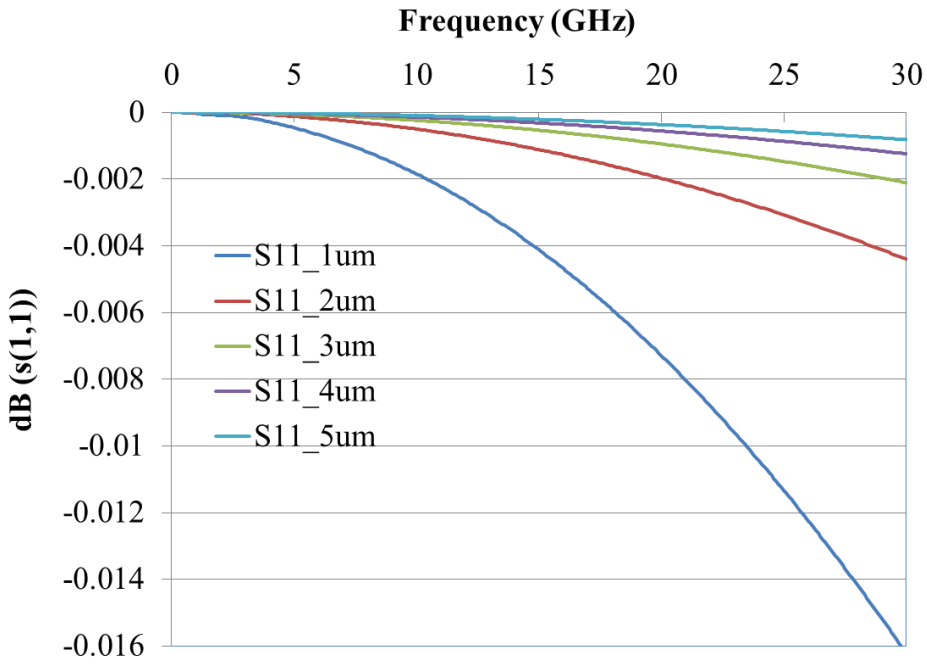


Fig. 2.1: Implemented contactless probe and TSV in HFSS environment (a) before excitation and (b) After excitation.

100nm dielectric layer within a substrate. The implemented structure is designed to represent an actual TSV by taking the effect of TSV surrounding environment into consideration. For instance the keep out zone which minimizes the effect of TSV stress on active circuits is considered. The passivation layer which protects the TSV structure against environmental effects has also been implemented. The probe tip is designed to have 10µm radius to match the size of TSV bump. The initial gap between TSV and probe is set to be 1µm to form a coupling capacitor between the probe and the TSV. Voltage excitations have been applied to the TSV and the probe to perform simulations in HFSS environment. Fig. 2.1(b) shows the distribution of electric field which indicates a strong field across the gap between the TSV and the probe. Simulation results show that up to 5µm gap, the electric field between the TSV and the probe is strong enough to be detected with the designed sensing circuit. Fig. 2.2 shows S-parameters for communication distance between the TSV and the probe varying from 1µm to 5µm. The S11 graph in Fig. 2.2(a) indicates that the applied input signal is mainly reflected at low frequencies. As the frequency increases the return loss falls indicating that the signal passes through the coupling capacitance, C_c, between the TSV and the probe. The variations of S21 parameter in Fig. 2.2(b) show that the insertion loss decreases with frequency. This is an expected result since the impedance of the coupling capacitance, X_C, calculated from $X_C = 1/C_c\omega$ decrease with frequency. As a result the signal picked up by the probe becomes stronger as the frequency rises. It can also be seen from Fig. 2.2(b) that the insertion loss increases as the gap between the TSV and the probe rises from 1µm to 5µm. As the gap increases, the coupling capacitance decreases which in turn increases the impedance of the coupling capacitance, X_C. The value of X_C affects the insertion loss directly and as X_C increases the insertion loss rises. The effective coupling capacitance between the TSV and the probe follows the principle of parallel plate capacitor. The calculated coupling capacitance for 1µm gap and 10µm radius is $C = \varepsilon A/d = 2.8fF$ where the extracted coupling capacitance from HFSS simulations is 3.18fF as shown in the low bandwidth lumped model in Fig. 2.3. The difference between them is due to the fringing effect which is not taken into consideration in the equation for parallel plate capacitance.

(a)



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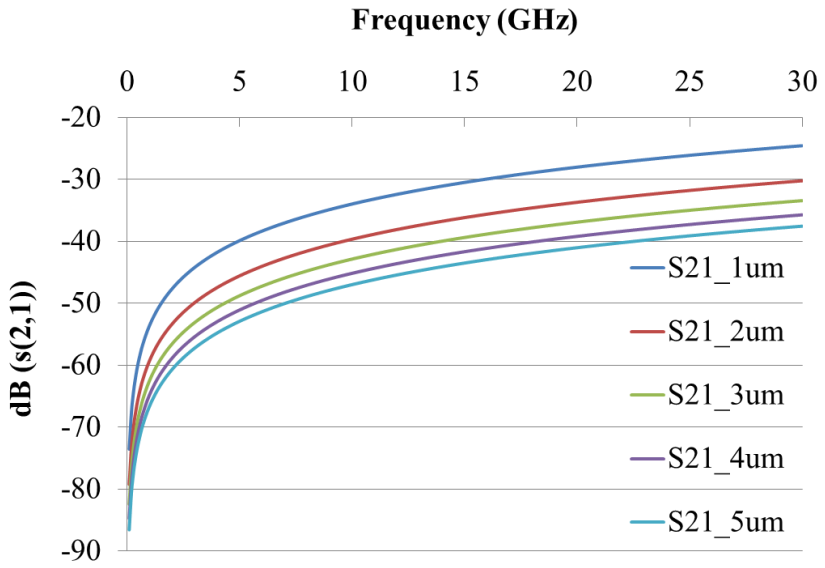


Fig. 2.2: S-parameters for communication distance between the TSV and the probe varying from 1µm to 5µm. (a) S11 and (b) S21.

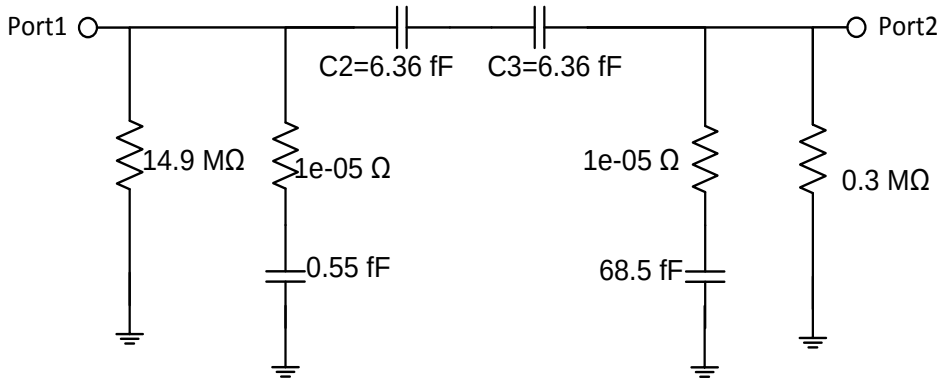


Fig. 2.3: Extracted low-bandwidth lumped model for the implemented TSV and probe from HFSS at 1GHz.

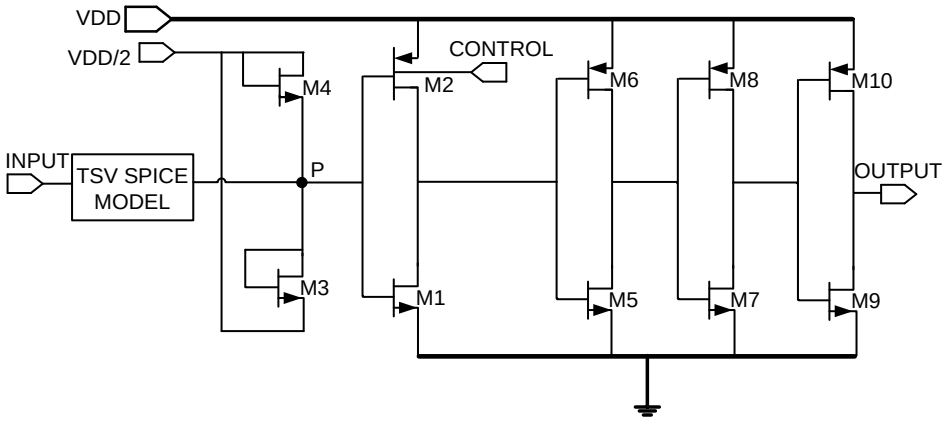


Figure 2.4: Sensing circuit used to reconstruct the TSV data.

To detect the coupled signal and reconstruct the TSV data, a sensing circuit is designed using ADS simulation tools with TSMC 65nm CMOS technology. Fig. 2.4 shows the schematic diagram of the designed sensing circuit which includes a switching amplifier (M1-M2) and three inverters (M5-M10). Additional transistors (M3-M4) are used to ensure that the input of the switching amplifier at node P does not accumulate charge and settles down properly. M1 and M2 are minimum size transistors to reduce the parasitic capacitances and support a high-speed data rate between the TSV and the probe. The switching amplifier stage is designed to minimize the effects of Process, supply Voltage and Temperature (PVT) variations on the output signal. The body voltage of M2 in the sensing circuit in Fig 2.4 is externally controlled to cancel out the effect of PVT in the calibration phase.

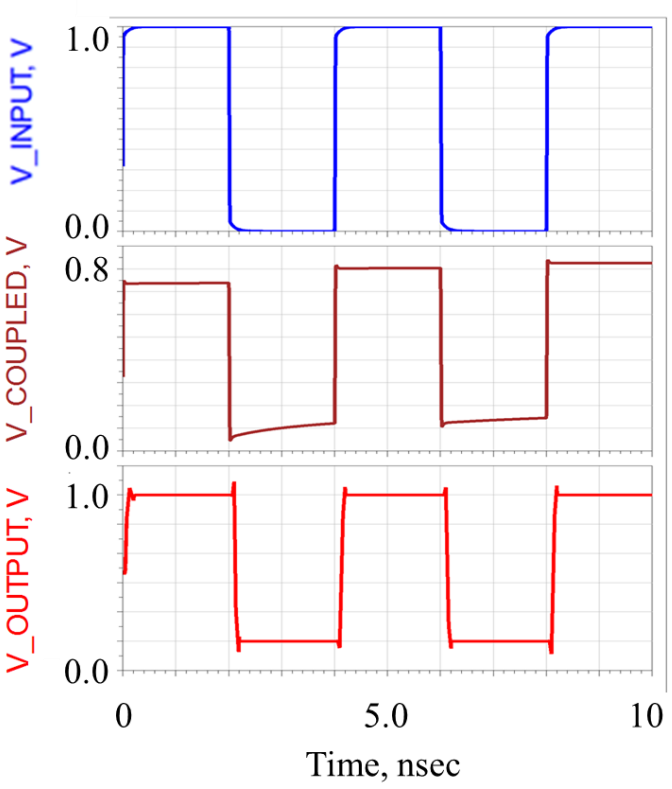
B. Circuit-level Simulation Results

The circuit in Fig. 2.4 is implemented in Agilent ADS environment and simulated to determine its performance. Fig 2.5(a) shows the TSV signal, the coupled signal at node P and the reconstructed TSV output data at 1Gbps rate. The input to the extracted TSV model is a time domain pseudorandom bit sequence. There is a delay of ≈55ps between the input and output data at 1 GHz, as shown in Fig. 2.5(b). It has to be noted that the TSV low-bandwidth model in Fig. 3 is valid for frequencies close to 1GHz. This is due to the effect of substrate on the overall behavior of TSV. The substrate conductivity and the frequency of operation affect the low-bandwidth circuit model considerably. Figure 2.6 shows the eye diagrams of the output TSV signals at 1Gbps and 5Gbps data rates. The speed of 5Gbps is to ensure the bit-error-rate (BER) of 10-12. When the speed increases the signal-to-noise ratio falls, as a result the BER increases. Table 2.II summarizes the details of the eye- diagram parameters at different data rates. It is clear from the table that Signal to Noise Ratio (SNR) decreases as the data rate rises with good eye opening and strong SNR of more than 100dB at 1Gbps. The eye closes at 10Gbps and beyond with SNR of about 12dB.

C. Misalignment and Crosstalk effects

Simulations were performed to determine the effects of misalignment varying from 1µm to 5µm. The effect of probe misalignment in the Z direction which affects the gap between probe and TSV is significant. Simulation results show that the coupling capacitance reduces linearly with the inverse of distance between the plates. The results in Table 2.III summarize the changes in electric field and coupling capacitance due to variations in Y and Z direction. As shown in Table 2.III when the gap between coupling interfaces in Z-direction increase, the capacitance reduces proportionally. As shown in Fig. 2.9, when the gap between the TSV and the probe increases in Z-direction, the capacitance reduces which is an expected result. When the gap size increases by a factor of two, the capacitance decreases by the same factor. The electric field also decreases accordingly from 2.13V/µm to 0.76V/µm. The misalignment of the probe on the Y-direction does not change the coupling capacitance considerably. This is due to the fact that the reduction of coupling capacitance caused by Y-direction misalignment is partly

(a)



(b)

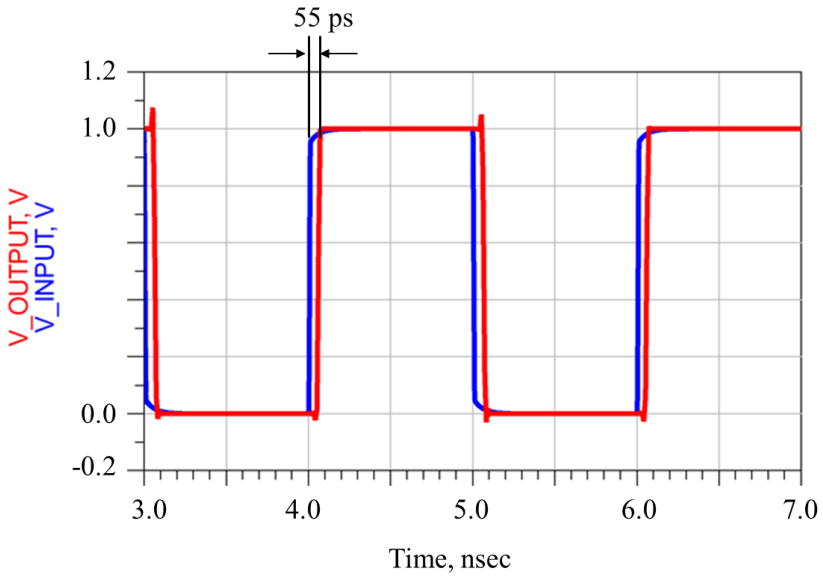
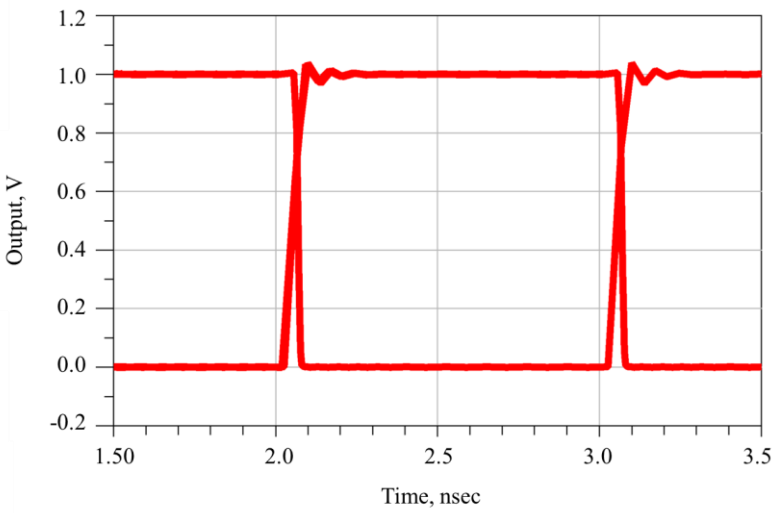


Fig. 2.5: (a) Input signal to TSV, coupled signal at node P and reconstructed TSV data at 1Gbps and (b) Delay between the input and the reconstructed TSV data.

(a)



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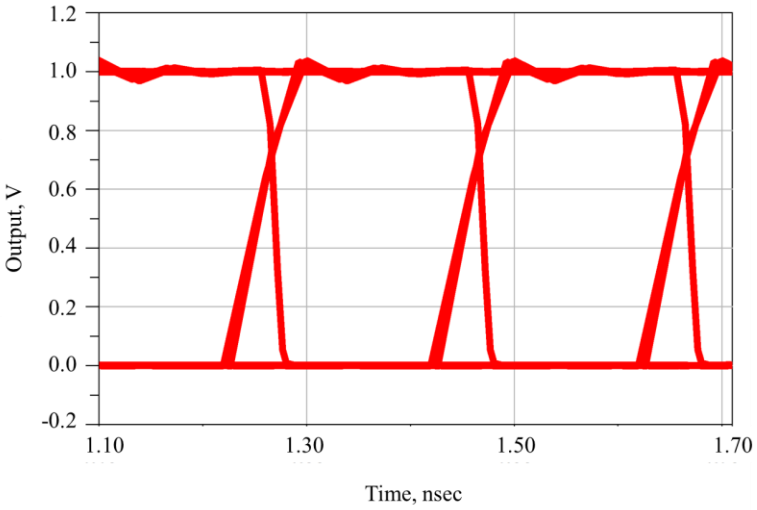


Fig. 2.6: Simulated eye-diagram at data rate of (a) 1Gbps and (b) 5Gbps.

TABLE 2.II

EYE DIAGRAM INFORMATION

Criteria	1 Gbps	5 Gbps	10 Gbps	20 Gbps
RMS Jitter (pp)	≈ 6.6ps	≈ 13.63ps	≈22.35ps	FALSE
Eye Width	≈ 980.6ps	≈194.5ps	≈81.6ps	FALSE
SNR	> 100dB	> 35dB	< 12dB	FALSE

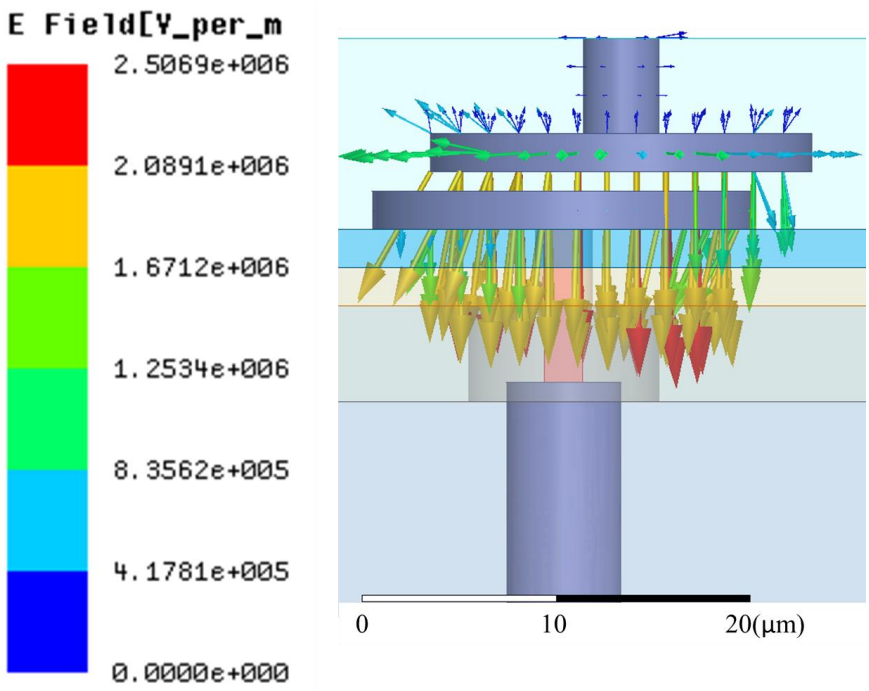


Fig. 2.7: E-field changes for 3µm misalignment between probe and TSV.

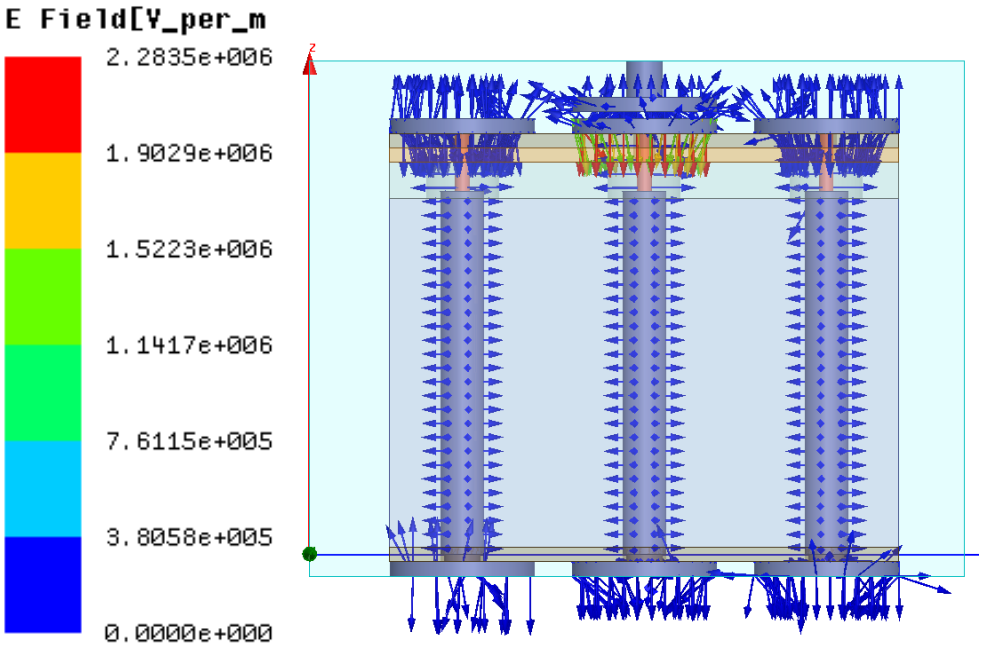


Fig. 2.8: Effect on the electric field from adjacent TSV with 25 µm apart.

TABLE 2.III

EFFECT ON E-FIELD AND COUPLING CAPACITANCE FOR DISPLACEMENT ALONG Y AND Z DIRECTION

Displacement (in µm)	Z-Direction (GAP)		Y-Direction (Misalignment)	
	E-Field Max (V/m)	C (fF)	E-Field Max (V/m)	C (fF)
1	2.13 e+006	3.18	2.31 e+006	3.14
2	1.11 e+006	1.64	2.70 e+006	3.02
3	0.92 e+006	1.12	2.51 e+006	2.88
4	0.84 e+006	0.85	2.44 e+006	2.72
5	0.76 e+006	0.67	2.56 e+006	2.56

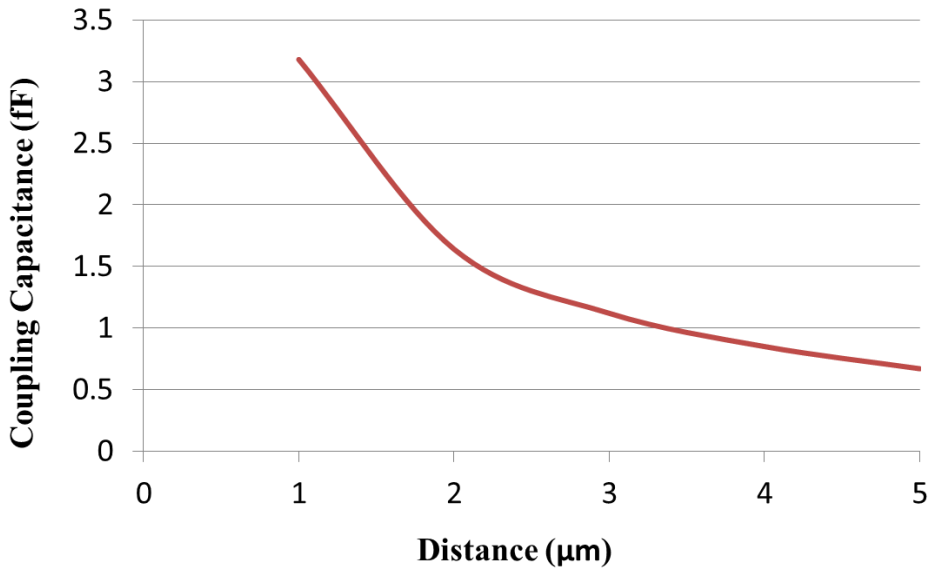


Fig. 2.9: Effect of the gap between TSV and probe on coupling capacitance.

compensated by the coupling between the probe and the surface of TSV sidewall. The coupling capacitance reduces to 2.56fF for 5µm misalignment from 3.14fF for 1µm. However, the maximum electric field varies randomly due to the misalignment ranging between 2.3V/µm to 2.7V/µm. Figure 2.7 shows the electric field distribution when there is 3µm misalignment between the TSV and the probe. Crosstalk from adjacent TSV affects the signal integrity of TSV signal. Figure 2.8 shows that the electric field increases due to the crosstalk between adjacent TSVs which are placed 25µm apart.

TABLE 2.IV

EFFECT ON COUPLING CAPACITANCE FOR PROBE SIZE

Probe radius (in μm)	Calculated C (fF)	Simulated C (fF)
3	0.25	0.7
5	0.7	1.75
7	1.4	2
9	2.3	2.85
10	2.8	3.18
11	2.8	3.4
13	2.8	3.5

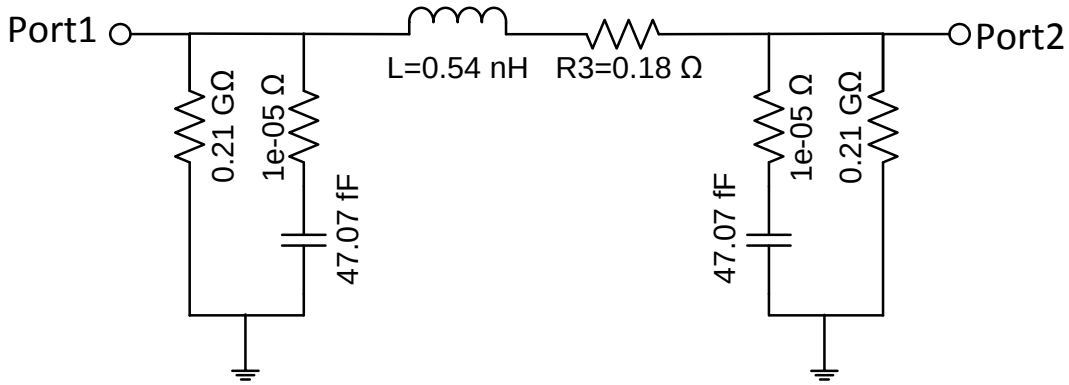
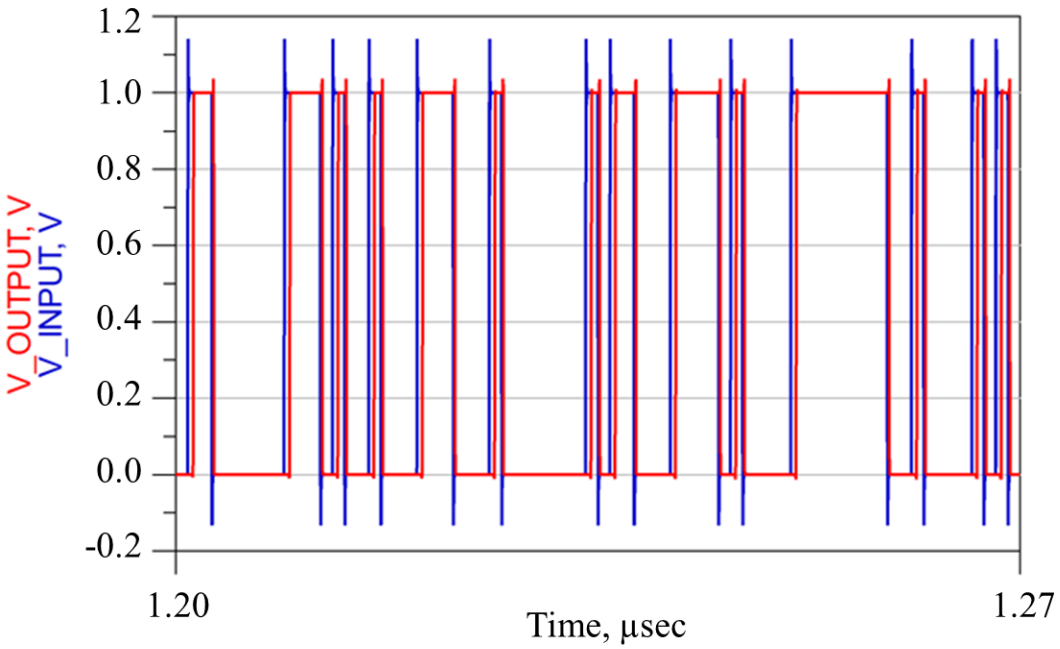


Fig. 10: Extracted lumped model for bond-wires.

Simulations were performed to analyze the effects of probe size on coupling capacitance. Table 2.IV summarizes the calculated and simulated coupling capacitance due to varying probe size. The decrease in capacitance for lower radius can be attributed to the lower shared area between the plates. The difference between simulated and calculated capacitance is also understandable due to the fringing capacitances. The difference between the calculated and simulated capacitances become minimum when the TSV and probe have the same radius since the fringing capacitance is not taken into consideration in the equation for parallel plate capacitance. The effect of bonding wires has also been investigated. A bond wire with 5μm diameter and 1mm length was designed in HFSS and its circuit model was extracted as shown in Fig. 2.10. The bonding wire is primarily characterized by series inductance, resistance and shunt capacitances.

(a)



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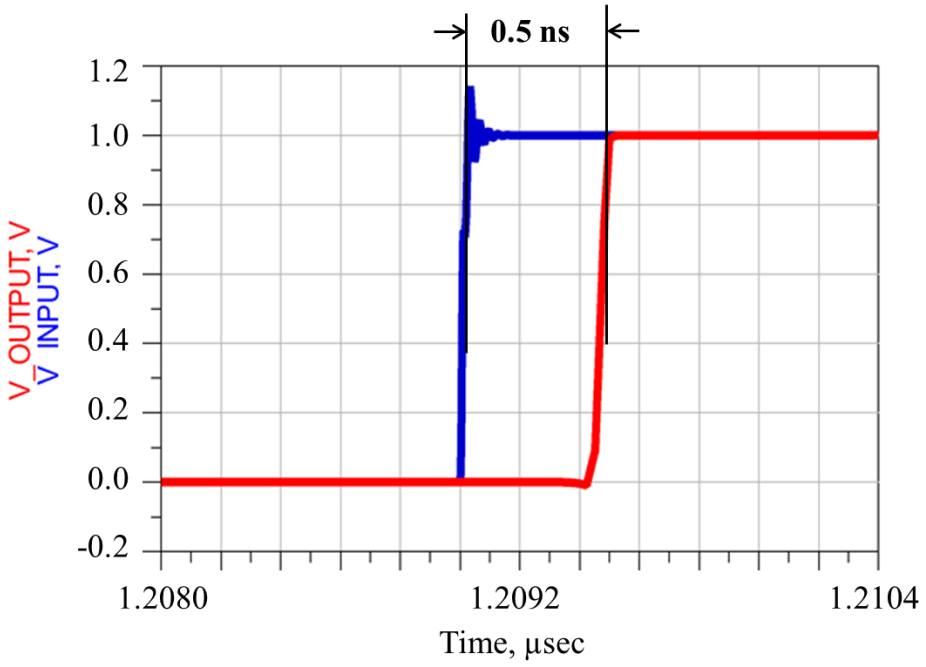


Fig. 2.11: Simulated TSV input and output with bond wires.

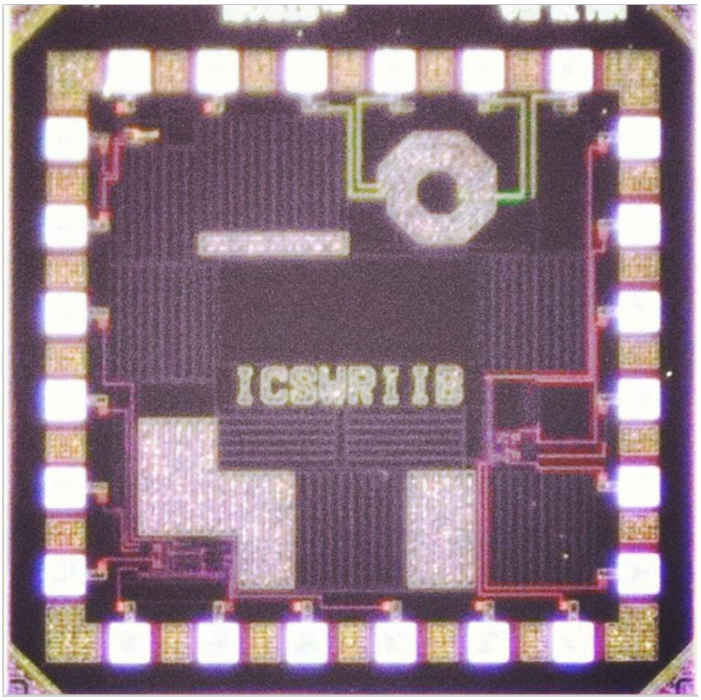


Fig. 2.12: Fabricated die photo.

This model is later used in ADS to perform simulations with TSV connected to the sensing circuit. Fig. 2.11 shows the simulated input and output signals and the delay between them. The delay has increased significantly to ≈500ps as compared to the case without the bonding wire at 1GHz with 55ps delay. The bonding wire also affects the overall SNR which falls from more than 100dB to lower than 60dB.

2.IV MEASUREMENT RESULTS

A prototype was implemented using TSMC 65nm CMOS technology, as shown in Fig 2.12, to verify the performance of the proposed contactless probing method. The equivalent circuit in Fig. 2.3 was used to implement the probe and the TSV. Fig. 2.13 shows the measurement setup which includes a probe station with microscope. Tektronix's MDO 4104 B-6 oscilloscope was used for time domain measurements. As shown in Fig. 2.14, the TSV data is reconstructed by the sensing circuit. The delay between the input and the output signals is ≈0.15ns which is higher than what is obtained from simulation in Fig. 2.5(b). This can be attributed to the parasitic capacitances added

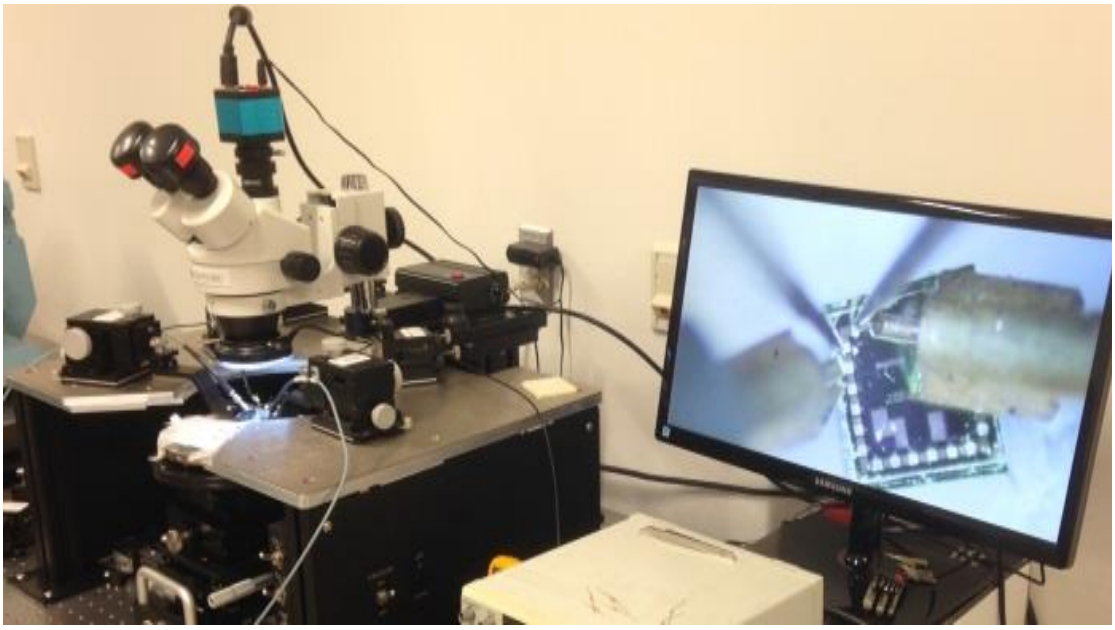


Fig. 2.13: Measurement setup to test the fabricated prototype.

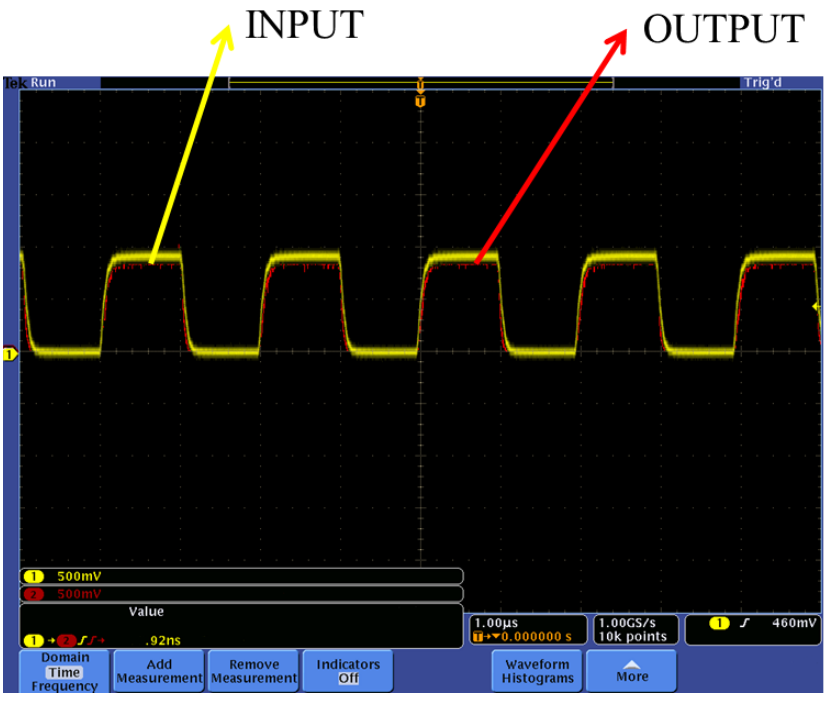


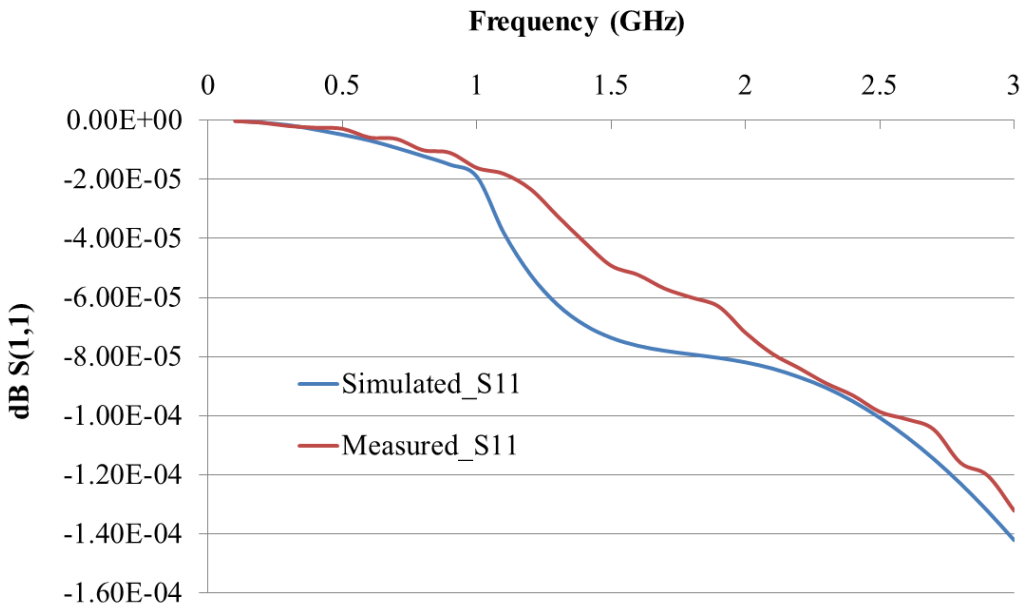
Fig. 2.14: Measured input and output of the fabricated chip using Tektronix oscilloscope.

by measurement instruments to the input and output pads. The measurement setup and the cables used to connect the device-under-test to the measurement instrument have parasitic capacitances. These capacitances at high frequencies can lead to signal leakage which can cause measurement error [33]. To minimize the measurement error, the instruments were calibrated using standard calibration kit. Fig. 2.15 shows the measured and simulated S11 and S22 using E5061B network analyzer from Agilent. Fig. 2.15 indicates the simulation results together with the experimental measurements up to 3GHz. Due to the bandwidth limitation of the measurement instruments, the comparison is performed up to 3GHz. A close examination of the graphs shows a good agreement between the simulation and the measurement results. Table 2.V shows the comparison of parameters between previous works and our current work. As compared to the reported works in the literature, the proposed method requires less area overhead and supports longer communication range. This is mainly due to the sensing circuit which is optimized to capture the coupled signals and reconstruct the TSV data. The data rate in this work is lower than what is reported in [34] and [35]. However, this is not a major drawback since the data rate depends on the size of the capacitor used to establish the contactless link. If the capacitor size is doubled the data rate increases by twofold. If we increase the channel size to $300\pi\ \mu m^2$, it can support 15Gbps data rate with a lower area overhead compared to [35].

2.V CONCLUSION

TSV based 3D circuit integration has emerged as a viable solution for next generation of high performance circuits. A test access mechanism is required to conduct manufacturing test on 3D ICs. Probing TSVs with conventional wafer probes can undermine their physical integrity. A contactless TSV probe based on the principle of the capacitive coupling is presented in this work. The proposed solution supports the high-density and low-pitch requirements for testing TSV based 3D ICs. Simulation results using HFSS and ADS CAD tools show that the proposed solution can be used to observe TSV data activity up to 5µm communication range with 5Gbps data rate and 35dB signal-to-noise ratio. The probe supports 10-12 BER at 5Gbps data rate if the distance between the probe and TSV remains less than 5µm. When the distance exceeds 5µm, the signal-to-noise

(a)



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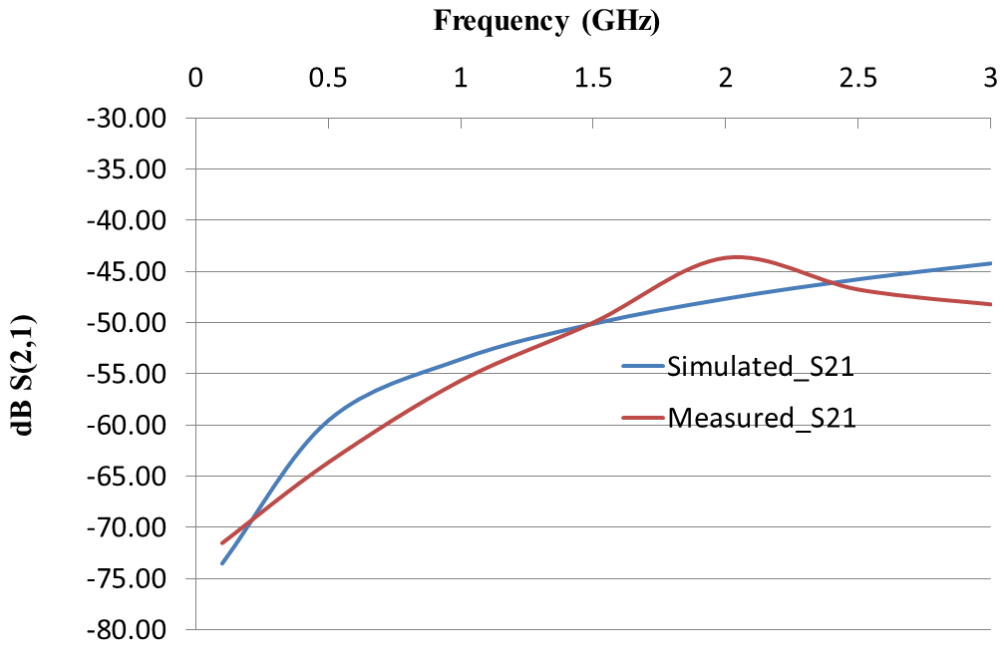

Fig. 2.15: Simulated and measured (a) S11 and (b) S22.

TABLE 2.V

PERFORMANCE PARAMETERS OF COMMUNICATION LINKS UTILIZING CAPACITOR COUPLING TECHNIQUE

	Daito et al [21]	A. Fazzi et al [31]	Gu et al [34]	Kim et al [35]	Our work
Application	IC testing	Data Communication	Chip-to-chip	IC testing	All
Energy/bit	2pJb	0.08pJb	0.27pJb	0.47pJb	0.31pJb
Data Rate/Channel	1Gbps	1.23 Gbps	10Gbps	15Gbps	5Gbps
BER	$<10^{-12}$	$<10^{-13}$	$<10^{-12}$	$<10^{-12}$	$<10^{-12}$
Process	90nm CMOS	0.13µm CMOS	0.18µm CMOS	65nm CMOS	65nm TSMC
Range R	4µm	N/A	3µm	4µm	5µm
Size of the channel	$80X80\mu m^2$	$8X8\mu m^2$	$2X48X18\mu m^2$	$80X80\mu m^2$	$100\prod \mu m^2$

ratio (SNR) falls and the BER increase. A prototype using TSMC 65nm technology was implemented to evaluate the performance. The measurement results show a good agreement with the simulation results and the applied input data was successfully reconstructed by the sensing circuit.

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CHAPTER 3

CONTACTLESS DETECTION OF FAULTY TSV IN 3D IC VIA CAPACITIVE COUPLING

3.I INTRODUCTION

With ongoing and aggressive downscaling of CMOS technology, Moore's law is facing a steep challenge. FinFET transistors are introduced as a potential solution for further scaling but this technology has its own implementation complexities [1]. With the advantage of possible heterogeneous integration and vertical stacking using Through Silicon Via (TSV), the 3D IC promises to be the viable solution for future semiconductor industry [2]. TSV's are conducting copper nails, which pass directly through the substrate to provide high-speed interconnects between the top and bottom of the substrate. TSV technology supports high performance, small footprint and lower power consumption [3]. Testing TSV interconnects for manufacturing defects poses major challenges and new Design-For-Test (DFT) techniques [4, 5] are needed. One major challenge for 3D IC is mainly focused with known-good-die (KGD) problem, which limits the yield of 3D-stacking. Test for TSV can be performed at the pre-bond or post-bond stages. The "pre-bond" testing aims at detecting faulty dies prior to adding them to a stacked-die. The "post-bond" testing makes sure the dies are working properly working after stacking, and detects any additional defects that may be introduced during the bonding process, misalignment, high temperature and high pressure [6].

Due to difference in thermal expansion coefficient of the dielectric and the substrate, pin-holes are sometime created in the insulator around the TSV and undesirable leakage current can flow between TSV and substrate resulting in a resistive short between them. Pin-holes may also be the result of impurities inside the insulator or the deposition method itself [7]. The magnitude of pinhole leakage current may be temperature and time dependent [8]. A micro-void defect begins from formation of cavity or void within the TSV body. It is a deformity in the TSV conductor due to incomplete fills, stress cracking or imperfect manufacturing technologies. Depending on the severity of the defect, micro-voids may cause small delay to resistive open through the faulty TSV [7]. Fig. 3.1 shows

the structure of a typical TSV alongside a contactless probe and Fig. 3.2 shows common TSV defects.

Pre-bond capacitive defects and leakage faults are detected using sensitive amplifiers for TSV in [9]. TSV pinholes and voids are detected through a resistance measurement method using a leakage-current sensor and a capacitive bridge in [10]. Another pre-bond testing method is presented in [11] where a group of TSVs are touched simultaneously by a probe needle to form a network of TSVs to measure TSV capacitance and resistance; however this method requires direct TSV probing. An all-digital pre-bond test solution using ring oscillator is presented in [12] to detect resistive open and leakage faults based on the variation of oscillation frequency. TSVs are used as capacitive loads to affect the propagation delay of a ring oscillator in [13] to perform pre-bond testing. Various TSV test solutions have been developed to detect post-bond TSV defects [14-17].

Test access for pre-bond testing is limited by current wafer probe technologies using cantilever or vertical probes. A mechanical probing is reported in [18] for a pitch of 40µm. Current TSVs is 5µm in diameter and has pitches of 10µm or smaller [19]. Thus, large probe pads are required to make contact with individual TSVs, which needs to be added to the die-under-test and may reduce TSV performance. MEMS technology has also been employed for TSV probing [20, 21] which supports the pitch requirement, but may leave scrub marks. Moreover, conventional wafer probes have the limitation of regular maintenance and cleaning, which increases the test time and the costs of manufacturing. Contactless TSV probes have been proposed in the literature to ensure the physical integrity of TSVs during the test phase. Contactless probes operate based on the principle of capacitive [22] or inductive [23] coupling. They offer better mechanical performance and durability than the conventional probes and they support high density and low-pitch requirement for high-density small-pitch probing. Contactless probes eliminate the risks of TSV structural integrity degradation.

In this paper a new delay model for fault free TSV using HFSS and ADS design environments is proposed. The variations of TSV parameters from its nominal values are analyzed to detect voids and pin-holes. The rest of the paper is organized as follows. Section 3.II describes the implemented contactless fault free and faulty TSV structure and

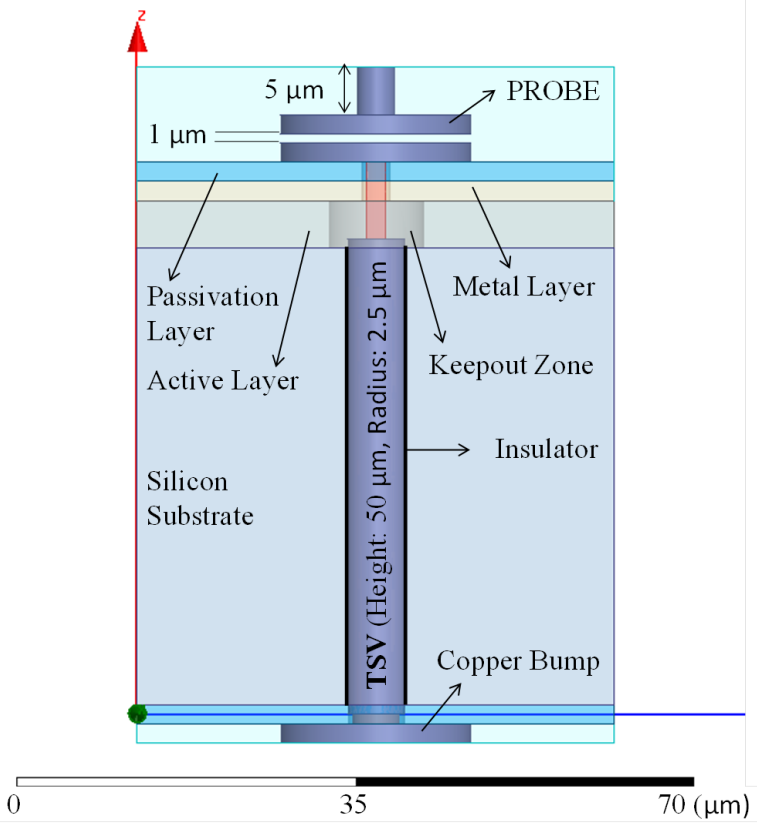


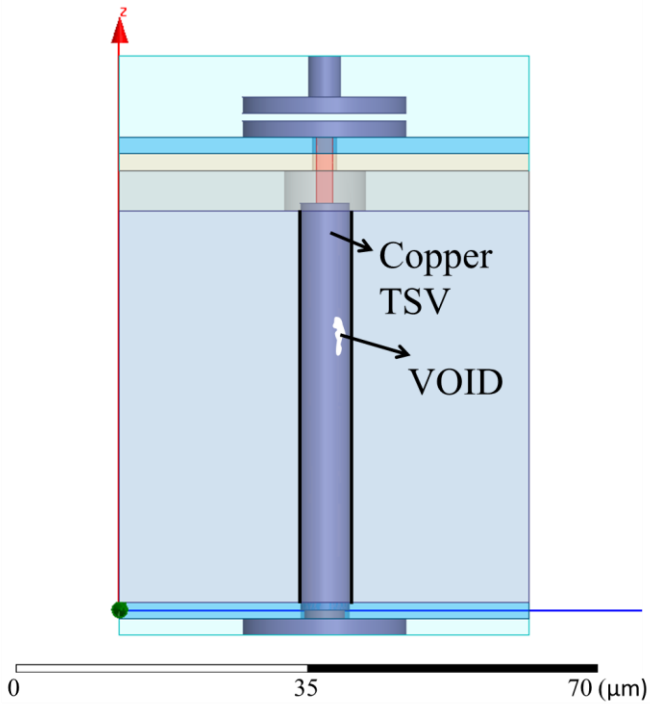
Fig. 3.1: Typical TSV with proposed contactless probe in HFSS.

their lumped models. Section 3.III presents the simulation results for faulty TSV's and Section 3.IV concludes the results.

3.II IMPLEMENTED TSV-PROBE IN HFSS

As shown in Fig. 3.1, a contactless probe and a TSV were designed in HFSS environment. HFSS allows the extraction of a passive Spice model. As shown in the figure, the TSV is realized by a copper wire with 50µm length and 2.5µm radius. There is also a 100nm dielectric layer (SiO2) covering the TSV. The "Keepout Zone" minimizes the effect of TSV stress on active circuits and the "Passivation Layer" protects the TSV structure against environmental effects. The probe tip is designed to have the same 10µm radius as a typical TSV bump. The gap between TSV and probe is 1µm which forms a coupling capacitor between them. The extracted coupling capacitance between the probe

(a)



(b)

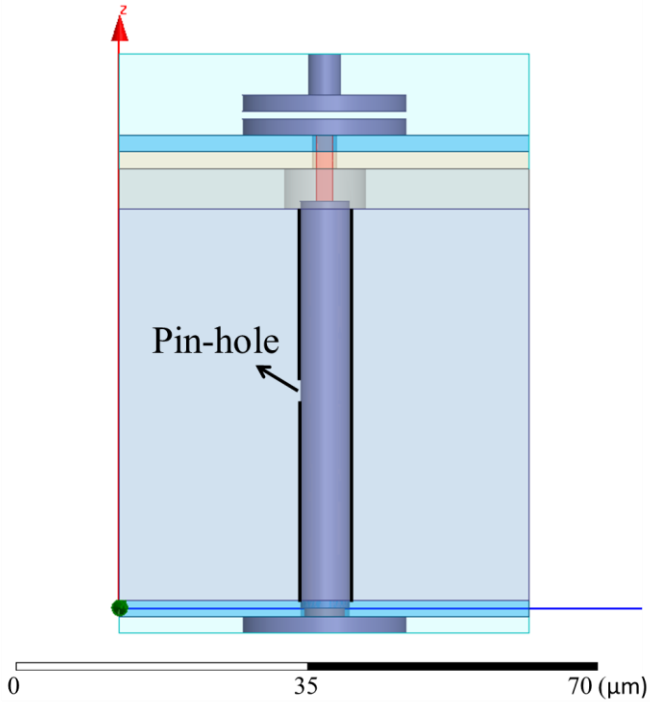


Fig. 3.2: Common TSV defects (a) void and (b) pinhole.

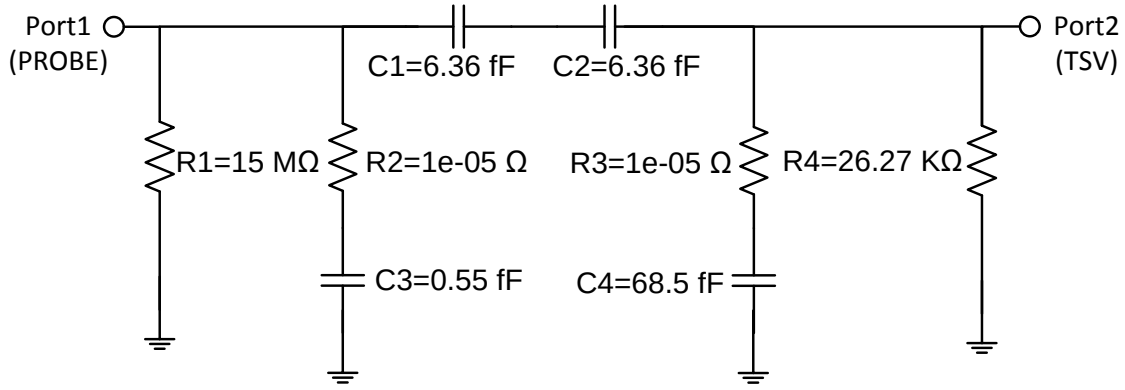


Fig. 3.3: Extracted low-bandwidth lumped model for the implemented fault-free TSV.

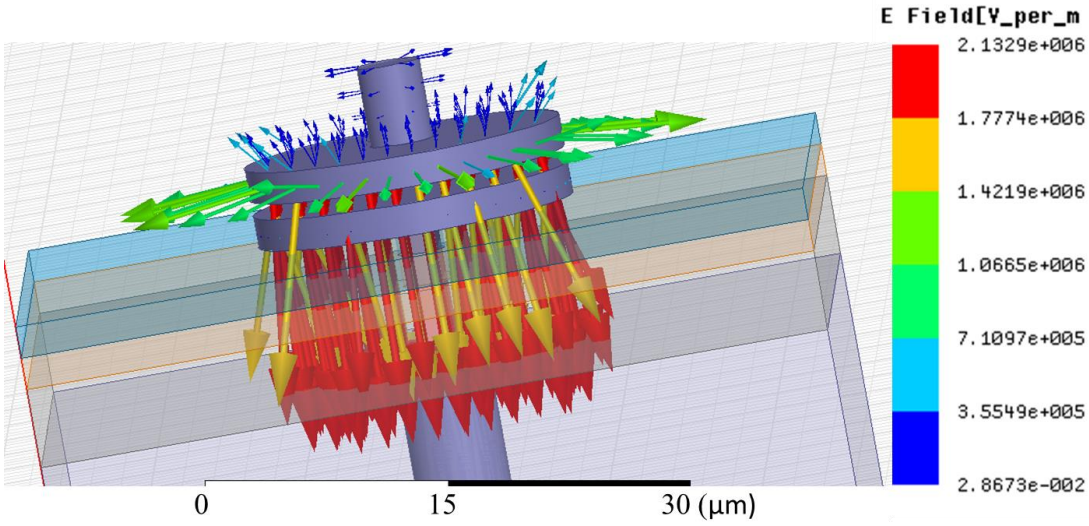


Fig. 3.4: Electric field distribution of the fault-free TSV.

and the fault free TSV is 3.18fF (C1 ‖ C2) as shown in the low bandwidth lumped model in Fig. 3.3, which closely matches the calculated capacitance (2.8 fF). The difference between them is understandable due to the fringing effect. The resistance between the probe and ground (R1) and also between the TSV and ground (R4) are high due to the presence of dielectric. There is a pair of resistor and capacitor in series in the extracted model: R2 in series with C3 between the probe and ground; R3 in series with C4 between TSV and ground. This is justifiable as each port and the substrate can be considered as two conducting plates of a capacitor. The small resistors represent the resistance of the probe and the TSV metal. When the excitation is applied, the maximum

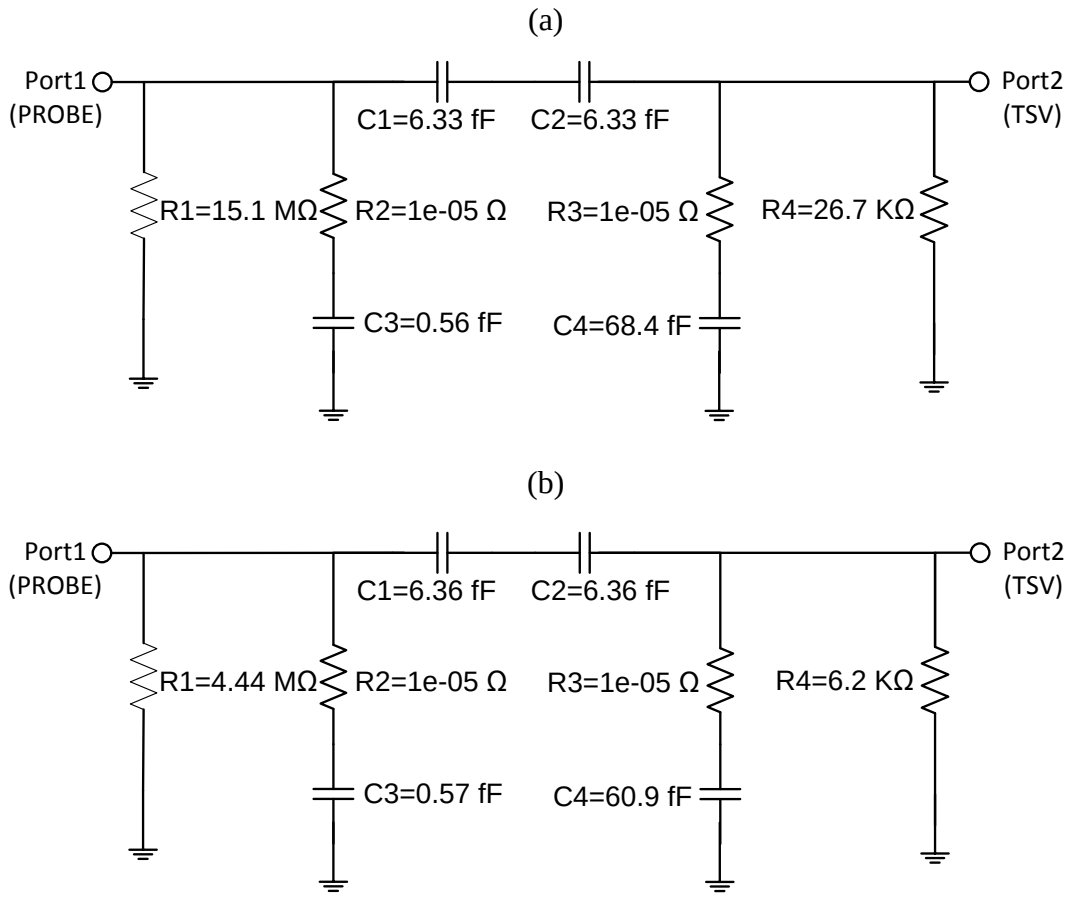


Fig. 3.5: Extracted low-bandwidth lumped model for faulty TSV (a) with a single VOID, (b) with a single pin-hole.

electric field exceeds 2.13 V/μm (Fig. 3.4) which is strong enough to be detected with a low noise amplifier.

To determine the effect of TSV defects on its circuit models, TSVs with pinholes and voids were also implemented using HFSS and their circuit models were extracted. Extracted lumped model in Fig 3.5 (a) shows a similar circuit model as a fault free TSV. The coupling capacitance is slightly reduced. Voids with different sizes were introduced and their circuit models were extracted at 1GHz solution frequency. The results indicate that voids have a minor and in most cases non detectable effect on the TSV equivalent circuit model. This can be understood if the skin effect is taken into consideration. At 1GHz solution frequency, most of the charge carriers find their way through the surface of the TSV and the inner portion of the TSV does not play an important role. To

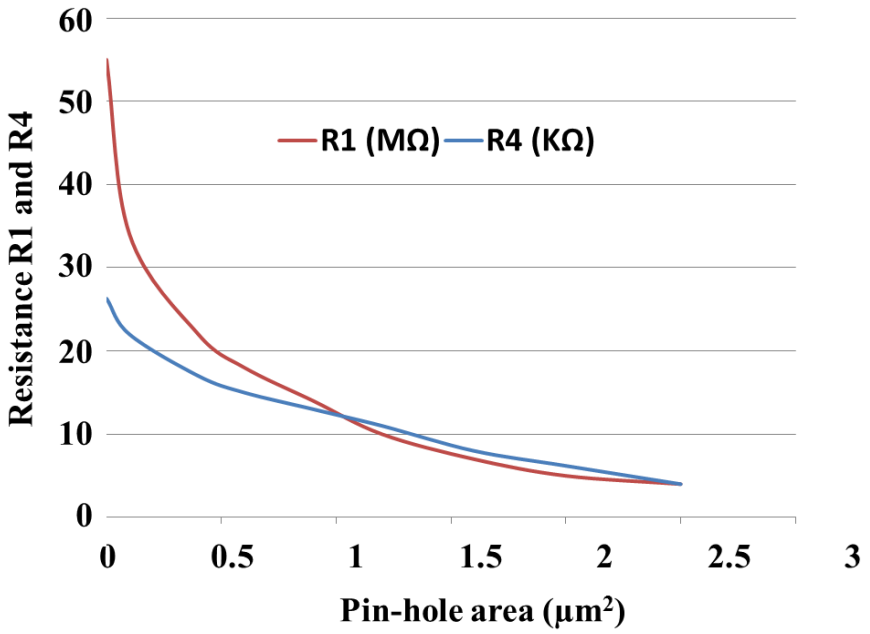


Figure 3.6: Variation in R1 and R4 based on pin-hole area.

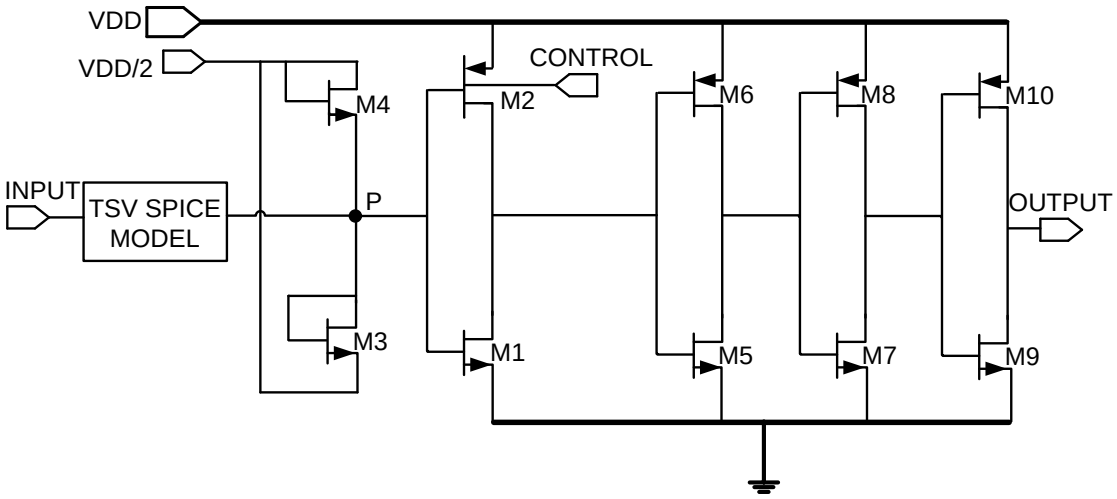


Figure 3.7: Sensing circuit used to reconstruct the TSV data

determine the effect of pin-holes on the TSV circuit model, a pin-hole with 0.5µm thickness and 1µm height is introduced as shown in Fig. 3.2. The extracted lumped model as shown in Fig. 3.5 (b) is very similar to the original fault free model; however the parameter values are different. R1 sharply reduces from 15 MΩ to 4.4MΩ and R4

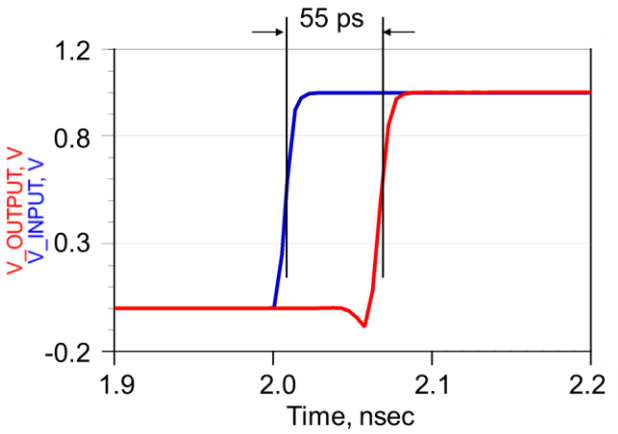
reduces from 26.27KΩ to 6.2KΩ. The coupling capacitance between the TSV and probe is unaffected by pin-holes. Simulations were performed to see the effect of pin-hole size on the TSV circuit model. The results as shown in Fig 3.6 indicate that R1 and R4 decrease non-linearly as the pin-hole size increases. Effects of pin-hole locations were also studied. It was observed that the model parameters are not affected by the physical location. Simulation with multi pin-holes also shows no major impact on the lumped model and parameter values.

3.III CIRCUIT-LEVEL SIMULATION RESULTS AND ANALYSIS

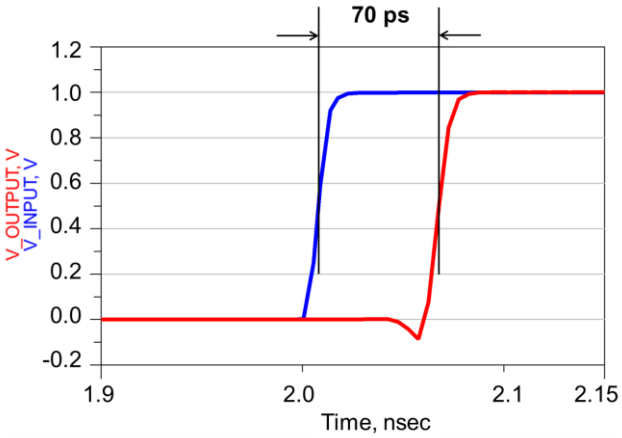
Since the variations of TSV circuit model parameters with defects are minor, a robust and optimal sensing circuit is needed to detect the variations and reconstruct TSV data. Fig. 3.7 shows the schematic diagram of the designed circuit in ADS using TSMC 65nm CMOS technology. M1-M2 form a switching amplifier and M5-M10 form three inverters. M3-M4 prevent node P from accumulating charge. The body of M2 can be controlled externally to minimize the effects of Process, supply Voltage and Temperature (PVT) variations. The TSV fault-free and faulty models are used to perform simulations. A time domain pseudorandom bit sequence was chosen as an input signal and applied to the TSV circuit model. Fig. 3.8 shows the output response of fault free and faulty TSV. As shown in the figure the propagation delay between the input and the output signals is different. For fault free TSV it is 55ps, but for faulty ones it increases to 65-70ps. Eye diagrams at 1Gbps for all three models were plotted. For a fault free TSV the RMS jitter is about 6.6ps with an eye width of 980.6ps. The signal to noise ratio (SNR) is greater than 100dB. For a single void the SNR falls to 42.6dB with jitter increasing to 49ps and with an eye opening of 970ps. For one pin-hole model the eye diagram shows a reduction in SNR to 41dB and the jitter increases to 77.5ps. However, there is still a good eye-opening of ≈940ps as compared to the fault-free TSV. Table 3.I summarizes the eye-diagram information and Fig. 3.9 shows the simulated eye diagrams for faulty TSV at 1Gbps data rate.

The simulation results show a TSV defect can change the propagation delay and the level of jitter and SNR at the output. A high-resolution and accurate sensing circuit can be used to detect TSV faults from the output response.

(a)



(b)



(c)

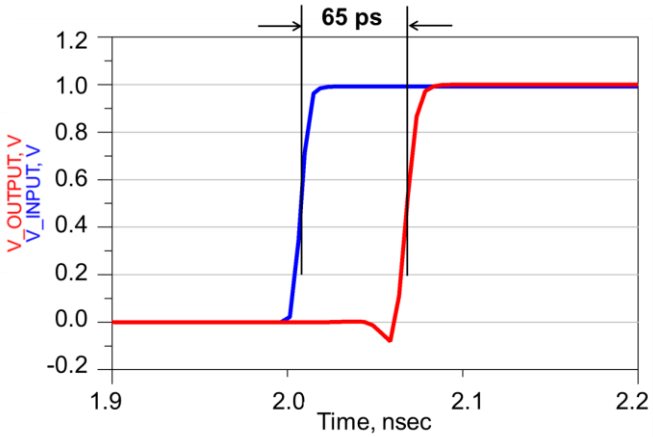


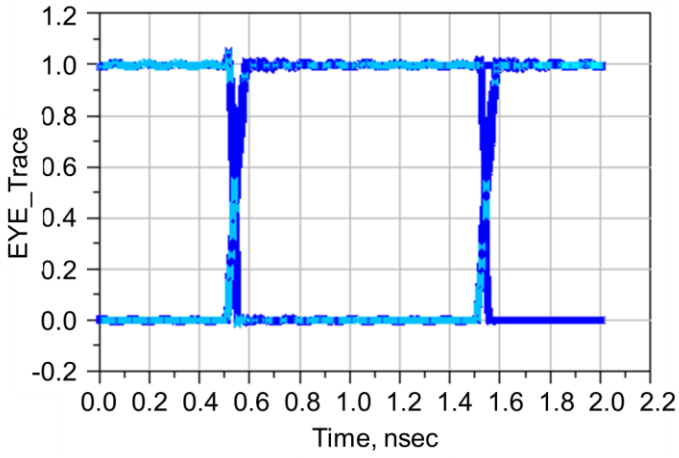
Fig. 3.8: Delay response between input and output in ADS for (a) fault-free TSV and faulty TSV for (b) void and (c) pin-hole.

TABLE 3.I

EYE DIAGRAM FOR FAULT-FREE AND FAULTY TSV AT 1 GHZ

Criteria	Fault-Free	1 VOID	1 Pin-hole
RMS Jitter (pp)	≈ 6.6ps	≈ 49ps	≈ 77.5ps
Eye Width	≈ 980.6ps	≈ 970ps	≈ 940ps
SNR	> 100dB	≈ 42.6dB	≈ 41dB

(a)



(b)

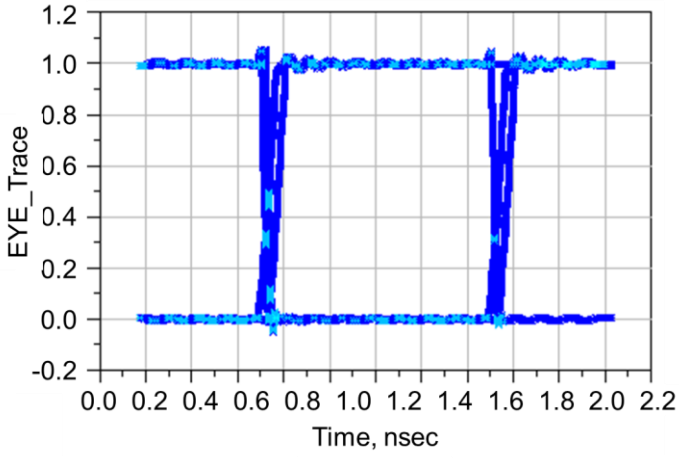


Fig. 3.9: Simulated Eye Diagram at 1 Gbps data rate (a) with a single VOID, and (b) with a single pin-hole.

3.IV CONLUSION

TSV probing with conventional wafer probes can undermine its physical integrity. A contactless TSV probe based on the principle of the capacitive coupling to detect common TSV faults is presented in this work. The proposed solution supports the high-density and low-pitch requirements for testing TSV in 3D stacked ICs. Simulation results using HFSS and ADS CAD tools show that the proposed solution can be used to detect voids and pinholes with 1µm communication range at 1Gbps data rate.

ACKNOWLEDGMENT

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CHAPTER 4

A TEST PROBE FOR TSV USING RESONANT INDUCTIVE COUPLING

4.I INTRODUCTION

Three-dimensional circuit integration has the potential to be a game changer in the field of microelectronics. This technology can open the path to implementation of new generation of low-power ultra-fast Microsystems with significant processing power. Among the potential 3D integration techniques, Through-Silicon Via (TSV) technology has emerged as a viable and efficient solution. TSV technology offers a number of advantages such as the shortest interconnect path between vertically stacked dies, lower power consumption and operation at higher speeds. However, testing TSV interconnects requires development of new design-for-test techniques and test access mechanisms [1, 2]. New fault models may also be required for induced intra-die defects caused by fabrication process variations. TSV testing can be performed at the pre-bond or post-bond [3] stages. Pre-bond tests are performed to detect faulty dies prior to stacking while post-bond tests are developed to not only cover pre-bond faults but also detect defects due to misalignment and imperfect bonding.

Various test methods have been proposed in literature to address the challenges of testing TSVs. A die-level wrapper based on IEEE 1500 has been proposed in [4]. This method supports post-bond die testing through dedicated probe pads on non-bottom dies and intra die interconnects between stacked dies. In [5] a digital test structure based on scan chain and on-chip voltage divider is proposed. This method can detect pre-bond resistive defects in TSVs; however capacitive and small-delay defects are not covered. In this method, tuning and calibration of on-chip sense amplifiers and voltage divider are needed for accurate fault detection. Tuned sense amplifiers have also been used for blind TSVs to detect pre-bond capacitive defects in [6]. To detect small variations of TSV capacitance in this method highly sensitive amplifiers are employed. In [7] a leakage-current sensor and a capacitive bridge are used to detect TSV pinholes and voids. The resistance between the TSV and the substrate is measured through a leakage-current sensor. A DFT based method for pre-bond testing is presented in [8] where multiple

TSVs are shorted together by a probe needle to form a network of TSVs. In this method, the capacitance and resistance of each TSV are detected in the TSV network to identify faulty TSVs. This scheme can detect main TSV defects, but it requires a direct access to TSVs through contact probes. Spring loaded probe technologies including membrane probe cards, thermally-actuated probe needles, and probe needles with electrostatic actuators have also been reported in the literature for TSV testing [9-12]. The technologies used in these methods provide varying degree of control over probe needles to lower the physical stress on the TSV structure. A test access mechanism based on microscale interconnect layer is presented in [13] to test TSVs and micro-bump arrays. In [14], scan chain has been proposed based on genetic algorithm and integer linear programming to detect post-bond TSV defects. Although extensive research has been undertaken in this field there are still major issues to be addressed. Among them a reliable high-speed test access mechanism for TSVs is considered one of the key challenges. Current probe technologies using cantilever or vertical probes cannot be readily used for TSV probing as they exert too much force on the TSV contact surface causing scrub marks and structural damage. Moreover, they require large contact pads to ensure the connectivity and they cannot be readily downscaled to meet the pitch and bump size requirements for new generation of 3D integrated circuits. Conventional wafer probes require routine check, maintenance, and cleaning; which increases the test time and eventually the overall cost of IC manufacturing.

MEMS based test probes [15] have also been proposed as an alternative solution to access TSVs without a considerable physical stress. Although MEMS technology can downscale with the advancement of IC fabrication process and meet the tight pitch requirements however, even this technology does not entirely rule out the possibility of TSV integrity degradation and scrub marks. Furthermore, reliability of physical access using MEMS probe can potentially be a limiting factor. A promising test access mechanism for TSVs which eliminates the risk of physical damage is to access them through contactless probes. Although contactless probing has not gained much ground in the probing industry yet; the difficulties of direct TSV access are expected to eventually drive the industry to seek new solutions and consider alternative methods.

The rest of the paper is organized as follows. The related prior works have been discussed in section 4.II. Section 4.III covers the mathematical representation of resonant inductive coupling and its advantages over the conventional inductive coupling. Circuit models for both cases of resonant and non-resonant coupling schemes have also been presented in this section. In section 4.IV, the implemented resonant inductive probe and 3D full-wave electromagnetic simulation results using High Frequency Structural Simulator (HFSS) from Ansys are presented. Circuit level simulations using Advanced Design System (ADS) tools from Agilent technologies are covered in section 4.V. Section 4.VI presents the discussion and finally conclusions are summarized in section 4.VII.

4.II OVERVIEW OF THE RELATED PRIOR WORKS

Contactless probing provides an attractive solution to overcome some of the limitations of current probe technologies. Unlike conventional probes, contactless probes do not require regular maintenance or cleaning which reduces the overall costs of testing. Besides, contactless probes are not subjected to physical force; hence their mechanical performance and durability are far better maintained as compared to contact probes. Noncontact testing can also be implemented earlier in the manufacturing chain, providing important feedback during the production process [16].

Various techniques have been reported in the literature for contactless communication based on inductive [17,18], capacitive [19,20] and radiative [21] coupling. Inductive based interconnections are current driven; hence energy transmission can be easily increased. Using conventional inductive coupling, contactless communication between two or more layers of stacked face-to-face or face-to-back dies within the same package is possible. For longer distances such as inter-chip or inter-tier communications, inductive signal coupling compared to capacitive coupling is generally more efficient since it exploits magnetic flux that is detectable from several hundreds of microns away.

On the other hand, capacitive coupling has a relatively limited range of operation and can be used for fine face-to-face die assemblies.

In [18] an inductive contactless link for inter-chip clock and data link is presented which supports data rate of 1 Gb/s per channel over distance of 15μm. In this work, conventional coupling technique has been utilized to implement the wireless links. Due to low coupling efficiency, several metal layers have been utilized to implement N-turn inductors to increase magnetic flux and support the communication link.

In this paper, a contactless TSV probe based on the principle of resonant inductive coupling is presented. Resonant inductive coupling has been widely used for proximity identification using Radio Frequency Identification (RFID) technology from the early years of RFID industry due to its high coupling efficiency. This technique has recently been utilized to design wireless chargers for portable devices such as cell phones and tablets. It will be shown that this coupling method has the potential to be used for implementation of a practical wireless probe for TSVs. Resonant inductive coupling as compared to the conventional inductive coupling not only increases the coupling efficiency but also offers a relatively simple implementation solution. In fact, only a microscale inductor and a switch which can be implemented using a transistor are needed at the TSV side to observe its data activity. Such a solution is ideal for TSV probing due to its low footprint. Inductive resonant coupling as compared to the conventional inductive coupling supports longer communication range and consumes less power. Simulation results show that the proposed method can achieve TSV data rate of 2 Gbps without significant signal degradation.

4.III INDUCTIVE COUPLING TECHNIQUE

Circuit diagram of inductively coupled inductors for non-resonant coupling case is shown in Fig. 4.1. The mutually coupled inductors are used to transfer energy from the source to the load. The coupled inductors form a transformer with no magnetic core where the coupling coefficient strongly depends on the distance between the inductors. To highlight the advantages of the resonant coupling compared to the non-resonant coupling, the power delivered to the load have been calculated for both cases. For non-resonant case in Fig. 4.1a, we can write

$$V_s = Z_{11}I_1 - j\omega MI_2 \qquad (1)$$

$$0 = -j\omega MI_1 + Z_{22}I_2 \qquad (2)$$

Where, $Z_{11} = R_1 + j\omega L_1 I_1$, $Z_{22} = R_2 + j\omega L_2 + R_L$ and V_s is the source voltage. M and ω are the mutual inductance and the angular frequency respectively. From (1) and (2) the input impedance Z_{in} is given by

$$Z_{in} = Z_{11} + \frac{(\omega M)^2}{Z_{22}} \qquad (3)$$

The term $(\omega M)^2 / Z_{22} = Z_{ref}$ is in fact the output impedance referred to the input. Thus the circuit in Fig. 1a can be represented by its equivalent circuit shown in Fig. 4.1b. To calculate the power delivered to the load we can represent Z_{ref} with its real and imaginary parts and then find the power delivered to the real part.

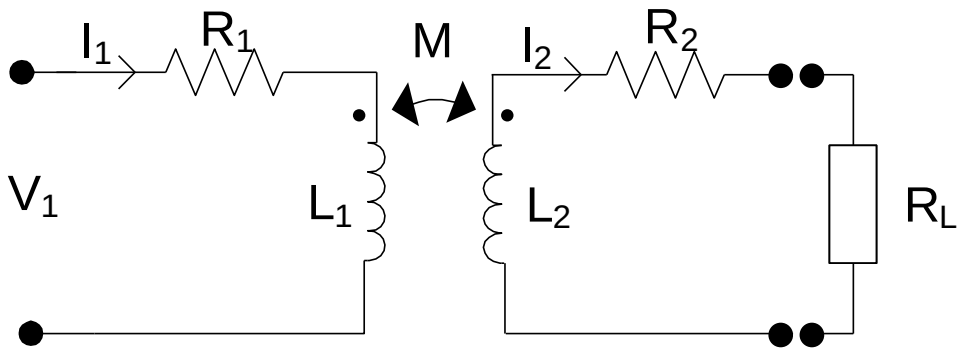
$$Z_{ref} = \frac{(\omega M)^2}{Z_{22}} = r + jx \qquad (4)$$

Substituting for $Z_{22} = R_2 + j\omega L_2 + R_L$ we have

$$r = (\omega M)^2 \times \left(\frac{R_2 + R_L}{(R_2 + R_L)^2 + (\omega L_2)^2} \right) \qquad (5)$$

$$x = -(\omega M)^2 \left(\frac{j\omega L_2}{(R_2 + R_L)^2 + (\omega L_2)^2} \right) \qquad (6)$$

(a)



(b)

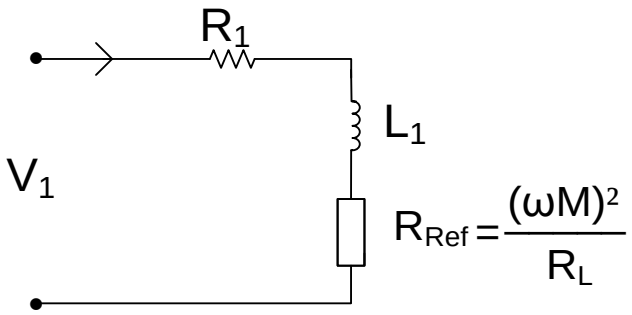


Fig. 4.1: Block diagram of (a) a non-resonant inductively coupled circuit and (b) Its equivalent circuit.

Representing $Z_{11} = R_1 + j\omega L_1 I_1$ and $Z_{ref} = r + jx$ from (3) the input impedance Z_{in} is

$$Z_{in} = [R_1 + r] + j[\omega L_1 + x] = R_{eq} + jL_{eq} \qquad (7)$$

Where R_{eq} and L_{eq} are the total equivalent resistance and inductance at the input of the circuit. The real power consumed at Z_{ref} is the power transferred to the secondary part, P_{22}, which can be determined from

$$P_{22} = |I_s|^2 r = \left(\frac{V_1}{\sqrt{R_{eq}^{\ 2} + L_{eq}^{\ 2}}} \right)^2 r \qquad (8)$$

Where $|I_s|$ is the magnitude of the current flowing in the primary. The total power at the secondary, P_{22}, includes the power delivered to the load R_L and the ohmic loss of R_2. Thus the load power can be found by substituting for r from (5) to (8) and subtracting the ohmic loss which leads to

$$P_L = \left(\frac{V_2}{\sqrt{{R_{eq}}^2 + {L_{eq}}^2}} \right)^2 \times \left(\frac{(\omega M)^2 R_L}{(R_2 + R_L)^2 + (\omega L_2)^2} \right) \qquad (9)$$

It is clear from (9) that both L_{eq} and L_2 play a negative role in the total power delivered to the load. The main idea behind the resonant inductive coupling is to cancel out these terms through resonance using capacitors added to the primary and secondary parts. In an ideal resonant coupling case where the ohmic loss is negligible and L_{eq} and L_2 resonant with C_1 and C_2 equation (9) reduces to

$$P_{L\_res} = \left(\frac{V_s}{R_L} \right)^2 \times \frac{(\omega M)^2}{R_L} \qquad (10)$$

Where P_{L_res} is the load power at resonant frequency. The effect of resonance on the power delivered to the load is significant and in practice P_{L_res} can exceed P_L by orders of magnitude.

In the following analysis it is shown that the current flowing through the primary inductor, L_1, is boosted by its quality factor, Q_1 at the resonant frequency. Where Q_1 by definition is given by $Q_1 = L_1\omega / R_1$. Thus the magnetic flux generated by the primary inductor increases Q_1 times at the resonant frequency which results in a Q_1 times larger voltage across the secondary inductor. Furthermore, the voltage across the load increases by the quality factor of the secondary inductor, Q_2, due to resonance at the secondary. As a result the total voltage across the load increases by a factor of Q_1Q_2 which can be a significant factor if inductors with high quality factors are used.

Assuming time harmonic dependency for the non-resonant circuit in Fig.4.1a we can write,

$$V_1 = I_1(R_1 + L_1 j\omega) \tag{11}$$

$$V_{L2} = k\sqrt{L_1 L_2}\, I_1 \tag{12}$$

Where k is the coupling coefficient and V_{L2} is the induced voltage at the secondary inductor L_2. The magnitude of I_1 from (11) is equal to

$$|I_1| = \frac{V_1}{\sqrt{R_1^{\,2} + (L_1\omega)^2}} \tag{13}$$

For the resonant coupling case, the imaginary part, $L_1 j\omega$, is cancelled out and the magnitude of current in the primary inductor can be determined from $I_{11} = V_1 / R_1$.

Thus, the ratio of the primary currents for resonant and non-resonant cases is

$$\frac{I_{11}}{I_1} = \frac{V_1 / R_1}{V_1 / \sqrt{R_1^{\,2} + (L_1\omega)^2}} = \sqrt{1 + \frac{(L_1\omega)^2}{R_1^2}}$$

which is

$$\frac{I_{11}}{I_1} = \sqrt{1 + Q_1^{\,2}} \approx Q_1 \tag{14}$$

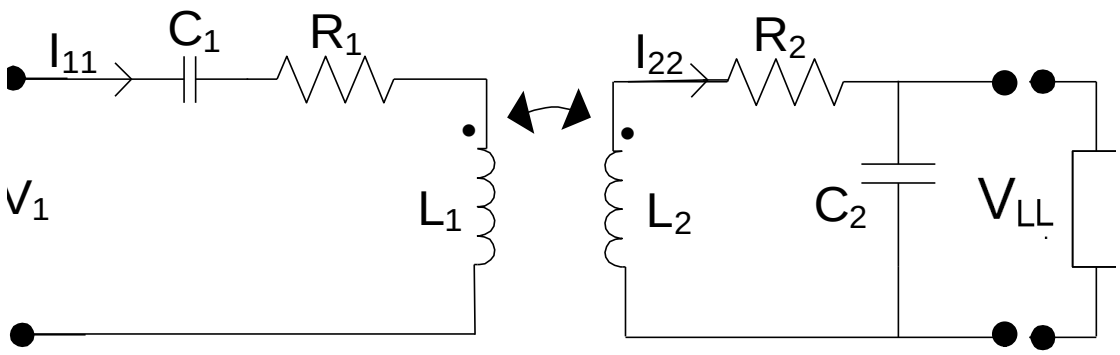
The voltage across the load in this case, V_{LL}, at the resonant frequency from Fig. 4.2a can be found from

$$V_{LL} = I_{c2} \times \frac{1}{C_2\omega} = \frac{V_{L2\_res}}{R_2} \times \frac{1}{C_2\omega} = Q_2 V_{L2\_res} \tag{15}$$

Where $Q_2 = \dfrac{1}{R_2 C_2 \omega} = \dfrac{L_2\omega}{R_2}$, I_{c2} is the current of C_2 at the resonant frequency and V_{L2_res} is the induced voltage in the secondary inductor L_2 at the resonant frequency which is given by

$$V_{L2\_res} = k\sqrt{L_1 L_2}\, I_{11} \tag{16}$$

(a)



(b)

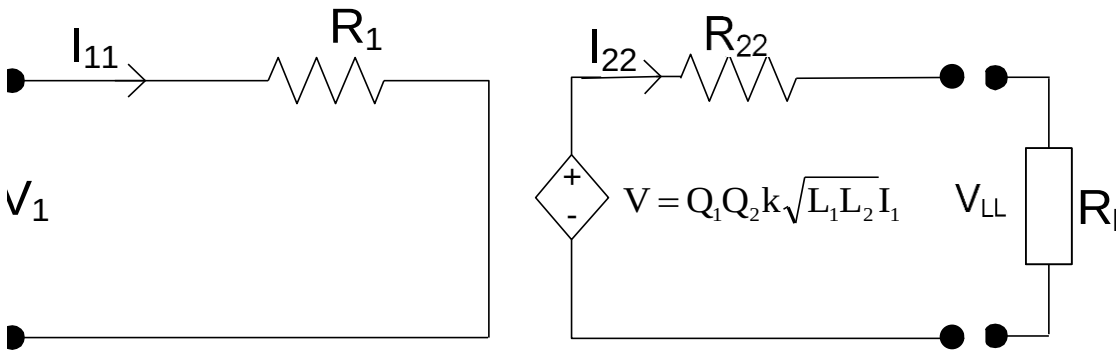


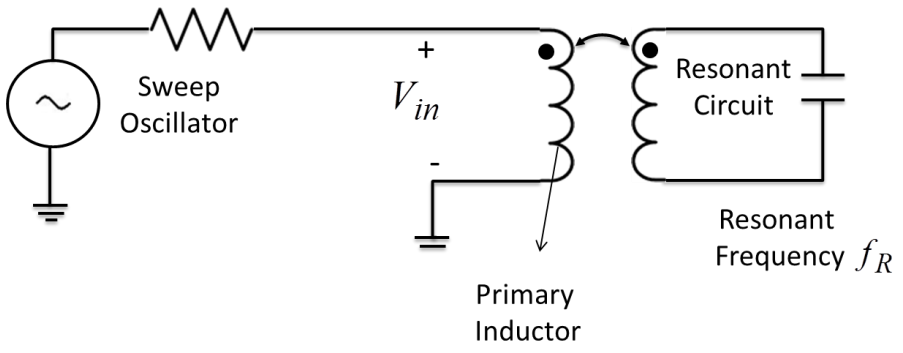
Fig. 4.2: Block diagram of (a) a resonant inductively coupled circuit and (b) Its equivalent circuit.

From (13), (15) and (16) we can write

$$V_{LL} = Q_1 Q_2 k \sqrt{L_1 L_2}\, I_1 \qquad (17)$$

The voltage across the load for the conventional coupling case from (12) compared to (16) indicate that the voltage across the load for the resonant coupling case is $Q_1 Q_2$ times higher than the conventional coupling case. In fact when the distance between the coupled inductors increases the coupling coefficient, k, decrease however the reduction of coupling coefficient can be compensated for by the quality factors of the inductor if resonant coupling is employed.

(a)



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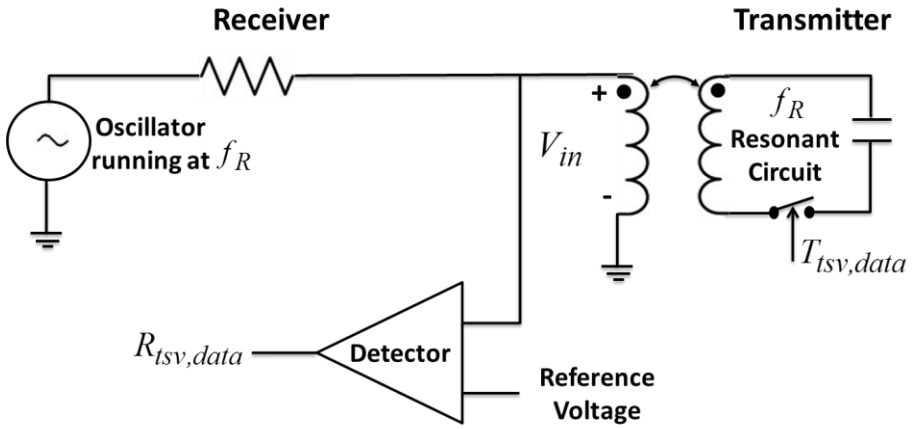


Fig. 4.3: Contactless link utilizing resonant inductive coupling (a) Using a sweep oscillator to detect resonant circuit. (b) Using an oscillator running at resonant frequency to observe TSV data.

Fig. 4.3a shows how the concept of resonant inductive coupling can be utilized to implement a contactless link. The circuit diagram in Fig. 4.3a includes two inductors which are mutually coupled and a capacitor which forms an LC tank with the secondary inductor. The oscillator sweeps its frequency over a certain range to detect the resonant circuit at the secondary from variations of voltage across the primary inductor. At the resonant frequency, the LC tank absorbs maximum amount of energy and a relatively high current flows through the primary inductor. As a result, the voltage across the primary inductor, V_{in}, drops abruptly.

Fig. 4.3b shows how a contactless link can be implemented to observe TSV data stream. TSV data are used to turn on and off a switch between L and C in the LC tank. As a

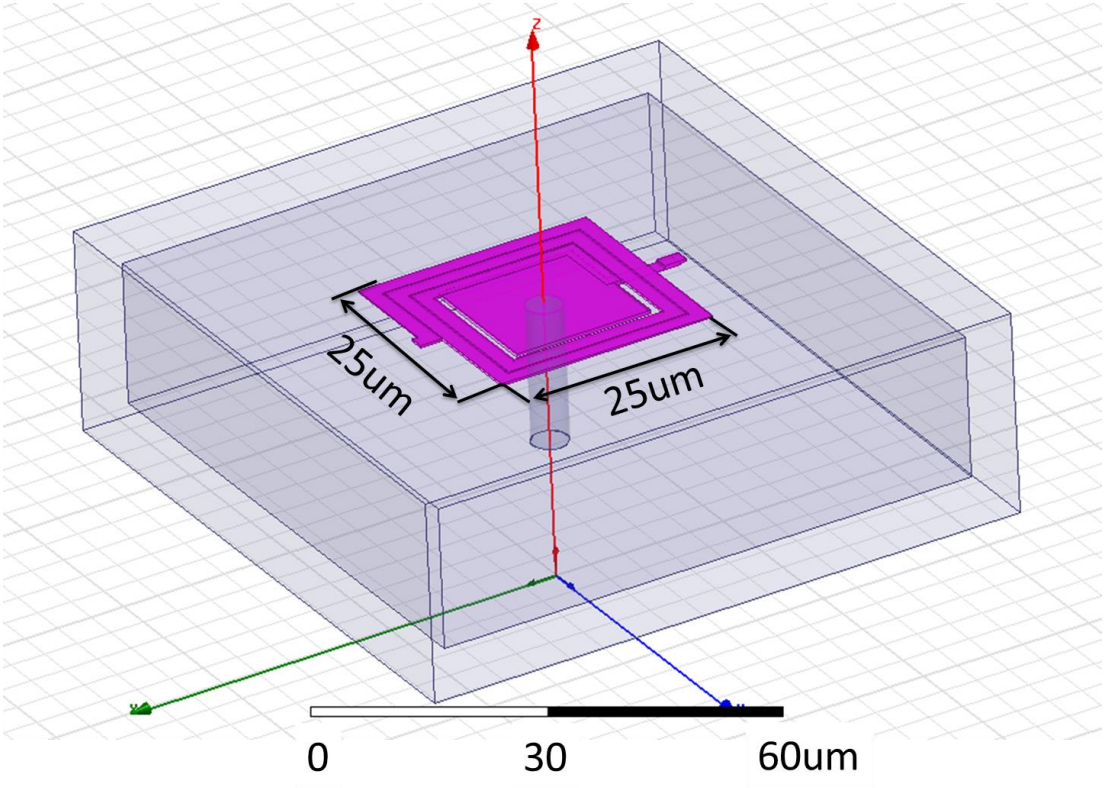
result, the voltage across the primary inductor is modulated by the TSV data. The TSV data can then be reconstructed from the voltage variations across the primary inductor. The communication range of resonant inductive coupling mainly depends on the intensity of the magnetic field at the primary and secondary inductors and the sensitivity of the detection circuitry used to demodulate voltage variations across the primary. This scheme can be used for communication over a few tens of micrometers in 3D IC configuration without a significant power consumption or area overhead.

4. IV 3D SIMULATION AND SPICE MODEL EXTRACTION

To analyze an inductively coupled TSV and extract its circuit model, three dimensional full wave simulations were performed using High Frequency Structure Simulator (HFSS) tools from Ansoft. Fig. 4.4 shows a TSV with a micro bump pad used to switch an inductor to perform 3D simulations. It has to be noted that the inductor can be implemented anywhere on the die-under-test. Nevertheless due to the small size of the required inductor, it can be fabricated around the TSV without affecting its pitch requirements considerably. As shown in Fig. 4.5a the probe which includes an inductor of the same size has been placed on top of the TSV inductor.

The magnetic field generated by the TSV inductor when excited by a voltage source of one volt with a source impedance of 50 ohms is shown in Fig. 4.5b. It is clear that the main portion of the magnetic flux finds its way into the probe inductor which can affect the voltage across its terminals. S-parameter simulation results in Fig. 4.6 for the implemented structure in Fig. 4 indicate that the inductor, which is controlled by the TSV, self-resonates at 92 GHz. To detect the resonance at such a high frequency a microwave sweep oscillator is needed. Implementation of such a high speed circuit using current CMOS technologies is a challenging task. Although, the transit frequency of the current CMOS technologies is far higher than 92GHz however a reliable operation cannot be guaranteed. An easy solution is to add an extra capacitor in parallel to the inductor to lower the resonant frequency.

(a)



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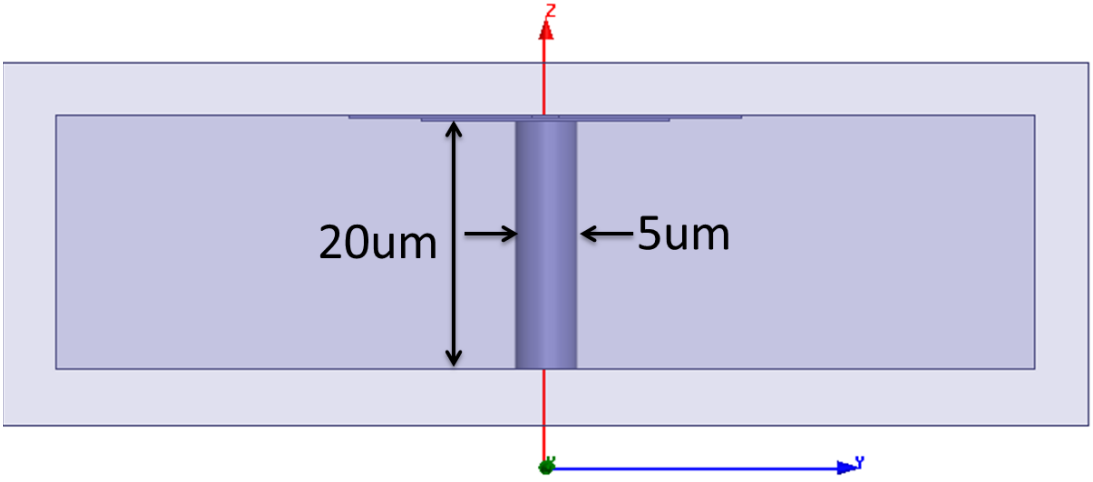
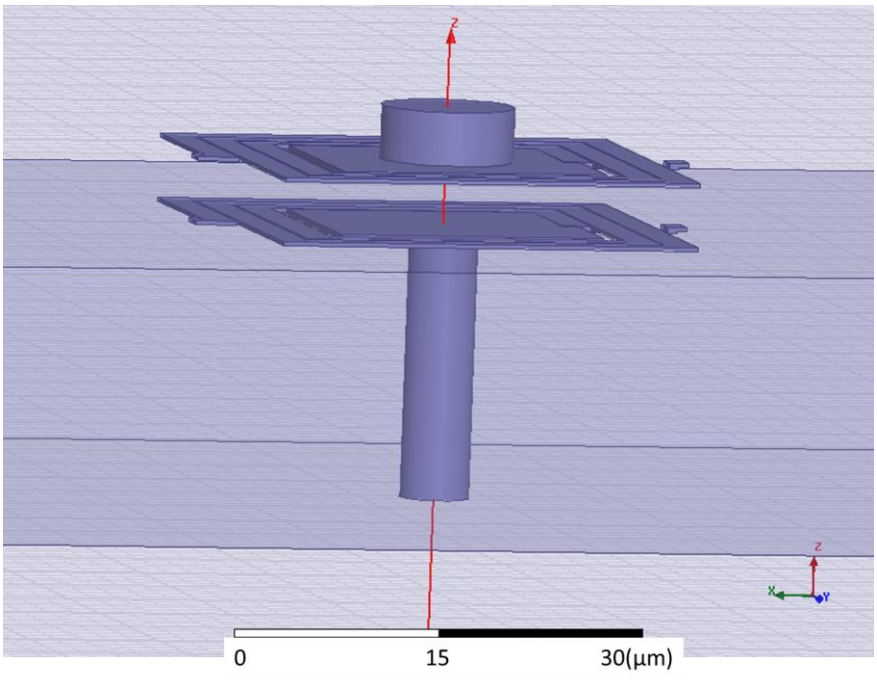


Fig. 4.4: TSV with a micro bump connected to an inductor used to perform 3D full wave simulations.

(a)



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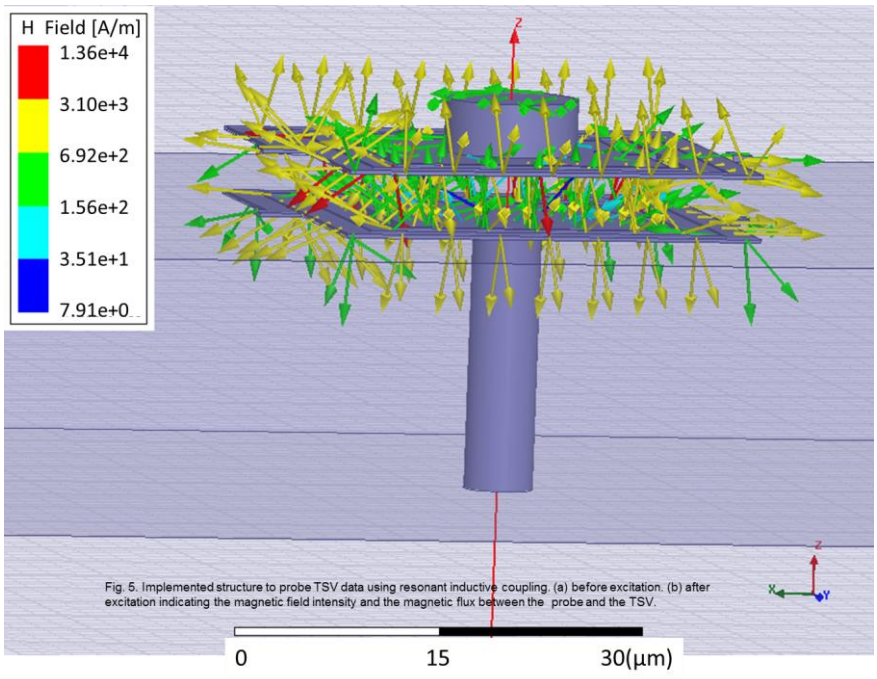

Fig. 4.5: Implemented structure to probe TSV data using resonant inductive coupling. (a) Before excitation. (b) After excitation indicating the magnetic field intensity and the magnetic flux between the probe and the TSV.

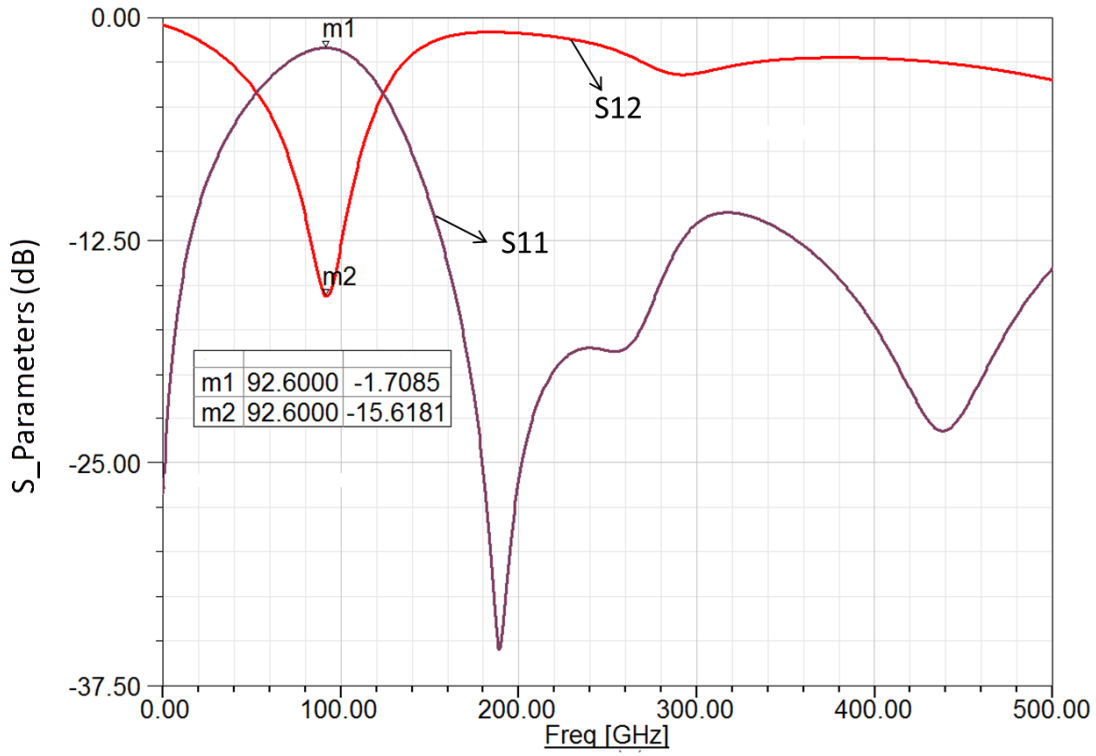

Fig. 4.6: S-parameter simulation results for the implemented structure shown in figure 4.

However, taking into consideration the number of TSVs in a typical 3D IC, this solution can increase the area overhead considerably. The required microwave oscillator and the detection circuitry which reside on the tester can be implemented using any high speed technology.

HFSS has the capability to automatically generate spice models from 3D simulation results. To perform circuit simulation, the structure shown in Fig. 4.5a was simulated in HFSS environment and spice models were generated for the gap between TSV and probe changing from 1μm to 15μm. The spice models were then imported to ADS environment for circuit simulations. It is shown in the following section that TSV data observation does not require any high frequency circuit at the TSV side.

4.V CIRCUIT SIMULATION RESULTS

Fig. 4.7 shows the schematic diagram of the circuit used to observe TSV data with the contactless probe. TSV data are used to turn on and off transistor M_1 which acts as a

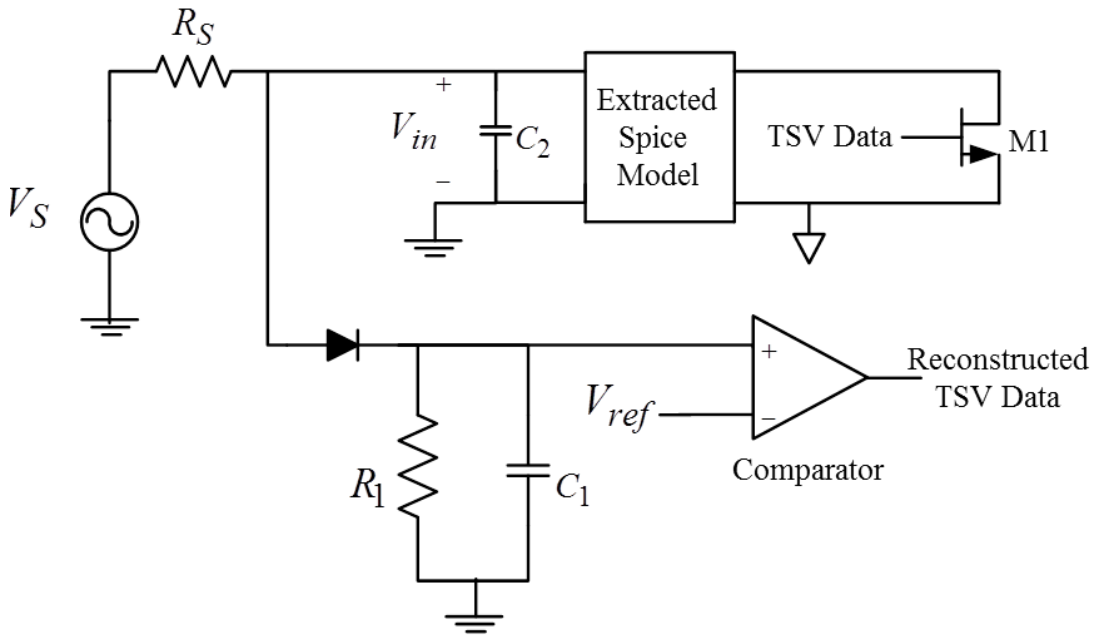

Fig. 4.7: Schematic diagram of the circuit used to observe TSV data with the contactless probe.

switch and controls the impedance across the secondary inductor. The detection circuitry includes an envelope detector which is formed by D_1, R_1 and C_1 to demodulate the source signal modulated by the TSV data. The output of the envelop detector is applied to a comparator to generate appropriate logic levels. Fig. 4.8 shows AC simulation results for a case where the probe and the TSV are 5μm apart. The two plots in this figure indicate the variations of voltage across the primary inductor, V_{in}, when M_1 is on and off. A slight variation of the voltage across the primary inductor can be seen at frequencies close to 60GHz. However, the peak value of V_{in} does not change with the state of M_1. This is due to the fact that the impedance seen from the primary and the secondary inductors are not equal and their resonant frequencies are different. In an ideal case the resonant frequencies of both sides of coupling inductors have to be equal. To increase the coupling efficiency and ensure maximum voltage variations across the primary a capacitor was added in parallel to the primary inductor to lower its resonant frequency. Fig. 4.9 shows simulation results after such modification. It can be seen that the inductors resonate at the frequency close to 60GHz. The voltage across the primary inductor experiences much higher variations in this case when M_1 turns on and off. Although the resonant frequency

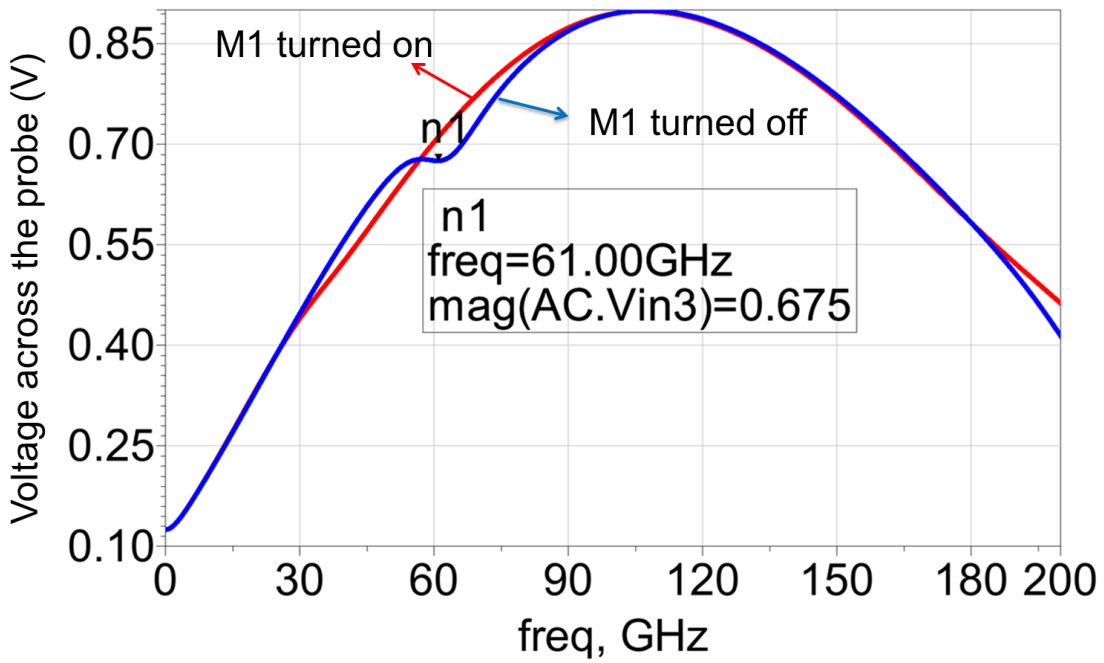

Fig. 4.8: AC simulation results when the TSV and the probe are 5µm apart and they have different resonant frequencies.

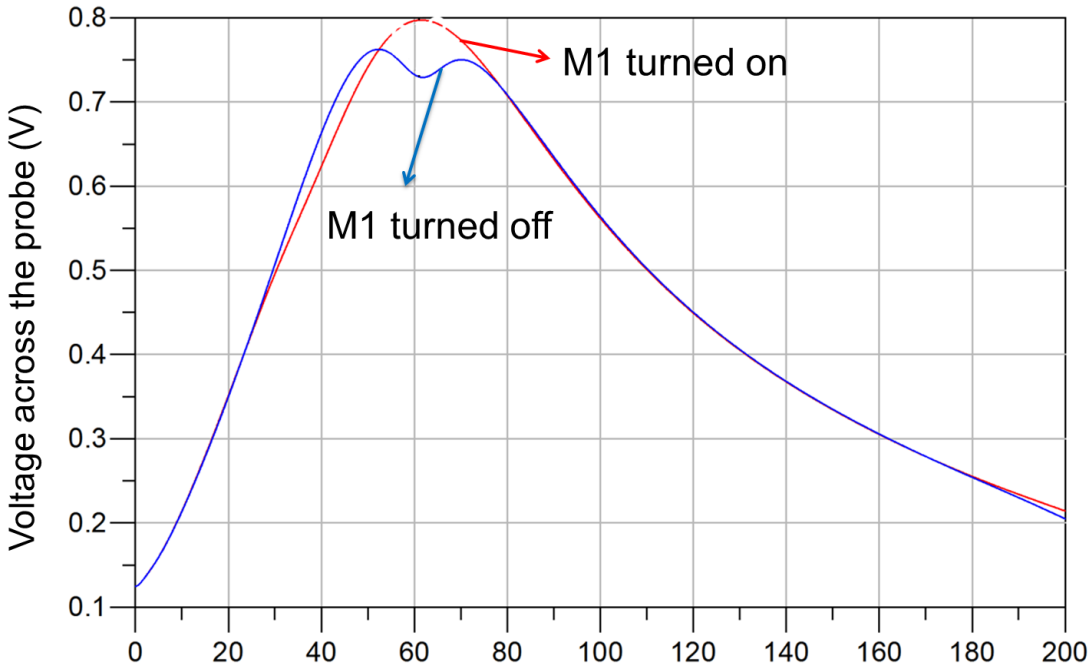

Fig. 4.9: Variations of voltage across the contactless probe when M1 is turned on for a case where both the primary and secondary resonate at the same frequency.

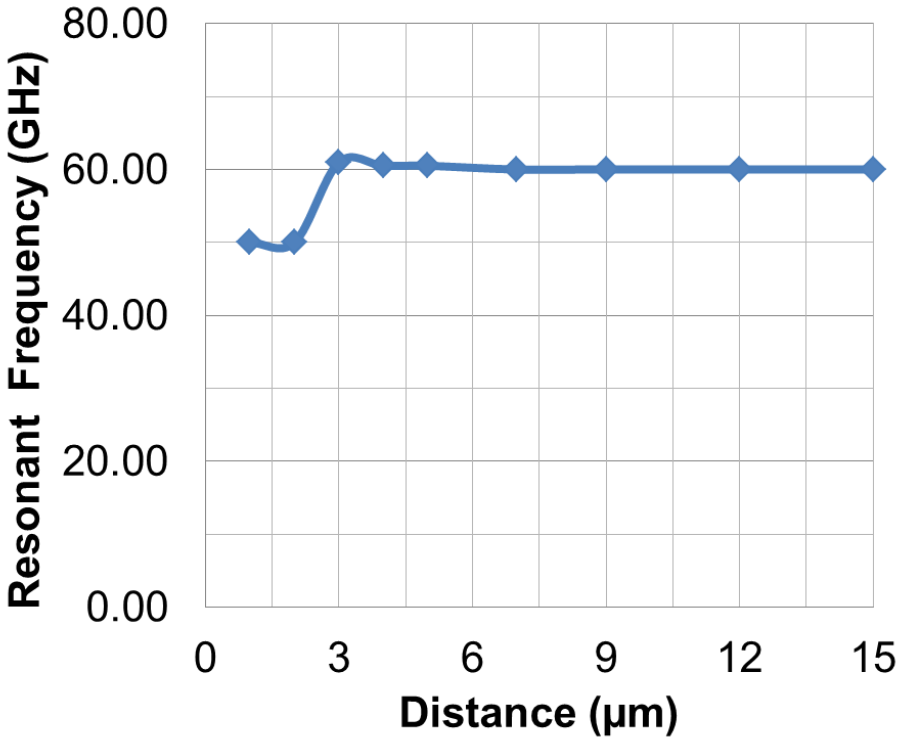

Fig. 4.10: Variations of resonant frequency with distance.

is expected to be constant but simulation results indicate that it changes considerably when the distance between the probe and the TSV falls below 2μm as shown in Fig. 4.10. At close distances a capacitance between the inductors, which have planar geometry, is formed increasing the total capacitance seen by them and lowering the resonant frequency. At distances higher than 3μm the effect of mutual capacitance fades away and the resonance frequency remains constant. Variations of distance between the probe and the TSV under test, as expected, affects the voltage drop across the probe. The communication range for the implemented scheme, where the probe can be effectively used to observe TSV data, is mainly determined by the magnitude of the voltage variations across the probe, V_{in} , when the TSV data are applied. Fig. 4.11 shows maximum variations of V_{in} versus distance between the probe and the TSV. For the implemented scheme, TSV data running at 2Gbps can be properly observed for the gap between the probe and TSV ranging from 1μm to 15μm. When the gap increases beyond 15μm the variations of the voltage across the primary inductor falls below 7mV which increase the RMS jitter of the reconstructed signal considerably.

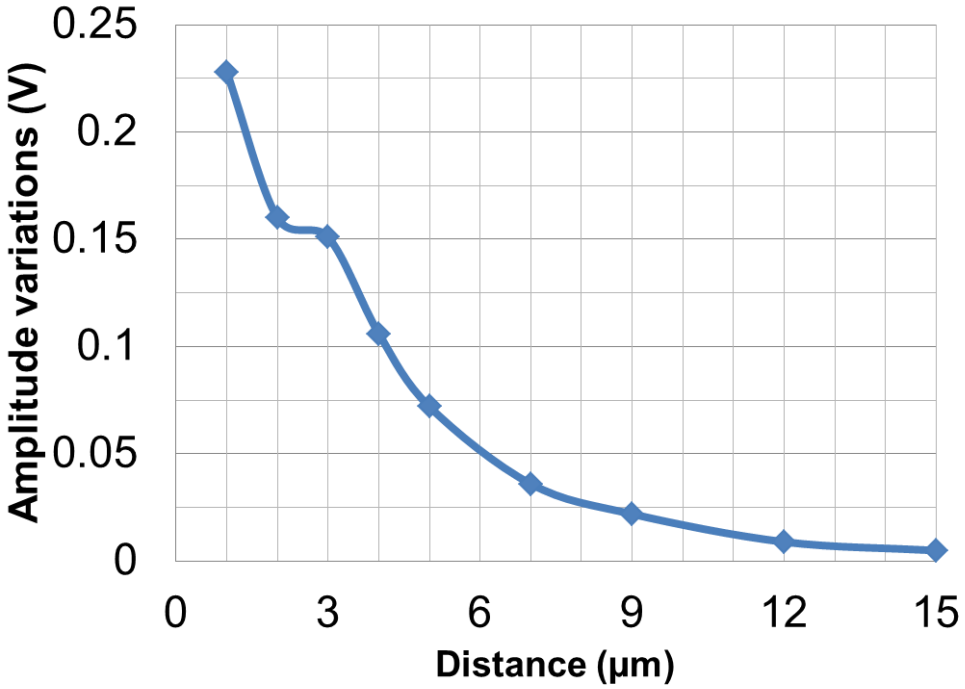

Fig. 4.11: Variations of voltage across the contactless probe with distance.

To evaluate the performance of the implemented wireless link, pseudorandom bit sequence (PRBS) with register length of 8-bits running at 2Gbps was applied, as TSV data, to the gate of transistor M_1 in Fig 4.7. The extracted spice model for a case where the TSV and the probe are 3µm apart was used to conduct the test. The applied TSV data and the voltage across the probe are shown in Fig 4.12. It can be seen that the voltage across the probe is modulated and the amplitude changes with the switching activity of TSV data. The modulated signal is applied to the envelop detector for demodulation and then compared against a reference voltage as shown in Fig. 4.7 to restore the logic levels. The applied data stream and the reconstructed signal in Fig. 4.13 show that the probe can successfully captured and reconstructed high speed TSV data streams. To evaluate the quality of the wireless link between the probe and the TSV, eye diagram of the output for TSV data comprising a stream of alternating binary zero and one bits running at 2Gbps was created. The measurement results on the eye-diagram in Fig. 4.14 show a good eye opening with eye-height of 0.94V and eye-width of 220ps. The maximum RMS jitter remains below 4.2ps and signal to noise ratio exceeds 35dB. At higher speeds the ratio of signal to noise as expected falls and the RMS jitter increases. When the data rate

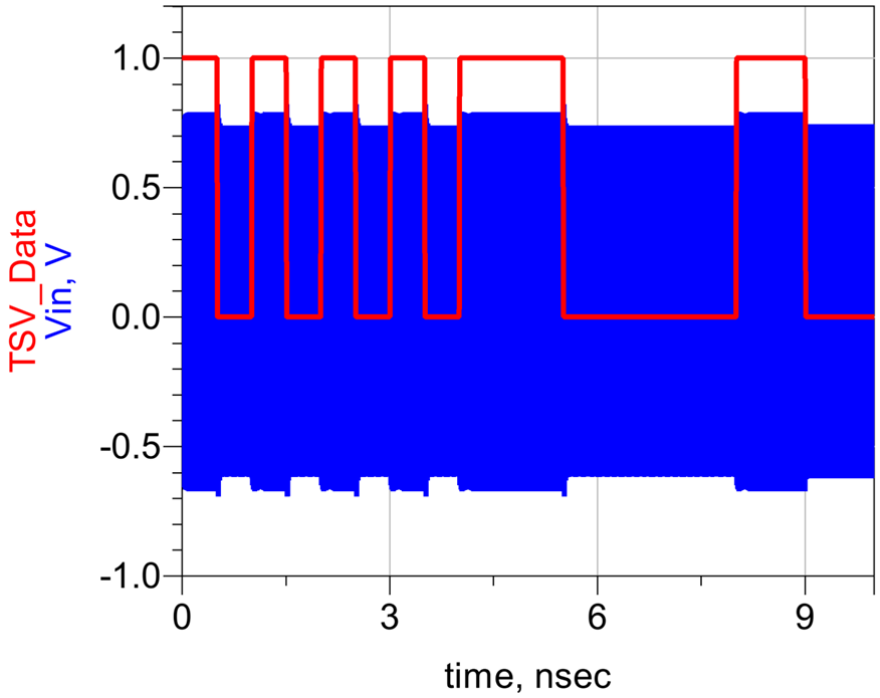

Fig. 4.12: TSV pseudorandom bit sequence running at 2 Gbps and the resultant modulated signal across the probe.

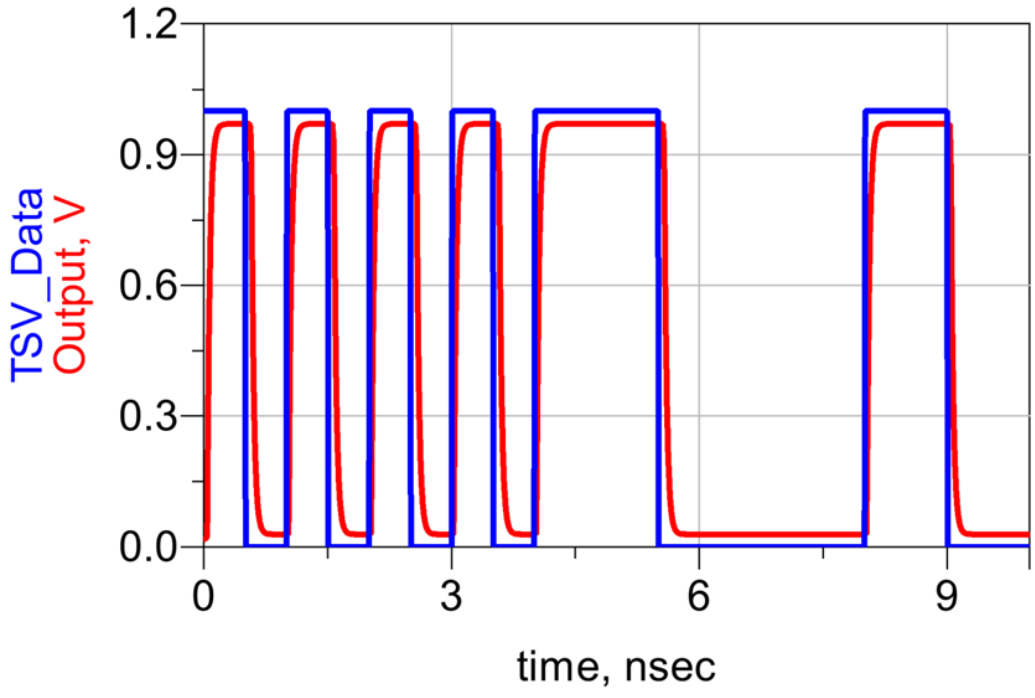

Fig. 4.13: TSV data sequence and the reconstructed data.

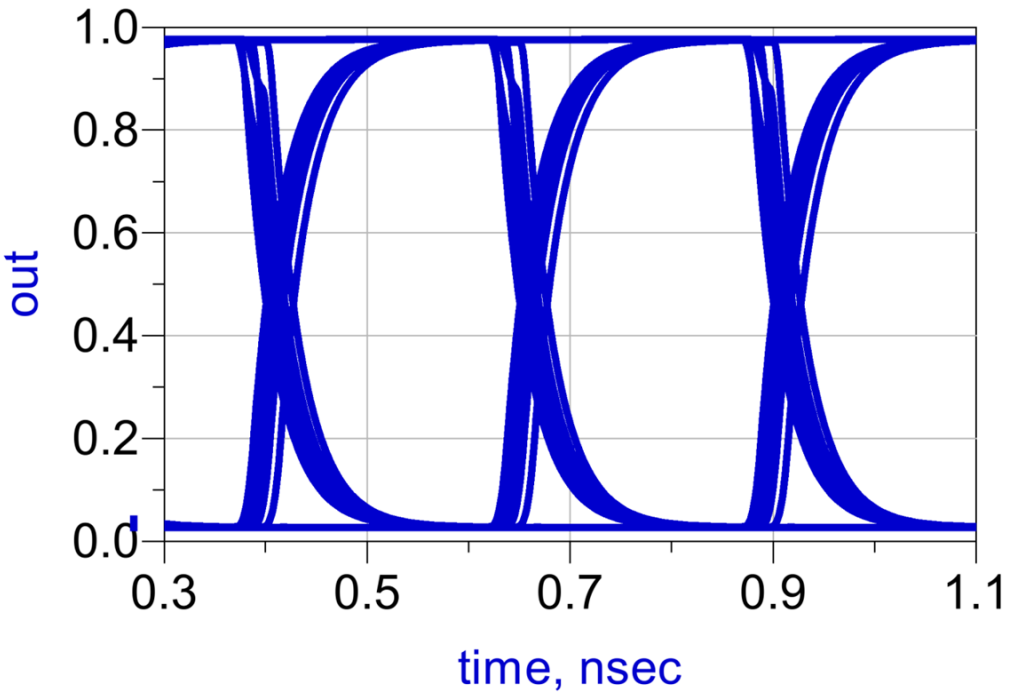

Fig. 4.14: Eye diagram of the signal observed by the contactless probe for TSV data running at 2Gbps.

increases to 10Gbps as shown in Fig. 4.15 the eye opening closes. At this speed the eye opening closes considerably and the RMS jitter raise to 9.4ps. To study the effects of interference from adjacent TSVs and probes two tests were conducted to cover multi-probe and multi-TSV cases. Three TSVs were placed 40µm far from each other as shown in Fig 4.16. Simulation results indicate that the intensity of the magnetic field and the magnetic flux passing though the adjacent probe decrease considerably. The induced magnetic field from adjacent TSV to the probe is 30.7dB lower than the field induced directly from the probe aligned with the TSV. The effect of adjacent probe activities on the TSV signal has also been studied. Fig. 4.17 shows multi-probe and single TSV. The magnetic field generated by an adjacent probe has a negligible effect on the TSV logic levels and induces less than 1mV voltage across the TSV inductor.

The effects of probe misalignment were also investigated. Misalignment in the directions are parallel to the TSV tip up to 1µm does not have a significant effect on the TSV data observation by the probe. This is expected as the length and width of the implemented inductors are much higher than 1µm and the overall magnetic field induced in the probe

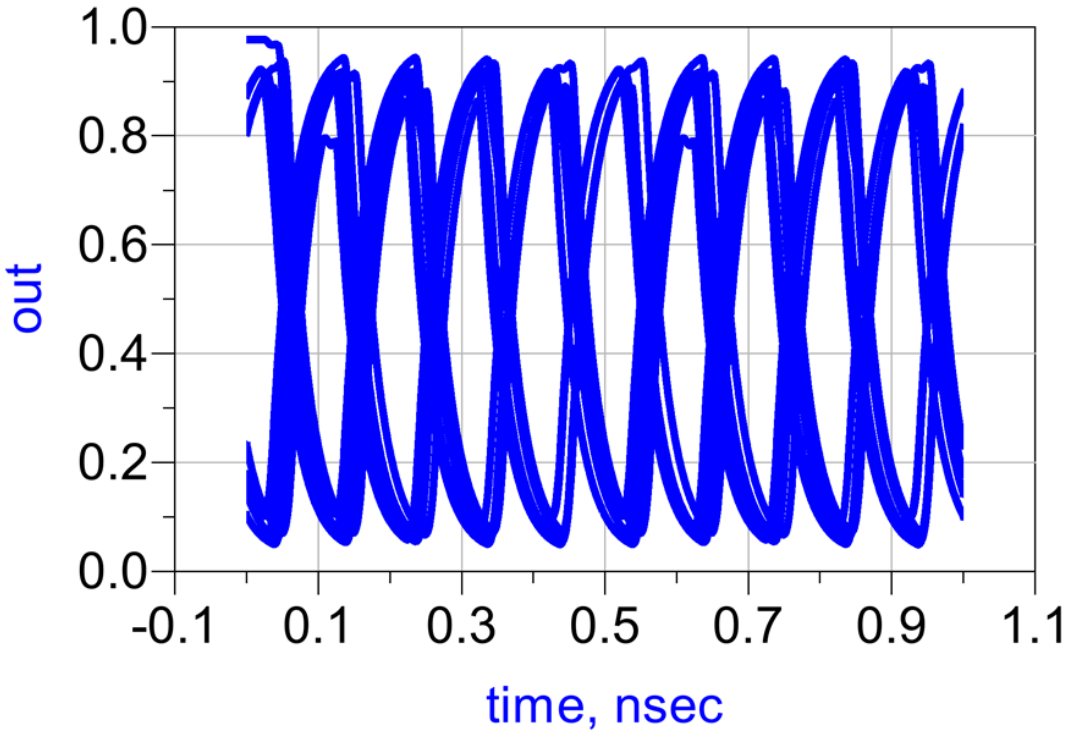

Fig. 4.15: Eye diagram of the output when the TSV data runs at 10Gbps.

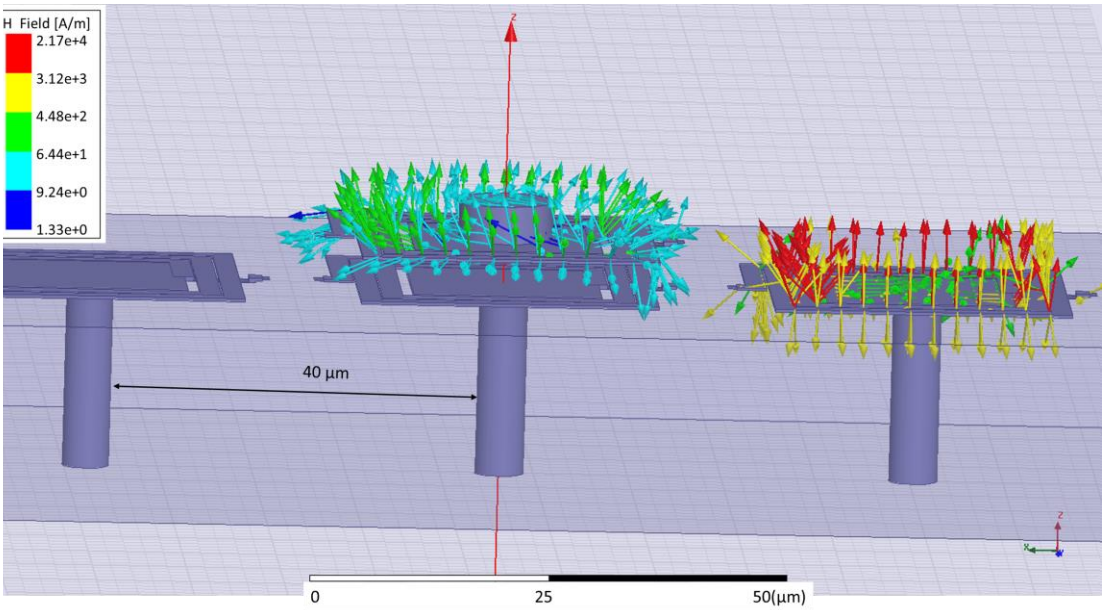

Fig. 4.16: Induced magnetic field from an active TSV on adjacent probe.

does not change significantly with a slight misalignment in the direction parallel to the TSV tip. However misalignment in the vertical direction by more than 0.2µm can

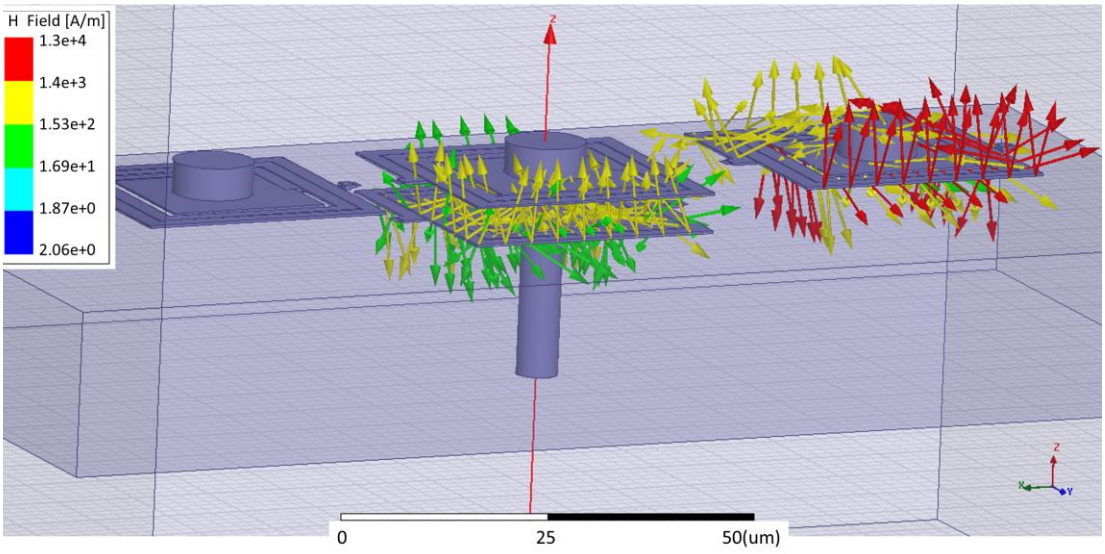

Fig. 4.17: Induced magnetic field from an excited probe on an adjacent TSV.

undermine the quality of the wireless link. This is due to the variation of magnetic field intensity between the probe and the TSV which is inversely proportional to the distance between them. It has to be mentioned that although the proposed contactless probing provides an attractive solution for TSV data observation, it cannot be readily used to control TSV in the test phase. To control TSV data in this method, a microwave oscillator and a high speed low noise comparator is needed. Implementation of these components on the tester for TSV data observation can be justified however adding them on the die-under-test to control TSV is not acceptable solution. To design a comprehensive contactless test mechanism for TSVs a hybrid solution composed of conventional coupling and resonant coupling can be adopted. In this scheme TSV data are controlled through conventionally coupled inductor while its data activities are observed via resonant coupling.

4.VI DISCUSSION

Although contactless TSV probing is an attractive alternative solution and it is a step in the right direction to handle the problem of 3D IC testing, there are major issues that need to be addressed. How to deliver power and how to simultaneously control and observe test data using contactless probes are some of the questions that need to be answered.

Among the different contactless probing methods, capacitive coupling is more suited for short range communication over a few micrometers. This method as shown in [20] can be implemented with minor changes to the die under test. For longer range communications, inductive coupling can be utilized. To further increase the communication range, instead of conventional coupling method, resonant inductive coupling technique can be used. The required communication range determines the number of turns for the inductor associated with the TSV and there is a tradeoff between the communication range and the TSV pitch requirements. It is clear that for a longer range communication larger inductors are needed. The size of the inductor can potentially affect the minimum pitch between the TSVs. Although the inductor can be implemented far from the TSV to handle the pitch requirement, the separation of TSV and its associated inductor increases the routing complexity.

How to power up the die-under-test for the purpose of contactless probing is an important issue that needs to be investigated. Wireless power delivery to microelectronic chips is not a new science and low power circuits such as passive UHF RFID tags extract their entire power from incoming electromagnetic waves to communicate over a few meters. However, implementation of this method for the purpose of die testing may not be justified due to the area overhead. A basic RF to DC converter requires an antenna, a rectifier and a few voltage doublers. It seems that the power delivery using dedicated power pads and contact probes is still the most viable solution.

Another important issue that needs to be addressed is the fact that contactless probes are more suited for data observation. To apply TSV test stimuli through a contactless probe, a sensing circuitry has to be added to the TSV side. The sensing circuit for capacitive coupling as presented in [20] is relatively simple. However, the sensing circuit for resonant inductive coupling is complicated and requires high-speed precision circuits. To control data over long distances instead of resonant inductive coupling the conventional inductive coupling similar to the method presented in [18] can be used. The sensing circuit in this case can be implemented using relatively large inductors to ensure a robust wireless link. Although further investigation is required to come up with a practical test

solution for 3D ICs using contactless probes, the authors believe that a hybrid contactless TSV probing has the potential to address most of the challenges.

In such a scheme power is delivered through contact probes, capacitance coupling is utilized to observe or deliver short distance data and resonant inductive coupling is used for long distance data observation.

4.VII CONCLUSION

Testing Through Silicon Vias (TSV) plays a critical role in successful integration of three dimensional ICs. TSV probing via commonly used wafer probes can lead to excessive stress on TSV and undermine its physical integrity. It is shown in this work that a high speed contactless probe, based on the principle of resonant inductive coupling, can be designed to observe TSV data stream. Resonant inductive coupling has been widely used for RFID applications due to its high coupling efficiency. This coupling method as compared to the conventional coupling offers much higher coupling efficiency and thus supports longer communication range. Moreover, it can be readily utilized for TSV data observation. The proposed scheme has a small footprint on the TSV side and can be implemented using just an inductor which is slightly larger than TSV bump and a transistor. Three dimensional fullwave electromagnetic simulations were conducted to extract spice model of the probe. Circuit level simulations indicate that a sequence of TSV data running at 2Gbps can be captured and reconstructed by the proposed probe with less than 4.2ps rms jitter and more than 35dB signal to noise ratio.

ACKNOWLEDGMENT

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CHAPTER 5

CONCLUSION

3D ICs provide a promising solution to the interconnect-related problems such as delay and power consumption encountered in 2D design. As discussed in chapter 1, 3D ICs offer many advantages including short interconnects, small footprints, high data rates, improved performance and bandwidth, and low power consumption. However, testing 3D ICs comes with some challenges and the 2D test technologies such as direct probing may not be able to address the challenges of test requirements for 3D ICs. Direct TSV probing can undermine their physical integrity and may cause defects during the test phase. Contactless testing using capacitive and inductive coupling provides an alternative solution for TSV probing without affecting their physical integrity.

This dissertation details the design and implementation of capacitive and inductive contactless methods, and reports simulation results performed in HFSS and ADS design environment. The capacitive coupling method is simple to implement but suffers from low communication range. On the other hand, the inductive coupling based method requires a more complex circuit implementation, but offers higher communication range. The effects of bond-wire, cross-talk, and probe size have also been analyzed and reported.

A prototype was fabricated using TSMC 65nm technology and Cadence design environment through CMC. The chip was tested and measured, and the results were compared with simulation results. Chapter 2 and Chapter 3 in this dissertation present the results and findings based on capacitive coupling. Chapter 4 shows the work based on inductive coupling. In Appendix B, a list of submitted journal and conference papers is presented.

The main contributions of the dissertation are summarized as follows:

- A contactless TSV probing method using capacitive coupling is proposed and simulated. A prototype is fabricated using TSMC 65nm CMOS technology and experimental measurements are carried out to validate the proposed method. The measurement results indicate that this TSV probing scheme presents -55dB insertion

loss at 1GHz frequency and maintains higher than 35dB signal-to-noise ratio within 5µm range.

- A microscale contactless probe based on resonant inductive coupling has also been developed and simulated. Experimental measurements on a prototype fabricated using TSMC 65nm CMOS technology indicate that TSV data can be captured by the probe and reconstructed when the distance between the TSV and the probe remains less than 15µm.

FUTURE DIRECTIONS

3D ICs with multiple layers of stacking may lead to higher power density and thus thermal issues are always a concern. Since the dimensions and pitch are very low, little variation in temperature may damage the chip permanently and decrease the yield. Thus, a thermal-aware testing method can be integrated with the contactless method in the future.

Transfer of power among the stacks is still a field of research. Even though there are published works for contactless power transfer, the size of the inductor needed for wireless power transfer is significant and may not be readily incorporated within a 3D IC. It is possible to use inductors with high quality factors using a separate layer on the stacked die to power up a 3D IC through a wireless channel.

APPENDIX A

LIST OF PUBLISHED TRANSACTIONS AND CONFERENCE PAPER NOT DIRECTLY RELATED TO THIS DISSERTATION

Title of the Publication	**Publication Status**
Nabeeh Kandalaft, Iftekhar Ibne Basith and Rashid Rashidzadeh, "Low-Contact Resistance Probe Card using MEMS Technology", IEEE Transaction for Instrumentation and Measurement (TIM), Volume: PP, Issue: 99, Publication Year: 2014, Page(s): 2882-2889.	Published in IEEE TIM
Mohammed Alamgir, Iftekhar Ibne Basith, Tareq Mohammad Supon, Rashid Rashidzadeh, "Improved Bus-Shift Coding for Low-Power I/O" in proceedings of the 2015 IEEE International Symposium on Circuits and Systems (ISCAS), May 24-27, 2015, Lisbon, Portugal.	Published in IEEE ISCAS 2015

APPENDIX B

LIST OF SUBMITTED TRANSACTIONS AND CONFERENCE PAPER, BOTH DIRECTLY RELATED AND NOT RELATED TO THIS DISSERTATION

Title of the Publication	**Publication Status**
Iftekhar Ibne Basith and Rashid Rashidzadeh, "A Contactless Test Probe for TSV Based 3D ICs using resonant inductive coupling".	Submitted to IEEE TIM
Iftekhar Ibne Basith, Tareq Mohammad Supon, Rashid Rashidzadeh, and Esam Abdel-Raheem, "Comparative Study on Bus-Coding Schemes and Improvement on SINV Coding".	Submitted to IEEE ICM 2016
Iftekhar Ibne Basith, Tareq Mohammad Supon, Esam Abdel-Raheem, and Rashid Rashidzadeh, "Efficient Integrated Bus Coding Scheme for Low-Power I/O".	Submitted to IET Journal for Circuits, Devices and Systems

APPENDIX C

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