# Hybrid MOS and Single-Electron Transistor Architectures towards Arithmetic Applications 

Guoqing Deng<br>University of Windsor

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# Hybrid MOS and Single-Electron Transistor Architectures towards Arithmetic Applications 

by<br>Guoqing Deng<br>A Dissertation<br>Submitted to the Faculty of Graduate Studies through the Department of Electrical and Computer Engineering in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy at the University of Windsor<br>Windsor, Ontario, Canada<br>2011<br>© 2011 Guoqing Deng

# Declaration of Co-Authorship / Previous Publication 

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I hereby declare that this thesis incorporates materials that are the result of research taken under the supervision of my supervisor Dr. C. Chen. Results related to this research are reported in Chapters 3 through 6, inclusive.

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| Thesis Chapter | Publication title / full citation | Publication status |
| :---: | :---: | :---: |
| Chapter 3 | G. Deng and C. Chen, "Performance Analysis and Improvement for Hybrid CMOS-SET Circuit Architectures," in Proc. 1st Microsystems and Nanoelectronics Research Conf. (MNRC), Ottawa, Canada, 2008, pp. 109-112. | published |
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| Chapter 4 | G. Deng and C. Chen, "Full Adder Design using Hybrid CMOS-SET Parallel Architectures," in Proc. 9th IEEENANO, Genoa, Italy, 2009, pp. 206-209. | published |
|  | G. Deng and C. Chen, "Hybrid CMOS-SET Arithmetic Circuit Design using Coulomb Blockade Oscillation Characteristic," Journal of Computational and Theoretical Nanoscience (JCTN), vol. 8, no. 8, pp. 1520-1526, Aug. 2011. | published |
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|  | G. Deng and C. Chen, "Frequency Synthesis for Arithmetic Operations using SET/MOS Hybrid Architectures," IEEE Transactions on VLSI Systems, August, 2011 (7 pages). | submitted |

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## Abstract

Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) and Single-Electron Transistor (SET) hybrid architectures, which combine the merits of both MOSFET and SET, promise to be a practical implementation for nanometer-scale circuit design. In this thesis, we design arithmetic circuits, including adders and multipliers, using SET/MOS hybrid architectures with the goal of reducing circuit area and power dissipation and improving circuit reliability.

Thanks to the Coulomb blockade oscillation characteristic of SET, the design of SET/MOS hybrid adders becomes very simple, and requires only a few transistors by using the proposed schemes of multiple-valued logic (MVL), phase modulation, and frequency modulation. The phase and frequency modulation schemes are also further utilized for the design of multipliers with more discussions.

Two types of SET/MOS hybrid multipliers are presented in this thesis. One is the binary tree multiplier which adopts conventional tree structures with multi-input counters (or compressors) implemented with the phase modulation scheme. Compared to conventional CMOS tree multipliers, the area and power dissipation of the proposed multiplier are reduced by half. The other is the frequency modulated multiplier following a novel design methodology where the information is processed in the frequency domain.

This method involves the design of digital-to-frequency and frequency-to-digital conversions which are also implemented with SET/MOS hybrid architectures. In this context, we explore the implicit frequency properties of SET, including both frequency gain and frequency mixing. The major merits of this type of multiplier include: a) simplicity of circuit structure, and b) high immunity against background charges within SET islands.

One of the biggest challenges associated with SET-based circuits is the background charge effect. Background charges are mainly induced by defects or impurities located within the oxide barriers, and cannot be entirely removed by today's technology. Since these random charges deteriorate the circuit reliability, we investigate different circuit solutions, such as feedback structure and frequency modulation, in order to counteract this problem. The feedback represents an error detection and correction mechanism which offsets the background charge effect by applying an appropriate voltage through an additional gate of SET. The frequency modulation, on the other hand, exploits the fact that background charges only shift the phase of Coulomb blockade oscillation without changing its amplitude and periodicity. Therefore, SET/MOS hybrid adders and multipliers using the frequency modulation scheme exhibit the high immunity against these undesired charges.

To my wife, Jieqiong Gu.

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## List of Abbreviations

| ADC | Analog-to-Digital Converter |
| :--- | :--- |
| BC | Background Charge |
| BCD | Binary-Coded Decimal |
| BDD | Binary Decision Diagram |
| BSIM | Berkeley Short-Channel Insulated-gate FET Model |
| CLA | Carry Look-ahead Adder |
| CMOS | Complementary Metal-Oxide-Semiconductor |
| CNT | Carbon Nano Tube |
| CP | Charge Pump |
| CPA | Carry Propagation Addition |
| DAC | Digital-to-Analog Converter |
| DFC | Digital-to-Frequency Converter |
| EC | Electron Counting |
| FA | Full Adder |
| FDC | Frequency-to-Digital Converter |
| FIB | Focused Ion Beam |
| FSR | Frequency Synthesizer |
| ITRS | International Technology Roadmap for Semiconductors |
| LPF | Low Pass Filter |
| MAJ | Majority Gate |
| MC | Monte Carlo |
| ME | Master Equation |
| MIB | SET compact model named after three authors |


| MOSFET | Metal-Oxide-Semiconductor Field-Effect Transistor |
| :--- | :--- |
| MVL | Multiple-Valued Logic |
| NTT | Nippon Telegraph and Telephone |
| PADOX | Pattern Dependent Oxidation |
| PDP | Power-Delay-Product |
| PFD | Phase Frequency Detector |
| PLL | Phase-Locked Loop |
| PPA | Partial Product Accumulation |
| PPG | Partial Product Generation |
| PTL | Pass-Transistor Logic |
| RCA | Ripple Carry Adder |
| RNG | Random-Number Generator |
| SED | Single-Electron Device |
| SEEL | Single-Electron-Encoded Logic |
| SET | Single-Electron Transistor |
| SIMON | Simulation Of Nanostructures |
| SOI | Silicon-On-Insulator |
| SPICE | Simulation Program with Integrated Circuit Emphasis |
| SRAM | Static Random-Access Memory |
| STM | Scanning Tunneling Microscope |
| TLG | Threshold Logic Gate |
| VCO | Voltage-Controlled Oscillator |
| VLSI | Very-Large-Scale Integration |

## List of Symbols

## Notation Definition

!.」 Floor function
$e \quad$ Fundamental charge of an electron, $e \approx 1.6 \times 10^{-19} \mathrm{C}$
$k_{B} \quad$ Boltzmann's constant, $k_{B} \approx 1.38 \times 10^{-23} \mathrm{~J} / \mathrm{K}$
$h \quad$ Planck's constant, $h \approx 6.63 \times 10^{-34} \mathrm{~J} \cdot \mathrm{~s}$
$E_{C} \quad$ Electron charging energy
$E_{k} \quad$ Electron kinetic energy
$\tau_{t} \quad$ Time taken by an electron tunneling through a junction
$R_{T} \quad$ Tunnel junction resistance
$C_{T} \quad$ Tunnel junction capacitance
$C_{G} \quad$ Gate capacitance of SET
$C_{\Sigma} \quad$ Total device capacitance on the island of SET with respect to ground
$\left.\begin{array}{l}C_{\text {gdo }} \\ C_{g s o}\end{array}\right\}$ Gate-drain and gate-source overlap capacitances per unit gate width
$\left.\begin{array}{l}C_{g d l} \\ C_{g s l}\end{array}\right\} \quad$ Gate-drain and gate-source overlap capacitances per unit gate length
$t_{o x} \quad$ Gate oxide thickness
$V_{\text {tho }} \quad$ Threshold voltage for the long channel device at zero $V_{D S}$
$T \quad$ Absolute temperature
$\delta \quad$ Slope of the ramp voltage with the unit of V/s

## Chapter 1

## Introduction

### 1.1 Motivations

The scaling-down of the size of MOS transistors according to Moore's law - the number of transistors on a chip doubles about every two years - has taken place for the last 40 years, and pushed today's CMOS technology towards the sub-50nm regime [1] (Moore's law has been adjusted around 2001 to reflect the realities of integrated circuits, and currently it states that the number of transistors is going to increase about 1.3 times every two years). However, MOSFET cannot be shrunk beyond certain limit. The International Technology Roadmap for Semiconductors (ITRS) [2] stated that "we have reached the point where the horizon of the roadmap challenges the most optimistic projections for continued scaling of CMOS." While some advanced technologies, such as high- $k$ dielectric, metal gate, or ultrathin silicon-on-insulator (SOI) film, may extend CMOS lifetime, 10 nm gate length is labelled as the showstopper region where CMOS is going to face some fundamental limits, such as quantum limit. In order to continue the fascinating performance of CMOS scaling, various nanotechnologies have been investigated, bringing forward the advent of a new generation of nano-devices.

### 1.2 Single-Electron-Tunneling Technology

Single-electron-tunneling technology [3] is among the most promising candidates for next-generation electronics which allows the control of a single electron or a small number of electrons. A basic element of this technology is the tunnel junction which can be used to build many different single-electron devices (SEDs), such as single-electron box, single-electron pump, single-electron trap, and so on. Single-electron transistor (SET) [4] is a special type of SED which is featured by its extremely-small size, ultra-low power dissipation, and unique Coulomb blockade oscillation characteristic. By utilizing such novel characteristics of SET, one is able to realize new functionalities with less number of devices.

In contrast to CMOS technology where current flows continuously, the charge transport in a SET is discretely controlled by the tunnel junction. Electrons are considered to tunnel through a tunnel junction strictly one after another.

SET itself exhibits some intrinsic drawbacks, such as low current drivability, small voltage gain, and low temperature operation. Studies have shown that MOSFET and SET are rather complementary. Hybrid MOS and SET architectures which combine the merits of both MOSFET and SET promise to be a much practical implementation for nanometre-scale circuit design [5].

### 1.3 Research Objectives

The work presented in this thesis has three objectives:

1. To design arithmetic circuits, including adders and multipliers, using hybrid MOS and SET architectures.
2. To further reduce circuit area and power dissipation by utilizing SET's unique Coulomb blockade oscillation characteristic.
3. To improve the reliability of SET-based circuits against background charges (BCs) by using different circuit structures.

It is desirable to design adders and multipliers using hybrid MOS and SET architectures which are able to dramatically reduce the circuit area and power dissipation. While it is straightforward to design these circuits following conventional CMOS design styles, they do not utilize the potential benefits offered by the SET. By using the unique Coulomb blockade oscillation characteristic (i.e., the periodic I-V curve of SET), new functionalities can be effectively achieved with less number of devices through novel design methodologies.

Since BCs (i.e., undesirable fractional charges on the island of SET induced by the defects or impurities located within the oxide barriers) create serious problem for SETbased circuits [6], people working at different abstraction levels (i.e., device level, circuit level, and system level) are trying to find solutions to deal with this effect. As the circuit designers, we need to build robust circuits that are able to work properly with certain tolerance against BCs.

### 1.4 Thesis Organization

This thesis is organized as follows. Chapter 2 introduces the background of singleelectron transistor (SET). It starts with the introduction of the related physics and theory of single-electron-tunneling technology. Then the structure of SET and its unique Coulomb blockade oscillation characteristic are presented to provide the reader a general idea about
how single electrons transport in a SET. This chapter also addresses some important aspects associated with the SET, including simulation techniques, applications, and fabrications. Since Coulomb blockade oscillation is the most important characteristic of SET which is utilized throughout the research work, a variety of simulations using SIMON simulator are introduced at the end of this chapter. The results are used as the basic principles that guide the design of more complex circuits.

Chapter 3 discusses the hybrid MOS and SET architectures. This chapter first introduces a simulation technique used to co-simulate MOSFET and SET, and then analyzes the performance of two typical SET/MOS hybrid architectures - serial SETMOS and parallel SETMOS - in terms of power dissipation, current driveability, and temperature effect. An adaptive feedback structure is also introduced in order to increase the circuit robustness against BCs. A SET/MOS hybrid analog-to-digital converter (ADC) is demonstrated as an example.

Chapter 4 deals with the design of 1-bit binary full adder (FA), and provides three different implementations using modified SET/MOS hybrid architectures based on the schemes of multiple-valued logic (MVL), phase modulation and frequency modulation. The proposed FA fully utilizes the Coulomb blockade oscillation characteristic of SET and hence consumes less number of devices and power. The frequency modulated FA exhibits the high immunity against BCs and can be used to build multi-bit FAs.

Chapter 5 focuses on the design of binary tree multipliers based on multi-input counters (or compressors) implemented using SET/MOS hybrid architectures. The structure of the proposed (3:2) and (7:3) counters is based on the phase modulation scheme presented in Chapter 4. We study the phase modulation scheme in details, and introduce new circuit
structures to deal with some practical issues associated with the SET-based counters, such as temperature, BCs , and the operating seed.

Chapter 6 proposes the SET-based frequency synthesis including frequency gain and frequency mixing, and introduces a novel design methodology for arithmetic operations based on the frequency modulation scheme (similar to the one used in Chapter 4). The main idea is to first convert the operands from digital to frequency representation, then perform arithmetic operations in the frequency domain before converting the result back to the digital representation. The demand for digital-to-frequency and frequency-to-digital conversions is driven by the simplicity of doing frequency multiplication and the high immunity against BCs.

Finally, Chapter 7 concludes this thesis and provides recommendations for future work.

## Chapter 2

## SET Background

### 2.1 Single-Electron Scaling

The manipulation of a single electron was first demonstrated at the beginning of last century, but in solid state circuits it was not implemented until the late 1980s. The necessary nanofabrication techniques have become available during the past three decades, and have made possible a new field of solid state physics, single-electronics [7].

Single-electronics allows us to control the movement and position of a single electron or a small number of electrons. Consider a small conductor (traditionally called an island) to be electrically neutral (i.e., the number of electrons equals to the number of protons). Initially, the island does not generate any electric field which can be easily charged by an electron from the outside. With the net charge on the island of $-e$ (i.e., fundamental charge of an electron, where $e \approx 1.6 \times 10^{-19} \mathrm{C}$ ), the resulting electric field (for the island with the size less than 10 nm ) repulses the following electrons to be added. Although the fundamental charge is small at the human scale of things, the electric field (which is inversely proportional to the square of the island size) is rather strong for nanometerscale structures (as large as $\sim 140 \mathrm{kV} / \mathrm{cm}$ on the surface of a 10 nm sphere in vacuum).

This phenomenon makes it possible to control a single electron in a solid-state structure. More accurately, we have not isolated a single electron since many other electrons are still presented. But we are able to add (or remove) electrons to (or from) the island with single-electron precision [3].

A more adequate measure to quantitatively understand single-electron transfer and related effects is not the electric field, but the charging energy, which is given by

$$
\begin{equation*}
E_{C}=e^{2} / 2 C \tag{2.1}
\end{equation*}
$$

where $C$ is the capacitance of the island. Since thermal fluctuations will disturb the motion of electrons, the minimum charging energy to control an electron is

$$
\begin{equation*}
E_{C}>k_{B} T \tag{2.2}
\end{equation*}
$$

where $k_{B}$ is Boltzmann's constant (i.e., $k_{B} \approx 1.38 \times 10^{-23} \mathrm{~J} / \mathrm{K}$ ) and $T$ is the absolute temperature. This means that the capacitance $C$ has to be smaller than 12 aF for the observation of charging effects at the temperature of liquid nitrogen ( 77 K ) and smaller than 3 aF for charging effects to appear at room temperature (300K). This requires the island size to be smaller than 15 nm and 5 nm , respectively. To use charging effects for the deterministic logic, most suggested single-electron devices (SEDs) require even higher values of $E_{C}$ (factor about 50) in order to avoid thermally-induced random tunneling events. As a result, for room temperature operation, the minimum feature size of the island has to be smaller than 1 nm [8].

In this size range, the electron kinetic energy (i.e., $E_{k}$ ) becomes substantial. It is very important to develop SEDs capable of working in this size range with $E_{C} \gg E_{k}$, thus avoiding complications stemming from the energy quantization effects.

### 2.2 Orthodox Theory

Orthodox theory [9] of single-electron tunneling provides the unique guiding role in single-electronics. The theory is developed with the following assumptions:

1) The electron energy spectrum within the island is continuous (i.e. the electron energy quantization is ignored). Strictly speaking this assumption is valid only if $E_{k} \ll k_{B} T$, but it frequently gives an adequate description of observations as soon as $E_{k} \ll E_{C}$. It should be mentioned that the electron transfer is discrete, but the electron energy is continuous. Since we are ignoring any quantization of electron energy in the island, SEDs cannot be included in the group of "quantum electronic devices" [10].
2) The time taken by an electron tunneling through the barrier (i.e., $\tau_{t}$ ) is assumed to be negligibly small in comparison with other time scales (including the interval between neighboring tunneling events). This assumption is valid for tunnel barriers used in SEDs of practical interest, where $\tau_{t} \sim 10^{-15}$ seconds.
3) Coherent quantum processes consisting of several simultaneous tunneling events (i.e., co-tunneling) are ignored. This assumption is valid only when the electrons are well localized in the island [11]. This leads to the requirement that the resistance (i.e., $R_{T}$ ) of all tunnel barriers in the system has to be large enough in order to effectively suppress the quantum-mechanical uncertainty of the electron location. According to Heisenberg's energy uncertainty principle, the minimum resistance of a tunnel barrier is given by

$$
\begin{equation*}
R_{T}>h / e^{2} \approx 26 K \Omega \tag{2.3}
\end{equation*}
$$

where $h$ is Planck's constant (i.e., $h \approx 6.63 \times 10^{-34} \mathrm{~J} \cdot \mathrm{~s}$ ). Notice that this relationship is of principal importance for SEDs as a whole which makes it possible to control a single electron.

With above assumptions to be satisfied, the Orthodox theory is in quantitative agreement with virtually all the experimental data for systems with metallic conductors and gives a qualitative description of most results for most semiconductor structures.

The main result of Orthodox theory can be concluded as follows [3]: the tunneling of a single electron through a particular tunnel barrier is always a random event with a certain rate which depends solely on the reduction of the free energy of the system as a result of this tunneling event.

### 2.3 SET Structure

The basic element of a SET [4] is the tunnel junction. If we consider a piece of conductor separated by an ultrathin dielectric, the overall structure will behavior as a tunnel junction, as shown in Figure 2.1 (a). Such arrangement of two conductors with an insulating layer in between not only has a huge resistance (up to $\mathrm{M} \Omega$ ), but also a finite capacitance (i.e., at the range of aF ). According to the laws of classical electromagnetism, no current can flow through an insulating barrier; however, from the viewpoint of quantum mechanics, there is a non-vanishing probability for electrons to pass through it as long as the barrier is thin enough [12]. Most SEDs can be constructed by placing such tunnel junctions in series, such as single-electron box [13], single-electron pump [14], single-electron trap [15], single-electron turnstile [16], and so on, where the transport of electrons through the tunnel junction is discrete strictly one after another.


Figure 2.1: (a) Structure of a tunnel junction; (b) Structure of a single-electron transistor (SET) where the left one is the one-gate SET and the right one is the two-gate SET. (Reproduced with permission from [32]).

With two tunnel junctions that share a common electrode, known as the island, one can build a SET, as shown in Figure 2.1 (b), where the gate terminal is capacitively coupled to the island via a thin dielectric (the left one is the one-gate SET while the right one is the two-gate SET).

If the source terminal of a SET is connected to the ground, and the drain and gate terminals are biased to the external voltage sources of $V_{D S}, V_{G S 1}$, and $V_{G S 2}$, respectively (for a two-gate SET), the potential on the island of SET can be expressed as:

$$
\begin{equation*}
V_{\text {Isand }}=\frac{C_{G 1}}{C_{\Sigma}} V_{G S 1}+\frac{C_{G 2}}{C_{\Sigma}} V_{G S 2}+\frac{C_{T D}}{C_{\Sigma}} V_{D S}-\frac{k \cdot e}{C_{\Sigma}} \tag{2.4}
\end{equation*}
$$

where $k$ is the net number of electrons on the island, $C_{\Sigma}$ is the total device capacitance of SET (i.e., $C_{\Sigma}=C_{G 1}+C_{G 2}+C_{T D}+C_{T S}$ ). It is $V_{\text {Island }}$ that determines the voltage across the two tunnel junctions and hence controls the electron transport.

According to the Orthodox theory, the electron tunneling event from a microscopic point of view is a stochastic process; however, from a macroscopic perspective, the current flowing through a SET is a deterministic behavior which depends on different external voltage or current biasing conditions.

### 2.4 Coulomb Blockade Oscillation

For constant voltage or current biased SET, its drain-to-source current or voltage exhibits an oscillating characteristic with respect to the input gate voltage. This phenomenon is known as Coulomb blockade oscillation [11], which is the most important property of the SET.

For the Coulomb blockade oscillation to occur, Orthodox theory must be satisfied. Other than this, SET's drain-to-source voltage (i.e., $V_{D S}$ ) cannot exceed $e / C_{\Sigma}$. With $e / C_{\Sigma}<$ $V_{D S}<3 e / 2 C_{\Sigma}$, Coulomb blockade region no longer exists but Coulomb oscillation remains. If $V_{D S}$ is further increased, Coulomb oscillation will vanish out and SET functions as a regular resistor.

To understand how electrons transprot in a SET, assume that initially the charge on the island is $Q$, then the electrostatic energy of the system (i.e., $E_{l}$ ) can be expressed as

$$
\begin{equation*}
E_{1}=\frac{Q^{2}}{2 C_{\Sigma}} \tag{2.5}
\end{equation*}
$$

Now if an electron tunnels from the source to the island, the total electrostatic energy of the system will become

$$
\begin{equation*}
E_{2}=\frac{(Q-e)^{2}}{2 C_{\Sigma}} \tag{2.6}
\end{equation*}
$$

According to the Orthodox theory, an electron tunneling event can only take place if it decreases the total energy of the system. That is

$$
\begin{equation*}
E_{1}-E_{2}=\frac{2 Q \cdot e-e^{2}}{2 C_{\Sigma}}>0 \Rightarrow Q>\frac{e}{2} \tag{2.7}
\end{equation*}
$$

Since $Q=C_{\Sigma} \cdot|V|$, where $|V|$ is the voltage drop across the tunnel junction, we can conclude that the electron tunneling event is possible only when

$$
\begin{equation*}
|V|>\frac{e}{2 C_{\Sigma}} \tag{2.8}
\end{equation*}
$$

Notice that at higher temperature, electron may tunnel through the junction even though $|V|$ is less than $e / 2 C_{\Sigma}$ due to the thermal energy effect. Assume that SET works at near absolute temperature (i.e., the thermal energy effect is negligible), then the electron tunneling event in a SET can only happen if $\left|V_{\text {Island }}\right|>e / 2 C_{\Sigma}$ (i.e., electron tunnels from the source terminal to the island) or $\left|V_{D S}-V_{\text {Island }}\right|>e / 2 C_{\Sigma}$ (i.e., electron tunnels from the island to the drain terminal).

To simplify the explanation, we set $V_{D S}$ equal to $e / 2 C_{\Sigma}$ and increase the gate votlage (i.e., $V_{G S}$ ) from 0 to a considerable positive value. Since $V_{I s l a n d}$ is determined by the external biasing voltages (refer to (2.4)), $V_{\text {Island }}$ will increase along with $V_{G S}$. Then from Figure 2.2 (where $\alpha=e / 2 C_{\Sigma}$ ), we can observe that:

1) When $V_{\text {Island }}<\alpha$, the voltage drop across both source and drain tunnel juctions is less than $\alpha$, hence there is no electron tunneling event happened and SET is in Coulomb blockade region - see Figure 2.2 (a).
2) If we increase $V_{G S}$ so that $V_{\text {Island }}$ is greater than $\alpha$ - see Figure 2.2 (b), one electron will tunnel from the source terminal to the island. Once an electron enters into the island, the $V_{\text {Island }}$ is dropped by $2 \alpha$ (from point A to point B). As a result, the voltage drop across the drain terminal is greater than $\alpha$, and then one electron tunnels from the island to the drain terminal. Right after the electron leaves the island, the $V_{\text {Island }}$ returns back to its original value (from point B to point C ) which induces another electron. In this way, a continuous current path is estabilished between the source and drain terminals.
3) With the further increase of $V_{G S}, V_{\text {Island }}$ is greater than $2 \alpha$ - see Figure 2.2 (c), where the voltage drop across both source and drain terminals is greater than $\alpha$.

However, since $\left|V_{\text {Island }}-V_{\text {source }}\right|>\left|V_{\text {drain }}-V_{\text {Island }}\right|$, from the probability point of view, electrons have more chance to tunnel from the source terminal to the island than from the island to the drain terminal. As a result, the net number of electrons on the island will be increased by one, and the $V_{\text {Island }}$ will be reduced by $2 \alpha$ (from point A to point B). Like Figure 2.2 (a), the SET again enters into the Coulomb blockade region.
4) When $V_{\text {Island }}>3 \alpha$ - see Figure $2.2(\mathrm{~d}), V_{\text {Island }}$ is first dropped by $2 \alpha$ (from point A to point B) with one more electron residuing on the island. Then similar to Figure 2.2 (b), electrons keep tunneling from the source terminal to the drain terminal which create a continuous current path.

From above observation, we can infer that the periodicity of electron tunneling current (i.e., $I_{T}$ ) is $2 \alpha$ (i.e., $e / C_{\Sigma}$ ) with respect to $V_{\text {Island }}$. By differentiating (2.4) (assume there is only one gate for SET, and $V_{D S}$ and $k$ are constant), we can get that

$$
\begin{equation*}
\Delta V_{\text {Island }}=\frac{C_{G}}{C_{\Sigma}} \cdot \Delta V_{G S} \tag{2.9}
\end{equation*}
$$

As a result, the periodicity of $I_{T}$ with respect to $V_{G S}$ is $e / C_{G}$.
For the current biased SET, the $V_{D S}$ will oscillate with the same periodicity as the $I_{T}$. The amplitude of $V_{D S}$ oscillation at near absolute temperature is $e / C_{\Sigma}$ with the positive and negative slopes of $C_{G} /\left(C_{\Sigma}-C_{T D}\right)$ and $-C_{G} / C_{T D}$, respectively. While these values will attenuate at higher temperature, they can be used as the good estimations to predict SET's performance.


Figure 2.2: Electron tunneling mechanisms in the SET. (Reproduced with permission from [32]).

### 2.5 Simulation Techniques

There are mainly three approaches used to simulate SET-based circuits:

1) Monte Carlo (MC) simulation technique: MC technique [17] is the most popular approach used to simulate SED-based circuits (including SET which is special type of SED). MC approach starts with all possible tunneling events, calculates their probabilities, and chooses one of the possible events randomly using the probabilities for weighting. This is done many times to simulate the transport of electrons through the network.
2) Master Equation (ME) simulation technique: ME technique is a description for the underlying Markov process [18] of electron tunneling from island to island, and thus the circuit occupies different states. With ME method, one needs the set of all possible states of the circuit, which are defined by the external voltage sources and the charge distribution in the circuit.
3) SPICE macro modeling technique: This method models SET's behaviour using equivalent circuits based on conventional microelectronic components [19, 20], such as voltage and current sources, diodes, and resistors. Although this approach is compatible with SPICE environment, the purely empirical nature makes them not convenient for the SET-based circuit design.

MC technique is considered to be the most accurate way to find the characteristics of not only SETs, but any SEDs. Some of the well-known MC simulators are SIMON [21], MOSES [22], KOSEC [23], and SENECA [24]. At the end this chapter, we will simulate a constant current biased SET using SIMON simulator so as to examine different parameter effects on the Coulomb blockade oscillation.

### 2.6 Background Charge Effect

One of the biggest disadvantages of single-electron-tunneling technology is its large charge sensitivity. This is good for sensors which can be used to build super sensitive electrometers. However, for logic applications which work at particular voltage or current biasing conditions, any trapped charge or the charge movement near the island could easily change the circuit operating point, and hence produces an error [25]. These undesirable charges are referred as BCs which are mainly induced by defects or impurities located within the oxide barriers, and cannot be entirely removed by today's technology. It has been measured that BCs on the island of SET vary over a period from a few minutes to hours, and the variation generally follows Gaussian distribution with the high probability of being less than $\pm 0.3 e[6,26]$.

Researchers are trying to find solutions dealing with this problem at different levels:

1) Device level: physicists and chemists are looking for different structures and materials to fabricate SET with as less BCs as possible.
2) Circuit level: circuit designers try to build robust circuits that are able to tolerant certain amount of BCs. Notice that BCs only shift the phase of Coulomb blockade oscillation without changing the amplitude and periodicity, SET-based circuits will exhibit high immunity against BCs if the information is encoded into the amplitude or frequency.
3) System level: people at this level try to add certain redundancy into the logic to tolerant BCs, such as using neural network.

This thesis deals with BCs at the circuit level by using novel circuit configurations and different design methodologies.

### 2.7 Applications

Memory design is the most attractive application of SET due to the fact that one can achieve extraordinary storage density at an extremely low power consumption by using SETs. Also, for SET-based memories, several known solutions exist to the effect of BCs [27]. Many research groups have reported different memory architectures based on SETs [28, 29], and a 128 MB prototype for giga-scale SET memory has already been implemented on the silicon wafer [30].

In terms of logic applications, SET is very suitable for the multiple-valued logic (MVL) design [31]. Because of the Coulomb blockade oscillation characteristic, SET has multiple threshold voltages (this is in contrast to MOSFET which has single threshold voltage) which can be directly linked to the MVL operations. MVL functions can be therefore realized by using SETs with a significant reduction of the number of devices.

### 2.8 Intrinsic Drawbacks

Despite limitations of low temperature operation and the background charge effect, SET suffers from low current drivability and small voltage gain. As mentioned before, to sustain Coulomb oscillation, the drain-to-source voltage of SET cannot exceed $3 e / 2 C_{\Sigma}$. This results in the biasing current of SET at the range of nA which cannot drive large capacitive load (say 100 aF ) at relatively high speed. Also, given the slopes of Coulomb oscillation (i.e., $C_{G} /\left(C_{\Sigma}-C_{T D}\right)$ and $-C_{G} / C_{T D}$, respectively), the voltage gain of SET is normally around (or less than) one. Since MOSFETs have advantages that can compensate these intrinsic drawbacks of SET, hybrid MOS and SET architecture is considered to be a more practical implementation for the nanometer-scale circuit design.

Although a complete replacement of MOSFET by SET is unlikely in the near future, it is true that by combining MOSFET and SET, we can bring out a lot of new functionalities which cannot be mirrored in pure CMOS technology [32].

### 2.9 Fabrications

Historically, the research on SET fabrications started with metals and superconductors [33-35] and then expanded to semiconductors [36]. The reason of using silicon as a base material for SET fabrication is that we can take advantage of the existing CMOS fabrication technologies. To fabricate SETs on the silicon wafer faces the following challenges:

1) Island dimension: the island diameter has to be on the order of $2 \sim 3 \mathrm{~nm}$ for subambient temperature operation (i.e., $-150{ }^{\circ} \mathrm{C} \sim-50{ }^{\circ} \mathrm{C}$ ), and $\sim 1 \mathrm{~nm}$ for room temperature. It is very difficult for today's lithography to isolate a tiny piece of material with a size of a few nanometers. An alternative to lithography techniques is needed for fabricating silicon SETs.
2) Batch processing: reproducibility in SET fabrication is very important. A costeffective SET fabrication technology should be the one that can be used for batch processing (like CMOS).
3) Background charge effect: since BCs create serious problem for the proper operation of SET [26], all the processing steps and materials used should be very clean in order to avoid charge trapping.
4) Energy quantization effect: quantization effect creates another problem for the practical operation of SET which introduces some unpredictable irregularities to the

Coulomb blockade oscillation. Among possible approaches to avoid such complex features might be the use of highly doped silicon nano-wires or the use of charge injection in silicon nano-crystals deposited on SETs [37].
5) Control of tunnel junction resistance: it is difficult to fabricate the tunnel junction with the resistance as small as possible which is still larger than $26 \mathrm{~K} \Omega$ for proper quantum confinement.

Despite so many difficulties, various SET fabrication techniques have been reported. Pattern Dependent Oxidation (PADOX) technique [38] appears to be a very reliable technology for fabricating SETs which is first introduced by NTT Research Laboratories. The process is based on the thermal oxidation of a short silicon wire which is connected to the wide silicon layers. The initial silicon wire is defined in a very thin silicon-on-insulator (SOI) layer by electron beam lithography and dry etching, and then it is thermally oxidized in dry oxygen ambient. A polysilicon gate deposition over the silicon wire defines the final SET structure. An equivalent island with 7 nm diameter is effectively formed in the silicon wire whose $C_{\Sigma}=1.5 \mathrm{aF}$. Such small dimensions which are below the lithographic limit are possible because the size of the remaining silicon is reduced as oxidation proceeds.

Providing islands with sub-lithographic controlled dimensions is one of the advantages of thermal oxidation. Another important feature of PADOX is that the gate capacitance (i.e., $C_{G}$ ) of the silicon island shows an almost linear relationship to the designed length of the silicon wire which makes the reproducible silicon SET fabrication possible.

Other SET fabrication techniques are listed as follows:
$\checkmark$ Lithographic point contact [37]: this SET architecture uses the point contact of two triangular-shaped MOSFETs which are fabricated on SOI wafer using electron beam lithography and an anisotropic etching technique. The width of the point contact channel is less than 30 nm . Although the tunnel barriers and silicon dots are not intentionally formed, they are naturally introduced in the channel. Some devices are found to operate as SETs even at room temperature.
$\checkmark$ Scanning Tunneling Microscope (STM) nano-oxidation [39]: a layer of 3 nm thick titanium is deposited by evaporation on the thermally oxidized $\mathrm{SiO}_{2} n$ - Si substrate. The Ti surface is oxidized by anodization using the STM tip as a cathode through the water that adhered to the surface of the Ti from the atmosphere, and oxidized titanium lines of nanometer size are formed which are used for the formation of the small island of SET.
$\checkmark$ Focused Ion Beam (FIB) prototyping [40]: this is based on two steps, the first one consists of preparing a relatively large and long SOI wire connected between two silicon pads on SOI with a thickness of around 30 nm , and the second one is the FIB treatment which reduces the channel width to a dimension as small as 50 nm . The silicon wire is further oxidized to decrease its size from 30 nm to around 15 nm in diameter, and to grow an all-around gate oxide.
$\checkmark$ Sidewall patterning method [41]: this is based on SOI nano-wire processing combined with an electrostatically defined island where the tunnel barrier are electrically formed by the sidewall depletion gates. This fabrication process is interesting because the tunnel barrier and the size of the island are controlled in a simple yet smart way, beyond the lithographic limits.

Recent alternatives to silicon SETs are based on carbon nano tubes (CNTs) [42] and some molecular materials [43, 44]. These new nano materials have the potential to be cointegrated in or above the silicon CMOS devices. CNTs have also been suggested as the possible candidates for room-temperate operated SETs [45].

### 2.10 Case Study: SIMON Simulations

Since Coulomb blockade oscillation is the unique characteristic of SET which can be utilized to effectively achieve a lot of functionalities with less number of devices through novel design methodologies, we first of all study this characteristic in detail, and examine different parameter effects on this characteristic using the SIMON simulator. The results can be used as the basic principles to guide the design of more complex circuits.

The circuit simulated in the SIMON simulator is shown in Figure 2.3 which is a constant current biased one-gate SET with a loading capacitor. The parameters used for the simulations are as follows: $R_{T D}=R_{T S}=1 \mathrm{M} \Omega, C_{T D}=C_{T S}=1 \mathrm{aF}$ (SET's source and drain junction resistance and capacitance), $C_{G}=2 \mathrm{aF}$ (SET's gate capacitance), $I_{\text {Bias }}=2 \mathrm{nA}$ (biasing current), $C_{\text {Load }}=100 \mathrm{aF}$ (loading capacitance), $T=1 \mathrm{~K}$ (operating temperature), and $\mathrm{BC}=0$ (background charge on the island of SET).

If increasing $V_{G S}$ from 0 to 80 mV , we will get a voltage oscillation at $V_{D S}$. By changing the following parameters one at a time, we can observe that:

1) Effect of loading capacitance: with $C_{\text {Load }}=1 \mathrm{aF}, 10 \mathrm{aF}, 100 \mathrm{aF}$, and 1 fF , respectively, we get four $V_{D S}$ oscillations, as shown in Figure 2.4. It is observed that when $C_{L o a d}$ is small (i.e., less than 10 aF ), it will have an effect on the $V_{D S}$ oscillation. The $V_{D S}$ oscillation with $C_{\text {Load }}$ greater than 100 aF reflects the real SET characteristic. This
indicates that when we build large SET-based circuits, interconnected SETs will affect each other. In order to prevent this effect, a large grounded capacitor (with the capacitance more than 100 aF ) needs to be added to the node of interconnected SETs.
2) Effect of biasing current: with $I_{\text {Bias }}$ increasing from 2 nA to 11 nA in the step of 3 nA , we get four $V_{D S}$ oscillations, as shown in Figure 2.5. It is observed that as $I_{\text {Bias }}$ increases, the level of $V_{D S}$ (i.e., the averaging $V_{D S}$ ) increases but the amplitude of $V_{D S}$ decreases. In order to sustain Coulomb oscillation, $I_{\text {Bias }}$ for this configuration cannot exceed 10 nA . With further reduced junction resistance and device capacitance, $I_{\text {Bias }}$ can be as high as a few hundred nA.
3) Effect of total device capacitance (i.e., $\boldsymbol{C}_{\Sigma}$ ): with $C_{T D}=C_{T S}=1 \mathrm{aF}, 1.5 \mathrm{aF}$, and 2 aF (i.e., $C_{\Sigma}=3 \mathrm{aF}, 4 \mathrm{aF}$, and 5 aF ), respectively, we get three $V_{D S}$ oscillations, as shown in Figure 2.6. It is observed that as $C_{\Sigma}$ increases, the amplitude of $V_{D S}$ oscillation decreases (i.e., the maximum $V_{D S}$ decreases but the minimum $V_{D S}$ remains constant). The amplitude of $V_{D S}$ oscillation is inversely proportional to $C_{\Sigma}$ which can be expressed as $e / C_{\Sigma}$ at near absolute temperature.
4) Effect of input gate capacitance: with $C_{G}=1 \mathrm{aF}, 2 \mathrm{aF}$, and 3 aF , respectively, we get three $V_{D S}$ oscillations, as shown in Figure 2.7, where we set $C_{T D}=C_{T S}=1.5 \mathrm{aF}, 1 \mathrm{aF}$, and 0.5 aF (corresponding to the $C_{G}$ of $1 \mathrm{aF}, 2 \mathrm{aF}$, and 3 aF , respectively) so as to maintain the same $C_{\Sigma}=4 \mathrm{aF}$ (this ensures the same amplitude of $V_{D S}$ oscillation for better comparison) and increase $V_{G S}$ from 0 to 160 mV . It is observed that as $C_{G}$ increases, the periodicity of $V_{D S}$ oscillation decreases. The periodicity of $V_{D S}$ oscillation is inversely proportional to $C_{G}$ which can be expressed as $e / C_{G}$.
5) Effect of temperature: with operating temperature increasing from 1 K to 21 K in the step of 10 K , we get three $V_{D S}$ oscillations, as shown in Figure 2.8. It is observed that as the temperature increases, the amplitude of $V_{D S}$ decreases (i.e., the maximum $V_{D S}$ decreases but the minimum $V_{D S}$ remains constant). In order to sustain Coulomb oscillation, the operating temperature for this configuration has to be less than 100 K . With further reduced device capacitance (i.e., $C_{\Sigma}<3 \mathrm{aF}$ ), SET is able to work at room temperature.
6) Effect of BCs: with BCs on the island of SET being $-0.1 e, 0$, and $0.1 e$, respectively, we get three $V_{D S}$ oscillations, as shown in Figure 2.9. It is observed that BCs only shift the phase of $V_{D S}$ oscillation without changing its amplitude and periodicity. Positive BCs shift $V_{D S}$ oscillation to the right while negative BCs move $V_{D S}$ oscillation to the left. Only fractional BCs will change the phase of $V_{D S}$ oscillation. This observation indicates that the SET-based circuits will exhibit high immunity against BCs if the information is encoded into the amplitude or periodicity of this oscillation.
7) Effect of second gate voltage: in order to examine this effect, we add one more gate for SET with the gate capacitance of 1 aF . With the voltage applied on the second gate of SET (i.e., $V_{G S 2}$ ) being $-100 \mathrm{mV}, 0$, and 100 mV , respectively, we get three $V_{D S}$ oscillations, as shown in Figure 2.10. It is observed that the effect of $V_{G S 2}$ is the same as the effect of BCs (i.e., only shift the phase of $V_{D S}$ oscillation without changing its amplitude and periodicity). Positive $V_{G S 2}$ shifts $V_{D S}$ oscillation to the left while negative $V_{G S 2}$ moves $V_{D S}$ oscillation to the right. This observation implies that one is able to offset the effect of BCs by applying appropriate voltage through an additional gate of SET.


Figure 2.3: Constant current biased SET in SIMON simulator environment.


Figure 2.4: Effect of $C_{\text {Load }}$ on $V_{D S}$ oscillation, where $C_{\text {Load }}=1 \mathrm{aF}, 10 \mathrm{aF}, 100 \mathrm{aF}$, and 1 fF .


Figure 2.5: $\quad$ Effect of $I_{\text {Bias }}$ on $V_{D S}$ oscillation, where $I_{\text {Bias }}=2 \mathrm{nA}, 5 \mathrm{nA}, 8 \mathrm{nA}$, and 11 nA .


Figure 2.6: Effect of $C_{\Sigma}$ on $V_{D S}$ oscillation, where $C_{\Sigma}=3 \mathrm{aF}, 4 \mathrm{aF}$, and 5 aF .


Figure 2.7: $\quad$ Effect of $C_{G}$ on $V_{D S}$ oscillation, where $C_{G}=1 \mathrm{aF}, 2 \mathrm{aF}$, and 3aF.


Figure 2.8: $\quad$ Effect of temperature on $V_{D S}$ oscillation, where $T=1 \mathrm{~K}, 11 \mathrm{~K}$, and 21 K .


Figure 2.9: $\quad$ Effect of BCs on $V_{D S}$ oscillation, where $\mathrm{BC}=-0.1 e, 0$, and $0.1 e$.


Figure 2.10: Effect of $V_{G S 2}$ on $V_{D S}$ oscillation, where $V_{G S 2}=-100 \mathrm{mV}, 0$, and 100 mV .

## Chapter 3

## SET/MOS Hybrid Architectures

### 3.1 Introduction

SET is considered to be a promising candidate for further VLSI design because of its nanometer-scale feature size, ultra-low power dissipation, and unique Coulomb blockade oscillation characteristic. Unfortunately, circuits with pure SETs have very limited applications due to the low current drivability, small voltage gain and low temperature operation. Study shows that MOSFET and SET are rather complementary. Since MOSFET has advantages such as high-speed driving and high voltage gain that can compensate for the intrinsic drawbacks of SET, hybrid MOS and SET architectures, which combine the merits of both MOSFET and SET, promise to be a more practical implementation for nanometer-scale circuit design [32]. With hybrid circuits, a lot of new functionalities can be achieved with less number of devices which cannot be mirrored in pure CMOS technology.

In this chapter, we first introduce the MIB compact mode which can be used to cosimulate MOSFET and SET. Then we simulate and compare two typical SET/MOS hybrid architectures - serial and parallel - in terms of power dissipation, current
drivability and the temperature effect. Since BCs create serious problem on the circuit performance, we propose an adaptive feedback structure which dramatically increases the robustness of hybrid circuits against BCs. An improved SET/MOS hybrid analog-todigital converter (ADC) is also presented as an example which takes advantage of the proposed feedback structure.

### 3.2 Hybrid MOS and SET Co-Simulation

MC technique is considered to be the most accurate method to simulate SED-based circuits (including SET) which is based on probability calculation. However, this method takes very long time if the circuit becomes large and cannot be used to co-simulate with MOSFETs. For example, each simulation conducted at the end of Chapter 2 using SIMON simulator takes more than three minutes (based on a general personal computer), and there are only components of tunnel junctions, resistors, capacitors, and voltage and current sources that can be used to build large circuits.

MIB (named after three authors [46]) compact model of SET achieves very fast simulation speed. The model is developed using ME technique and has been verified with perfect match to the MC result. The Verilog-A version of this model can be easily integrated into a conventional SPICE simulator through the Verilog-A interface [47].

MIB model is founded on the following assumptions:

1) It obeys Orthodox theory of single-electron tunneling;
2) The interconnect capacitances associated with gate, source, and drain terminals are much larger than the device capacitances (i.e., $C_{T D}, C_{T S}, C_{G}$, or $C_{G 2}$ ), which ensures that the total device capacitance with respect to ground (i.e., $C_{\Sigma}$ ) equals to the summation of all device capacitances.

Remember the simulation conducted at the end of Chapter 2 where the small loading capacitance has an effect on the actual SET characteristic. In fact, in a circuit where many SETs are connected to each other, $C_{\Sigma}$ of any SET not only depends on its own device capacitances but also on the parameters of other SETs. This difficulty can be solved if the second assumption holds true. For hybrid MOS and SET circuits, because the interconnect capacitance between MOSFET and SET (via connection lead) is much larger than SET's device capacitances (a few aF at most), the second assumption appears to be very practical.

MIB compact model not only integrates device capacitances and resistances but also temperature and BCs as the model parameters which is very attractive for hybrid MOS and SET co-simulation [48].

In the following of the thesis, we use MIB compact model for SETs along with BSIM3v3 (for CMOS 180nm technology) and BSIM4 (for CMOS 65 nm technology) Spector models for MOSFETs. The hybrid MOS and SET co-simulations are conducted using conventional Spector simulator in Cadence analog environment.

### 3.3 Serial and Parallel SETMOS

There are two widely used hybrid MOS and SET architectures, one is SET and MOSFET connected in serial biased by one current source, and the other is SET and MOSFET connected in parallel biased by two current sources, as shown in Figure 3.1. In the remainder of the thesis, they are called serial SETMOS and parallel SETMOS, respectively.


Figure 3.1: (a) Serial SETMOS; (b) Parallel SETMOS.

The serial SETMOS structure is first proposed by Inokawa et al. [31] and has been used as the basic building block to construct many functional circuits, such as static random-access memory (SRAM) [31], analog-to-digital converter (ADC) [31, 49], random-number generator (RNG) [50], voltage-controlled oscillator (VCO) [51], and so on. The parallel SETMOS structure is first introduced by Mahapatra et al. [46-48] which increase the current drivability at the cost of increased power consumption.

In both structures, NMOS transistor is biased in the sub-threshold region in order to achieve a high voltage gain. This is done by changing the gate voltage of NMOS transistor in the serial SETMOS and the source voltage of NMOS transistor in the parallel SETMOS, respectively. $V_{P C}\left({ }^{〔}{ }_{P C}\right.$ ' stands for phase control) is used to adjust the phase of voltage oscillation at SET's drain terminal (i.e., $V_{D S \mid S E T)}$ as a result of increasing the input gate voltage (i.e., $V_{I N}$ ). Due to the constant biasing current for NMOS transistor in both structures, $V_{D S \mid S E T}$ oscillation is then transferred with amplified amplitude to the output node (i.e., $V_{\text {OUT }}$ ).

We then simulate the two structures and compare their performance in terms of power dissipation, current drivability, and temperature effect. The following device parameters are used for the simulations: for all SETs, $C_{T D}=C_{T S}=0.1 \mathrm{aF}, C_{G 1}=C_{G 2}=0.13 \mathrm{aF}, R_{T D}=$ $R_{T S}=1 \mathrm{M} \Omega$; for the NMOS transistors, $W=500 \mathrm{~nm}$ and $L=180 \mathrm{~nm}$. To sustain Coulomb blockade oscillation, the constant current source connected with the SET in Figure 3.1 need to be chosen properly - normally set as several tens of nA. The values of all current and voltage sources used in Figure 3.1 are summarized in Table 3.1.

Figure 3.2 shows the simulation results for both serial and parallel SETMOSs at room temperature. It can be seen that the amplitude and periodicity of $V_{D S \mid S E T}$ oscillation with respect to $V_{I N}$ are about 200 mV and 1.24 V , respectively. The output voltages of both serial and parallel SETMOSs oscillate with amplitude of 1.6 V and the same periodicity as $V_{D S \mid S E T}$. Notice that the output voltage polarity for serial SETMOS is the same as $V_{D S \mid S E T}$ while for parallel SETMOS it is inversed.

TABLE 3.1 PARAMETERS OF SERIAL AND PARALLEL SETMOSS

| Serial SETMOS | $I_{D C}$ | 40 nA |
| :---: | :---: | :---: |
|  | $V_{G G}$ | 655 mV |
|  | $V_{P C}$ | 330 mV |
| Parallel | $I_{D C 1}$ | 40 nA |
|  | $I_{D C 2}$ | $1 \mu \mathrm{~A}$ |
|  | $V_{S S}$ | -283 mV |
|  | $V_{P C}$ | 330 mV |



Figure 3.2: $\quad V_{D S S E T}$ and output voltage oscillations where $V_{O U T I}$ is the output of serial SETMOS and $V_{\text {OUT2 }}$ is the output of parallel SETMOS.

### 3.3.1 Power Dissipation

It is known that the power dissipation of MOSFETs is dominated by dynamic power during the logic transition region where there is a current from $V_{D D}$ to ground. However, the power dissipation of SETs is mostly consumed by static power at non-transition regions (i.e., the output is logic ' 0 ' or ' 1 ') [52]. This is because for constant current biased SET, electrons keep tunneling into and out of the island which produce the continuous current path. To calculate the total power dissipation of serial and parallel SETMOS in Figure 3.1, we use an ideal clock signal as the input with voltage levels of 0 and 450 mV (as a result, according to Figure 3.2, the serial SETMOS functions as an inverter while the parallel SETMOS acts as a buffer) and the period of $2 \mu \mathrm{~s}$, and then run transient analysis at room temperature.

Simulation results are shown in Figure 3.3. It is found that the serial SETMOS has ultra-low power dissipation of 35.1 nW due to the small biasing current of $I_{D C}$ which is 40nA. For the parallel SETMOS, however, the total power dissipation turns out to be as high as 676.5 nw which is dominated by the power of NMOS transistor $(665.5 \mathrm{nW})$.

### 3.3.2 Current Drivability

The driving drivability of both serial and parallel SETMOS can be tested by adding a loading capacitance at output node. Figure 3.4 shows output voltages (based on the same input used in Figure 3.3) with different loading capacitances for both serial and parallel SETMOSs. It is observed that the serial SETMOS can only drive a capacitive load of several fF ; however, the parallel SETMOS is able to drive up to several hundreds of fFs due to large biasing current of $I_{D C 2}$ which is $1 \mu \mathrm{~A}$.


Figure 3.3: Transient analysis of serial and parallel SETMOSs where $V_{I N}, V_{D S S E T}, V_{\text {OUTI }}$, and $V_{\text {OUT2 }}$ are defined in Figure 3.2.


Figure 3.4: Loading effect on the output of serial SETMOS (a) and parallel SETMOS (b).

### 3.3.3 Temperature Effect

Pure SET-based circuits can only work at extremely low temperature (usually less than 100 K ). At higher temperature, the amplitude of Coulomb Blockade oscillation will be reduced. One of the most important advantages of hybrid MOS and SET architectures is that they can work at much higher temperature [53]. Due to the fact that MOSFET has a large voltage gain which can amplify the tiny output voltage swing of SET to an acceptable level. Serial and parallel SETMOSs are able to work at room temperature; however, they are still very sensitive to the temperature variation. Figure 3.5 shows output voltages (based on the same input used in Figure 3.3) at different temperature (from $10^{\circ} \mathrm{C}$ to $30^{\circ} \mathrm{C}$ with increment of $5^{\circ} \mathrm{C}$ ).


Figure 3.5: $\quad$ Temperature effect on the output of serial SETMOS (a) and parallel SETMOS (b).

Some experimental data with different temperatures are shown in Table 3.2, indicating that as the temperature decreases, the threshold voltage $\left(V_{T H}\right)$ of NMOS transistor increases while the amplitude of $V_{D S}$ oscillation decreases (i.e., the peak value of $V_{D S \mid S E T}$ decreases, but the valley value of $V_{D S \mid S E T}$ remains almost the same). In other words, the voltage gain of NMOS transistor has a positive temperature coefficient, while the amplitude of $V_{D S}$ oscillation of SET exhibits a negative one. Therefore, by utilizing the opposite temperature responses of SET and NMOS transistor, both serial and parallel SETMOSs could be less temperature-dependent.

TABLE 3.2 TEMPERATURE EFFECT ON SET AND MOSFET DEVICES

| Temperature | $V_{T H}(\mathrm{mV})$ of <br> NMOS transistor | Peak voltage (mV) <br> of $V_{D S} \mid S E T$ | Valley voltage (mV) <br> of $V_{D S \mid S E}$ |
| :---: | :---: | :---: | :---: |
| $100^{\circ} \mathrm{C}$ | 497.2 | 312.7 | 160.1 |
| $80^{\circ} \mathrm{C}$ | 509.8 | 320.1 | 160.1 |
| $60{ }^{\circ} \mathrm{C}$ | 522.3 | 327.3 | 160.1 |
| $40^{\circ} \mathrm{C}$ | 534.8 | 334.3 | 160.1 |
| $20{ }^{\circ} \mathrm{C}$ | 545.4 | 340.9 | 160.4 |
| $0{ }^{\circ} \mathrm{C}$ | 554.1 | 347.5 | 160.3 |
| $-20^{\circ} \mathrm{C}$ | 562.7 | 353.7 | 160.2 |
| $-40^{\circ} \mathrm{C}$ | 572.1 | 359.7 | 160.4 |
| $-60^{\circ} \mathrm{C}$ | 581.1 | 365.4 | 160.3 |
| $-80^{\circ} \mathrm{C}$ | 588.9 | 370.5 | 160.1 |
| $-100^{\circ} \mathrm{C}$ | 594.3 | 375.5 | 160.1 |

### 3.4 Robust Design against Background Charges

It is known that BCs shift the phase of Coulomb blockade oscillation which for SETs working at voltage or current mode will result in circuit malfunction. Remember that the effect of BCs on $V_{D S \mid S E T}$ oscillation is the same as that of voltage applied on the second gate of SET; we therefore propose a feedback structure which counteracts the effect of BCs by introducing a feedback voltage through another gate of SET.

### 3.4.1 Adaptive Feedback Structure

Since the fluctuation of BCs is random in nature, we need to find a way that is able to automatically adjust the output voltage, depending on the amount of charges on island of SET. Figure 3.6 shows a parallel SETMOS with an adaptive feedback structure which actually employs an error detection and correction mechanism.


Figure 3.6: $\quad$ Parallel SETMOS with an adaptive feedback structure.

Before explaining how the feedback works, let us first examine the effect of BCs on the output of parallel SETMOS. Figure 3.7 shows the voltage oscillations of $V_{D S \mid S E T}$ and $V_{\text {OUT }}$ versus $V_{I N}$ of the parallel SETMOS with different BCs. In this case, the phase of $V_{D S \mid S E T}\left(\right.$ also $\left.V_{\text {OUT }}\right)$ is initially shifted by $2 \pi$ compared to the one in Figure 3.2 (i.e., $V_{\text {OUT2 }}$ ), which can be done by changing the value of $V_{P C}$.


Figure 3.7: $\quad V_{D S S E T}$ and $V_{O U T}$ oscillations of the parallel SETMOS (without feedback) with BCs changing from $-0.3 e$ to $0.3 e$.

For $V_{D S \mid S E T}$ and $V_{O U T}$ oscillations of Figure 3.7, if input voltages are chosen to be $V_{L}$ and $V_{H}$ (representing logic ' 0 ' and ' 1 ', respectively), the parallel SETMOS structure exhibits good immunity against BCs when the input is logic ' 1 ' (i.e., $V_{I N}=V_{H}=700 \mathrm{mV}$ ). This is because that the transfer of voltage oscillation from SET's drain terminal (i.e., $V_{D S \mid S E T}$ ) to the output node (i.e., $V_{O U T}$ ) is based on the threshold logic of NMOS transistor. Even though $V_{D S \mid S E T}$ varies a lot when $V_{I N}=V_{H}$ due to the presence of BCs, $V_{\text {OUT }}$ remains almost zero since $V_{D S \mid S E T}$ is always greater than the threshold voltage of NMOS transistor. However, when the input is logic ' 0 ' (i.e., $V_{I N}=V_{L}=0 \mathrm{~V}$ ), $V_{\text {OUT }}$ changes significantly even with small amount of BCs, resulting in incorrect logic operation. As a result, for the circuit robustness against BCs , we only need to consider the reliability issue during the input period of logic ' 0 '.

The working principle of the circuit in Figure 3.6 is as follows. When $V_{I N}$ is logic ' 0 ', P 1 is on. If there is no BC during this period, $V_{\text {OUT }}$ will be logic ' 1 ' and P 2 will be off, resulting in no feedback path in the circuit. However, if there are BCs that are large enough to change $V_{\text {OUT }}$ from logic ' 1 ' to ' 0 ', P 2 will be on, forcing the feedback voltage (i.e., $V_{F B}$ ) to increase which adjusts $V_{O U T}$ accordingly. Once $V_{O U T}$ returns back to logic '1' for correct logic operation, P2 will be off again, leaving $V_{F B}$ constant to offset certain amount of BCs. On the other hand, when input is logic ' 1 ', P 1 is off with no feedback path in the circuit. In fact, since $V_{\text {OUT }}$ is always logic ' 0 ' during this period which is logically correct regardless the presence of BCs. Thus, no feedback is required at this moment.

It should be mentioned that the operating speed of SET is much slower than MOSFET due to the low biasing current. The delay of the circuit in Figure 3.6 from the input to the
output is about 10 ns , most of which is required by SET. Since the feedback is designed to play a role right after the circuit becomes logically incorrect, the first step of the circuit in each clock cycle is to evaluate the logic correctness. Therefore, it is critical to add a buffer in the feedback path to match the delay.

Simulation results show that the circuit in Figure 3.6 is able to counteract the effect of BCs effectively, as shown in Figure 3.8, where $V_{F B}$ varies with different amount of BCs on island of SET. The circuit is able to tolerance BCs up to $\pm 0.3 e$.


Figure 3.8: Simulation result of parallel SETMOS with adaptive feedback of Figure 3.6 where $\mathrm{BCs}=0,0.1 e, 0.2 e$, and $0.3 e$.

### 3.4.2 Improved SET/MOS Hybrid ADC using Adaptive Feedback

The proposed parallel SETMOS with adaptive feedback structure if working as an inverter is more complicated than its CMOS counterpart. However, parallel SETMOS is not just an inverter (because of the Coulomb blockade oscillation). Other circuits that incorporate it as the basic building block can be much simpler. SET/MOS hybrid ADC is such an example.

SET/MOS hybrid ADC has already been proposed by other research groups which consists of a sample/hold circuit, a capacitor divider, and several ADC units (which is actually the serial SETMOS) [31, 49]. The circuit has very low current drivability due to the small biasing current. Also, the effect of BCs significantly limits the practical application of this circuit.

In this work, we use parallel SETMOS as the ADC unit in order to increase current drivability. Also along with adaptive feedback structure, the circuit exhibits higher immunity against BCs. Since the input of ADC is a continuous analog signal, we need to consider the background charge effect over the entire input range instead of certain values as mentioned previously for the digital applications. Therefore, the adaptive feedback structure used for ADC units is re-designed, as shown in Figure 3.9. Assume all MOS transistors in this figure have the same threshold voltage (i.e., $V_{T H \mid N 1}=V_{T H \mid N 2}=$ $\left.\left|V_{T H \mid P 1}\right|=\left|V_{T H \mid P 2}\right|=V_{T H}\right)$. With an appropriate parameter selection, one can guarantee that with no BC, $V_{O U T}$ will be smaller than $V_{T H}$ as long as $V_{I N}$ is smaller than $V_{T H}$, thus producing logic ' 0 '. During this period, P1 and P2 are on while N1 and N2 are off, resulting in no feedback in the circuit. However, if there are BCs that cause $V_{\text {OUT }}$ to be greater than $V_{T H}, \mathrm{~N} 1$ will be on and P2 will be off, and hence a feedback path through P1
and N 1 will be established, forcing $V_{\text {OUT }}$ to go back to its desired value. Once $V_{\text {OUT }}$ is reduced to be smaller than $V_{T H}$ again, the feedback path will be cut off, leaving $V_{F B}$ constant to offset the BCs. On the other hand, when $V_{I N}$ is greater than $V_{T H}$, the feedback path through N 2 and P 2 will play a role in the same way to correct the output logic regarding to the BCs .

In the real situation, it will take some time for MOSFETs to turn on and off, and the switching time for PMOS and NMOS is a little different. However, if the threshold voltage of PMOS and NMOS in the feedback is chosen carefully, the circuit will converge to an appropriate point where the output can be adjusted accordingly.


Figure 3.9: Parallel SETMOS with adaptive feedback used for the ADC units.

Figure 3.10 shows the simulation result of the circuit in Figure 3.9 with different amount of BCs on island of SET. Since SET is a multi-threshold device, the feedback structure is only valid during the first period of $V_{\text {OUT }}$ oscillation where $V_{F B}$ stays at different voltage levels that maintain the constant phase of $V_{O U T}$ oscillation without being affected by the BCs.


Figure 3.10: Simulation result of the circuit of Figure 3.9 with $\mathrm{BCs}=0,0.1 e, 0.2 e$, and $0.3 e$.

In order to make all the periods of $V_{\text {OUT }}$ oscillation less sensitive to the BCs, the input voltage needs to be biased within the range corresponding to the first period of $V_{\text {OUT }}$ oscillation before going to the feedback structure. Figure 3.11 (a) shows the input and output of an ADC circuit. The feedback structure with a biasing network used for output bit $D_{l}$ and $D_{0}$ is shown in Figure 3.11 (b) and (c), respectively.

(a)

(b)

(c)

Figure 3.11: (a) Input and output relationship of a 3-bit ADC circuit; (b) The feedback structure with the biasing network used for the output bit $D_{l}$; (c) The feedback structure with the biasing network used for the output bit $D_{0}$.

It can be seen from Figure 3.11 (b) and (c) that each digital output bit is determined by the combination of higher bits. The biasing network for a higher bit turns out to be simpler and faster. Since the most significant bit (i.e., $D_{2}$ which only utilizes the first period of $V_{\text {OUT }}$ ) is very reliable against BCs , the lower output bits (i.e., $D_{l}$ and $D_{0}$ ) are quite reliable as well. The feedback structure applied on each ADC unit acts as a shield covering every period of $V_{\text {OUT }}$ oscillation which protects the ADC circuit from being affected by the BCs.

Figure 3.12 shows the entire schematic of a 3-bit SET/MOS hybrid ADC circuit. Simulation results in Figure 3.13 shown that without feedback, the circuit output will be totally destroyed due to the effect of BCs; however with feedback, the output is highly immune to BCs with the tolerance up to $0.3 e$.


Figure 3.12: Improved 3-bit SET/MOS hybrid ADC with adaptive feedback structure.

(a)



(b)

Figure 3.13: Simulation results of the 3-bit SET/MOS hybrid ADC without (a) and with (b) the feedback, where $\mathrm{BCs}=0,0.1 e, 0.2 e$, and $0.3 e$.

### 3.5 Summary

In this chapter, we first introduced the simulation technique used for SET/MOS hybrid circuits based on MIB compact model for SET. Then we analysed the performance of two widely used SET/MOS hybrid architecture - serial and parallel SETMOSs - in terms of power dissipation, current drivability, and temperature effect. Study shows that serial SETMOS has extremely low power dissipation and very weak current drivability because of the small biasing current. Parallel SETMOS has strong current drivability at the cost of increased power dissipation. Both serial and parallel SETMOSs are able to work at room temperature, but still very sensitive to the temperature variation. By taking advantage of the opposite temperature coefficients of the voltage gain of MOSFETs and the amplitude of Coulomb oscillation, SET/MOS hybrid circuits could be less temperature-dependent. In order to increase the circuit robustness against BCs, we also proposed an adaptive feedback structure which is actually an error detection and correction mechanism. The offset of BCs is realized by applying a feedback voltage through a gate terminal of SET. Finally, a SET/MOS hybrid ADC is demonstrated as an example that uses such a feedback structure and exhibits high immunity against BCs with the tolerance up to $0.3 e$.

## Chapter 4

## SET/MOS Hybrid Binary Full Adders

### 4.1 Introduction

Binary full adder (FA) is the key element for arithmetic operations. It is therefore of special interest to design FA with extremely small size and ultra-low power dissipation. Extensive research work has been done on the FA design based on single-electrontunneling technology, utilizing a variety of methods such as majority logic [54, 55], linear threshold logic [56], pass-transistor logic (PTL) [57], binary decision diagram (BDD) [58], and many others [59-61]. While these pure SED-based FAs consume small area and power, they can only work at very low temperature (less than 10 K ), making them impractical for real applications. Several FAs using hybrid MOS and SET architectures have also been reported with increased temperature operation (up to room temperature) [62-64]; However, some of them [62, 63] simply adopted conventional CMOS FA structures which did not adequately take advantage of the new characteristic of SET. The hybrid FA in [64] did utilize Coulomb blockade oscillation characteristic that reduced the number of devices, the less regularity of those circuits made them not suitable for further

VLSI design. Also, the background charge effect creates serious problem on the circuit reliability, which has not been taken into account in above FAs.

In this Chapter, we propose three different implementations for the 1-bit binary FA using parallel SETMOS structure based on the schemes of multiple-valued logic (MVL), phase modulation and frequency modulation, respectively. Theses FAs fully utilize the Coulomb blockade oscillation characteristic of SET which further reduces the circuit area and power dissipation with high regularity. In particular, the frequency modulated 1-bit FA exhibits high immunity against BCs and can be easily extended to multi-bit FAs.

### 4.2 Implementations of SET/MOS Hybrid FAs

### 4.2.1 Multiple-Valued Logic (MVL) Scheme

For a constant current biased SET, due to hole accumulation at SET's drain terminal, electrons induced from the ground will tunnel through both source and drain junctions of SET via the island, leading to a tunneling current. At steady state, the tunneling current equals to SET's biasing current, which means that the number of electrons successfully passed through SET's source and drain junctions equals to the number of holes accumulated at SET's drain terminal per unit time. The excess number of accumulated holes during transient response contributes to SET's drain voltage (i.e., $V_{D S \mid S E T}$ ). Since SET's input gate voltage (i.e., $V_{G S \mid S E T}$ ) has an impact on electron tunneling rate, it affects the net amount of holes at SET's drain terminal at steady state, and hence affects $V_{D S S E T}$. In other words, SET can be considered as a tunable resistor whose resistance is controlled by $V_{G S \mid S E T}$.

Consider a parallel SETMOS structure employing three SETs, as shown in Figure 4.1 (a) where the three SETs are identical with the same biasing voltage of $V_{P C}$ applied on each one's second gate. Such parallel connected SETs are analogous to three parallel resistors. Through appropriate configuration, each SET reaches its minimum (or maximum) resistivity with its input gate voltage (i.e., $V_{I N-A}, V_{I N-B}$, and $V_{I N-C}$ ) being logic ' 0 ' (or ' 1 '). As a result, if all three inputs are logic ' 0 ', the total equivalent resistance (i.e., $R_{\text {eq }}$ ) of three SETs is minimal, and thus $V_{D S \mid S E T}$ reaches its minimum value. As the number of 1's in the input increases, so do the values of $R_{e q}$ and $V_{D S \mid S E T}$. With all three inputs being logic ' 1 ', $R_{e q}$ and $V_{D S \mid S E T}$ will reach their maximum values.

More specifically, as shown in Figure 4.1 (b), if one input voltage (say $V_{I N-A}$ ) increases from zero to a considerable value with two other inputs being:
(1) both logic ' 0 ',
(2) logic ' 0 ' for one and logic ' 1 ' for the other, or
(3) both logic ' 1 ',
one can obtain three $V_{D S \mid S E T}$ oscillations which have the same periodicity and phase but at different voltage levels. For digital applications (i.e., digital voltage levels are $V_{L}$ and $V_{H}$ ), eight input patterns (i.e., from ' 000 ' to ' 111 ') correspond to six points (i.e., $P 0 \sim P 5$ ) on three voltage oscillating curves which are located at four voltage levels (i.e., $V 0 \sim V 3$ ).

Notice that each voltage level represents different number of 1's within the input. Since a 1-bit FA is equivalent to a (3:2) counter whose input and output relationship is listed in Table 4.1, the four voltages of $V 0 \sim V 3$ have to be appropriately converted to $V_{L}$ and $V_{H}$ (i.e., logic ' 0 ' and ' 1 ') so as to generate correct output carry and sum logics. This can be done by using two more parallel SETMOSs. Because the NMOS transistor within the
parallel SETMOS inverses the voltages of $V 0 \sim V 3$, as shown in Figure 4.1 (c), the $V_{\text {OUT }}$ oscillations (i.e., inversely amplified $V_{D S \mid S E T}$ oscillation) of the parallel SETMOSs used to realize carry and sum output bits need to be configured to the pattern as shown in Figure 4.1 (d), where the periodicity and phase can be set by choosing different input-gate capacitances and second-gate voltages for SETs. The entire schematic of 1-bit FA based on MVL scheme is shown in Figure 4.1 (e).

TABLE 4.1 INPUT AND OUTPUT RELATIONSHIP OF A (3:2) COUNTER

| \# of 1's within the input | Carry Out | Sum |
| :---: | :---: | :---: |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |

Parallel connected multiple-SET architecture can also be used to implement digital-toanalog converter (DAC). Since SET can be viewed as a voltage controlled tunable resistor, the equivalent resistance of all SETs and hence the corresponding voltage at $V_{D S \mid S E T}$ can be modulated to represent the evaluations of digital inputs (i.e., decimal representation) rather than the number of 1's in the inputs as long as the resistivity of each individual SET is properly weighted.

(a)


(b)


(c)

(d)

Figure 4.1: (a) Parallel SETMOS with three SETs connected in parallel; (b) $V_{D S \mid S E T}$ oscillation and the voltage conversion of the NMOS transistor; (c) Output voltage oscillations used to realize carry and sum functions; (d) Overall schematic of 1-bit FA based on the MVL scheme.

### 4.2.2 Phase Modulation Scheme

Instead of applying inputs on three SETs, one can use only one SET with multiple input gates to accommodate three input digits, as shown in Figure 4.2 (a) where the three left-hand-side gates of SET are identical and used to accept three input digits, and the fourth right-hand-side gate of SET is used to adjust the phase of $V_{D S \mid S E T}$ oscillation. This is known as phase modulation scheme. Unlike MVL scheme which moves $V_{D S \mid S E T}$ oscillation vertically, phase modulation scheme moves $V_{D S \mid S E T}$ oscillation horizontally based on different input patterns.

By adjusting the device capacitance of SET and biasing voltage of $V_{P C}$, the $V_{D S \mid S E T}$ oscillation (as a result of increasing one input) can be configured to the pattern as shown in Figure 4.2 (b) where the axes Y0, Y1 and Y2 correspond to the condition of two other inputs being:
(1) both logic ' 0 ',
(2) logic ' 0 ' for one and logic ' 1 ' for the other, or
(3) both logic ' 1 ',

It is observed that eight input patterns (i.e., from ' 000 ' to ' 111 ') are well distributed at four points (i.e., $P 0 \sim P 3$ ) on the oscillation curve. For the sum function, a $\pi$ phase shift occurs each time one input digit alters its logic value. For the carry function, since the periodicity is doubled, only $\pi / 2$ phase shift is obtained under the same operation. Both carry and sum outputs can be implemented using the same circuit architecture with different parameters.


Figure 4.2: (a) Overall schematic of a 1-bit FA based on the phase modulation scheme; (b) $V_{D S \mid S E T}$ oscillations used to realize sum and carry functions.

### 4.2.3 Frequency Modulation Scheme

It should be noticed that previous two schemes for FAs strongly rely on particular voltage or current operating point. They work properly with no BC on island of SET. However, with BCs which are random in nature and cannot be entirely removed by today's technology, those schemes may fail to function correctly, depending on the amount of charges. In order to construct a robust SET/MOS hybrid FA against background charge fluctuation, we propose another scheme - frequency modulation scheme - as follows.

## A. 1-bit FA

The circuit structure based on frequency modulation scheme is shown in Figure 4.3 (a), where three left-hand-side gates of SET are identical and connected to a voltage source (i.e., $V_{S}$ which changes monotonically) through three NMOS transistors that function as switches controlled by the digital inputs. Due to the fact that the node capacitance between NMOS and SET is relatively large (at the range of several fF ), SET's input gate capacitance (at the range of several aF ) in such a structure would not be affected by the NMOS switches. It is known that the period of $V_{D S \mid S E T}$ oscillation (as a result of increasing the input gate voltage) is inversely proportional to SET's input gate capacitance. If the $V_{S}$ in Figure 4.3 (a) is applied to multiple input gates of SET, the period of $V_{D S \mid S E T}$ oscillation is thus determined by the total capacitance of the gates that are connected with $V_{S}$ (similar to parallel connected capacitors). Since three input digits applied on the NMOS switches are able to control the connection between $V s$ and input gates of SET, the period of $V_{D S \mid S E T}$ oscillation is hence modulated by different input patterns. When $V s$ increases from zero to
$V_{T O P}$ (i.e., $V_{T O P}=e / C_{G I}$ ), as shown in Figure 4.3 (b), the number of 1's in the inputs equals to the number of $V_{D S \mid S E T}$ oscillating cycles.

The $V_{D S \mid S E T}$ oscillation can be reflected into the time domain if one applies a ramp $V_{S}$ that varies linearly over time. By using a 2-bit ripple counter, the number of voltage oscillation cycles at the output with respect to time is recorded in the binary system, and the counter's outputs represent the carry and sum bits. As long as BCs on island of SET keep constant during the period of varying $V s$, same number of voltage oscillation cycles will appear at the output. Since the amount of BCs on SET's island varies at very low frequency (from minutes to hours), the circuit exhibits much higher immunity against the background charge effect.

(a)

(b)

Figure 4.3: (a) Overall schematic of a 1-bit FA based on the frequency modulation scheme; (b) $V_{D S \mid S E T}$ oscillations with different digital inputs.

## B. Multi-bit FA

Frequency modulation scheme can also be used to implement multi-bit FAs. To accept higher-order input bits, one simply needs to add more input gates for SET, which are connected with $V s$ via NMOS switches, and higher-order output bits can be obtained by adding more cells for the ripple counter.

As an example, Figure 4.4 shows the schematic of a 2-bit FA, where input gate capacitances for $x l$ and $y l$ are twice as much as those for $x 0$ and $y 0$, and three D flip-flops are used to generate three output bits. For a $n$-bit FA in general, SET will have $(2 n+1)$ input gates whose capacitance corresponding to the $i$ th ( $i$ starts from 1 ) input bit is $i$ times as much as that for the least significant input bit, and the number of D flip-flops for the ripple counter is $n+1$. Since each D flip-flop can be implemented with minimum of 8 MOSFETs, the total number of MOSFETs needed is $(2 n+1)+3+8 n=10 n+4$ (each
current source is implemented by a PMOS transistor). With CMOS technology, an $n$-bit ripple carry adder (RCA) (an implementation with minimum hardware) requires $24 n$ MOSFET. A $n$-bit SET/MOS hybrid FA based on frequency modulation scheme dramatically reduces the circuit area and power dissipation, especially for a large $n$ (the area and power consumed by SET are negligible compared to MOSFET).


Figure 4.4: Overall schematic of a 2-bit FA based on the frequency modulation scheme.

### 4.3 Parameter Selection of the Proposed FAs

All proposed SET/MOS hybrid FAs share the same parameters of $R_{T D}=R_{T S}=1 \mathrm{M} \Omega$ and $C_{T D}=C_{T S}=0.1 \mathrm{aF}$ (SET's source and drain junction resistance and capacitance), $I_{D 1}=40 \mathrm{nA}$ (SET's biasing current), $I_{D 2}=1 \mathrm{uA}$ (biasing current for the NMOS transistor), $V_{T H \mid N M O S}=150 \sim 200 \mathrm{mV}$ (threshold voltage of the NMOS transistor), and $T=300 \mathrm{~K}$ (operating temperature). Other parameters used in the proposed FAs (i.e., in Figure 4.1 (d),

Figure 4.2 (a) and Figure 4.3 (a)) are listed in Table 4.2. Figure 4.5 shows the simulation result of FA based on MVL scheme using the provided parameters.

To simulate FA based on frequency modulation scheme, extra control units are needed so that the ripple counter is initialized to zero each time before the evaluating operation (i.e., get the output by changing $V_{S}$ ). For multi-bit FA, as shown in Figure 4.4, $C_{G l}$ and $C_{G 2}$ are the same as those used in Figure 4.3 (a) but with different values of $V_{P C}$.

TABLE 4.2 SET'S INPUT-GATE CAPACITANCE AND THE BIASING VOLTAGES USED IN THREE FAS

| Based on Multiple- <br> Valued Logic (MVL) | MVL block | $C_{G 1}=C_{G 2}=0.13 \mathrm{aF}$ |
| :---: | :---: | :---: |
|  |  | $V_{P C-M}=650 \mathrm{mV}$ |
|  | Carry circuit | $C_{G 1}=C_{G 2}=0.13 \mathrm{aF}$ |
|  |  | $V_{P C-C}=-450 \mathrm{mV}$ |
|  | Sum circuit | $C_{G 1}=C_{G 2}=0.2 \mathrm{aF}$ |
|  |  | $V_{P C-S}=-315 \mathrm{mV}$ |
| Based on Phase <br> Modulation | Carry circuit | $C_{G I}=0.1 \mathrm{aF}, C_{G 2}=0.4 \mathrm{aF}$ |
|  |  | $V_{P C-C}=100 \mathrm{mV}$ |
|  | Sum circuit | $C_{G I}=0.2 \mathrm{aF}, C_{G 2}=0.1 \mathrm{aF}$ |
|  |  | $V_{P C-S}=600 \mathrm{mV}$ |
| Based on Frequency <br> Modulation |  | $C_{G 1}=C_{G 2}=0.1 \mathrm{aF}$ |
|  |  | $V_{P C}=-450 \mathrm{mV}$ |



Figure 4.5: $\quad$ Simulation result of a FA based on the MVL scheme using parameters in Table 4.2.

### 4.4 Summary

We have proposed three SET/MOS hybrid FAs based on the schemes of MVL, phase modulation and frequency modulation. For MVL scheme, SET is considered as a voltage controlled tunable resistor. This method can also be used to implement the DAC. For phase modulation scheme, the carry and sum functions are realized by changing the phase of $V_{D S \mid S E T}$ oscillation. For frequency modulation scheme, the $V_{D S \mid S E T}$ oscillation is reflected in the time domain, and the output is generated by counting the number of oscillation cycles. With this method, a higher immunity against BCs is achieved when the circuit works at a relatively high frequency. Frequency modulation scheme can also be utilized easily to implement multi-bit FAs.

## Chapter 5

## SET/MOS Hybrid Binary Tree Multiplier

### 5.1 Introduction

Due to the fact that MOSFET cannot be shrunk beyond certain limit, more advanced technologies need to be investigated in order to continue the improvement for high performance of multipliers. There has been some research on multipliers based on single-electron-tunneling technology [65-70]. Lageweg et al [65] designed a binary tree multiplier using Threshold Logic Gates (TLGs) as the basic building blocks that operated following Single-Electron Encoded Logic (SEEL). Cotofana et al [66] proposed a novel multiplication scheme using Electron Counting (EC) paradigm through controlled transport of charge, based on which Meenderinck et al [67] designed a high-radix multiplier. Recently, $W u$ et al [68] designed a ternary multiplier based on the 3-T gate using SET. These pure SED-based multipliers exhibit extraordinary performance compared to conventional CMOS multipliers due to the extremely small feature size and ultra-low power consumption of SEDs; however, the low temperature operation ( $<10 \mathrm{~K}$ ) and high sensitivity to environment noises (such as BCs) make them not suitable for practical implementations.

Further, Inokawa et al [69] designed multi-input counters for tree multipliers using SETs combined with MOSFETs which utilized the unique Coulomb blockade oscillation characteristic of SET. Zhang et al [70] introduced a fast multiplication approach which is similar to EC paradigm but implemented using MOSFET-based single-electron turnstiles that can transfer single electrons with fast speed at high temperature. While SET/MOS hybrid multipliers are able to work at relatively high temperature (around 100 K ), BCs still create serious problems which are not discussed in [69] and [70].

Inokawa's counter is much simpler than conventional CMOS counters (or compressors); however, its circuit structure is a little complicated which uses inverting adder, latched quantizer and voltage divider along with negative input voltages. In this chapter, we simplify Inokawa's counter by using multi-input-gate SET with MOSFET through phase modulation scheme, where the output is generated through appreciate configuration on the phase and periodicity of Coulomb blockade oscillation. Moreover, a phase adjustment scheme is introduced for the counter which improves the circuit reliability against BCs. The proposed (7:3) counter can be alternatively viewed as a 2-bit full adder which if employed as the building block for carry propagation adder during the final step of multiplication will further reduce the area and delay of a multiplier.

This chapter is organized as follows. Section 5.2 starts with the introduction of phase modulation scheme, based on which a SET/MOS hybrid (3:2) counter and (7:3) counter are proposed along with improvement for temperature, BCs, and the speed. Section 5.3 presents the implementation of parallel tree multipliers using proposed phase modulated (3:2) and (7:3) counters. Section 5.4 provides the simulation results along with discussions
and comparisons in terms of area, delay and power dissipation. In the end, Section 5.5 concludes the chapter.

### 5.2 Multi-Input Counters for Tree Multiplier

Multi-input counters are the basic building blocks of tree multipliers which output a BCD code (a condensed form) representing the number of 1 's within the input (unitary weighted). Thanks to Coulomb blockade oscillation of SET, the structures of counters implemented using SET/MOS hybrid architectures are very simple, and hence the complexity of the multiplier using these counters is significantly reduced.

### 5.2.1 Phase Modulation Scheme

One big difference between CMOS and single-electron-tunneling technologies is that MOSFET can only have two gates (bulk terminal is viewed as a second gate) while singleelectron devices (SEDs) are able to accommodate multiple gates. Multi-input-gate SET has already been fabricated [71] and the structure of charge storage node (i.e., island) with capacitively coupled multiple gate terminals is widely used, such as single-electron tunneling based majority gate (MAJ) [54, 55], threshold logic gate (TLG) [56], passtransistor logic (PTL) [57], and so on.

Figure 5.1 (a) shows a serially connected SET and NMOS transistor (i.e., serial SETMOS) biased by a current source where SET is associated with multiple gate terminals. In this figure, the left $n$ gates (with the same gate capacitance of $C_{G}$ ) of SET are used to accept $n$ input voltages (i.e., $V_{\text {in } 0}, V_{i n 1}, \ldots, V_{\text {in(n-l) }}$ ) while the one on the right (with the bias voltage of $V_{P C}$, where ' $p c^{\text {' }}$ stands for phase control) is used to control the phase of $V_{D S \mid S E T}$ oscillation (i.e., the drain-to-source voltage of SET which oscillates with respect to
the gate voltage for constant current biasing). The NMOS transistor used here is biased in the sub-threshold region (with the threshold voltage of $V_{t h}$ ) which maintains the small value of $V_{D S \mid S E T}$ so as to obtain observable Coulomb blockade oscillation. Ideally, when $V_{g g}-V_{D S \mid S E T}>V_{t h}$, the NMOS transistor is on and $V_{\text {out }}$ equals to $V_{D S \mid S E T}$ which is nearly zero (because $V_{g g} \approx V_{t h}$ for sub-threshold operation), otherwise, the NMOS transistor is off and $V_{\text {out }}=V_{D D}$.

Figure 5.1 (b) shows the $V_{D S \mid S E T}$ and $V_{\text {out }}$ oscillations of Figure 5.1 (a) (corresponding to the leftmost $y$ axis) as a result of increasing one input voltage (say $V_{i n-i}$, where $0 \leq i<n$ ) from zero to a considerable value with all other input voltages being zero; $V_{P C}$ is configured such that $V_{D S \mid S E T}$ reaches the minimum value at origin; $V_{g g}$ is chosen to be $V_{M}+$ $V_{t h}$, where $V_{M}=\left(V_{H}+V_{L}\right) / 2$, which ensures the $50 \%$ duty cycle for $V_{o u t}$. Note that: 1 ) $V_{D S \mid S E T}$ shown here is symmetric for demonstration purpose which is not necessary for the real implementation as long as $V_{\text {out }}$ maintains $50 \%$ duty cycle; 2) the square $V_{\text {out }}$ is the ideal characteristic curve of a threshold logic which for a real NMOS transistor will have certain transition regions when $V_{D S \mid S E T}$ approaches to $V_{M}$.

For digital application, let 0 V and $e / 2 C_{G} \mathrm{~V}$ (i.e., half of the periodicity of $V_{D S \mid S E T}$ ) be logic ' 0 ' and ' 1 '. Then with one other input voltage (say $V_{i n-j}$, where $0 \leq j<\mathrm{n}$ and $j \neq i$ ) being logic ' 1 ', the $V_{D S \mid S E T}$ in Figure 5.1 (b) will be shifted half of the period to the left. Instead of drawing another oscillation curve, we moves the $y$ axis half of the period to the right. Likewise, with $k(0 \leq k<n-1)$ other input voltages being logic ' 1 ', the $y$ axis will be shifted $k / 2$ periods to the right. It can be seen from Figure 5.1 (b) that if $k$ is an even number, $y$ axis will stop at the valley point on $V_{D S \mid S E T}$; otherwise, it falls at the peak point. As a result, all kinds of $n$-bit digital inputs are separated into two groups where the


Figure 5.1: (a) Serial SETMOS with $n$ input gates for SET; (b) $V_{D S S E T}$ and $V_{\text {out }}$ oscillations.
number of 1's within the input is even or odd. With $V_{D D}=e / 2 C_{G} \mathrm{~V}$ (i.e., the same as input digital level), the input and output relationship of Figure 5.1 (a) is given by

$$
\begin{equation*}
d_{o u t}=d_{i n 0} \oplus d_{i n 1} \oplus \cdots \oplus d_{i n(n-1)} \tag{5.1}
\end{equation*}
$$

where $\oplus$ denotes the XOR logic, $d_{\text {in }}, d_{\text {in }}, \ldots, d_{\text {in(n-l) }}$ and $d_{\text {out }}$ are digital representations of the input and output. The structure of Figure 5.1 (a) with $n=2$ is actually a XOR gate which is first demonstrated by Ono et al [57]. Equation (1) represents a chain of XOR gates connected in serial which if implemented using CMOS technology will require a lot more transistors.

### 5.2.2 Primitive Implementation of (3:2) and (7:3) Counters

(3:2) counter (i.e., full adder) and (7:3) counter can be implemented through the phase modulation scheme with great simplicity. According to the input and output relationships of the two counters summarized in Table 5.1 (circled parts are used for the (3:2) counter), it is observed that output bit $d_{\text {out0 }}$ (i.e., the least significant bit) represents an even/odd logic with respect to $k$ (i.e., the number of 1's within the input) which can be therefore generated using the structure of Figure 5.1 (a) with $n=3$ for a (3:2) counter and $n=7$ for a (7:3) counter.

In fact, with two 1's and four 1's to be considered as a unit, respectively, output bits $d_{\text {outl }}$ and $d_{\text {out } 2}$ stand for the even/odd logic as well (with respect to $\lfloor k / 2\rfloor$ and $\lfloor k / 4\rfloor$, where $\lfloor\cdot\rfloor$ indicates the flow value) which can be produced by the same structure of Figure 5.1 (a) with different input gate capacitances for SET.

TABLE 5.1 INPUT AND OUTPUT RELATIONSHIPS OF (3:2) AND (7:3) COUNTERS

| \# of 1's within <br> the input (i.e., $k$ ) | $\mathrm{d}_{\text {out2 }}$ | $\mathrm{d}_{\text {out1 }}$ | $\mathrm{d}_{\text {out0 }}$ |
| :---: | :---: | :---: | :---: |
| 0 0 0 <br> 0   <br> 1 0 0 <br> 1   <br> 2 0 1 <br> 3 0 1 <br> 4 1 0 <br> 5 1 0 <br> 6 1 1 <br> 7 1 1 |  |  |  |
| 2 |  |  |  |

It is understood that by scaling $C_{G}$ down to the half and quarter values, the periodicity of $V_{D S \mid S E T}$ will be doubled and quadrupled, as shown in Figure 5.2. With the same digital levels at the input (i.e., $y$ axes remain unchanged), the points associated with different $y$ axes (i.e., point A, B, C, D, E, F, G, and H) on $V_{D S \mid S E T 0}$ are re-grouped which with the help of MOSFET's threshold logic generate the desired logic for outputs bits $d_{\text {outl }}$ and $d_{\text {out } 2}$. Notice that for the three $V_{D S \mid S E T}$ oscillations in Figure 5.2 the initial phases are different which can be set through $V_{P C}$, while the amplitude is the same which requires the same total device capacitance of SET (i.e., $C_{\Sigma}=n \cdot C_{G}+C_{G 2}+C_{T D}+C_{T S}$ for the SET in Figure 5.1 (a)). The reduced $C_{\Sigma}$ as a result of scaling $C_{G}$ can be compensated by $C_{T D}$, $C_{T S}$, or $C_{G 2}$.

Figure 5.3 shows a basic implementation of a (3:2) counter and (7:3) counter, where the current source used to bias SET is implemented using a PMOS transistor; the input gate capacitance of SET used for $d_{\text {out }}, d_{\text {out }}$, and $d_{\text {out } 2}$ is configured as $C_{G}, C_{G} / 2$, and $C_{G} / 4$,
respectively. It should be mentioned that the node capacitance at each input is much larger (several fF ) than SET's input gate capacitance (1aF at the most) which protects SETs from being affected by each others.


Figure 5.2: $\quad V_{D S S E T}$ oscillations with the input gate capacitances of $C_{G}, C_{G} / 2$, and $C_{G} / 4$ for SET used to realize $d_{\text {out }}$, $d_{\text {out }}$, and $d_{\text {out }}$, respectively.


Figure 5.3: Primitive type (3:2) (a) and (7:3) (b) counters based on the phase modulation scheme.

### 5.2.3 Enhanced Implementation of the (7:3) counter

Primitive type (3:2) and (7:3) counters are very simple, with which as the basic building blocks tree multipliers will consume extremely small area and power with high regularity. However, this type of counters suffers from some critical limitations, such as operating temperature, reliability against BCs , and the operating speed. In order to deal with these practical issues, we introduce some modifications as follows.

## A. Increased Temperature using Input Capacitor Array

With large number of input gates for SET, $C_{\Sigma}$ of SET becomes relatively large which significantly limits the operating temperature (because $C_{\Sigma}$ is inversely proportional to the amplitude of Coulomb blockade oscillation which attenuates with increased temperature). It is known that Coulomb blockade oscillation is essentially determined by potential on island of SET (i.e., $V_{\text {Island }}$ ) which for the SET in Figure 5.1 (a) is given by

$$
\begin{align*}
V_{\text {Island }} & =\frac{C_{G}}{C_{\Sigma}} V_{i n 0}+\cdots+\frac{C_{G}}{C_{\Sigma}} V_{i n(n-1)}+\frac{C_{T D}}{C_{\Sigma}} V_{D S \mid S E T}-\frac{m \cdot e}{C_{\Sigma}}  \tag{5.2}\\
& =\frac{C_{G}}{C_{\Sigma}}\left(V_{i n 0}+\cdots+V_{i n(n-1)}\right)+\frac{C_{T D}}{C_{\Sigma}} V_{D S \mid S E T}-\frac{m \cdot e}{C_{\Sigma}}
\end{align*}
$$

where $m \cdot e$ is net charges on the island. Therefore, instead of applying individual input voltages to SET through multiple input gates, we can first accumulate input voltages and then apply the total voltage to SET through only one input gate. Normally, this can be done by using an analog voltage adder, such as the one used in Inokawa's counter which is actually a cascode stage voltage amplifier with feedback that provides a linear relationship between the input and output (as long as the gain of voltage amplifier is large
enough). Consider that fact that the input gate capacitance of SET is extremely small, a simple CMOS capacitor array is able to sum the input voltages without being affected by SET (there is no loading effect associated with SET at the input node). Figure 5.4 shows the implementation of a (7:3) counter with input capacitor array, where $C_{i n} \gg C_{G}$ (say a thousand times). With digital input levels being 0 V and $V_{D D}$, the summing voltage can be expressed as

$$
\begin{equation*}
V_{s u m}=k \cdot \frac{V_{D D}}{8} \tag{5.3}
\end{equation*}
$$

where $k$ represents the number of 1 's within the input. In order to generate correct output following phase modulation scheme (refer to Figure 5.2), $V_{D D}$ has to be $4 e / C_{G}$. If $C_{G}$ is chosen to be 0.64 aF , then $V_{D D}=1 \mathrm{~V}$ which is quite suitable for practical circuits.

The structure of serial SETMOS with input capacitor array has also been used in Inokawa's ADC [31] and counter [69] and Ou's DAC [49] without any problem. By using input capacitor array, $C_{\Sigma}$ of SET is reduced, and hence the (7:3) counter is able to work at even room temperature.

## B. Improved Reliability using Phase Adjustment Scheme

Since BCs on island of SET shift the phase of Coulomb blockade oscillation without changing its amplitude and periodicity, the proposed phase modulated multi-input counters are very sensitive to BCs. Thanks to the threshold logic of MOSFET, however, the output of counters exhibits certain redundancy against BCs. It can be seen from Figure 5.2 that with the input to be biased at peak and valley points of $V_{D S \mid S E T 0}, d_{\text {out } 0}$ exhibits the highest tolerance to BCs which is up to $\pm 0.25 e$; while with the input to be


Figure 5.4: Implementation of a (7:3) counter with temperature enhancement using serial SETMOS and input capacitor array.
biased away from peak and valley points, $d_{\text {out }}$ and $d_{\text {out } 2}$ can only bear BCs up to $\pm 0.12 e$ and $\pm 0.065 e$ (worst case) for correct logic operation.

With inputs biased close to the transition region (such as point $\mathrm{A}, \mathrm{D}, \mathrm{E}$, and H for $d_{\text {out } 2}$ ), the output characteristic curve has to be very sharp which also places a lot design difficulties. In order to improve the reliability of $d_{\text {out } 1}$ and $d_{\text {out } 2}$ and alleviate the design difficulty, we need to dynamically adjust the phase of $V_{D S \mid S E T 1}$ and $V_{D S \mid S E T 2}$ so that all inputs are well located at the peak or valley point. This can be done by adding a bias voltage through an additional gate of SET.

Notice that for $V_{D S \mid S E T I}$ in Figure 5.2, each peak and valley point is surrounded by two input points. If a input corresponds to the point on the left side of the peak and valley (i.e., point $\mathrm{A}, \mathrm{C}, \mathrm{E}$, and G$)$, the $V_{D S \mid S E T I}$ need to be shifted to the left, otherwise, it has to be moved to the right (i.e., input corresponds to point B, D, F, and H). Since $d_{\text {out }}$ generates different output logic for the two groups of input points, the direction of phase adjustment for $d_{\text {outl }}$ can be therefore controlled by $d_{\text {out } 0}$. It is known that BCs vary from minutes to hours generally following Gaussian distribution with the high probability of being less than $\pm 0.3 e$. If BCs are restricted within $\pm 0.25 e$ due to the manufacturing advancement, we can say $d_{\text {out }}$ is rather reliable against BCs which also results in the same reliability level for $d_{\text {out }}$.

One is able to use two constant biasing voltages with equal amount and opposite polarity for $d_{\text {outl }}$ controlled by $d_{\text {out }}$; however, this will need a multiplexer which consumes extra area and power. Instead of using the multiplexer, we can simply apply $d_{\text {out0 }}$ to the SET (used for $d_{\text {outl }}$ ). This requires the phase of $V_{D S \mid S E T}$ in Figure 5.2 to be readjusted (through $V_{P C}$ ) as shown in Figure 5.5.


Figure 5.5: $\quad V_{D S S E T}$ and output voltage oscillations used for reliability improvement.

It is observed that for $V_{D S \mid S E T I}$ in Figure 5.5 , input point $\mathrm{B}, \mathrm{D}, \mathrm{F}$, and H are already at the best position where $d_{\text {out } 0}=1$, so there is no need to adjust the phase; while input point $\mathrm{A}, \mathrm{C}, \mathrm{E}$, and G are located at the switching point where $d_{\text {out } 0}=0$. As a result, when the input is biased at point $\mathrm{A}, \mathrm{C}, \mathrm{E}$, and G , the phase of $V_{D S \mid S E T I}$ needs to be shifted $\pi / 2$ to the
right so as to generate correct output (refer to Figure 5.2, where point A, C, E, and G are grouped with point $\mathrm{B}, \mathrm{D}, \mathrm{F}$, and H , respectively). The phase adjustment for $d_{\text {out }}$ can be therefore accomplished by applying $\overline{d_{\text {out } 0}}$ (i.e., the inverse of $d_{\text {out } 0}$ through a CMOS inverter) to the SET (used for $d_{\text {out }}$ ) though an additional gate. If the capacitance of the additional gate (i.e., $C_{G 3}$ ) is the same as the input gate capacitance (i.e., $C_{G 3}=C_{G} / 2$ ), $\pi / 2$ phase adjustment for $V_{D S \mid S E T 1}$ will require a voltage of $e / 2 C_{G} \mathrm{~V}$. A capacitive voltage divider will be used so as to generate desired voltage from $V_{D D}$.

For $V_{D S \mid S E T 2}$ in Figure 5.5, point D and H are on the right position, while point $\mathrm{A}, \mathrm{B}, \mathrm{C}$ and point $\mathrm{E}, \mathrm{F}$, G need to be grouped with point D and point H . The correct output of $d_{\text {out } 2}$ can be realized by applying $\overline{d_{\text {out } 0}}$ and $\overline{d_{\text {out } 1}}$ to SET (used for $d_{\text {out } 2 \text { ) through two additional }}$ gates that generate $\pi / 4$ and $\pi / 2$ phase adjustment for $V_{D S \mid S E T 2}$, respectively.

Figure 5.6 shows the implementation of a (7:3) counter with phase adjustment scheme, where $C_{G 3}=C_{G} / 2$ and $C_{G 4}=C_{G} / 4$. With the help of capacitive voltage divider, $V_{P A I}=$ $V_{P A 2}=V_{D D} / 8=e / 2 C_{G} \mathrm{~V}$ (' $p a$ ' stands for phase adjustment). Notice that $V_{P A 1}$ is connected to the gate that has the same gate capacitance as the input, hence it produces $\pi / 2$ and $\pi / 4$ phase adjustment for $V_{D S \mid S E T 1}$ and $V_{D S \mid S E T 2}$, respectively; while $V_{P A 2}$ is connected to the gate that has twice gate capacitance of the input gate, it thus generates $\pi / 2$ phase adjustment for $V_{D S \mid S E T 2}$. Such configuration results in the same gate capacitance (i.e., $C_{G}$ $+C_{G 2}$ ) for three SETs which simplifies the parameter selection.

Because output bit $d_{\text {out } 0}$ is reliable against BCs, output bits $d_{\text {out } 1}$ and $d_{\text {out } 2}$ are rather reliable as well. The reliability of the (7:3) counter is therefore improved.


Figure 5.6: Implementation of a (7:3) counter using phase adjustment scheme.

## C. Increased Speed using Parallel SETMOS Structure

Due to the small biasing current (i.e., $I_{\text {Bias }}$ ) that drives MOSFET with large RC constant, the speed of the serial SETMOS is significantly limited. On the one hand, to sustain Coulomb blockade oscillation, $I_{B i a s}$ has to be a small value which with $C_{\Sigma}$ and the junction resistance (i.e., $R_{T D}$ and $R_{T S}$ ) of SET being a few aF and hundreds of $\mathrm{K} \Omega$ is about tens of nA. With further reduced $C_{\Sigma}, R_{T D}$ and $R_{T S}, I_{\text {Bias }}$ can be as high as hundreds of nA which is able to keep the delay of SET less than 0.5 ns (with the loading capacitance of a few hundred aF ). On the other hand, because of the small amplitude of $V_{D S \mid S E T}$ especially at higher temperature, the sub-threshold slope of NMOS transistor has to be steep so as to generate the square-like $V_{\text {in }}$ vs. $V_{\text {out }}$ characteristics shown in Figure 5.1 (b). This requires large width and length for the NMOS transistor that provides high voltage gain with relatively low on-state resistance. Also, with the current source to be implemented by a PMOS transistor, the length of PMOS has to be large as well which with large voltage swing at the output produces near constant $I_{\text {Bias }}$ (fixed $I_{\text {Bias }}$ is desirable so as not to kill the voltage gain of NMOS transistor). The large size of NMOS and PMOS transistors generate lots of parasitic capacitance which therefore introduces a large delay at the output. Even with hundreds of nA for the $I_{\text {Bias }}$, it is very difficult to constrain the delay of serial SETMOS within 1ns range.

In order to increase the operating speed, we can use different biasing currents for SET and NMOS transistor that are connected in parallel (i.e., parallel SETMOS) and followed by a CMOS inverter, as shown in Figure 5.7, where $V_{S S}$ is used to bias $M_{n}$ in the subthreshold region so as to obtain a large voltage gain. The parallel SETMOS structure reduces the delay at the cost of increased power consumption where the biasing current
for $M_{n}$ (i.e., $I_{\text {Biass }}$ ) is up to the range of $\mu \mathrm{A}$.
However, If one solely uses parallel SETMOS to generate a square-like $V_{\text {in }}$ vs. $V_{\text {out }}$ characteristics, the size of $M_{n}$ and $M_{p 2}$ has to be very large (generate very high voltage gain) which requires substantial $I_{\text {Bias2 }}$ to maintain the high speed. To improve the power-delay-product (PDP), we use small size of $M_{n}$ and $M_{p 2}$ (produce moderate high voltage gain) which amplify the amplitude of $V_{D S \mid S E T}$ at high speed with less $I_{\text {Bias } 2}$, and the squarelike $V_{\text {in }}$ vs. $V_{\text {out }}$ characteristics is generated through a CMOS inverter. With advanced CMOS technology (such as 65 nm ), the delay and power consumption (with the load of hundreds of aF and the working frequency of hundreds of MHz ) contributed by the CMOS inverter is very small (i.e., tens of ps delay and hundreds of $n W$ power dissipation) [72]. Therefore, the structure of parallel SETMOS followed by a CMOS inverter exhibits less PDP. Detail discussions will be provided in the simulation part in section 5.4.


Figure 5.7: Parallel SETMOS followed by a CMOS inverter

### 5.3 Implementation of Parallel Tree Multipliers

A parallel tree multiplier involves three steps which are partial product generation (PPG), partial product accumulation (PPA), and carry propagation addition (CPA), respectively [73]. Each step (including PPG and CPA) can be implemented based on the proposed phase modulated multi-input counters.

### 5.3.1 Partial Product Generation (PPG)

The first PPG step requires an array of AND gates that generate a bit matrix used for the next PPA step. Notice that with two input gates for SET, a (3:2) counter becomes a (2:2) counter of which the output bits $d_{\text {out }}$ and $d_{\text {out }}$ actually realize the XOR logic and AND logic. Therefore, an AND gate can be implemented using the serial SETMOS of Figure 5.1 (a) with $n=2$ but $C_{G} / 2$ input gate capacitance for SET. According to the $V_{D S \mid S E T I}$ in Figure 5.2, an AND gate (with 0 V and $e / 2 C_{G} \mathrm{~V}$ as two digital levels) only corresponds to the left three points that represent four input patterns (i.e., logic ' 00 ' at point $\mathrm{A}, \operatorname{logic}$ ' 01 ' and ' 10 ' at point B , and logic ' 11 ' at point C ). In general, with the initial phase of $V_{D S \mid S E T I}$ to be set at point $\mathrm{B}, \mathrm{C}$, and D (through $V_{P C}$ ), the same structure becomes the OR gate, NAND gate, and NOR gates, respectively.

Furthermore, the three points used for the AND gate (i.e., point A, B, and C) can be evenly distributed over an entire period of the $V_{D S \mid S E T I}$, as shown in Figure 5.8. This can be realized by changing the gate voltage of NMOS transistor (i.e., $V_{g g}$ ) until the output reaches $33.3 \%$ duty cycle. In this case, digital levels are set as 0 V and $2 e / 3 C_{G} \mathrm{~V}$ (i.e., one third of the periodicity of $\left.V_{D S \mid S E T I}\right)$. Such configuration increases the reliability of an AND gate against BCs up to $\pm 0.167$ e (instead of $\pm 0.125 e$ ).


Figure 5.8: $\quad V_{D S S E T}$ oscillation with $33.3 \%$ duty cycle at the output for an AND gate that has increased reliability against BCs.

### 5.3.2 Partial Product Accumulation (PPA)

The second PPA step reduces the number of bits in a bit matrix through several levels until two rows remain. This is accomplished by using multi-input counters, such as (3:2) or (7:3) counter, following advanced tree algorithms. Because the number of bits is reduced more than half for a (7:3) counter but just one third for a $(3: 2)$ counter, the PPA step if utilizing (7:3) counters will experience less levels. However, in CMOS technology, a (7:3) counter is actually implemented by four (3:2) counters which require $3 \Delta_{\mathrm{FA}}$ delay $\left(\Delta_{\mathrm{FA}}\right.$ represents the delay unit of a (3:2) counter). The overall performance (such as area, delay, and power dissipation) of the tree multipliers, if not worse, may not be improved that much when employing (7:3) counters. Reference [74] presented a $16 \times 16$ multiplier using (7:3) counters which is a little faster than the one using (3:2) counters but the total transistor count is about $10 \%$ higher.

It is observed from previous session that the phase modulated (3:2) counter and (7:3)
counter exhibit a comparable complexity (even though including the input capacitor array and phase adjustment scheme which are also applied to the (3:2) counter). In addition, the (3:2) and (7:3) counters of Figure 5.3 (with no phase adjustment scheme) are carry free which exhibit the same delay. While there will be the propagation delay if employing the phase adjustment scheme of Figure 5.6, the delay of a (7:3) counter is about 1.5 times of that of a (3:2) counter (instead of 3 times in CMOS technology). Therefore, the multiplier if employing such $(7: 3)$ counters is expected to be superior in terms of area, delay, and power dissipation.

While (2:2), (4:3), (5:3), and (6:3) counters are also used during the PPA step, they are modified (3:2) and (7:3) counters with reduced input gates for SET.

### 5.3.3 Carry Propagation Addition (CPA)

The third CPA step combines last two rows of bits together to generate the final output. This is accomplished through a multi-bit FA based on a group of 1-bit FA, such as ripple carry adder (RCA) or carry look-ahead adder (CLA). Similar to a (3:2) counter which is considered as a 1-bit FA, a (7:3) counter can be alternatively viewed as a 2-bit FA.

Figure 5.9 shows the implementation of a (7:3) counter as a 2-bit FA, where each higher bit of the input controls two input terminals which are short connected; seven input terminals are assigned to two 2-bit inputs (i.e., $X=x_{I} x_{0}$ and $Y=y_{I} y_{0}$ ) with a carry input (i.e., $c_{i n}$ ) that generate a 3-bit output (i.e., $Z=X+Y+c_{i n}=z_{2} z_{I} z_{0}$ ).

In CMOS technology, such realization for a 2-bit FA is not acceptable because a (7:3) counter is composed of four 1-bit FAs while a 2-bit FA can be simply built with two 1-bit FAs. However, a 2-bit FA if implemented using the phase modulated (7:3) counter requires three serial or parallel SETMOSs which is even smaller than the implementation
of two (3:2) counters (needs four serial or parallel SETMOSs). More importantly, a 2-bit FA implemented using the proposed (7:3) counter of Figure 5.3 (with no phase adjustment scheme) exhibits the same delay as a 1-bit FA. Even though with the phase adjustment scheme (for both (3:2) and (7:3) counters), the (7:3) counter (used as a 2-bit FA) occupies three delay units which is still less than the delay of two propagated (3:2) counters (i.e., four delay units). With such 2-bit FA (i.e., the phase modulated (7:3) counter) as the basic building block, the propagation delay of a RCA will be reduced, and the circuitry used to generate and propagate carries for a CLA will be much simplified which also reduces the delay.


Figure 5.9: A 2-bit full adder implemented using a (7:3) counter.

### 5.4 Simulations and Discussions

We use MIB compact model for SETs along with BSIM4 Spector model for MOSFETs. All simulations are conducted using conventional SPICE simulator in Cadence based on CMOS 65 nm technology.

### 5.4.1 Simulation of the Enhanced Type (7:3) Counter

To verify the proposed phase modulation scheme, we simulate the enhanced type (7:3) counter (a (3:2) counter is the sub-circuit of a (7:3) counter) based on the input capacitor array of Figure 5.4, the phase adjustment scheme of Figure 5.6, and the parallel SETMOS followed by a CMOS inverter structure of Figure 5.7. All parameters used for the simulation are listed in Table 5.2, and the design strategy is given as follows.

With $V_{D D}$ of 1 V , the periodicity of $V_{D S \mid S E T 0}$ (refer to Figure 5.2 or Figure 5.5) is set as 250 mV which requires $C_{G}=0.64 \mathrm{aF}$. As a result, the input gate capacitance is 0.64 aF , 0.32 aF , and 0.16 aF for SETs used to generate $d_{\text {out } 0}, d_{\text {out }}$, and $d_{\text {out }}$, respectively, and the phase-adjustment gate capacitance is $C_{G 3}=0.32 \mathrm{aF}$ and $C_{G 4}=0.16 \mathrm{aF}$ (see Figure 5.6). With SET's junction capacitance and phase-control gate capacitance of $C_{T D}=C_{T S}=$ 0.1 aF and $C_{G 2}=0.1 \mathrm{aF}$, the total device capacitance is $C_{\Sigma}=0.94 \mathrm{aF}$ (identical for three SETs) which enables the room temperature operation with 25 mV amplitude of $V_{D S \mid S E T}$ (varying from 125 mV to 150 mV ).

SET's junction resistance is chosen to be $R_{T D}=R_{T S}=100 \mathrm{~K} \Omega$ which along with the biasing current of $I_{\text {Bias }} \approx 300 \mathrm{nA}$ (refer to Figure 5.7 ) achieves 0.25 ns delay for SET. Because the voltage swing of $V_{D S \mid S E T}$ is very small, we use minimum width and length for $M_{p 1}$ (i.e., $W_{\min }=120 \mathrm{~nm}$ and $L_{\text {min }}=60 \mathrm{~nm}$ for CMOS 65 nm technology) with the gate
biasing voltage of $V_{\text {ctrll }}=670 \mathrm{mV}$ which is able to produce near constant current without introducing too much parasitic capacitance that increases the delay.

The small $V_{D S \mid S E T}$ needs to be amplified to a detectable level before fed to the CMOS inverter that generates the square-like output characteristic. To achieve a high voltage gain, $M_{n}$ is biased in the sub-threshold region with the width and length of 120 nm and 180 nm and the source biasing voltage of $V_{S S}=-200 \mathrm{mV}$. Because the voltage swing of $V_{\text {out }}$ is much larger, the length of $M_{p 2}$ has to be large so as to maintain the high voltage gain. With the width and length of $M_{p 2}$ being 120 nm and 600 nm , the amplitude of $V_{\text {out }}$ is about 400 mV that varies from 300 mV to 700 mV .

To realize fast operating speed with large RC constant (the on-resistance of $M_{n}$ is about $2.5 \mathrm{M} \Omega$ ), the biasing current of $I_{\text {Bias } 2}$ is around $1 \mu \mathrm{~A}$ with the gate biasing voltage of $V_{c t r l 2}=487 \mathrm{mV}$ for $M_{p 2}$ which ensures another 0.25 ns delay (from $V_{D S \mid S E T}$ to $V_{o u t}$ ). With the transition width of the CMOS inverter to be 80 mV (reasonable range) centering at 500 mV , a quasi square-like output characteristics is therefore obtained which can be used to realize the phase modulated (7:3) counter with certain redundancy.

Figure 5.10 shows the simulation result at room temperature with the working frequency of 100 MHz (there is no BC ). It can be seen that with the number of 1 's within the input increasing from 0 to $7, V_{\text {sum }}$ increases from 0 V to 875 mV with each step of 125 mV , and the 3-bit output experiences all possible values from " 000 " to " 111 " which verifies the design. Notice that because of the propagation chain used by the phase adjustment scheme, the delay of the $(7: 3)$ counter is determined by $d_{\text {out } 2}$ which is about 1.5 ns .

TABLE 5.2 Parameters for SPICE SIMULATION IN CADENCE

| SET | $R_{T D}, R_{T S}$ | $100 \mathrm{~K} \Omega$ |
| :---: | :---: | :---: |
|  | $C_{T D}, C_{T S}$ | 0.1 aF |
|  | $C_{G}$ | 0.64 aF |
|  | $C_{G 2}$ | 0.1 aF |
|  | $C_{G 3}$ | 0.32 aF |
|  | $C_{G 4}$ | 0.16 aF |
| NMOS | $W_{n}$ | 120 nm |
|  | $L_{n}$ | 180 nm |
|  | $C_{\text {gdo }}, C_{\text {gso }}$ | $100 \mathrm{pF} / \mathrm{m}$ |
|  | $C_{g d l}, C_{\text {gsl }}$ | $73.6 \mathrm{pF} / \mathrm{m}$ |
|  | $t_{o x}$ | 2.4 nm |
|  | $V_{\text {tho }}$ | 228 mV |
|  | nfactor | 1.82 |
|  | $\operatorname{minv}$ | -0.6 |
| PMOS | $W_{p}$ | 120 nm |
|  | $L_{p 1}\left(\right.$ for $M_{p 1}$ ) | 60 nm |
|  | $L_{p 2}\left(\right.$ for $\left.M_{p 2}\right)$ | 600 nm |
|  | $C_{\text {gdo }}, C_{\text {gso }}$ | $79.48 \mathrm{pF} / \mathrm{m}$ |
|  | $C_{g d l}, C_{g s l}$ | $67.97 \mathrm{pF} / \mathrm{m}$ |
|  | $t_{o x}$ | 2.4 nm |
|  | $V_{\text {tho }}$ | -284 mV |
|  | nfactor | 0.92 |
|  | $\operatorname{minv}$ | -0.52 |
| Biasing Voltage | $V_{D D}$ | 1 V |
|  | $V_{\text {trll }}$ | 670 mV |
|  | $V_{t r l 2}$ | 487 mV |
|  | $V_{S S}$ | $-200 \mathrm{mV}$ |
|  | $V_{P C 0}$ | $-300 \mathrm{mV}$ |
|  | $V_{P C I}$ | 900 mV |
|  | $V_{P C 2}$ | 700 mV |
| Capacitor | $C_{\text {IN }}$ | 1 fF |
| Temperature | $T$ | 300 K |

* nfactor and minv affect the sub-threshold slope


Figure 5.10: Simulation result of the enhanced type phase modulated (7:3) counter.

### 5.4.2 Background Charge Effect

To verify the reliability of the enhanced type phase modulated (7:3) against BCs, we compare the simulation result of the counter with and without the phase adjustment scheme of Figure 5.6 . For the $(7: 3)$ counter to generate correct output without phase adjustment scheme, the initial phase of $V_{D S \mid S E T}$ oscillation has to be configured to the pattern shown in Figure 5.2. This requires the phase control voltage of SET (used for three output bits) to be $V_{P C 0}=-300 \mathrm{mV}, V_{P C 1}=900 \mathrm{mV}$, and $V_{P C 2}=700 \mathrm{mV}$, respectively.

Figure 5.11 shows the simulation results under the same input pattern as Figure 5.10, where (a) and (b) are the outputs without phase adjustment scheme that has no BC and $0.1 e \mathrm{BCs}$ on each island of SET; while (c) and (d) are the outputs with phase adjustment scheme along with $0.1 e \mathrm{BCs}$ and $0.2 e \mathrm{BCs}$ on each island of SET. It is observed that without phase adjustment scheme, the output of the (7:3) counter is not reliable which falls corrupt with $0.1 e$ BCs (refer to Figure 5.11 (b) where $d_{\text {out }}$ is not affected, $d_{\text {outt }}$ is weakly affected but still works properly, and $d_{\text {out }}$ is strongly affected which does not function correctly); however, with phase adjustment scheme, the (7:3) counter is highly reliable which generates desired output even with $0.2 e \mathrm{BCs}$.

### 5.4.3 Area-Delay-Power Analysis

Due to the small amplitude of $V_{D S \mid S E T}$ at room temperature (around 25 mV ), to generate square-like output characteristics using serial SETMOS requires very large size for both NMOS and PMOS transistors (refer to [31] and [49] where the width and length are chosen to be a few $\mu \mathrm{m}$ ) so as to achieve very high voltage gain. This results in the delay of serial SETMOS to be more than 1 ns . One possible solution to speed up the serial

(a)

(b)

(c)

(d)

Figure 5.11: Output of the (7:3) counter without phase adjustment scheme and no BC (a); without phase adjustment scheme and $0.1 e \mathrm{BCs}$ (b); with phase adjustment scheme and $0.1 e$ BCs (c); and with phase adjustment scheme and $0.2 e \mathrm{BCs}$ (d).

SETMOS is to reduce the temperature. At lower temperature, the amplitude of $V_{D S \mid S E T}$ is increased which relaxes the requirement of high voltage gain, and hence reduces the size of MOSFETs and the delay (refer to [69] where the delay of the serial SETMOS is less than 0.5 ns at temperature of 77 K ). From this point of view, the speed trades off the temperature.

Another practical solution is to use parallel SETMOS which also requires large MOSFETs to reach very high voltage gain. The reduced delay is because of the increased biasing current which increases the power dissipation (refer to [51] where the delay of the parallel SETMOS is about 0.5 ns with the power dissipation of $2 \mu \mathrm{~W}$; the generated output voltage is not a square-like wave). In this case, the speed trades off the power dissipation. Because of the extremely low power consumption of the serial SETMOS (within the range of nW ), to increase the speed at the cost of moderate power overhead is reasonable.

To further improve the PDP, we reduce the size of MOSFETs for the parallel SETMOS which generates 400 mV output voltage swing with 0.5 ns delay and $1.3 \mu \mathrm{~W}$ power dissipation. The quasi square-like output characteristics is then generated by a CMOS inverter which has the delay of about 10ps. Unlike the serial or parallel SETMOS where the static power (i.e., $P_{\text {static }}=V_{D D} \times I_{\text {Bias }}$ ) is dominant, most power consumed by the CMOS inverter is the dynamic power (i.e., $P_{\text {dynamic }}=C_{\text {Load }} \times V_{D D}{ }^{2} \times f$ ). Due to the speed limitation, the power dissipation contributed by the CMOS inverter at the frequency of 100 MHz with $V_{D D}=1 \mathrm{~V}$ and the loading capacitance of 1 fF is only 100 nW .

With the parallel SETMOS and CMOS inverter as the basic building cell, the area (i.e., transistor count), delay and power dissipation of the enhanced type phase modulated (3:2) and (7:3) counters are listed in Table 5.3, where each capacitor is counted as a MOSFET
and the power dissipation is evaluated at the frequency of 100 MHz . From Figure 5.11 (d), it is observed that the worst case delay of a (7:3) counter is about 3 ns with $0.2 e \mathrm{BCs}$ on island of SET. The maximum working frequency of the proposed (7:3) counter is up to 300 MHz with a little increased power dissipation of $4.5 \mu \mathrm{~W}$.

TABLE 5.3 Area-Delay-Power Estimations of The Enhanced Type Phase Modulated (3:2) AND (7:3) COUNTERS

|  | Area |  | Delay <br> $(\mathrm{ns})$ | Power <br> $(\mu \mathrm{W})$ |
| :---: | :---: | :---: | :---: | :---: |
|  | MOSFETs | SETs |  | 1.0 |
| $(3: 2)$ Counter | 18 | 2 | 2.7 |  |
| $(7: 3)$ Counter | 31 | 3 | 1.5 | 4.1 |

We then construct a $16 \times 16$ multiplier as an example. During the PPA step, 212 units of (3:2) counter (each (2:2) counter is viewed as a (3:2) counter) are needed when using the Dadda's tree structure [73]; while if (7:3) counters are utilized following Dadda's strategy, there will need 40 units of (3:2) counter and 53 units of (7:3) counter (each (6:3), (5:3), and (4:3) counter is treated as a (7:3) counter) [74]. Table 5.4 summarizes the total cost of a $16 \times 16$ multiplier, where the PPG is implemented using CMOS AND gates (this ensures high reliability against BCs ), the PPA is realized based on the elements in Table 5.3, and the CPA is finished through the RCA (implemented using the (3:2) counter as a 1-bit FA or the (7:3) counter as a 2 -bit FA). It is observed from Table 5.4 that the multiplier when employing both (3:2) and (7:3) counters consumes less area, delay and power compared to the one only uses the (3:2) counters which verifies our initial
prediction in section 5.3.

TABLE 5.4 Area-Delay-Power Estimations of a $16 \times 16$ MULTIPLIER using Elements in Table 5.3

|  | Area |  | Delay <br> $(\mathrm{ns})$ | Power <br> $(\mu \mathrm{W})$ |
| :---: | :---: | :---: | :---: | :---: |
|  | MOSFETs | SETs |  | $\sim 780$ |
| (3:2) Counter <br> Only | 8452 | 484 | $\sim 40$ | $\sim 30$ |
| $(3: 2) \&(7: 3)$ <br> Counters | 6924 | 284 | $\sim 500$ |  |

### 5.4.4 Comparisons

To complete the discussion, we compare the binary tree multipliers implemented with different technologies, as shown in Table 5.5, where the multiplier employs both (3:2) and (7:3) counters following the same circuit structure as the above and the power is estimated at the frequency of 100 MHz . For the multiplier based on pure single-electrontunneling technology in [65], we treat each TLG equivalently to 3 SETs so that the area can be evaluated by the number of SETs for easy comparison. Because the TLG is operated at a single-electron precision, the error probability (i.e., $P_{\text {error }}$ ) is so important that the delay is calculated by the equivalent RC constant with a certain order of magnitude (i.e., factor $-\ln \left(P_{\text {error }}\right)$, where $P_{\text {error }}=10^{-8}$ ). For SET/MOS hybrid circuits where electrons keep tunneling into and out of the island of SET, there is a tunneling current and the analytical model of SET can be used for the delay estimation [70, 49, 51] which is actually the simple RC constant.

TABLE 5.5 AREA-DELAY-POWER ESTIMATIONS OF A $16 \times 16$ MULTIPLIER using Different Technologies

|  | Area |  | Delay <br> (ns) | Power |
| :---: | :---: | :---: | :---: | :---: |
|  | MOSFETs | SETs |  | $\sim 130$ |$\sim 10 \mathrm{nW} ~\left(\begin{array}{c}\text { Pure SET [65] }\end{array}\right.$

TABLE 5.6 TEmperature and BC Performances of Single-Electron TunNELING BASED MULTIPLIERS

|  | Temperature | Reliability against BCs |
| :---: | :---: | :---: |
| Pure SET [65] | $<10 \mathrm{~K}$ | Not reliable |
| Hybrid MOS and <br> SET [69] | 77 K | Less reliable (tolerant BCs <br> up to $\pm 0.05 e)$ |
| This paper | 300 K | Quite reliable (tolerant BCs <br> up to $\pm 0.2 e$ ) |

It is observed from Table 5.5 that pure SET-based multiplier (SET equivalent) consumes extremely small area (the size of SET is much smaller than the size of MOSFET) and power but the delay is substantial; the pure MOSFET-based multiplier (with 65 nm technology) is very fast but requires a lot of area and power; the performance of hybrid MOS and SET multiplier lies in the middle. Notice that the proposed SET/MOS hybrid multiplier (the one uses both (3:2) and (7:3) counters) consumes more power than the one in [69] with comparable area and less delay. The increased power dissipation
stems from the fast operating speed at higher temperature. Table 5.6 shows the performances of multipliers involving the usage of SETs in terms of operating temperature and reliability against BCs. The proposed multiplier is able to work at room temperature and exhibits the high immunity against BCs , hence provides a practical solution for nanometer-scale integration.

Compared to pure MOSFET-based multiplier, the speed of the proposed multiplier is much slower with the area and power dissipation to be reduced by about $50 \%$. It should be mentioned that the power dissipation of the CMOS multiplier (dominated by the dynamic power) significantly increases with further increased frequency, while for the proposed multiplier, it remains nearly constant (dominated by the static power). At the frequency of 300 MHz , the power dissipation of the proposed multiplier is just about $16.7 \%$ of that of the CMOS multiplier. The proposed multiplier is quite appealing for low-power and low-speed applications.

### 5.5 Summary

We have proposed multi-input counters for binary tree multipliers using hybrid MOS and SET architectures based on phase modulation scheme. Thanks to Coulomb blockade oscillation of SET, the primitive type (3:2) and (7:3) counters are very simple which require only a few MOSFETs and several multi-input-gate SETs. To solve the practical issues associated with the SET/MOS hybrid circuits, we introduce the enhanced type (7:3) counter (also applied to the (3:2) counter) which works at room temperature with 1.5 ns delay and $4.1 \mu \mathrm{~W}$ power dissipation (at the frequency of 100 MHz ), and is able to tolerant BCs up to $0.2 e$. The proposed (7:3) counter can be alternatively used as a 2-bit FA for the

CPA which further reduces the area and delay of a multiplier. The multiplier when employing both (3:2) and (7:3) counters consumes less area, delay and power compared to the one only uses the (3:2) counters which is in contrast to CMOS technology.

## Chapter 6

## SET/MOS Hybrid Frequency Synthesis for Arithmetic Applications

### 6.1 Introduction

Hybrid MOS and SET architecture has been studied widely. A variety of functional circuits have been realized using such a structure. However, one of the biggest challenges facing the SET is the random background charge effect [25], which limits the application of SET mainly in the field of memory design [27]. For logic applications, SET-based circuits are sensitive to random BCs, which are inherent on the islands of SET and may lead to circuit malfunction. While it is possible to design SET logic circuits with certain redundancy or error correction [75], the hardware overhead makes these schemes less attractive. Since BCs only change the phase of Coulomb blockade oscillation with no effect on its periodicity and amplitude, SET logic circuits can become highly immune to these charges if the information is modulated into the frequency or amplitude of this oscillation [25, 76].

In this chapter, we first discuss SET based frequency synthesis including frequency gain and frequency mixing, followed by the design of SET/MOS hybrid frequency
synthesizer. Thanks to Coulomb blockade oscillation of SET, the proposed frequency synthesizer is much simpler compared to their CMOS counterparts which require a lot more transistors. Based on this frequency synthesizer, we then present a new design methodology for arithmetic operations using frequency modulation technique. The main idea is to first convert the operands from digital to frequency representation, then perform arithmetic operations in the frequency domain before converting the result back to the digital representation.

The advantages of the designed arithmetic circuits are:

1) Compared with conventional CMOS technology, the circuit structures are simple and hence consume less area and power;
2) Compared with SET-based circuits operating in the time domain [54-70, 77], the proposed circuits are less sensitive to random BCs and are able to work at room temperature.

This chapter is organized as follows. In section 6.2, we introduce SET's frequency properties including frequency gain and frequency mixing, followed by sawtooth/ reverse-sawtooth wave generation which is required for SET-based frequency synthesis. Then, we present a SET/MOS hybrid frequency synthesizer (FSR) for signal processing in the frequency domain. Section 6.3 provides details about circuit implementations for arithmetic operations, including the design of digital-to-frequency converter (DFC), frequency-modulated arithmetic circuits, and frequency-to-digital converter (FDC). In section 6.4, we show some simulation results along with discussions in terms of background charge effect, temperature effect, and other practical considerations. In the end, section 6.5 concludes the chapter.

### 6.2 SET Based Frequency Synthesis

Frequency synthesis refers to a set of operations in the frequency domain, including frequency multiplication and frequency mixing (i.e., a process that generates sum and difference frequencies). While these can be generally realized by using a phase locked loop (PLL) and mixer, there are still many design challenges ahead. Thanks to Coulomb blockade oscillation, however, SET devices with a sawtooth or reverse-sawtooth voltage as their input exhibit very good frequency properties and hence provide an interesting solution for frequency synthesis.

### 6.2.1 Frequency Gain

A simple SET device is able to achieve the frequency gain which, analogous to the voltage gain of MOSFET, is defined as the ratio of the output frequency at drain terminal to the input frequency at gate terminal. Consider a constant current biased SET where $V_{D S}$ oscillates with respect to $V_{G S}$, as shown in Figure 6.1 (a), where SET's drain and source junction resistance $R_{T D}=R_{T S}=1 \mathrm{M} \Omega$ and capacitance $C_{T D}=C_{T S}=0.1 \mathrm{aF}$, gate capacitance $C_{G}=C_{G 2}=0.1 \mathrm{aF}$, biasing current $I_{\text {Bias }}=30 \mathrm{nA}$, second gate voltage $V_{G S 2}=0$, and load capacitance $C_{\text {Load }}=10 \mathrm{fF}$. It is observed from Figurer 6.1 (b) that the amplitude and periodicity of $V_{D S}$ oscillation with respect to $V_{G S}$ are 240 mV and 1.6 V , respectively (note that the second gate of SET is also shown here for future discussions). The load capacitance has to be relatively large so as not to affect $V_{D S}$.

Throughout this chapter, the above parameter values are used for SET, unless otherwise specified. With such a simple configuration, one can easily realize the frequency gain as well as frequency mixing operation.

(a)

(b)

Figure 6.1: (a) Constant current biased SET with two gate terminals; (b) The voltage oscillation of $V_{D S}$ vs. $V_{G S}$ at room temperature.

If $V_{G S}$ is a ramp voltage that linearly increases over time, the voltage oscillation of $V_{D S}$ vs. $V_{G S}$ is then transformed to a time-domain periodic signal. Since every $e / C_{G}$ increment of $V_{G S}$ produces a complete cycle of $V_{D S}$, this time interval corresponds to the period of $V_{D S}\left(\right.$ i.e., $\left.T_{D S}\right)$. The frequency of $V_{D S}$ (i.e., $f_{D S}=1 / T_{D S}$ ) is therefore given by

$$
\begin{equation*}
\delta=\frac{\Delta V_{G S}}{\Delta t}=\frac{e / C_{G}}{T_{D S}}=\frac{e / C_{G}}{1 / f_{D S}} \Rightarrow f_{D S}=\frac{C_{G} \cdot \delta}{e} \tag{6.1}
\end{equation*}
$$

where $\delta$ is the slope of ramp $V_{G S}$ with the unit of V/s. Figure 6.2 (a) shows the time domain $V_{D S}$ oscillation based on the ramp input $V_{G S}$. For instance, with $C_{G}=0.1 \mathrm{aF}$ and $\delta$ $=1.6 \mathrm{~V} / \mu \mathrm{s}$, the frequency of $V_{D S}\left(\right.$ i.e., $\left.f_{D S}\right)$ is 1 MHz .

Instead of applying a ramp signal $V_{G S}$, a sawtooth wave can be used to generate the same $V_{D S}$ oscillation, as shown in Figure 6.2 (b) where the amplitude and frequency of $V_{G S}$ is 1.6 V (i.e., $e / C_{G}$ with $C_{G}=0.1 \mathrm{aF}$ ) and 1 MHz , respectively. The slope of $V_{G S}$ in each period of the sawtooth wave is the same as that of ramp $V_{G S}$ used in Figure 6.2 (a). In this case, each period of $V_{G S}$ generates a complete cycle of $V_{D S}$ that repeats itself with end-toend periodically, hence making $V_{D S}$ a pseudo-periodic signal with the same frequency as $V_{G S}$. With a sawtooth input $V_{G S}$, one is able to achieve the frequency gain (i.e., $G_{f}=f_{D S} /$ $\left.f_{G S}\right)$. Assuming the amplitude of $V_{G S}$ (i.e., $A_{G S}$ ) is $N \cdot e / C_{G}$, where $N$ must be an integer which ensures integral $V_{D S}$ cycles for each period of $V_{G S}$, the frequency of $V_{D S}$ based on (6.1) is then derived as

$$
\begin{equation*}
f_{D S}=\frac{C_{G} \cdot \delta}{e}=\frac{C_{G}}{e} \cdot \frac{A_{G S}}{1 / f_{G S}}=\frac{C_{G}}{e} \cdot \frac{N \cdot e}{C_{G}} \cdot f_{G S}=N \cdot f_{G S} \tag{6.2}
\end{equation*}
$$



Figure 6.2: Time domain $V_{D S}$ oscillation for the SET of Figure 6.1 based on ramp $V_{G S}$ with slope of $1.6 \mathrm{~V} / \mu \mathrm{s}$ (a); sawtooth $V_{G S}$ with the amplitude and frequency of 1.6 V and $1 \mathrm{MHz}(\mathrm{b})$; sawtooth $V_{G S}$ with the amplitude and frequency of 3.2 V and 1 MHz (c); and sawtooth $V_{G S}$ the same as the one in (b) but with $C_{G}=0.2 \mathrm{aF}$ for SET (d).

On the other hand, if the amplitude of $V_{G S}$ is fixed at $e / C_{G}$, SET's input gate capacitance has to be $N \cdot C_{G}$ in order to get the frequency gain of $N$. Figure 6.2 (c) and (d) show the $V_{D S}$ oscillations with frequency gain of 2 . For Figure 6.2 (c), $C_{G}=0.1 \mathrm{aF}$ and $A_{G S}=3.2 \mathrm{~V}=2 \cdot e / C_{G}$, so $G_{f}=2$. For Figure $6.2(\mathrm{~d}), C_{G}=0.2 \mathrm{aF}$ and $A_{G S}=1.6 \mathrm{~V}=2 \cdot e / C_{G}$, which results in the same $G_{f}$. Note that the amplitude of $V_{D S}$ oscillation in Figure 6.2 (d) is decreased which is the result of increased $C_{\Sigma}$ with a larger value of $C_{G}$.

### 6.2.2 Frequency Mixing

A SET device with two input gates is able to achieve the frequency mixing operation. To understand how frequencies are mixed through an SET, we express the potential of the island as (for the SET in Figure 6.1 (a))

$$
\begin{equation*}
V_{\text {Isand }}=\frac{C_{G}}{C_{\Sigma}} V_{G S}+\frac{C_{G 2}}{C_{\Sigma}} V_{G S 2}+\frac{C_{T D}}{C_{\Sigma}} V_{D S}-\frac{k \cdot e}{C_{\Sigma}} \tag{6.3}
\end{equation*}
$$

where $k \cdot e$ is net charges on the island. If both $k$ and $V_{D S}$ are constant, differentiating (6.3) will lead to

$$
\begin{equation*}
C_{\Sigma} \cdot \Delta V_{\text {Island }}=C_{G} \cdot \Delta V_{G S}+C_{G 2} \cdot \Delta V_{G S 2} \tag{6.4}
\end{equation*}
$$

In reality, $k$ is not fixed. Once $V_{\text {Island }}$ (with respect to the source) is greater than $e / C_{\Sigma}$, one more electron will be trapped in the island (i.e., $k$ increases by one), forcing $V_{\text {Island }}$ to drop by $e / C_{\Sigma}$. Therefore, $V_{\text {Island }}$ as a result of linearly increasing the gate voltage is a sawtooth wave whose amplitude is $e / C_{\Sigma}$. It is understood that with a full swing of $V_{\text {Island }}$, the tunneling current (because of constant $V_{D S}$ ) experiences a complete cycle, which means that the frequency of $V_{\text {Island }}$ equals to the frequency of tunneling current (i.e., $f_{T C}$ ). The
slope in each period of $V_{\text {Island }}$ can be therefore written as $\Delta V_{\text {Island }}=\left(e / C_{\Sigma}\right) \cdot f_{T C}$. On the other hand, if $V_{G S}$ and $V_{G S 2}$ are sawtooth voltages (assuming the amplitude and frequency for $V_{G S}$ are $N \cdot e / C_{G}$ and $f_{G S}$, and the amplitude and frequency for $V_{G S 2}$ are $M \cdot e / C_{G 2}$ and $\left.f_{G S 2}\right)$, their slopes in each period are then represented by $\Delta V_{G S}=\left(N \cdot e / C_{G}\right) \cdot f_{G S}$ and $\Delta V_{G S 2}$ $=\left(M \cdot e / C_{G 2}\right) \cdot f_{G S 2}$. With $V_{G S}$ and $V_{G S 2}$ being applied simultaneously, substituting derivations of $\Delta V_{\text {Island }}, \Delta V_{G S}$, and $\Delta V_{G S 2}$ into (6.4) gives

$$
\begin{equation*}
f_{T C}=N \cdot f_{G S}+M \cdot f_{G S 2} \tag{6.5}
\end{equation*}
$$

If one gate voltage is a sawtooth wave while the other is a reverse-sawtooth wave (i.e., the slope polarities in each period of $V_{G S}$ and $V_{G S 2}$ are opposite), one frequency component would be subtracted from the other.

In terms of constant current biased SET, $V_{D S}$ oscillates with the same frequency as $f_{T C}$, which also equals to the sum or difference of frequencies associated with two input gate voltages. Figure 6.3 shows two $V_{D S}$ oscillations for the constant current biased SET of Figure 6.1 (a), where the gate capacitances of SET are set to $C_{G}=0.2 \mathrm{aF}$ and $C_{G 2}=0.4 \mathrm{aF}$. Since the amplitudes of $V_{G S}$ and $V_{G S 2}$ are both 1.6 V , the frequency gain factor is 2 for gate1 (i.e., $\left.N=1.6 /\left(e / C_{G}\right)=2\right)$ and 4 for gate2 (i.e., $M=1.6 /\left(e / C_{G 2}\right)=4$ ). For example, with the frequency of $V_{G S}$ and $V_{G S 2}$ being 3 MHz and 2 MHz , respectively, the mixed frequencies of $V_{D S}$ are 14 MHz and 2 MHz , respectively.

Due to the equivalent effect of each gate terminal of SET, the superposition theorem can be used to evaluate the frequency of $V_{D S}$ with reduced complexity. In general, more frequency components can be mixed through SET with multiple gate terminals.


Figure 6.3: Time domain $V_{D S}$ oscillations for the SET of Figure 6.1 where $C_{G}=0.2 \mathrm{aF}, C_{G 2}=$ 0.4 aF , the amplitude of $V_{G S}$ and $V_{G S 2}$ is 1.6 V , the frequencies of $V_{G S}$ and $V_{G S 2}$ are 3 MHz and 2 MHz respectively. Both $V_{G S}$ and $V_{G S 2}$ are sawtooth waves in (a) while the reverse-sawtooth wave for $V_{G S}$ and sawtooth wave for $V_{G S 2}$ in (b).

### 6.2.3 Sawtooth/Reverse-Sawtooth Wave Generation

SET-based frequency gain and frequency mixing require the use of sawtooth and reverse-sawtooth waves. Through the configuration on slope of Coulomb oscillation, an SET device is able to generate a reverse-sawtooth wave, which, if passing through a voltage amplifier with gain of -1 , becomes a sawtooth wave. For a constant current biased SET working at near absolute temperature, the amplitude of $V_{D S}$ oscillation with respect to $V_{G S}$ is $e / C_{\Sigma}$ with positive and negative slopes being $C_{G} /\left(C_{\Sigma}-C_{T D}\right)$ and $-C_{G} / C_{T D}$, respectively. While these values will attenuate at higher temperature, they can still be used to predict SET's performance. This implies that if $C_{T D}$ dominants SET's device capacitances such that $C_{\Sigma} \approx C_{T D}$, the positive slope goes to infinity, making $V_{D S}$ oscillation a reverse-sawtooth wave. Consider the second gate of a current biased SET to be short-connected to the drain terminal, as shown in Figure 6.4 (a). With $V_{G S 2}=V_{D S}$, the potential on the island from (6.3) becomes

$$
\begin{equation*}
V_{I s l a n d}=\frac{C_{G}}{C_{\Sigma}} V_{G S}+\frac{C_{T D}+C_{G 2}}{C_{\Sigma}} V_{D S}-\frac{k \cdot e}{C_{\Sigma}} \tag{6.6}
\end{equation*}
$$

Thus, the parallel-connected SET's second gate and drain junction can be viewed equivalently as one junction with the capacitance of $C_{T D}+C_{G 2}$. The positive and negative slopes of $V_{D S}$ oscillation is then estimated as $C_{G} /\left(C_{\Sigma}-C_{T D}-C_{G 2}\right)$ and $-C_{G} /\left(C_{T D}+C_{G 2}\right)$. This equivalence can be better understood from the feedback point of view. By introducing $V_{D S}$ as a feedback voltage applied to the second gate, there will be a phaseshift on $V_{D S}$ itself. Since $V_{D S}$ is a periodic signal, the amount of phase-shift (proportional
to the second gate voltage) varies from peak to valley points. The difference in phaseshift results in the change in slope of $V_{D S}$ oscillation.

Figure 6.4 (b) shows $V_{D S}$ oscillations without and with feedback (see curves A and B, respectively), where dashed curves are shifted versions of curve A with different values of $V_{G S 2}$ being indicated by the horizontal lines. Here, curve B converges to the points where $V_{D S}$ and $V_{G S 2}$ are equal.

More changes in slope of $V_{D S}$ oscillation can be expected if there is a voltage gain (say, $G_{v}$ ) between SET's second gate and drain terminals, as shown in Figure 6.5 (a) where $V_{G S 2}=G_{v} \cdot V_{D S}$. According to (6.3), the equivalent drain junction capacitance of SET is $C_{T D}+G_{v} \cdot C_{G 2}$, which (assuming $G_{v}>1$ ) further pushes the positive slope to climb up and the negative slope to reduce. Again, from a feedback perspective, the amplified $V_{G S 2}$ enlarges the difference of the phase-shift from peak to valley of $V_{D S}$ oscillation. If $G_{v}$ is large enough so that the above difference equals to $e \cdot\left(C_{\Sigma}-C_{T D}\right) / C_{G} C_{\Sigma}$ (i.e., the amplitude of $V_{D S}$ oscillation divided by the positive slope), $V_{D S}$ and $V_{G S 2}$ become reversesawtooth waves.

Figure 6.5 (b) shows $V_{D S}$ oscillations with enhanced feedback strength, where $G_{v}$ varies from 1 to 8 with increment of 1 . It can be seen from the figure that once $G_{v}>4$, SET enters the deep feedback region, where the amplitude of $V_{D S}$ goes down for further increase in $G_{v}$ while the amplitude of $V_{G S 2}$ remains nearly constant regardless of the change of $G_{v}$. In other word, as long as SET is in the deep feedback region, $V_{G S 2}$ is pretty much stabilized.

(b)

Figure 6.4: (a) Current biased SET with a short-connection between the drain and second gate terminals (load capacitor exists but not shown here); (b) $V_{D S}$ oscillations without (i.e., curve A) and with (i.e., curve B) the feedback, where dashed curves are shifted versions of curve A with $V_{G S 2}=120 \mathrm{mV}, 180 \mathrm{mV}, 240 \mathrm{mV}, 300 \mathrm{mV}$ and 360 mV (from right to left).

(a)

(b)

Figure 6.5: (a) Constant current biased SET with enhanced feedback strength; (b) $V_{D S}$ and $V_{G S 2}$ oscillations, where $G_{v}$ increases from 1 to 8 with the step size of 1 .

### 6.2.4 SET/MOS Hybrid Frequency Synthesizer (FSR)

Based on previous discussions, we look at circuit implementation of frequency synthesizer. Figure 6.6 (a) shows a schematic which adopts hybrid MOS and SET architecture, where both $\mathrm{A}_{1}$ and $\mathrm{A}_{2}$ are voltage amplifiers that can be implemented using CMOS differential pairs. By taking advantage of SET's frequency properties, the input frequencies in this figure (i.e., $f_{0}, f_{l}, \ldots, f_{n-1}$ ) are first amplified and mixed through multiple input gates of SET. $\mathrm{A}_{1}$ in the feedback loop amplifies the amplitude of $V_{D S}$ oscillation without changing its voltage polarity. The output of $\mathrm{A}_{1}$ (i.e., $V_{\mathrm{fb}}$ ) is fed to SET's second gate in order to generate a reverse-sawtooth wave. $\mathrm{A}_{2}$ further amplifies the amplitude of $V_{\mathrm{fb}}$ which also changes its voltage polarity. With the help of $\mathrm{A}_{1}$ and $\mathrm{A}_{2}$, the circuit is able to generate matched input and output which enables cascaded FSR structures for signal processing.

Figure 6.6 (b) shows a circuit symbol for SET/MOS hybrid frequency synthesizer, where $C_{G}$ at the right bottom corner indicates that the amplitude of both input and output sawtooth waves is $e / C_{G}$, and $x_{0}, x_{1}, \ldots, x_{n-l}$ on the left side correspond to the frequency gain factors. The output frequency is thus given by

$$
\begin{equation*}
f_{o u t}=x_{0} \cdot f_{0}+x_{1} \cdot f_{1}+\ldots+x_{n-1} \cdot f_{n-1} \tag{6.7}
\end{equation*}
$$

Note that if any particular input is a reverse-sawtooth wave, the corresponding frequency component in (6.7) should change its sign. For illustration purpose, SET shown here has $n$ input gates. For practical implementation, however, the number of SET's input gates is limited due to the upper bound of $C_{\Sigma}$ for room-temperature operation.

(a)

(b)

Figure 6.6: (a) Implementation of SET/MOS hybrid frequency synthesizer (FSR); (b) Symbol of SET/MOS hybrid frequency synthesizer (FSR).

### 6.3 Frequency Modulated Arithmetic Operations

The block diagram of arithmetic operations using frequency modulation is shown in Figure 6.7, which involves the design of digital-to-frequency converter (DFC), frequency-modulated arithmetic circuits, and frequency-to-digital converter (FDC). All these components are based on SET/MOS hybrid frequency synthesizer (FSR) presented in previous section.


Figure 6.7: Block diagram of frequency modulated arithmetic operations.

### 6.3.1 Digital-to-Frequency Converter (DFC)

The design of DFC is based on FSR along with NMOS switches. Figure 6.8 shows the schematic and symbol of a 3-bit DFC, where a sawtooth input is connected to FSR through three NMOS switches controlled by a 3-bit binary operand (i.e., $d_{2} d_{1} d_{0}$ ). The FSR has three input gates for SET, and the associated capacitances are configured as 1,2 and 4 times of $C_{G}$. With input frequency being $f_{\text {in }}$, the output frequency is expressed as

$$
\begin{equation*}
f_{\text {out }}=\left(2^{2} d_{2}+2^{1} d_{1}+2^{0} d_{1}\right) \cdot f_{\text {in }}=D_{3} \cdot f_{\text {in }} \tag{6.8}
\end{equation*}
$$

where $D_{3}$ represents the evaluation (i.e., decimal value) of a 3-bit digital operand, and the
subscript denotes the number of bits. The node capacitance between NMOS and SET devices is much larger ( $\sim \mathrm{fF}$ ) than SET's input gate capacitance $(\sim \mathrm{aF})$, and hence has negligible effects on the output frequency.

Since the input gate capacitance of SET associated with each bit of the digital operand depends exponentially on bit's weight, the total device capacitance of SET (i.e., $C_{\Sigma}$ ) for multiple-bit DFC will become considerably large. This puts a limit on the number of bits for the DFC operating at room temperature. To overcome this limitation, multiple-bit DFCs can be built using several small ones. Figure 6.9 shows examples of 4-bit, 6-bit and 8-bit DFCs that use 3-bit DFC as a basic building block.

(a)

(b)

Figure 6.8: (a) Implementation of a 3-bit digital-to-frequency converter (DFC); (b) Symbol of a 3-bit digital-to-frequency converter (DFC).

(a)

(b)

(c)

Figure 6.9: Implementations of a 4-bit (a), 6-bit (b), and 8-bit (c) DFC.

### 6.3.2 Frequency-Modulated Arithmetic Circuits

One of the advantages of converting a digital operand to frequency representation is the simplicity of performing multiplication in frequency domain. By connecting two DFCs serially, as shown in Figure 6.10 (a) where each DFC accepts one $n$-bit digital operand, the product of two operands is modulated into the output frequency (i.e., $f_{\text {out }}=$ $\left.A_{n} \cdot B_{n} \cdot f_{\text {in }}\right)$. If more stages of DFC are cascaded, multiplication for multiple operands can also be achieved using such a simple structure.

Frequency division can be implemented using a phase locked loop (PLL), as shown in Figure 6.10 (b) where a $2 n$-bit dividend is applied to the DFC in the forward path while a $n$-bit divider is applied to the DFC in the feedback path. The PLL consists of phase frequency detector (PFD), charge pump (CP), low pass filter (LPF), and voltage controlled oscillator (VCO). At steady state, two input frequencies of PFD are locked, producing VCO's output frequency of $\left(A_{2 n} / B_{n}\right) \cdot f_{\text {in }}$ which incorporates the information of both quotient and reminder. Note that the output of VCO has to be a sawtooth wave with the amplitude of $e / C_{G}$.

Figure 6.10 (c) shows the implementation of frequency addition, where two $n$-bit digital operands are first modulated into frequencies through two DFCs, which are then added together with the help of FSR. Because the FSR in this circuit has unity gain for each input frequency, the output frequency is given by $\left(A_{n}+B_{n}\right) \cdot f_{i n}$. If one inserts a voltage amplifier with gain of -1 between one of the DFCs and FSR (convert a sawtooth wave to a reverse-sawtooth wave), a frequency subtraction operation could be achieved with the output frequency of $\left|A_{n}-B_{n}\right| \cdot f_{i n}$.

(a)

(b)

(c)

Figure 6.10: Implementations of frequency multiplication (a), frequency division (b), and frequency addition (c).

### 6.3.3 Frequency-to-Digital Converter (FDC)

After performing arithmetic operations in frequency domain, the results have to be converted back to digital representation. This can be done with a binary counter. By counting the number of cycles at the output during the time period of $1 / f_{\text {in }}$, the counter will generate the frequency-modulated computation result in digital format (except for division operation where the output frequency may not be multiples of the input frequency).

An alternative way of doing frequency-to-digital conversion is to use a frequency comparator. One-bit frequency comparator can be implemented using a D flip-flop with a delay unit, as shown in Figure 6.11 (a), where the delay (i.e., $t_{d}$ ) sets the threshold frequency (i.e., $f_{t h}=1 / 2 t_{d}$ ). If the input frequency is greater than $f_{t h}$, at each rising edge of clock signal, $d_{\text {out }}$ turns out to be logic 1 . Otherwise, $d_{\text {out }}$ is logic 0 , as shown in Figure 6.11 (c). Some research groups have proposed flash type frequency based ADC using such a frequency comparator [78]. Similar to voltage based flash type ADC, a group of 1bit frequency comparators (their threshold frequencies differ slightly) are used to generate a thermometer code which is further encoded into a binary number through another digital circuitry. The circuit consumes less power and is able to operate at very high speed. However, it requires a large number of frequency comparators (i.e., $2^{n}-1$ units for $n$-bit output). Also, it could be a big challenge to precisely control the delay.

In this work, we propose a pipeline type frequency based ADC , where the residue frequency for each stage irritation is generated with the help of SET/MOS hybrid frequency synthesizer (FSR).


Figure 6.11: One bit frequency comparator (a) and its symbol (b) as well as the frequency comparisons under different input conditions (c)

Figure 6.12 (a) shows the circuit implementation of one stage in the pipeline structure based on 1-bit frequency comparator. The FSR used here has two input gates for SET. The input with frequency gain factor of one is connected to the bias signal (i.e., a reversesawtooth wave with the frequency of $f_{\text {Bias }}$ and amplitude of $e / C_{G}$ ) through an NMOS switch controlled by $d_{\text {out }}$, while the other input with frequency gain factor of two is fed by the input signal (i.e., a sawtooth wave with the frequency of $f_{\text {in }}$ and amplitude of $e / C_{G}$ ) which is also connected to a 1-bit frequency comparator through a buffer that changes the sawtooth wave into a square wave. With the dynamic range of $f_{\text {in }}$ from $f_{\text {ref }}^{-}$to $f_{\text {ref }}{ }^{+}, f_{\text {Bias }}$ and $f_{\text {th }}$ of Figure $6.11\left(\right.$ a) is given by $\left(f_{\text {ref }}^{+}-f_{\text {ref }}{ }^{-}\right)$and $\left(f_{\text {ref }}^{-}+f_{\text {ref }}{ }^{+}\right) / 2$, respectively. If $f_{\text {in }}<f_{\text {th }}$, then $d_{\text {out }}=0$. The NMOS switch turns off, and $f_{\text {Bias }}$ is not applied to FSR, leading to $f_{\text {out }}=2 f_{\text {in }}$, however, if $f_{\text {in }}>f_{\text {th }}$, then $d_{\text {out }}=1$, making NMOS switch on, which results in $f_{\text {out }}=2 f_{\text {in }}-f_{\text {Bias }}$. In other words, we have

$$
\begin{align*}
& d_{\text {out }}=\left\{\begin{array}{lll}
0 & \text { if } & f_{\text {in }}<f_{\text {th }} \\
1 & \text { if } & f_{\text {in }}>f_{\text {th }}
\end{array}\right. \\
& f_{\text {out }}=\left\{\begin{array}{lll}
2 f_{\text {in }} & \text { if } & d_{\text {out }}=0 \\
2 f_{\text {in }}-f_{\text {Bias }} & \text { if } & d_{\text {out }}=1
\end{array}\right. \tag{6.9}
\end{align*}
$$

Note that due to the positive sign of $f_{\text {out }}\left(2 f_{\text {in }}>f_{\text {Bias }}\right.$ with the condition of $\left.f_{\text {in }}>f_{\text {th }}\right)$, the output of FSR is a sawtooth wave as well. Figure 6.12 (b) shows the circuit symbol for a 1-bit FDC. By connecting multiple 1-bit FDCs in series, we realize an $n$-bit FDC, as shown in Figure 6.12 (c) where $f_{\text {out }}$ from previous stage is directly connected to $f_{\text {in }}$ in the next stage and all stages are driven by a same $f_{\text {Bias }}$. This $n$-bit pipeline type FDC requires only $n$ 1-bit frequency comparators with the same threshold frequency. The resolution of pipeline type FDC can be improved by cascading more stages of 1-bit FDC.


Figure 6.12: Frequency comparator based one-bit FDC (a) and its symbol (b) as well as frequency comparator based $n$-bit FDC (c).

### 6.4 Simulation Result and Discussions

To verify the proposed designs, we simulated a 3-bit DFC (refer to Figure 6.6 and Figure 6.8) which is a basic building block for large DFCs. The parameters for SET are the same as those in Figure 6.1 (a). With $C_{G}=0.1 \mathrm{aF}$, the amplitude of sawtooth wave $V_{G S}$ turns out to be 1.6 V (i.e., varies from 0 to 1.6 V ). The increased $C_{\Sigma}$ results in decreased $V_{D S}$ which at room temperature oscillate from 113 mV to 133 mV with amplitude of 20 mV . The voltage gain of $\mathrm{A}_{1}$ is 50 , which keeps SET in the deep feedback region and generates a reverse-sawtooth $V_{\mathrm{fb}}$ with amplitude of $1 \mathrm{~V}\left(V_{\mathrm{fb}}\right.$ changes from 0 to 1 V with $V_{C M I}$ being $113 \mathrm{mV})$. The voltage gain of $\mathrm{A}_{2}$ is 1.6 , producing matched input and output sawtooth waves (with $V_{C M 2}$ being grounded).

Figure 6.13 shows output voltage oscillations of 3-bit DFCs cascaded by three stages with the input reference frequency being 1 MHz . The digital operand of each stage is configured as 3, 4, and 3. Each stage outputs multiple oscillating cycles within one period of the input, depending upon the specified digital operand. As can be seen from the figure, there is voltage distortions on $V_{\text {out } 2}$ and $V_{\text {out } 3}$ associated with the falling edges of $V_{\text {out }}$ and $V_{\text {out } 2}$, respectively. This represents a nonlinearity effect of the sawtooth wave, which can be better observed in Figure 6.14, where $V_{i n}$ is an ideal sawtooth input applied to a DFC and $V_{\text {out }}$ (same frequency as $V_{\text {in }}$ for comparison) is the real sawtooth output which has a finite difference in amplitude with $V_{i n}$. Either reducing the temperature or strengthening the feedback will improve the linearity of the sawtooth output. The voltage distortions on $V_{\text {out } 2}$ and $V_{\text {out } 3}$ compress the voltage oscillating cycles, raising the output frequency, thus have to be smoothed out through low pass filters when performing frequency-to-digital conversion using pipeline type FDC presented in Figure 6.12.


Figure 6.13: Output voltage oscillations of 3-bit DFCs cascaded by three stages with the input reference frequency being 1 MHz and the digital operands of these stages configured as 3,4 , and 3 .


Figure 6.14: Nonlinearity of the sawtooth wave at the output of DFC which has the same frequency as the input. The bottom curve shows the difference between the real and ideal sawtooth outputs.

### 6.4.1 Background Charge Effect

The most important merit of the proposed frequency synthesis is the high immunity to BCs due to the fact that the periodicity of Coulomb blockade oscillation is independent of BCs. Figure 6.15 shows the background charge effect on the output voltage oscillations of Figure 6.13 (only $V_{\text {out }}$ and $V_{\text {out } 2}$ are shown for demonstration), where BCs in the firststage of SET change from 0 to $0.3 e$ at $0.8 \mu \mathrm{~s}$ and from $0.3 e$ to 0 at $2.4 \mu \mathrm{~s}$. It can be seen from the figure that at the time when BCs changes, there is a certain discontinuity on $V_{\text {out }}$, which is further propagated to $V_{\text {out } 2}$. This will cause an error at the digital output if using a counter-based FDC that counts the number of voltage oscillation cycles corresponding to the first or third input period. However, the digital output will represent the correct value if generated from the second input period when the amount of BCs is not changed (stays at $0.3 e$ ). Actually, no matter how much BCs exist, as long as its value keeps constant during the counting process, they will have no effect on the digital output. Since RBCs vary at very low frequency, the digital output is rather reliable if the circuit works at a relatively high frequency.

While BCs might strike a disturbance on $V_{\text {out }}$ and $V_{\text {out }}$, their slopes remains unchanged, keeping the same output frequency (see (6.3) - (6.5)). Therefore, using a frequencycomparator based FDC will produce a more reliable output. The spikes at the digital output due to the change of BCs can be easily removed through a low-pass digital filter.

It is worth mentioning that, for the proposed frequency modulation technique, the output voltage can recover its normal oscillation even if BCs keep staying on the island. This high immunity against the charges can be viewed as a result of the time-redundancy characterized by the proposed design. In contrast, conventional SET circuits using
voltage or current mode will produce erroneous results (depending on the specific logic and the amount of charges) until BCs disappear or become small enough.


Figure 6.15: Output voltage oscillations with BCs in the first-stage of DFC SET changing from 0 to $0.3 e$ at $0.8 \mu \mathrm{~s}$ and from $0.3 e$ to 0 at $2.4 \mu \mathrm{~s}$.

### 6.4.2 Amplitude Effect of Input Sawtooth Wave

For a given input frequency, the amplitude sets the slope of sawtooth wave which determines the output frequency (see (6.1)). Therefore, the amplitude of a sawtooth input is critical for SET-based frequency synthesis. Consider the worst case (i.e., all input digits are 1 's) for an $n$-bit DFC where the amplitude of both input and output sawtooth waves is $e / C_{G}$. A small change (say, $\Delta x$ ) in the amplitude of input (assuming there is no nonlinearity effect) will generate an error in the output frequency (refer to (6.2)):

$$
\begin{equation*}
f_{\text {error }}=\frac{\left(2^{n}-1\right) \cdot C_{G}}{e} \cdot \Delta x \cdot f_{i n} \tag{6.10}
\end{equation*}
$$

Since the output frequency of DFC is digitized, there is no quantization error when performing frequency based ADC. As long as the error frequency of (6.10) is less than half of the input frequency, the variation in input amplitude will have no impact on the digital output. The maximum tolerant amplitude variation is thus given by

$$
\begin{equation*}
\left.\Delta x\right|_{\max }<\frac{e / C_{G}}{2 \cdot\left(2^{n}-1\right)} \tag{6.11}
\end{equation*}
$$

For instance, if the input amplitude is 1.6 V with $C_{G}=0.1 \mathrm{aF}$ and $n=3,\left.\Delta x\right|_{\max }$ is less than 114 mV . This means that the maximum tolerant amplitude variation for a 3-bit DFC is $7.14 \%$. However, from (6.11), $\left.\Delta x\right|_{\text {max }}$ decreases exponentially with $n$, down to only 3 mV for $n=8$. With the input amplitude of 1.6 V , the maximum tolerant variation is within $0.2 \%$ only. This indicates that the input amplitude is required to be very accurate when designing DFC with more bits. Since $\left.\Delta x\right|_{\max }$ in (6.11) is independent of $f_{i n}$, high speed operation can be achieved by choosing a large input reference frequency which is
limited only by the pole of voltage amplifier used in FSR.

### 6.5 Summary

We have proposed SET-based frequency synthesis which takes advantage of unique Coulomb blockade oscillation to implement arithmetic operations using hybrid SET/MOS architectures. The frequency synthesis mainly consists of frequency gain and frequency mixing. The former is obtained by applying a sawtooth wave to SET's input gate, while the latter is achieved by using multiple sawtooth inputs. In order to generate the required sawtooth waves, a feedback structure has been introduced and discussed. We have also presented an SET/MOS hybrid frequency synthesizer - a hardware implementation for frequency synthesis - which allows us to use frequency modulation technique for arithmetic circuit design, including design of digital-to-frequency converter, arithmetic operations in frequency domain, and frequency-to-digital converter. As shown during the simulation and discussion, the main benefits of using frequency synthesis for this application lie in a) the high immunity against background charges on island of SET, and b) the simple implementation of arithmetic operations in frequency domain.

## Chapter 7

## Conclusions and Future Work

### 7.1 Conclusions

In this thesis, we have studied the Coulomb blockade oscillation characteristic of SET in detail, and fully utilized such characteristic for the design of arithmetic circuits, including adders and multipliers. Since pure SET-based circuits suffer from low current driveability, small voltage gain and low temperature operation, hybrid MOS and SET architectures have been used as the basic building blocks throughout the thesis in order to provide practical solutions for the nanometer-scale integration.

To increase the circuit robustness against BCs, an adaptive feedback has been introduced to the SET/MOS hybrid architecture which offsets the background charge effect by applying an appropriate voltage through an additional gate of SET.

Three implementations of 1-bit FA have been presented using SET/MOS hybrid architectures based on the schemes of multiple-valued logic, phase modulation, and frequency modulation. Thanks to the Coulomb blockade oscillation characteristic of SET, the structure of the proposed 1-bit FAs requires only a few MOSFETs and SETs.

Furthermore, the phase modulation and frequency modulation schemes have been studied in more detail. Multi-input counters used for the binary tree multipliers have been implemented using SET/MOS hybrid architectures based on the phase modulation scheme. By using an input capacitor array, phase adjustment scheme, and parallel SETMOS followed by a CMOS inverter structure, the enhanced type of phase modulated counters is able to work at room temperature with improved reliability against BCs and increased operating speed.

The frequency modulation scheme has been used to realize arithmetic operations following a novel design methodology. Because SET exhibits a good frequency property, including frequency gain and frequency mixing, the proposed frequency modulated arithmetic operations are easy to implement. Since the information is processed in the frequency domain, the circuit operation exhibits the high immunity against BCs.

### 7.2 Future Work

The phase adjustment scheme for the proposed phase modulated multi-input counters works properly under the condition that BCs on the island of SET are within $\pm 0.25 e$. Since BCs are random in nature with the highest possibility within $\pm 0.3 e$, such requirement depends on the technology improvement.

Also, even though the speed of hybrid counters is improved when employing the parallel SETMOS structure, it is still much slower than the CMOS counterpart. Binary tree multipliers implemented using the proposed hybrid counters can only find applications where the area and power consumption is predominant but the speed is less important. The large delay of SET/MOS hybrid architecture limits the size of multipliers
implemented using the frequency modulation scheme as well. The higher operating speed also depends on further technology improvement.

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## VITA AUCTORIS

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