2010

A Nano-Power Voltage-Controlled Oscillator Design for RFID Applications

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A Nano-Power Voltage-Controlled Oscillator Design for RFID Applications

by

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A Thesis
submitted to the Faculty of Graduate Studies
through the Department of Electrical and Computer Engineering
in Partial Fulfillment of the Requirements for
the Degree of Master of Applied Science at the
University of Windsor

Windsor, Ontario, Canada
August 2010

A Nano-Power Voltage-Controlled Oscillator Design for RFID Applications

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Declaration of Co-Authorship/ Previous Publication

I. Co-Authorship Declaration

I hereby declare that this thesis incorporates materials which are result of joint research, as follows:

In all cases, the primary contributions, derivations, experimental setup, data analysis and interpretation were performed by the author through the supervision of Dr. C. Chen. In addition to supervision, Dr. C. Chen provided the author with the project idea, guidance, and financial support.

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Thesis Chapter	Publication title	Publication status
Chapter 4,5	Suzana Farzeen, Guoyan Ren, Chunhong Chen," An Ultra-Low Power Ring Oscillator for Passive UHF RFID Transponders", in Proc. 53rd IEEE Midwest Symposium on Circuits and Systems, pp. 558-561, Aug. 2010, Seattle, USA.	"accepted" for publication in a lecture session
Chapter 4,5, 6	Chunhong Chen and Suzana Farzeen, "A Nano-Power Ring Oscillator Design for RFID Applications"	to be submitted for publication

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ABSTRACT

Passive RFID (radio frequency identification) transponder is a tiny device that has unique ID information for communication with RFID readers and relies on the reader as a source of power supply. The main components of a typical transponder IC (integrated circuit chip) include antenna, analog front-end circuit and baseband processor, where the system clock is provided by a local oscillator. One of the biggest challenges for the oscillator is to ensure the lowest possible power consumption for passive RFID applications.

This work presents a new two-stage CMOS voltage-controlled ring oscillator (VCO) designed for passive UHF RFID transponders. The goal is to explore the design space for ultra-low power dissipation. A nano-power VCO capable of functioning as a local oscillator for the transponders is obtained by biasing the delay cells to operate in weak inversion region. Further power reduction is achieved by transistor sizing. Designed in a 90-nm CMOS technology, the proposed circuit oscillates with a power supply of 0.3V with frequency tuning characteristics and consumes only 24nW. The center frequency is 5.12MHz and the phase noise is -80.43 dBc/Hz at 10KHz offset.

To my mother

ACKNOWLEDGEMENT

It is a pleasure to convey my gratitude to my advisor Dr. Chunhong Chen for his supervision and guidance throughout this research. His constant encouragement and support has led to the successful completion of this project. I would like to take this opportunity to thank my committee members Dr. Shervin Erfani and Dr. Biao Zhou for their useful suggestions. I gratefully acknowledge Dr. Rashid Rashidzadeh for his advice and support in my academic courses as well as in my research. I would like to express my appreciation to AUTO21 Network of Centers of Excellence, Canada who provided the financial support for this project. Thanks to Dr. Roberto Muscedere for chairing my defense. Many thanks to Ms. Andria Ballo who always helped me with administrative procedures.

I would like to express my gratitude to my uncle Dr. Asad Asaduzzaman and my aunt Rebecca Arzoo who are my family in Canada. Their encouragement and support throughout my two years in Windsor, have led me to achieve this milestone in my life. Many thanks to my cousins Anindita and Arundip. I wish to especially thank my brother and sister in Windsor, Mohammed Sarwer and Dilshad Hussain for all the support and care. My heartfelt appreciation goes to my friends Manjit Kaur and Manjinder Singh for helping me get through the difficult times. At the end, I thank everyone who supported me in any respect to complete this work successfully.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER I

INTRODUCTION

1.1 Radio Frequency Identification (RFID)

Radio Frequency Identification (RFID) technology enables electronic and wireless labeling and identification of objects. Table 1.1 lists the four primary frequency bands which are being used for RFID applications. For LF and HF systems inductive coupling is used to communicate with the reader while for UHF and microwave systems backscatter principle is employed. The reader initiates a communication by transmitting an RF signal, and the tag containing the requested information responds by reflecting back a portion of the interrogating RF wave [13].

Table 1.1: Frequency Allocation for RFID Applications

Band	*Frequency*	*Read Range*	*Application Example*
LF	125 KHz	Few cm	Auto-Immobilizer
HF	13.5 MHz	1m	Building Access
UHF	900 MHz	7m	Supply Chain
Microwave	2.4 GHz	10m	Traffic Toll

1.2 Operational Principle of UHF RFID

The general operational principle is shown in Fig. 1.1 [14]. The concept is to address a number of passive transponders in order to wake up only one of them. The reader sends an N-bit

address (ID) and only the transponder that contains the requested ID wakes up. All steps in a communication session are reader controlled. A successful communication session is divided into three parts:

- *Power-Up Mode:* A reader radiates high-frequency power to the transponders. The power captured by the transponders' antenna is converted to dc power supply that energizes the circuits. In this mode a power-on-reset occurs that turns the transponders to the addressing mode.
- *Addressing Mode:* During the addressing mode, the transponders wait for the reader to send information. The reader sends an ID that is saved by all transponders in their shift registers. If a transponder successfully detects its ID, it switches to the reading mode and modulates its input impedance so that the reader can detect its presence. All other transponders go into quiet mode.

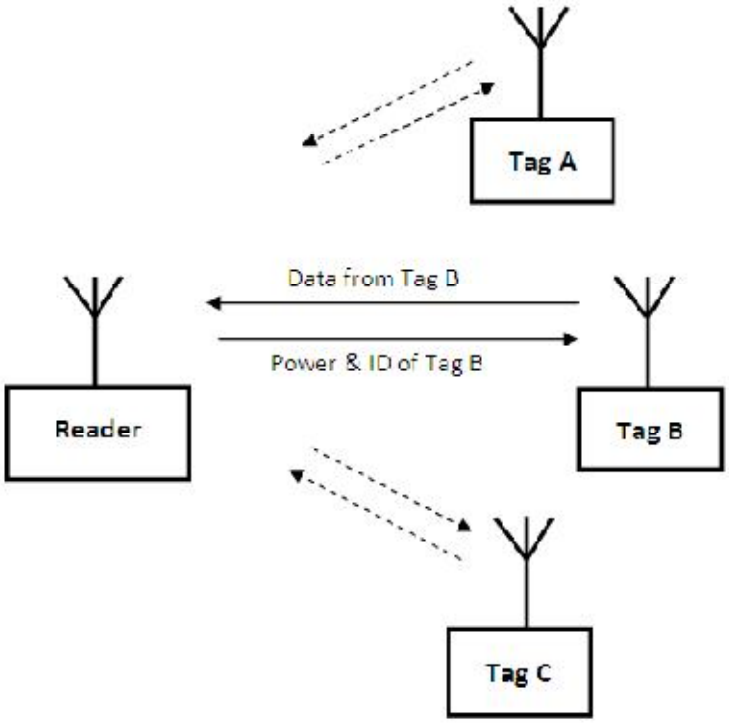


Figure 1.1: Operational principle of UHF RFID

- *Reading Mode:* Only the transponder that successfully detects its ID switches to the reading mode. It modulates its input impedance at an intermediate frequency (typically MHz). The reader detects this modulation and sends RF interrupts, to force the transponder to communicate the next bit of information. If the next bit is a "1", the transponder switches the IF oscillator on and the reader detects the backscattered signal. If the next bit is a "0", the oscillator is turned off and the reader detects the lack of backscattered signal. The reader can then verify the transponder's ID to check if it matches the one sent.

1.3 Transponder Architecture

The RFID transponder is a tiny device that holds certain information about the object it is attached to. It typically consists of an on-chip circuitry, antenna and memory. The whole device can be encapsulated in different materials depending upon application. There are three different types tags as discussed below:

- *Passive Tags:* A passive RFID transponder is a tiny device that operates without any power storage and retrieves a DC power supply by converting the incoming RF signal where only a few microwatts power is achievable for the operation of the entire chip [1]. Thus, efficient use of power is a crucial factor in determining the performance of the tag. Fig. 1.2 depicts a simplified block diagram of a passive RFID transponder. The main components of the transponder IC include antenna, analog front-end circuit and baseband processor. In the analog front-end, it has communication circuitry to receive and send back information, a rectifier that converts the incoming RF signal to a DC power supply and clock generator that delivers system clock to the digital processor to perform command handling, encoding and decoding.

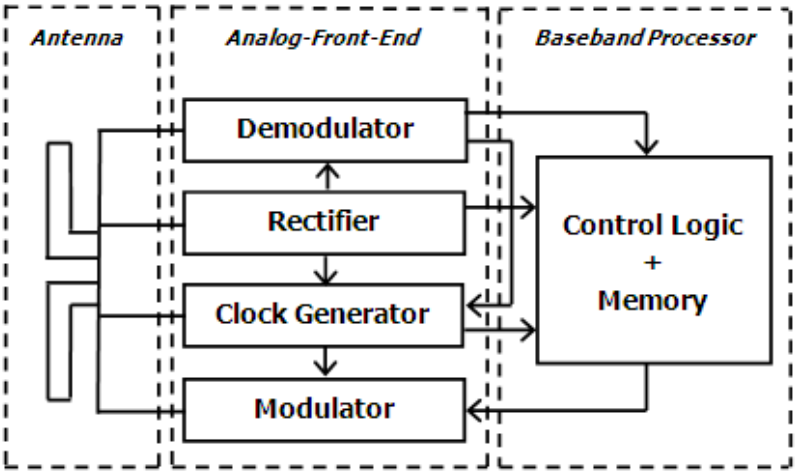


Figure 1.2: Simplified block diagram of UHF RFID transponder.

- *Active Tags:* Active RFID tag contains a battery and an active transmitter. The operational range of active tags can be more than 30 meters. It can contain a larger memory, microprocessor and sensors. It works better with RF absorbent material. It usually has a lifetime of five years.

- *Semi-active Tags:* Semi-active tags contain a battery but no active transmitter. The battery runs the chip circuitry but uses EM waves to power the communication with the reader. It supports longer operating range than passive tags, typically 30 meters.

1.4 Analog Front-End

1.4.1 Rectifier

A four transistor cell based CMOS rectifier topology is shown in Fig 1.3 [15]. This structure is preferred when compared to diode-based rectifiers and the Schottky diodes with low turn-on voltage are not available. In Fig 1.3, V_P and V_P' are complementary input ac signals received from the reader, and the rectified dc output voltage is $(V_H\text{-}V_L)$. The operation of the

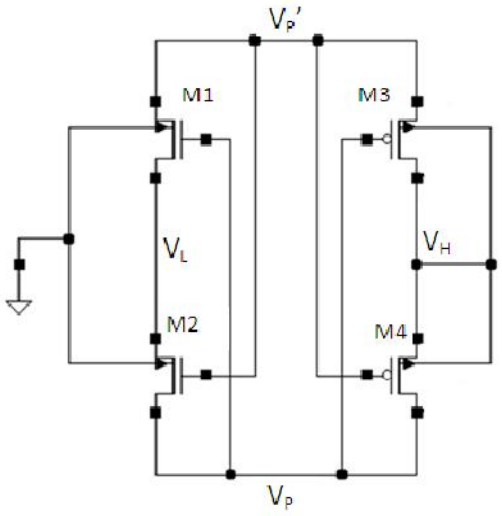


Figure 1.3: Four-transistor recifier cell.

four-transistor rectifier cell is explained here assuming V_P and V_P' are large enough to turn the transistors on and off. The transistors then operate as switches. During half of the switching cycle, V_P is high and V_P' is low. In this case *M1* and *M4* are on and *M2* and *M3* are off. Thus, current flows into V_H through *M4* and out of V_L through *M1*. During the other half of the cycle, *M1* and *M4* are off and *M2* and *M3* are on. Current flow at V_H and V_L has the same direction as before. Thus, a dc voltage is developed across a load connected between V_H and V_L. In general, $V_{DC} = (V_H - V_L) = (2V_{RF} - V_{DROP})$, where V_{RF} is the input ac voltage amplitude of V_P or V_P' and V_{DROP} represents losses due to resistance of the transistors and reverse conduction.

The maximum value of $(V_H - V_L)$ that can be obtained from a single four-transistor cell is limited to $2V_{RF}$. To obtain larger values of V_{DC}, N cells can be cascaded in series as shown in Fig. 1.4. V_P and V_P' for the first stage are directly connected to the succeeding stages are capacitively coupled to V_{RF} through C_P, allowing V_{DC} to build up at the output. The circuit behaves as a charge pump voltage multiplier.

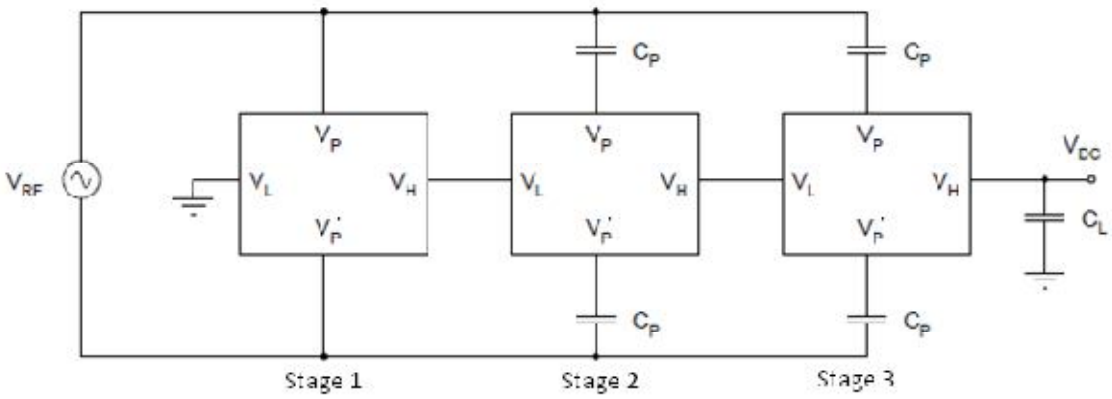


Figure 1.4: Rectifier formed by cascading N rectifying cells in series.

1.4.2 Antenna and Matching Network

The power conversion efficiency of the rectifier must be improved at low input power levels in order to get good power-up range. The rectifier dead zone severely affects this efficiency when input voltage amplitudes are low. An impedance transformation that increases the impedance and thus the RF voltage amplitude is thus desirable at the rectifier input terminals.

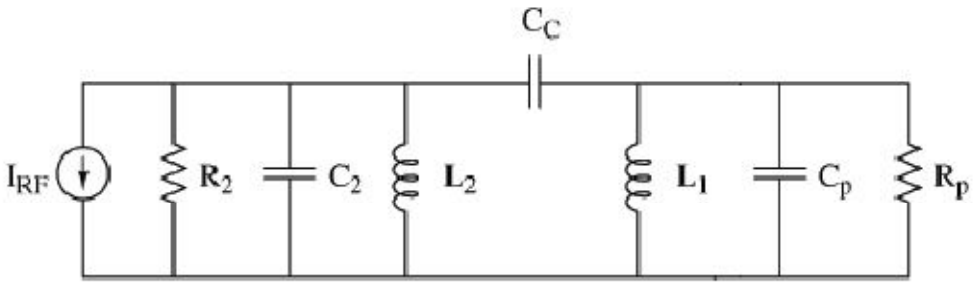


Figure 1.5: Equivalent circuit of the rectifier, antenna and impedance matching network.

An antenna can be impedance matched to the rectifier through two coupled resonators [15]. The rectifier input impedance at frequencies of interest is capacitive and can be represented

as C_P in parallel with a resistance R_P. C_P is resonated with a parallel inductor L_1 which creates the first resonator. This parallel resonant circuit is shown in Fig. 1.5. The antenna itself acts as the second resonant circuit. A parallel resonant half wavelength loop antenna is used because of its simplicity and relatively small area. The antenna is represented in Fig. 1.5 by the R_2-L_2-C_2 resonant tank. The two resonators, the chip and the antenna, can be coupled using a J-type impedance inverter (i.e., C_C couples the two resonators) to obtain a second-order impedance matching network. It can be shown that second-order matching networks have approximately double the bandwidth of first-order networks such as *L*-matches. Fig. 1.6 shows the physical structure of the tag antenna. The antenna is planar and uses a single metal layer on a printed circuit board. The small loop creates L_1; the large loops produce R_2, L_2, and C_2. The transmission lines connecting the inner loop with the larger ones produce the coupling capacitance C_C. During fully differential operation, the line of symmetry *AA'* acts as a virtual ground plane. The entire antenna can be regarded as the combination of two single ended antennas back to back.

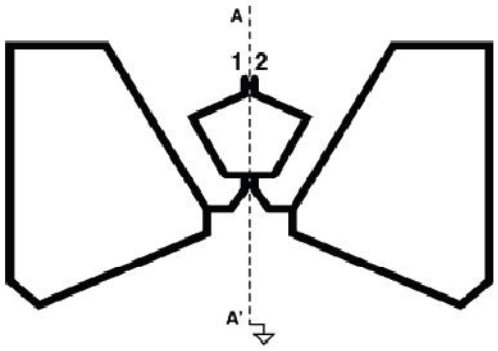


Figure 1.6: Physical structure of the antenna.

1.4.3 Clock Generation Circuit

The schematic of a clock generator proposed for UHF RFID transponder is shown in Fig 1.7. The circuit consists of a cross-coupled relaxation oscillator core and an output buffer [5]. The small-signal impedance connected between nodes 1 and 2 is approximately equal to $-2/g_m - 1/sC$. At high frequency, the first item cancels out the loss of the resistor R, while the second item oscillates with the capacitance between nodes 1 and 2. The oscillator's output frequency can be expressed as:

$$f = \frac{I_0}{2\Delta V_c C} \tag{1.1}$$

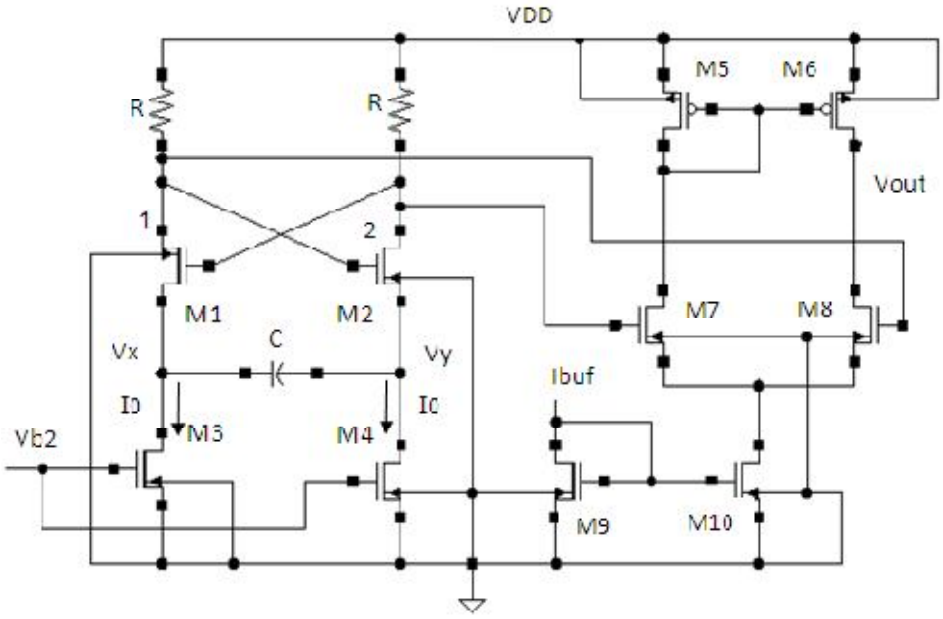


Figure 1.7: Schematic of a clock generation circuit designed for UHF RFID

where ΔVc is the maximum voltage change of Vx or Vy during oscillation. $M1$ and $M2$ can be regarded as perfect switches so that they can go into the triode and cutoff region in turn to make the capacitance be charged and discharged. In the low-voltage application, when the

current I_0 is quite small, the effect of the sub-threshold current of *M1* and *M2* cannot be neglected. Therefore, *M1* and *M2* will have a sub-threshold current instead of being totally cut off. Hence, the expression of ΔVc can be derived as:

$$\Delta V_c = 2I_0 R - \left(V_{T1,2} - nV_t \ln \frac{I_0}{I_{D0}}\right) - \sqrt{\frac{4I_0}{K'(W/L)_{1,2} + \left(2I_0 R - V_{T1,2}^{\,2}\right)}} \qquad \textbf{(1.2)}$$

where $V_{T1,2,}$ $K' = \mu Cox$ and $(W/L)_{1,2}$ for transistors *M1* and *M2* are threshold voltage , transconductance parameter and size of *M1* and *M2*, respectively; while $Vt = kT/q$, n and I_{D0} are thermal voltage, sub-threshold slope factor and a process-dependent parameter, respectively. From eq. (1.1) and (1.2), the oscillation frequency can be calculated. The power dissipation of this oscillator is reported as 750 nW when the frequency of oscillator is 5.65 MHz.

1.4.4 Demodulator

For the forward link from the reader to the tag, an ASK demodulator is commonly employed. An envelope detector consisting of diodes and capacitors is used in the ASK demodulator. Therefore, it is difficult to reduce the chip area. The current-mode ASK demodulator is also proposed. Because of the current-sensing technology, the current peak hold circuit and the current comparator are needed in this design, thus the architecture is very complex. Instead of ASK demodulator, an FSK demodulator (Fig. 1.8) consisting of data recovery circuit, multiplexer (MUX), shift registers, the phase frequency detector (PFD), and charge-pump (CP) circuit is discussed here to realize the analog front-end circuit for RFID tags [16].

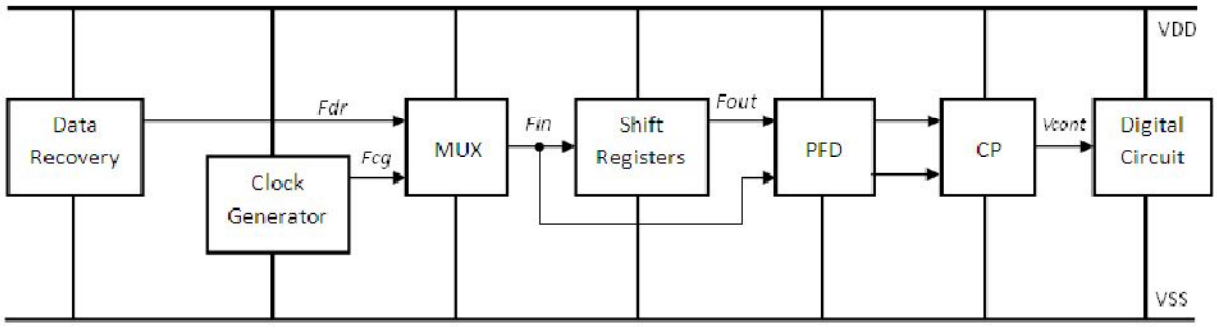


Figure 1.8: FSK demodulator for RFID transponders

The input signal *F*dr of the MUX is the output of the data recovery circuit, and another input signal *F*cg of the MUX is obtained from the clock generator with the half frequency of *F*dr. When two different input signals are delivered to the MUX, the function of FSK can be obtained at the output *F*in. The signal *F*in passes through the shift register to obtain the output signal *F*out. The *F*in and *F*out serve as the inputs of the PFD to detect the phase and frequency differences. When the control clock is in high state, the capacitor of C_P charges up and the output signal *V*cont is high. On the other hand, when the control clock is in low state, the capacitor of C_P discharges and the output signal *V*cont is low. Therefore, the high or low-output digital signals of FSK demodulator can be obtained.

1.4.5 Voltage Regulator

The typical voltage regulator circuit consists of a diode regulator and a series regulator. The diode regulator simply uses four series diodes to confine the excessive power and the function of limiter is performed. A shunt regulator with a parallel power MOSFET can be used which can limit the large output swing from the rectifier and thus the use of a limiter can be avoided.

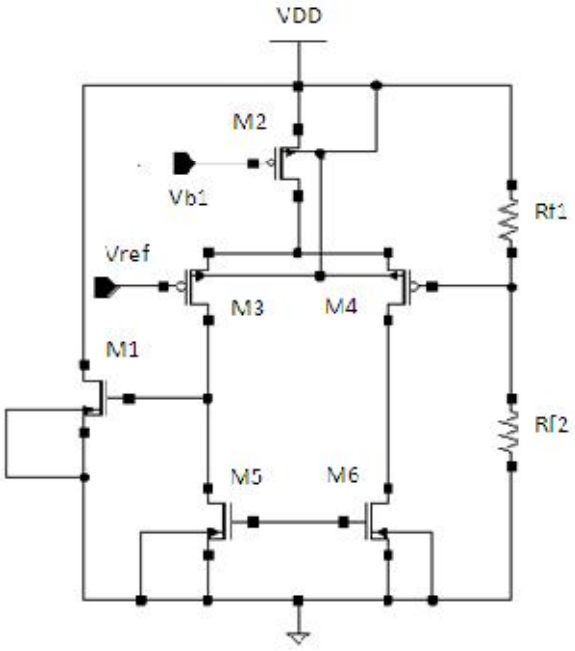


Figure 1.9: Voltage regulator circuit

The shunt voltage regulator circuit consists of a single-stage operational amplifier, a power MOSFET *M*1, and two feedback resistors R_{f1} and R_{f2}, as shown in Fig. 1.9 [16]. The single-stage amplifier is composed of the PMOS transistors *M*2 and *M*4 with the NMOS current mirror *M*5 and *M*6 as the active load. The single-stage amplifier compares the reference voltage *V*ref and the output feedback voltage, and sends a control signal to *M1* to regulate the output voltage. When the open loop gain is larger than one, the negative feedback system is stable. The reference voltage *V*ref and the bias voltage *V*b1 are generated by a band-gap reference circuit. The output voltage can be expressed as

$$V_{DD}\text{-}V_{SS} = (V_{ref}\text{-}V_{SS})\left(1+\frac{R_{f1}}{R_{f2}}\right) \qquad \textbf{(1.3)}$$

1.4.6 Modulator

The modulation for UHF RFID is done using a backscatter approach. When the backward link is active, the reader transmits a continuous wave carrier for the data transfer. The electromagnetic wave scattered back by the antenna is modulated by changing the transponder IC's input impedance. This modulated backscattered signal is used for the reverse link from the transponder IC to the reader.

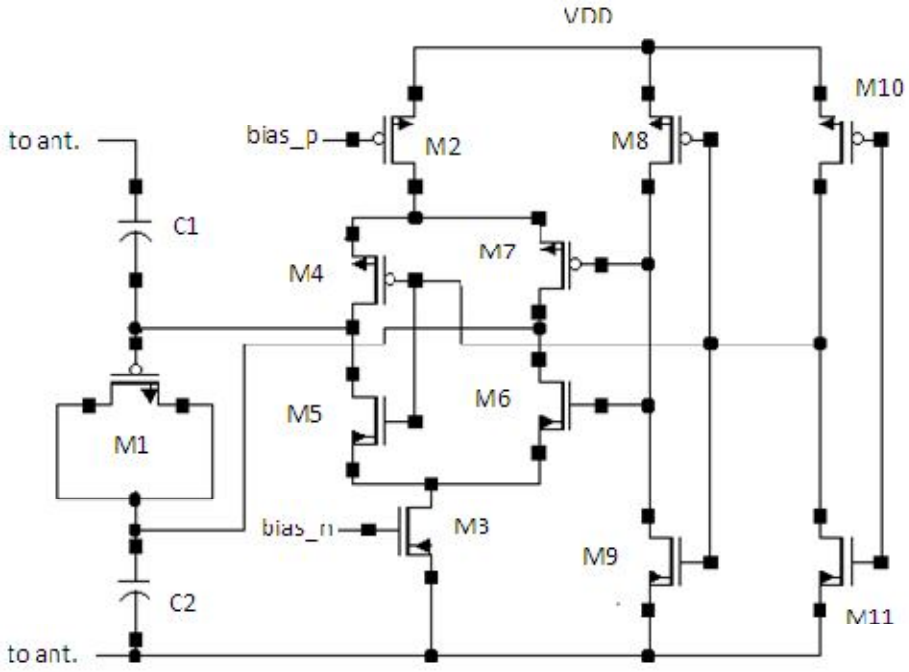


Figure 1.10: Schematic of the backscatter phase modulator.

The schematic of the modulator circuit is shown in Fig. 1.10. The circuit changes the input capacitance (rather than the input resistance) and leads to a phase modulation [phase shift keying (PSK), rather than amplitude shift keying (ASK)] of the backscattered wave [17]. The input impedance is changed by using accumulation mode MOS varactor *M1*. With help of the

two capacitors *C1* and *C2*, the dc voltage across the varactor can be set to +/- V_{DD} and thus changes the varactor's capacitance between its maximum and minimum value. *M8* to *M11* operate as two simple inverters for the incoming logic signal. Depending on the logic state, either *M4* and *M6* or *M5* and *M7* are switched off. Biasing of *M2* and *M3* decides how fast the varactor is charged and discharged and thus determines the bandwidth of the backscattered signal to be consistent with regulations. With this PSK approach, high power efficiency for dc voltage generation and high modulated backscattered power for the reverse link are achieved simultaneously. In addition, the signal-to-noise ratio and the bit-error rate are better than ASK.

CHAPTER II

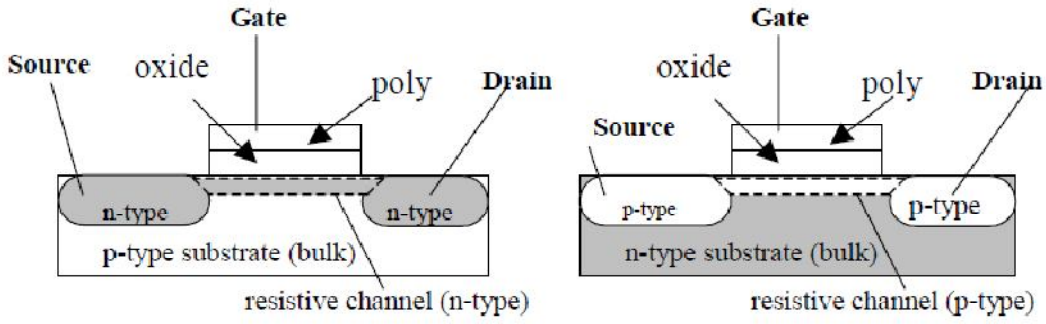
ANALOG CMOS CIRCUIT DESIGN

2.1 The MOS Transistor

The MOSFET is a four terminal device. At the most primary level, the transistor can be considered to be a switch. When a voltage is applied to the gate terminal that is larger than a given value called the threshold voltage V_{TH}, a conducting channel is formed between the drain and source terminals. In the presence of a voltage difference between the latter two, current flows between them. The larger the voltage difference between gate and source, the smaller the resistance of the conducting channel and the larger the current. When the gate voltage is lower than the threshold, traditionally the switch is considered to be open. However, a very small current called the leakage current exists under this condition. The body represents the fourth terminal of the transistor. Its function is secondary as it only serves to modulate the device characteristics and parameters.

Two types of MOSFET devices are identified. The NMOS transistor consists of n+ drain and source regions, embedded in a p-type substrate. The current is carried by electrons moving through an n-type channel between source and drain. MOS devices can also be made by using an n-type substrate and p+ drain and source regions where current is carried by holes moving through a p-type channel. The device is called a p-channel MOS, or PMOS transistor. In a

complementary MOS technology (CMOS), both devices are present. The cross-section of both devices are presented in Fig. 2.1.



(a) (b)

Figure 2.1: Structure of (a) NMOS device, (b) PMOS device

Circuit symbols for the MOS transistors are shown in Fig. 2.2. As mentioned earlier, the transistor is a four-terminal device with gate, source, drain, and body terminals. Since the body is generally connected to a dc supply that is identical for all devices of the same type (gnd for NMOS and Vdd for PMOS), it is most often not shown on the schematics.

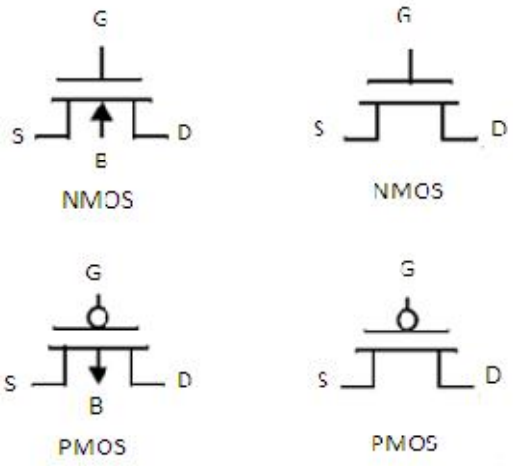


Figure 2.2: Circuit symbols for MOS transistors

2.2 Current-Voltage Characteristics

2.2.1 Strong Inversion

When $V_{GS}>V_{TH}$ and a small voltage V_{DS} is applied between drain and source, the voltage difference causes a current I_D to flow from drain to source. When $V_{DS}< V_{GS}-V_{TH}$, the device operates in triode region. The current in triode region is given by [18] [29]

$$I_D= \mu C_{ox} \frac{W}{L} \left[(V_{GS}-V_{TH})V_{DS}-\frac{1}{2} V_{DS}^2\right] \quad \textbf{(2.1)}$$

where μ is the surface mobility, C_{OX} is the gate oxide capacitance per unit area, V_{TH} the threshold voltage, and W and L are the transistor's effective channel width and length, respectively. $V_{GS}-V_{TH}$ is called the overdrive voltage and W/L the aspect ratio. The MOS transistor operates as a linear resistor when $V_{GS} << 2(V_{GS}-V_{TH})$ and the value of the resistance is controlled by the overdrive voltage. The resistance is given by [18],

$$R_{on}= \mu C_{ox} \frac{W}{L} [V_{GS}-V_{TH}]^{-1} \quad \textbf{(2.2)}$$

When $V_{DS} > V_{GS}-V_{TH}$, the drain current I_D becomes relatively constant and the device is said to operate in saturation region. The I_D vs. V_{DS} curve for NMOS transistor in 90-nm CMOS technology is shown in Fig. 2.3.The drain current in saturation region is given by [18] [29]

$$I_D=\frac{1}{2}\mu C_{ox} \frac{W}{L} (V_{GS}-V_{TH})^2 \quad \textbf{(2.3)}$$

The relationship between I_D and V_{GS} is given by the slope of the I_D versus V_{GS} characteristic which is called the transconductance; g_m. It is basically a measure of how well the device converts an input voltage to an output current. The transconductance is expresses as [18] [29]

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{ox} \frac{W}{L} (V_{GS}-V_{TH}) \quad \textbf{(2.4)}$$

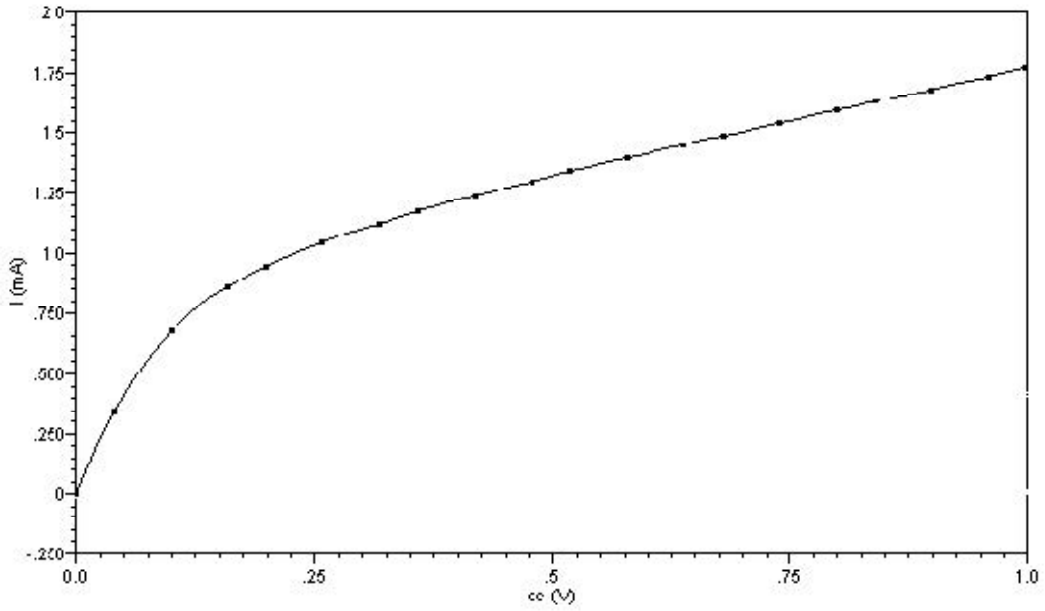


Figure 2.3 : I_D vs. V_{DS} curve for 90-nm CMOS technology ($L=0.1um$)

In analogue circuits it is essential to make calculations for small changes in the signal. The small-signal model of MOS transistors is presented in Fig. 2.4. In the model *ro* represent the output resistance of the transistor and determined by the channel-length modulation. The current sources, $gm*V_{GS}$ and $gmb*Vsb$ represent the small signal currents going through the transistor. The capacitances denoted by C_{GD}, C_{GS} and C_{DB} are the parasitic capacitances of the transistor which is determined by the length of the channel and the width of the device.

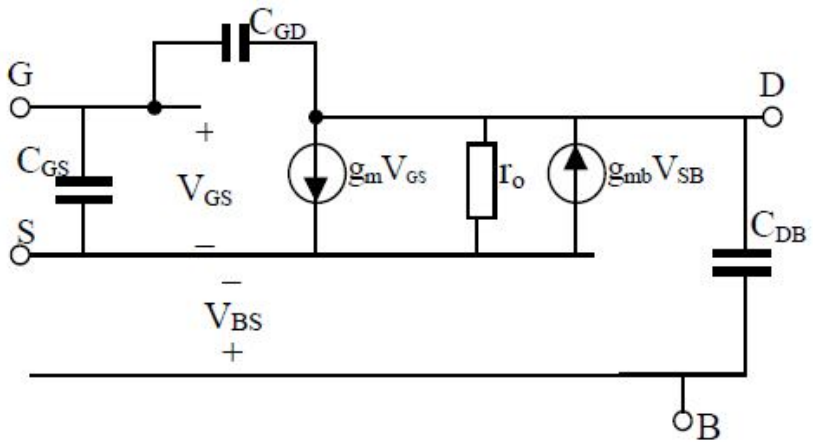


Figure 2.4 : MOSFET Small Signal Model

2.2.2 Weak Inversion

The motivation of designing circuits in weak inversion mode is to be able to exploit the leakage current of the transistors as the circuit driving current. Leakage currents are orders of magnitude smaller than the drain current in strong inversion, which brings the power dissipation down to a much lower level. Weak inversion is not recommended for high performance systems because of the increased delay the devices become slow. However, in extremely energy constrained systems like RFID, where minimum power dissipation is the primary concern with low-to-moderate performance; weak inversion proves to be an advantageous design approach [37]. The approximate relation between drain current I_D and gate-to-source voltage V_{GS} in weak inversion region is given by [3]

$$I_D = 2n\mu C_{OX}\left(\frac{W}{L}\right)U_T^2\, e^{\frac{V_{GS}-V_{TH}}{nU_T}} \qquad \textbf{(2.5)}$$

where, $U_T=KT/q$ is the thermal voltage, $n=(1+C_{DEP}/C_{OX})$ is the slope factor ,C_{OX} is the gate oxide capacitance per unit area, C_{DEP} is the depletion capacitance per unit area, μ is the surface mobility , V_{TH} is the threshold voltage, W and L are the effective channel width and length, respectively. In weak inversion region, a much lower voltage is needed to guarantee saturation approximated by $|V_{DSAT}|$=4-5U_T. The transconductance in weak inversion is given by,

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{nU_T} \tag{2.6}$$

Voltage gain of a single MOS transistor is the product of g_m and the output conductance r_{ds} which can be replaced by the ratio of Early voltage (V_E) to the drain current. The MOS transistor achieves the highest voltage gain in weak inversion which is given by [3],

$$Gain = g_m r_{ds} = g_m \frac{V_A}{I_D} = \frac{V_A}{nU_T} \tag{2.7}$$

2.3 The g_m/I_D Methodology

In gm/I_D methodology, the relationship between the ratio of the transconductance *gm* over dc drain current I_D and the normalized drain current $I_D/(W/L)$ is considered as a fundamental design tool to calculate the dimensions of the transistors [8][38]. The gm/I_D ratio is strongly related to the performance of analog circuits. It also gives an indication of the device operating region. The gm/I_D ratio is a measure of the efficiency to translate current, hence power into transconductance. The greater the gm/I_D value, the greater the transconductance is obtained at a

constant current value. Hence, the gm/I_D ratio is sometimes interpreted as a measure of the transconductance generation efficiency.

The relation of the gm/I_D ratio with the transistor operating region can be observed from the fact that it is equal to the derivative of the logarithmic of I_D with respect to V_G, as shown below [8]

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_G} = \frac{\partial (ln I_D)}{\partial V_G} = \frac{\partial \left\{ ln\left[\frac{I_D}{\frac{W}{L}}\right]\right\}}{\partial V_G} \qquad \textbf{(2.8)}$$

This derivative is maximum in the weak inversion region where the dependence of I_D on V_G is exponential while it is quadratic in strong inversion and becomes almost linear deeply in strong inversion because of the velocity saturation. The theoretical maximum is $1/nU_T$ where n is the sub-threshold slope factor and U_T the thermal voltage. The gm/I_D ratio decreases as the operating point moves toward strong inversion when I_D or V_G are increased as shown in Fig. 2.5. Therefore, the gm/I_D ratio is also an indicator of the region of operation of the transistor.

The normalized current $I_D/(W/L)$ is independent of the transistors size. According to eq. (2.8) the gm/I_D ratio is also size independent. Therefore, the relationship between gm/I_D and the normalized current $I_D/(W/L)$ is a unique characteristic for all transistors of the same type (N or P) and the same process. The unique characteristic of the gm/I_D versus $I_D/(W/L)$ curve can be extensively employed when the transistor aspect ratios (W/L) are unknown. The W/L of the transistor can be determined easily once a pair of values among gm/I_D, gm and I_D has been derived.

The actual gm/I_D versus $I_D/(W/L)$ curve can be obtained either analytically or from measurements on a typical transistor. The curves shown in Fig. 2.5 are obtained from simulations on typical transistors using 90-nm CMOS technology

Choosing the values for g_m/I_D, $I_D/(W/L)$ is determined for each transistor from the experimental g_m/I_D versus $I_D/(W/L)$ curves. The intended values of g_m/I_D are chosen accordingly to their effect on the circuit performance. Assuming the total supply current is known as a priori, the drain current of each transistor is determined from the specified total current, and the normalized current is determined for each transistor from the experimental g_m/I_D versus $I_D/(W/L)$

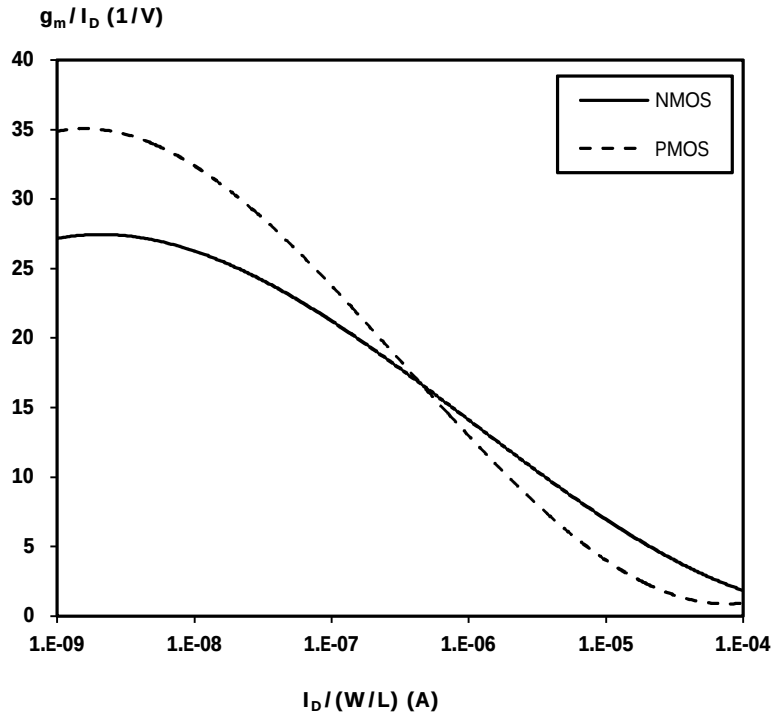


Figure 2.5: Simulated characteristic curves for NMOS and PMOS using 90-nm CMOS technology.

curves. Then, the dimensions of the transistors can be determined from the ratio of the drain current dictated by the total supply current and the normalized drain current.

The weak inversion analysis considers the exponential approximation for the drain current versus the gate voltage. This approximation predicts g_m/I_D to be independent of the current and is equal to $1/nU_T$. Therefore, for weak inversion design, the g_m/I_D value does not determine an I_D value in this simplified model. The $I_D/(W/L)$ value must be chosen to guarantee weak inversion operation. The criterion that can be applied is to choose $I_D/(W/L)$ at least ten times smaller than the value corresponding to the limit between the weak and strong inversion approximations equal to $2n\mu C_{OX}U_T^2$, which is a classical criterion to guarantee weak inversion operation. A new method to design weak inversion circuits is discussed in Chapter V which is base on the relationship between MOS inversion coefficient and the normalized current $I_D/(W/L)$.

CHAPTER III

VOLTAGE-CONTROLLED OSCILLATORS

3.1 General Considerations

An oscillator is a circuit that generates a periodic output waveform, usually in the form of voltage. Oscillators have numerous applications from serving as reference tone generators for receivers to clocks for digital circuits. They also serve as the central component in frequency synthesizers. The oscillator circuits have no input while sustaining the output indefinitely. An oscillator can be viewed as a negative feedback system, as shown in Fig. 3.1. The transfer function of the system can be expressed as:

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1+H(s)} \qquad \textbf{(3.1)}$$

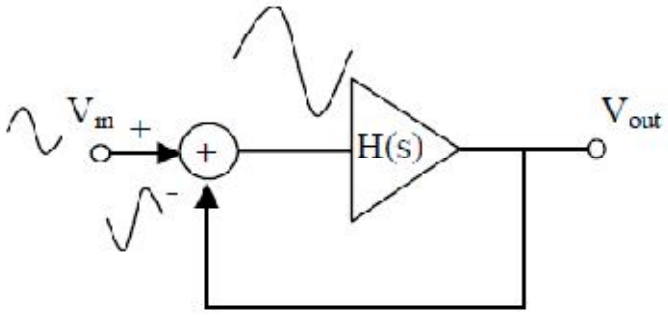


Figure 3.1: Regenarative feedback system.

The negative feedback system begin to oscillate when the close-loop gain approaches infinity at ω_0 and for $s = j\omega_0$, $H(j\omega_0) = -1$. Under this condition, the circuit amplifies its own noise components at ω_0 indefinitely. A noise component at ω_0 experiences a total gain of unity and a phase shift of 180^o, returning to the subtractor as a negative replica of the input. Upon subtraction, the input and the feedback signals give a larger difference, Thus, the circuit continues to regenerate, allowing the components at ω_0 to grow. Hence, A negative feedback system may oscillate if it satisfies the following conditions [5] [18]:

$$| H(j\omega_0) | \geq 1 \tag{3.2}$$

$$H(j\omega_0) = 180^o \tag{3.3}$$

Most applications require the oscillators to be tunable. A voltage controlled oscillator or as more commonly known, a VCO, is an oscillator where the output frequency can be adjusted by tuning the control voltage. The general tuning characteristics of a VCO is shown in Fig. 3.2.

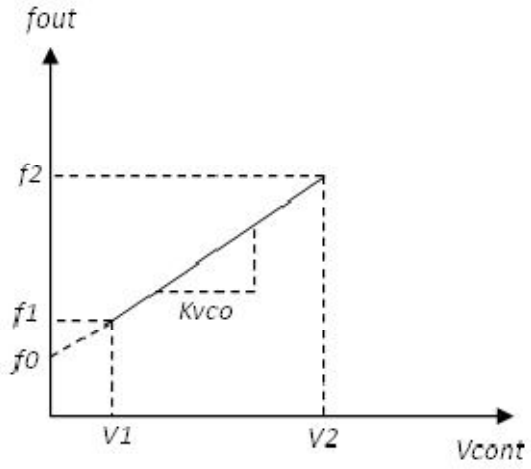


Figure 3.2: Tuning characteristics of voltage-controlled oscillators

For an ideal VCO, the output frequency can be expressed as,

$$f_{out} = f_o + K_{VCO}V_{cont} \quad \textbf{(3.4)}$$

where, f_0 represents the intercept corresponding to $V_{cont} = 0$ and K_{VCO} is the tuning gain or the sensitivity of the circuit. When the control voltage is varied from *V1* to *V2*, the frequency of oscillation is tuned from *f1* to *f2* (Fig. 3.2). The achievable frequency range $f_2 - f_1$ is called the tuning range.

3.2 Performance Parameters

- *Center Frequency*: The center frequency is the midrange value in the characteristics curve shown in Fig. 3.2 which is determined by the particular application the VCO is designed for. Today's CMOS VCOs can achieve center frequencies as high as 10 GHz.
- *Tuning Range*: For most applications it is required for the VCO to provide a wide tuning range to make sure the output of the circuit can be driven to the desired value for process and temperature variation. Wide tuning range in oscillators has a direct conflict with the phase noise performance. To optimize phase noise, the VCO should be designed to have minimum sensitivity to the control lines which reduces the gain of the circuit and degrades the tuning range.
- *Tuning Linearity*: The output frequency of the VCO must be linearly proportional to the control voltage. The tuning characteristics shown in Fig. 3.2 may exhibit nonlinearity as the gain of the VCO is not constant for the entire tuning range. It is desirable to minimize the variation of *Kvco* across the tuning range.

- *Output Amplitude*: It is desirable to have large output amplitude which makes the oscillator less sensitive to noise. The output amplitude has trade-offs with power dissipation, power supply and tuning range. The amplitude is desired to be constant across the tuning range.
- *Power Dissipation*: The design of oscillators is a tradeoff process that involves power consumption, speed and phase noise performance. Depending upon application some metrics need to be traded for the others. If the power consumption of an oscillator is to be optimized, its phase noise performance degrades.
- *Supply and Common-mode Rejection*: Oscillators are sensitive to noise from the power supply and control lines. The sensitivity is even higher when they are designed in single-ended form which is why differential structures are often preferred.
- *Phase noise performance*: The output signal of the oscillator is not perfectly periodic as generally assumed. The intrinsic noise of the devices and the sensitivity if the oscillator results in random variation in output phase and frequency leading to undesirable effects. These effects are characterized by phase noise and determined by the requirements of each application, discussed in Chapter VI.

3.3 Voltage-Controlled Oscillators

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3.3.1 LC Based VCOs

In LC based VCOs, the LC resonator forms feedback mechanism to obtain steady oscillations and determines the frequency of oscillation. The oscillation frequency is approximately by [18] [19]

$$\omega_{osc} = \sqrt{\frac{1}{LC}} \tag{3.5}$$

Eq. 3.5 suggests that the frequency of oscillation can be tuned by varying the inductor and capacitor values. Since it is difficult to vary the value of monolithic inductors, voltage-dependent capacitors called "varactors" are employed for frequency tuning. In CMOS technology, a varactor can be realized by a regular MOS transistor where the source and drain terminals are tied together.

The quality factor Q of a passive circuit element can be defined as [19]

$$Q = \frac{|Im(Z)|}{|Re(Z)|} = \frac{\omega L}{R_s} = \frac{|Im(Y)|}{|Re(Y)|} = \frac{R_P}{\omega L} \tag{3.6}$$

where Z is the impedance and Y is the admittance of the inductor, L is the equivalent inductance at frequency ω, and R_s and R_p are the equivalent series and parallel resistance of the inductor at frequency ω . Most integrated inductors have quality factors that rise at low frequencies and then have some peak beyond which the losses make the resistance rise faster than the imaginary part of the impedance, and the Q starts to fall off again. Thus, Q dictates the need for proper optimization to ensure that the inductor has peak performance at the frequency of interest.

3.3.1.1 Colpitts Oscillator

The Colpitts oscillator shown in Fig. 3.3 is an important block of RF circuits. The small-signal linearized model of the Colpitts oscillator is also shown in Fig. 3.3. The nodal equations for this model are [20]

$$\left(\frac{1}{R_T}+\frac{1}{L_T s}+C_1 s\right) v_{out} - C_1 s v_b = g_m v_b \quad \textbf{(3.7)}$$

$$-C_1 s v_{out} + (C_1 + C_2) s v_b = - g_m v_b \quad \textbf{(3.8)}$$

The characteristic equation of this oscillator can be found as,

$$R_T L_T C_1 C_2 s^3 + L_T (C_1 + C_2) s^2 + \left[L_T g_m + R_T (C_1 + C_2)\right] s + R_T g_m = 0 \quad \textbf{(3.9)}$$

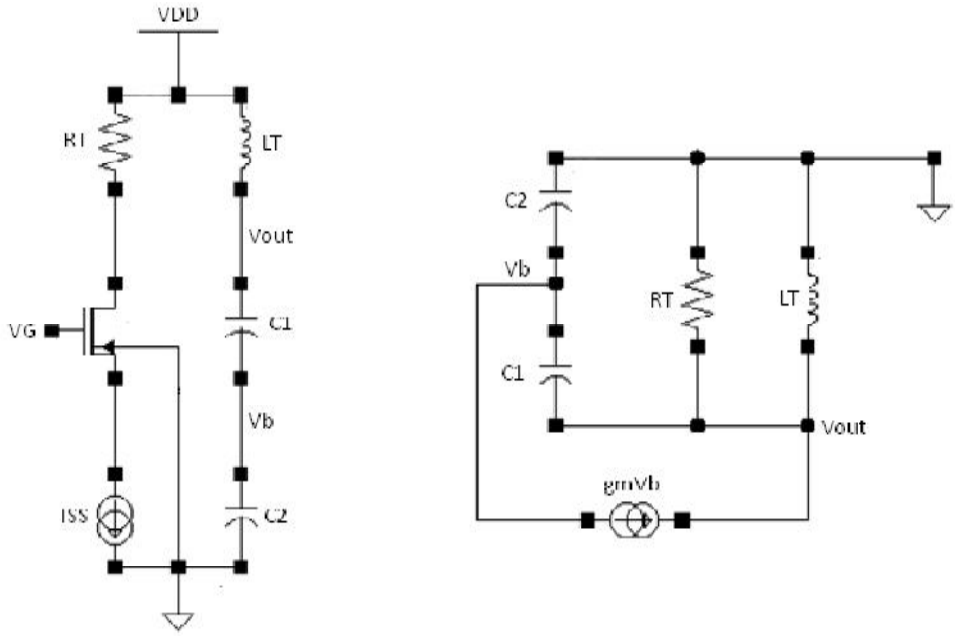


Figure 3.3: Colpitts oscillator and the small signal model

The start-up oscillation conditions is given by [20],

$$L_T (C_1 + C_2)\left[L_T g_m + R_T (C_1 + C_2)\right] - R_T^2 L_T C_1 C_2 \, g_m < 0 \quad \textbf{(3.10)}$$

which can be written as,

$$g_m > \frac{(C_1+C_2)}{R_T C_T - (L_T/R_T)} \quad \textbf{(3.11)}$$

where $C_T = (C_1C_2)/(C_1+C_2)$. For every practical coil the term L_T/R_T in the denominator of eq. (3.11) is nearly two orders of magnitude less than R_TC_T. Hence, eq. (3.11) can be written as,

$$g_m R_T \left(\frac{1}{n}\right)\left[1-\left(\frac{1}{n}\right)\right] > 1 \quad \textbf{(3.12)}$$

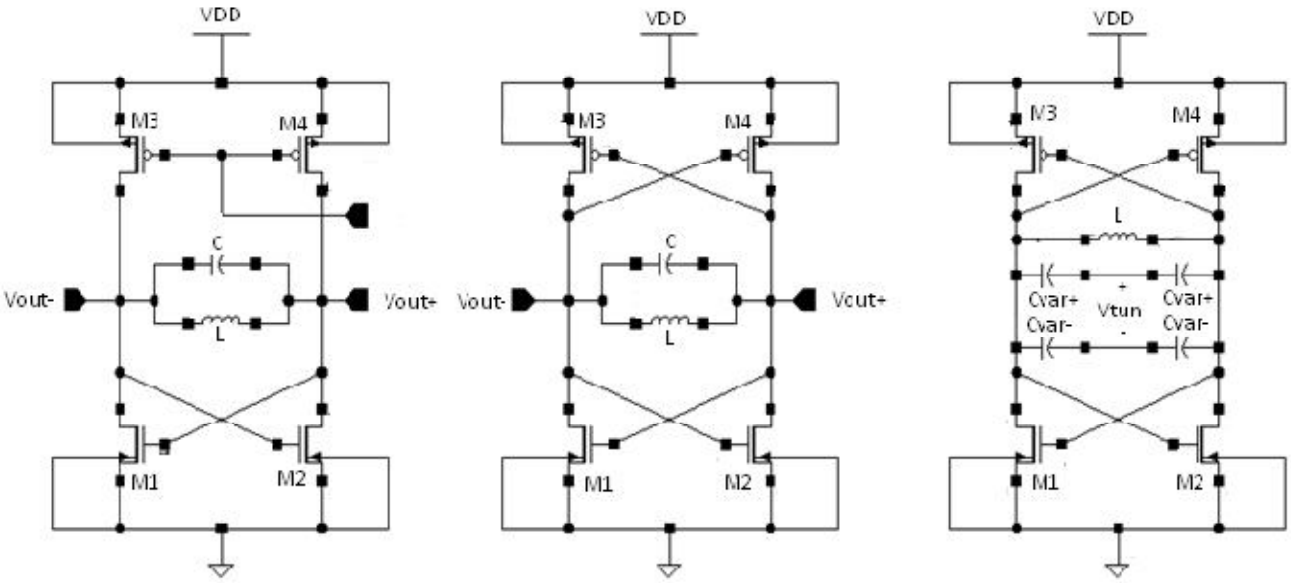
where $n=1+(C2/C1)$. During the oscillation development gm changes from $g_{m0}=2\sqrt{(kI_{ss})}$ defined by the bias current I_{ss} (here $k=(\mu Cox/2)(W/L)$) down to the value of $g_{mc}=(C_1+C_2)/R_TC_T$. The recommended choice of $g_{m0}/g_{mc} \approx 3$ ensures a start of oscillation [20].

3.3.1.2 Negative-Gm Oscillator

Fig. 3.4(a) presents the cross-coupled pair LC oscillator topology with PMOS active load which is called a negative-Gm oscillator. The cross-coupled pair realizes a negative resistance to compensate for the losses of the tank circuit. It can be shown that, a cross-coupled pair of transistors has an impedance of [21]

$$Z_i = \frac{-2}{g_m} \quad \textbf{(3.13)}$$

Assuming the losses are mostly related to the series resistance of the inductor, the cross-coupled pair has to provide enough negative resistance to compensate for them so that oscillation is sustained. By changing the gate bias voltage V_G it is possible to control the current at the drain of the NMOS transistors. Due to limited differential transconductance provided by this topology, a high Q is required to sustain oscillation. In CMOS technology, high quality factor inductors are difficult to implement. Hence, a complementary topology is often employed that doubles the total differential transconductance and sustains oscillation for lower values of Q [Fig 3.4(b)].



(a) (b) (c)

Figure 3.4: (a) NMOS negative-Gm oscillator with PMOS active loads,(b) Complementary cross-coupled LC oscillator (c) Differential varactor tuning

Differential varactors controlled by a differential tuning voltage, as shown in Fig. 3.4(c), can be used for frequency tuning. The varactors labeled *C*var+ have capacitance that increases with applied voltage, while the varactors labeled *C*var- decrease with applied voltage. Thus, if a differential voltage is applied, *C*var+ varactors see a positive voltage, while *C*var- varactors see a negative voltage. Hence, both varactors are increased in capacitance for an increase in differential input voltage. However, for a common-mode voltage, both varactors see a voltage in the same direction; hence, the increase in capacitance from the *C*var+ varactor is matched by an equal decrease in the capacitance from the *C*var- varactors.

3.3.2 Injection Locked Oscillator

When, rather than noise, an oscillator is disturbed by a second oscillator operating at a nearby frequency, the phenomenon is called injection locking. When the coupling is strong

enough and the frequencies near enough, the second oscillator can capture the first oscillator, causing it to have essentially identical frequency as the second. The most common technique is the parallel connection shown in Fig. 3.5, where each oscillator is made up of a tank circuit and cross-coupled feedback circuit. In addition, each oscillator output is connected to the other oscillator with transistors in parallel to the cross-coupled transistors. Thus, oscillator 1 has feedback transistors*M*1 and*M*2 and coupling from oscillator 2 via transistors *M*5 and *M*6. Typically, feedback and coupling transistors are made the same size. Furthermore, because of symmetry, the oscillation amplitudes of the two oscillators should be the same. The phase shift in the injection locked oscillator is given by [19],

$$\Phi_{inj} = -2\tan^{-1}\left[\left(\omega C - \frac{1}{\omega L}\right)R\right] \qquad \textbf{(3.14)}$$

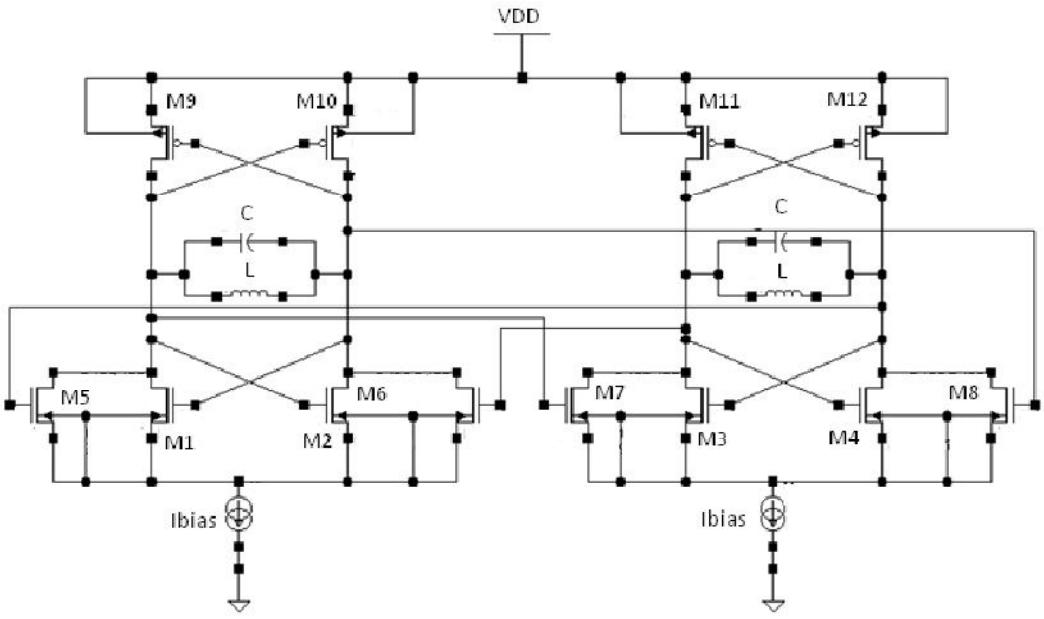


Figure 3.5: Injection locked oscillator

An analysis of the loop gain of this oscillator results in the expression of the frequency of oscillation given by,

$$\omega = \sqrt{\frac{1}{LC} + \frac{g_m^2}{4C}} \pm \frac{g_m}{2C} \tag{3.15}$$

The "±" is used because two solutions can be found for ω, one is above the resonant frequency and the other one is below the resonant frequency.

3.3.3 Ring Oscillator

The ring oscillators consist of delay cells connected in cascade and in a closed loop. A behavior model of N stage ring oscillator is shown in Fig. 3.6.

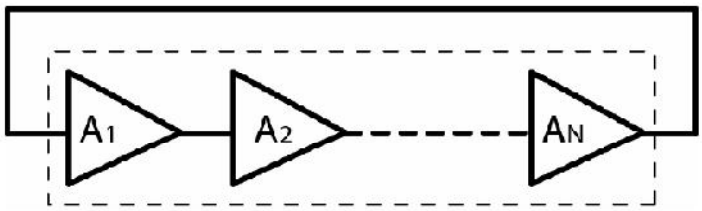


Figure 3.6: Ring oscillator with N number of stages

Let $A_N(t)$ be the transfer function of each delay stage and $A_t(s)$ be the transfer function of *N* delay stages. The closed loop transfer function can be expressed as [22] [18],

$$A_f(s) = \frac{A_t(s)}{1\text{-}A_t(s)} \tag{3.16}$$

Assuming, $A_1(s) = A_2(s) = \ldots = A_N(s)$, the loop gain of the circuit is defined as,

$$L(s) = A_1(s)\, A_2(s) A_3(s) \ldots\ldots A_N(s) = A^N(s) = A_t(s) \tag{3.17}$$

According to the oscillation condition discussed in section 3.1, the system must satisfy the following requirements to ensure oscillation [22] [18]

$$| A(j\omega_0) |^N \geq 1 \tag{3.18}$$

$$A(j\omega_0) = \frac{180^o}{N} \tag{3.19}$$

3.3.3.1 Linear Model

In the linear model of ring oscillators, each delay cell is modeled with a transconductance stage g_m and an RC circuit as shown in Fig. 3.7. [22].

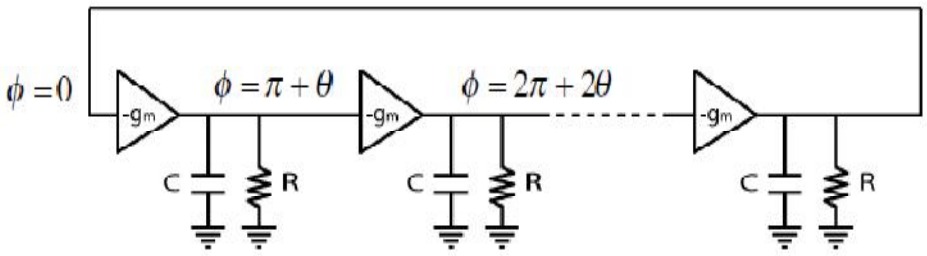


Figure 3.7: Ring oscillator linear model

The open-loop transfer function can be calculated as,

$$A(j\omega) = \frac{-g_m R}{1 + j\omega RC} \tag{3.20}$$

The frequency of oscillation can be derived as,

$$\omega_0 = \frac{tan\theta}{RC} \tag{3.21}$$

In S-domain, the transfer function can be modeled as,

$$A(j\omega) = \frac{A_0}{1 + \frac{s}{\omega_0}} \tag{3.22}$$

where A_o is the voltage gain per stage and ω_o is the 3-db bandwidth of each stage. The gain requirements to ensure oscillation for an N stage ring oscillator can be derived from the following equations: [18]

$$tan^{-1}\ \frac{\omega_{osc}}{\omega_0} = \frac{180^o}{N} \tag{3.23}$$

$$\left[\frac{A_0}{\sqrt{1 + \left(\frac{\omega_{osc}}{\omega_0}\right)^2}} \right]^N = 1 \tag{3.24}$$

3.3.3.2 Time-Domain Analysis

In time domain, the circuit consisting of *N* delay stages and oscillates with a delay of T_D between consecutive node voltages, yielding a period of $2NT_D$. Fig. 3.8 shows a three stage ring oscillator with CMOS inverters yielding a period of $6T_D$.

The frequency of oscillation can be expressed as [18] [5],

$$f = \frac{1}{2NT_D} \tag{3.25}$$

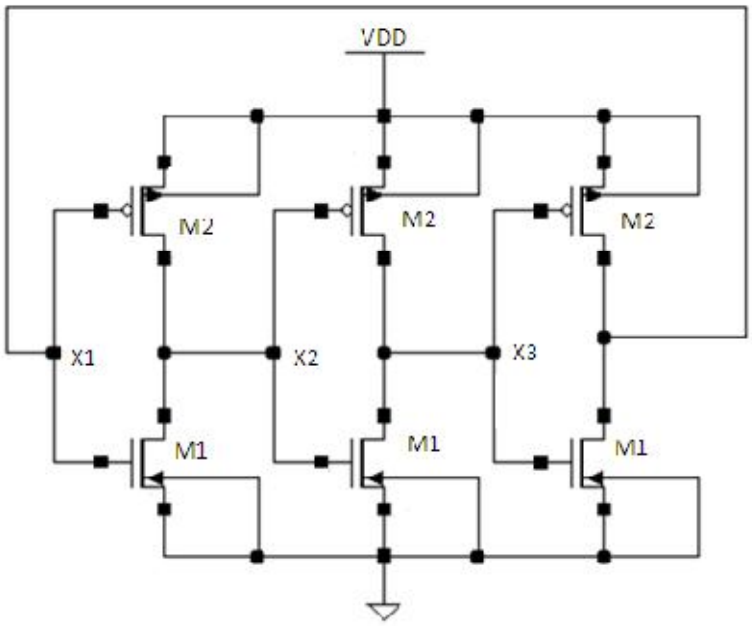
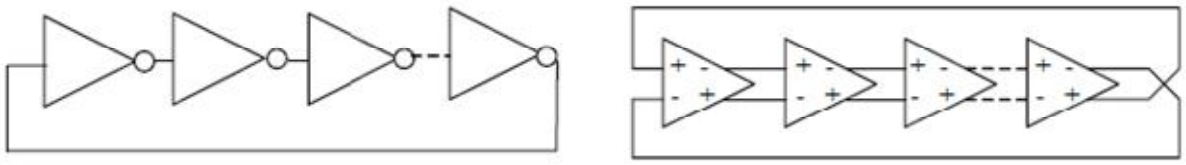


Figure 3.8: Three stage ring oscillator with CMOS inverters

Thus, frequency of oscillation can be adjusted by varying the delay T_D. Assuming the circuit of Fig 3.8 begins with $V_{X1}=V_{DD}$. Under this condition, $V_{X2}=0$ and $V_{X3}=V_{DD}$. Thus when the circuit is released, V_{X1} begins to fall to zero forcing V_{X2} to rise to V_{DD} after one inverter delay and V_{X3} to fall to zero after another inverter delay.

3.3.3.3 Ring Oscillator Topologies

Ring oscillators can be designed with single-ended or differential structures. The total number of inversions in the loop must be odd so that the circuit doesn't latch up. Single-ended structures can be implemented only with odd number of delay stages. Differential structures can be designed also with even number of delay stages simply by configuring one stage such that it doesn't invert. Fig 3.9 shows basic N stages single-ended and differential ring oscillator structures.



(a) (b)

Figure 3.9: Block Diagram of (a) Single-ended ring oscillator (b) Differential ring oscillator.

- **Single-ended topology**

The basic single-ended topology consists of CMOS inverters. Current is consumed in CMOS inverters when the output node capacitances are charged and discharged. At an input step the capacitances is charged/discharged by a constant current generated by the transistor that is currently on. Consequently, a lower charging current would cause a longer transition time that translate to a longer delay and lower frequency of operation. A typical delay cell topology for single-ended ring oscillator is shown in Fig. 3.10. The delay cell consists of two input transistors *M1* and *M2*. Two extra transistors *M3* and *M4* are added in the inverter cell to tune the frequency of oscillator by adjusting the control voltages *Vcont1* and *Vcont2*. With this modification the delay in the cell, and thereby the frequency of oscillation, can be controlled with a voltage. This type of delay cell is called current-starved inverter [23].

- **Differential Topology**

The differential topology consists of a load pair and an NMOS differential pair (Fig. 3.11) [24]. The delay of the cell is set by the charge in each node and the current through the load. The load can be implemented with resistors for fixed frequency or PMOS devices, which makes the oscillator tunable with a control voltage. The PMOS load is usually implemented as

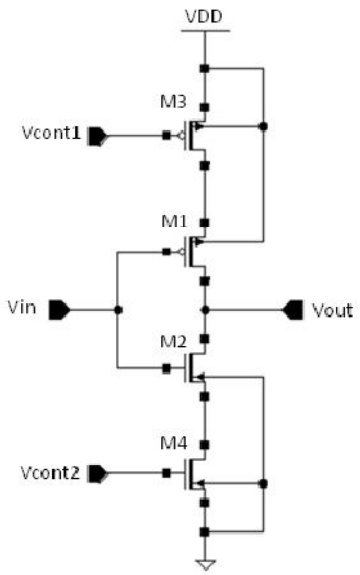


Figure 3.10: Current-starved inverter

symmetric or cross-coupled [5] [6]. Tail current source transistor in this delay cell can be avoided to attain a maximal output voltage swing since the current limitation of tail current sources can be avoided. It also helps to reduce the 1/f noise.

The single-ended topology dissipates power on a per transition basis only and therefore has a better phase noise for a given power dissipation. The difference in phase noise becomes even larger when the number of stages increases. However, in digital circuits differential ring oscillators are often preferred because they have much better common noise rejection of substrate-coupled noise than its single-ended counterpart, even if the single-ended topology has a superior phase noise. Differential ring oscillators also have a lower noise injection into other circuits on the same chip. Another advantage of the differential ring oscillator over the single ended is the possibility to implement it with an even number of cells and less number of transistors. Thus, it is possible to generate quadratic signals with the differential ring oscillator.

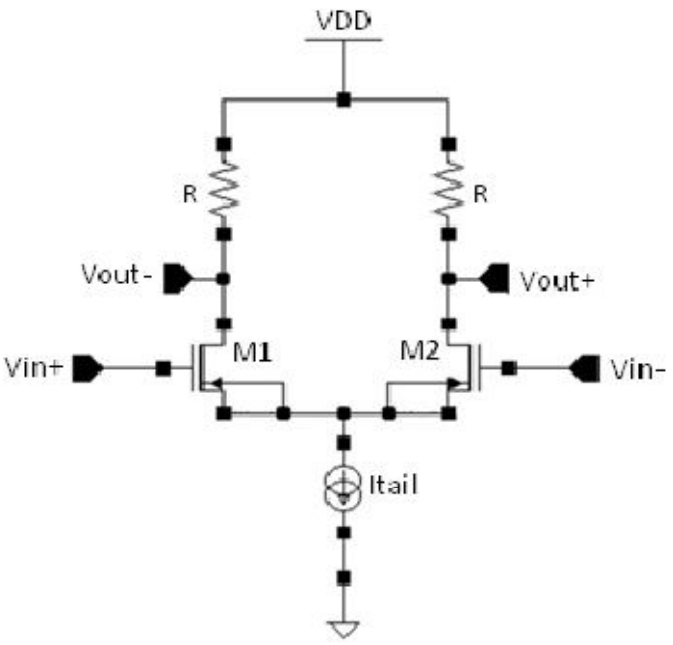


Figure 3.11: A Basic differential delay cell

3.3.3.4 Dual-Delay Path Technique

The frequency of a conventional single-loop ring oscillator is limited by the smallest delay provided by the basic inverter delay cell. Hence, various techniques had been explored to reduce the smallest achievable delay per stage, and one of which is the feed-forward or dual-delay paths technique [25] [34]. A block diagram of a three-stage ring oscillator using dual-delay paths is shown in Fig. 3.12.

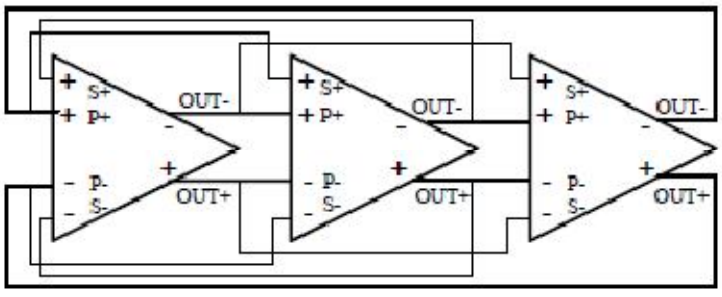


Figure 3.12: Block diagram of a ring oscillator with dual-delay paths

The principle of feed-forward oscillator is to add another secondary feed-forward path into the loop to make the delay per stage smaller than that of the single-loop oscillators. The bold lines seen in Fig. 3.12 represent the primary loop and the solid lines represent the secondary loop. The differential outputs of each stage are connected to the primary inputs of the next stage as well as the secondary inputs of the stage after the next. Hence, the load transistors that serve as the secondary inputs are turned on prematurely before the primary input transistors. The architecture of the feed-forward ring oscillator allows a minimum stage of three and the less number of stages implies a higher oscillating frequency.

3.3.3.5 Delay Variation by Interpolation

One approach to tuning ring oscillators is based on interpolation [3] [4]. As shown in Fig 3.13, each stage consists of a fast path and a slow path whose outputs are summed and whose gains are adjusted by the control voltage in opposite directions.

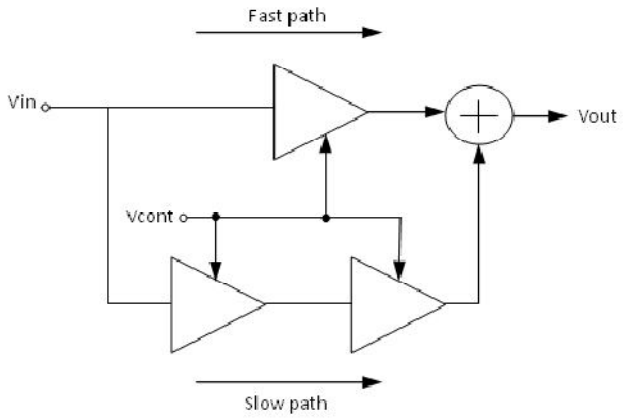


Figure 3.13: Block digaram of delay interpolation

At one extreme of control voltage, only fast path is on and the slow path is disabled, yielding the maximum oscillator frequency. Conversely, at the other extreme, only slow path is on and the fast path is off, providing the minimum oscillation frequency. If the control voltage lies between the two extremes, each path is partially on and the total delay is a weighted sum of their delays [18].

3.3.4 Crystal Oscillator

Crystal oscillators use mechanical resonance of a vibrating crystal to produce oscillation signals with accurate frequency. Quartz crystal resonators are widely used in frequency-control applications because of their high quality factor, stability, and small size. When a potential difference is applied across opposite faces of a quartz crystal, mechanical deformation takes place. If the frequency of the potential is appropriate, the crystal vibrates and resonates. The resonant frequency, *Q*, and temperature coefficient depend on the physical size and orientation of faces relative to the crystal axis. For most applications, the two-terminal equivalent circuit consisting of the static capacitance C_0 , in parallel with the dynamic branch, *L*1 -*C*1 -*R*1 , is used as shown in Fig. 3.14, in which f_s is called motional resonance frequency given by,

$$f_s = \frac{1}{2\pi L_1 C_1} \tag{3.26}$$

For crystal oscillator applications, the figure of merit, *M*, is a useful indicator that is defined as

$$M = \frac{1}{2\pi f_s C_0 R_1} \tag{3.27}$$

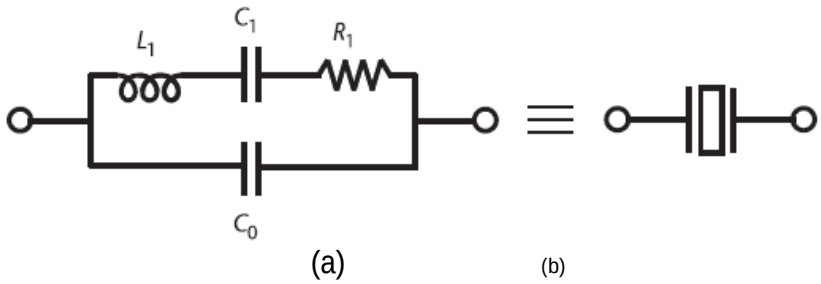


Figure 3.14: Two terminal equivalent circuit of a crystal

For $M < 2$, the crystal reactance is never inductive at any frequency, and an additional inductor would be required to form an oscillator. In general, a larger M results in a more useful resonator. In a crystal resonator, the quality factor is defined as:

$$Q = \frac{|X_1|}{R_1} = \frac{2\pi f_s L_1}{R_1} = \frac{1}{2\pi f_s C_1 R_1} \tag{3.28}$$

where the time constant $\tau = C_1 R_1$ depends on the mode of vibration and on the angles of cut. If the crystal is used to replace an inductor in an oscillator circuit, for example, as shown in Fig. 3.4, then oscillations will only occur in the frequency range where the crystal is actually inductive. While the crystal behaves like an inductor at the oscillating frequency, unlike a real inductor, no dc current flows through the crystal because, at dc, it is like a capacitor.

3.4 Comparison of Oscillator Performance

Table 3.1 provides a quick summary comparison of the LC oscillator, ring oscillator, and crystal oscillator. From the table, it can be seen that there are significant differences between the oscillators, and each can be said to be the best in certain applications.

Table 3.1: Comparison Summary for Crystal, LC and Ring Oscillators

Parameter	*Crystal*	*LC*	*Ring*
Output frequency	Low	High	Medium
Quality factor	High	Medium	Low
Phase noise	Best	Good	Poor
Power consumption	Low	High	Highest
Multiphase output	No	No	Yes
Frequency stability	Best	Good	Poor
Tuning Range	Narrow	Medium	Wide
Integration	No	Large size	Small size
Applications	Reference source	GHz VCO	Digital clock

3.5 Application Example: PLL

Almost all digital circuits depend on at least one clock source, which generates a rail-to-rail square wave. The most common approach for the generation clock signals is through Phase Locked Loop (PLL). The oscillator is the core of phase locked loops. The simple PLL, presented in Fig. 3.16, consists of a Phase Detector (PD) a Low-Pass Filter (LPF) and a Voltage Controlled Oscillator (VCO). Once the PLL is locked, any change in relative phase between the reference and output signal is detected by the phase detector. The feedback loop ensures that the VCO control voltage is changed to keep the phase difference constant and hence the output frequency constant. PLLs are not preferred to be used in realization of RFID transponders because of their relatively higher power dissipation and larger chip area.

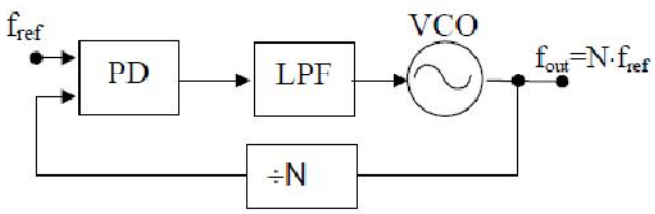


Figure 3.15: Block digaram of a phase locked loop

CHAPTER IV

CIRCUIT IMPLEMENTATION OF THE PROPOSED VCO

4.1 Basic Two-Stage Ring Oscillator

The linearized model of a basic two-stage ring oscillator is shown in Fig. 4.1, where each delay cell is modeled with a transconductance stage *Gm* and an *RC* circuit. The open-loop transfer function can be calculated as

$$H(s) = -\left(\frac{-G_m R}{1+j\omega RC}\right)^2 \qquad \textbf{(4.1)}$$

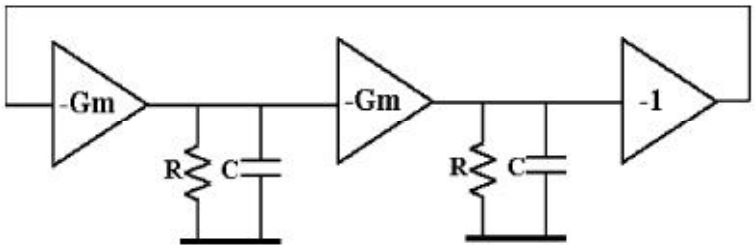


Figure 4.1: Linearilzed model of a simple two-stage ring oscillator

Assuming that the phase shift introduced by *Gm* is small and by applying the steady oscillation criteria $H(j\omega) = 1$ to eq. 4.1, the oscillation condition occurs for

$$RC\omega \gg 1 \tag{4.2}$$

which is equivalent to

$$G_m R \gg 1 \tag{4.3}$$

with the oscillation frequency expressed as

$$\omega = \frac{G_m}{C} \tag{4.4}$$

The condition 4.3 implies that for a certain loss *R*, an extremely high *Gm* is required in order to ensure a steady oscillation state. Consequently, the current consumption level is required to be high which in turn requires large components with increased parasitics, thus making the oscillation condition difficult to obtain.

4.2 Two-Stage Ring Oscillator Using Double Amplifier

As discussed earlier, steady oscillation in a ring oscillator requires a total phase shift of 360^o around the loop at a frequency where small-signal loop gain is above 0 db. In an N-stage ring oscillator, each stage contributes a phase shift of 180^o/ N for a total of 180^o and another 180^o is provided by dc phase inversion. The dc phase inversion is automatically achieved through inverting stages (N odd), or by swapping two feedback lines in a differential architecture (N even). As discussed in the previous section, it is difficult to obtain sufficient gain and phase from each stage to ensure oscillation with a two stage structure. The use of parallel differential amplifier simultaneously increases the absolute phase shift and the gain of a differential stage, making it easier to meet the oscillation condition [31].

A delay cell for two-stage differential oscillator is shown in Fig. 4.2, where each stage is based on a pair of differential amplifiers in parallel. Each amplifier in the parallel pair provides its full gain on a single-ended output, using a differential current- mirror load, while the outputs from the two amplifiers are in opposite phase. Figure 4.2 shows the schematic of the double differential amplifier as one stage of the oscillator. A double differential amplifier has a symmetrical topology that provides a differential gain twice that of a single amplifier. The tail currents are varied in both stages to control the delay per stage and thus the oscillation frequency.

Nevertheless, the structure requires extra circuitry and the power consumption stays high due to the use of four differential amplifiers. The required characteristics can be obtained by means of local positive feedback in the delay cells as discussed in the next section.

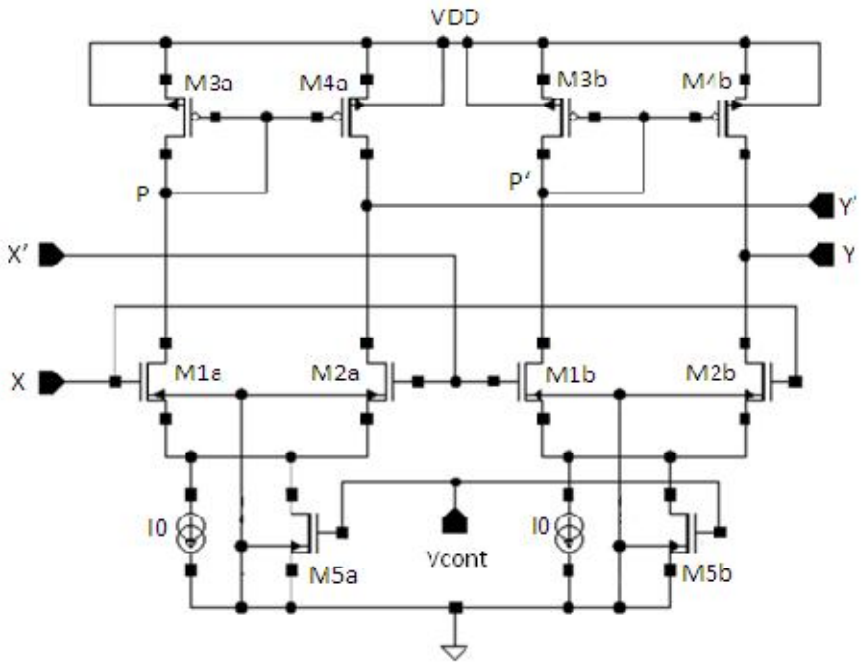


Figure 4.2: Delay cell with double differential amplifier

4.3 Two-Stage Ring Oscillator Using Negative Resistance

The linearized model shown in Fig. 4.3 employs an additional active positive feedback in each delay cell which is equivalent to a negative resistance (R_n=*-1/Gm'*) that compensates the resistive losses and makes the oscillation condition achievable at much lower power consumption. The new equivalent resistance *Rq* can be written as

$$R_q = \frac{R.R_n}{R+R_n} = \frac{R}{1-G_m'.R} \tag{4.5}$$

and the new open-loop transfer function can be expressed as

$$H(j\omega) = - \left(\frac{-G_m R_q}{1+j\omega R_q C} \right)^2 \tag{4.6}$$

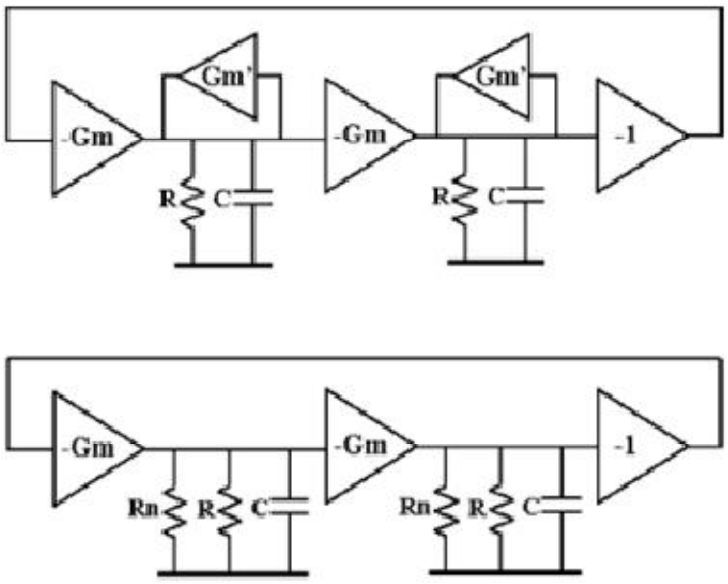


Figure 4.3: Linearilzed model of a two-stage ring oscillator with local feedback

By calculating the modulus and the phase expressions of this transfer function, we get

$$|H(j\omega)| = \frac{(G_m.R_q)^2}{1+\omega^2 R_q^2 C^2} \tag{4.7}$$

$$tg(\Phi(j\omega)) = \frac{-2R_q C\omega}{1-\omega^2 R_q^2 C^2} \tag{4.8}$$

The extraction of the oscillation condition from eqs. 4.7 and 4.8 leads to

$$G_m \gg \frac{1}{|R_q|} = \frac{1}{R} - G_m^{'} \tag{4.9}$$

And the oscillation frequency is given as

$$\omega = \frac{G_m}{C} \tag{4.10}$$

The frequency of oscillation in 4.10 is the same as the expression for a simple two-stage oscillator in eq. (4.4), while the oscillation condition is now dependent on a new factor. This factor facilitates steady oscillation at lower power consumption as compared to the simple two-stage ring oscillator. This becomes particularly true around the ideal case of $Gm'=1/R$, which means a compensation for all resistive losses and almost an oscillation condition is satisfied for any $Gm>0$.

Hence, the use of a two-stage ring oscillator with local positive feedback presents the advantage of making the oscillation condition more easily achievable at lower power consumption levels in comparison with a simple two-stage ring oscillator. In addition, this architecture maintains the small-signal relationship between frequency and transconductance which is exactly the same as that of a simple two-stage ring oscillator [6] [32] [35].

4.4 Basic Delay Cell with Local Feedback

A basic differential delay cell architecture utilizing a local positive feedback is shown in Fig. 4.4. The cell consists of one NMOS input pair (M_N) and one PMOS cross-coupled load pair (M_{P1}). As discussed in the previous section, if this structure is used to construct a two-stage ring oscillator, a complete compensation for all resistive losses is possible and an oscillation condition is satisfied for any $G_m > 0$, where G_m is the equivalent transconductance of the delay stage. However, a control mechanism is needed in the cell so that the frequency of oscillation of the ring oscillator can be adjusted to meet a specific requirement. In [6], a tail resistive network is employed in each delay cell for frequency tuning. With the area and power constraints in mind, the proposed structure seeks to avoid a large resistive network.

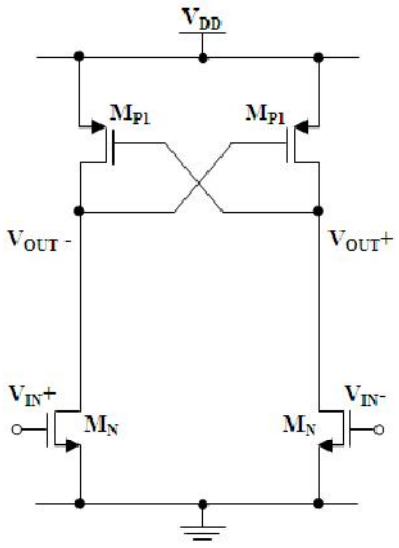


Figure 4.4: Schematic of a basic delay cell with local feedback

4.5 The Proposed Ring Oscillator

The circuit schematic of the proposed delay cell topology and the two-stage ring oscillator is shown in Fig. 4.5. The cell consists of one NMOS input pair (M_N) and one PMOS cross-coupled load pair (M_{P1}). A controller block constituted by PMOS transistor pair M_{P2} is added in the cell for frequency tuning. The delay of the stage and hence the oscillating frequency is tuned by adjusting the resistance of the M_{P2} pair. When the gate voltage V_{CTRL} is low, the strength of the M_{P2} block becomes strong, resisting the voltage switching in the cell. As a result, the delay increases. By contrast, when V_{CTRL} is high, the M_{P2} block becomes weak and the delay is reduced, and the oscillation frequency increases. The odd number of phase inversion is achieved by swapping two feedback lines in the differential architecture (Fig. 4.5b). Since the delay cell is basically a differential inverter, a full-swing waveform can be generated from the ring oscillator.

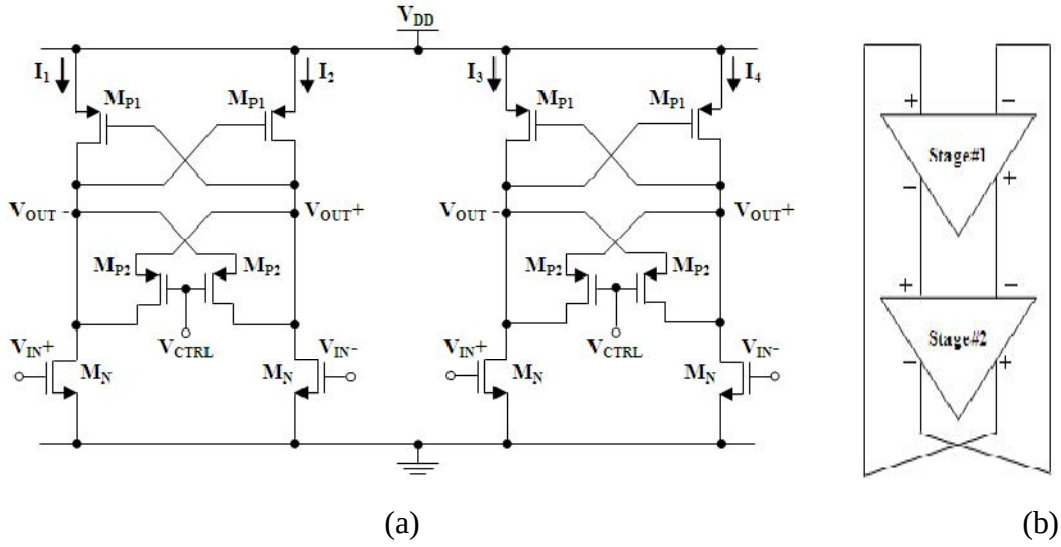


Figure 4.5: (a) Circuit implementation of the proposed structure. (b) Block diagram of two-stage ring oscillator.

CHAPTER V

NANO-POWER OSCILLATOR DESIGN

5.1 Channel Length and Inversion Level Selection

Analog CMOS design involves the selection of circuit topologies and individual transistor currents and sizing and the balancing of performance tradeoffs through the variation of several device level parameters. MOS channel width, length and inversion level strongly influence the circuit performance, for example, speed, gain, noise immunity and power dissipation. In analog designs, longer channels have often been preferred to achieve higher voltage gains and less complicated operation by avoiding short-channel effects. In addition to the channel length, the channel inversion level must be considered in analog circuit design. The three possible regions of operation, defined by the drain current and other device parameters are weak, moderate, and strong inversion. Traditional analysis of analog CMOS circuits is often based on the strong inversion region. However, the recent trend towards low-power systems gives the motivation to study the weak and moderate inversion regions. Table 5.1 lists a summary of the performance of analog cell in different inversion level and channel length that indicates the lowest power dissipation is achieved when short channel transistors operate in weak inversion region [3].

Table 5.1: The “four corners” approach for analog cell design

Short Channel - WI	***Short Channel - SI***
Advantages Relatively high voltage gain Lowest power dissipation Lower harmonic distortion Lower threshold voltages	***Advantages*** Fastest Lower threshold voltages
Disadvantages Relatively slow Short channel effects	***Disadvantages*** Lowest voltage gain Higher harmonic distortion Short channel effects Mobility degradation
Long Channel - WI	***Long Channel - SI***
Advantages Higher voltage gain Lower power dissipation Lower harmonic distortion Simple model	***Advantages*** Relatively high voltage gain Relatively fast Traditional, simple model
Disadvantages Slowest Higher threshold voltages Smaller usable inversion region	***Disadvantages*** Decreasing voltage gain Highest power dissipation Greatest harmonic distortion Higher threshold voltages

The motivation of designing the VCO in weak inversion mode is to be able to exploit the leakage current of the transistors as the circuit driving current. The leakage current is orders of magnitude smaller than the drain current in strong inversion, which brings the power dissipation down to a much lower level. Weak inversion operation is not recommended for high

performance systems because of the increased delay the devices become slow. However, in extremely energy constrained systems like RFID, where minimum power dissipation is the primary concern while maintaining low-to-moderate performance; weak inversion operation proves to be an advantageous design approach.

5.2 MOS Inversion Coefficient

The transistors must be properly biased to operate in a selected region of operation. This can be done by defining an inversion coefficient, *IC* that approximates the boundaries between different inversion regions. The *IC* is a normalized measure of drain current I_D that numerically describes the level of channel inversion. The inversion coefficient is given by [4]

$$IC = \frac{I_D}{2n\mu C_{ox}(\frac{W}{L})U_T^2} \qquad \textbf{(5.1)}$$

where, $U_T=KT/q$ is the thermal voltage, $n=(1+C_{DEP}/C_{OX})$ is the slope factor ,C_{OX} is the gate oxide capacitance per unit area, C_{DEP} is the depletion capacitance per unit area, μ is the surface mobility , V_{TH} is the threshold voltage, W and L are the effective channel width and length, respectively. MOS operation at the center of moderate inversion occurs for a drain current of $I_D=2n\mu C_{OX}U_T^2(W/L)$ where the asymptotic values of weak inversion transconductance $g_{m,weak}=I_D/nU_T$ and strong inversion transconductance $g_{m,strong}= \sqrt{2I_D(\mu C_{OX}/n)(W/L)}$ are equal. As explained in [4], the weak inversion operation occurs when $IC < 0.1$, and the center of moderate inversion and strong inversion occur at $IC = 1$ and $IC > 10$, respectively. In weak inversion, the gate-source overdrive voltage $(V_{GS} - V_{TH})$ is an exponential function of the MOS drain current and sizing and could be used as a degree of

design freedom. However, the inversion coefficient *IC* is preferred here since it is linearly related to the MOS drain current and sizing.

Since both n (decreases from approximately 1.5 in weak inversion to 1.3 in strong inversion) and μ decrease with the increasing gate voltage associated with increasing inversion, a fixed-normalized inversion coefficient can be defined where $n=n_o$ is held fixed at its value in moderate inversion and $\mu=\mu_o$ is held fixed at its low field value. This permits a fixed drain-current normalization given by

$$IC = \frac{I_D}{2n_o\mu_o C_{ox}(\frac{W}{L})U_T^2} = \frac{I_D}{I_0(\frac{W}{L})} \qquad \textbf{(5.2)}$$

where $I_0=2n_o\mu_o C_{OX}U_T^2$ is a technology current which is independent of MOS bias conditions, channel width and channel length. An estimate of I_0 can be made from the estimated values of n and μCox above for the center of moderate inversion. I_0 can be verified by observing the asymptotic intersection of measured weak and strong inversion transconductance efficiency. Since the thermal voltage is part of the inversion coefficient *IC*, all the normalizations and measurements are made in room temperature.

5.3 Analysis of the Proposed Design

5.3.1 Power Consumption

The circuit implementation of the proposed oscillator is shown in Fig. 4.5 in the previous chapter and is repeated here for convenience. The power consumption of the oscillator can be

approximated by looking at the total supply current, $I_{TOTAL}=I_1+I_2+I_3+I_4$ (Fig. 4.5). Hence, the power consumption can be approximated by

$$P \propto 8n\mu_p C_{OX}\left(\frac{W}{L}\right)_{M_{P1}} U_T^2\, e^{\frac{V_{DD}-V_{TH}}{nU_T}} \qquad \textbf{(5.3)}$$

In weak inversion region, a much lower voltage is needed to guarantee saturation approximated by $|V_{DSAT}|$=4-5U_T where U_T is the thermal voltage [7]. The power supply V_{DD} is chosen to be 0.3 V ensuring the transistors M_N and M_{P1} operate in saturation. eq. (5.3) indicates that power dissipation can further be optimized by choosing proper transistor dimensions. Traditionally the optimum selection of transistor dimension and drain current are made based on three degrees of design freedom which are drain current I_D, channel width W and channel length

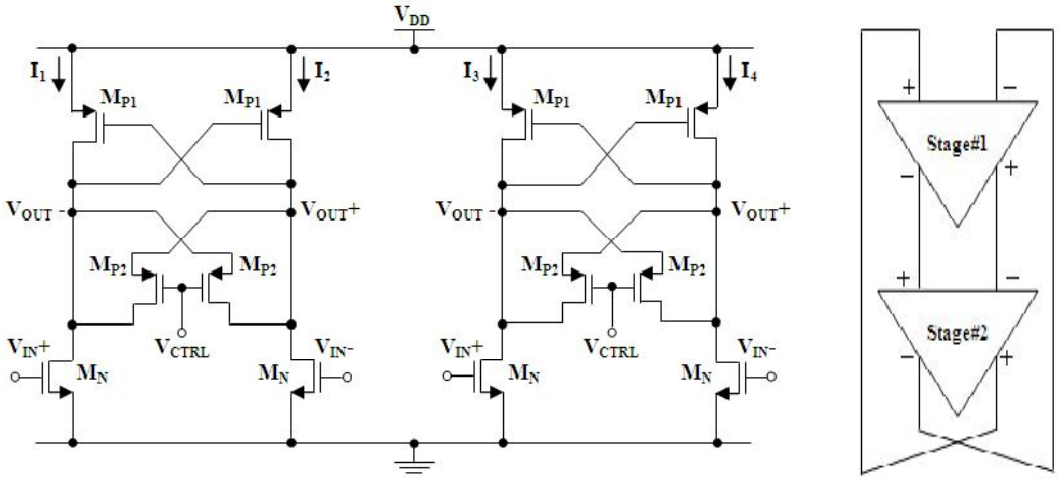


Figure 4.5: (a) Circuit implementation of the proposed structure. (b) Block diagram of two-stage ring oscillator.

L. The three degrees of design freedom considered in this work are drain current I_D, inversion level *IC* and channel length *L*. Then channel width *W* is found from the selected drain current I_D, inversion level *IC* and channel length *L*. We consider the normalized drain current, $I_D/(W/L)$ versus the inversion coefficient, *IC* curve as a fundamental design tool for optimum selection of the transistor dimensions. This curve is unique for all transistors belonging to the same type (N or P) and the same process. The curves shown in Fig. 5.1 are obtained from simulations on typical transistors using 90-nm CMOS technology.

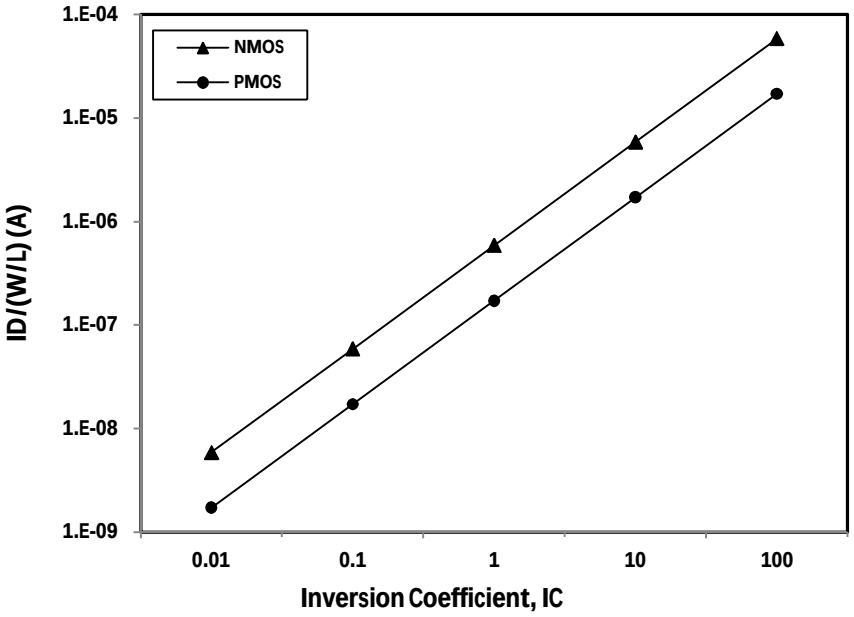


Figure 5.1: Simulated normalized drain current versus inversion coefficient curves for NMOS and PMOS using 90-nm CMOS technology.

The design space is explored here aiming at the lowest possible power dissipation. We assume that the total supply current is known as a priori and the current allowed to each delay stage in Fig. 4.5 is 40 nA and the power supply is 0.3V. The drain current of each transistor is determined from the specified total current and the normalized current is determined for each

transistor from the experimental $I_D/(W/L)$ versus the inversion coefficient, *IC* curves. The value of the normalized current must be chosen to guarantee weak inversion operation. The criterion applied here is to choose $I_D/(W/L)$ at least ten times smaller than the technology current equal to $2n\mu C_{OX}U_T^2$ so that the weak inversion requirement for the inversion coefficient is satisfied ($IC<0.1$). Then, the dimensions of the transistors can be determined from the ratio of the drain current dictated by the total supply current and the normalized drain current. In section 5.1, a four corners design approach to optimize analog cells has been discussed that demonstrates, for different combination of channel length and channel inversion, the lowest power dissipation is obtained when minimum channel length transistors operate in weak inversion [3]. Thus, using minimum channel length $L = 0.1\mu m$ for all transistors, the widths are found as $W_{M_N} = 0.25\mu m$ and $W_{M_{P1}} = 0.78\mu m$.

5.3.2 Frequency Tuning

One of the important performances for a VCO is the linear relationship between the control voltage and the oscillating frequency. Tuning characteristic is a strong function of the transistor operation region and careful considerations must be made for choosing the control voltage. For proper tuning, the control voltage of a regular strong inversion ring VCO is limited by the value of supply voltage. However, a control voltage exceeding the power supply voltage is found suitable for the proposed weak inversion mode VCO. While designing a VCO in weak inversion region, it is difficult to obtain a linear relation by tuning the transconductance g_m as extensively done in strong inversion circuits. We prefer not to choose the transconductance for frequency tuning because of its exponential dependence on gate-to-source voltage. As shown in [9], by choosing body bias voltage to function as the control voltage to fine tune the frequency,

linear tuning can be achieved for a weak inversion mode VCO. In this work, frequency tuning is achieved with standard zero body bias conditions by tuning the resistance of the controller block formed by M_{P2} pairs (Fig.2). The idea is to bias M_{P2} to operate in saturation and extend the control voltage to strong inversion region. Thus, the bias condition for M_{P2} is

$$V_{CTRL} \geq V_{DD} + |V_{THP}| \quad \textbf{(5.4)}$$

5.4 Simulation Results

The performance of the proposed ring oscillator is validated in 90-nm CMOS technology using *Cadence Custom IC Design Tool*. Fig. 4 depicts the layout of the proposed circuit with a dimension of 10.66 μm x 10.76 μm. Simulation results show that the proposed structure oscillates in weak inversion generating full-swing output signals with frequency tuning characteristics. The transient response of the proposed oscillator is shown in Fig. 5.3. The frequency tuning characteristics were simulated for different power supply voltages and the results are plotted in Fig. 5.4. The VCO is capable to operate with linear tuning charactertistic even if the power supply is as low as 0.15V. When the power supply is 0.3V, the output frequency is tuned from 4.43-6.15MHz when the control voltage is varied from 0.5-1.5V. Hence, it is possible to avoid exponential tuning of the weak inversion mode VCOs. The technique to employ should be to bias only the control transistors in strong inversion region while all the other transistos in the delay cells operate in weak inversion. The average tuning gain of the oscillator is found to be around 1.5 MHz/V. The tuning gain can be increased to about 2.4 MHz/V by making the transistors M_{N1} and M_{P1} larger at the expense of more power dissipation.

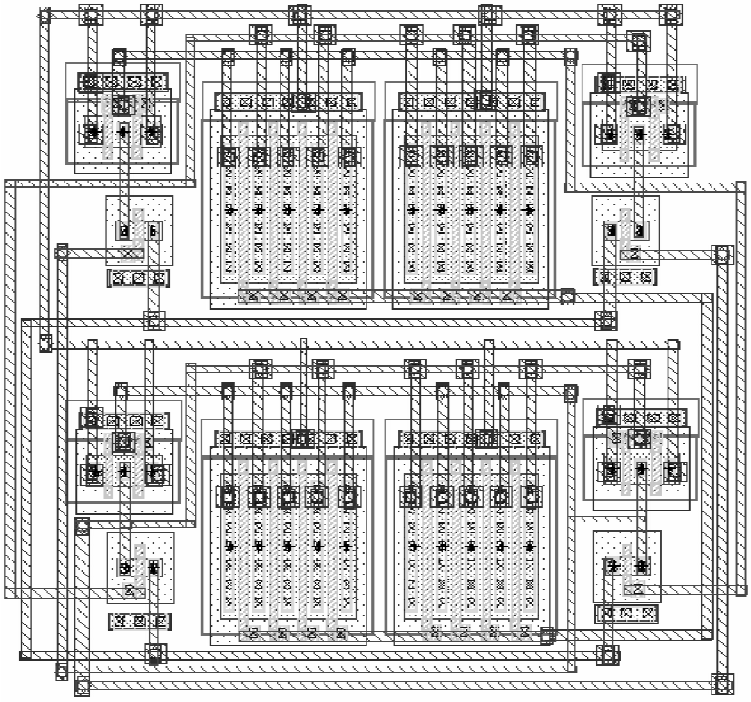


Figure 5.2: Physical layout of the proposed structure in 90-nm CMOS

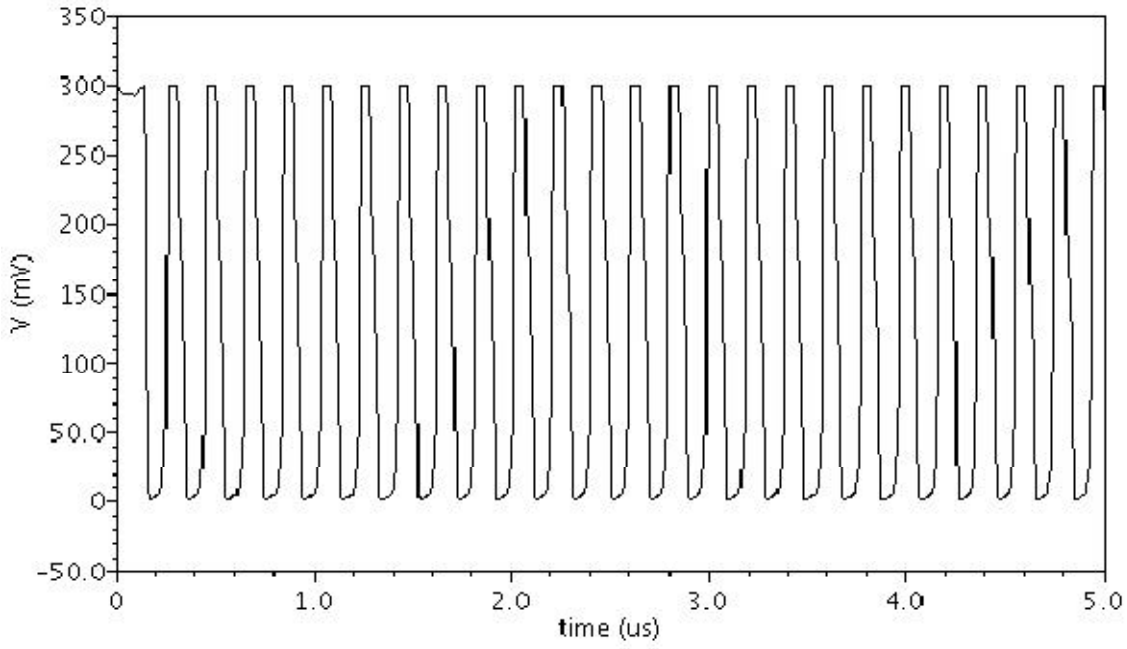


Figure 5.3: Transient response of the proposed ring oscillator @ 5.12 MHz

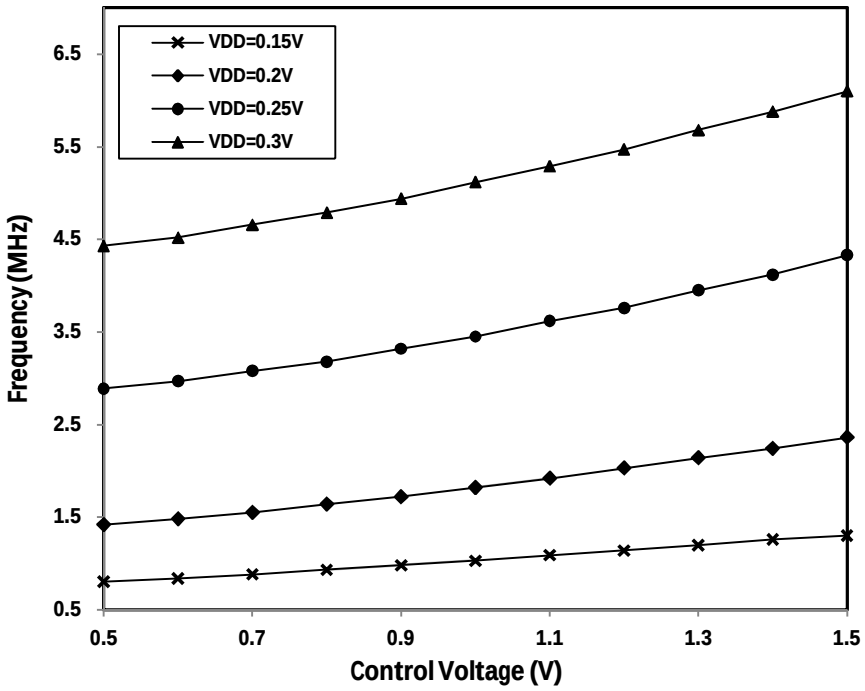


Figure 5.4: Frequency tuning characteristic of the proposed VCO

5.5 Comparison

As the proposed VCO is designed to offer ultra-low power dissipation, the results show that the power consumption of the oscillator is only 24 nW. This result is superior to any previously reported oscillator designed for RFID transponders. For comparison, Table 5.2 lists some of the existing oscillators designed for RFID applications. All designs are based on UHF RFID standards EPC C1 G2 except for [11] which is based on ISO 18000-6. The new VCO utilizes minimum number of stages taking advantage of differential structure reducing both power and area. The oscillator is capable of operating at a supply voltage of 0.3 V which is much lower than other designs. This type of low voltage circuits can be proven advantageous for RFID applications as minimum power dissipation is of main concern with low-to-moderate performance.

Table 5.2: Comparison with Existing Designs

Design	*Type of Oscillator*	*Power Supply*	*Frequency*	*Power consumption*	*Process*
[1]	Relaxation	0.6 V	5.65 MHz	720 nW	0.13-µm
[2]	Relaxation	0.5 V	3.5 MHz	7 µW	0.18-µm
[10]	Single-ended Ring	0.9 V	1.28 MHz	440 nW	0.14-µm
[11]	Single-ended Ring	1.5 V	500 KHz	0.4 µW	0.35-µm
[12]	Relaxation	0.8 V	2.52 MHz	320 nW	0.13-µm
This work	Differential Ring	0.3 V	5.12 MHz	24 nW	90-nm

CHAPTER VI

PHASE NOISE ANALYSIS

6.1 Frequency Instability

The output of an idea oscillator can be expressed as $V_{out}(t)=V_0 cos\ [\omega_0 t+\Phi_0]$ where the maximum output voltage swing V_0, output frequency ω_0 and phase reference Φ_0 are constants. For an ideal oscillator operating at ω_0, the spectrum consists of an impulse, as shown in Figure 6.1. The output of a practical oscillator is generally given by [26]

$$V_{out}(t)=V_0\ .\ [1+A(t)]\ .\ f\ [\omega_0 t+\Phi(t) \quad \textbf{(6.1)}$$

where $A(t)$ and $\Phi(t)$ are functions of time representing random fluctuations in the output amplitude and phase, respectively. As a consequence of the fluctuations in amplitude and phase, the spectrum of a practical oscillator exhibits sidebands close to the frequency of oscillation ω_0, and its harmonics, as shown in Figure 6.1. These sidebands are generally referred to as *phase noise* sidebands.

6.2 Phase Noise

To quantify phase noise, we consider a unit bandwidth at an offset $\Delta\omega$ with respect to ω_0, calculate the noise power in this bandwidth, and divide the result by the carrier power. Phase

noise is conventionally given in the units of decibels below the carrier per Hertz (dBc/Hz) and is defined as [26] [27]

$$L\{\Delta\omega\}=10\log\left[\frac{P_{sideband}[\omega_0+\Delta\omega]}{P_{carrier}}\right] \quad \textbf{(6.2)}$$

where the numerator represents the single sideband power at a frequency offset Δω, from the carrier in a measurement bandwidth of 1Hz as shown in Figure 6.1, and the denominator represents the total power under the power spectrum.

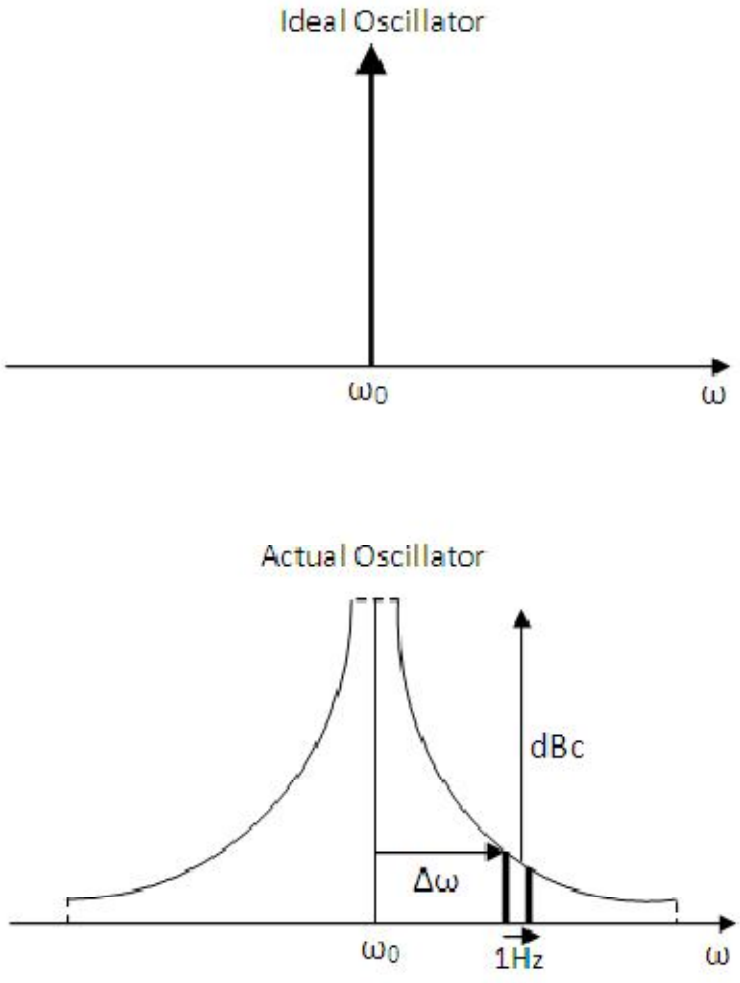


Figure 6.1: The phase noise in an oscillator

If $L\{\Delta\omega\}$ is plotted for a free-running oscillator as a function of $\Delta\omega$ on logarithmic scales, regions with different slopes may be observed, as shown in Figure 6.2. The first region is the $1/f^2$ region, which is due to the thermal noise in the MOS devices in the oscillator. The second region, $1/f^3$ is due to up conversion of low frequency noise, such as flicker noise from MOS devices. The intercept point of the $1/f^2$ and $1/f^3$ asymptotes is referred as the $\omega_{1/f}{}^3$ corner. At large offset frequencies, there is a flat noise floor.

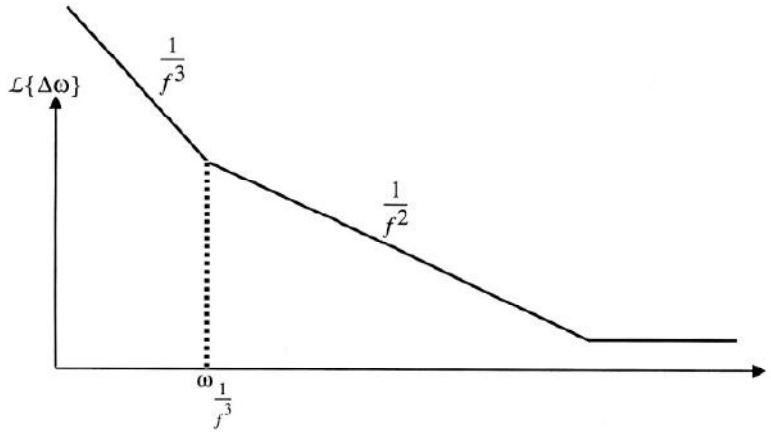


Figure 6.2: A typical phase noise plot of a free-runing oscillator.

6.3 Time-Variant Phase Noise Model

An oscillator can be treated as a system that converts voltages and currents to phase. For small perturbations this is a linear system. It is also a time-variant system no matter how small the perturbations are. As an example, we consider the five-stage single-ended ring oscillator with a single current source on one of the nodes, as shown in Fig. 6.3. A current source consisting of an impulse of current with area Δq (in coulombs), occurring at time $t=\tau$, will cause an instantaneous change in the voltage of that node which is given by [26]

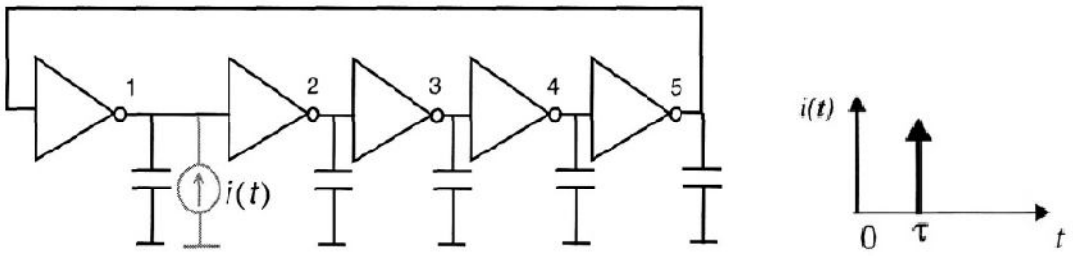


Figure 6.3: CMOS 5 stage inverter chain ring oscillator

$$\Delta V = \frac{\Delta q}{C_{node}} \tag{6.3}$$

where C_{node} is the effective capacitance on the node of interest at the time of charge injection. This corresponds to an equivalent shift in the transition time for small changes in voltage. Hence, the change in the phase, Φ(t) can be expressed as,

$$\Delta \Phi \propto \frac{\Delta V}{V_{swing}} = \frac{\Delta q}{q_{max}} \tag{6.4}$$

where $q_{max}=C_{node}V_{swing}$ and V_{swing} is the voltage swing across the capacitor. The time-dependency of the proportionality constant can be visualized by considering two extreme cases. In the first extreme, the impulse is injected during an output transition which results in a large phase shift. In the other extreme case, the impulse is injected while the output is saturated either to supply or ground. This impulse will have minimal effect on the phase of the oscillator, as shown in Fig. 6.4.

Unlike the amplitude variation, once the phase shift is introduced into the oscillator its effect persists indefinitely, since subsequent transitions are shifted by the same amount. Thus, the

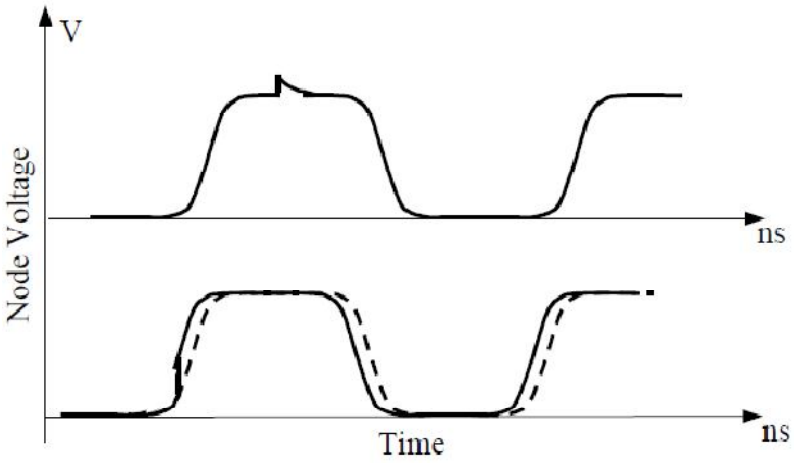


Figure 6.4: Waveforms for injection during transition and peak.

phase response of an oscillator to an impulse is a time varying step. As long as the change introduced in the voltage due to the current impulse is small, the resultant phase shift is linearly proportional to the injected charge, and hence the transfer function from current to phase is linear. However, the time variant nature of the system does not disappear even for small perturbations.

The unit impulse response of the system can be defined as the amount of phase shift for a unit current impulse. Based on the foregoing argument, the following time dependent impulse response is obtained [26]

$$H_{\Phi}(t, \tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}}\, u(t-\tau) \qquad \textbf{(6.5)}$$

Now, Φ (t) can be calculated using the superposition integral [26]

$$\Phi(t) = \int_{-\infty}^{\infty} H_{\Phi}(t\,,\,\tau) i(\tau) d\tau = \int_{-\infty}^{t} \frac{\Gamma(\omega_0\tau)}{q_{max}} i(\tau) d\tau \qquad \textbf{(6.6)}$$

where *i(t)* represents the input noise current injected into the node of interest. Here, the integration arises from the closed loop nature of the oscillator. For a white noise current source, the argument of the second integral of eq. (6.6), [26]

$$\psi(t) = \frac{\Gamma(\omega_0 \tau)}{q_{max}} i(t) \tag{6.7}$$

has the following power spectrum

$$S_{\psi}(f) = \Gamma_{rms}^2 \frac{i_n^2/\Delta f}{2q_{max}^2} i(t) \tag{6.8}$$

where $i_n^2/\Delta f$ represents the single-sideband power spectrum of the noise current source and Γ_{rms}^2 is the root mean square (RMS) value of the impulse sensitivity function (ISF) discussed in the next section. *Φ(t)* is related to ψ(t) through an ideal integration; therefore, the single sideband phase noise spectrum for a ring oscillator with *N* identical stages is [26]

$$L\{\Delta f\} = N \cdot \frac{\Gamma_{rms}^2}{16\pi^2 f_{off}^2} \cdot \frac{i_n^2/\Delta f}{q_{max}^2} \tag{6.9}$$

where f represents the frequency offset from the carrier. In the case of multiple noise sources, $i_n^2/\Delta f$ represents the total current noise on each node and is given by the power sum of individual sources.

6.4 The Impulse Sensitivity Function

To calculate the phase noise using eq. (6.9), the RMS value of the ISF is needed. This can be done by finding the ISF through simulation. However in this section a closed-form equation is explained for the RMS value of the ISF of ring oscillators which makes such simulations unnecessary.

To estimate *Γrms*, we assume that the ISF is triangular in shape and that its rising and falling edges are symmetric as shown in Fig. 6.5. The ISF has a maximum of $1 / f_{max}$, where *f'* is the maximum slope of the normalized waveform. Also the width of the triangles is *2/f'* and hence the slope of the sides of the triangles is +1. Therefore *Γrms* is given by [26] [28]

$$\Gamma_{rms}^2 = \frac{1}{2\pi}\int_0^{2\pi} \Gamma^2(x)dx = \frac{4}{2\pi}\int_0^{1/f'_{max}} x^2\,dx = \frac{2}{3\pi}\left(\frac{1}{f'_{max}}\right)^3 \qquad \textbf{(6.10)}$$

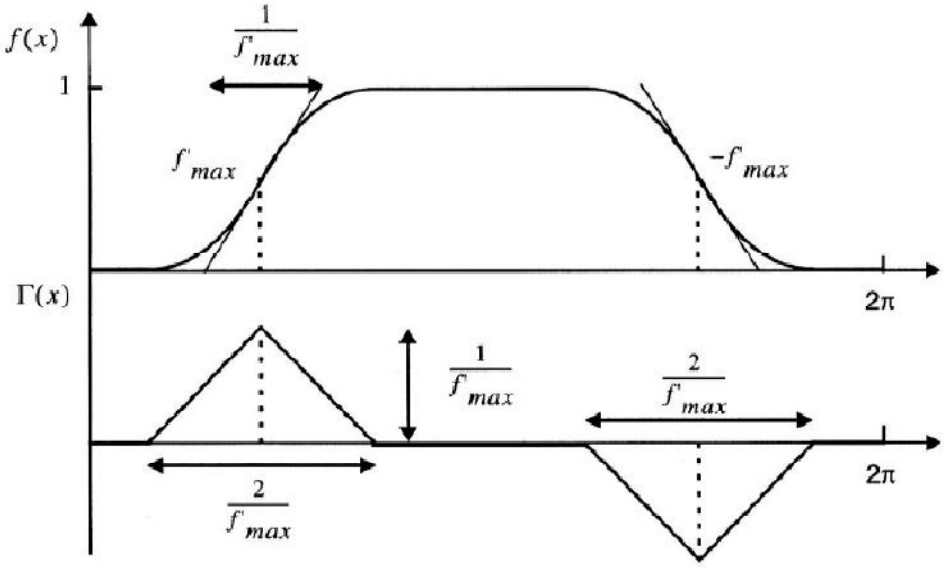


Figure 6.5: Approximate waveform and ISF for ring oscillator

6.5 *Phase Noise Analysis of the Proposed Oscillator*

The phase noise analysis is performed based on the noise model proposed in [26] discussed in section 6.3. The phase noise of a ring oscillator can be defined as:

$$\pounds\{f_{off}\} = N \cdot \frac{\Gamma_{rms}^2}{16\pi^2 f_{off}^2} \cdot \frac{i_n^2/\Delta f}{C_L^2 V_{pp}^2} \qquad \textbf{(6.11)}$$

where f_{off} is the offset frequency, Γ_{rms} is the rms value of the impulse sensitivity function (ISF) defined as $\frac{1}{2\pi}.\int_0^{2\pi}\Gamma(x)dx$, N is the number of noise stages, i.e., N=4 for a two-stage differential ring oscillator since the analysis is based on each half stage and V_{PP} is the peak-to-peak output amplitude. The noise current Power Spectral Density of the active devices in the ring oscillator can be modeled as

$$\frac{i_n^2}{\Delta f} = 4KT\gamma(g_{mn1}+g_{mp1}+g_{mp2}) \qquad \textbf{(6.12)}$$

$$g_m = \frac{1}{nU_T} I_0\left(\frac{W}{L}\right) e^{\frac{V_{DD}-V_{TH}}{nU_T}} \qquad \textbf{(6.13)}$$

where g_m is the transconductance of the transistor. Phase noise performance can be improved by either increasing the carrier power or reducing the noise power. eq. (5) dictates that the phase noise performance can be improved by allowing the output swing to reach the maximum. Large output amplitude increases the carrier power and improves the signal-to-noise ratio (SNR) at the expense of more power dissipation. While carrier power can be increased by making the output amplitude large, noise power can be reduced by choosing proper device

dimension and bias condition. When the transistors are biased to operate in weak inversion, the small output swing is expected to give a rise to the phase noise but it does not get worse due to the reduction in noise power as a result of less noise current generation of the devices at low supply voltage. In addition to the intrinsic device noise, the noise sensitivity of the oscillator should also be taken into consideration to predict the phase noise performance. In conventional strong inversion mode ring oscillators, excessive tuning gain often increases the sensitivity of the oscillator. Phase noise performance can be improved by making the oscillator less sensitive to the noise generated by the control lines. The best situation would be maintaining a moderate tuning gain without impairing the tuning range. In the proposed weak inversion mode oscillator, the lower tuning gain makes the oscillator less sensitive to the voltage at the control line which helps to maintain a moderate phase noise performance in spite of low swing.

6.6 Simulation Results

The phase noise of the VCO was estimated using SpectreRF simulations (Fig. 6.6). The phase noise at the center frequency of 5.12MHz with a supply voltage of 0.3V is -80.43 dBc/Hz at 10 KHz offset . When the supply voltage is increased to 0.4V and 0.5V, the phase noise is -68.45 dBc/Hz and -55.67 dBc/Hz at 10KHz offset, respectively. The results indicate that the phase noise performance of the ring oscillator operating in weak inversion is dominated by the noise current generation of the transistors which increases with increasing the supply voltage.

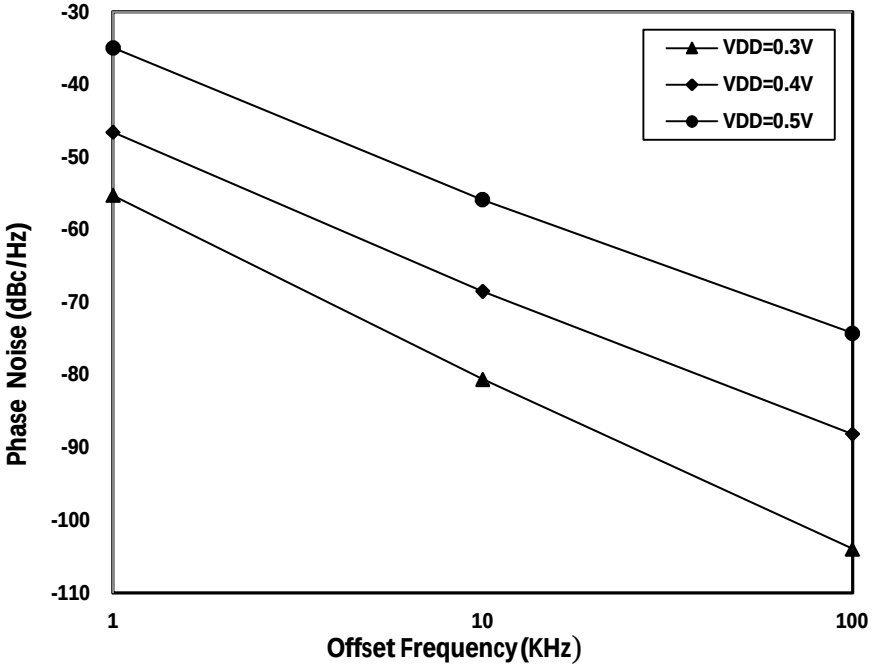


Figure 6.6: Phase noise extracted from SpectreRF simulations.

CHAPTER VII

CONCLUSIONS

A new two-stage CMOS voltage-controlled ring oscillator has been presented in this work. The delay cells are biased in weak version region to ensure ultra-low power operation. It has been shown that the proposed oscillator operates in weak inversion with frequency tuning characteristics. A significant power reduction is achieved by optimizing transistor current and sizing. It has been demonstrated that the proposed VCO is much better than the other existing structures in terms of power consumption. Designed in a 90-nm CMOS technology, the circuit generates oscillation signals at 5.12 MHz and consumes only 24 nW with a 0.3 V power supply. Table 7.1 lists the performance summary of the proposed VCO. The application of such an oscillator would minimize the area and cost of the transponders, meeting the low-cost and low-power requirements of RFID systems

Table 7.1: Performance summary of the proposed VCO

Technology	90-nm CMOS
Area	10.66 μm x 10.76 μm
Tuning Range	4.43-6.15 MHz
Tuning Gain	1.5 MHz (average)
Supply Voltage	0.3V
Current Consumption	80nA (average)
Phase Noise (@10K)	-80.43 dBc/Hz

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APPENDIX A: PERMISSION FROM CO-AUTHORS

In this section a letter that permits the author of this thesis to use papers that were co-written by Dr. C. Chen and Guoyan Ren is attached.

Permission to Use Previously Accepted / Submitted Papers

Dr. Chunhong Chen and Guoyan Ren give permission to Suzana Farzeen to include the following papers into her Master's thesis.

1) Paper accepted in lecture session of MWSCAS'10, Aug 2010, Seattle, Washington, USA, entitled:

   Suzana Farzeen, Guoyan Ren and Chunhong Chen, "An Ultra-Low Power Ring Oscillator for Passive UHF RFID Transponders", in Proc. 53rd IEEE International Midwest Symposium on Circuits and Systems, pp. 558-561, Aug. 1st-4th, 2010.

2) Paper to be submitted, entitled:

   Suzana Farzeen and Chunhong Chen, "A Nano-Power Ring Oscillator Design for RFID Applications".

Sincerely,

Dr. Chunhong Chen

Gouyan Ren

VITA AUCTORIS

Suzana Farzeen was born in 1986 in Dhaka, Bangladesh. She graduated from Viqarunnisa Noon School and College in 2003. From there she went on to the North South University, Dhaka, Bangladesh where she obtained a BS degree in Computer Engineering. She is currently a candidate for the Master of Applied Science degree in Electrical Engineering at the University of Windsor and hopes to graduate in Summer 2010.