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TSV Equivalent Circuit Model using 3D Full-Wave Analysis

By

Zheng Gong

A Thesis

Submitted to the Faculty of Graduate Studies through the Department of **Electrical and Computer Engineering** in Partial Fulfillment of the Requirements for the Degree of **Master of Applied Science** at the University of Windsor

Windsor, Ontario, Canada

2014

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TSV Equivalent Circuit Model using 3D Full-Wave Analysis

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DECLARATION OF ORIGINALITY

I. Co-Authorship Declaration

I hereby declare that this thesis paper incorporates the outcome of a joint research in collaboration with, and under the supervision of, Dr. Rashid Rashidzadeh, with the review and revision being provided by Dr. Rashid Rashidzadeh.

I am aware of the University of Windsor Senate Policy on Authorship and I certify that I have properly acknowledged the contribution of other researchers to my thesis, and have obtained written permission from each of the co-author(s) to include the above material(s) in my thesis. I certify that, with the above qualification, this thesis, and the research to which it refers, is the product of my own work.

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	Conference (DAC	C), June 1-5,		
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	Title: TSV Equi	ivalent Circuit	Prepared	for
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ABSTRACT

This work presents a study to build lumped models for fault-free and faulty Through Silicon Vias (TSVs). Three dimensional full-wave simulations are performed to extract equivalent circuit models. The effects of parametric and catastrophic faults due to pin-holes, voids and open circuits on the equivalent circuit models have been determined through 3D simulations. The extracted TSV models are then used to conduct delay tests to determine the required measurement resolution to detect TSV defects. It is shown that the substrate conductivity has a considerable effect on TSV fault characterization. It is also shown that, regardless of the substrate type, even a relatively large void does not alter the TSV resistance or its parasitic capacitance noticeably at 1GHz solution frequency. An on-chip test solution for TSV parametric faults requires a dedicated high resolution measurement circuit due to the minor variations of TSV circuit model parameters.

DEDICATION

To my parents, supervisors and friends

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I would like to thank my supervisors, Dr. Rashid Rashidzadeh and Dr. Esam Abdel-Raheem, for their support, encouragement and valuable suggestions. I greatly benefited from discussions with them during my research work. Their creativeness, diligence and passion towards research inspired me a lot when I had a hard time in my research. I also would like to thank Dr. Mitra Mirhassani and Dr. Reza Riahi for their valuable comments.

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LIST OF ABBREVIATIONS/SYMBOLS

Abbreviations:

ABBREVIATIONS	DESCRIPTION
TSV	Through Silicon Via
SET	Single Electron Transistor
C2C	Chip to Chip
W2W	Wafer to Wafer
CMP	Chemical Mechanical Polishing
BEOL	Back End of Line
HFSS	High Frequency Structural Simulator
IC	Integrated Circuit
CMOS	Complementary Metal–Oxide–
CAD	Semiconductor
ADS	Computer-Aided Design
	Advanced Design System

Symbols:

Symbols	DESCRIPTION
h _{TSV}	TSV height
ρ_{TSV}	TSV Resistance per unit
L_{TSV}	TSV Inductance per unit
C_{TSV}	TSV Capacitance per unit
G_{TSV}	TSV Admittance per unit
C _{di}	Dielectric Capacitance
t _{di}	Dielectric Thickness
σαί	Silicon bulk conductivity
δ_{TSV}	Skin depth of TSV
- / \/	

Chapter 1

Introduction and Background

1.1 Three Dimensional Integrated Circuits

1.1.1 A brief introduction to Three Dimensional Integrated Circuits

Integrated circuit [1] technology is probably one of the most significant invention in the past century. It is considered the backbone of progress and technology. In addition to Electrical Engineering, other fields such as medical equipment, auto industry, and navigation industry have all heavily benefited from the rapid progress in IC fabrication. We could not have imagined that humans could possess such powerful handsets that make it possible for people to communicate with each around the globe. We could not have imagined that navigation systems, backlit cameras, gyroscopes, web browsers and music players could be packaged in something as small as a smart phone. Moore's law predicts that the number of transistors per chip will double every 18 months [2], as shown in Figure 1.1. This allows us to meet the increasing demand for high-speed and lowpower consumer products.

However, there are many factors that will eventually limit the scaling speed of CMOS transistors [3, 4] such as physical limitation, non-deterministic behavior of small currents, quantum effects and above all the costs of fabrications and tests. It is predicted that the technology scaling will lose its benefits if the length of CMOS transistors falls below 10nm [5]. As CMOS technology scales down, the undesired effects such as power consumption caused by leakage current becomes more important [6].

Moreover, supply voltage [7], which plays a major role in the dynamic power consumption of CMOS circuits, cannot be scaled as fast as device dimensions due to fundamental limitations in decreasing the threshold voltage.



Microprocessor Transistor Counts 1971-2011 & Moore's Law

Figure 1.1 Microprocessor Transistor Counts from 1971 – 2011 [56]

Single Electron Transistor [8] (SET), FinFet Transistor [9, 10] and three dimensional IC [11] are three popular solutions that have been presented to keep up with the demand for high density integration.

Although SET devices can provide a solution to the scaling trend of Moore's law, this technology has a limited application due to temperature constraints [12]. SET circuits can operate at a temperature close to absolute zero. If the temperature increases, SET devices will suffer from background charge and their reliability will be severely compromised. Researchers are still working on this technology to design SET devices to operate at room temperature.

Although three-dimensional integration has emerged as a viable solution to the CMOS technology scaling problem, the concept of three-dimensional integration is not new. The first U.S. patents on 3D-IC integration was issued more than 50 years ago. The fabrication technology at that time was not mature enough to implement 3D ICs.

Three dimensional ICs contain integrated circuits stacked vertically and connected by Through Silicon Vias (TSVs) [13], as shown in Figure 1.2 [14].



Figure. 1.2 Three-dimensional IC [14]

TSV technology as compared to conventional wiring technology reduces the distance between connected nodes [15] and lowers interconnect parasitic capacitances [16], as shown in Figure 1.3 [17]. In three-dimensional integration, shorter wires are needed for interconnects as compared to 2D integration. This reduces the complexity of the entire system [18]. As a result,



Figure. 1.3 Wire connections comparison between 2D IC and 3D IC [17]



Figure. 1.4 Stacked devices using C2C integration [19]

three-dimensional integration can support higher operation frequency and lower power consumption. Figure 1.4 [19] shows TSV fabrications, for stacked devices using chip-to-chip (C2C) integration.

1.1.2 Three-dimensional IC fabrication process

In two-dimensional IC, all components are at the same plane while in threedimensional IC, components are in different planes connected by TSVs. TSV as an enabling technology plays a critical rule in 3D IC integration.

Figure 1.5 [20] shows the fabrication process for three-dimensional ICs.



Figure. 1.5 Fabrication process of 3D ICs [20]

TSV is a vertical electrical connection passing through a silicon wafer or die. TSV fabrication is commonly completed in four steps [20]:

- I. Deep silicon etching: This is to make holes in a silicon substrate and prepare it for copper injection.
- II. Via oxide deposition: To deposit and insulate the copper from substrate
- III. Copper plating: To inject liquid copper
- IV. CMP+BEOL: In this step the wafer surface is polished.

After TSV fabrication, the bonding process starts, including:

- I. Temporary carrier bonding.
- II. Back side thinning: This to thin the wafer and allow access to the TSV.
- III. Expose copper nails: To expose TSV copper nails for bonding.
- IV. Dicing.
- V. Permanent bonding.

1.1.3 TSV structure

Figure 1.6 shows a fault-free TSV and a TSV with typical structural defects.



Figure 1.6. TSV structures (a) Fault free (b) Faulty.

- I. Passivation layer: A layer that separates the metal layer from TSV bump. This layer protects the TSV against environmental effects.
- II. Metal layer: This is a layer for interconnects to connect TSV to other components such as transistors.

- III. Active layer: Usually made of silicon with bulk conductivity where active components are fabricated.
- IV. Keep out zone: Commonly considered to minimize the effect of TSV stress on active circuits.
- V. Copper bump: To create a small pad for TSV bonding.
- VI. Dielectric: Usually made of silicon dioxide to insulate the TSV from substrate.
- VII. TSV body: Usually made of copper.
- VIII. Substrate: Usually made of silicon. Bulk conductivity of the substrate has a significant effect on the whole TSV structure's performance, which will be discussed later in this paper.

TSVs can suffer from various types of defects [21, 22] such as pin-holes and voids that can affect the performance parameters of 3D ICs significantly. Common TSV defects include:

- I. Voids: These are small cavities that have not been filled with copper. Voids affect the physical integrity of TSVs.
- II. Open defects: In this case TSV acts like a capacitor rather than an interconnect.
- III. Pinholes: When there is a hole in the insulator around the TSV causing a leakage current to follow between TSV and substrate. This usually occurs when there is a big difference between the thermal expansion coefficient of the dielectric and the substrate.

Figure 1.7 shows a fabricated TSV and its common defects [17].

1.2 Challenges in Three-dimensional testing methods



Although TSV technology has many advantages, there are also many challenges.

Figure. 1.7 Fabricated fault-free and faulty TSV [17]

TSVs are fragile [23] with small areas for bonding or probing. As a result, TSV probing for the purpose of testing has become a major challenge. Figure 1.8 [24] shows the damages on TSV after a probe touchdown. Efficient design-for-test methodologies for 3D integrated circuits have to be developed to minimize the costs and the test time for 3D ICs. How to conduct pre-bond tests on a bare die prior to integration into a die-stack and how to design a robust test access mechanism to cover TSV defects are among the main issues that have to be addressed to develop a test solution for 3D ICs. Testing TSV interconnects requires development of new design-for-test techniques and test access mechanisms [25, 26]. Conventional wafer probes cannot be readily used to access TSVs on 3D ICs due to excessive force exerted by these probes that can undermine the physical integrity of TSV structures [27]. Furthermore, wafer probe technology cannot support the pitch requirement of high density TSV probing [28].



Figure. 1.8 Damages on TSV after probe touchdown [20]

To keep TSVs' integrity, test technology needs to find solutions to reduce the damage caused by probe scrub marks. Advanced probing techniques are developed to minimize the effects of probing on TSVs.

I. MEMS Probe

In [29], MEMS technology has been utilized to address the problem of direct TSV probing. MEMS technology has also been used to design low-contact-force high-pitch probes supporting high frequency operation. The performance of MEMS probes is affected by thermal expansion and structural fatigue caused by cyclical loadings. Further improvement is needed to employ MEMS probes to conduct manufacturing tests in production lines. A MEMS based probe is shown in Figure 1.9 [29].

It can be seen that the contact force on the top surface of the MEMS probe is low, thus it can be used to probe TSVs without affecting their integrity.



Figure. 1.9 MEMS Probe and its Contact Force Distribution [29]

II. Nano-Fiber Probe

Nano-Fiber Probe [24] is also proposed as a solution to reduce the contact force on TSVs. Figure 1.10 shows the physical structure of a nano-fiber probe.



Figure. 1.10 Nano-fiber Probe for TSV probing [24]

III. Contactless Probe

Contactless TSV probes have also been proposed in the literature to ensure the physical integrity of TSVs during the test phase [30]. The advantage of the contactless probe is that there is no need for the probe to touch the TSV. These probes generally operate based on principles of electric or magnetic coupling. The probe is positioned close to the desired TSV where a small capacitor or a coreless transformer is formed

between the probe and the TSV. This probing method supports high density and lowpitch probing and eliminates the risks of TSV structural integrity degradation. Detecting circuits have to be added to the device under testing to implement this probing technique. The structure of the contactless probe is shown in Figure 1.11. [30]



Figure. 1.11 Structure of Contactless Probe [30]

1.3 TSV test solutions proposed in the literature

TSV test architectures based on standard IEEE 1500 and IEEE 1149.1 die wrappers have been developed to cover TSV defects [4]. Boundary scan based test methods for TSVs rely on full controllability at the inputs and observability at the outputs. It is assumed that TSV defect mechanisms are similar to failures affecting wiring networks [31]. Therefore, the available automatic test pattern generators for interconnects are utilized to generate test vectors for TSVs and the die wrappers are used as test access mechanisms to apply the test vectors and to observe the outputs. The die wrapper [32] based TSV test approach can be employed successfully to detect hard faults such as open and short faults. Most of the TSV test and access methods in the literature have been developed to cover catastrophic TSV faults. While capturing these faults could understandably be the highest priority, a comprehensive test methodology for TSV has to cover parametric faults as well. Developing tests for TSV parametric faults is quite challenging and requires accurate TSV fault characterization [33]. The frequency response of TSV interconnects is commonly affected by TSV structural defects such as pin-holes. These defects cannot be detected readily by conventional interconnect tests using standard die wrappers. A test method to cover TSV parametric faults based on small delay measurement has been proposed in the literature [34]. In this method, a pair of TSVs are used as interconnects within a ring oscillator where the delay of the TSVs affects the oscillation frequency. Variations in the oscillation frequency from its nominal value are indications of a faulty TSV. While many TSV test methods have been presented in the literature [35, 36, 37, 38, 39, 40], the lack of an accurate model to characterize variations in TSV performance parameters limits our ability to determine the coverage of test methods and to further improve their performance. In this work, TSV circuit models have been extracted using three dimensional full-wave simulations where the electric and magnetic fields are calculated within the entire 3D structure using Maxwell equations. The extracted models were used to determine the effects of pin-holes and voids on the TSV parameters to identify the required measurement resolution to cover TSV defects.

The rest of this thesis paper is organized as follows. Chapter two presents the setup used to implement a 3D TSV and shows the distribution of electric and magnetic fields within a fault free TSV; the circuit model representing the fault free TSV has also been extracted in this section, the effects of pin-holes and voids on field distributions under different circumstances have been presented in chapter three; the effects of substrates resistivity on the TSV equivalent circuit model is covered in chapter four; and chapter five presents simulation results indicating the required measurement resolution for TSV parametric fault detection; and finally, chapter six summarizes the results and presents the conclusions.

Chapter 2

Implemented TSV Structure and the Equivalent Circuit

2.1 CAD Tools

TSV can be modeled using transmission line theory. In [41], a scalable electrical model for TSV has been provided using analytical equations derived from physical configurations. In [42, 43], the equivalent circuit of a TSV with passive components is presented. The parameters of the components are derived through analytical equations and the results are verified by numerical simulators. These models are only limited to fault-free TSVs, but they do not take faulty TSVs into consideration. How to develop a model using an analytical approach for TSV with structural defects is a major challenge. The location and the shape of defects are not known, but even if we have this information, an accurate analytical model is still difficult to develop.

There are also some structural defects that are unique to TSVs such as pin-holes and voids, which are difficult to capture as they commonly affect TSV performance parameter rather than TSV logical function [44]. While the analytical methods developed to characterize TSV faults [45, 46] provide valuable information, they are limited since some important factors such as skin effect in TSV and eddy current within the substrate cannot be easily taken into consideration. These methods are mainly developed based on the TSV conducting body without considering the effects of the surrounding environment. As a result, they cannot be easily used to characterize the effect of TSV defects on the circuit model. For instance, it is not clear how the TSV circuit model varies if the substrate conductivity changes. TSV characterization through measurement results are equally difficult as they require full control over the injected faults such as the size of pin-holes and voids in order to measure TSV performance parameter variations.

The emergence of 3D full-wave simulation tools has opened the path for accurate characterization of 3D structures. Powerful 3D full-wave simulation tools such as High Frequency Structural Simulator (HFSS) from Ansoft and EMPro [47] from Agilent are now available to conduct simulations on three dimensional structures. It has to be noted

that HFSS generates full-wave circuit models which includes dependent sources. To model TSV in this work, low bandwidth equivalent circuits which include R,L and C components have been extracted. These models are valid at frequencies close to the HFSS solution frequency.

2.2 Why HFSS

HFSS is a finite element method solver for electromagnetic structures [48]. It is ideal for TSV fault analysis since the effect of various defects on the TSV performance parameters can be fully characterized. It can be used to determine the distribution and the intensity of electric and magnetic fields not only within the entire TSV structure but also in the surrounding medium including the dielectric and the substrate. It can also generate equivalent SPICE models for simulated 3D structures. The SPICE model can then be imported to a circuit simulator such as Agilent's Advanced Design System [49] (ADS) or Cadence's virtuoso schematic for detailed analysis.

2.3 Implemented TSV Structure

Fig. 2.1(a) shows the implemented fault free TSV within a silicon-box surrounded by an air-box in the HFSS environment. TSV interconnects share some of the common defects of conventional 2D interconnects resulting in short and open faults.



Figure 2.1 (a) Implemented fault free TSV for 3D simulations

Table 2.1 shows the parameters of the implemented TSV structure.

Parameters	Values	Parts	Materials
TSV Length	50 um	TSV body	Copper
TSV Radius	2.5 um	Dielectric	Silicon
			Dioxide
Dielectric Thickness	0.5 um		
Silicon box	$10\Omega.cm$ or		
Conductivity	1mΩ.cm		

Table 2.1 Parameters of the implemented TSV structure

The silicon box has been chosen to have resistivity of 10Ω .cm or conductivity of 10 Siemens per meter. The effect of highly conductive substrates, known as epi-substrates with conductivity of 100000 Siemens per meter (1m Ω .cm), on TSV equivalent circuit model will be covered in Chapter 4. The implemented TSV for this work is a copper bar 50 µm in length with cross-section diameter of 5 µm. It is covered with a layer of silicondioxide with a 0.5 µm thickness to insulate the TSV from the substrate. The top and bottom plates of the TSV are selected as wave port terminals to apply the excitations. It can be seen in Fig. 2.1(b) that the electric field is uniformly distributed along the faultfree TSV within the substrate.



Figure 2.1 (b) Electric field distribution of a fault free TSV

2.3.1 S-Parameters of the Implemented TSV Structure

Scattering parameters describe the linear electrical networks' behavior [50]. The implemented TSV structure is a two port system, thus we can obtain the S-parameters to determine the performance parameters of the structure. The solution frequency was set to 1.00GHz and the frequency of stimulus was swept from 1.00MHz to 1.00GHz with 1.00MHz step size to extract S-parameters of the TSV.

S11 is the input port voltage reflection coefficient, S21 is the reverse voltage gain [51], and the equations are given by 2.2(a) and 2.2(b).

 $b1 = S11 \times a1 + S12 \times a2 (2.2 a)$ $b2 = S21 \times a1 + S22 \times a2 (2.2 b)$

As a result, we can derive the expressions of S11 and S21 in equation 2.3(a) and 2.3(b) from equation 2.2.

$$S11 = \frac{b1}{a1} = \frac{V_1^-}{V_1^+}$$
(2.3 a)
$$S22 = \frac{b2}{a1} = \frac{V_2^-}{V_1^+}$$
(2.3 b)

The variations of S11 parameter in Fig. 2.2(a), as expected, shows a minor insertion loss at high frequencies. This can be understood because we have both DC resistance and AC resistance between port 1 and port 2, and when the frequency is high, the AC resistance will play a more important role than the DC resistance.

The S21 graph in Fig. 2.2(b) indicates that the input signal is attenuated by less 0.004dB at 1 GHz. This is a relatively good result because we expect S21 to be close to 0.

The results of S-parameter simulation are used by HFSS to generate a two-port equivalent SPICE model for the implemented TSV by HFSS.



Figure 2.2(a). Extracted s-parameters of the TSV. S11



Figure 2.2(b). Extracted s-parameters of the TSV. S21
2.3.2 Extracted Equivalent Circuit of a TSV

The SPICE model was imported to ADS environment to create a schematic diagram representing the TSV. The generated low-bandwidth circuit model which is symmetrical with respect to the TSV terminals is shown in Fig. 2.3



Figure 2.3. Low bandwidth lumped circuit model representing a fault free TSV generated by HFSS 5MHz solution frequency from 3D full wave simulation results.

Though there are many components in Figure 2.3 to represent a simple TSV, which is just a small copper bar, each of them can be explained. We classify these components into two categories:

• Components connecting TSV terminals

There are resistors and inductors in series R1 and L1 between the TSV input and output terminals. The presence of a small resistances, R1, is expected because of the high conductivity of copper used to implement the TSV. The impedance between the TSV terminals cannot be modeled by a small resistor alone. At high frequencies, the impedance of copper increases due to the skin effect [52], which reduces the effective cross section of the TSV contributing to the conduction of current. The impedance elevation caused by skin effect is modeled by an inductor, L1, in the TSV circuit model.

Components connecting TSV terminal and ground.

The high resistors, R3 and R4, connecting each terminal to ground are due to the presence of dielectric between the TSV and the substrate which is connected to the ground. There are a pair of resistor and capacitor in series connection, R5 in series with C1 and R6 in series with C2, connecting each TSV terminal to ground. TSV metal at each port and the substrate can be considered as two conducting plates of a capacitor separated by the dielectric between them, which is by definition a capacitor. The small resistors R5 and R6 in series with the capacitors represent the resistance of the TSV metal from its terminals to the surface of the dielectric layer.

2.4 Analytical Verification

Here we only develop analytical approaches for a fault-free TSV.

A fault-free TSV can be modeled as a transmission line; we can develop the TSV's analytical model with transmission line's theory. Because the TSV is symmetrical, it can be represented by the transmission line model shown in Figure. 2.4.



Figure. 2.4 TSV transmission line model

In Figure 2.4, the voltage between port a and c, b and d is V(l, t), $V(l+h_{TSV}, t)$ respectively. If we apply Kirchhoff's voltage law, we get equation (2.4)

$$-\frac{V(l+h_{TSV},t)-V(l,t)}{h_{TSV}} = \rho_{TSV} \times I\left(l+\frac{1}{2}h_{TSV},t\right) + L_{TSV} \times \frac{\partial I\left(l+\frac{1}{2}h_{TSV},t\right)}{\partial t}$$
(2.4)

Equation (2.4), if $h_{TSV} \rightarrow 0$, can be written as

$$-\frac{\partial V(l,t)}{\partial l} = \rho_{TSV} \times I(l,t) + L_{TSV} \times \frac{\partial I(l,t)}{\partial t}$$
(2.5)

after applying Kirchhoff's current law, we can

$$-\frac{I(l+h_{TSV},t)-I(l,t)}{h_{TSV}} = G_{TSV} \times V\left(l+\frac{1}{2}h_{TSV},t\right) + C_{TSV} \times \frac{\partial V\left(l+\frac{1}{2}h_{TSV},t\right)}{\partial t}$$
(2.6)

From equation (2.6), if $h_{TSV} \rightarrow 0$, we can write

$$-\frac{\partial I(l,t)}{\partial l} = G_{TSV} \times V(l,t) + C_{TSV} \times \frac{\partial V(l,t)}{\partial t}$$
(2.7)

From equation (2.5) and (2.7), we can derive (2.8) and (2.9)

$$\begin{cases} -\frac{dV_s}{dh_{TSV}} = (\rho_{TSV} + jwL_{TSV})I_s \quad (2.8) \\ -\frac{dI_s}{dh_{TSV}} = (G_{TSV} + jwC_{TSV})V_s \quad (2.9) \end{cases}$$

If we take the derivation of (2.8) and replace $\frac{dI_s}{dh_{TSV}}$ from (2.9), we get (2.10)

$$-\frac{d^2 V_s}{dl^2} - \gamma^2 V_s = 0 \ (2.10)$$

Solving equation (2.10), results in equation (2.11), (2.12).

$$\begin{cases} \gamma = \sqrt{(\rho_{TSV} + jwL_{TSV})(G_{TSV} + jwC_{TSV})} (2.11) \\ Z_0 = \sqrt{\frac{\rho_{TSV} + jwL_{TSV}}{G_{TSV} + jwC_{TSV}}} \end{cases}$$
(2.12)

TSV resistances can be modeled with two components of AC resistance and DC resistance.

DC resistance is easy to calculate, the equation is given in (2.13)

$$R_{DC_TSV} = \rho_{TSV} \times \frac{h_{TSV}}{\pi \times (\frac{d_{TSV}}{2})^2} \quad (2.13)$$

In (2.13), $\rho_{TSV} = 1.724 \times 10^{-8} \Omega.m$, $h_{TSV} = 50 \mu m$, $d_{TSV} = 5 \mu m$.

If we take these three values into equation (2.13), then we can get the DC resistance of the TSV, which is 0.043 Ω . It has to be noted that the extracted resistance by CAD tools takes both the AC resistance and the DC resistance to extract the circuit models.

The skin depth of TSV, δ_{TSV} can be calculated with equation (2.14) [53]

$$\delta_{TSV} = \sqrt{\frac{2\rho_{TSV}}{\omega\mu_{TSV}}} \times \sqrt{\sqrt{1 + (\omega\rho_{TSV}\varepsilon_0)^2} + \omega\rho_{TSV}\varepsilon_0} \quad (2.14)$$

The skin depth for the TSV at 1GHz operation frequency is 2.09 μm .

$$R_{AC_{TSV}} = \frac{\rho_{TSV} \times h_{TSV}}{\pi \times (d_{TSV} \times \delta_{TSV}' - (\delta_{TSV}')^2) \times (1+Y)}$$

Where $\delta_{TSV}' = \delta_{TSV} (1 - e^{\frac{-d_{TSV}}{2 \times \delta_{TSV}}})$

The TSV body and the substrate are separated by the dielectric, which is by definition the capacitor, and its shape is a cylinder.



Figure.2.5 Cylindrical capacitor between TSV conducting body and

For the cylindrical capacitance, we have equation 2.15 to calculate the capacitance

$$C = \frac{2\pi\varepsilon h_{TSV}}{\ln\left(\frac{b}{a}\right)} \quad (2.15)$$

Where "*a*" represents the radius of the TSV and "*b*" is equal to the inner thickness of the substrate. Taking all this information into consideration, we get the capacitance is equal to 0.0594 pF, which has a small variation with the results given by the CAD tool.

2.5 Summary

This chapter presents the implemented 3D TSV structure in HFSS environment for 3D full wave analysis. The equivalent circuit models are extracted from the S-parameters, and imported to ADS environment for further circuit analysis. Analytical explanations for the structure and parameters of the TSV's equivalent circuit are also given in this chapter. The mathematical model is developed with transmission line theory. The components in the TSV circuit models meet the analytical expectations.

Chapter 3

Effects of Faults on TSV Model Parameters

As mentioned in Chapter 1, there are typical defects such as pin-holes, voids and open circuits. We will study these defects in this chapter. In the real world, pin-holes or voids or opens cannot be added manually to TSVs, we cannot control the position of the pin-holes or voids, the size of the pin-holes or voids, or other key parameters to analyze those faults. While with HFSS, we can easily deal with these kinds of faults. For example, to create a void fault, we can simply extract a small part of the inner side of the TSV body; to create an open fault, we can cut off the TSV body. Taking these advantages into consideration, we can study different types of faults to develop a solid model for TSV.

3.1 Effects of Pin-holes

3.1.1 Electric field distribution of a TSV with a pin-hole

For pin-holes, we expect a much higher leakage current compared with a fault-free TSV. In the fault free TSV model, the TSV body is surrounded by a dielectric, which is usually made of silicon dioxide. As a result, the path from TSV body to ground is open. In this case, we have a very small leakage current because of the high resistance from TSV terminals to ground. While for a TSV with a pinhole, there is a path from the TSV body to ground, which connects TSV to the substrate directly.

A pin-hole with dimensions of $2 \mu m \times 2 \mu m$ was created to see its effects on the electric field distribution. 3D simulations were performed under the same conditions as fault free TSV.

It can be seen in Figure. 3.1 that the electric field distribution as compared to the fault free TSV is altered significantly. The field intensity is much higher within the substrate because of the open path from the TSV terminal to ground through the pin-hole.



Figure 3.1. The effect of a pin-hole with dimensions of 2 μm ×2 μm on the electric field intensity in a resistive substrate.

3.1.2 Equivalent circuit of a TSV with a pin-hole

We can calculate the resistance from TSV terminals to ground from equations 3.1 and 3.2. For a fault free TSV,

$$R_{Terminal to ground} = R_{copper} + R_{dielectric} + R_{substrate}$$
(3.1)

For a TSV with a pinhole,

$$R_{Terminal to ground} = R_{copper} + R_{substrate} (3.2)$$

Figure 3.2 (a) and (b) show the resistance from TSV terminals to ground for a fault-free TSV and a TSV with a pinhole, respectively.



Figure 3.2. Resistance from TSV terminals to ground (a) Fault-free TSV, (b) TSV with a pin-hole

For a TSV with a pin-hole, resistance of the dielectric is neglected because the pin-hole punches through the dielectric, connecting the TSV body to the substrate directly. The resistance of the dielectric is much greater than the resistance of the substrate and thus a significant fall in the resistance from TSV terminals to ground is expected.

The schematic diagram of the extracted circuit model remains almost unchanged, shown in Figure 3.3. The impedances between TSV terminals and ground, R3 and R6 in Figure. 2.3, fall sharply from $208M\Omega$ to about $23k\Omega$.



Figure 3.3. The equivalent circuit of a pin-hole with dimensions of $2 \mu m \times 2 \mu m$ on the electric field intensity in a resistive substrate.

We noticed that there is a minor difference between the impedance connecting the TSV terminals of faulty and fault free TSVs. This is an acceptable result as pin-holes in general are not in the electrical path between TSV terminals. Thus, they are not expected



Figure 3.4 Capacitance variations for pin-holes with different sizes

to affect the impedance connecting TSV terminals in the circuit model.

The overall TSV capacitance does not change significantly; the variation is only up to 14.3%. This can be understood if the nature of the TSV capacitance is taken into consideration. A cylindrical capacitor is formed between the TSV surface and the surrounding substrate that can be considered as two plates of a capacitor separated by silicon dioxide as an insulator. The pin-hole adds a resistor between the plates of TSV capacitors. If the added resistance becomes comparable with the AC resistance of the TSV capacitor, the TSV capacitance in the model will change as reported in section 4 where the effect of highly conductive substrate on the TSV model is characterized. Figure 3.4 shows the variations of capacitance to ground for different pin-hole sizes. Variations can be calculated by equation 3.1. For the case of a resistive substrate with low conductivity of 10 Siemens per meter, the variations in TSV capacitance due to the pin-hole are negligible.

Variation =
$$\frac{C_{faulty} - C_{fault-free}}{C_{fault-free}} \times 100\% (3.1)$$

In fact, the displacement current between the TSV and the substrate remains the dominant factor compared to the conduction current through the pin-hole. As a result, the TSV capacitance does not change significantly in the extracted circuit model. For resistances from TSV terminals to ground, the effect of different size pin-holes on the circuit models has been presented in Figure. 3.5.



Figure 3.5. Variations of the resistance of TSV terminals to ground in the equivalent circuit with different pin-holes for a resistive substrate with 10 Siemens per meter conductivity.

It can be seen that the resistance of the TSV terminals to the ground, R3 and R6, decreases when the pin-hole size increases. However, the relationship between resistance to ground and pin-hole size is not linear. For instance, when the size of a pin-hole increases by a factor of 2 from $1 \mu m^2$ to $2 \mu m^2$, R3 and R6 fall from $54k\Omega$ to $32k\Omega$ which is less than a twofold drop. The inductors, L3 and L4, in the path of TSV terminals to ground in Figure. 3.5 are also dependent on the size of pin-hole, and as the size of the pin-hole increases, they decrease with the same variation rate of R3 and R4. The impedance composed of R1 and L1 connecting the TSV terminals remains nearly constant.

3.1.3 Effects on pin-hole positions

The above results have been obtained for a pin-hole right at the middle of the TSV. We may wonder whether the positions of the pin-holes can also affect the parameters of the equivalent circuit. As a result, the effects of different pin-hole locations on the extracted circuit model have also been determined through simulations.

Two pinhole are created near the top and the bottom of the TSV, respectively, shown in Figure 3.6. The equivalent circuit of these two cases are shown in Figure 3.7.



Figure 3.6. (a)Pin-hole near the top. (b) Pin-hole near the bottom.



Figure 3.7. Equivalent circuit for TSV with a Pin-hole. (a) Near the top. (b) Near the bottom

The results indicate that the overall effect of pin-hole location on the circuit model parameters is negligible. When the pin-hole is chosen to be very close to a TSV terminal, variations of the equivalent circuit parameters are less than 0.1%.

3.1.4 Effects on multi-pin-holes

The effects of multi-pin-holes have also been studied. The results indicate that the total area of the pin-holes determines the circuit parameters of the TSV model and the number of pin-holes, or their distributions over the TSV do not have a noticeable effect.

3.2 Effects of Voids

3.2.1 Equivalent circuit for a TSV with a pin-hole

In a TSV with a void, we expect an increase in the resistance connecting both terminals of the TSV because part of the TSV conducting body is not formed, thus reducing the effective TSV cross section. Figure 3.8 shows the extracted circuit for TSV with a void, the cross section of which is $3 \mu m$ in diameter, extending $3 \mu m$ from the TSV surface toward the TSV body.



Figure 3.8. Equivalent circuit for TSV with a void (cross section 3 µm diameter extending 3 µm from the TSV surface toward the TSV body).

The extracted circuit model at 1GHz solution frequency shows that the equivalent circuit is the same circuit as in Figure 2.3 with almost the same parameter values. The presence of a void neither affects the TSV capacitance nor its resistance. We created voids of different sizes inside the TSV to see if there are any changes in the parameters of the equivalent circuit. Table 3.1 shows the variations of the parameters in the equivalent of different cylindrical shaped void sizes.

	R1(m	R2(R3(R4(R5(L1	C1	C2
Void Size (μm³)	Ω)	ΜΩ)	mΩ)	Ω)	Ω)	(nH)	(fF)	(fF)
0π (fault-free)	3	208	0.01	0.01	208	0.011	62.74	62.74
0.25π	3	208	0.01	0.01	208	0.011	62.74	62.74
1π	3	208	0.01	0.01	208	0.011	62.72	62.72
2.25π	3	208	0.01	0.01	208	0.011	62.72	62.72
4π	3	208	0.01	0.01	208	0.011	62.72	62.72
6π	3	208	0.01	0.01	208	0.011	62.71	62.71

Table 3.1.Variations of TSV equivalent circuit parameters with different voids fora substrate with 10 Siemens per meter conductivity.

The created voids are at the middle of the TSV. The height of all cylindrical shaped voids is $1 \,\mu$ m, with different radius ranging from $0.5 \,\mu$ m to $2.45 \,\mu$ m.

From Table 3.1 we can see that parameters of the equivalent circuit remain almost the same. The simulation results indicate that even a larger void of cylinder shape with $4.9 \,\mu\text{m}$ diameter within a TSV of $5 \,\mu\text{m}$ does not have a noticeable effect on the equivalent circuit parameters.

This seems against intuition as a void takes a portion of TSV body and is expected to have an effect on the circuit parameters, such as increasing the resistances between the TSV's terminals (R1 and L1). This result can be understood if the tendency of AC currents to be distributed over the surface of conductors is taken into consideration. At 1GHz solution frequency, where simulations have been conducted, the inner portion of the TSV does not play an important role as most of the charge carriers find their way through the surface of the TSV to flow from one TSV terminal to the other.

3.2.2 Current density distribution of a TSV with a void

Figure. 3.9(a) shows a TSV with a cylindrical void with cross-section of 3 µm diameter



Figure 3.9. (a) TSV with a cylindrical void of 3 µm diameter and 3 µm height. (b) Surface current density distribution at 1GHz.

extending $3\,\mu m$ from the TSV surface toward the TSV body.

It can be observed that the surface current density changes right after the void but it rapidly returns back to its nominal value. The void is just like a big obstacle at the center of a flowing river and the current is like the water flow, although the direction or performance of the water flowing near the obstacle will be abnormal, the general flow is mostly unchanged.

As a result, presence of voids in a TSV can be considered as a reliability issue which undermines its physical integrity. The electrical performance of TSV at high frequencies is not notably affected by voids unless they become large enough to reduce the overall AC current passing through the TSV.

3.2.3 Effects on multi-voids

The effects of multi-voids have also been studied. We created multi-voids as shown in Figure 3.10.



Figure 3.10. (a) TSV with cylindrical multi-voids. (b) TSV with one cylindrical void

In Figure 3.10 (a), we have a TSV with three cylindrical voids in series. In Figure 3.10 (b), we have one cylindrical void with the same volume. The results indicate that the total volume of the voids, the number of voids or their distributions over the TSV do not have a considerable effect on the electric performance.

3.3 Effects of Opens

3.3.1 Equivalent circuit for a TSV with an open fault

The TSV in Figure 3.11. is cut right at the middle, the gap between the two plates is $1 \,\mu m$.



Figure 3.11. TSV cut off right at the middle

The equivalent circuit of a TSV with an open fault is shown in Figure 3.12. It can be seen from Figure 3.12 that the small resistance and inductance connecting TSV terminals are replaced by small capacitances.



Figure 3.12. Equivalent circuit for a TSV with an open fault

From Figure 3.12, we note that the capacitors connecting TSV terminals to ground, C3 and C4, is almost half that of a fault-free TSV.

We expect that as the open length increases, the capacitances decrease. Because the equivalent circuit is symmetrical, we can just take one capacitor into consideration, Table 3.2 shows the capacitance (C3) connecting TSV terminals with different open lengths.

A TSV with an open fault can be treated as two-plate capacitors, when the distance between the plates increases, the capacitance will decrease.

Open Lengths (µm)	1	2	3	4	5
C3 (fF)	0.45	0.23	0.12	0.11	0.10

Table 3.2. Capacitances connecting TSV terminals with different open lengths

3.3.2 Current density distribution of a TSV with an open fault

Figure 3.13 shows the current density distribution of a TSV with an open fault.



Figure 3.13. Current density distribution of a TSV with an open fault

It is clearly shown that since the TSV is cut off and there is no current flowing from one terminal to the other.

3.4 Summary

In this typical TSV defects including pin-holes, voids and opens are studied. The equivalent circuit models and the current density distributions were also presented. The results shows that voids do not have a noticeable effect on the equivalent circuits' parameters at 1GHz solution frequency. The inner portion of the TSV does not play an important role in the conduction current due to the skin effect. For a TSV with pin-hole, the resistance from TSV terminals to ground reduces sharply due to the open path from the pin-hole to ground.

Chapter 4

Substrate Effects on TSV Model Parameters

4.1 Equivalent circuit of a fault-free TSV in a highly conductive substrate

The resistivity of the substrate has a considerable effect on TSV model parameters. For instance, if a highly conductive epi-substrate with resistivity of $1m\Omega$.cm or conductivity of 100,000 Siemens per meter is used, the resistances from TSV terminals to ground fall significantly. The circuit model of a 50 µm long TSV with 5 µm diameter within a highly conductive substrate is shown in Fig 4.1



Figure 4.1. TSV equivalent circuit models for a TSV within a highly conductive substrate with 1mΩ.cm resistivity.

As compared to the circuit model for resistive substrate in Fig. 2.3, all component values remain unchanged other than R2 and R5 which fall from 208M Ω to less than 3.2M Ω . We can calculate the resistance from TSV terminals to ground:

$$R_{Terminal to ground} = R_{copper} + R_{dielectric} + R_{substrate}$$
(3.1)

In the case of TSV in a resistive substrate, $R_{substrate}$ contributes the most to the resistance to ground. The bulk conductivity increases from 10 Siemens per meter to 10^5 Siemens per meter. As a result, the resistance to ground will be dramatically reduced.

4.2 Analysis of a TSV with pin-holes in a highly conductive substrate

4.2.1 Current density distribution

Figure 4.2(a) shows the current density distribution for a faulty TSV within a highly conductive substrate with $1 \,\mu\text{m}^2$ pin-hole.



Figure 4.2(a). Current density distribution for a faulty TSV within a highly conductive substrate with 1 µm² pin-hole.

It can be observed that most of the current flows from one terminal, through the pinhole, and then into the substrate in many directions. There is very limited current flowing to the other terminal after passing the pin-hole in a highly conductive substrate. This is because the substrate bulk conductivity is relatively high, which is close to the range of conductor. We may expect when the pin-hole size is large enough, there will be no connections between both terminals because in that case, the current will flow throughout the pin-hole totally. For the low conductivity case, Figure 4.2(b) shows the current density distribution for a faulty TSV within a resistive substrate with $1 \,\mu\text{m}^2$ pin-hole.



Figure 4.2(b). Current density distribution for a faulty TSV within a resistive substrate with 1 µm² pin-hole.

It can be observed that although the current density decreases after the current passed the pin-hole, there are no considerable changes in the current flow in general. There are some leakage currents after the pin-hole is created, but it is not high enough to create component changes in the equivalent circuit model.

4.2.2 Equivalent Circuit

A pin-hole of 1 μ m²on TSV within a resistive substrate reduces the resistances of TSV terminals to ground from 208M Ω to 23.6K Ω as shown in Figure. 3.3. All other components in the TSV extracted model remain unaffected.

A pin-hole with the size of $1 \,\mu\text{m}^2$ on the same TSV within a highly conductive substrate (10^5 Siemens per meter) is also created. The equivalent circuit model is shown in Figure 4.3.



Figure 4.3. TSV equivalent circuit models for a TSV within a highly conductive substrate with 1 µm² pin-hole.

We find that there are two main difference between these cases. One is that the pinhole itself reduces the resistances of the paths to ground to less than 6Ω . The other is that the pin-hole changes the components of the TSV equivalent circuit model. It can be seen that the large resistors between TSV terminals and ground, R2 and R5 in Figure. 3.3, have been replaced with relatively small resistors in series with inductors. The resistors are attributed to the low impedance path opened from TSV terminals to ground through the pin-hole and the inductors indicate that the impedances of the paths to ground increase with frequency.



Figure 4.4. Impedances for a TSV within a highly conductive substrate with a pin-hole.

We may notice that the extracted circuit model does not include any capacitor since the pin-hole punched through the insulator and connected the plates of the capacitors formed between the TSV and the substrate. In this case, contrary to the case of high resistivity substrate, the current from TSV to ground is dominated by the conduction current through the low resistive paths from TSV terminals to ground.

The displacement current through the capacitors formed between the TSV and the substrate become negligible as compared to the conduction current. Thus the capacitors is omitted from the circuit model. Variations of TSV equivalent circuit components for highly conductive substrate with different size pin-holes are shown in table 4.1.

Pin-hole						
Size (µm²)	R1(mΩ)	L1 (nH)	R2(Ω)	L2 (nH)	R3(Ω)	L3 (nH)
1	3	0.011	5.47	0.038	5.47	0.039
2	3	0.011	3.32	0.038	3.32	0.040
4	3	0.011	2.29	0.037	2.29	0.040
6	3	0.011	1.76	0.036	1.76	0.040
9	3	0.011	1.4	0.036	1.4	0.040
12	+∞	+∞	1.15	0.034	1.15	0.040

Table 4.1.Variations of TSV equivalent circuit parameters with different pin-holes for a substrate with 10⁵ Siemens per meter conductivity.

It can be seen that the impedance between the TSV terminals, R1 and L1, is constant while both the resistance and the inductance of each TSV terminal to ground experience a considerable reduction when the size of pin-hole increases.

When the pin-hole size reaches 12 μ m², R1 and L1 both become infinity, which means that under this condition there is no connection between both terminals. When the pin-hole size reaches 12 μ m², the current generated from one TSV's terminal will mainly flow into the substrate.

4.3 Analysis of a TSV with voids in a highly conductive substrate

4.3.1 Current density and electric field distribution

Figure 4.5 shows the current density and electric field distribution for a faulty TSV within a highly conductive substrate with $37 \,\mu m^3$ void.







Figure 4.5. (a) Current density distribution. (b) Electric field distribution for a faulty TSV within a highly conductive substrate with 1 µm² pin-hole.

From current density distribution, we note that some fluctuations of the current flow occur near the void, but the main flow in general is smooth, there are almost no changes

of current distribution for this case as compared to the case that TSV in a resistive substrate.

For electric field distribution, although there is a small field intensity change near the void, the field is more or less uniformly distributed. We can expect that the equivalent circuit for this case will not have a significant change.

4.3.2 Equivalent circuit

The structure and parameters of the equivalent circuit remain almost the same as compared to Figure 4.1.

4.4 Analysis of a TSV with opens in a highly conductive substrate

Figure 4.6 shows the current density distribution for a TSV within a highly conductive substrate with an open fault.



Figure 4.6. Current density distribution for a TSV within a highly conductive substrate with an open fault

We note that as compared to the open TSV in a resistive substrate, the current density of the surface is reduced to 10%, but the current density distribution remains with almost no changes.

4.5 Summary

In this chapter we studied the effects of different bulk conductivity of the substrate on the equivalent circuit models and their parameters.

We noted that for TSVs with voids or opens, the substrate's bulk conductivity does not have a significant effect on the equivalent circuits' parameters. While for TSVs with pinholes, the resistance from TSV terminals to ground reduces sharply. Moreover, the structure of the equivalent circuit is affected. The capacitors in the circuit model are replaced with inductors. This is due to the fact that the TSV body in this case is connected to a highly substrate and the plates of the capacitors are shorted. Also the resistances from TSV terminals to ground reduces sharply to less than 6Ω when a small pin-hole with the size of 1 µm by 1 µm is created on the dielectric layer. When the pinhole size exceeds 12um² the current flows mainly through the highly conductive substrate.

Chapter 5

TSV with Bumps and Layers

5.1 Fault-free TSV structure

Based on the discussions in Chapter 2, we have implemented a TSV structure shown in Figure. 2.1. This structure only includes the TSV body, the dielectric layer and the substrate, while a complete TSV includes a passivation layer, bumps on the top and bottom of the TSV, a metal layer, a keep out zone and an active layer. For an accurate analysis, we have implemented a complete TSV structure as shown in Figure 5.1. The length, width and height of the bumps are $20 \,\mu\text{m}$, $20 \,\mu\text{m}$ and $5 \,\mu\text{m}$, respectively. The thickness of the dielectric is $0.5 \,\mu\text{m}$.



Figure 5.1 Implemented TSV structure

5.2 Analysis of the complete fault-free TSV structure

5.2.1 Electric field and current density distribution

The TSV was excited with one voltage at its port to extract S-parameters. The frequency is swept from 1MHz to 1GHz, with the step size of 1MHz, and the solution frequency is set to 1GHz.

The top tin bump is assigned as terminal_1 and the bottom tin bump as terminal_2. Figure 5.2 (a) shows the electric field distribution and Figure 5.2(b) shows the current density distribution of the fault-free TSV. The electric field and the current density are uniformly distributed over the surface of the TSV and there is no current flowing into the substrate.



Figure 5.2 (a) Electric field distribution of a complete TSV structure

(b) Current density distribution of a complete TSV structure

5.2.2. Equivalent circuit and S-parameters

Figure 5.3 shows lumped circuit model representing the complete fault free TSV generated by HFSS from 3D full wave simulation at 1GHz solution frequency.



Figure. 5.3. Lumped circuit model representing a fault free TSV generated by HFSS from 3D full wave simulation at 1GHz solution frequency.

As compared to Figure 2.3, there are no significant changes, only the capacitors to ground, C1 and C2, increase from 0.0627pF to 0.079pF. The contact area of the dielectric and the conducting plates are larger, which will increase the capacitance.

Figure 5.4 shows the S-parameters of the TSV. S11 shows a minor return loss at 1GHz solution frequency and likewise, S21 indicates an insertion loss at high frequencies. These results are similar to what we got in Chapter Two.



Figure. 5.4. S-parameters of the fault-free TSV with ultimate structure.

(a) S11 and (b) S21

5.3 Analysis of the complete TSV structure with a pin-hole

5.3.1 Electric field and current density distribution

A pin-hole with the size of $2 \mu m$ by $2 \mu m$ was created on the silicon dioxide to see the electric field and current density distribution under this case. Figure 5.5(a) shows the electric field distribution and Figure 5.5(b) shows the substrate volume current intensity. The electric field intensity is higher near the pin-hole in the substrate because the dielectric separating the two conductors is broken. The current density of this fault model is also higher than the fault-free model because of the electric path from the pin-hole to ground which will result in greater leakage current.



Figure. 5.5. (a) Electric field distribution. (b) Substrate volume current intensity for a TSV with a pin-hole size of 2 µm by 2 µm

5.3.2 Equivalent circuit and S-parameters

Figure 5.6 shows lumped circuit model representing a faulty TSV with a pin-hole size of $2\mu m \times 2\mu m$ ultimate structure generated by HFSS from 3D full wave simulation at 1GHz solution frequency. As expected, most of the parameters keep no changes except the resistance to ground, say, R3 and R6, drop from 220M Ω to less than 23K Ω . This results are consistent with the results shown in chapter 3.



Figure. 5.6. Lumped circuit model representing a faulty TSV with a pin-hole size of 2 µm×2 µm.



Figure. 5.7. S-Parameters for a TSV with Pinhole of $2\,\mu m \times 2\,\mu m.$ (a) S11. (b) S21.

Figure 5.7 shows the S-parameters of the TSV with a pin-hole of $2\mu m \times 2\mu m$. As compared with Figure 5.4, both return loss and insertion loss have noteworthy changes, e.g., the maximum return loss decreases from -75dB to -55dB and the insertion loss increases from -0.04dB at 1GHz to -0.05dB at 1GHz.

5.3.3 Effect of pin-hole sizes on equivalent circuit

Table 5.1 shows the parameters of the equivalent circuit with different pin-hole sizes. If we recall the discussions in Chapter Three, the variations of parameters other than the resistance from TSV terminals to ground retain almost no changes. We have the same situation here. We note that the resistance to ground, R3 and R6, fall from 220M Ω to 55K Ω immediately after a pin-hole of 1 µm by 1 µm is created. R3 and R6 is decreasing when the pin-hole size is increasing, but the relationship is not linear. For example, when
the pin-hole size is $2\mu m \times 2\mu m$, 4 times greater than $1\mu m \times 1\mu m$, R3 and R6 fall from 55K Ω to 23K Ω , which is not 4 times smaller.

TABLE 5.1

Variations of TSV equivalent circuit parameters with different pin-holes for a substrate with 10 Siemens per meter conductivity.

Pin-hole Size										
(μm²)	R1(Ω)	R2(Ω)	R3(KΩ)	R4(Ω)	R5(Ω)	R6(KΩ)	L1 (nH)	L2 (nH)	C1 (pF)	C2(pF)
1	0.016	0.003	55	1E-5	1E-5	55	0.164	0.488	0.078	0.078
2	0.016	0.003	33	1E-5	1E-5	33	0.164	0.488	0.077	0.077
4	0.016	0.003	23	1E-5	1E-5	23	0.164	0.488	0.076	0.076
6	0.016	0.003	17	1E-5	1E-5	17	0.164	0.488	0.076	0.076
9	0.016	0.003	14	1E-5	1E-5	14	0.164	0.488	0.074	0.074
12	0.016	0.003	11	1E-5	1E-5	11	0.164	0.488	0.074	0.074
16	0.016	0.003	9.5	1E-5	1E-5	9.5	0.164	0.488	0.073	0.073
20	0.016	0.003	8.2	1E-5	1E-5	8.2	0.164	0.488	0.072	0.072
25	0.016	0.003	7.0	1E-5	1E-5	7.0	0.164	0.488	0.071	0.071

5.4 Analysis of the complete TSV structure with a void

Figure 5.8 shows TSV with a cylindrical void of 3 µm diameter and 3 µm height. The experimental results are almost the same as shown in Chapter Three, with no significant changes on the equivalent circuit's parameter, the S-parameters, the electric field distribution and the current density distribution. As a result, although a void affects the TSV's physical integrity, it does not have a noticeable effect on the electric performance of the TSV at high frequencies unless the void becomes large enough to either cut off the TSV or severely limit the current flow



Figure. 5.8. (a) TSV with a cylindrical void of 3µm diameter and 3µm height. (b) Surface current density distribution at 1GHz solution frequency.

5.5 Analysis of the complete TSV structure in a highly conductive substrate

5.5.1 Fault-free model

5.5.1.1 Equivalent circuit

Figure 5.9 shows the equivalent circuit for the complete TSV structure in a substrate with the conductivity of 10^5 Siemens per meter.



Figure. 5.9. TSV equivalent circuit models for a fault free TSV at 1GHz solution within a highly conductive substrate with $1m\Omega$.cm resistivity.

If we compare Figure 5.9 with Figure 5.3, we can see that all the parameters remain almost the same except the resistances to ground which falls from $220M\Omega$ to $5.4M\Omega$. This result is also consistent with the result in chapter 3.

5.5.1.2 S-parameters

Figure 5.10 shows the effect of substrate on TSV S-parameters. The red curve shows the S-parameters of the TSV in a resistive substrate while the blue curve shows the S-parameters of the TSV in a highly conductive substrate. We find that for the return loss, S11, there are minor changes while for the insertion loss, S21, the TSV in the highly conductive substrate has a higher loss.



Figure. 5.10. The effect of substrate's bulk conductivity on TSV Sparameters. (a) S11. (b) S21.

5.5.2 TSV with a pin-hole

Figure 5.11 shows the equivalent circuit of a TSV with a pin-hole size of $1 \mu m$? It can be seen that the small capacitors which are in series connection with small resistors are replaced by small inductors. Table 5.2 shows the variations of TSV equivalent circuit parameters with different pin-holes for a substrate with 10^5 Siemens per meter conductivity. The resistors connecting TSV terminals to ground fall as the pin-hole size increases.



Figure. 5.11. Equivalent circuit model at 1GHz solution within a highly conductive substrate with $1m\Omega$.cm resistivity for a TSV with a pin-hole of $1\mu m^2$ area.

TABLE 5.2Variations of TSV equivalent circuit parameters with different pin-holes for asubstrate with 10⁵ Siemens per meter conductivity.

Pin-hole Size		L2		L1		L3	R4(L4
(μm²)	R2(Ω)	(nH)	R1(Ω)	(nH)	R3(Ω)	(nH)	Ω)	(nH)
1	0.08	0.30	0.08	0.12	5.4	0.08	5.4	0.023
2	0.08	0.30	0.08	0.12	3.2	0.08	3.2	0.025
4	0.08	0.30	0.08	0.12	2.3	0.08	2.3	0.025
6	0.08	0.29	0.08	0.11	1.7	0.08	1.7	0.025
9	0.08	0.29	0.08	0.11	1.4	0.08	1.4	0.025

5.6 Pre-bond TSV testing

The major difference between pre-bond TSV testing and post-bond TSV testing is that we can only access one TSV terminal at the pre-bound stage while we have access to two TSV terminals in the post-bond TSV stage. Figure 5.12 shows the implemented pre-bond TSV structure, its equivalent circuit and the return loss.

For the equivalent circuit, there is a capacitor with the value of 0.07pF connecting the TSV terminal to ground. From S-parameters, it can be seen that the return loss increases with frequency to about -12dB at 1GHz frequency.

Voids in the pre-bond TSV body can barely affect the TSV's electric performance while a pin-hole sharply decreases the resistances connecting TSV terminals to ground, which is consistent with the results in Chapter Two.

It is easy to detect open faults in post-bond TSVs as there will be capacitors instead of resistors in the TSV model. While for pre-bond TSVs, it is challenging to detect this kind of fault due to limited access. The variations of capacitances is a function of the locations of opens. Figure 5.13 shows a pre-bound TSV with an open defect which is 10 µm away from the TSV port. It shows that the farther the open fault is from the TSV terminal, the more difficult it is to detect the open fault. This is due to the fact that as the distance between the open fault and the TSV terminal increases, the parasite capacitance increases.







Figure. 5.12. (a) Implemented pre-bound TSV and its (b) equivalent circuit and (c) return loss at 1GHz solution.



Figure.5.13. (a) A pre-bound TSV with an open defect 10 µm far from the TSV port. (b) Variations of the pre-bound TSV parasitic capacitance with distance of the open defect from the TSV port.

5.7 TSV Misalignment

When TSVs are not packed together exactly on top of each other the performance of the TSVs are affected due to misalignment. Figure 5.14 shows an example of TSV misalignment.



Figure. 5.14. TSV misalignment reducing the effective contact surface between the TSV ports by 75%.

The variations of capacitors to ground is shown in Table 5.3

Misalignment		
percentage	C1(fF)	C2(fF)
0%	157.5	157.5
25%	157.8	157.8
50%	158.4	158.4
75%	159.5	159.5

TABLE 5.3Variations of TSV capacitance to ground with misalignments

5.8 Summary

Instead of the simple copper bar surrounded by a dielectric layer implemented in previous chapters, this chapter studies the complete TSV structure, with interconnects, bumps, keep out zone, and metal layer added.

We performed simulations on fault free TSVs and TSVs with different types of faults, the results are consistent with the results obtained with the TSV structure in previous chapters. TSV misalignment and pre-bond testing are also studied. Misalignment does not have a significant effect on the TSV's electric performance if the overlap area exceeds 0.25%. The current find its way from one TSV to the other through the surface of the conducting metal. For pre-bond TSV testing, the effects of pin-holes and voids are similar to post-bond TSVs. It is more challenging to test the open fault of pre-bond TSVs due to the limited access to the ports.

Chapter 6

Measurement resolution to detect TSV defects

6.1 Delay test

Delay test is an essential part of circuit debugging. In [21], a solution has been presented for wire delay measurement using random samplings of signals with different periods. A method to detect TSV faults through delay measurement is also presented in [17]. In this method, the delay is determined by changing an inverter from a normal operation to a Smith Trigger. In [13], a small delay test scheme for through-silicon vias (TSVs) is presented.

Although a fault free TSV presents a high capacitance and the delay caused by a TSV is dominated by its capacitance, the rate of TSV capacitance variations due to voids and pin-holes is too small for low conductivity substrates. In a resistive substrate, the TSV capacitance value remains nearly constant even in the presence of large square pin-holes of $20 \,\mu\text{m}^2$ or sphere voids of 800 μm^3 . The total TSV capacitance does not vary noticeably with voids even in highly conductive substrates. Interestingly, pin-holes have a significant effect on the TSV capacitances and resistances on highly conductive substrates.

6.2 Elmore delay

As the inductance of the TSV can be neglected when calculating the delay [13], we can just take the resistance and the capacitance of the TSV into consideration. Elmore delay [54] formula fits perfectly into this kind of situation. Figure 6.1 shows the tree-structured RC network [55].



Figure 6.1 Tree-structured RC network

The Elmore delay from node s to node i is given in equation 6.1.

$$\tau_{Di} = 0.69 \sum_{k=1}^{N} C_k R_{ik} = 0.69 [R_1(C_1 + C_2 + C_3 + C_4 + C_i) + R_2C_2 + R_3(C_3 + C_4 + C_i) + R_4C_4 + R_iC_i]$$
(6.1)

In the same way, if we take the equivalent circuit of a TSV shown in Figure 2.3 into consideration, the Elmore delay for a TSV can be given in equation 6.2.

$$t_{delay_TSV} = 0.69(R_1 + R_4)C_2 \tag{6.2}$$

A challenge is raised here: The capacitance of a TSV is around pico-farad range and the resistance of a TSV is only a few mili-Ohm, the delay for a fault-free TSV should be very small and difficult to capture. How to expand this small delay to an acceptable range is a critical issue.

6.3 Circuit designed for delay test

A test circuit has been implemented using Agilent Advanced Design System (ADS) to estimate the required delay measurement resolution to detect a TSV pin-hole of 1 μ m² on a resistive substrate. As shown in Figure. 6.2, a step voltage of 1V has been applied to the TSV circuit model through a driver with R_{driver} and C_{driver} of 10K Ω and 10fF, respectively.



Figure 6.2. Test circuit implemented to determine the required measurement resolution for TSV parametric fault detection.

For this circuit, we expect the delay should be calculated by equation 6.3.

$$t_{delay_{TSV}} = 0.69[(R_{driver} + R_3)C_1 + (R_{driver} + R_1 + R_4)C_2] \quad (6.3)$$

Equation 6.3 can be simplified to equation 6.4

$$t_{delay_{TSV}} \approx 0.69 R_{driver} (C_1 + C_2) \quad (6.4)$$

 R_{driver} is in more than 10⁷ times greater than R_1 , R_3 and R_4 , as a result of which, we can remove R_1 , R_3 and R_4 in equation 6.3.

The variation of delay can be calculated by equation 6.5

$$\Delta t_{delay \ TSV} \approx \ 0.69 R_{driver} (\Delta C_1 + \Delta C_2) \quad (6.5)$$

Simulation results for a substrate of 10 Siemens per meter conductivity with a pin-hole of $4\mu m^2$ in Figure. 3.5 indicate that the resistances of the TSV terminals to ground, R2 and R5 in Figure. 3.3, fall to 23.6K Ω while all other component values remain unchanged. The delay difference between the responses of fault-free and faulty TSV in this case is negligible. When the output exceeds the threshold of 0.5V, the difference between the responses becomes less than 0.1ps, which is much lower than the resolution of current on-chip time measurement circuits. A relatively large pin-hole of 20 μm^2 still requires less than 1ps measurement resolution to be detected. As a result, such defects remain unnoticed even though they potentially can have significant effects on the circuit

performance. In the case of resistive substrates, pin-holes neither affect the swing nor the delay noticeably if typical drivers and receiver are used. To properly detect such TSV defects the output resistance of the driver has to be high enough to allow pin-holes to have a meaningful effect on the time constant of the output. For instance, if the output resistance of the driver, R_{driver} , changes to $10k\Omega$, the delay at the TSV output as shown in Figure. 6.2 exceeds 20ps.



Figure 6.3. Simulation results indicating measurement resolution of 20ps to detect a pin-hole of 1 µm²

The effects of pin-holes on highly conductive substrates can be detected readily as they reduce the output swing and delay significantly. In this case, a pin-hole acts like a stuckat zero fault if a driver with high output resistance is used.

6.4 Summary

In this chapter, a circuit is presented to analyze the required time measurement resolution to detect TSV faults. Simulation results in ADS environment indicate that the output resistance of the driver used to apply the test signal to TSV affects the required measurement resolution considerably. The time measurement resolution of about 20ps is needed to detect a pin-hole of $1\mu m^2$ with a driver with $10K\Omega$ output resistance. Due to the minor variations of TSV model parameter with pin-holes and voids, a test solution for TSV parametric faults needs a dedicated high resolution on-chip measurement circuit.

Chapter 7

Conclusion and Future work

Conclusion

One of the main challenges of 3D IC integration is how to test TSVs to cover their physical defects. TSV as a new structure presents some unique test challenges. Conventional test methodologies developed for interconnects can be used to cover catastrophic TSV defects including open and short faults. However, new test techniques are needed to cover TSV parametric faults.

In this work, analytical approach using transmission line to present a TSV is shown, and 3D full wave simulations using industry standard CAD tool, HFSS, have been performed to extract TSV equivalent circuit model under different conditions. The extracted models indicate that the delay of a 50 µm long TSV with 5 µm diameter is dominated by its capacitance. However, the variations of total TSV capacitance in a resistive substrate with different size pin-holes are too small for the purpose of fault detection. In this case, variations of the resistive paths from TSV terminals to ground have to be monitored to detect pin-holes. It is shown that the substrate has a significant effect on TSV fault characterization. A circuit used to detect a TSV pin-hole on low conductivity substrate cannot be easily used to detect the same fault on a highly conductive substrate. It is also shown that regardless of the substrate type, even a relatively large void does not noticeably alter the TSV model parameters with pin-holes and voids, a test solution for TSV parametric faults may need a dedicated high resolution on-chip measurement circuit.

Future Work

Although this work presents good models from CAD tools for faulty and fault free TSVs in different conductivity of the substrate, the need for fabricating TSVs cannot be neglected. We need the test results from the fabricated TSVs to support our work. Also,

we should develop an on-chip testing circuit with high-resolution and is independent from temperature, supply voltage and process to test the TSV faults.

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