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An embedded tester core for mixed-signal System-on-Chip circuits

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AN EMBEDDED TESTER CORE FOR MIXED-SIGNAL SYSTEM-ON-CHIP CIRCUITS

by

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ABSTRACT

A new methodology for testing high frequency analog/RF cores in a mixed-signal System-on-Chip (SoC) environment using an embedded tester core is presented. The proposed test method provides a solution to the problem of bandwidth limitation associated with I/O transmission paths and eliminates the need for an advanced external Automatic Test Equipment (ATE) to interact with the embedded tester. The design of the tester is based primarily on a digital level solution, except for a Track and Hold (T/H) circuit and a few CMOS switches, so as to offer the scalability advantages of a soft core description.

In the proposed test method, low frequency waveforms are generated by an external Arbitrary Waveform Generator (AWG) and then upconverted from low to high frequency through an on-chip modulator to excite fast analog circuits. The high frequency response waveforms on the other hand, are down converted from high to low frequency via subsampling techniques and then sent to an external controller for test result evaluation. In this method all high speed operations are performed onboard the chip and only low frequency signals are transmitted between the embedded tester core and the external environment.

A coupled Phase-Locked-Loop (PLL) and Delay-Locked-Loop (DLL) module is employed to generate a carrier signal in the 2.7 GHz range and to synchronize sampling operations to achieve an effective 10 ps interval between sampling points. Coherent subsampling is achieved using a track and hold circuit that is synchronized

with the embedded tester's internal voltage controlled oscillator. The circuits have been designed so that to minimize oscillator jitter and the nonlinear effects associated with the sampling circuit. Simulation studies using an RF oscillator and a Low Noise Amplifier (LNA) as circuits under test verified the measurement capabilities of the proposed tester architecture.

A prototype of the tester core with a chip area of 1 mm^2 has been fabricated in 0.18 μm CMOS process. Experimental measurements performed on the embedded tester have determined that the bandwidth of the T/H circuit is approximately 4.8 GHz. The overall coherent sub-sampling path accuracy was measured and found to have less than 5.3 % error in amplitude. The simulation and measurement results show that the proposed test methodology can successfully be employed to measure the performance of very fast analog/RF circuits via a low speed transmission path.

To the memory of my mother

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I owe a great debt to my family. I thank them most sincerely for their patience, understanding, encouragement and unfailing moral support over the long period of time spent on this research.

[1] www.nserc-crsng.gc.ca
[2] www.micronetrd.ca
[3] www.gennum.ca

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CHAPTER I

INTRODUCTION

1.1 Statement of the Problem

It is possible to design and fabricate an incredibly dense integrated circuits comprised of interconnected modules or cores. These cores can be reused in many other different systems. This type of architecture is called a System-on Chip (SoC). A typical SoC can contain various digital, analog and mixed signal cores fabricated all together on a single chip. While SoC technology presents new opportunities, it also poses some significant challenges. Testing the emerging generation of SoCs poses unique challenges and risks. According to the International Technology Roadmap for Semiconductors (ITRS), "the ability to deliver high frequency signals to external Automatic Test Equipment (ATE) without much loss and distortion becomes a monumental task in test engineering". The problem of integrated circuit testing becomes even more complicated to solve when high-speed analog circuits are involved. High-frequency analog signals are difficult to measure and challenging to route to ATE pin electronics due to the continuous nature of analog signals and their sensitivity to signal integrity degradation. Advanced ATEs with customized interface circuits and matching impedances are required to perform test on high-speed analog/RF circuits. These test requirements contribute to a substantial increase in the cost and complexity of test setup for high-speed mixed-signal devices. Given the cost curve that ATE has followed over the last decade, a machine that could test a complex SoC, if it were at all technically feasible, would carry a huge price tag on the order of 50-100 million US dollars. Even if the semiconductor industry were willing to pay such costs, few believe that any ATE machine of a presently known architecture would be able to test tomorrow's SoCs as

accurately and reliability as would be required. A fresh approach is needed to explore new solutions to the problems of mixed-signal IC testing in a SoC environment.

1.2 Proposed Test Solution

There is a general consensus that some form of on-chip measurement is needed to relieve the critical bottlenecks in testing analog/RF circuits. An on-chip ATE that is located within a microscopic distance of the Circuit-Under-Test (CUT) and has a down frequency conversion capability can perform high-speed tests without the limitations imposed by the I/O transmission paths. Moreover, in very high frequency ranges this approach can eliminate the need for matching impedances owing to negligible signal reflection at lower frequencies. However, embedding all the functions of an ATE inside a chip increases the area overhead, power consumption and complexity to a level that may not be practical. A viable solution is to embed only the high frequency analog measurement functions of an ATE inside the SoC and generate low frequency signals to communicate the measurements to an external low performance, low price external ATE or even a laptop computer. In the proposed test method, all high frequency test operations are performed inside an embedded tester core and the results are communicated at low frequencies with an external controller. To generate test stimulus waveform, an on-chip high frequency digital level signal is mixed with an off-chip low frequency analog. Using a digital carrier in this method reduces the need for analog circuits to a significant degree. The proposed test method advances the state-of-the-art by providing an almost entirely digital solution for the problem of RF/Analog circuit testing (except for T/H circuit and a few switches). Using an all digital PLL and DLL to implement the test method, an RF/analog tester can be offered as a synthesizable RTL code that is scalable and not technology dependent. The need to transmit lower frequency signals over the I/O transmission paths is realized using a coherent sub-sampling technique. The proposed embedded tester core

offers a solution for embedded SoC testing that provides several major advantages as follows:

1. **Provides a solution to generating very high frequency stimulus signals for testing purposes**

   The use of a squarewave carrier that can be modulated by an external waveform offers the ability to generate very high order harmonics that can be used as a test stimulus for the mixed-signal circuits under test. The high frequency test signals generated in this manner have the same stability and controllability as the modulated carrier itself.

2. **Provides a solution to the problem of bandwidth limitation of SoC I/O paths**

   An embedded tester can be located very close to the internal cores that comprise the SoC implementation. The bandwidth limitations of the connectivity between the embedded tester core and the CUT are relatively minor. However, the bandwidth limitations associated with the I/O transmission path to an external device are significant. The physical length of the transmission path and the physical nature of the I/O pads impose severe limitations on attempts to measure very high speed internal core performance. In the proposed tester architecture coherent sub-sampling is used to measure very high frequencies and communicate the values at low frequencies. Therefore, the embedded tester core can transmit test results without the speed limitations normally imposed by the overall transmission paths.

3. **Soft Core Advantages**

   The architecture of the embedded tester employs an all digital realization wherever possible. This allows for the major part of the tester circuitry to be described in terms of a soft core. This in turn allows the design to be more readily

scalable and migrated to other process technologies. Only the track and hold circuit and a few switches have an analog realization.

4. **Reduces the Cost and the Complexity of Testing**

   The embedded tester core employs coherent sub-sampling to generate and transmit low frequency test result signals externally from the SoC. The lower frequency range simplifies the requirements of the ATE, the fixture and the transmission lines used to connect the SoC to the ATE. This can significantly reduce the cost and complexity of test procedure.

1.3 Outline of the Thesis

The rest of this dissertation is organized as follows. Chapter 2 introduces the basic concepts of mixed signal device testing, starting with a short overview of digital circuit testing followed by descriptions of the test methods developed in the context of analog/RF device testing over the years. The most recent studies in this field and the latest mixed signal ATE architecture employed by semiconductor industry are also covered in this chapter. Chapter 3 begins with the description of the proposed test method for fast RF/Analog circuits. Mathematical foundations of the employed enabling techniques, system level representation of the proposed test scheme and the architecture of the embedded tester are also presented in this chapter. Chapter 4 discusses topology selections and high level simulations of the building blocks of the tester. Schematic and layout level implementation of the analog and digital circuits are described in chapter 5. This chapter also includes the results of simulations performed on various modules of the tester. Chapter 6 presents simulation results for two test cases in which an RF oscillator and a Low Noise Amplifier (LNA) are used as CUTs. The experimental results are presented in chapter 7 and finally, in chapter 8 conclusions are drawn and recommendations are made for future work in this field.

CHAPTER II

DESIGN FOR TEST METHODOLOGIES

In general, testing a mixed signal chip is performed in two different domains of digital and analog electronics with different methods of testing. The interactions between analog and digital circuits are also tested in a separate phase. Digital circuit testing has been under intense research for a long time resulting in accurate fault models and powerful automatic test generation methods [6, 7, 8, 9]. While digital circuit testing is a mature subject, design for test methodologies for analog circuits [10] is still in its early stages and fundamental research is needed to address numerous challenges in this area. In this chapter first IEEE 1149.1 standard [11] for digital circuit testing is briefly discussed and then various test methods developed for analog circuits are covered and finally the state of the art in this field is presented.

2.1 Digital Circuit Testing

Generally, any circuit or methodology used to utilize the process of testing a product is called Design For Test (DFT). DFT, if properly implemented, has the potential to offer higher product quality at lower production cost. The DFT methods in the digital domain has reached to a satisfactory level and now it is considered as an inseparable part of digital IC design. IEEE 1149.1 standard boundary scan, also called JTAG, is among the most successful DFT methods developed for digital circuits.

2.1.1 IEEE 1149.1 Standard Boundary Scan

Boundary scan has been successfully incorporated into digital designs and has considerably simplified the test or even diagnosis of advanced electronic devices. The IEEE 1149.1 standard can be divided into two parts: 1149.1a, or the digital boundary scan

standard [12], and 1149.1b, or the Boundary Scan Description Language (BSDL). The IEEE 1149.1a standard defines the chip level test architecture for digital circuits, and 1149.1b defines the boundary scan description language.

2.1.2 IEEE P1500 Standard for Embedded Core Test

There is a close relationship between the structure of IEEE P1500 [13, 14] and the standard for boundary scan (IEEE 1149.1). IEEE 1149.1 architecture has been developed to facilitate board-level interconnect testing through chip-level wrappers. The same idea has been utilized to design a wrapper based test structure at the chip level for SoC devices containing embedded cores. Although the basic idea beyond these two methods is the same, they have important differences due to the significant flexibility required for embedded core testing. The wrapper in P1500 standard is used as a shell around a core under test. It allows the core to be isolated from its environment and tested independently. Figure 1 gives an overview of the main elements of the P1500 wrapper architecture. The wrapper in P1500 has three main types of modes:

1. Functional Operation

   In this mode the wrapper is transparent and operates as if it does not exist.

2. Inward-facing

   The test access to the embedded core is provided in this mode.

3. Outward-facing

   This mode provides test access to the circuitry outside the core.

As shown in Figure 1a, the P1500 wrapper has functional input and output ports. It also includes a Wrapper Interface Port (WIP) and an internal Wrapper Instruction Register (WIR) to control the test process. The operation of the wrapper is controlled by both the WIP signal and the instruction loaded into the WIR.

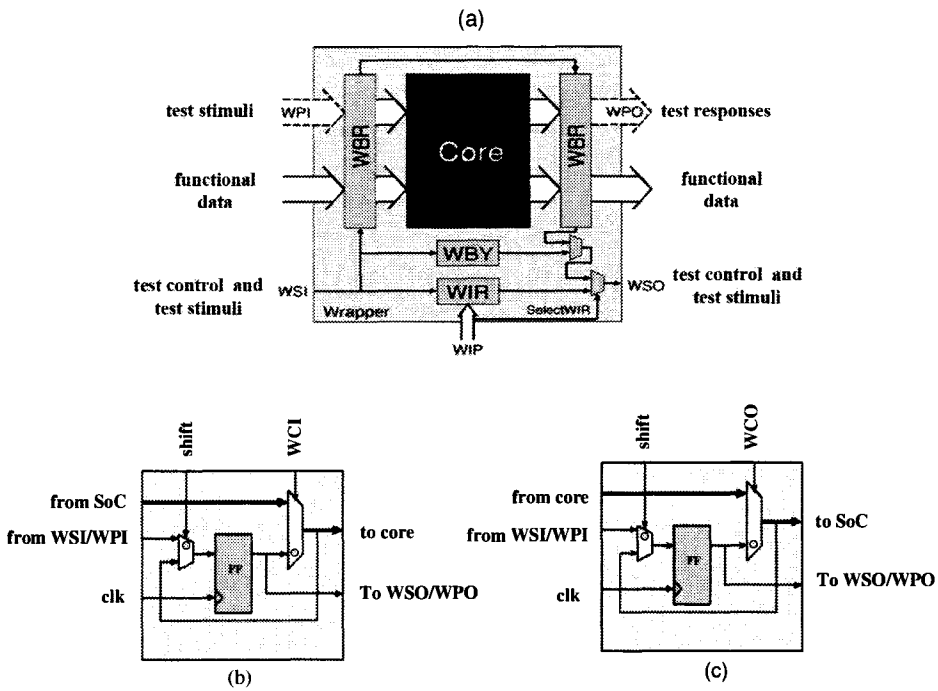

Figure 1: IEEE P1500 (a) wrapper architecture. (b) wrapper boundary input cell. (c) wrapper boundary output cell.

2.2 Analog Circuit Testing

Testing analog circuits is proven to be more challenging as compared to digital circuit testing due to the continues nature of analog signals and their sensitivity to signal degradation. Although just a small portion of most of the modern ICs is analog, the cost of analog circuit testing exceeds the cost of digital circuit testing in mixed signal environments due to the complexity of analog test generation and required equipment for test execution [15]. In a typical test scenario, a stimulus waveform is applied to the CUT and then the CUT's response is captured to evaluate the test result either in the time or frequency domain. Basic analog testers evaluate the test results in the time domain while advanced ATEs employ Fast Fourier Transform (FFT) as an effective tool for test-result analysis in the frequency domain.

1. Traditional Analog Tester

A basic test setup in the time domain as shown in Figure 2 involves applying a stimulus input to the analog circuit under test to excite the CUT with a dc, sinusoidal, squarewave, or some random signals and to measure the response with a power meter [10].

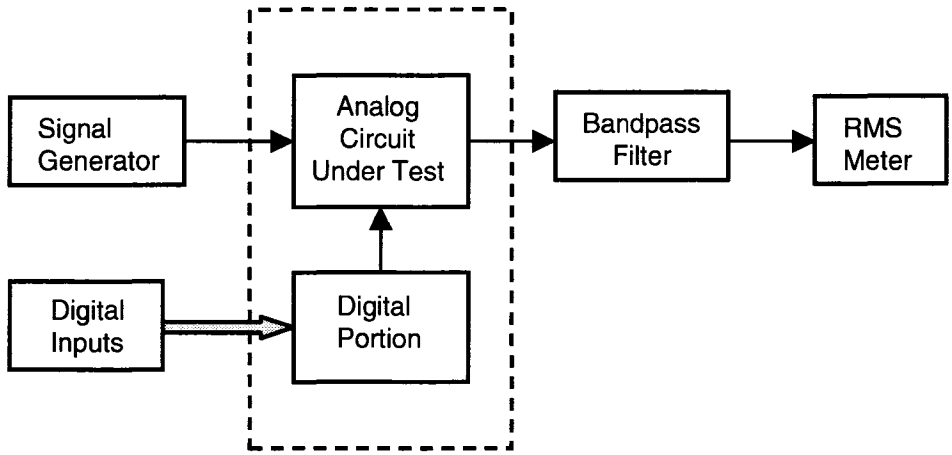

Figure 2: Traditional test setup for mixed-signal devices.

The traditional method of testing suffers from many factors limiting the application of such an approach. First, all defects in this method are assumed to have a detectable effect on the rms value at the output which in a general case of testing is not a valid assumption leading to a considerable number of undetected faults. Moreover, complete testing of some analog circuit specifications can take a significant amount of time. Consider, for example, measuring the integral nonlinearity of an ADC [16]. For a 12-bit ADC, this would require locating 4096 input voltages. Such a large number of tests can limit throughput during the device production phase and can significantly add to the cost of production.

2. Digital Signal Processing (DSP) Based Analog Tester

DSP based testing of analog circuits [17] has been widely employed by ATE industry due to the flexibility and test reliability that this method provides. DSP is a powerful methodology that allows faster, more reliable and more accurate analog testing as compared to the traditional rms measurement method. A typical DSP based test setup for analog circuits as shown in Figure 3, involves applying analog stimulus to the CUT and sampling the output waveform to evaluate the response. The advantages of DSP based testing over traditional

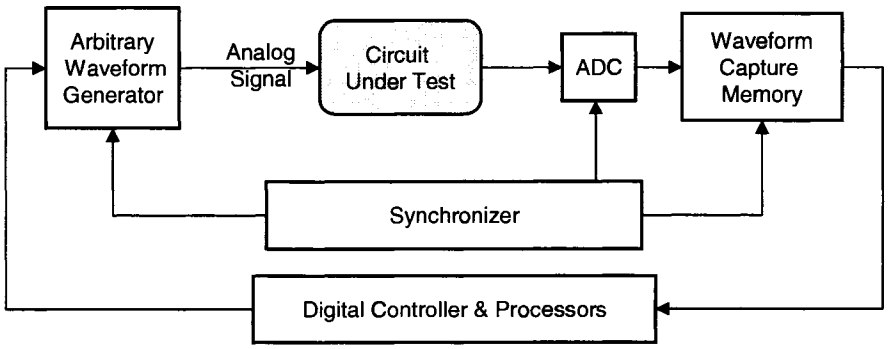

Figure 3: DSP based analog tester scheme.

measurement techniques are summarized as follow:

- Reduced Test Time

  In this method several sinusoidal waveforms with different frequencies and amplitudes can be added together to generate a multiple tone stimulus waveform. When the CUT response to such a stimulus waveform is captured, the responses to the different components of the applied multi-tone waveform are simultaneously determined. For example to test a filter, a multi-tone waveform can be applied and a serious of magnitude and phase responses can be measured at several frequencies at the same time. This capability eliminates the need for separate tests at different frequencies and significantly reduces the time required to carry out a complete test on

a typical CUT.

- Spectrum Analysis

  The FFT analysis in the DSP based measurement provides a spectrum of the sampled signal, indicating the strength of each component in the frequency domain. This capability is a major advantage over non-DSP test methods. Using FFT analysis, the noise and distortion components can easily be separated from the CUT response to the fundamental component enabling an accurate and repeatable measurement.

- Advanced Signal Processing

  Since in this method the test results are evaluated in the digital domain, various DSP methods can be employed to improve the results. For example, the output resolution can be enhanced by interpolation between the samples or zero padding.

2.2.1 Analog DFT Methods

There are many types of mixed signal DFT techniques, some of them are summarized as follows:

1. Mixed signal boundary scan (IEEE Standard 1149.4)

   IEEE 1149.4 is regarded as a mixed signal counterpart of the 1149.1 boundary scan for digital circuits. The 1149.4 standard [18] specifies the same signal pins that are associated with the 1149.1 standard. It is compliant with the digital Test Access Port (TAP) and boundary architecture. The main difference is that the 1149.4 includes new pins and analog switches to support analog signals. Figure 4 shows the 1141.4 architecture in which Digital-Boundary Modules (DBMs) are the boundary-scan cells defined in 1149.1 and Analog Boundary Modules (ABM) are the cells introduced in 1149.4 for mixed-signal devices. The IEEE

1141.4 standard employs two Analog-Test (AT) pins one to apply test signals and the other to route the response waveforms to the measurement equipment. The external analog-test bus, which connects to AT1 and AT2, accesses the internal bus under the control of the Test Bus Interface Circuit TBIC. The TBIC allows the internal test-bus lines to connect to either or both AT pins, isolates the internal test bus when it is not in use to eliminate unwanted noise interference, or connects the bus to one of two dc voltages (VH and VL). Interconnects between ICs can be tested by applying either V_H or V_L through an AT pin in one side and check the status of the signal at the other side.

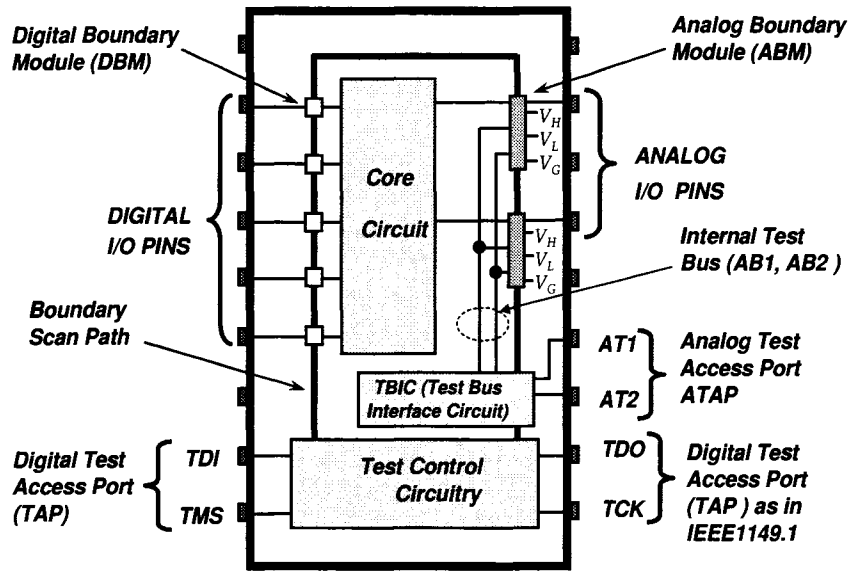

Figure 4: Mixed signal boundary scan architecture.

The 1149.4 standard primary target is to perform a simple chip-to-chip interconnect testing similar to that used in traditional digital boundary scan. however, it can also be utilized to perform internal analog circuit testing [19]. Figure 5 shows the details of an ABM module which provides access to analog input and output signals via external pins.

2. Ad-Hoc Mixed-Signal DFT

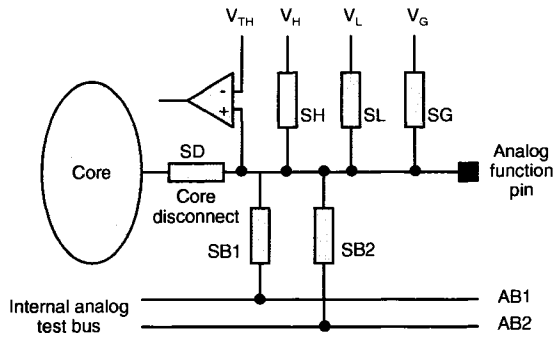

Figure 5: Analog boundary module in the 1149.4 standard.

Other than IEEE 1149.4 and IEEE P1500 standard there are a few generally accepted methods in the area of mixed-signal testing. Most of the mixed signal DFT methods are based on ad-hoc techniques that are developed for particular applications. Many companies deploy their own application-specific ways to improve testability, such as adding special function modes, increasing the number of output and input pins, and providing internal loops.

For a large analog circuit, applying the test signal to an input pin and capturing the response from the output provides a limited observability. Therefore, it is desirable to divide the CUT into several parts and add some test pins between them so that each part of the circuit can be tested separately. One of the popular methods to provide access to the internal nodes of a CUT is through analog test buses (Figure 6). This method can increase the testability and the observability of integrated circuits significantly. However, it suffers from several drawbacks. First, the switches are commonly implemented using complementary CMOS P and N transistors that introduce a parasitic capacitance in parallel with the switch. The parasitic capacitances provide an AC path between the analog nodes in the CUT that may cause instability and oscillation. Moreover, the crosstalk and clock feed through [20] between the observed nodes may become a serious problem undermining the accuracy of the measurement.

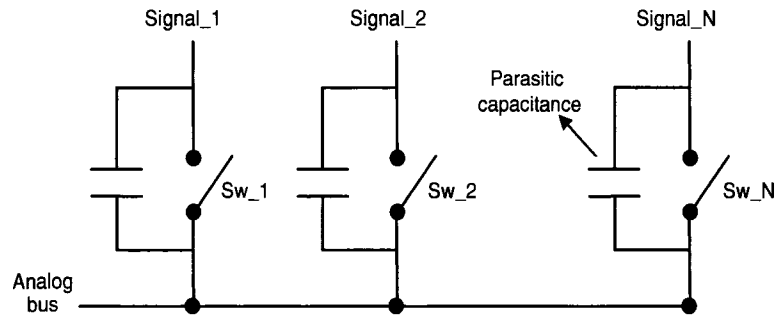

Figure 6: A typical analog test bus.

3. Mixed-Signal Built-in-Self Test (BIST)

   BIST is the most promising approach to improving mixed-signal DFT. One of the main advantages of BIST method is the protection of analog signals against distortion. BIST techniques employ on-chip signal generators and analysis circuitry, which results in less distortion and greater measurement accuracy. If BIST is fully implemented, the only signal that needs to be routed off chip is a pass/fail bit indicating the test results. The main problem faced by BIST is the fact that the BIST circuitry is exposed to the same process and temperature variations as the CUT. Therefore, it is critical for any BIST scheme to support self test and calibration. To reduce the BIST area overhead, existing on-chip hardware can be used. On-chip DACs and ADCs can effectively be employed to build a BIST structure for low speed mixed-signal devices.

   A typical on-chip test architecture for a mixed-signal circuit is shown in Figure 7. Digital input data for the DAC can be provided by a linear feedback shift register (LFSR) or a Read Only Memory (ROM) and a built-in logic block observers (BILBO) [7] can be utilized to capture the ADC output. The data stored in the BILBO registers can be compared against a known response stored in a on-chip memory or it can be analyzed using a Multiple Input Signature Register

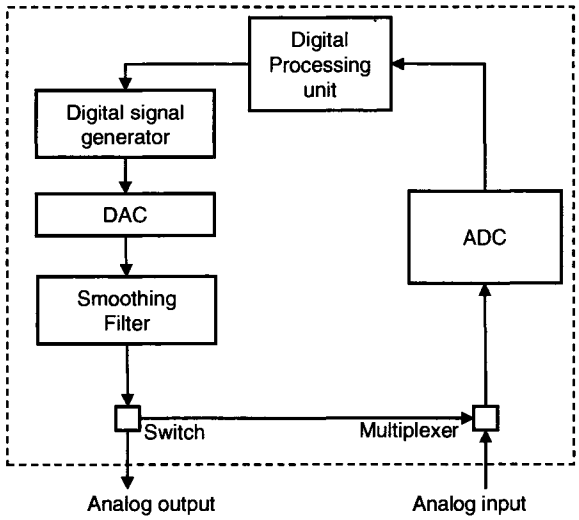

Figure 7: Mixed-signal BIST architecture using on-chip ADC and DAC modules.

(MISR). In [21], a BIST scheme is introduced to detect faults based on the auto-correlation and cross-correlation of the impulse responses for a pseudorandom piecewise-constant input signal. In [22], a BIST circuit is proposed to observe changes in the power supply current as an indicator for detecting faults. The main idea behind this approach is that faults will either increase or decrease the power supply current compared to the fault-free circuit. In [23] a BIST circuit has been designed to test DACs. The samples of the response waveforms in this scheme are captured with a sample-and-hold circuit to measure offset, gain, integral linearity, and differential linearity of DACs. A modified version of this circuit has also been proposed for testing successive approximation ADCs.

In [24, 25] a vectorless BIST technique called Oscillation Built in Self Test (OBIST) is proposed. In this method the CUT is converted to an oscillator. Then the oscillation frequency and the amplitude of the output are used as indicators for test result evaluation. The deviation of the oscillation frequency and the output amplitude from their nominal values indicate a faulty circuit. Most of the test methods developed for analog circuits are based on functional tests

while the OBIST can be implemented for structural tests. This is a significant advantage over the other methods since it opens the way for development of CAD tools for analog circuit testing. The oscillation-test method can provide a test solution to low frequency analog and mixed-signal circuits such as active filters and operational amplifiers [26, 27]. The only complication is how to add analog switches to establish feedback paths and meanwhile reduce the effect of test circuitry on normal CUT operation. Achieving this goal at the RF frequency range poses a formidable challenge where the loading effect of switches can undermine the performance of the CUT.

Due to various problems such as impact on performance, area overhead or implementation difficulties most of the analog BIST methods have not been used in industry. For an analog BIST to be successful at least to main condition should be satisfied: First, it must be accurate in the presence of normal noise and process variation to achieve test repeatability, and second it has to be easily implemented and if possible offered as a digitally synthesizable module.

4. Separation of Analog and Digital Circuits

   The separation of analog and digital circuits provides better control over analog circuits. Scan cells known as scan collars can be employed to break a mixed-signal circuit to analog and digital parts. Once the circuit is broken into digital and analog parts, digital circuits can be tested using the efficient CAD based test methods developed for digital circuits. The analog portion can be analyzed separately and proper test method can be developed accordingly. This divide and conquer methodology is particularly useful when a small analog circuit is integrated with a large digital circuit on a chip.

2.2.2 State of the Art

Some of the analog test methods developed over the years to lower the burden of analog circuit testing in mixed-signal environment were presented in the previous section. In this section the state of the art research works in the area of on-chip analog/RF circuit testing and their advantages and limitations are presented.

In [28] a test method for high frequency analog circuit is presented. The test scheme as indicated in Figure 8 employs two on-chip mixers. The first mixer is used to

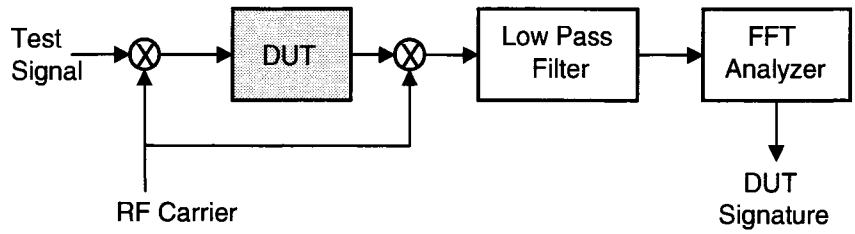

Figure 8: Signature test configuration for RF circuits [28].

up convert a low frequency test waveform to a high frequency test stimulus signal. The second mixer is employed to down convert the CUT response from high to low frequency. The demodulated signal is used to evaluate the performance metric of the CUT. This method has potential to enable a low performance external tester to carry out test on high speed embedded circuits. The main disadvantage of this method is that it does not take into account the nonlinearity effects of the on-chip mixers. Moreover since the mixers are exposed to the same process variation as the embedded circuits, the scheme can not provide reliable measurement results without calibration.

In [29, 30, 31] a compact DSP tester has been developed for analog circuit testing. It is a general purpose mini-ATE with an on-chip arbitrary waveform generator an a compact ADC for result evaluation. The functional diagram and detail view of this tester is shown in Figure 9. The tester retains all the advantages of the DSP-based

test method moreover it provides an easy implementation solution. The proposed test scheme has been almost entirely implemented in digital domain using standard CMOS gates expect for an op-amp and a basic low pass filter. Although this tester

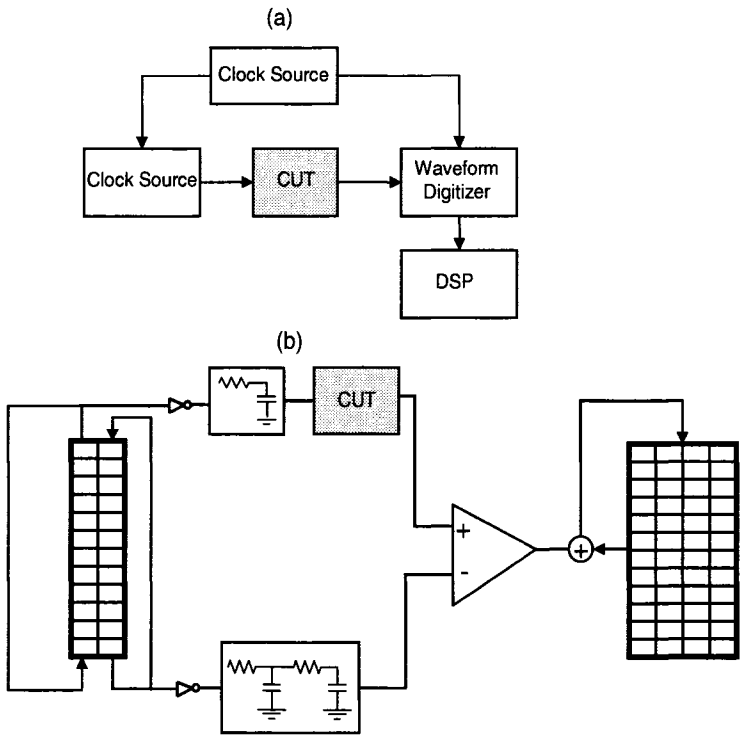

Figure 9: (a) Functional diagram and (b) detailed view of the proposed on-chip test system in [29]

can be employed to perform test on numerous analog circuits, it can not be used for high frequency analog/RF cores due to the frequency limits of the employed signal generator .

In [32] a modular test approach for mixed signal SoCs has been proposed. A unified test access architecture has been developed for both digital and analog cores. Each analog core in this method is wrapped by a pair of digital-to-analog converter and analog-to-digital data converters as shown in Figure 10. The proposed method provides a solution for low speed analog circuits in mixed signal environments. However, due to a limited speed of the employed ADC and DAC converters, this method also

cannot be utilized for high speed analog circuits testing.

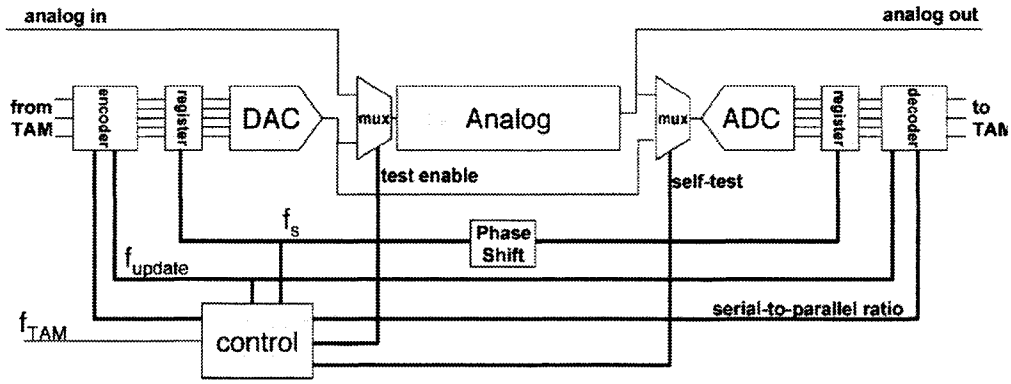

Figure 10: Block diagram of the test wrapper proposed in [32] for mixed-signal SOCs testing.

Leading companies in the ATE industry such as Advantest [33] and Teradyne [34] have also intensified efforts to provide a test solution for the next generation of mixed signal devices. The ATE industry is moving toward an open architecture automatic test equipment to integrate software and instruments of different vendors into ATEs. The use of modules in this framework is based on plug-and-play to achieve the optimal test configuration. Each modular unit can be removed, replaced with another unit from a different vendor, or reconfigured to map the test resources according to the requirements of device-under-test (DUT). Open architecture tester eliminates fixed configuration and provides a considerable flexibility to meet various chip test requirements resulting in an optimized and cost effective ATE. Figure 11 shows a typical open architecture ATE.

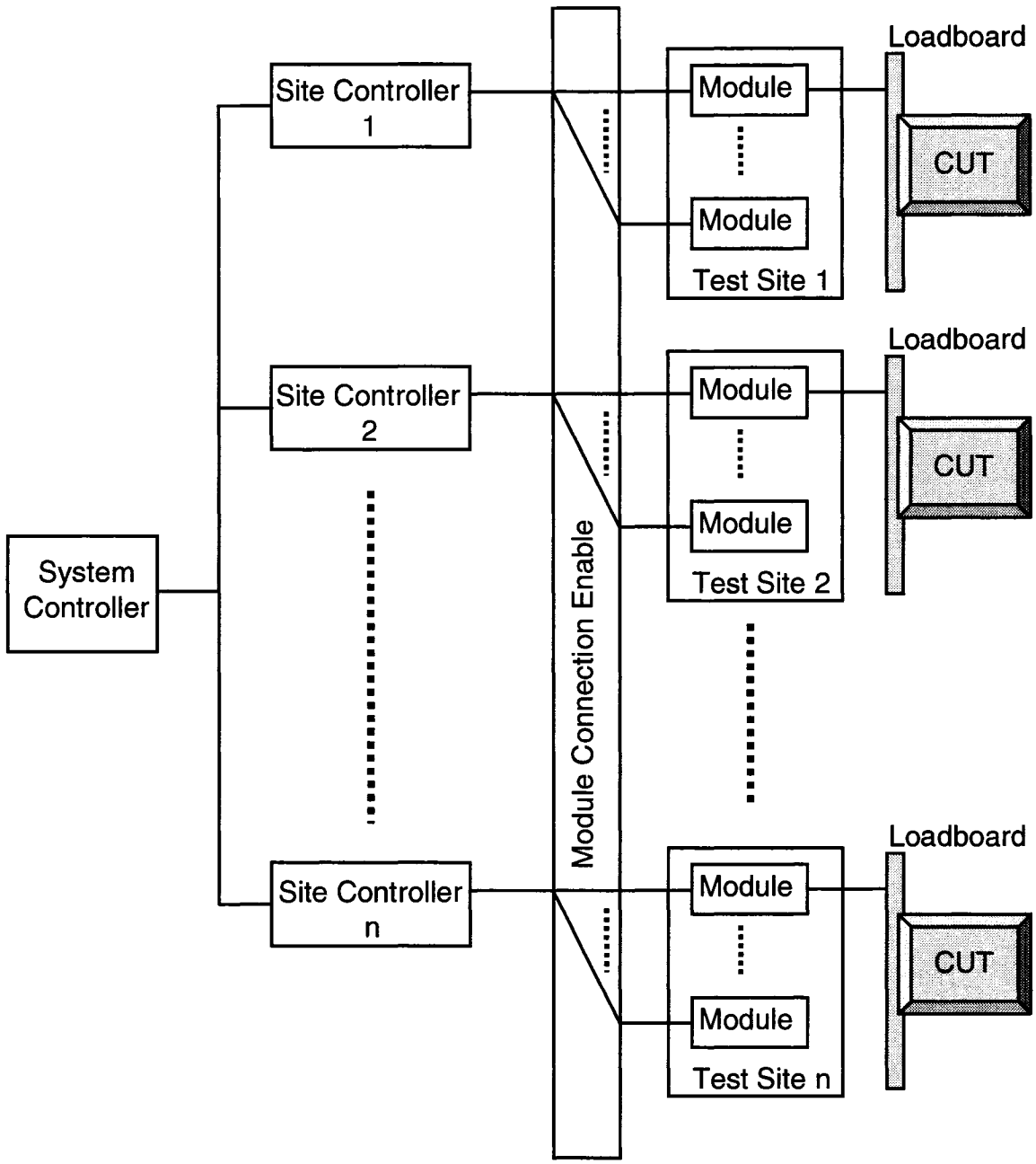

Figure 11: Block diagram of an open architecture ATE.

2.3 Summary

This chapter presented introductory material that relates to DFT for mixed signal devices. IEEE 1149.1 and P1500 standards which are the most successful DFT methods in the field of digital and analog circuits were briefly covered. Dominant test techniques developed over years to address the problem of analog circuit testing were introduced. The last part of the chapter focused on the state of the art in the field of Analog/RF circuit testing in both academia and industry.

CHAPTER III

PROPOSED TEST METHOD

Previous research works in the area of mixed-signal IC design have considered the integration of some test functionality to lower the burden of analog circuit testing; however they have been mainly aimed at providing test solutions for low frequency mixed-signal ICs [35]- [38] or developing customized test methods [39]- [47] for specific high-speed analog/RF circuits or applications. In this work a new test methodology based on an on-chip tester for high speed analog/RF circuits is presented. The proposed test method utilizes DSP techniques due to significant advantages of DSP based test methods over traditional approaches. To test fast analog/RF circuits, high-speed stimulus waveforms are required to excite the CUTs. Response waveforms are also needed to be captured at high speed to prevent the loss of information. These requirements can not be met by generic DSP based test scheme in which the stimulus generation and response measurement can hardly exceed maximum frequency of a few tens of MHz due to the speed limitation of DAC and ADC converters.

In the proposed test solution, modulation and subsampling methods have been employed as enabling techniques to overcome the limitations of the DSP based test approach. In this method a low frequency stimulus waveform is generated by an external Arbitrary Waveform Generator (AWG). This waveform is then mixed with a high frequency on-chip signal and upconverted from low to high frequency. The resultant waveform is used as a high-speed test stimulus signal to excite a CUT. On the other hands, the high frequency response of the CUT is down converted from high to low frequency through subsampling techniques. This test method eliminates the need for high speed interactions between the CUT and the external environment

since all high speed tests are carried out inside the chip.

It is highly desirable to implement on-chip testers in the digital domain due to various reasons such as scalability, ease of implementation, and lower noise sensitivity. Therefore, to design an embedded tester for analog/RF circuits, it is essential to choose proper modulation method among numerous modulation techniques to reduce the complexity of the tester and minimize the number of analog circuits. In this chapter first the enabling techniques are described and then a system level simulation in Matlab/Simulink is performed to validate the proposed test method and in the end the conceptual block diagram of the tester is presented.

3.1 Modulation Based Test Stimuli Generation

The stimulus waveform in the DSP test method is generated by an Arbitrary Waveform Generator (AWG). The basic idea behind AWG is to digitally store the samples of the desired signal in a memory and convert them to an analog signal through a digital to analog converter. Figure 12 shows a typical AWG in which a waveform memory is employed to provide data for a DAC. This method of test waveform gen-

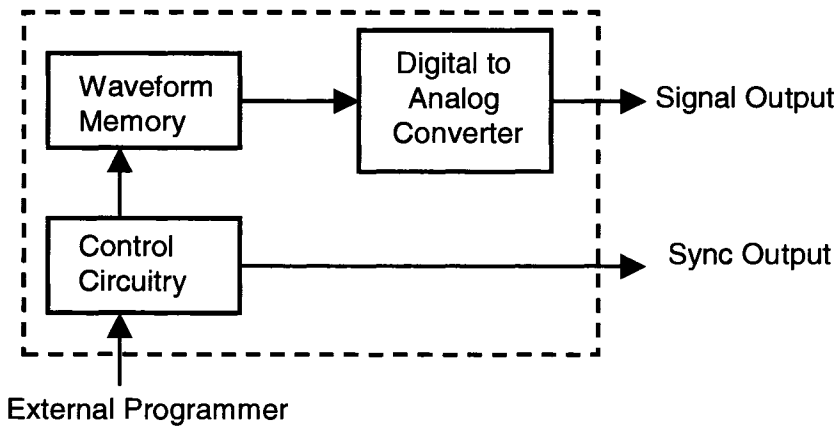

Figure 12: Block diagram of a typical programmable AWG.

eration offers several advantages such as a very low phase noise and direct mixing of signals in digital domain. Moreover, since the waveform is digitally stored in a memory it can readily be modified to generate any desired waveform without the limitations imposed by hardware in basic waveform generators. However, the maximum frequency of the signal supplied by a generic AWG is limited by the speed of the employed DAC.

Modulation techniques can be utilized to overcome that barrier. There are numerous methods of modulation developed over years for different applications, however for the purpose of fast analog circuit testing, a balanced modulator based on a bipolar chopper modulator (Figure 13) offers attractive properties that can be summarized as: (a) It can be implemented using a simple passive mixer which presents a higher linearity compared to active mixers. (b) Its carrier signal is a squarewave that can be generated and controlled by digital circuits. The Fourier series expansion representing

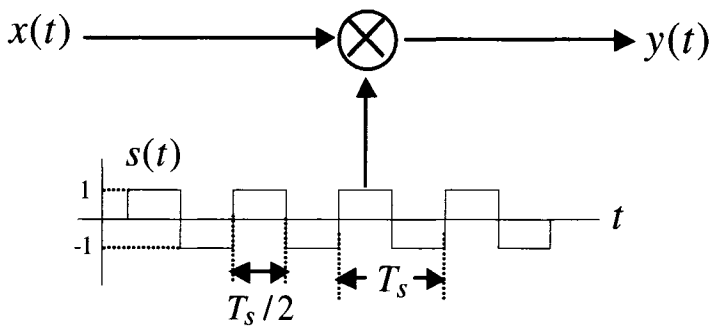

Figure 13: Bipolar chopper modulator.

the output waveform $y(t)$ of a bipolar chopper modulator is given by:

$$y(t) = \frac{4}{\pi}x(t)cosw_st - \frac{4}{3\pi}x(t)cos3w_st + \frac{4}{5\pi}x(t)cos5w_st - ... \quad (1)$$

Where $x(t)$ is a modulating signal and ω_s is the circular frequency of the carrier. If $x(t)$ is sinusoidal, the spectrum of $y(t)$ will have two tones that are repeated at odd harmonics of the carrier signal enabling the tester to perform two-tone tests and

measure intermodulation distortion of RF components. The use of a square wave carrier instead of a sine waveform introduces higher frequency harmonics, adding to the computational complexity of the response measurement. However, as outlined below, using a digital level squarewave carrier offers a number of advantages that justify its use for on-chip high-speed stimuli generation.

1. Wide tuning range

   For a sinusoidal oscillator, once the design is completed, the test frequency range is fixed by the oscillator's tuning range and cannot be easily expanded. However, with a squarewave digital level oscillator, the range can simply be expanded by adding a divide by N counter to the output of the oscillator and using the counter's output as a new lower frequency carrier.

2. Lower sensitivity

   Digital level signals are generally more immune to noise and distortion than analog signals.

3. Lower nonlinearity effect of the mixer

   A passive CMOS mixer driven by a squarewave instead of a sinusoidal signal exhibits less nonlinearity due to a relatively high overdrive voltage [49].

3.2 Sampling Techniques

To perform DSP based measurement, samples of the desired waveform have to be obtained via sampling techniques [50]. In a general case of DSP based measurement, samples of the desired waveforms are captured through a sampler and converted to digital data via an ADC. The outputs of the ADC are stored in a memory and supplied to an FFT analyzer as a set of data representing the captured waveform. Finally, the spectrum of the captured signal is determined by FFT techniques from the test result evaluation. However, FFT analysis can produce misleading results if it is not

implemented properly.

The FFT method essentially assumes that each given set of samples represent a periodic signal. This periodicity assumption introduces error if the given set of samples does not contain an integer number of cycles of the sampled waveform. Figure 14 shows a non-coherent [17] set of samples of a sinusoidal waveform used for an FFT calculation and the actual waveform represented by the computed FFT. It can be

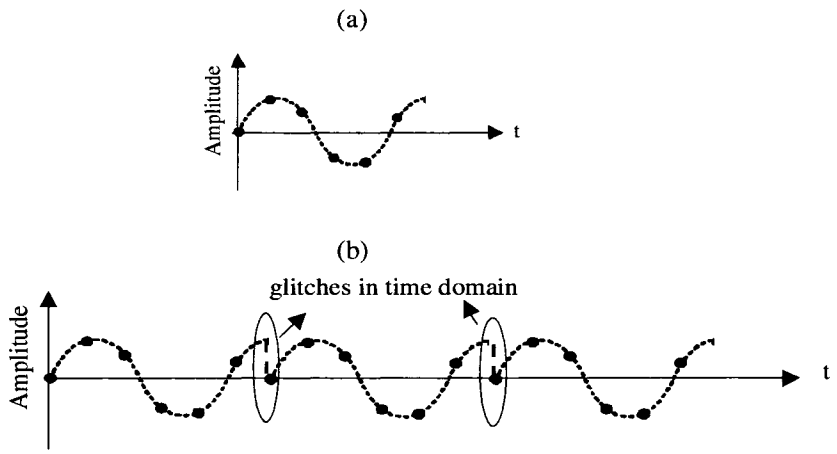

Figure 14: (a) Non coherent samples of a sinusoidal waveform used for FFT calculation. (b) the waveform represented by the FFT spectrum.

observed that the periodicity assumption translates into glitches in the time domain. As a result, the spectrum obtained by the FFT shows frequency leakage distortion. To deal with this problem various windowing techniques (e.g. Kaiser, Hamming, Han, etc.) have been developed. However, none of them can entirely eliminate the effect of the frequency leakage.

3.2.1 Coherent Sampling

In a general case of sampling, spectral leakage is unavoidable. However, if the period of the desired signal is known, then by obtaining a proper set of samples the frequency leakage can be avoided.

For the purpose of testing where the tester has full control over the signals and

samples frequency leakage can be avoided by coherent sampling which is widely used by ATE industry for FFT calculation. The following equation has to be satisfied to successfully obtain a coherent set of samples.

$$F_s/N = F_t/M \tag{2}$$

Where F_s, F_t, N and M represent sampling clock frequency, test signal frequency, total number of samples taken and total number of cycles respectively. Figure 15 shows a coherent set of samples used for the FFT calculation and the associated periodic waveform represented by the computed FFT. Coherent sampling not only eliminates

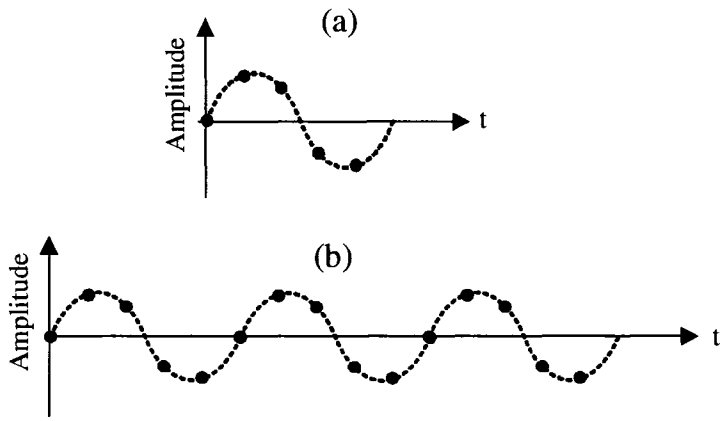

Figure 15: (a) Coherent samples of a sinusoidal waveform used for FFT calculation. (b) the waveform represented by the FFT spectrum.

the frequency leakage problem but leads to faster test time and less computation. The only complication is that a timing synchronization between the test signal and the sampling clock is required. In the proposed embedded tester scheme in this work, the AWG and the sampling clock generator have been synchronized through a coupled DLL and PLL structure to satisfy the coherent sampling requirement.

3.2.2 Subsampling Method

The basic DSP test setup can not properly test high speed devices even if the problem of high speed test stimulus generation by the AWG is solved. In order to successfully

convert high-speed analog waveforms into digital data, a fast ADC is required. However, due to the limited speed of ADC devices a direct conversion method can hardly be applied to digitize signals running faster than a few tens of MHz. The subsampling method is proven to be an efficient technique to enable low speed ADCs to digitize high speed waveforms. To illustrate the technique, consider a periodic signal $x(t)$ with frequency equal to f_s that is sampled with frequency $f_s + \Delta f$ where Δf is a small increment. As indicated in Figure 16, the sampling points walk along the waveform

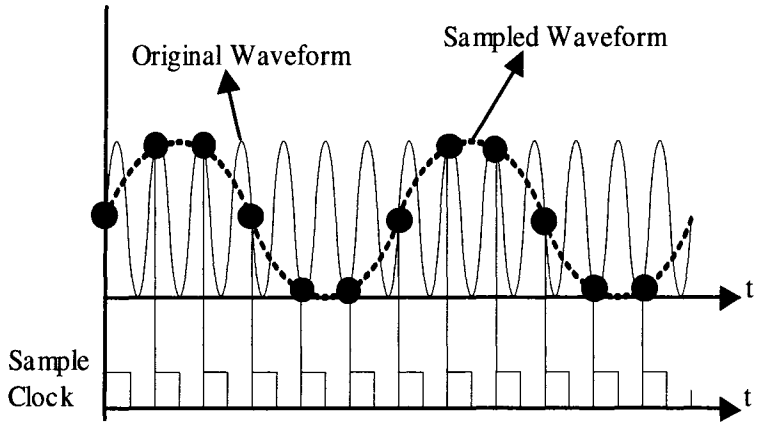

Figure 16: Subsampling a periodic waveform.

$x(t)$ at a rate equal to Δf capturing an expanded version of the original waveform. The sampled waveform $y(t)$ is expressed as $y(t) = x(\alpha t)$ where $\alpha = \frac{\Delta f}{f_x}$. Thus, a low-speed ADC can be employed to digitize the expanded waveform. The original high-speed signal can later be reconstructed from the samples of the expanded waveform by digital signal processing methods. To illustrate the operation of subsampling technique in frequency domain, consider a typical periodic waveform characterized by a discrete spectrum in frequency domain, ideally sampled by a train of impulses; the result can be expressed as:

$$y_1(t) = x(t) \sum_{i=-\infty}^{+\infty} \delta(t - KT_s) \tag{3}$$

Where T_S is the sampling period and $\delta()$ represents the delta function. The corresponding spectrum is represented by:

$$Y_1(f) = f_s \sum_{i=-\infty}^{+\infty} X(f - Kf_s) \tag{4}$$

As a result the fundamental appears at the beat frequency $f_y = f_s - f_x = \Delta f$ and compressed images of the spectrum centered at Kf_s are created as indicated in Figure 17. To reconstruct the high frequency signal, a low pass filter can be used to separate

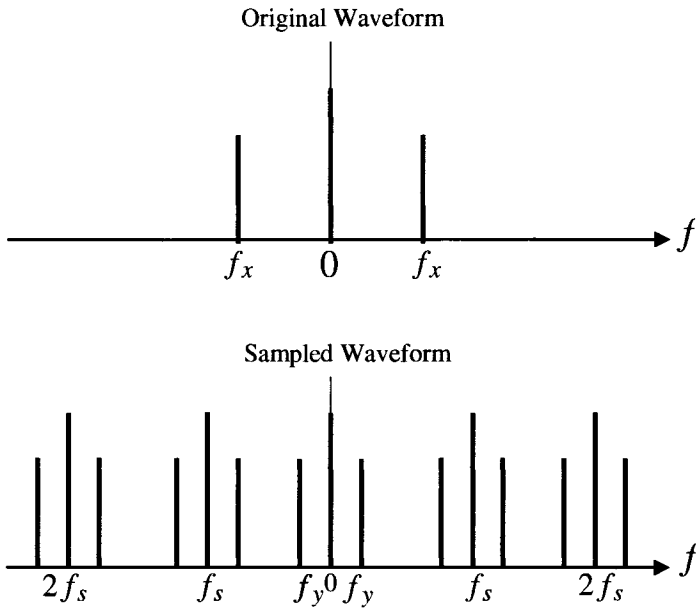

Figure 17: Subsampling spectrum.

the fundamental from the spectrum of the sampled waveform.

3.3 System Level Simulation of the Proposed Test Method

To verify the application of the proposed enabling techniques a Matlab/Simulink simulation is conducted. The simulation setup is shown in Figure 18. A sinusoidal signal with a period of $5ns$ represented by $x(t) = 1.5\sin(2\pi \times 200 \times 10^6 t))$ is applied to a bipolar mixer to modulate a 2 GHz square carrier. The output of the mixer is

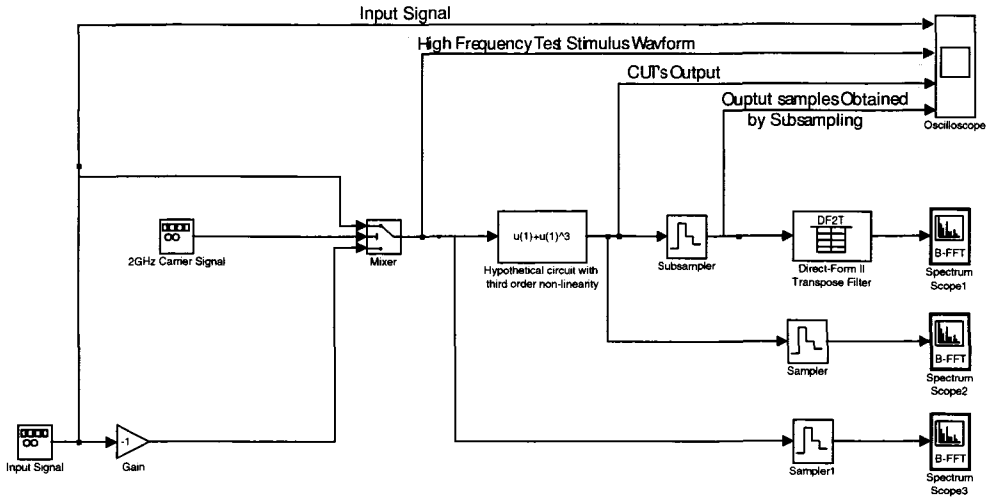

Figure 18: Simulation setup to verify the proposed test technique.

applied to a hypothetical CUT with third order non-linearity which is represented by $y = u(1) + u(1)^3$ where $u(1)$ is the input variable. The response waveform is subsampled with the speed of $5\ ns + 5\ ns/32$. The samples are processed via a digital filter and then applied to a spectrum scope for FFT analysis. A four-channel oscilloscope is used to display signals before and after subsampling in the time domain. The signals obtained by the oscilloscope are shown in Figure 19. Three FFT analyzer modules are used to determine the spectrum of the stimulus signal applied to the CUT, the spectrum of the CUT response and the spectrum of the output after subsapling respectively. The spectrum of the output as shown in Figure 20 indicates that the response of the CUT at 2 GHz is downconverted to 2 GHz/32=62.5 MHz. The effect of the third harmonic distortion is also shown in the simulation results. The conducted simulation shows that if the mixing and subsampling techniques are properly employed a high speed circuit can effectively be tested with low speed measurement instruments.

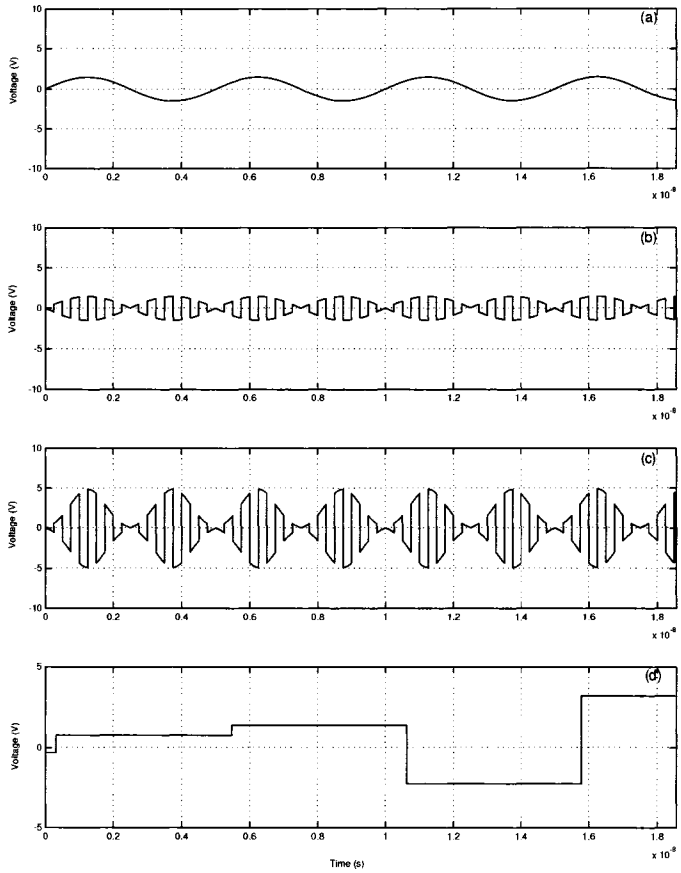

Figure 19: Modulation and subsampling techniques (a) low frequency test generated by the AWG. (b) high frequency test signal applied to a hypothetical CUT. (c) CUT's output signal. (d) samples of the CUT obtained by subsampling.

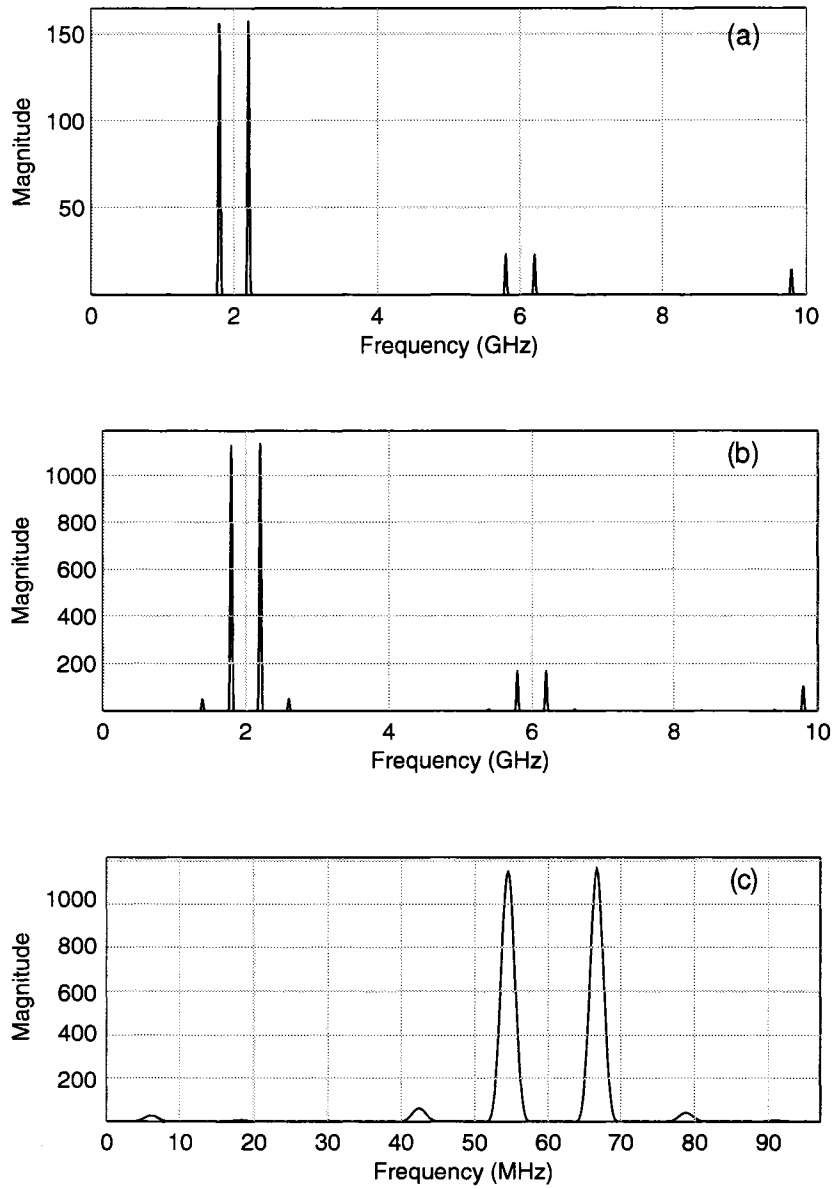

Figure 20: (a) Spectrum of the input waveform applied to the hypothetical CUT. (b) spectrum of the CUT's response waveform. (c) spectrum of the CUT's response after downconversion.

3.4 Architecture of the Proposed Embedded Tester

Figure 21 shows the conceptual block diagram of the tester core. The high frequency

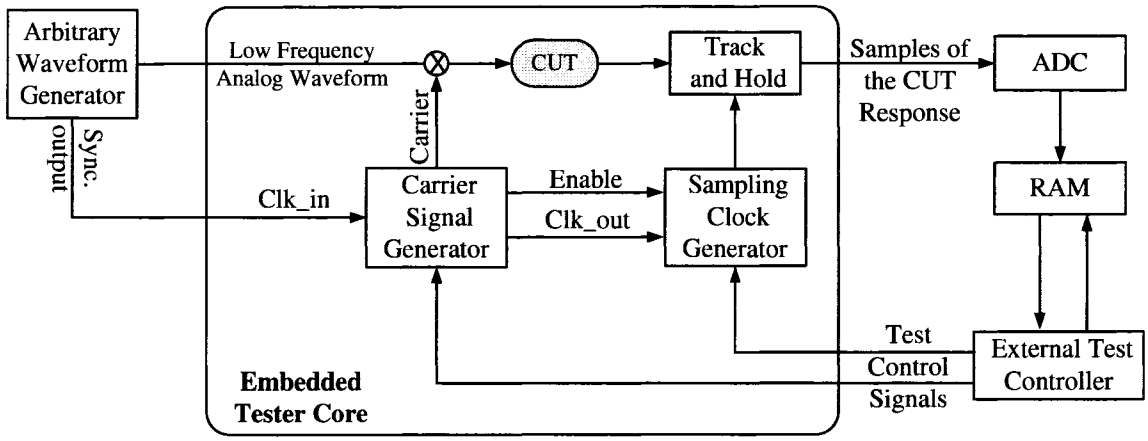

Figure 21: Block diagram of the proposed tester core.

portion of the tester is embedded inside the chip as part of the DFT implementation while the low frequency part that includes AWG, ADC, RAM and Test Controller are externally configured. The tester operates as described below:

The AWG provides a low frequency periodic waveform that modulates the carrier through the mixer. It also provides a sync output which is a digital version of the supplied analog waveform. The sync signal is applied to a PLL driven carrier signal generator to synchronize the carrier with the low frequency waveform supplied by the AWG. This synchronization is required to support coherent subsampling. The mixer's output, which is a high frequency waveform, is applied to the CUT as a test stimulus. The samples of the CUT response waveform are captured through a track and hold circuit. The sampling clock generator provides the T/H with a synchronized clock to obtain proper samples of the CUT's output through subsampling. The captured samples are then transferred to an external controller for test result evaluation.

The proposed test scheme requires precise timing edges to sample the CUT's output at the right moment otherwise the captured samples do not represent the original high frequency waveform. In the proposed tester a coupled PLL and DLL module has been employed for the purpose of synchronization. The external stimulus waveform, the internal carrier and the sampling clock are all synchronized together through this module. This multi-level synchronization enables the tester to chop the AWG waveform to integer-N slices and at the meantime provide a sampling clock to obtain coherent samples of the CUT response through subsampling.

3.5 Test Protocol

The detailed block diagram of the tester in which the digital and the analog portions of the tester are separated is shown in Figure 22. The analog section contains four modules (a) a PLL based synthesizer (b) a DLL (c) a Mixer and (d) a Track and hold circuit. Although in our design the first two modules are designed in the analog domain, it is possible to design them using digital techniques. The digital portion of the circuit receives the timing and control signals as inputs and generates the carrier and the sampling clock as outputs. The timing signals produced by the PLL are used as carrier signals and the DLL timing signals are employed as sampling clocks for the track and hold circuit. Sel_A and Sel_B are applied to multiplexer_A (Mux_A) and multiplexer_B (Mux_B) respectively to select proper PLL and DLL timing signals during the test phase. Data_in and serial clock (Ser_Clk) are used to load required control data in series rather than parallel to lower the number of required I/O pins. Sel_C, which determines the stimulus segment number, is also supplied serially.

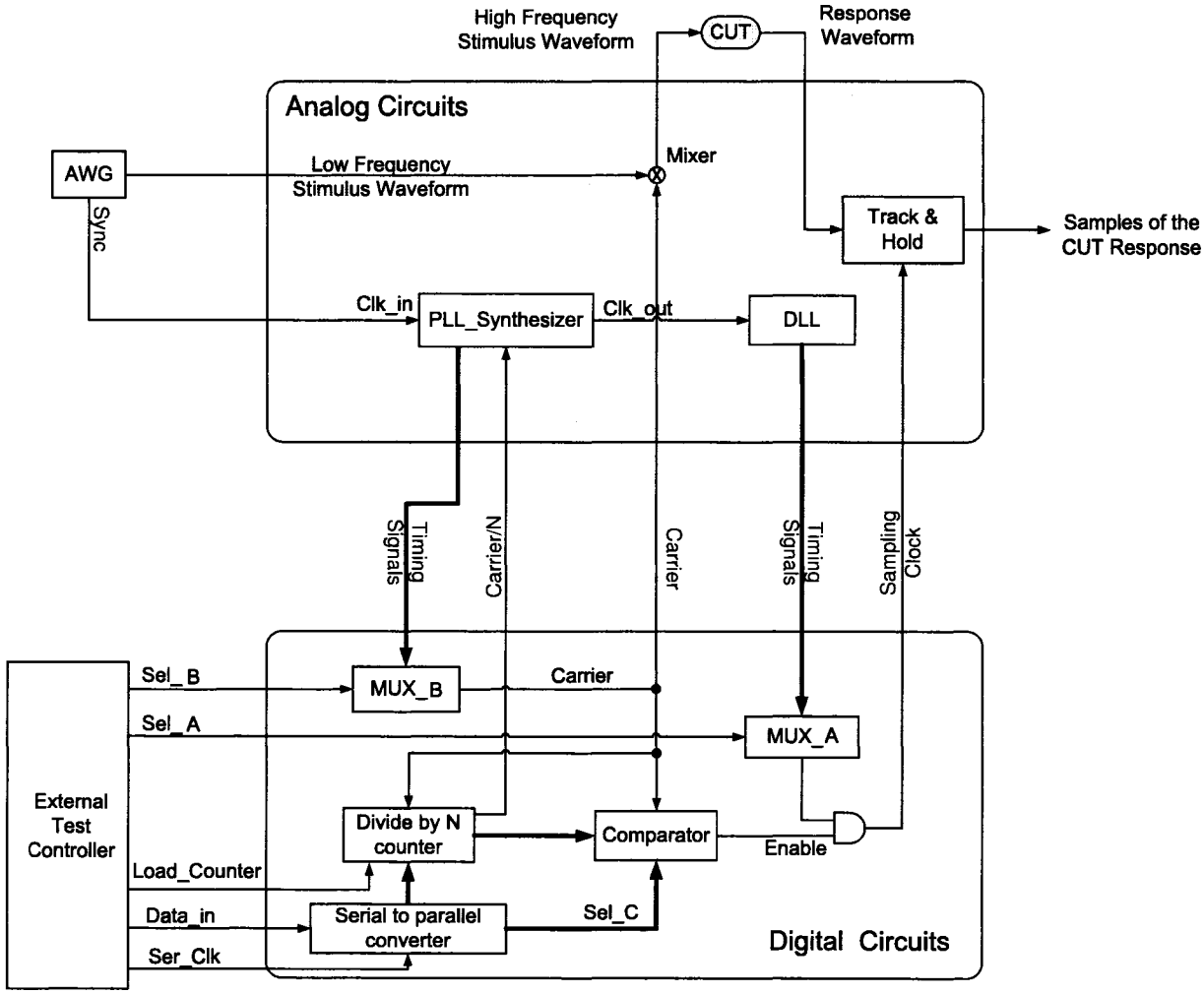

Figure 22: Detailed block diagram of the proposed tester core.

A low frequency periodic stimulus waveform and its sync signal are supplied by the AWG. The PLL receives the sync signal as an input and generates a set of timing signals running N-times faster than the applied AWG waveforms. The timing signals generated by the PLL are equal in frequency but different in phase. Moreover, they are equally distributed over one period of the PLL output signal (Clk_out). These timing signals are selected by Mux_B one by one as a carrier and mixed with the AWG waveform. Figure 23 shows a typical AWG waveform, the PLL timing signal used as a carrier and the mixer's output waveform. The output of the mixer is in fact a periodic set of segments where each segment lasts for one period of the carrier signal. The CUT response to each segment of the stimulus waveform is obtained separately through subsampling until the responses to all segments in one period of the AWG waveform are determined. The DLL circuit provides another set of timing signal to enable the scheme to subsample the response to each stimulus segment separately. To illustrate how a test is carried out, assume that the AWG provides a

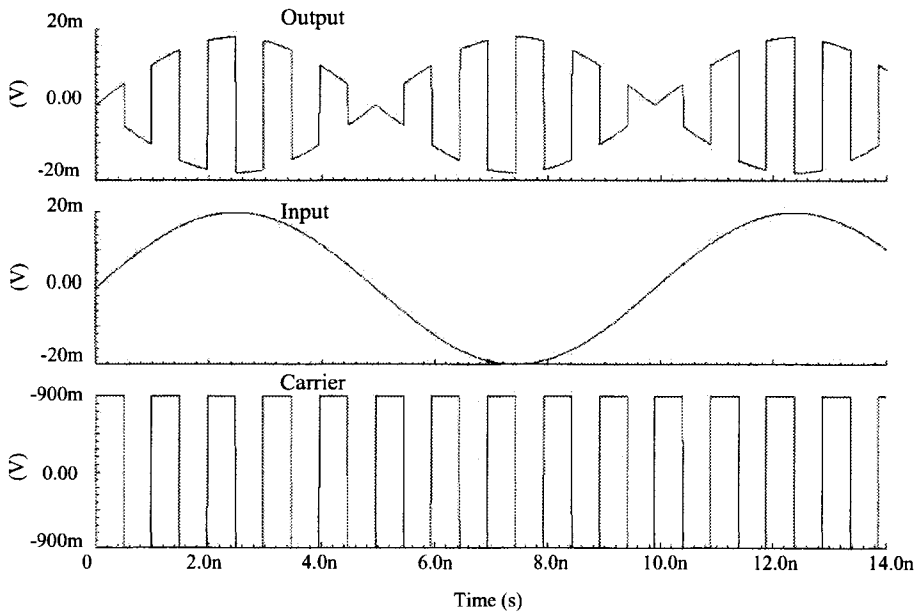

Figure 23: Typical input and carrier signals applied to the mixer and the corresponding output.

low frequency periodic waveform and the PLL and the DLL are in a locked condition. To obtain the CUT's response to a particular segment, for instance segment P, the external test controller sets the segment address (Sel_C) to P and thus, whenever that segment is applied, the segment identifier generates a pulse enabling the T/H module to capture the instances of that particular segment. The T/H repeats the capturing samples of the same instance in every period of the AWG waveform as long as the address lines of the multiplexers (Sel_A and Sel_B) and the segment address remain unchanged. The sampled instance is digitized by a low speed ADC and saved in the RAM memory. To obtain a new instance, Sel-B is advanced by one and a new timing signal is applied to the T/H module as a sampling clock. A total number of K instances of the CUT's response are captured by incrementing Sel-B. Once all DLL timing signals are selected, Sel_A is incremented and the next PLL timing signal is selected as a carrier. Since the newly selected PLL signal is not in phase with the input clock, the PLL starts varying the location of its timing signal edges in time to reacquire the lock again. When the PLL and subsequently the DLL settle down, the edges of all PLL and DLL timing signals are shifted in time and consequently new samples are obtained. The shift and sample procedure for a case wherein the AWG supplies a sinusoidal input of 101.01 MHz (T=9.9 ns) has been illustrated in Figure 24 in which just the first two PLL signals (Carrier_1 and Carrier_2) and the first two sampling clocks (Sampling_Clk_1 and Sampling_Clk_2) are plotted and instances of the second segment of the input waveform are captured. The PLL synthesizer is set such that its oscillator runs 10 times faster than the input, generating signals of 990 ps period. In the implemented tester core, the PLL and the DLL provide 10 and 11 timing signal respectively and thus the PLL timing signals are separated by 99 ps while the DLL timing signals are separated by 90 ps.

3.6 Summary

In this chapter a new test methodology based on an embedded tester for high speed analog/RF circuits was presented. Bipolar modulation and subsampling techniques which are employed as enabling methods were also introduced and then the mathematical description of the proposed test method was presented. To ensure the validity of the proposed test method, a system level simulation was performed using Matlab/Simulink models. In the last sections of this chapter, the conceptual block diagram of the embedded tester was illustrated and the test protocol was specified.

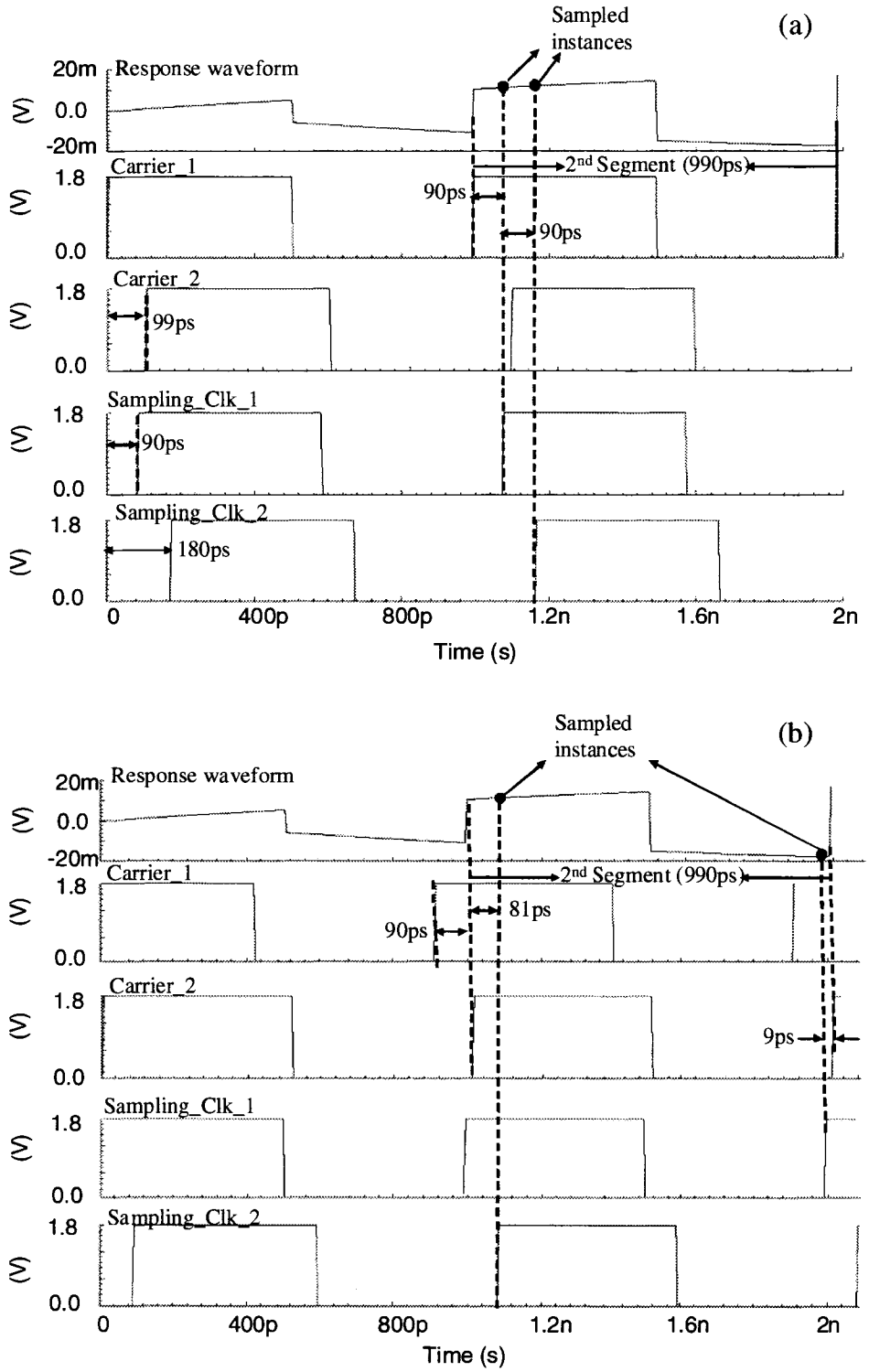

Figure 24: Shift and sample process. (a) when carrier-1 is in phase with the input. (b) when carrier-2 is in phase with the input.

CHAPTER IV

TOPOLOGY SELECTION AND SYSTEM LEVEL SIMULATION

To show the application of the test methodology in practice, an embedded tester core for high speed analog/RF circuits with target specifications detailed in Table 1 has been designed. The proposed tester as shown in Figure (21) has two main units of

Table 1: Embedded Tester Core Design Goals

Technology	1.8 V, 6 Metal, 0.18 μm CMOS Process
Target devices	CMOS RFICs, LNA's, Mixers, Power amplifiers, PLLs, etc.
Area	< 1.00 mm^2
Test frequency range	100 MHz - 2.5 GHz
Maximum sampling clock resolution	< 10 ps

(a) high frequency stimulus generator and (b) response capturing circuitry each of them containing several modules. The topology of each module is selected based on the target specifications of the tester and practical implementation limits imposed by the CMOS 0.18 μm fabrication process.

4.1 High Frequency Stimulus Generator

The employed high frequency stimulus generator (Figure 25) includes an external AWG, a mixer and a carrier signal generator. The AWG provides a sync output in addition to a low frequency stimulus waveform. The carrier signal generator gets the sync signal and supplies the mixer with a digital level signal which is integer-N times faster than the input waveform. The operations of the mixer and the carrier signal

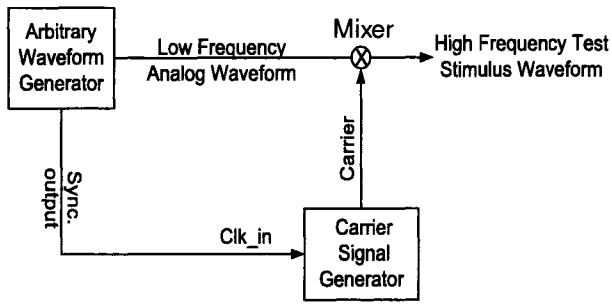

Figure 25: Block diagram of the employed high frequency stimulus generator.

generator are explained below.

4.1.1 Mixer

One of the advantages of using bipolar modulation technique is the direct control over the output amplitude. From Equation (1) it can be seen that the fundamental component at the output is a linear function of the signal level at the input. Consequently, the power of the signal delivered to the CUT at the fundamental frequency can be linearly controlled by the power of the signal supplied by the AWG. This capability simplifies the design of the mixer since regardless of the mixer's conversion gain the amount of power transferred to the CUT can be controlled by the AWG. Therefore, instead of an active mixer a passive mixer can be used which provides a better noise characteristic and improved linearity.

A bipolar chopper can be implemented using a passive mixer [51] that constitutes just a single selector switch as shown in Figure 26. Assuming an ideal squarewave carrier, the voltage conversion gain of the mixer can be calculated as follows. For an input signal of $x(t) = A_{in}cosw_{in}t$ from (1) the output $y(t)$ is equal to:

$$y(t) = \frac{2A_{in}}{\pi}cos(w_s - w_{in})t - \frac{2A_{in}}{3\pi}x(t)cos(3w_s - w_{in})t + ... \quad (5)$$

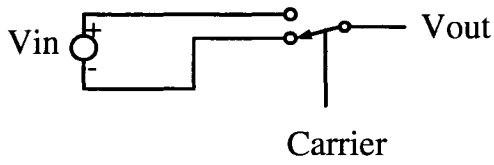

Figure 26: Block diagram of a passive chopper modulator.

and the voltage conversion gain is:

$$G_c = \frac{amplitude\ \ of\ \ the\ \ fundamental}{amplitude\ \ of\ \ the\ \ input} = \frac{\frac{2A_{in}}{\pi}}{A_{in}} = \frac{2}{\pi} \tag{6}$$

To verify the parameters and specification of the mixer a Matlab/Simlink model has been developed and simulated. Figure 27 shows the simulation setup to test the mixer. The input and output waveforms and their spectrum are shown in Figure 28. It can be observed that the output spectrum as expected just contains the odd harmonics. The mixer's power conversion gain by definition is equal to $G_c = \frac{power\ \ of\ \ the\ \ fundamental\ \ at\ \ the\ \ output}{power\ \ of\ \ the\ \ input\ \ signal}$ and thus from the simulation results we can write: $G_c \simeq 68/170 = 0.4 \simeq (\frac{2}{\pi})^2$ which confirms the conversion gain obtained form mathematical model using Equation (6).

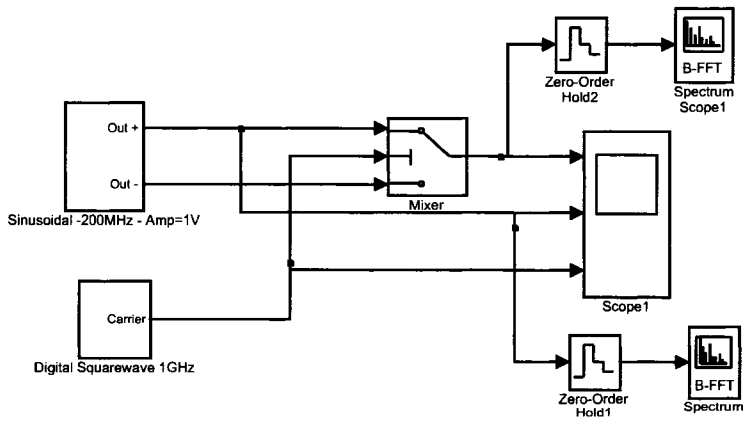

Figure 27: Simulation setup in Matlab/Simulink to test the mixer.

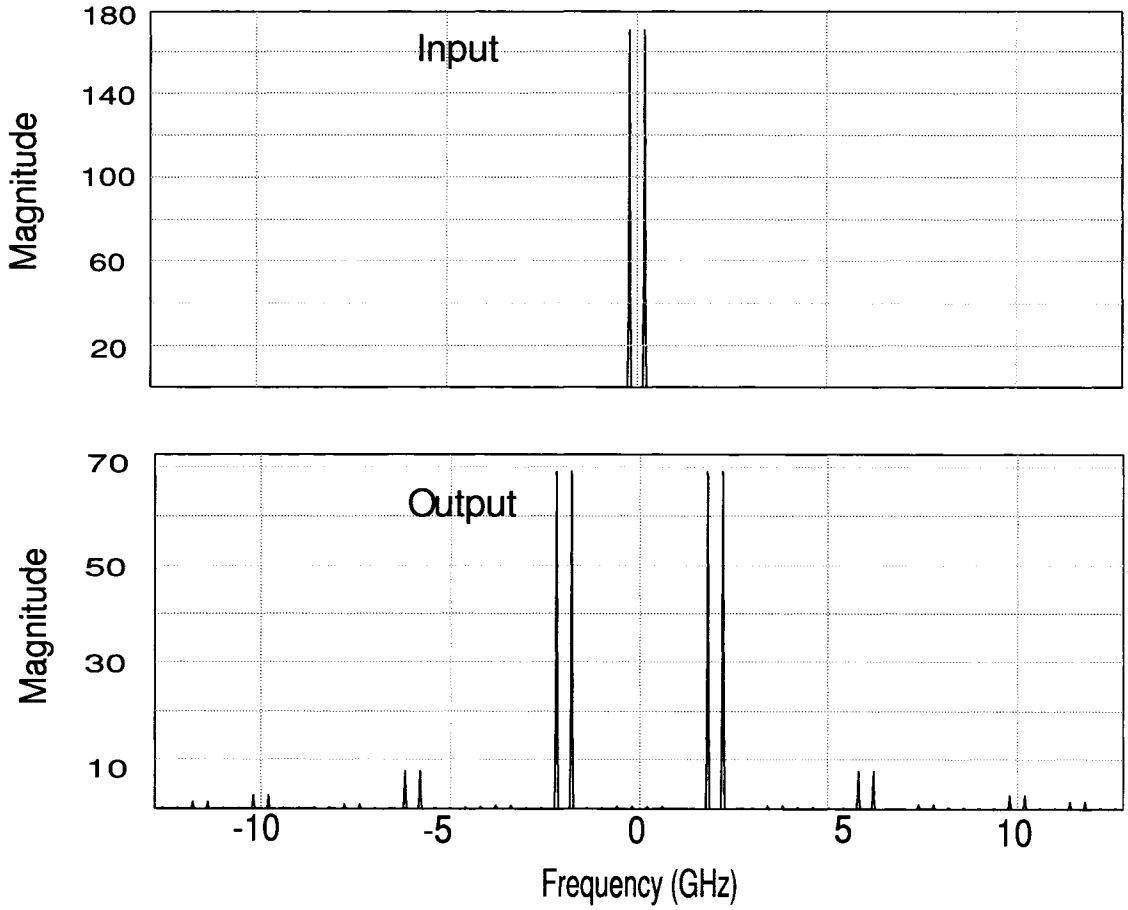

Figure 28: Simulated spectrum of the input and output waveforms.

4.1.2 Carrier Signal Generator

The carrier signal generator is expected to get the sync signal as an input and generate a carrier signal which is N-times faster than the sync signal. An integer-N PLL-synthesizer [48, 49, 51] can be utilized as a core block to meet this requirement. There are two major types of PLL architectures: (a) traditional linear architecture which is also called type I and (b) charge pump PLL also called type II. Although type I has been widely used in various applications, it has several shortcoming such as a limited acquisition range and trade off between its filter bandwidth and the phase error. Thus, the charge pump PLL (type II) topology is selected to design the carrier generator. The type II PLL synthesizer comprises a Phase Frequency Detector (PFD), a Charge Pump (CP), a Low Pass Filter (LPF) and a Voltage Controlled Oscillator (VCO) as shown in Figure 29.

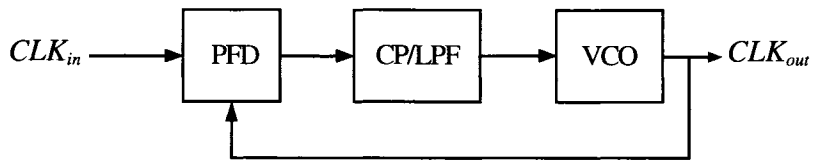

Figure 29: Block diagram of type II PLL.

1. **Phase Frequency Detector** [48]

   The performance of the PLL is greatly affected by the type of the employed phase detector. There are four main types of phase detectors as follows.

   (a) XOR gate which can be used as a simple PD. It produces error pluses on both rising and falling edges of the input signals.

   (b) Four-quadrant analog multiplier which offers significant noise suppression.

   (c) J-K flip flop which is an edge-triggered PD and produces an output that is not sensitive to the input waveform asymmetry.

(d) Phase Frequency Detector

The output signal of PFD depends on the phase error in the locked state and in the unlocked condition, the output is a function of frequency error. Consequently, a PLL using PFD always locks on the input irrespective of the type of loop filter used.

Due to the advantages of the PFD, this architecture is selected for the design of the PLL. Figure 30 shows the implementation of the PFD and its typical input and output waveforms. Defining the output as the average of Q_A and Q_B when

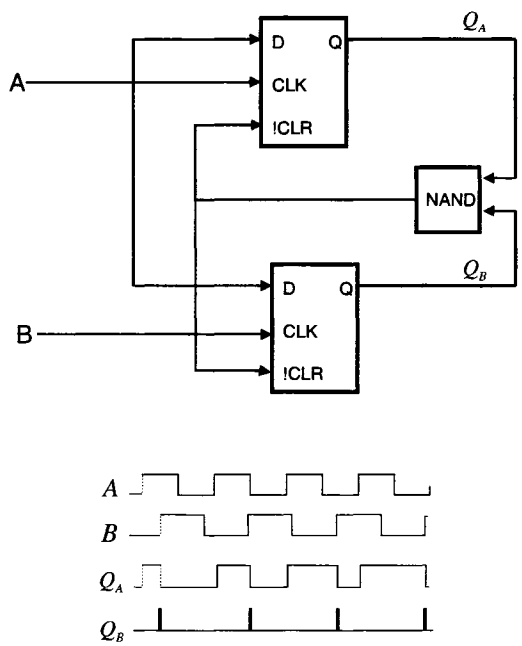

Figure 30: Selected PFD architecture and its typical input and output signals waveforms.

$\omega_A = \omega_B$, the output varies linearly when the phase difference changes from -360 to +360 as illustrated in Figure 31.

2. **Charge Pump**

A common approach to obtain average value of the PFD outputs is to use a charge pump [52]. The PFD with a charge pump circuit is shown in Figure 32.

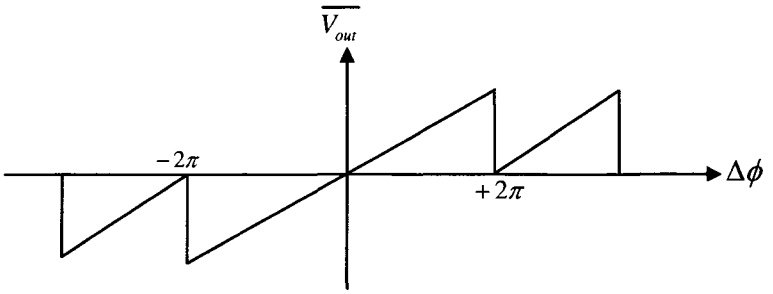

Figure 31: Characteristic of the PFD.

It has three states as follows:

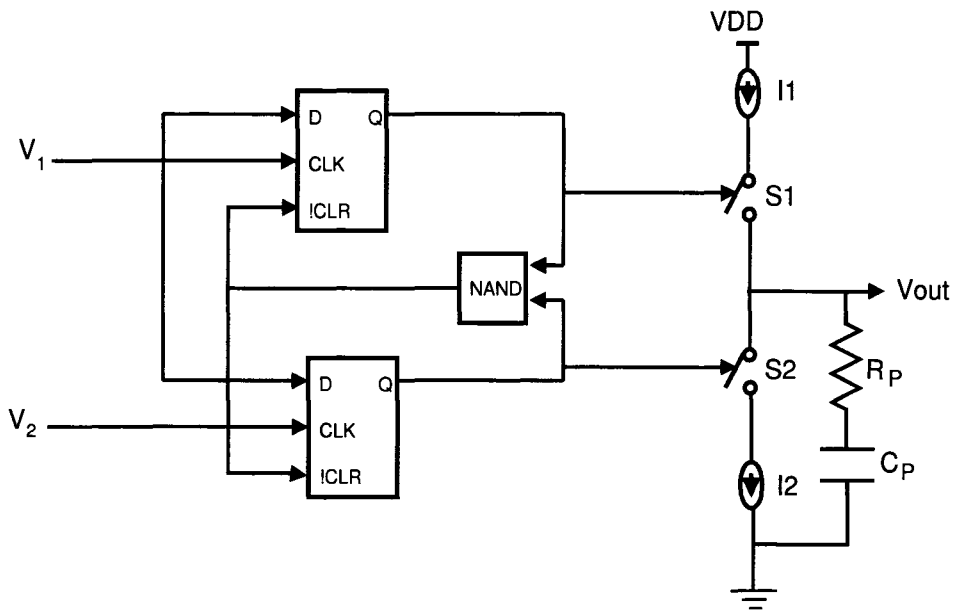

Figure 32: PFD followed by a charge pump.

(a) $Q_A = Q_B = 0$ and thus S_1 and S_2 are off and V_{out} remains unchanged.

(b) Q_A=high, Q_B=low where S_1 is on and I_1 charges C_p.

(c) Q_A=high, Q_B =low where S_2 is on and I_2 discharges C_p.

If at $t = 0$ a step phase of ϕ_0 is injected to the input B, Q_A produces error pulses (Figure 33) with duration of $\phi_0 T_{in}/(2\pi)$. Consequently, the output voltage is

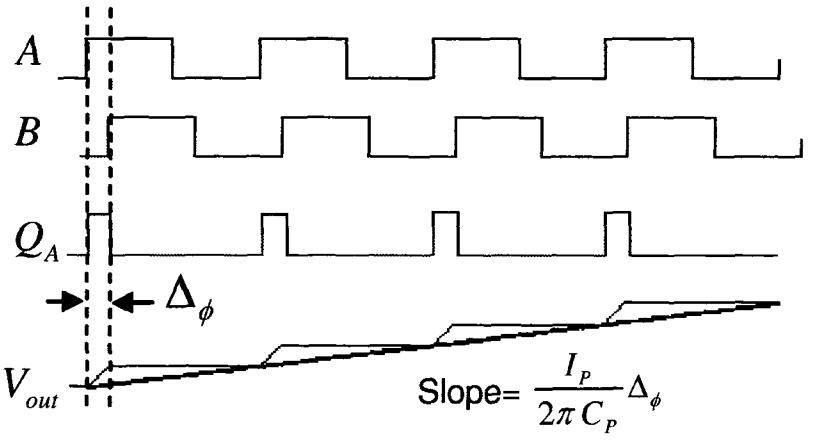

Figure 33: Step response of the employed PFD/CP/LPF module.

increased by $(I_P/C_P)\phi_0 T_{in}/(2\pi)$ in every period. If the output is approximated by a ramp, V_{out} can be expressed as [48]:

$$V_{out}(t) = \frac{I_p}{2\pi C_p} t\phi_0 u(t) \tag{7}$$

From Equation (7) the impulse response is equal to:

$$\frac{dV_{out}(t)}{\phi_0 dt} = h(t) = \frac{I_p}{2\pi C_p} u(t) \tag{8}$$

Thus, the transfer function can be expressed as:

$$\frac{V_{out}}{\Delta\phi_s}(s) = \frac{I_p}{2\pi C_p} \times \frac{1}{s} = K_{PFD} \times \frac{1}{s} \tag{9}$$

$K_{PDF} = \frac{I_p}{2\pi C_p}$ is the gain of the PFD.

Figure 34 shows the system level representation of the PD/CP/LPF module in Matlab/Simulink environment. The current injected and drawn ($I1$ and $I2$) by the charge pump is assumed to be 20 μA and modeled by constant value of $\pm\frac{3.6}{18e4}$. This amount of current can be supplied by a moderate size transistor in the target CMOS technology without oxide breakdown. The value of the resistor and capacitor in the charge pump are chosen to be $R_P = 7\ K$ and $C_P = 3\ pf$. A higher value for C_P is desirable owing to its positive effect on enhancing the stability and jitter reduction; however, due to the considerable area overhead of

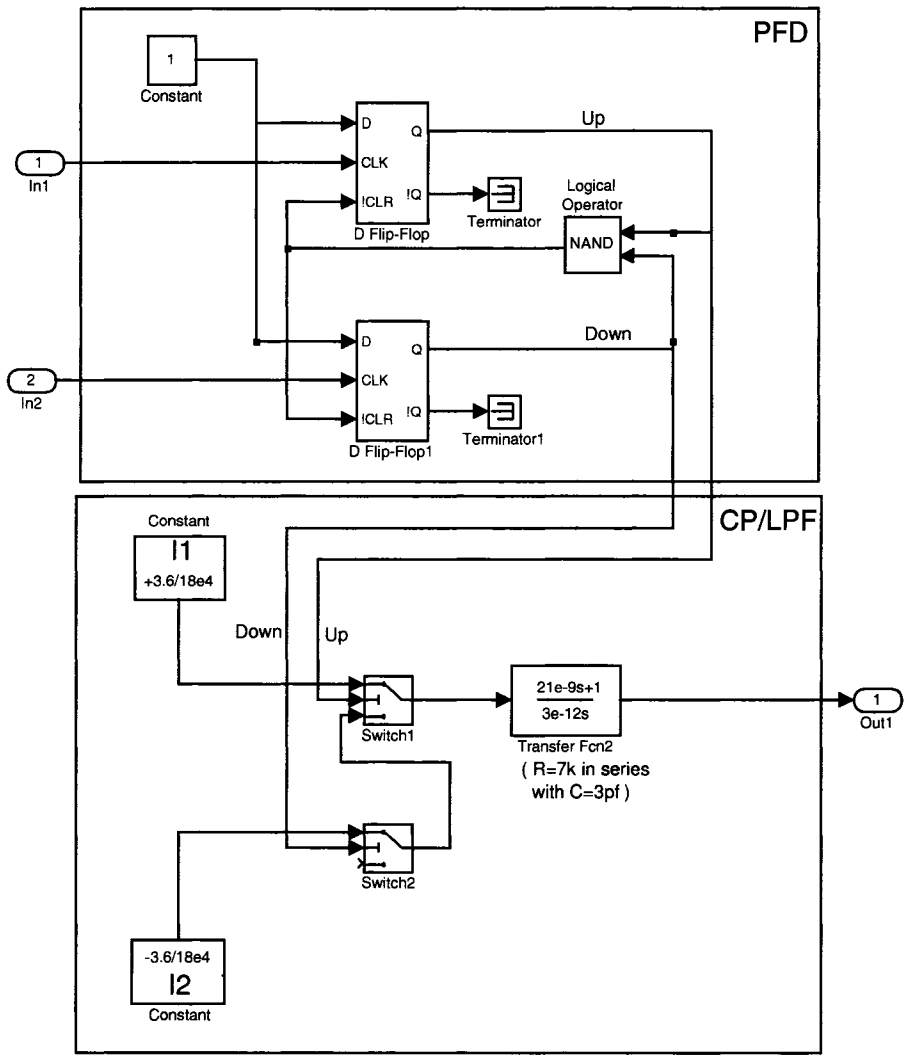

Figure 34: System level representation of the PD/CP/LPF module in Matlab.

capacitance implementation on CMOS process maximum amount of 3 pf appears to be reasonable. The simulation results in Figure 35 show two inputs of 1 GHz with $\pi/2$ phase difference together with the output of the system. The gain of the PFD, which by definition is given by: $K_{PFD} = \frac{I_P}{2\pi C_p} = \frac{20e-6}{2\pi \times 3.3e-12} = 9.65e5$, form Figure 35 is determined to be $K_{PFD} = \frac{slope}{\pi/2} = \frac{0.05/(3\times 10^{-8})}{\pi/2} \simeq 1e6$ confirming the calculated value.

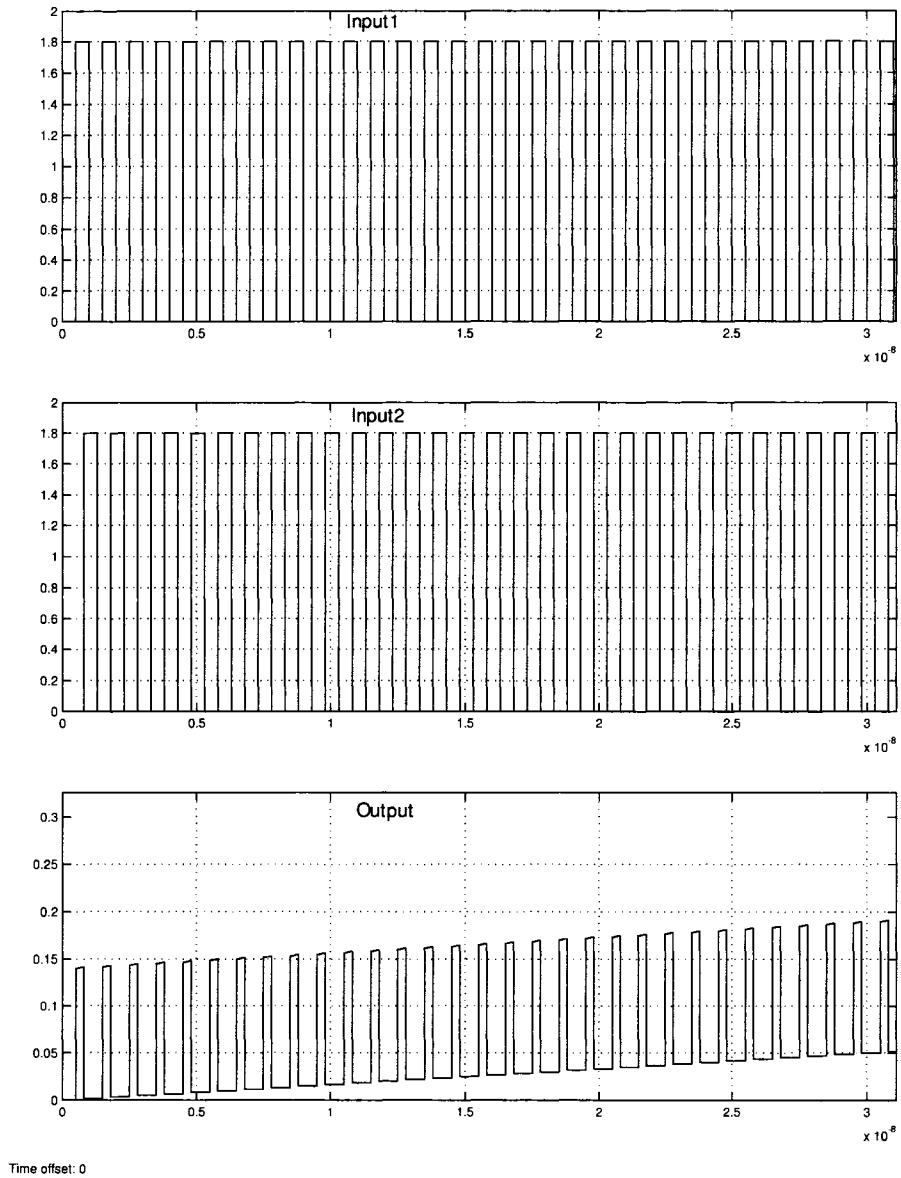

Figure 35: Input and output of the PFD/CP/LPF.

3. **Voltage Controlled Oscillator (VCO)**

There are two main types of VCO (a) LC based VCO and (b) ring oscillator type VCO. Generally, an LC based VCO offers a high quality factor (Q) and a relatively low phase noise [53]. However, with on-chip inductors the high Q advantage is largely diminished due to the low quality factor of on-chip inductors. Off-chip inductors can be used to achieve high Q, however this approach can significantly add to the complexity of test setup. Thus, the ring oscillator based VCO is selected to be used in the PLL. Linear model of an ideal VCO is defined by:

$$\omega_{out} = \omega_0 + K_{VCO} V_{cnt} \tag{10}$$

Where ω_0 is angular frequency corresponding to $V_{cnt} = 0$ and K_{VCO} represents the gain. The relationship between the phase and frequency of a waveform is given by:

$$\phi(t) = \int \omega dt + \phi_0 \tag{11}$$

for a sinusoidal output we can write:

$$V_{out}(t) = V_m cos(\int \omega_{out} dt + \phi_0) \tag{12}$$

substituting for ω_{out} from equation (10) yields to:

$$V_{out}(t) = V_m cos(\omega_0 t + K_{VCO} \int V_{cnt} dt + \phi_0) \tag{13}$$

The term $K_{VCO} \int V_{cnt} dt$, which is called excess phase (ϕ_{ex}), can be used to define the PLL transfer function as follows:

$$\frac{\phi_{ex}}{V_{cnt}}(s) = \frac{K_{VCO}}{s} \tag{14}$$

4.1.2.1 Linear Model and Stability Analysis of the Employed PLL

The linear models of the PFD/CP/LPF and VCO can be used to construct a linear model for the employed PLL. From the linear model presented in Figure 36 the relationship between the input and the output can be determined and the transfer function is defined by:

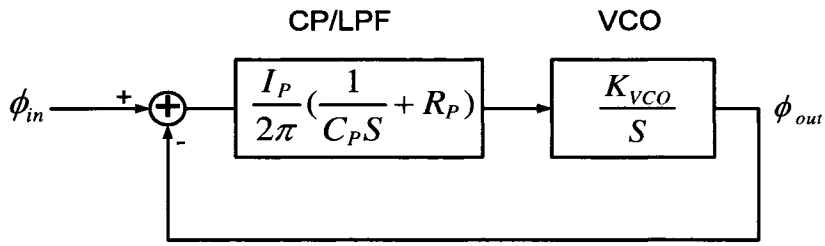

Figure 36: Linear model of the employed PLL.

$$H(s) = \frac{I_p K_{VCO}/2\pi C_P}{s^2 + I_p K_{VCO}/2\pi C_P} \tag{15}$$

The loop gain has two poles at the origin one established by the CP/LPF and the other by the VCO. These poles at the origin will cause stability problem since each of them contributes 90^0 phase shift allowing the system to oscillate at the crossover frequency. One solution to the stability problem is to add a zero to the transfer function. This can be done by adding a resistor in series with the loop filter capacitor. The transfer function of the modified PFD/CP/LPF module is given by:

$$\frac{V_{out}}{\Delta\phi} = \frac{I_p}{2\pi}(R_p + \frac{1}{C_p s}) \tag{16}$$

and thus the PLL transfer function is modified to:

$$H(s) = \frac{\frac{I_p K_{VCO}}{2\pi C_P}(R_P C_P s + 1)}{s^2 + \frac{I_P K_{VCO}}{2\pi} R_P s + \frac{I_P K_{VCO}}{2\pi C_P}} \tag{17}$$

This transfer function represents a second order system with a zero at $s = -1/(R_P C_P)$. The natural frequency and damping factor of the system are given by:

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_P}} \tag{18}$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi}} \tag{19}$$

After determining the stability criteria and the topology of the building blocks, a system level simulation can be conducted. The system level model for each block has been developed based on the assumption that the system is going to be implemented on CMOS 0.18 μm process. Therefore, initial values for the power supply and the circuit elements are chosen to be within reasonable limits imposed by the process, area overhead and power consumption limitations.

An important concern in the design of the VCO is the deviation of its output frequency from its nominal value due to the process variation. Therefore, it is required to increase the tuning range to make sure that the desired frequency range can be supported under the worst case process variation. This requirement is in sharp contrast with the requirement to minimize the noise effect. If a noise amount of ν is imposed on the control voltage of a VCO, the output frequency changes from $\omega_{out} = \omega_0 + K_{VCO} V_{cnt}$ to $\omega_{out} = \omega_0 + K_{VCO}(V_{cnt} + \nu)$ indicating a frequency variation of $\Delta\omega = K_{VCO}\nu$. Generally, for allowable control voltage range of $V_1 < V_{cnt} < V_2$ and tuning range of $\omega_1 < \omega_{out} < \omega_2$ the VCO gain (K_{VCO}) has to satisfy the following requirement:

$$K_{VCO} \geq \frac{\omega_2 - \omega 1}{V_2 - V_1} \tag{20}$$

Based on the above discussion and the target specification of the tester, the center frequency of 1.7 GHz and the VCO gain of $K_{VCO} = 5e9\ Hz/V$ with a tuning range of 1 $GHz < f < 2.5\ GHz$ are chosen as target design parameters

of the VCO. Based on the design values of $K_{VCO} = 5e9\ Hz/V$, $I_P = 20\ \mu A$, $R_P = 7\ K$ and $C_P = 3\ pf$ from (16) the damping factor of the system is given by:

$$\zeta = \frac{7000}{2} \times \sqrt{\frac{20e-6 \times 3e-12 \times 5e9}{2\pi}} \simeq 0.7 \tag{21}$$

The bode diagram of the open loop transfer function shown in Figure 37 indicates that the PLL system is stable and presents a phase margin of 80^o.

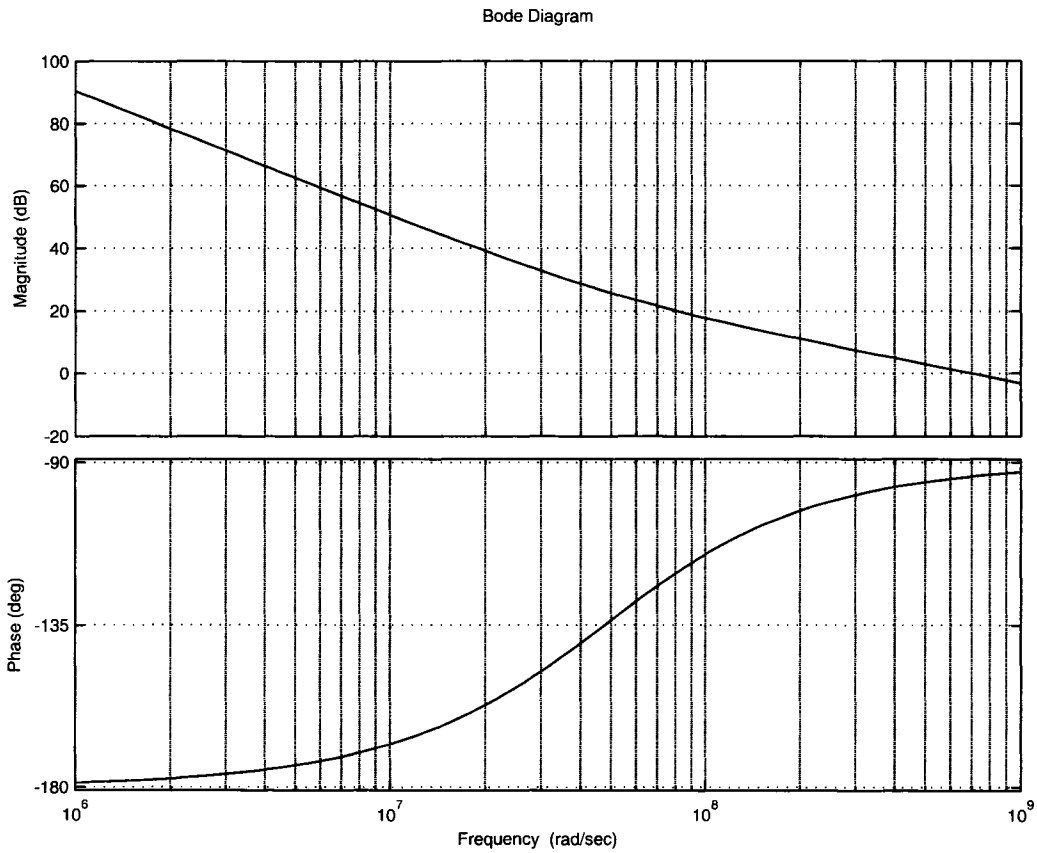

Figure 37: Bode diagram of the open loop transfer function of the PLL.

Figure 38 shows the simulated control voltage of the PLL. It indicates that the PLL can successfully lock on the input signal with an acceptable overshoot. When the PLL is in the locked condition the simulation result shows no noise or

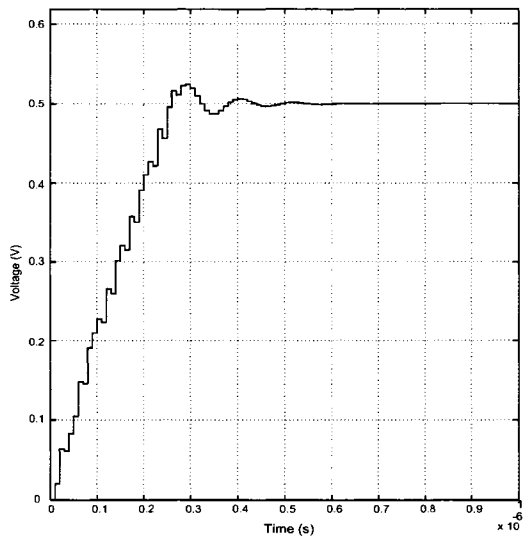

Figure 38: The simulated control voltage of the PLL.

ripple on the control voltage. This is due to the ideal models used for the system level simulation. In practice, various sources of noise such as clock feedthrough, CMOS switch charge injection [54, 55] and the power supply noise contribute to the total amount of the ripple imposed on the control voltage that eventually translates into jitter.

4.1.2.2 Frequency Synthesizer

Synthesizers are actually frequency multipliers and a PLL [56, 57] can readily be modified to a frequency synthesizer by inserting a frequency divider in the feedback loop as indicated in Figure 39. At the locked condition, the signals applied to the PFD must have the same frequency. For the configuration indicated in Figure 39 when the PLL locks we can write $f_{in} = f_{lp}$ and $f_{lp} = f_{out}/N$

thus $fout = N \times f_{in}$. To provide a range of frequencies a programmable divide by N counter can be used. Assuming that N is an integer number and $N_{min} < N < N_{max}$ the output frequency is given by: $N_{min}f_{in} < f_{out} < N_{out}f_{in}$. It is important to note that if N is incremented by one the output frequency is

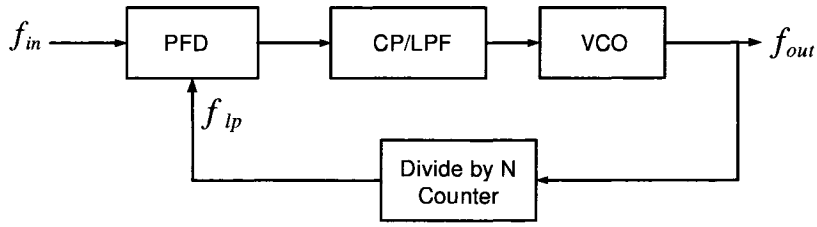

Figure 39: Block diagram of the employed PLL synthesizer.

increased by f_{in}. Thus, the output frequency changes in steps with a minimum value determined by the frequency of the input. The integer-N architecture can be modified to overcome this limitation however for our test application it is not required. Since we have control over the signal through the external AWG, the desired VCO frequency can be selected by changing both the AWG frequency and the value of N.

When the PLL locks on the applied sync signal, the VCO is synchronized with the input waveform causing the carrier to oscillate exactly integer-N times faster than the AWG waveform. Figure 40 shows a Matlab/Simulink setup in which a divide by N counter added to the PLL creating an integer-N synthesizer. The simulation results for N=8 are shown in Figure 41. In the locked condition, as indicated in Figure 41 the VCO output runs 8 times faster than the input signal.

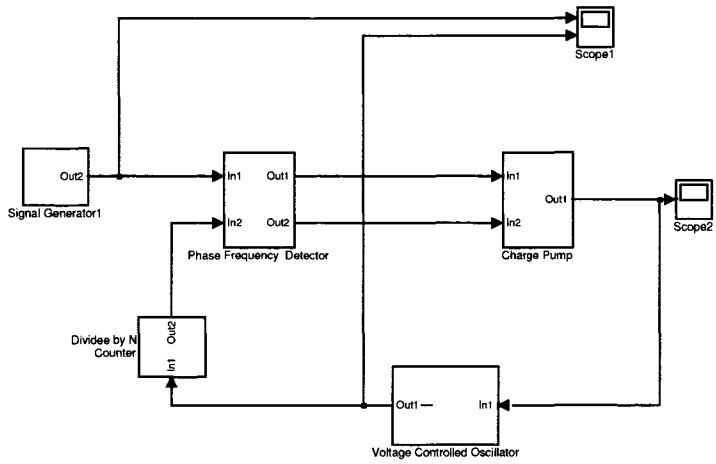

Figure 40: Matlab/Simulink setup for the synthesizer.

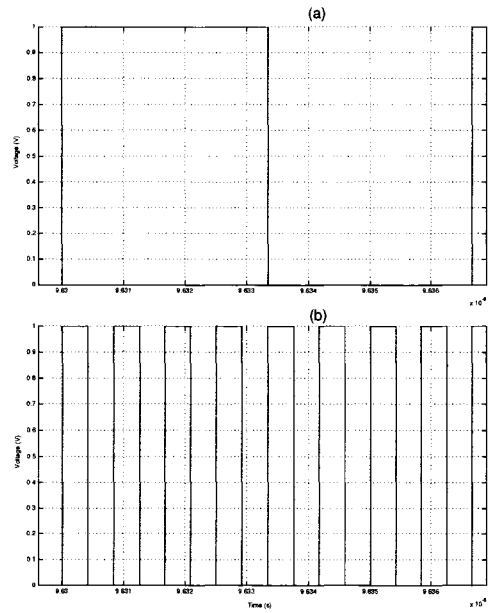

Figure 41: Synthesizer simulation results for N=8. (a) input and (b)output.

4.1.3 Block Diagram of the Carrier Signal Generator in Matlab

After topology selection and performance verification for each unit of the high frequency stimuli generator module, its overall performance can be evaluated through simulation. Figure 42 shows the system level implementation of the high frequency stimulus generator. A 200 MHz sinusoidal waveform with its sync signal has been generated by the AWG and applied to the PLL synthesizer. The value of N is chosen to be 8 for this experiment. The output of the mixer is

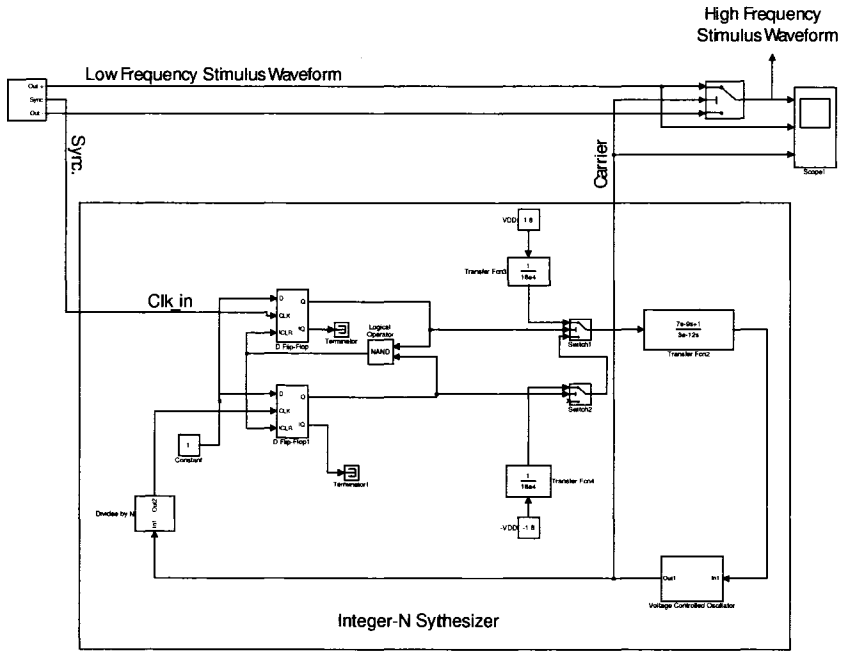

Figure 42: Simulink test setup for the high frequency stimulus generator.

shown in Figure 43 which in fact is the chopped version of the input signal. As expected, it can be observed that each period of the AWG waveform is chopped into eight equal-size segments.

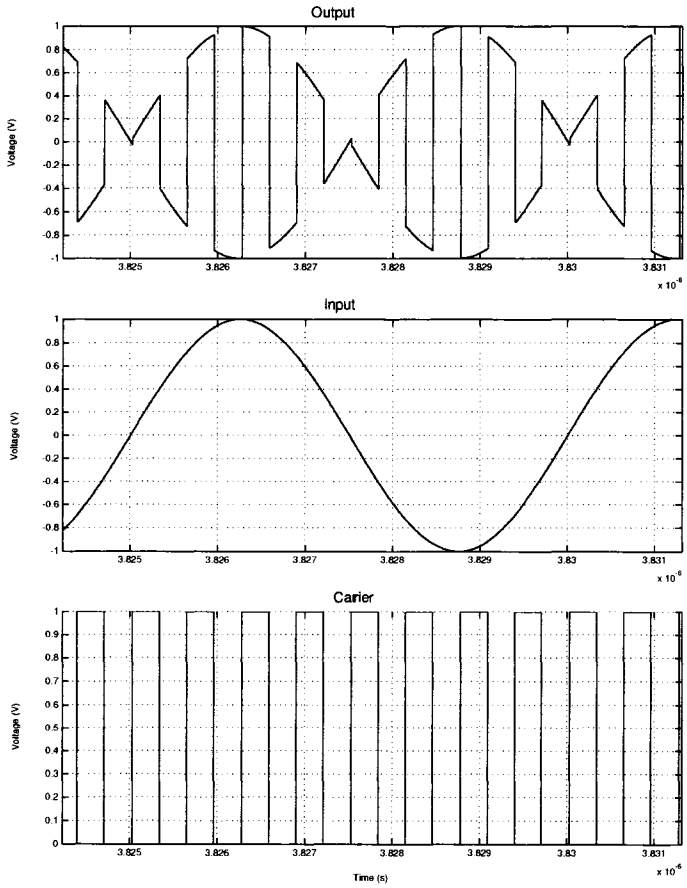

Figure 43: Simulation results for the high frequency stimulus generator.

4.2 Response Capturing Circuitry

The response capturing unit as shown in Figure 44 includes two main modules of (a) Sampling clock generator and (b) Track and hold circuit. The sampling clock generator synchronizes the sampling clock with the CUT's response waveform in order to obtain proper samples through the T/H circuit.

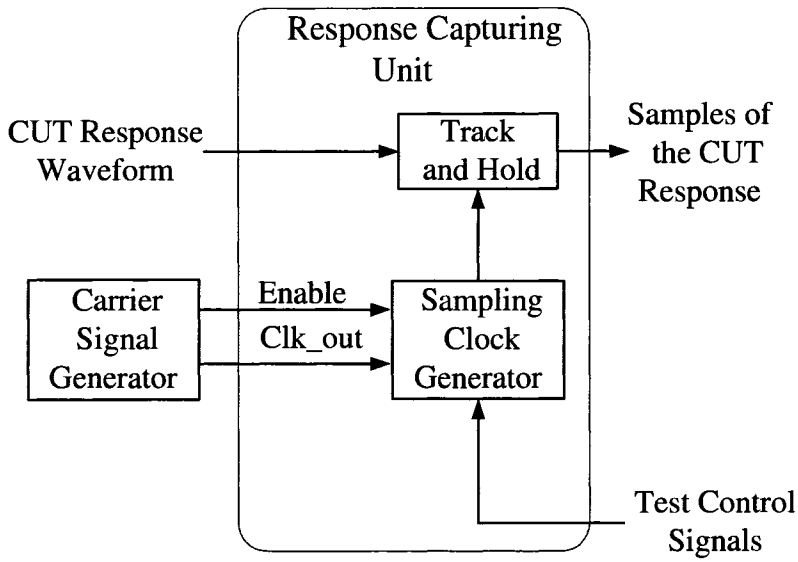

Figure 44: Block diagram of the response capturing module.

4.2.1 Sampling Clock Generator

In the proposed test scheme, the applied stimulus is a periodic set of analog segments where each segment lasts for one period of the carrier. To determine the CUT's overall response, its response to each segment is obtained separately until the CUT's response to all segments in one period of the AWG waveform is determined. This operation requires a precise sampling clock and a segment identifier. To capture the CUT's response to a particular segment, the segment identifier is programmed to enable the sampling clock whenever the desired segment is applied to the CUT and disable it afterwards.

The carrier signal generator contains a segment identifier to provide Enable signal in addition to the Clk_out for the sampling clock generator. The operation of timing signal generator and its interaction with the segment identifier unit is described below.

1. Timing Signal Generator

   To capture proper instances of the CUT's response waveform through subsampling, the period of the sampling clock has to be $T_{clk} = M \times T_{in} + \Delta T$ where ΔT is a small increment and M is an integer number. Due to practical implementation problems, instead of a clock with a programmable period a set of timing signals that are accurately distributed over one period of the sampled waveform is employed for the purpose of subsampling. A single symmetrical delay line either in the form of a VCO in a PLL or a Voltage Controlled Delay Line (VCDL) in a delayed locked loop [57, 58] can be used to provide accurate timing signals. Figure 45 shows a delay line composed of three inverter cells configured as a ring oscillator. Assuming that the propagation delay of each inverter is equal to T_d and the circuit begins with $V_A = high$, after three cell delays ($3T_d$) the voltage at node A falls and it takes the same amount of time for V_A to rise back again yielding an oscillation period of $6T_d$. The difference between the rising edges at the output of the inverter cells as shown in Figure 45 is equal to $T_{VCO}/3 = 2T_d$.

   The sampling clock and the sampled waveform can be synchronized using

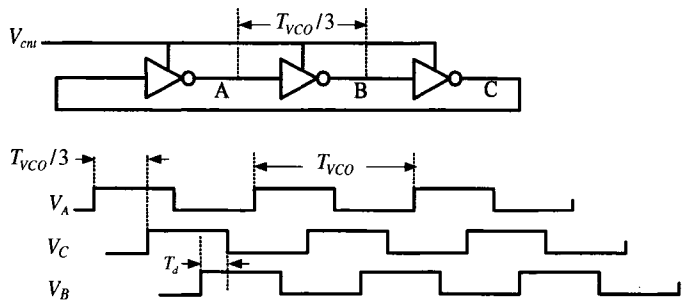

Figure 45: Timing signal generator using a VCO.

either a PLL or a DLL block. For the purpose of frequency synthesis it is preferred to use a PLL since frequency multiplication is difficult to handle with DLL circuits. However, for the purpose of subsampling, using a DLL offers attractive advantages such as lower jitter and higher degree of stability. Therefore, a DLL architecture was chosen to generate timing signals. The building blocks of DLL and PLL are quite similar. The only difference is the replacement of the VCO with a VCDL in DLL. The main idea is that if a periodic waveform is delayed by an integer times of its period, then the phase difference between the original and the shifted waveforms will be zero. Figure 46 shows the block diagram of a DLL which includes a VCDL. The VCDL comprises a series of identical delay stages to provide phase shift between the input and the output waveforms. The DLL loop settles down when the phase difference between the input and output approaches kT_{in} where k is an integer value and T_{in} is the period of the input. The VCO module in a PLL contributes a pole at

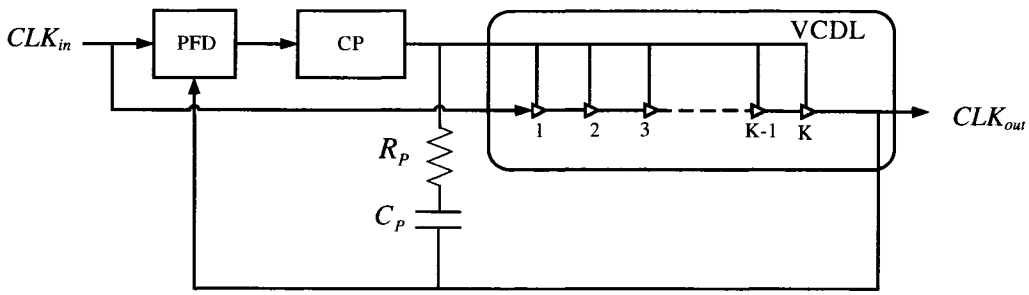

Figure 46: DLL building blocks.

the origin to the transfer function undermining the loop stability. However, as shown in Figure 47 the transfer function of a DLL contains just one pole and thus its loop is always stable. For a DLL containing the same delay stages the delay between the input and output, at the locked condition, is given by nT_{in} thus the phase difference between each consecutive stages is equal to nT_{in}/K

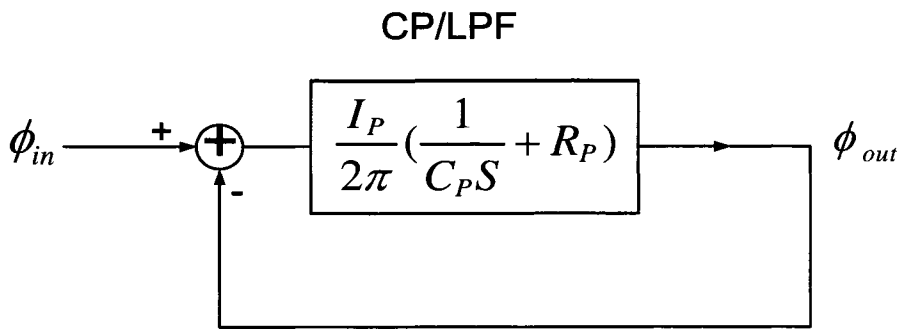

Figure 47: DLL linear model.

regardless of the process or temperature variations. Although a PLL or a DLL based timing signal generator can offer accurate timing signals, they suffer from a limited timing resolution of one cell delay (T_d). To overcome this limitation, in the proposed sampling scheme, Vernier method [59] that comprises two delay lines has been employed so that the difference between the cell delay values determines the timing resolution. Figure 48 shows a timing signal generator that includes two delay lines wherein the first one is configured as a VCO and the second as a VCDL creating a coupled PLL and DLL structure that generates precisely aligned timing signals. Assuming both the PLL and the DLL are in a locked condition and the DLL is locked on one period of its input clock, the structure generates two sets of timing signals that are distributed over one period of the VCO. The delay between the rising edges at the input and the output of each delay cell in the VCO equals to T_{VCO}/L and in the VCDL it is equal to T_{VCO}/K where L and K are the number of delay cells in the VCO and the VCDL respectively and T_{VCO} represents one period of the VCO. If the timing signals supplied by the PLL and the DLL are properly employed, the scheme supports timing resolution of $\Delta = T_{VCO}/L - T_{VCO}/K$ which can be significantly less than one cell delay.

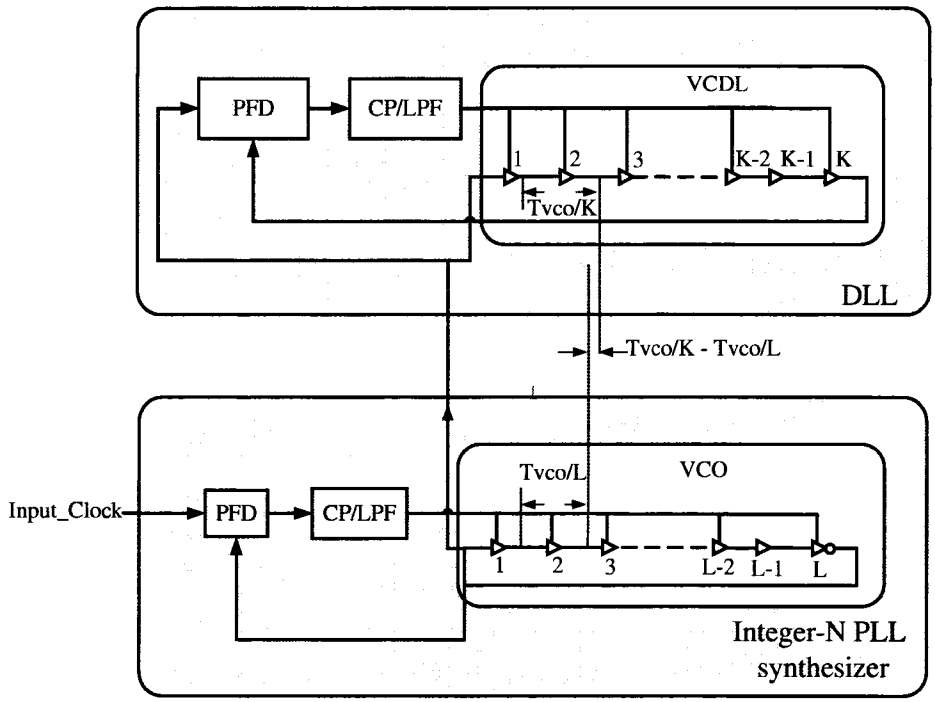

Figure 48: Precision timing signal generator using a coupled PLL and DLL module.

To take the advantages of such a high resolution timing signal generator, the VCO and the VCDL in the embedded tester are implemented using the same type of delay cells. For the application of high resolution sampling the timing signals have to be selected in sequence and applied as sampling clocks to an ADC. This is done by adding multiplexers to the VCO and the VCDL outputs as illustrated in Figure 49. The timing signal generator illustrated in Figure 49 operates as follows:

The propagation delay of Mux-A, Mux-B and the divide by N counter add a constant offset to the location of the rising edges at the output Y. The constant offset delay does not undermine the subsampling procedure and thus for the sake of simplicity, the offset delay is not included in the following analysis. When both the DLL and the PLL are locked to their inputs, the VCO output at node X is in-phase with the input clock. Thus, the delay between the rising edges at

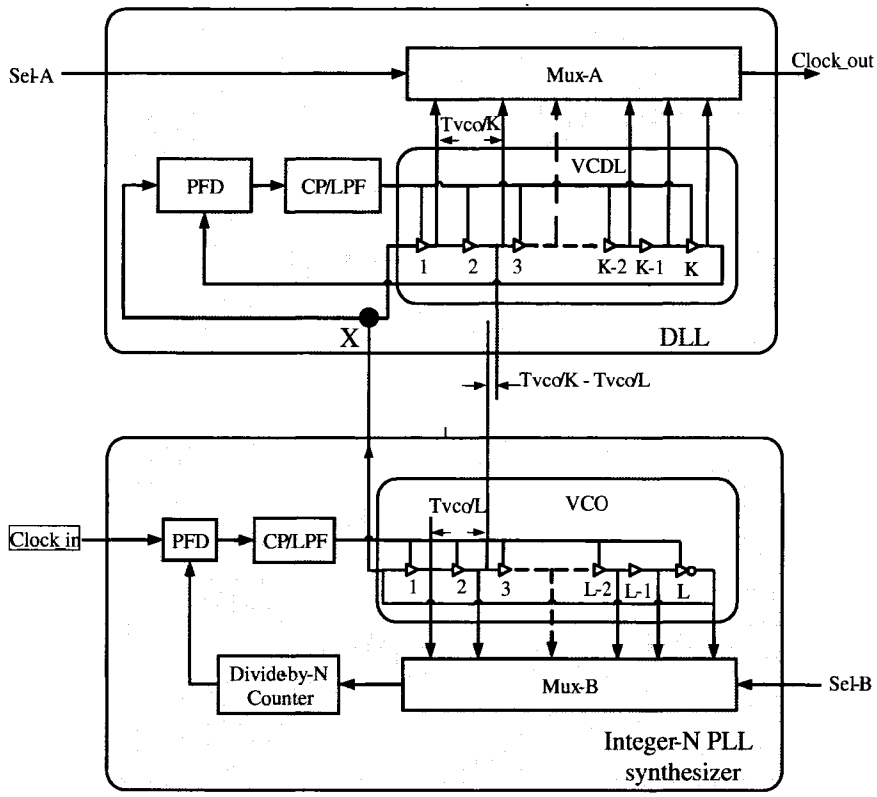

Figure 49: Employed precision timing signal generator.

the output Clock_out (Δ_y) and the input clock can be expressed as:

$$\Delta_y = M \times T_{VCO}/K \qquad where \qquad 1 \leq M \leq K \tag{22}$$

M is an integer number and depends on the selected VCDL timing signal by Mux-A. If the address of Mux-B is incremented, both the PLL and the DLL lose the phase lock because the newly selected signal is not in phase with the input clock. The PLL mechanism varies the phase of the VCO timing signals by shifting them in the time domain to reacquire the lock. When the PLL locks again, all VCO timing signals are shifted by T_{VCO}/L with respect to the input clock. Since the DLL is driven by the VCO, it is also enforced to shift its timing signals by T_{VCO}/L to maintain the lock. Therefore, the expression for Δ_y changes to $\Delta_y = T_{VCO}/L + M \times T_{VCO}/K$. However, since the VCO

and the VCDL timing signals are periodic, Δ_y in one period of the VCO can be expressed as:

$$\Delta_y = M \times T_{VCO}/K \quad for \quad 0 \leq \Delta_y \leq T_{VCO} \tag{23}$$

and

$$\Delta_y = M \times T_{VCO}/K - T_{VCO} \quad for \quad T_{VCO} \leq \Delta_y \leq 2T_{VCO} \tag{24}$$

If all VCDL and VCO signals are selected in sequence we can write

$$\Delta_y = \frac{M_1 \times T_{VCO}}{L} + \frac{M_2 \times T_{VCO}}{K} \quad for \quad 0 \leq \Delta_y \leq T_{VCO} \tag{25}$$

$$\Delta_y = \frac{M_1 \times T_{VCO}}{L} + \frac{M_2 \times T_{VCO}}{K} - T_{VCO} \quad for \quad T_{VCO} \leq \Delta_y \leq 2T_{VCO} \tag{26}$$

Where M_1 and M_2 are integer values and $1 \leq M_1 \leq L$, $1 \leq M_2 \leq K$. Thus, if the output of Mux-A is used as a sampling clock for the T/H circuit, a total number of $K * L$ samples of the input waveform over one period of the VCO can be obtained by subsampling. The coupled PLL and DLL module can provide timing signals just over one period of the VCO and thus the measurement can only be performed over a limited time interval determined by the VCO tuning range. To overcome this limitation, a new measurement method has been developed in which the input waveform is first divided into equal-size segments and then the segments are subsampled separately to obtain the overall samples of the input waveform. Input signals with fundamental frequencies varying within the tuning range of the VCO are treated as one segment while inputs with fundamentals below the VCO tuning range are considered as integer-N segments. To support this measurement method instead of a conventional PLL an integer-N PLL synthesizer is used. As a result when the PLL locks on the input clock , the VCO is forced to oscillate integer-N times faster than the input signal. Consequently, one period of the input waveform is divided into N equal segments.

2. Segment Identifier

The divide-by-N counter in the PLL synthesizer can be designed to start from one when the first segment of the input waveform is applied to the input of the T/H circuit, and advances by one in every cycle of the VCO up to N when the last segment is applied. The segment identifier module, which is a digital comparator, compares the output of the divide-by-N counter with an address supplied by an external controller (Sel-C) and whenever they are equal, generates a single pulse (Enable) that lasts for one period of the VCO. This control pulse enables the sampling clock when a particular segment is applied and disables it afterwards allowing the T/H circuit to capture the samples of the desired segment. Figure 50 indicates a simulation result in which the input waveform is divided into eight segments and three samples of the 2nd segment are obtained through the subsampling method.

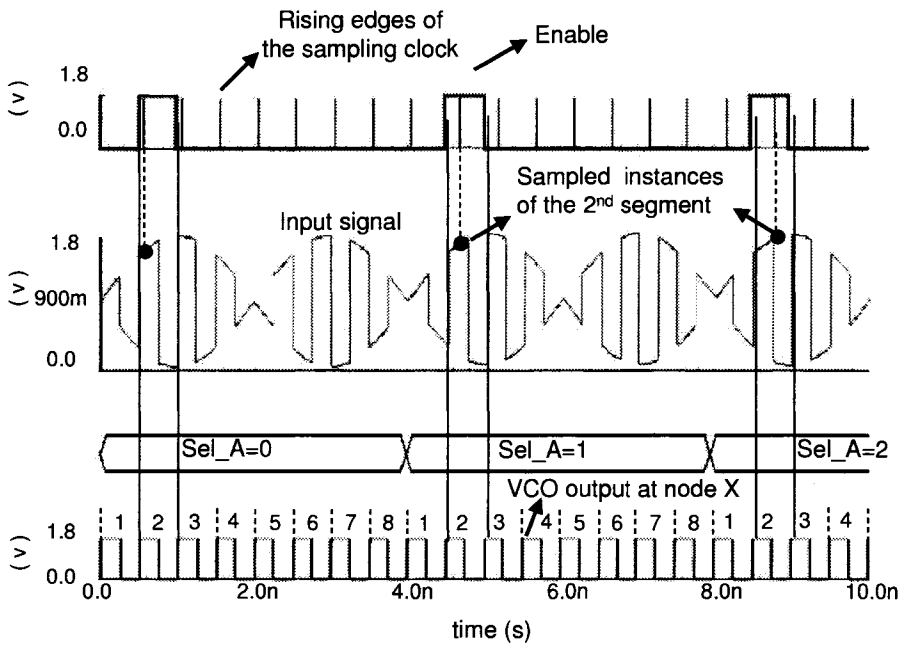

Figure 50: Input waveform chopped into eight segments and the samples of the 2nd segment taken by subsampling.

4.2.2 Track and Hold

This circuit captures the instances of the CUT's response waveform at the rising edges of the sampling clock. Although, the system level implementation of T/H circuit is straight forward, the actual implementation in CMOS environment is quite challenging. The design of the T/H circuit needs to satisfy two critical requirements. It has to have a high bandwidth to track high-speed input waveforms and it has to introduce a low pedestal error to support a high-resolution sampling. At the next chapter the design challenges of the T/H circuit is discussed and a new design for T/H circuit is proposed to overcome the problems.

4.3 Packaging Selection

Package selection is a critical decision that has to be made at the early stages of the design. The number of I/O pins, test fixture, cavity size and the speed of the circuit are among the main factors that determine the type of the package. The tester is designed to work at low speed with the outside world, however some high frequency signals are required to be routed to the package pins in order to measure the parameters of the prototype. Thus, a package with low parasitic capacitances is required. Considering the target area of 1 mm^2 a package with a cavity size greater than 1 mm^2 is required to accommodate the design. Referring to the package list supported by CMC (40-DIP, 68-PGA, 84-PGA, 24-CFP, 44-CQFP, 80-CFP, 120-CQFP, 208-PGA) 80-Pin CFP is selected and CFP80TF (printed circuit board test fixture for 80-Pin CFP) is chosen as a test fixture.

4.4 Summary

To implement the tester core top-down design methodology is followed in which modules are defined at the block level and then each part of the system is refined by designing it in more detail. Topology selection for building blocks of the tester was

covered in this chapter. In each case several possible topologies were examined and heir advantages and disadvantages were discussed. Once the a topology was determined, a mathematical model developed to describe the module and then linear models were determined for system level analysis. Matlab/Simulink tools were used to carry out system level simulations. The performance metric of the selected topologies and the effect of their parameter variations on the performance of the tester were determined through high level simulation.

CHAPTER V

PHYSICAL LEVEL DESIGN OF BUILDING BLOCKS

The tester as shown in Figure 22 constitutes various analog and digital modules. To physically implement the entire design the top-down design methodology has been followed. Each module is designed and tested separately and then building blocks containing several modules are built and finally the building blocks are connected together to realize the tester.

5.1 Analog Circuits

Physical implementation of analog circuits especially at the gigahertz range is a challenging task and in general requires several iterations to meet the design specifications. To design the analog circuits, first the topologies at the system level were determined and then schematic and layout of the circuits were implemented using Cadence design tools. The operation of the circuits were verified using both spectreRF and Hspice simulators.

5.1.1 Phase Locked Loop

A charge pump PLL is utilized to implement the carrier signal generator. Delay cells are used as building blocks of the VCO module in the PLL. Therefore, first the design of the delay cells is covered and then the VCO design is discussed.

5.1.1.1 *Delay Cell*

The performance metric of the delay cells has a major effect on the accuracy of the measurement scheme. Thus, its circuit topology has to be carefully selected to reduce the level of noise introduced by delay cell nonlinearity. There are a wide range of delay cells [60]- [64] for different applications in the literature. Conventional single-ended delay cells [60] provide low intrinsic device noise and high Signal-to-Noise Ratio (SNR) mainly due to their full voltage swing, however they suffer from a poor Power Supply Rejection Ratio (PSRR). As a result any oscillator built based on this type of delay cell introduces a considerable jitter. The dominant source of timing jitter is the switching noise originated in the digital portion of mixed-signal systems. Differential delay cells are less sensitive to the supply voltage fluctuations due to differential operations and thus they are more suitable for low jitter applications. Based on the design objectives a cross-coupled differential delay cell presented in Figure 51 is selected and the design goals for the delay cell were defined as follows. For a ring oscillator to oscillate, the loop gain has to be higher than one. However, to guarantee the oscillation in the presence of process and temperature variations as shown in Table 2 the desired gain of each the delay cell is chosen to be higher than two.

Table 2: Delay Cell Design Goals

Parameter	Value
Output Voltage Level	Digital
Gain	>2
Delay Range	50 ps - 100 ps
Control Voltage	0 - 1.8 V

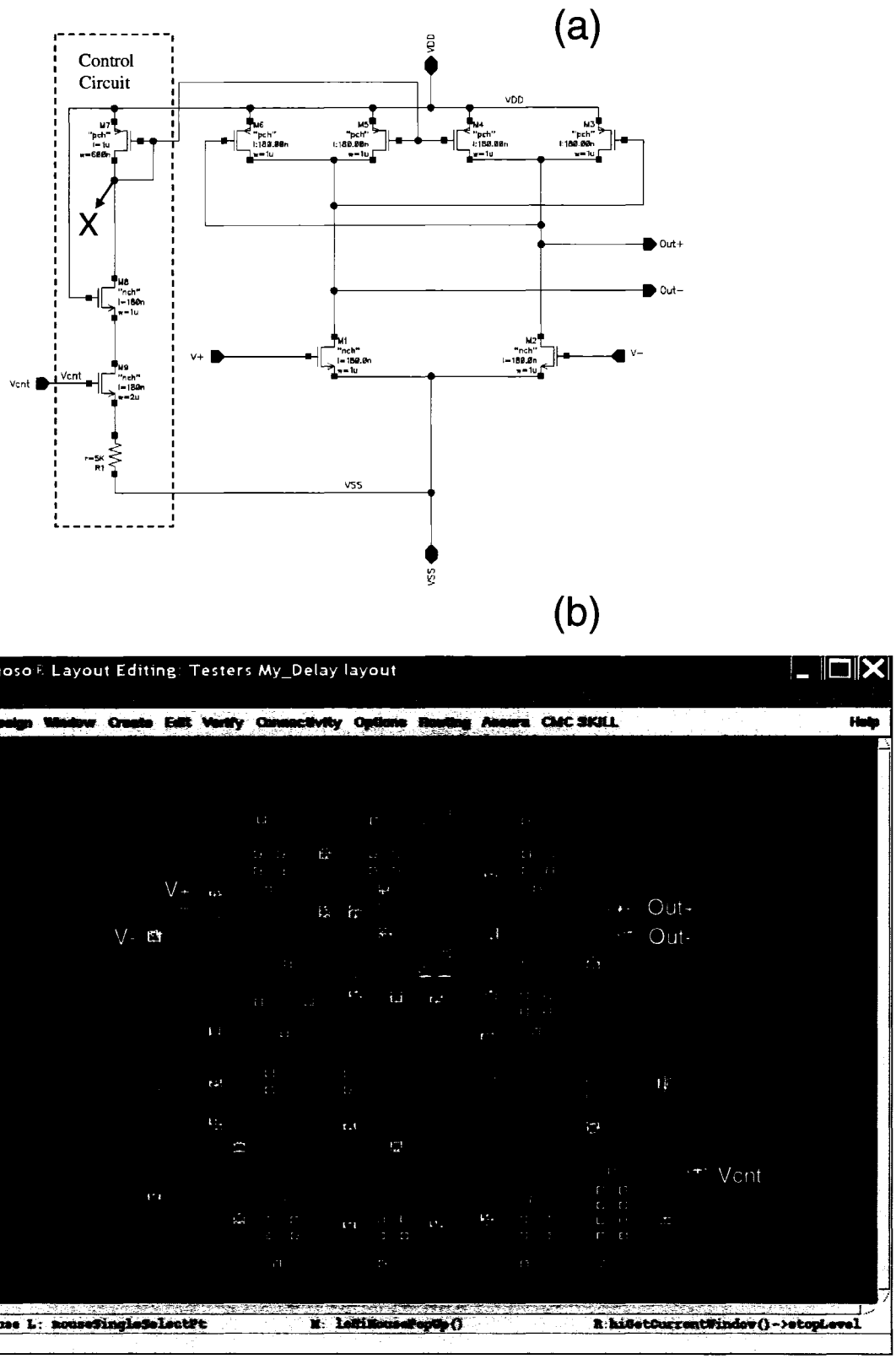

Figure 51: The employed cross-coupled differential delay cell. (a) schematic diagram. (b) layout.

In general, delay in integrated circuits can be modeled by a series resistor-capacitor circuit. The delay is controlled by changing either the value of the resistor or the capacitor. In Figure 51 the delay is controlled by resistance of M4 and M5. The cross-coupled transistors, M3 and M6, guarantee the differential operation while eliminating the need for a conventional tail bias current commonly used in differential designs. Moreover, the cross-coupled transistors sharpen the edges at the output and give less chance to the power supply noise to be converted to jitter. The output swings rail-to-rail and generates digital voltage levels without requiring a level shifter. M1 and M2 are differential pairs operating either in cut-off or deep triode regions. The delay range can be determined based on the test frequency range of (100MHz-2.5GHz) outlined in the design objectives, the number of required timing signals and the desired VCO gain. The maximum test frequency is 25 times higher than the minimum frequency. Designing an oscillator with such a wide tuning range is difficult in practice. It requires a considerable number of delay cells to cover a significant delay range. While for a practical implementation, the difference between the maximum and the minimum delay values should not be more than a few times. To overcome this problem, we can use a delay cell with a reasonable delay range to support just the high portion of the test frequency band and then expanded the range by connecting the VCO output to a digital divide by N counter and using its outputs to support lower frequency bands. This approach can easily be adopted since the employed delay cell provides digital level signals. The delay cell in Figure 51 includes two sub-circuits, the control circuit that comprises M7, M8, M9 and R1 and the pseudo-differential circuit that includes the rest of the delay cell.

The control voltage is applied to the gate terminal of M9 to change the reference current flowing through M7. As a result the current injected by M4 and M5 into the pseudo-differential circuit is varied and the speed of transition at the output node

changes. In the design of the control circuit several factors have been taken into consideration. First the reference current is adjusted to change as a linear function of the control voltage to lower the effect of the jitter. Moreover to support the VCO tuning range and the PLL stability requirement, the control circuit is designed to provide a high voltage gain.

The reference current flowing through M7 can be limited either by the amount of R1 resistor or the output resistance of M7. Limiting the current by R1 requires a large resistor and results in a considerable area overhead. Thus, in the proposed design, the reference current is controlled by the aspect ratio of M7. To estimate the upper limit for the drain current of M7, we assumed M8 and M9 are is deep triode region and the voltage across R1 is negligible these assumptions were later checked and validated. Based on the transistor parameters in CMOS 0.18 μm technology specified as: $\mu_p C_{ox} = 17.7\ \mu A/V^2$ and $V_{th} = 0.35\ V$, for a maximum reference current of 20 μA we can write:

$$I_D = \mu_p C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 \tag{27}$$

$$20 \times 10^{-6} = 17.7 \times 10^{-6} \frac{W}{L}(1.8 - 0.35)^2$$

$$\frac{W}{L} = 0.56$$

Since there are two variables and one equation, one of the variables can be arbitrarily selected. The aspect ration is rounded up to $\frac{W}{L} = 0.6$ and the length of 1-μm is chosen for M7 in order to minimize the short channel effect. The width from the aspect ratio of 0.6 is $W = 600\ nm$. R1 has a positive effect on the linearity of the scheme however due to area overhead $R1 = 5\ K$ is chosen. It is desirable for the control circuit to have a low frequency AC response in order to reduce the effect of noise and ripple on the control line. This goal is partially achieved by choosing proper width and length for M8 and M9. However, since the maximum and minimum amount of delay introduced

by the delay cell is affected by M8 and M9, the sizes of these transistors have been determined through simulation after a few iterations.

Figure 52 shows the simulation result of DC analysis for the control circuit using Spectres circuit simulator. It can be seen that the reference current starts growing at $V_{cnt} = 0.3\ V$ and reaches to the maximum value of 22.4 μA at $V_{cnt} = 0.8\ V$. It is also can be observed that M9 enters to the triode region when V_{cnt} exceeds 0.7 V. The circuit exhibits a good linearity for $4.2\ V < V_{cnt} < 6.9\ V$. The minimum amount of

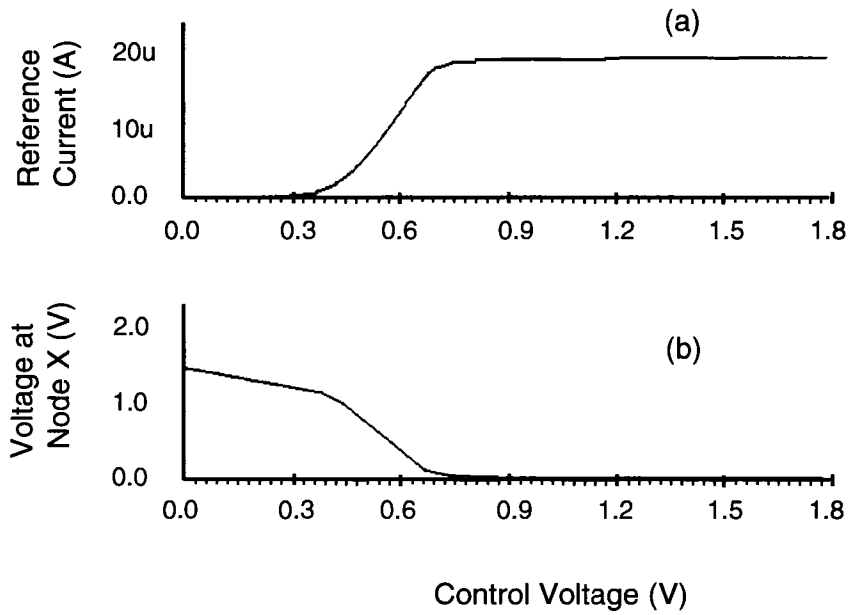

Figure 52: Simulation result of DC analysis performed on the control circuit.

delay occurs when the maximum amount of current is injected by M4 and M5 since the total capacitance at the output node is charged faster. Assuming ideal current mirrors and equal size M4 and M5, the drain current of M4 and M5 is determined by:

$$I_{D4} = I_{D5} = I_{D7} \times \frac{W_4/L_4}{0.6} \tag{28}$$

The voltage at positive output node (out+) is defined by: $V_{out+}C_{eq} = (I_{D4} + I_{D3})T$ where C_{eq} is the total amount of capacitance seen at each output node of the differential delay cell and T is the amount of the delay. Limiting the maximum amount of

switching current of M3 and M6 to less than 200 μA, the sizes of M3 and M6 can be determined from (27) as

$$200 \times 10^{-6} = 17.7 \times 10^{-6} \frac{W_3}{L_3}(1.8 - 0.35)^2$$

$$\frac{W_3}{L_3} = 5.37$$

In the design $W = 1\ \mu m$ and $L = 0.18\ \mu m$ have been chosen for both M3 and M6. Assuming the voltage level of $0.5V_{DD}$ as a reference to calculate the delay introduced by the cell, the minimum and maximum delay can be approximated by:

$$T_{min} = \frac{0.5V_{DD} \times C_{eq}}{(I_{D4-max} + I_{D3})} \qquad (29)$$

$$T_{max} = \frac{0.5V_{DD} \times C_{eq}}{(I_{D4-min} + I_{D3})}$$

Where C_{eq} denotes the total amount of capacitance seen at the output node.

The current flowing through M4 has to be high enough to change the total current of $(I_{D4-max} + I_{D3})$ significantly in order to have a tangible effect on the cell delay. On the other side it has to be as low as possible to limit the power consumption. A maximum amount of $I_{D3} = 200\ \mu A$ is reasonable and meets the design requirements. For $I_{D4} = 200\ \mu A$, from equation 28 the aspect ratio of M4 is determined to be $\frac{W_4}{L4} = 5$. For consistency with M3, the length and width of M4 and M5 are chosen to be 0.18 μm and 1.0 μm respectively.

The delay cells are designed to support just the upper band of the desired test frequency range (1.0 GHz-2.5 GHz) due to implementation problems arising from a wide tuning range. To cover the desired frequency band the period of the VCO has to be able to vary from 400 ps to 1.0 ns. Thus, if ten delay elements are implemented to construct the VCO, each delay element has to support a delay range of 40 ps to 100 ps.

From equation (29) for a minimum delay of 40 ps the estimated amount of C_{eq} is equal to 8.6 fF. This amount can be achieved if M1 and M2 are properly sized. The

size of M1 and M2 can be determined via simulation to meet the expected amount of delay. The width of 1.0 μm and the length of 0.18 μm, which satisfy the design requirements, are chosen for M1 and M2. The simulation result shown in Figure 53 indicates the transient response of the delay cell for both the minimum and the maximum amount of control voltage. It can be seen that the delay introduced by each delay element covers the span of 36 $ps < T_d < 91$ ps. The main characteristic of the

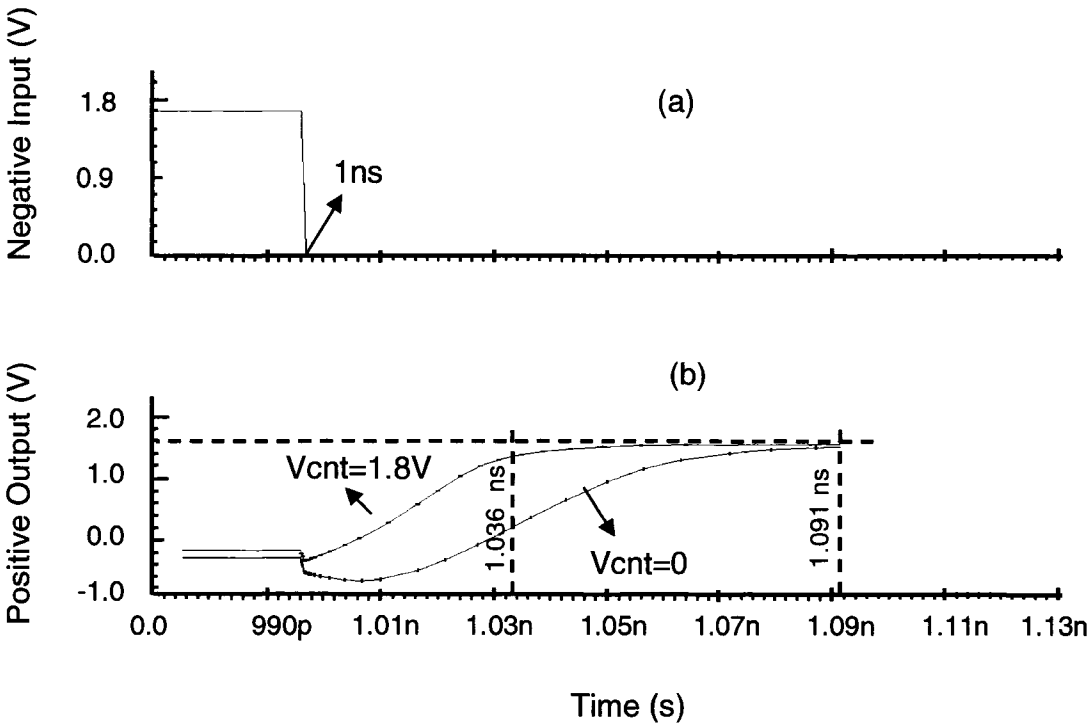

Figure 53: The AC response of the delay cell. (a) applied input signal. (b) output response for Vcnt=0 and Vcnt=1.8 V

delay cell that shows the amount of the delay versus the applied control voltage is shown in Figure 54. It can be observed that the designed delay cell presents a good linearity as control voltage is swept from 0.34 V to 0.68 V. The simulation results shown in Table 3 indicate that the design goals for the delay cell are met.

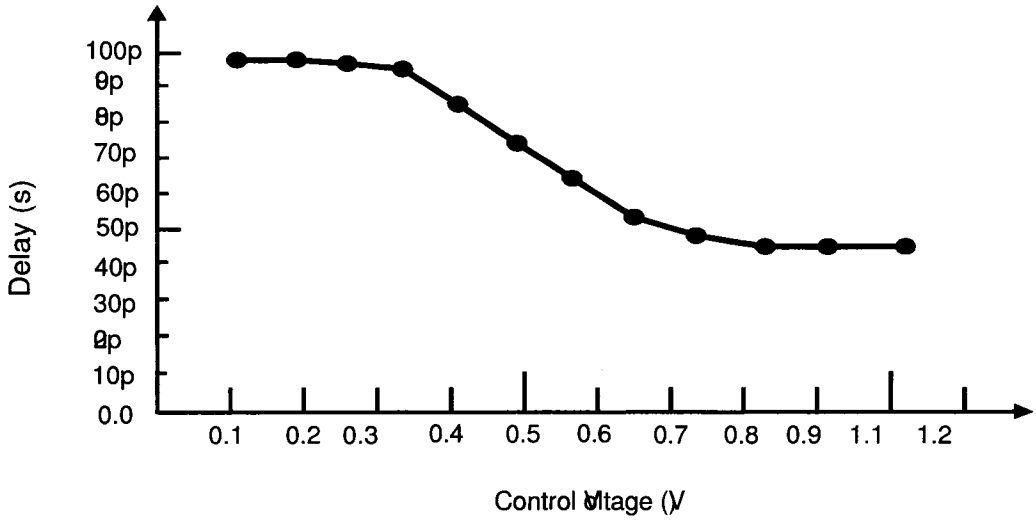

Figure 54: Delay characteristic of the employed delay cell.

Table 3: Delay Cell Design Goals and Simulation Results

Parameter	Design Goals	Simulation Results
Output Voltage Level	Digital	0.05 V - 1.8 V
Gain	>2	10
Delay	50 ps - 100 ps	43 ps -100 ps
Control Voltage	0 - 1.8 V	0 - 1.8V

5.1.1.2 Voltage Controlled Oscillator

A circuit represented by a negative feedback system (Figure 55) may oscillate if the following two conditions knows as "Berkhausen criteria" are satisfied.

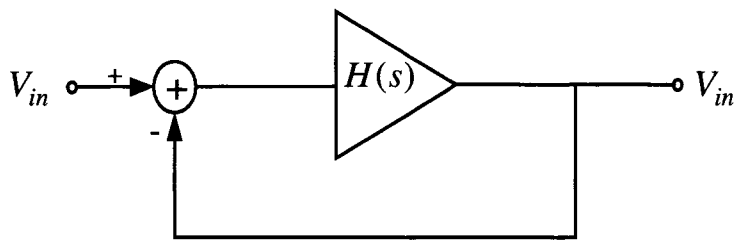

Figure 55: Linear model of oscillator circuits.

$$|H(j\omega_0)| \geq 0 \tag{30}$$
$$\angle H(j\omega_0 = 180^o$$

For a circuit to oscillate these conditions are necessary but not sufficient. The employed VCO is a ring oscillator that constitutes five cross-coupled differential delay cells. The tuning range of a ring oscillator, in general, is determined based on the number of delay elements and the amount of delay presented by each delay element. The employed delay cells as shown in Figure 53 support a delay range of $36\ ps < T_d < 91\ ps$. To generate the desired maximum frequency of 2.5 GHz, ten delay elements or five differential delay cells can be employed to build the VCO.

Denoting the transfer function of each delay element by $-A_0/(1 + s/\omega_0)$ for a VCO containing ten delay elements the open loop transfer function is given by:

$$H(s) = -\frac{A_0^{10}}{(1 + \frac{s}{\omega_0})^{10}} \tag{31}$$

For the circuit to oscillate the total phase shift has to be equal to 180° at the crossover frequency. Thus each delay element has to contribute $\frac{180°}{10} = 18°$. The oscillation

frequency is given by:

$$tan^{-1} = \frac{\omega_{osc}}{\omega_0} = 18^\circ \tag{32}$$

$$\omega_{osc} = 0.32\ \omega_0 \tag{33}$$

The minimum voltage gain per stage has to satisfy the gain requirement and thus

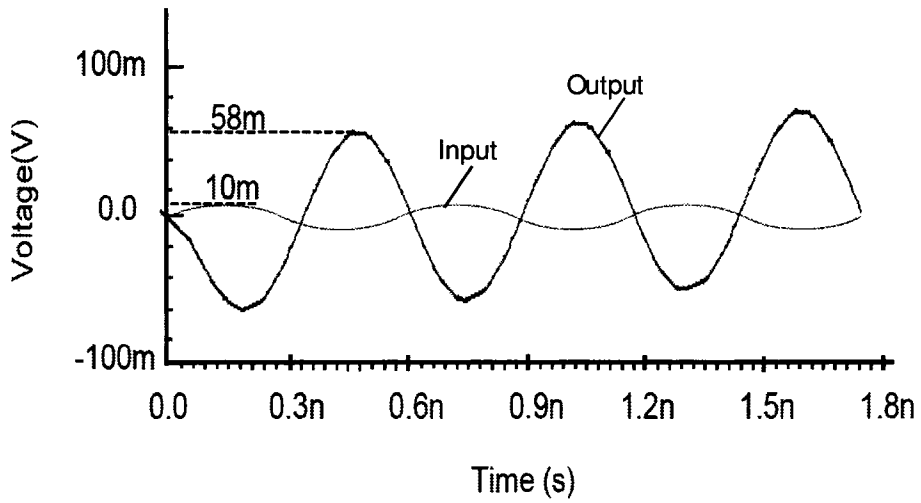

Figure 56: Simulation result from transient analysis of the delay cell.

the magnitude of the loop gain at ω_{osc} must be equal to unity.

$$\frac{A_0^{10}}{(\sqrt{1+(\frac{\omega_{osc}}{\omega_0})^2})^{10}} = 1 \tag{34}$$

and hence:

$$A_0 = \sqrt{1+0.32^2} \approx 1.05 \tag{35}$$

The transient analysis of the delay cell shown in Figure 56 indicates that the gain of each delay element is greater than five and thus the gain requirement for oscillation is satisfied. Figure 57 shows a feedback circuit containing 10 delay elements. This circuit does not oscillate due to the signal inversion through each stage resulting in a positive feedback near zero frequency. The circuit latches-up rather than oscillates. To solve

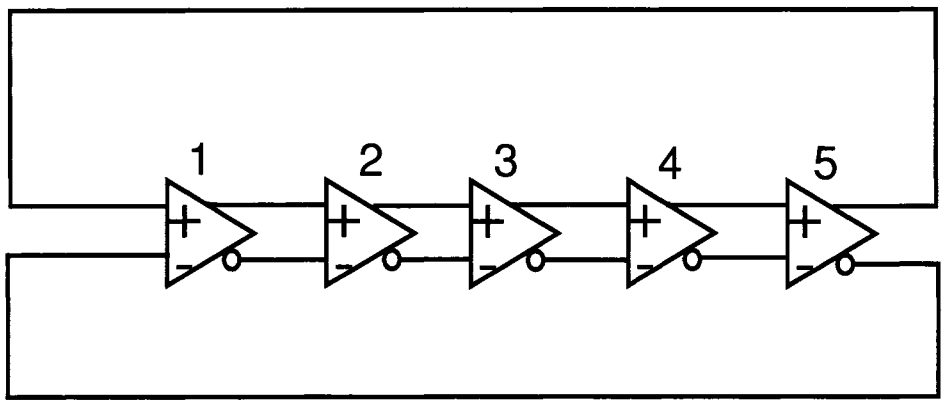

Figure 57: Ten delay elements employed to build a ring oscillator.

this problem, as shown in Figure 58(a), the interconnects between the outputs and the inputs of one delay cell are cross coupled to provide a negative feedback near zero. The physical implementation of the VCO is indicated in Figure 58(b). Post layout simulation using Spectre simulator as indicted in Figure 58(c) shows a tuning range of 1.1 GHz-2.8 GHz. The VCO gain, from Figure 58(c), for input range of $0.36\ V < V_{cnt} < 0.68\ V$ is equal to: 5.6 GHz/V.

The simulation results shown in Table 4 indicate that the VCO design goals are met.

Table 4: Voltage Controlled Oscillator Design Goals and Simulation Results

Parameter	Design Goals	Simulation Results
Output Voltage Level	Digital	0.05 V - 1.8 V
Gain	5.0 GHz/V	5.9 GHz/V
Tuning Range	1.2GHz-2.5GHz	1.1 GHz - 2.8 GHz

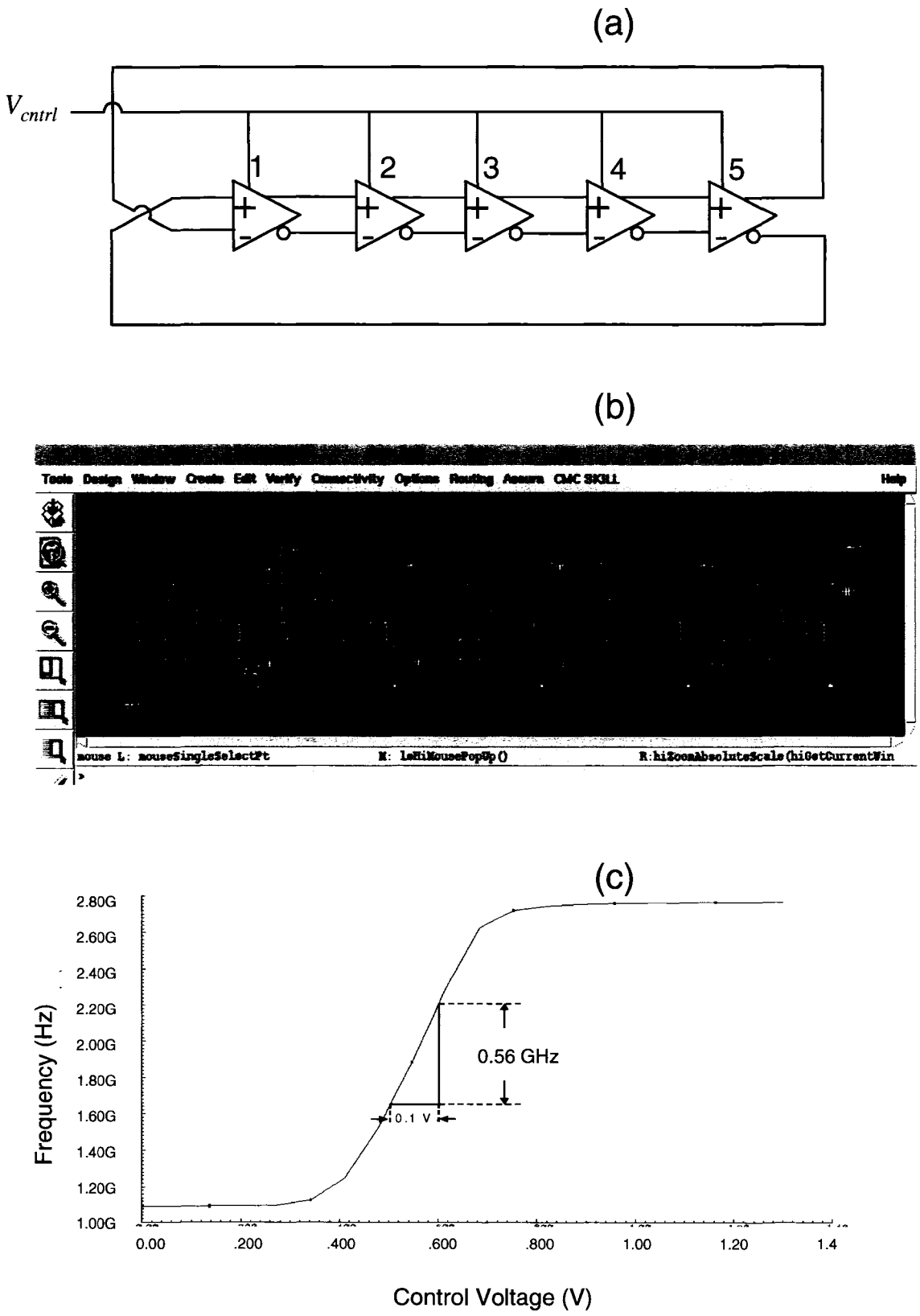

Figure 58: Implemented voltage controlled oscillator. (a) block diagram. (b) physical implementation. (c) post layout tuning range simulation.

5.1.1.3 *Phase and Frequency Detector*

The system level design of the PFD presented in Figure 30 can be implemented at the circuit level using digital cells from CMOS 0.18 μm library. Figure 59 shows the schematic diagram of the PFD using standard library cells which operates as follows: A reference clock (R-IN) is applied to the circuit and compared with a feedback signal

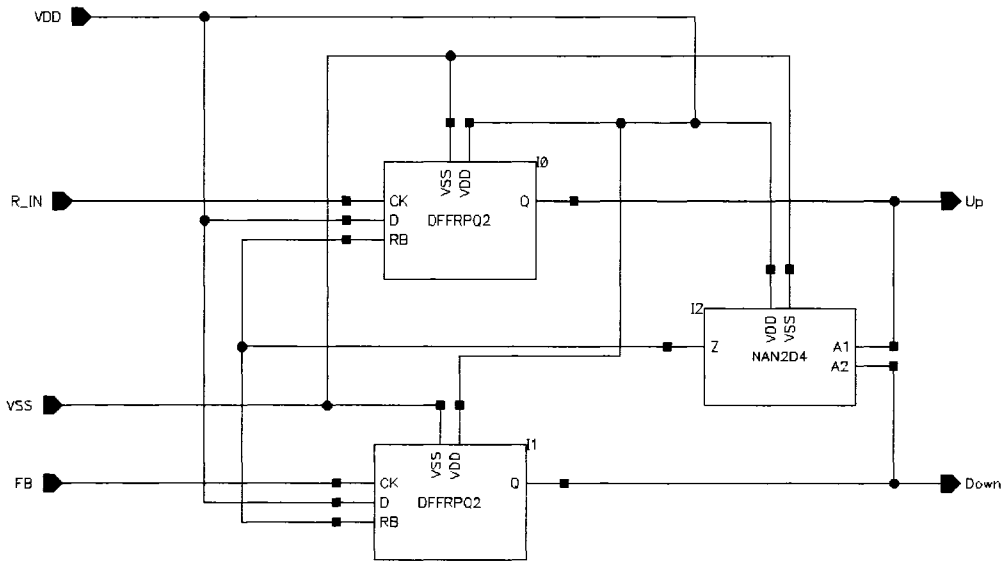

Figure 59: PFD implementation using CMOS 0.18 μm standard library cells.

(FB). Based on their frequency or phase difference, error pulses on either Up or Down outputs are generated.

5.1.1.4 Charge Pump

Circuit level implementation of the charge pump is quite critical due to various factors that may undermine the proper operation of the circuit. Figure 60 shows the implementation of a basic charge pump using CMOS transistors. The edges of Up

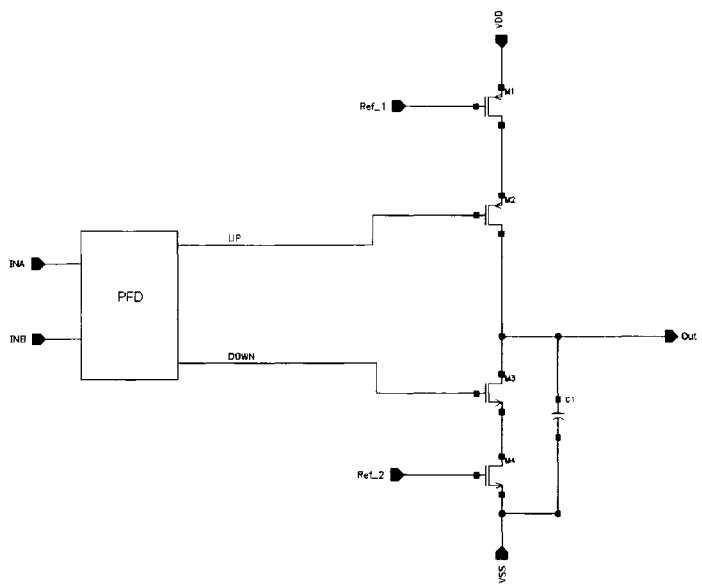

Figure 60: Basic charge pump.

and Down signals in this scheme have to be precisely aligned since any time difference between them introduces noise on the control voltage (Figure 61). The other issue is the mismatch between the current injected and drawn through current sources which eventually turn into a phase error between the reference clock and the feedback signal. Moreover, the charge distribution between the main capacitance (C_1) and the parasitic capacitances produces noise at the output.

Figure 62 shows the employed charge pump in which the edges of Up and Down signals have been aligned through proper sizing of M7-M12 transistors. The currents passing through M1 and M4 have also been carefully adjusted to minimize the effect of mismatch. The charge distribution is handled through a relatively large output

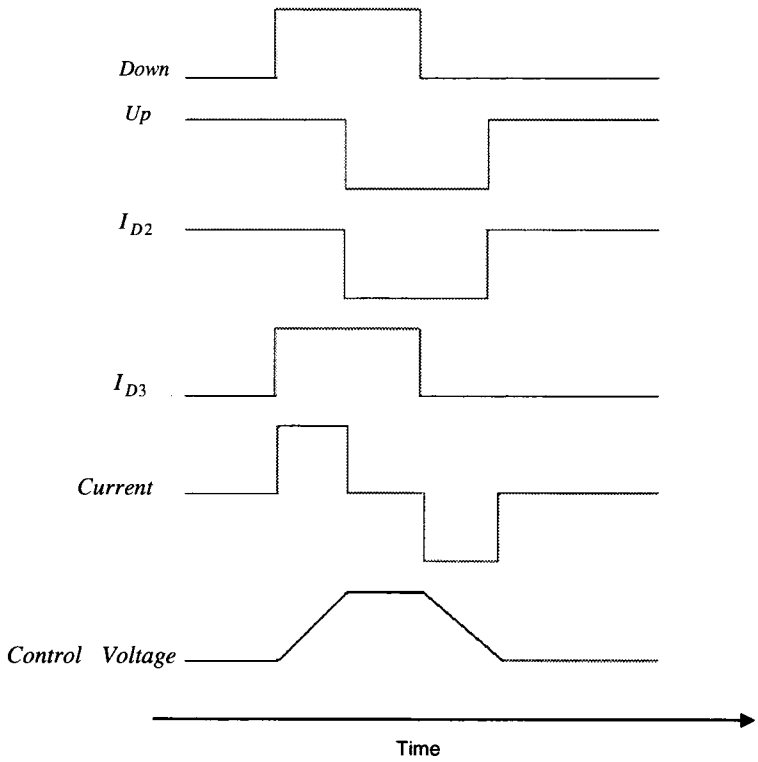

Figure 61: Skew effect on control voltage.

capacitance ($C_1 = 3\ pF$) in series with $R_1 = 5\ K$. A small capacitor ($C_2 = 200\ fF$) has also been added to the output to suppress the spikes on the control voltage.

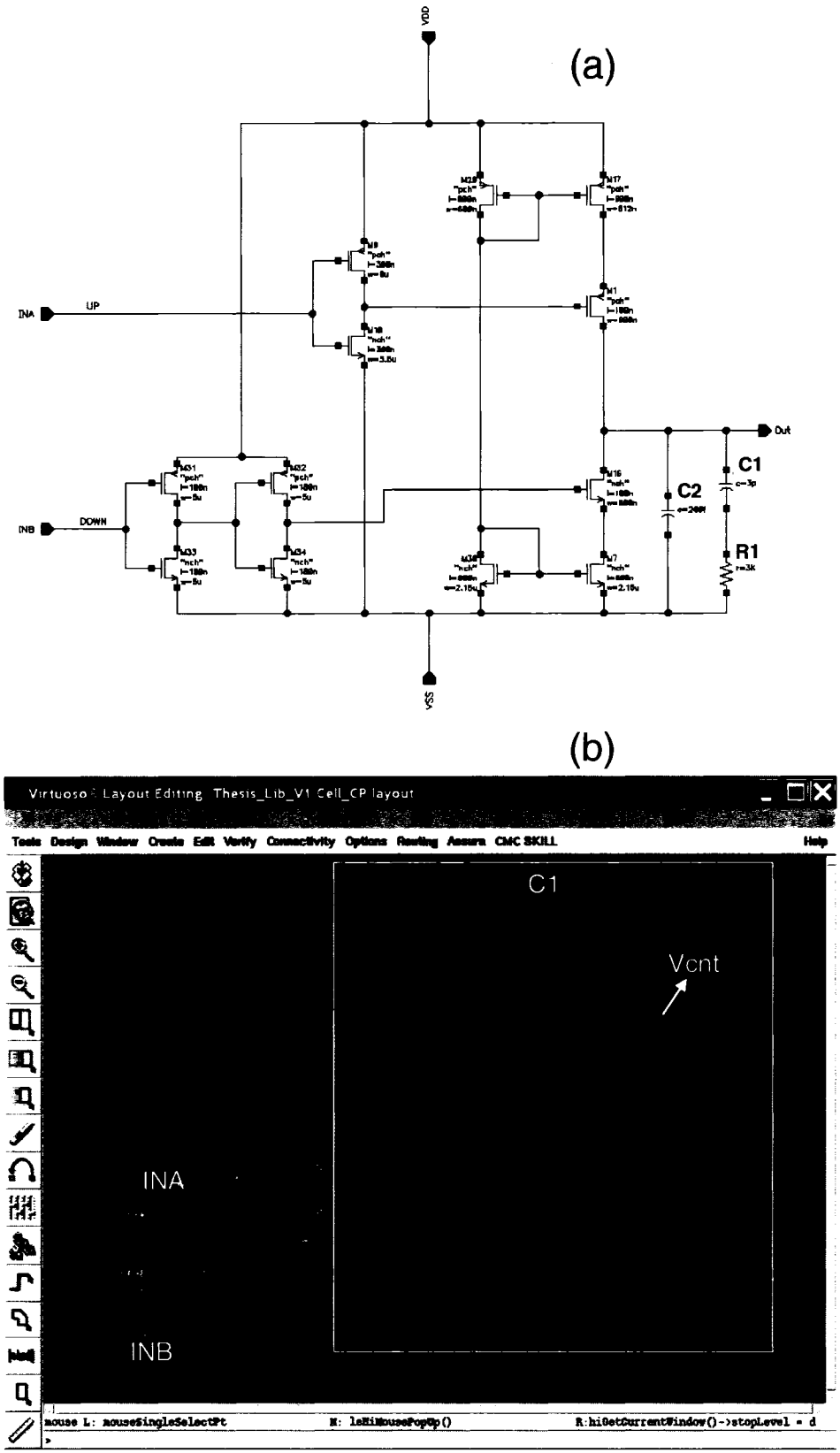

Figure 62: Implemented charge pump (a) schematic diagram. (b) layout.

The current supplied or drawn by charge pump for $0.32\ V < V_{cnt} < 0.8\ V$ is set to be 22 μA to support the PLL stability requirement. Adding C_2 to the output of the charge pump introduces a zero in the overall PLL transfer function. This modification introduces a third order PLL system and changes the stability criteria. In our design, C_2 is chosen to be less than 10% of C_1 to minimize the effect of C_2 on the PLL closed loop frequency response. To verify the specifications of the designed charge pump a test has been conducted to determine the CP gain. Figure 63 shows a test setup in which the PFD is driven by two signals of equal frequency but different phase. The input signals are later switched to obtain the CP response for both positive and

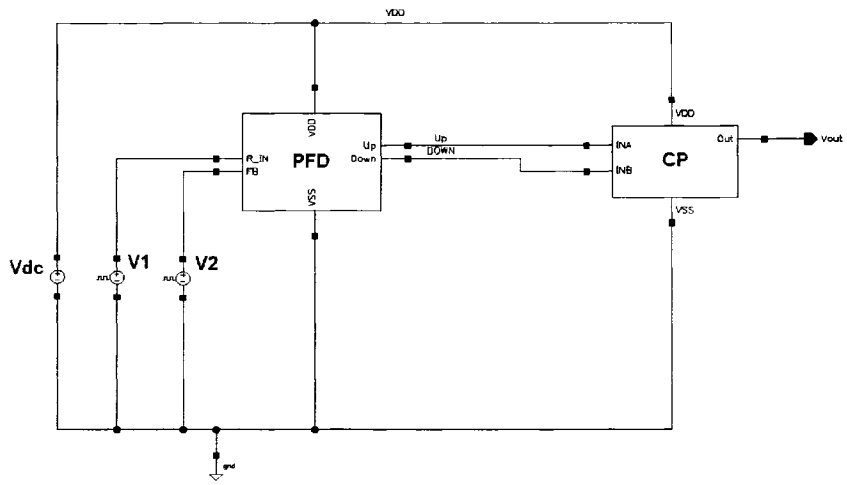

Figure 63: Test setup for the charge pump gain measurement.

negative phase difference. Figure 64 shows the Up, Down pulses and the CP output signal for a positive phase difference. It can be observed that the slope of output from Figure 64(a) is equal to 2.6×10^3. When the input signals are switched from Figure 64(b) the slope of the output is equal to -2.7×10^3 indicating that the positive and negative currents of the CP are properly equalized.

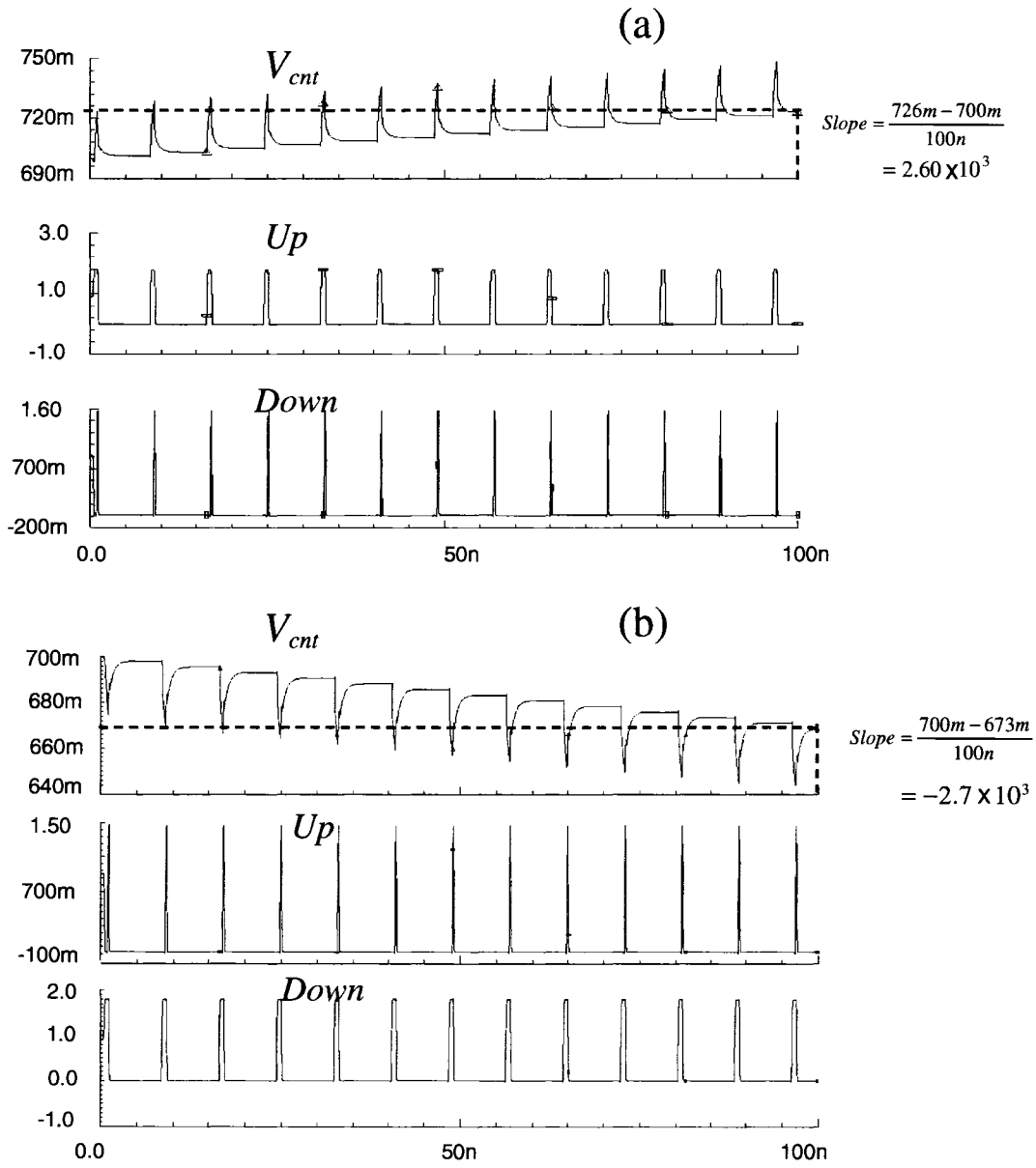

Figure 64: Charge pump response for (a) inputs with positive phase difference. (b) the same inputs but switched to present negative phase difference.

Once all three main modules of the PLL were designed the PLL was built and tested (Figure 65). A digital signal with frequency of 1.25 GHz has been applied to the

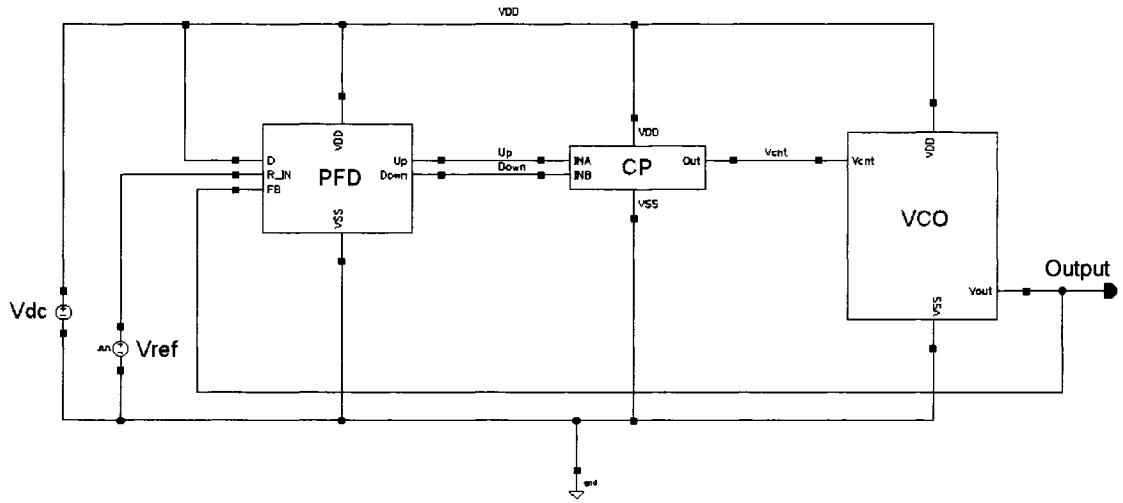

Figure 65: The PLL test setup.

PFD module. Figure 66 shows that it takes 160 ns for the loop to settles down and acquire the lock. The input and output signals at the locked condition are shown in Figure 67.

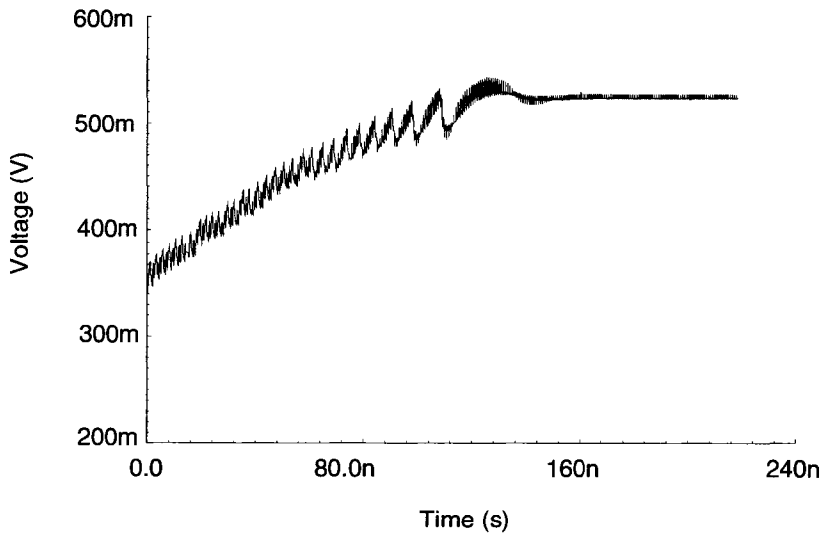

Figure 66: The PLL control voltage during lock acquisition.

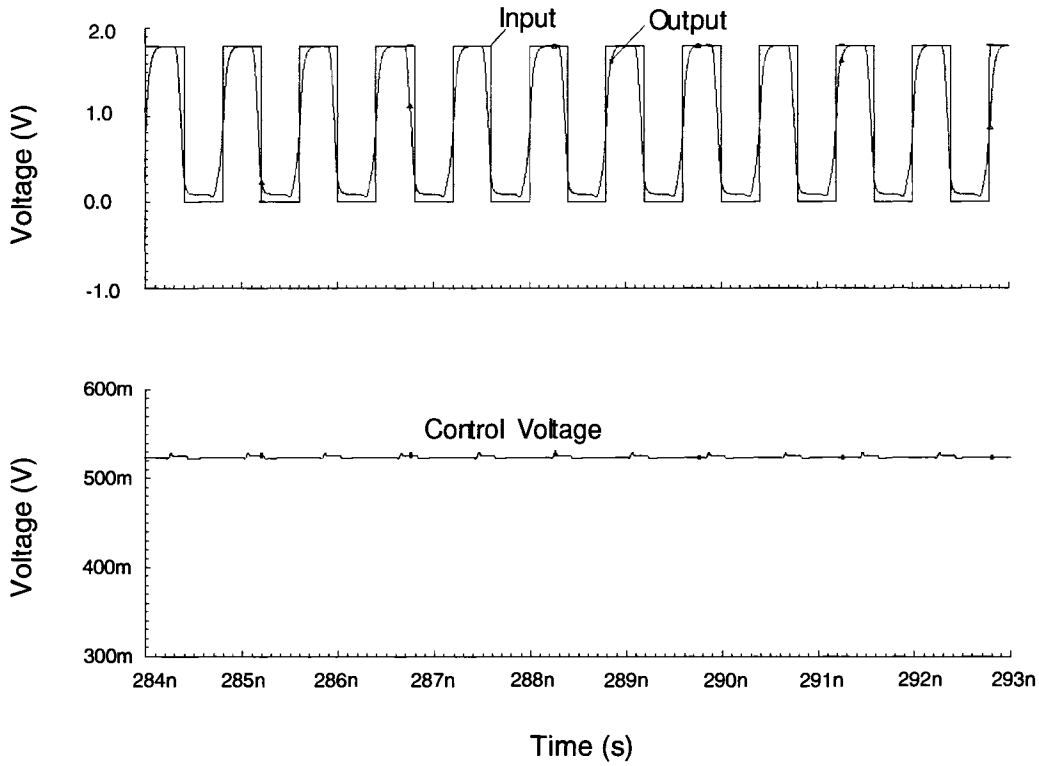

Figure 67: Input, output and control voltage of the PLL at the locked condition.

5.1.2 Delay Locked Loop

The transfer function of standard DLL represents a first order system and thus it is always stable. Using a second order charge pump similar to the one developed for the PLL yields a second order system and may result in unstable closed-loop. Figure 68 shows a DLL with a second order charge pump. The open loop transfer function of the scheme presented in Figure 68 is given by:

$$\frac{V_{cnt}}{\Delta\phi} = \frac{I_P}{2\pi}[\frac{1}{C_2 s} \| (R_1 + \frac{1}{C_1 s})] \tag{36}$$

Where I_p represents the current supplied by the CP module.

The closed loop transfer function is equal to:

$$\frac{\phi_{out}}{\Delta\phi_{in\,s}} = \frac{\frac{I_P K_{VCDL}}{2\pi}(R_1 C_1 s + 1)}{R_1 C_1 C_2 s^2 + [C_1 + C_2 + I_P K_{VCDL} R_1 C_1/(2\pi)]s + I_P K_{VCDL}/(2\pi)} \tag{37}$$

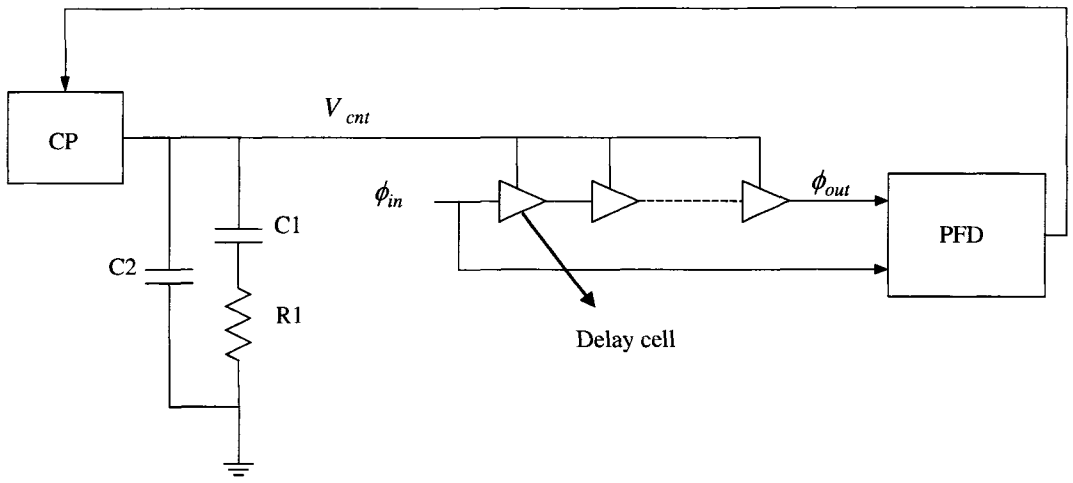

Figure 68: DLL with a second order closed loop transfer function.

In practice, R_1 can be removed since the open loop transfer function, as can be seen from equation (36), contains just one pole at the origin. Alternatively C_2 can be chosen to be less than one-fifth of C_1 to satisfy the closed loop stability requirement.

The DLL in the proposed tester is designed using the same building blocks used for the PLL design. The only difference is the use of VCDL instead of VCO. Figure 69 shows how the designed delay cells were configured as a VCDL. Total number of eleven delay elements from six differential delay cells was employed to build the VCDL. The number of delay elements in the VCO and VCDL are selected to be 10 and 11 which are mutually prime numbers to guarantee unique sampling points.

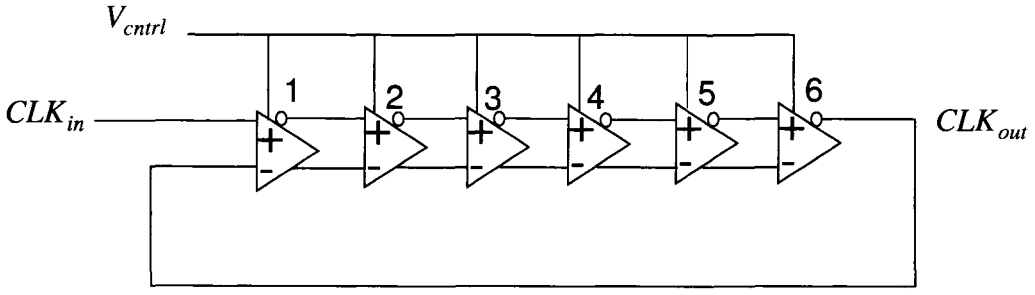

Figure 69: Differential delay cells configured as a voltage controlled delay line.

Since the DLL includes eleven delay elements its delay range (T_d) id given by $11 * T_{min} < T_d < 11 * T_{max}$ where T_{min} and T_{max} are the minimum and the maximum amount of delay supported by each delay element. From the simulation results presented in Figure 53, $T_{min} = 36\ ps$ and $T_{max} = 91\ ps$ and therefore $396\ ps < T_d < 1.001\ n$. In other word the DLL theoretically can lock on input signal with tuning range of $999\ MHz < f_{in} < 2.5\ GHz$. Simulation results presented in Figure 70 indicates how the lock is acquired by the DLL. It can be observed that the control voltage grows rapidly when the phase difference between the input and output is high. When the phase difference decreases the control voltage changes slowly until the loop settles down and the lock is achieved.

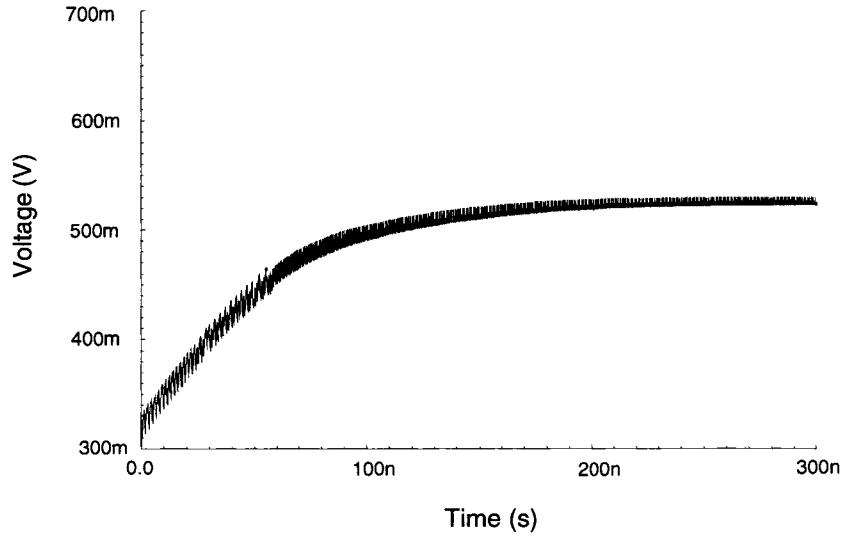

Figure 70: Control voltage variation of the DLL indicating how the lock is acquired.

Due to the fact that the sampling clock jitter plays a very important rule in the measurement accuracy of the designed test scheme. Extensive simulations have been performed in various frequencies using both Spectres and Hspice to ensure the performance of the sampling clock generator. Figure 71 shows the eye diagram of the sampling clock supplied by the coupled PLL and DLL module at 1.1 GHz before and after achieving the phase lock. The rising edges of the sampling clock shown in

Figure 72, indicate the reduction of jitter levels from 28 ps to 2.5 ps peak-to-peak once the lock is acquired.

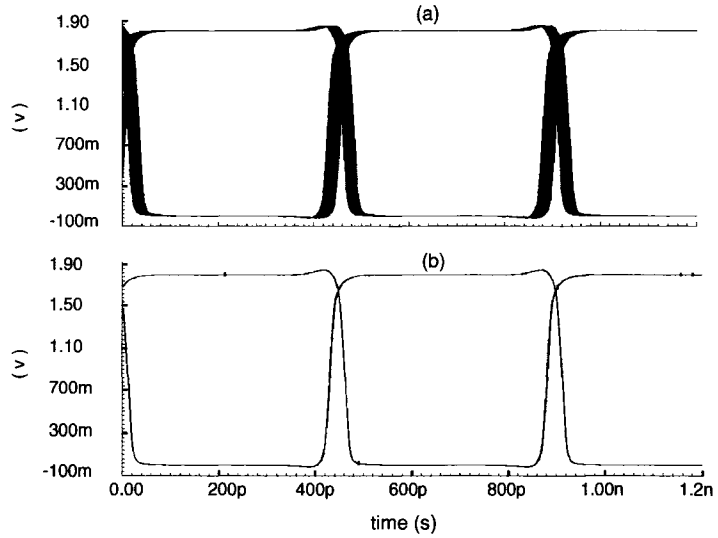

Figure 71: Simulated eye diagram for the sampling clock of 1.1 GHz. (a) before attaining the phase lock. (b) after attaining the phase lock.

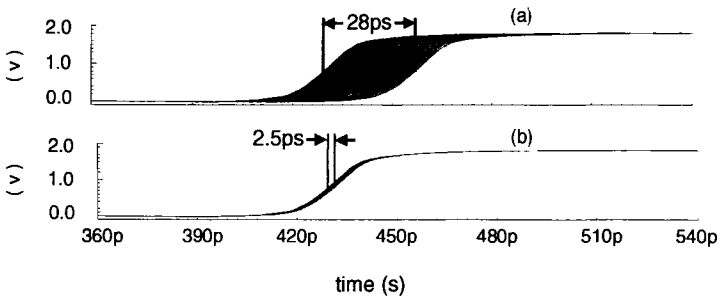

Figure 72: Peak-to-peak jitter of the sampling clock at 1.1 GHz. (a) before attaining the phase lock. (b) after attaining the phase lock.

5.1.3 Mixer

The design of the mixer is simplified as: (a) The carrier is a square waveform and (b) The mixer's conversion gain is not a critical design parameter. Thus, instead of an active mixer a double-balanced passive mixer has been designed. Figure 73 shows the schematic diagrams of the employed mixer. It includes two CMOS switches each

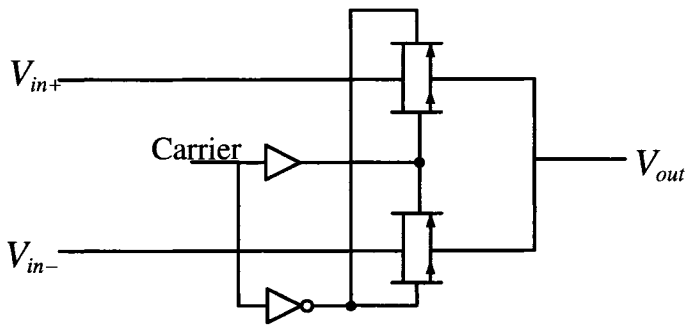

Figure 73: Schematic level implementation of the mixer.

containing a pair of complementary P and N transistors. The operation is quite simple, the switches turn on and off with the speed of the carrier to chop the input signal. Two critical design issues were taken into consideration to lower the error introduced by the mixer, first the rising and the falling edges of the signals applied to the gate terminals of P and N transistors were accurately aligned to simultaneously turn on and off each pair of transistors. Second, the on-resistance of the switches was minimized and kept constant over the input voltage range by using high aspect ratio transistors. Figure 74 shows the simulated DC characteristic of the employed CMOS switch terminated by a 50 Ω resistor. The scheme presents a significant linearity over the input range of $0 - 0.5\ V$. The simulation results performed on the mixer show an excellent frequency response and confirm that the conversion gain remains unchanged up to 10.0 GHz (Figure 75). The conversion gain however, varies slightly with the amplitude of the input signal. Figure 76 shows the mixer's voltage conversion gain

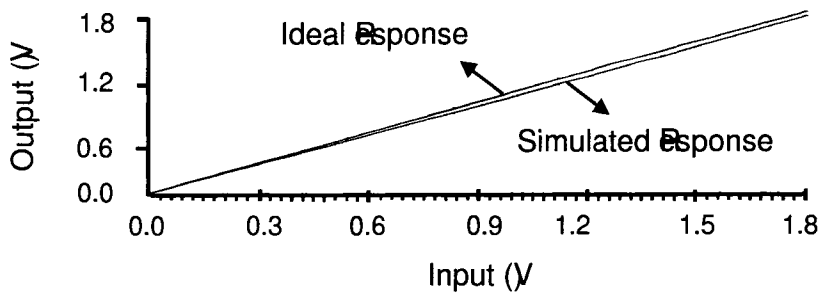

Figure 74: Simulated DC characteristic of the employed CMOS switches for mixer realization.

versus the input voltage amplitude. It can be observed that the conversion gain varies less than one percent for inputs up to 0.5 V amplitude.

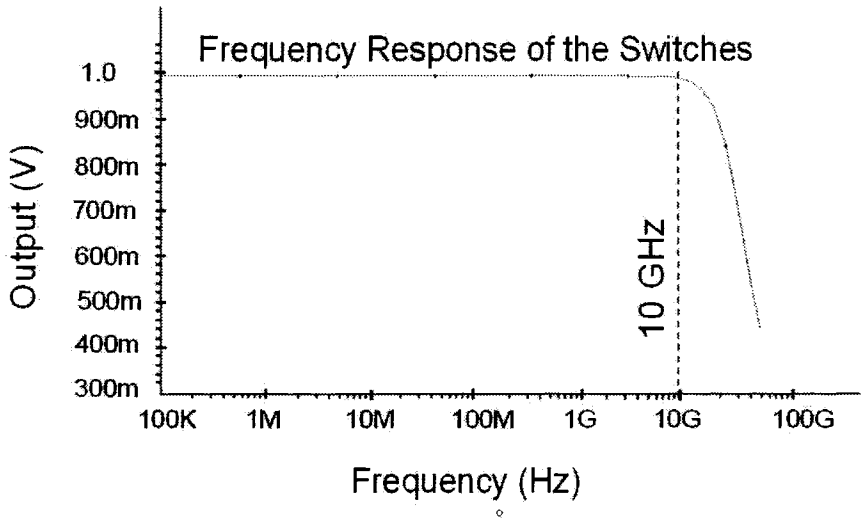

Figure 75: Frequency Response of the Analog Switches Used in the Mixer.

The mixer's transient response for a sinusoidal input of $V_{in} = 0.9sin(2\pi \times 250 \times 10^6 t)$ and a 2.0 GHz squarewave carrier is presented in Figure 77. The spectrum of the output shows fundamentals and harmonics together with the additional components produced by the mixer's nonlinearity and the carrier feedthrough.

Simulation results presented in Table 5 indicate that the Mixer's design goals are

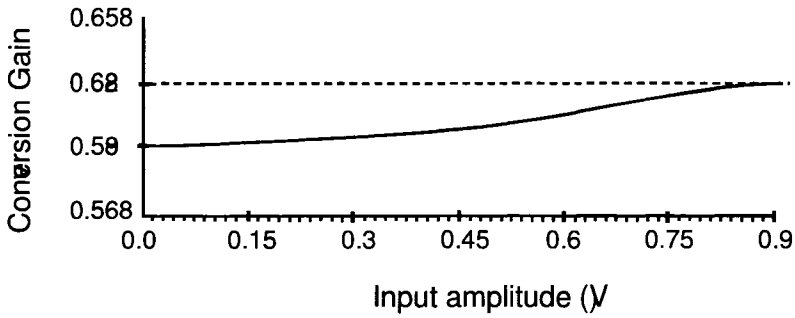

Figure 76: Mixer's voltage conversion gain versus input voltage amplitude.

met.

Table 5: Mixer's Design Goals and Simulation Results

Parameter	Design Goals	Simulation Results
RF Input Frequency	1.0 MHz - 3.0 GHz	1.0 MHz - 10.0 GHz
IF Input Frequency	DC - 25 MHz	DC - 100 MHz
Conversion Gain Variation for $Vin_{pp} = 1.8V$	$< 5\%$	4.8%
Isolation	>35 dB	38dB

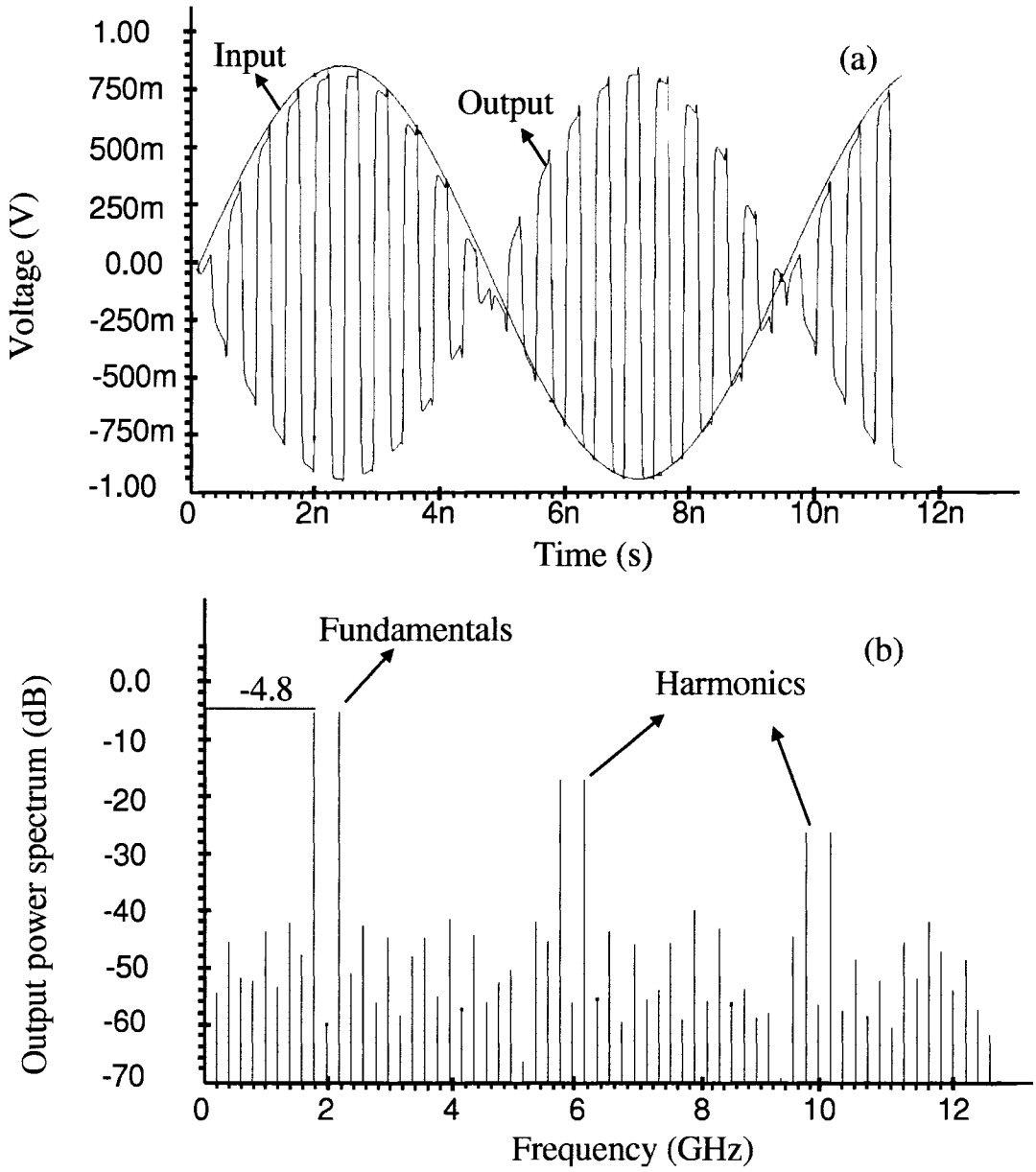

Figure 77: (a) Mixers input and output waveforms. (b) spectrum of the output.

5.1.4 Track and Hold

Channel charge injection associated with CMOS switches and clock feedthrough via parasitic capacitances is often the primary sources of error in open loop sampling circuits [65]. High-resolution fast CMOS T/H circuits utilize switched capacitor (SC) techniques [66, 48] or exploit the Miller hold capacitance method [67] to suppress the sampling error. Conventional SC samplers are mainly designed in differential configurations. They can substantially reduce the sampling error by differential operation [68] however they introduce a significant offset error if used as single-ended samplers. For the purpose of on-chip sampling a new single-ended high speed CMOS T/H circuit is designed in which the sampling error is reduced through the use of a pseudo-replica circuit and dummy transistors [69].

The proposed T/H circuit as indicated in Figure 78 includes a sampling module with series capacitor and a replica circuit. It operates as follows. In the acquisition

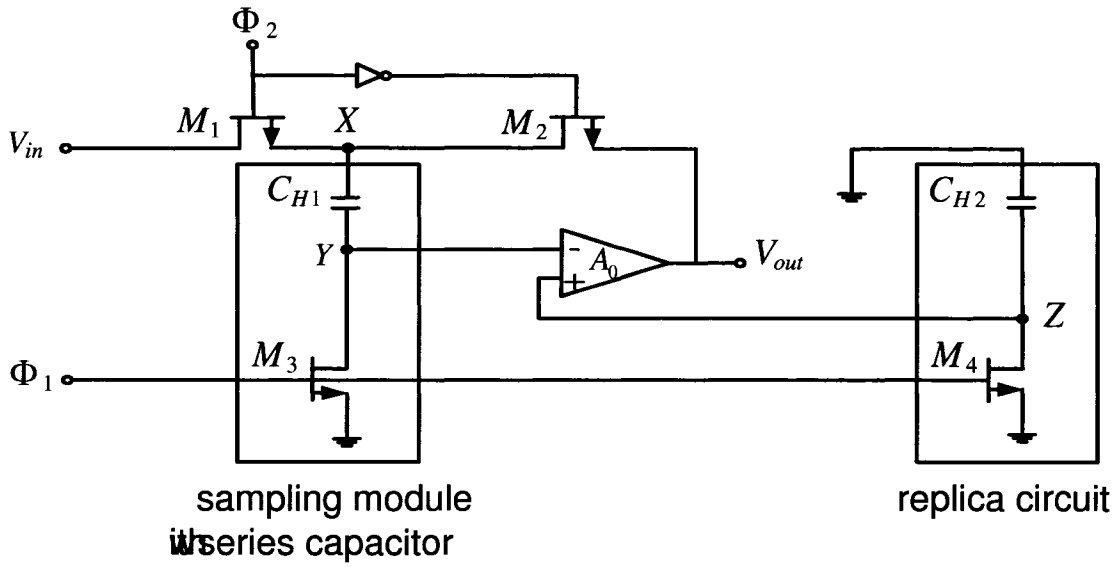

Figure 78: Track and hold circuit with a replica circuit.

mode M1 and M3 are on, M2 is off and the voltage across C_{H1} tracks the input (V_{in}) . In transition to the hold mode, first M3 goes off and after a slight delay ϕ_2 falls

turning M1 off and M2 on. M3 does not suffer from the body effect since its source junction is connected to the ground and as a result its channel charge produces an input-independent offset error on C_{H1} . When M3 turns off, the conducting path from C_{H1} to ground is opened and consequently the charge corresponding to the instantaneous input voltage level is trapped on C_{H1}. The voltage level across C_{H1} does not change until M3 turns on again and provides the conducting path from the hold capacitance to the ground. Thus, the charge injected by M1 does not affect the voltage level on C_{H1} . To derive an expression for the output (V_{out}), it is assumed that the effect of clock feedthrough is negligible. This assumption is later validated by adding dummy transistors to the T/H scheme.

Assuming M3 and M1 turn off at $t = t_s$ and $t = t_h$ respectively, the voltage level at the upper plate (X) and the lower plate (Y) of C_{H1} in Figure 78 at $t = t_s$ can be expressed as: $V_x(t_s) = V_{in}(t_s)$ and $V_y(t_s) = V_{\Delta M3}$. Where $V_{\Delta M3}$ is the offset voltage produced by M3 at node Y. During the time period of $t_s \leq t < t_h$ M3 is off and thus any voltage variation at node X is reflected at node Y and one can write:

$$V_y(t) = V_{\Delta M3} + V_x(t) - V_{in}(t_s) \qquad for \qquad t_s \leq t < t_h \tag{38}$$

When M1 goes off at $t = t_h$ its charge injection produces an error ($V_{\Delta M1}$) affecting the voltage levels at both plates of the hold capacitance. Therefore, at $t = t_h$ we can express the voltage levels at the upper and lower plates of C_{H1} as:

$$V_x(t_h) = V_{\Delta M1} + V_{in}(t_h) \tag{39}$$

$$V_y(t_h) = V_{\Delta M3} + V_{\Delta M1} + V_{in}(t_h) - V_x(t_s) \tag{40}$$

The voltage across C_{H1} for $t_s \leq t < t_h$ is given by:

$$C_{CH1} = V_x(t_s) - V_y(t_s) = V_x(t_h) - V_y(t_h) \tag{41}$$

that is:

$$V_{CH1} = V_{in}(t_s) - V_{\Delta M3} \tag{42}$$

When M2 goes on, the negative feedback is established and the voltage level at the lower plate of the hold capacitance starts to change. However, the voltage level across C_{H1} remains unchanged since the conducting path is still open. When the feedback loop around the op-amp settles down, the voltage levels at the negative input (V_y) and the positive input (V_z) become equal. The output voltage can be expressed as: $V_{out} = V_{CH1} + V_y$. Substituting for V_{CH1} from 42 gives $V_{out} = V_{in}(t_s) - V_{\Delta M3}$ and since $V_y = V_z$ we can write:

$$V_{out} = (V_{in}(t_s) - V_{\Delta M3}) + V_z \tag{43}$$

The fraction of charge injected through the source and drain of a CMOS transistor depends on the source and drain voltages, the impedances seen by them and the speed of the clock at the gate junction. Thus, if we choose the same size of M3 and M4 in Figure 78 and drive them with the same clock speed and also if $C_{H1} = C_{H2}$ then we can conclude that the offset error at node Z ($V_{\Delta M4}$) produced by M4 is equal to the offset error at node Y ($V_{\Delta M3}$) introduced by M3 and thus $V_z = V_{\Delta M3} = V_{\Delta M4}$. Substituting V_z in 43 gives:

$$V_{out} = (V_{in}(t_s) - V_{\Delta M3}) = V_{in}(t_s) \tag{44}$$

In summary, the voltage across C_{H1} in the hold mode comprises the sampled instance of the input and the offset error introduced by M3 charge injection. The replica circuit supplies the op-amp with an offset voltage equal to the error voltage produced by M3 enabling the op-amp to remove the error from the output. It can be shown that if a non-ideal op-amp with a limited gain of A_0 and input capacitance of C_{in} is used the output voltage in equation 44 changes to:

$$V_{out} = \frac{V_{in}(t_{ts})}{1 + (C_{in}/C_{H1} + 1)/A_0} \simeq V_{in}(t_s)[1 - (C_{in}/C_{H1} + 1)/A_0] \tag{45}$$

Thus, the T/H circuit introduces a gain error of approximately $-(C_{in}/C_{H1} + 1)/A_0$ in practice. This error can be considerably reduced by an appropriate op-amp design.

While the circuit presented in Figure 78 effectively eliminates the error produced by charge injection, the scheme still suffers from a limited input dynamic range and the error introduced by clock feedthrough. The dynamic range is simply extended to the supply voltages by replacing M1 and M2 with complementary pairs of P and N channel transistors. To suppress the clock feedthrough dummy transistors with half the width of the main transistors have been added. The T/H scheme with an extended dynamic range and dummy transistors is presented in Figure 79.

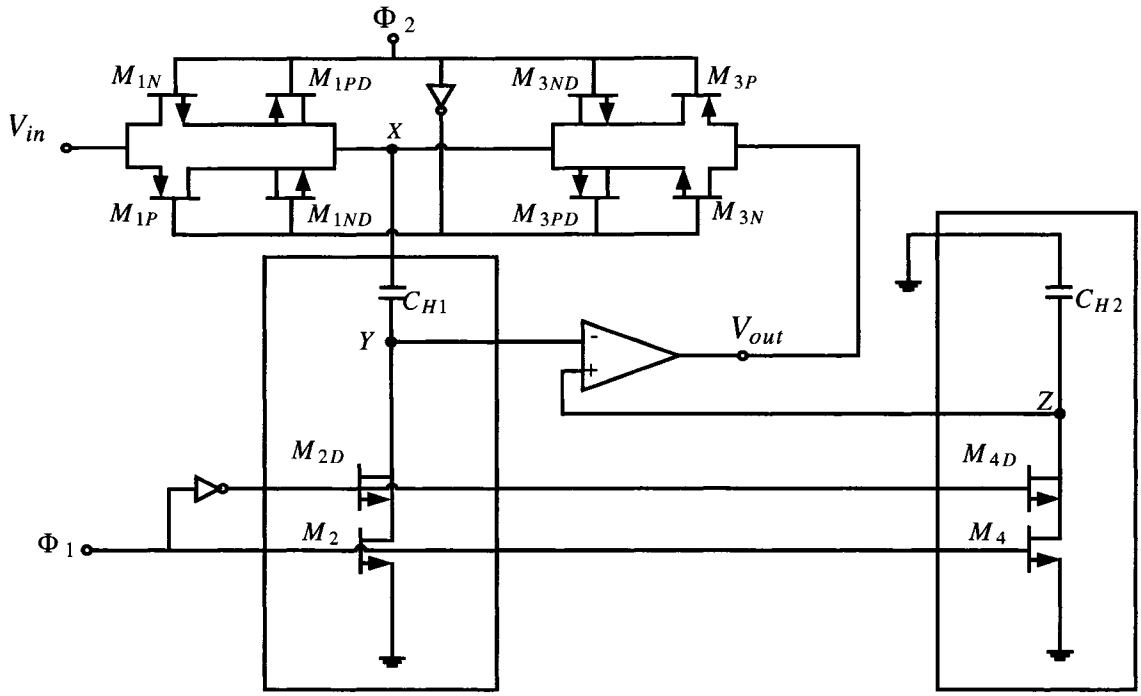

Figure 79: T/H circuit with complementary and dummy transistors.

The size of the transistors are given in Table 6

The input and output waveforms for a test case where a sinusoidal input of 1.8 V_{PP} and 10 MHz is sampled with 100 MHz clock are depicted in Figure. 80. The spikes can be explained by noting that the voltage level at the negative input of the op-amp is a function of the input signal in transition to the hold mode and whenever that

N Transistors			P Transistors		
No.	Width	Length	No.	Width	Length
M_{1N}	50μm	180nm	M_{1P}	200μm	180nm
M_{1ND}	25μm	180nm	M_{1PD}	100μm	180nm
M_{2N}	50μm	180nm	-	-	-
M_{2ND}	25μm	180nm	-	-	-
M_{3N}	20μm	180nm	M_{3P}	80μm	180nm
M_{3ND}	10μm	180nm	M_{3PD}	40μm	180nm
M_{4N}	50μm	180nm	-	-	-
M_{4ND}	250μm	180nm	-	-	-

Table 6: The width and length of transistors in the implemented T/H circuit

voltage falls below the level at the positive input, voltage spikes are generated. When the circuit enters the hold mode, the output is adjusted to the sampled input and the spikes are eliminated. Figure 81 shows the simulated hold pedestal error for the sampling scheme presented in Figure 79 as a function of DC input voltage for two different clocks with transition times of 300 ps and 600 ps.

From Figure 81, we can observe that the proposed cancellation technique presents a low sensitivity to the clock transition time. The hold pedestal errors for the applied clocks are almost equal and less than 1.6 mV over the input voltage range of 0-1.8 V. Table 7 indicate the summary of track and hold design goals and simulation results.

Table 7: Track and Hold Circuit Design Goals and Simulation Results

Parameter	Design Goals	Simulation Results
Pedestal Error for $Vin_{pp} = 1.8V$	<2 mV	1.6 mV
-3db Bandwidth	> 3 GHz	4.8 GHz
SNDR at 1.0 GHZ	>50 dB	54 dB

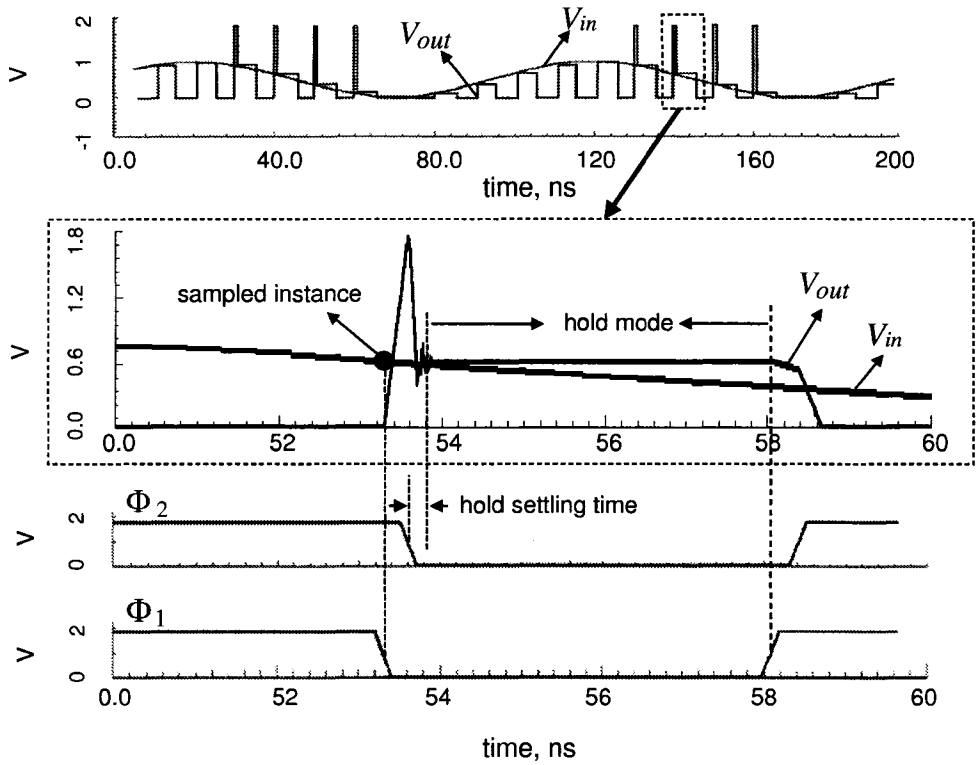

Figure 80: The input and output waveforms of the T/H circuit for a sinusoidal input of 1.8 V_{PP} at 10 MHz with a 100 MHz sampling clock.

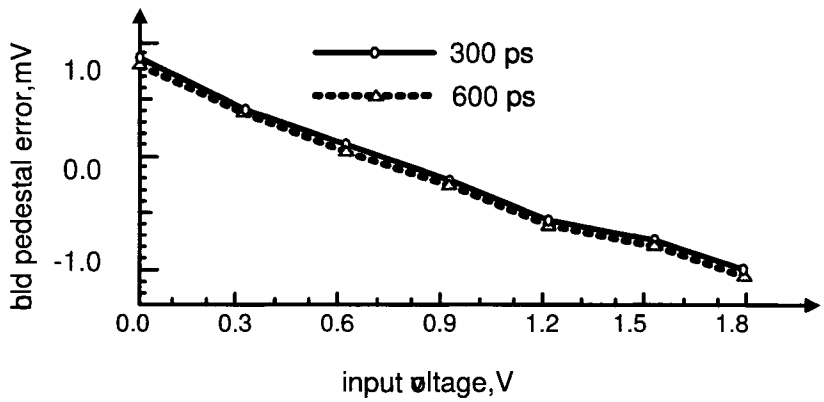

Figure 81: Simulated hold pedestal error as a function of DC input voltage for two different clock transitions of 300 ps and 600 ps.

5.2 Digital Circuits

To design digital circuits, first Verilog Register Transfer Level (RTL) codes were prepared and synthesized using VrilogXL simulator, the test benches were designed in Verilog and then the behavior of the designed circuits were verified using Cadence Simvision tool. The synthesized codes were transferred to Cadence Silicon Ensemble for automatic layout generation. The extracted physical layouts of the circuits were tested again to ensure that the design targets are met. To protect the analog circuit from switching noise, all digital circuits (Figure 82), except for the multiplexers, were placed in a different part of the chip and supplied with a separate power supply.

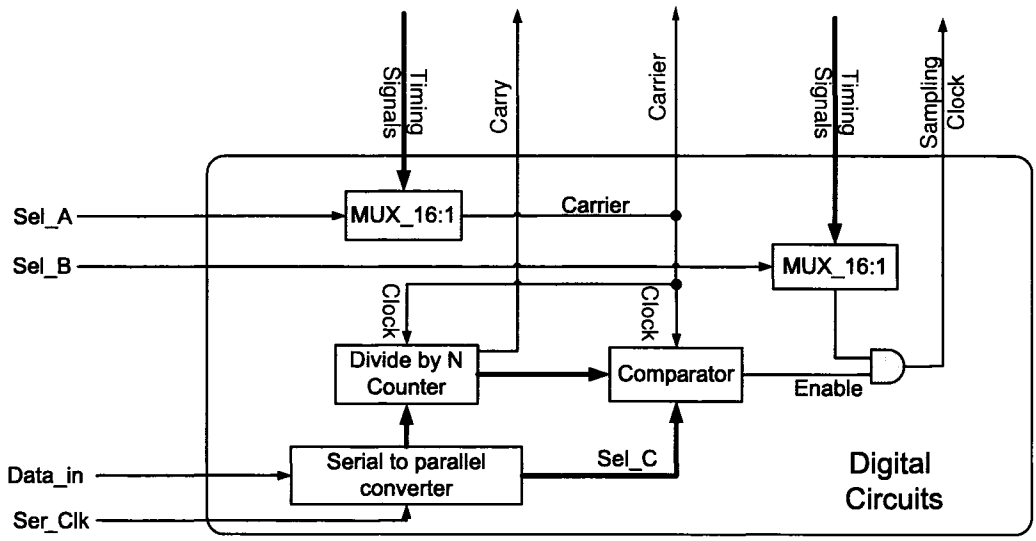

Figure 82: Block diagram of digital circuits.

5.2.1 Multiplexer

As shown in 22 two digital multiplexers (Mux_A & Mux_B) are required to select timing signals generated by the PLL and DLL modules. The design of the multiplexers have to satisfy two conditions: (a) It has to be able to operate over a frequency range up to 2.7 GHz and (b) present equal propagation delay from each input line to the output. To meet the second requirement, a sixteen to one multiplexer is designed

to have a complete symmetry between each input line and the output. The speed condition is met by constraining the design before logic synthesis. Figure 83 shows the circuit diagram after the codes are complied with the Synopsys design analyzer tool. It can be seen that the circuit has symmetry with respect to the inputs.

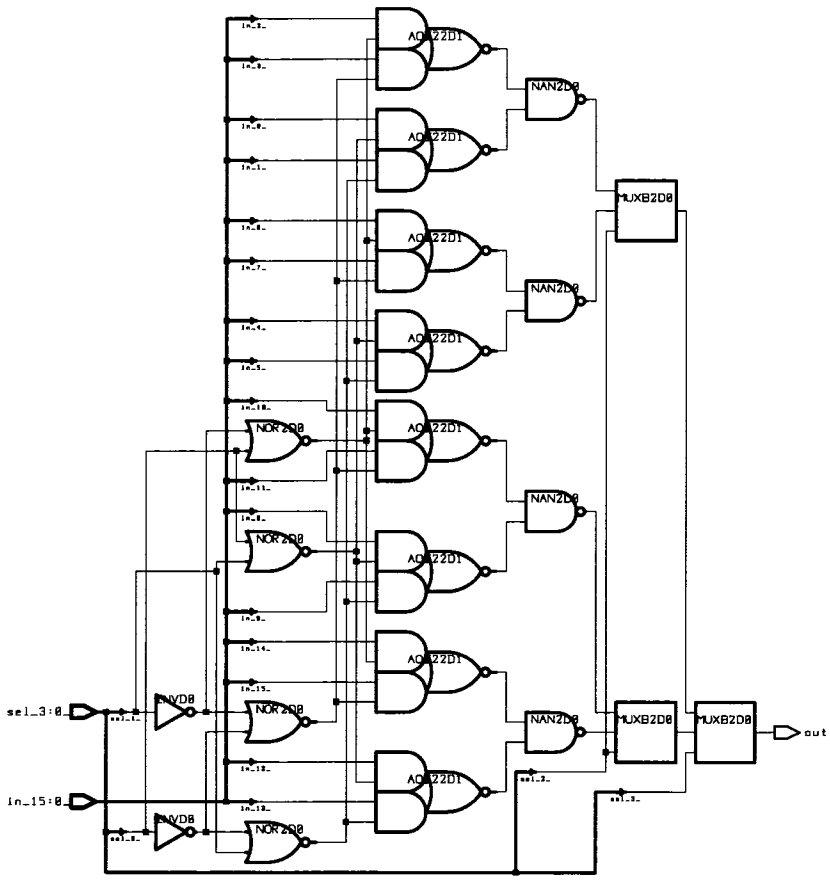

Figure 83: Circuit diagram of the multiplexer generated by synopsys design analyzer.

5.2.2 Counter

To convert the designed PLL to an integer-N frequency synthesizer, a divide by N counter is required. The frequency of the VCO output is divided by N through the counter and then applied to the PFD module to get synchronized with the input signal. Since the maximum VCO frequency (2.7 GHz) is more than two times higher than the minimum VCO frequency (1.0 GHz), a simple ripple counter is employed as a divide by N counter. The RTL code representing the counter is listed below. The counter receives a clock signal and 10-bit data as inputs and generates *carry* and q signals as outputs. The 10-bit input data is compared with the counter's output value and whenever they are equal a carry signal is generated and then the counter is cleared to restart the counting again.

Figure 84 shows the circuit diagram of the counter generated by synopsys design analyzer.

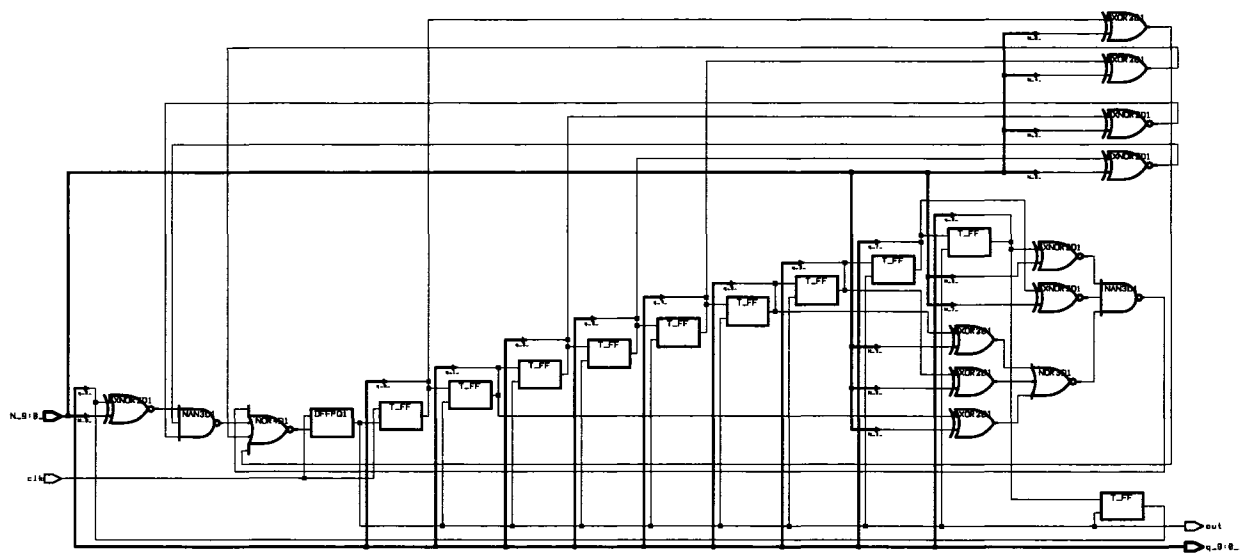

Figure 84: Circuit diagram of the counter generated by synopsys design analyzer.

5.2.3 Comparator

The comparator receives two 10-digit numbers and a clock signal. It generate a pulse that last for one period of the clock when the input numbers are equal. The only design complication is the speed of the operation which is defined by the maximum frequency of the VCO. This condition is met by constraining the clock signal during the synthesis process. The RTL code of the comparator is given below and its circuit diagram is presented in Figure 85

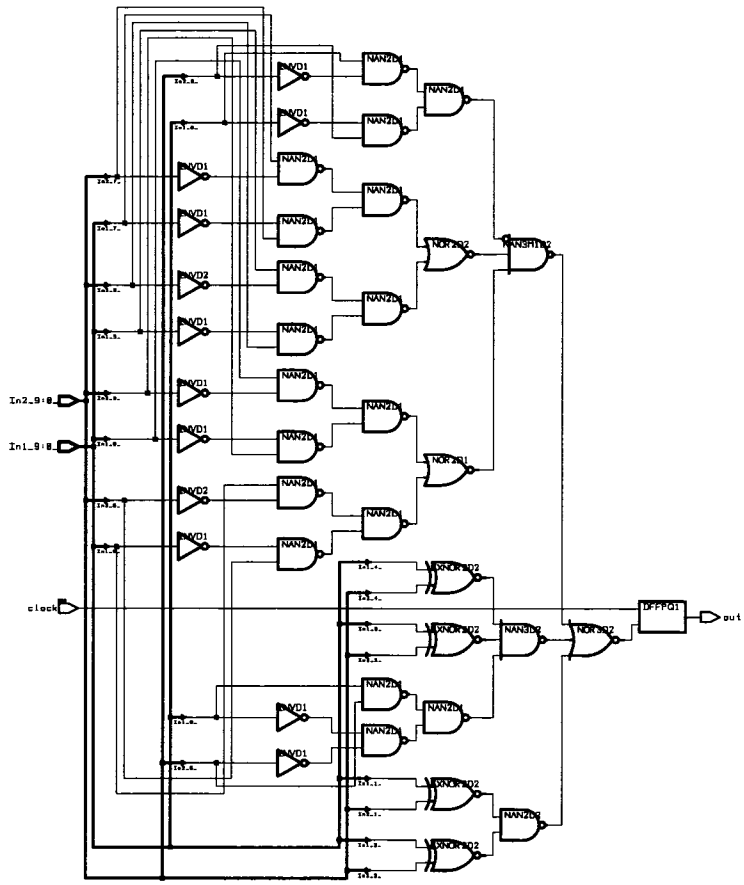

Figure 85: Circuit diagram of the comparator.

5.2.4 Serial-to-Parallel Converter

To reduce the number of required I/O pins, data is serially loaded into a register and then converted to parallel data inside the tester core. The RTL code for the serial to parallel module is listed below and its circuit diagram is shown in Figure 86.

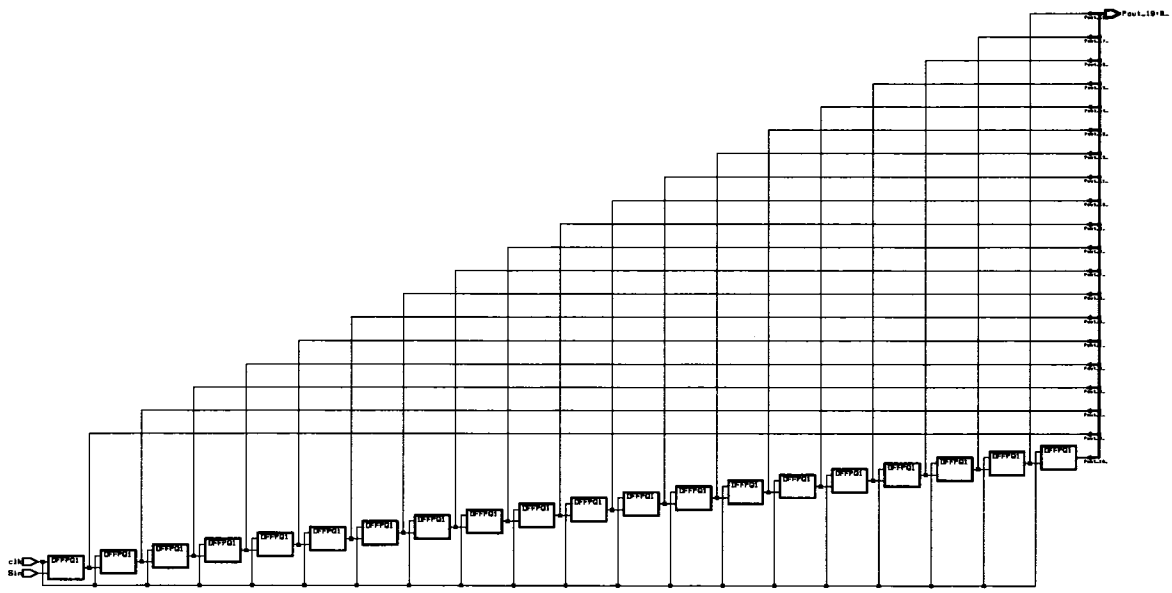

Figure 86: Circuit diagram of the serial to parallel converter module.

5.3 Measurement Accuracy

The main sources of measurement error are related to: (a) the nonlinear nature of the mixer used to generate the test stimulus; (b) the jitter associated with the PLL and DLL circuits; and (c) the hold pedestal error produced by the T/H circuit. Errors associated with the T/H circuit and the sampling clock jitter are the main sources of measurement uncertainty. The limits of the error introduced by jitter can analytically be determined while the T/H error has to be obtained through simulation.

1. **Error introduced by the T/H circuit**

   To evaluate the nonlinearity of the T/H circuit, Cadence tools were used to

setup a simulation environment for the T/H circuit. Sinusoidal waveforms were generated and applied to the T/H input and samples of the output were collected. Cadence calculator was used to calculate FFT of the samples. From the FTT results signal to noise and distortion ratio (SNDR) of higher than 53 dB for input sinusoidal signals of 0.5 V_{PP} up to 100 MHz was achieved.

2. **Error introduced by jitter**

The jitter of the sampling clock [70, 71] introduces noise on the captured response waveforms. To estimate the error, we assume a sinusoidal input of $V_{in} = Asin2\pi f_{in}t$ and a small sampling clock jitter of ϵ. Thus, the samples are obtained at $t = KT_s + \epsilon$.

$$V_s = Asin2\pi f_{in}(KT_s + \epsilon) \tag{46}$$

For a small $\epsilon 2\pi f_{in}$ that is

$$V_s = Asin(2\pi f_{in}(KT_s)) + \epsilon 2\pi f_{in} Acos(2\pi f_{in} KT_s) \tag{47}$$

Thus, the sampled waveform can be viewed as an ideal wave and a noise component of

$$\epsilon 2\pi f_{in} Acos(2\pi f_{in} KT_s) = \epsilon dV_{in}/dt \tag{48}$$

Assuming that ϵ is not correlated to V_{in} , the noise power is expressed as:

$$P_\epsilon = \epsilon_{rms}^2 \frac{1}{T_{in}} \int_0^{T_{in}} (\frac{dV_{in}}{dt})^2 dt = \epsilon_{rms}^2 2\pi^2 f_{in}^2 A^2 \tag{49}$$

where $T_{in} = 1/(2\pi f_{in})$. The signal to noise ratio (SNR) is given by:

$$SNR = -20log2\pi f_{in}\epsilon_{rms} dB \tag{50}$$

As indicated in equation (49) the noise power produced by the sampling clock jitter is a function of the input frequency square which increases rapidly for high frequency input signals.

5.4 Mixed Signal Interconnect and Packaging

The physical implementations of the analog circuits were carried out manually according to analog layout techniques [72] in order to minimize the effect of crosstalk and noise on the circuits. Figure shows the layout of the entire chip.

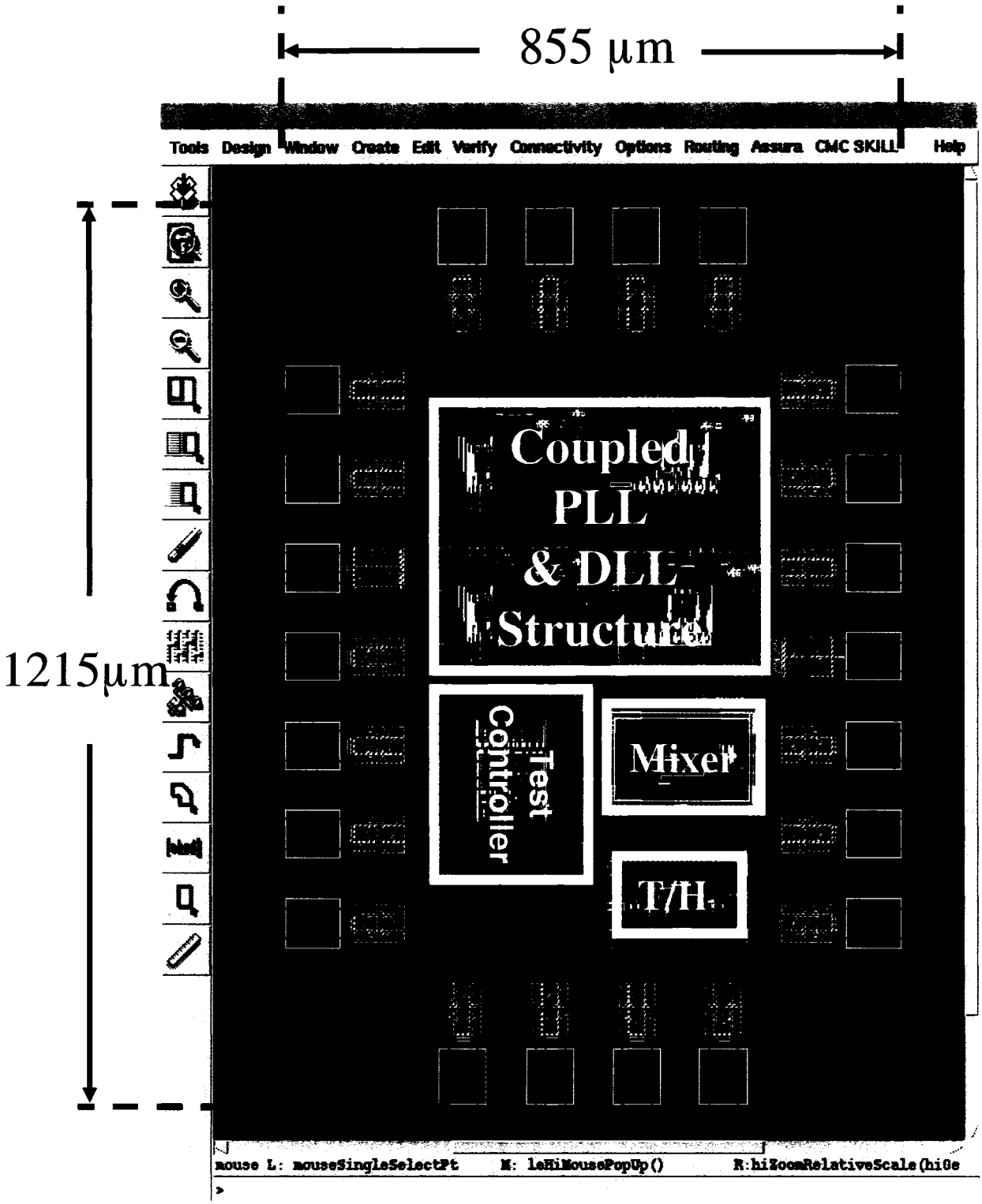

Figure 87: Layout of the tester core.

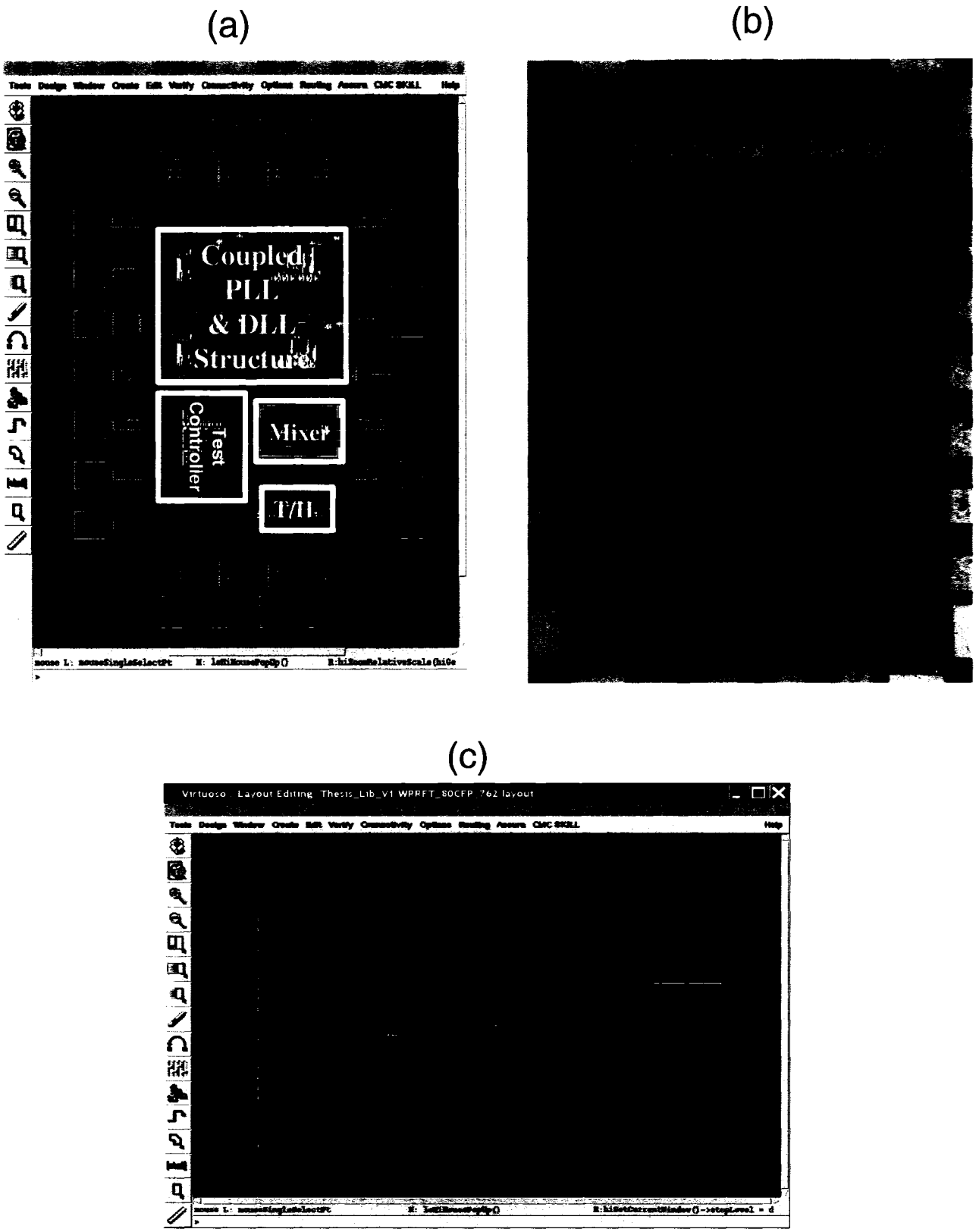

Figure 88: Designed tester core (a) chip layout. (b) chip photo. (c) bonding diagram.

The post layout simulation of the VCO output shown in Figure 89 matches the schematic level simulation result to a reasonable degree.

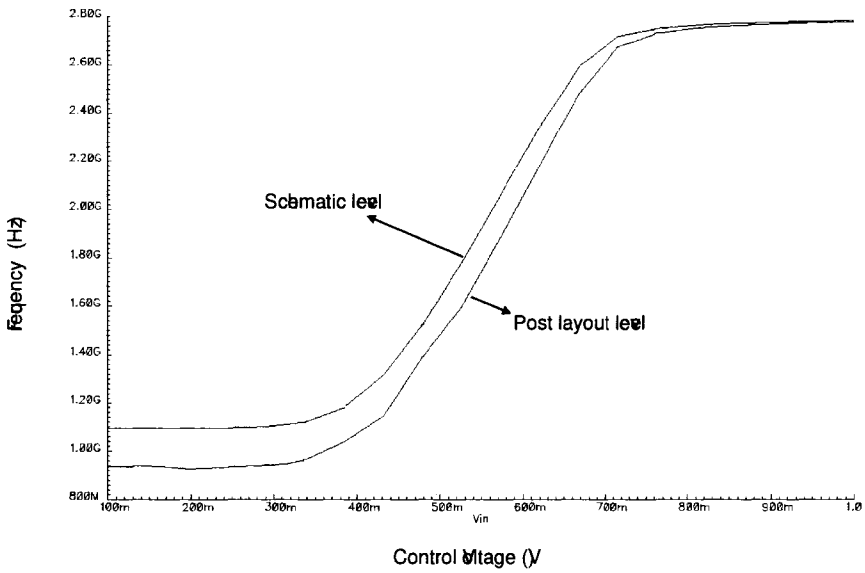

Figure 89: Simulation of VCO tuning range before and after physical implementation.

5.5 Summary

Physical level implementations of the individual parts of the tester were presented in this chapter. The schematic and layout views were generated using Cadence tools and their performance matric were determined via simulation using Spectrs and Hspice simulators. In the first part of this chapter, the implementation of analog portion of the tester which includes phase locked loop, delay locked loop, mixer and track and hold were presented. Using Cadence design tools, simulations were performed to examine the performance of the analog circuits. Verilog codes representing digital circuits and their associated schematic diagrams were also represented in this chapter. In the last part, the potential sources of noise and distortion were discussed and mathematical model developed to formulate the power of the noise associated with the sampling clock jitter.

CHAPTER VI

CALIBRATION PROCEDURE AND SIMULATION RESULTS

The first step in the process of testing a circuit is to verify the operation of the tester to ensure accurate measurement and reliable performance. This requirement is particularly important when embedded testers are designed since they are subjected to the same process variations as the rest of the circuitry on the chip. To deal with this problem three switches have been added to the tester for the purpose of calibration and self-test as shown in Figure 90. In normal operation mode, test waveforms are applied to the CUT and the response signals are sampled by the T/H circuit. In

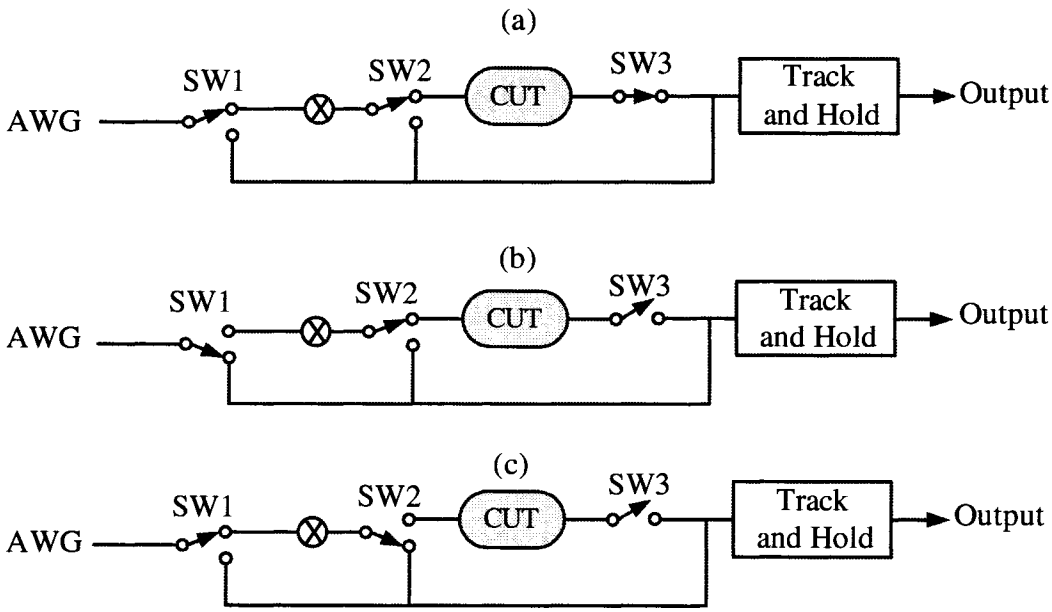

Figure 90: (a) Normal operation mode. (b) calibration and self-test mode to measure the sampling module performance. (c) calibration and self-test mode to measure the performance of the mixer module.

the calibration and self-test mode, the switches are set so that a direct signal path between the input and the T/H circuit is established. At this stage, DC and AC input signals are applied to the T/H circuit and its responses are measured. The measurement results show the errors introduced by the sampling module containing the T/H circuit and the sampling clock generator. At the next step, the switches are set so that the output of the bipolar chopper modulator, which includes the mixer and the carrier signal generator, is applied to the T/H circuit. The spectrum of the mixer's output is measured to reveal the distortion added by the chopper modulator. The error measured in the calibration mode has three different sources: nonlinearity, DC offset error and gain error. The gain and DC offset errors can simply be eliminated by data processing in software domain. However, the nonlinearity error introduced by the T/H circuit and the jitter of the sampling clock cannot be completely eliminated and eventually they determine the tester's measurement accuracy.

To evaluate the measurement capability of the tester, an RF oscillator and a Low Noise Amplifier (LNA) were selected to be tested. The simulation results as indicated below show that the tester can measure the performance metric of high-speed CUTs with an acceptable degree of accuracy.

6.1 RF Oscillator Performance Metric Measurement

The selected RF oscillator as shown in Figure 91 is a Colpitts oscillator that generates a sinusoidal waveform of 0.875 V amplitude at 1.13 GHz frequency (Figure 92). To measure the parameters of the oscillator, the tester have to be synchronized with the oscillator's output waveform. A comparator is used to change the sinusoidal output to a digital level squarewave. Then the output of the comparator is applied to the sync input of the tester. A total number of 110 samples over one cycle of the oscillator's output waveform were obtained through subsampling and then fast Fourier transform

of the samples were calculated. Figure 93 shows the spectrum of the output obtained by FFT. From the simulation result, the amplitude of the fundamental component is found to be 846 mV which indicates less than 14 mV amplitude error.

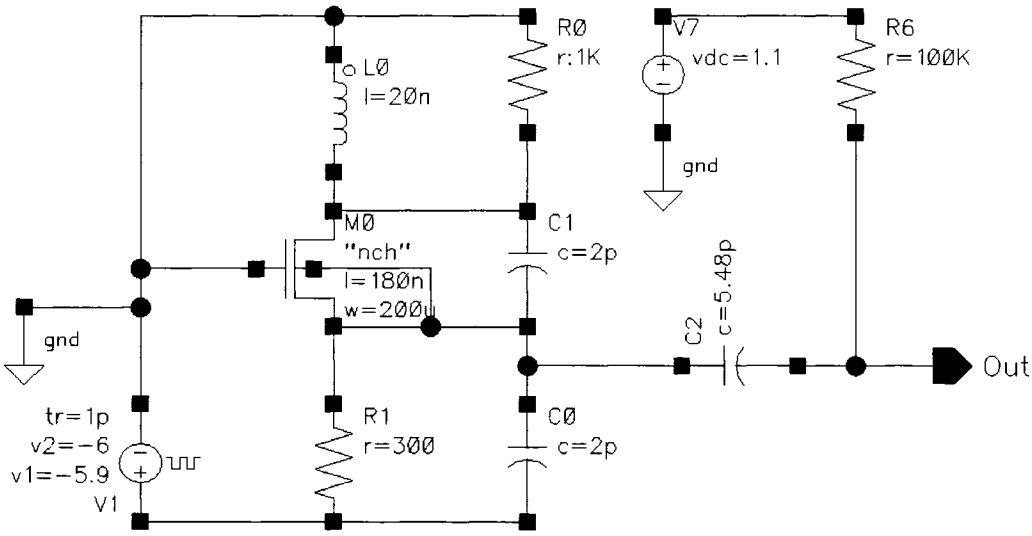

Figure 91: Schematic diagram of the RF oscillator used a CUT.

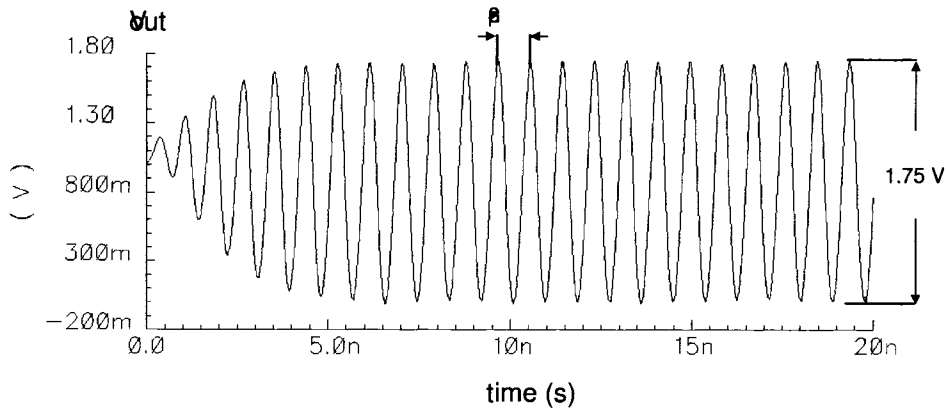

Figure 92: RF oscillator output waveform.

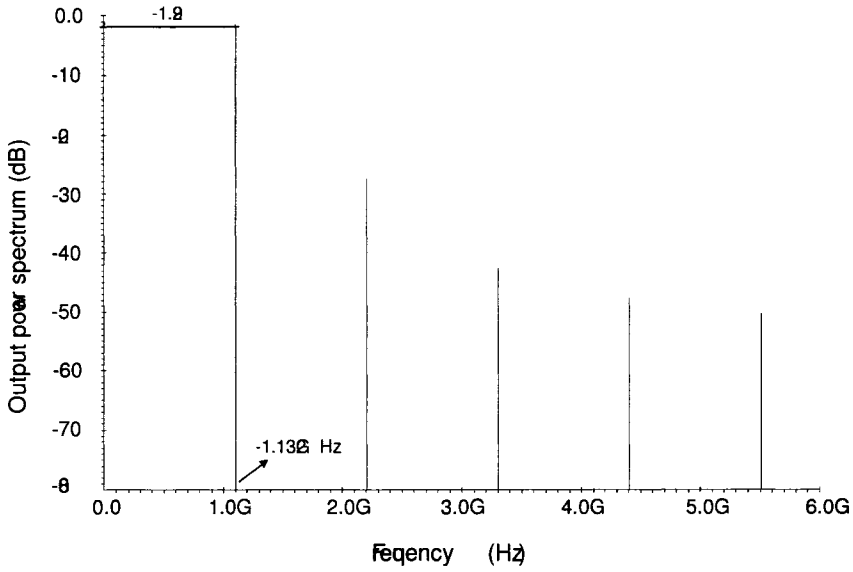

Figure 93: Simulated power spectrum of the oscillator output.

6.2 Performance Metric Measurement of a Low Noise Amplifier

To further evaluate the measurement capabilities of the tester an LNA specified in Table 6.2 was selected as a CUT. The AWG was programmed to generate a sinusoidal test waveform of $40mV_{pp}$ at 2MHz and the synthesizer was set to generate a 2 GHz squarewave as carrier. The CUT's response was captured by collecting samples of

Parameter	Unit	Value
Power Gain (S21)	dB	28
Input Referenced IP3	dBm	-10
Frequency	MHz	700 - 2400
Noise Figure(NF)	dB	2

Table 8: Performance parameters of the LNA used as a CUT

the output waveform in a time slot of 500ns through subsampling method. The FFT of the samples was calculated with the Cadence calculator. Figure 94 shows the single-sided spectrum of the applied stimulus and the CUT's response.

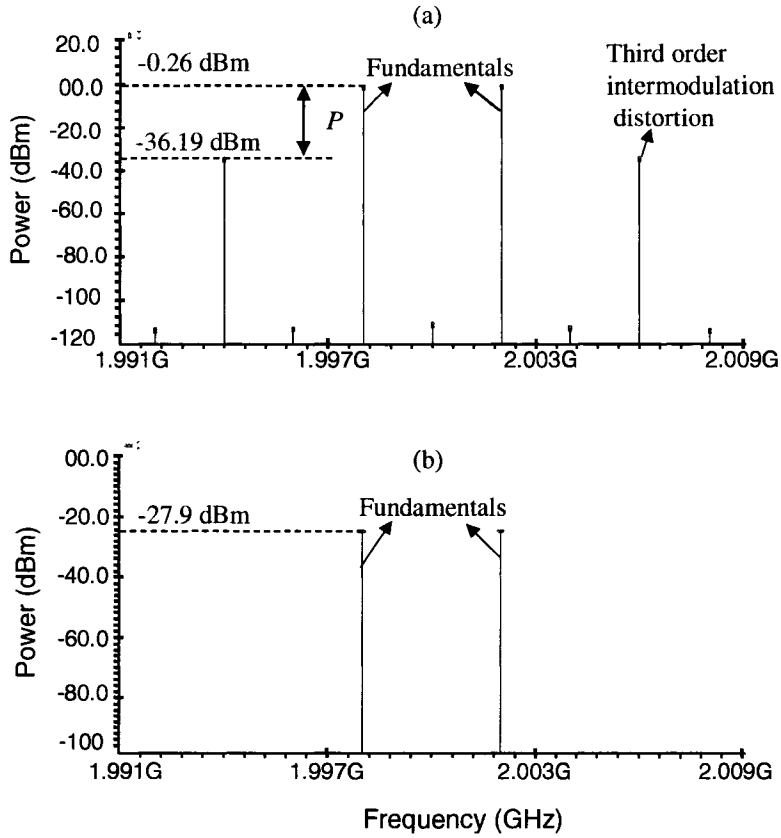

Figure 94: Simulated two-sided power spectrum of (a) CUT's response. (b) applied stimulus.

The spectrum of the stimulus shows two lines representing the fundamentals of the applied high frequency stimulus waveform at 2GHz-2MHz and 2GHz+2MHz corresponding to a power of -27.9 dBm in 50 Ω. The LNA's output spectrum includes two lines of -0.26 dBm at 2GHz ± 2MHz representing the LNA's response to the two tone fundamentals and two lines of -36.19 dBm at 2GHz+4MHz and 2GHz-4MHz that are generated by the third-order intermodulation. The power gain can be obtained from the spectrum of the input and output as:

$$Gain = -0.27 - (-27.9) = 27.64\ dB \tag{51}$$

which has less than two percent difference as compared to the ideal gain value. To calculate the third-order intercept point (IP3) without extrapolation the following

Equation [49] was used:

$$IP_3|_{dBm} = \frac{\Delta|dB}{2} + P_{in}|_{dB} \tag{52}$$

where $P_{in}|_{dB}$ denotes the input signal power in dBm and $\Delta P|_{dB}$ is the difference between the power of the fundamentals and the power of the third order intermodulation at the output if the power levels are expressed in dBm. For the simulation case presented in Figure 94, the IP3 is equal to:

$$IP_3|_{dBm} = \frac{-0.26 - (-36.19)}{2} - 27.9 = -9.93\ dBm \tag{53}$$

Figure 95 indicates the simulated nominal gain and IP3 for an input power ranging from -60 dBm to -20 dBm. For low level input signals, the simulation results are approximately equal to the nominal values with less than 2% difference. When the

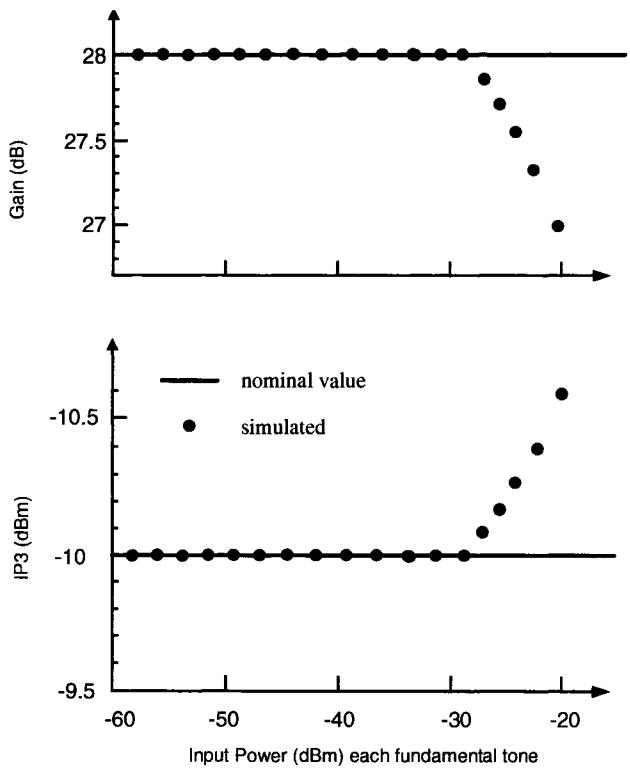

Figure 95: Simulated (a) gain and (b) IP3 against the power of the fundamental tone at the input.

input power increases to -27 dBm and higher, the difference between the expected

Technology	1.8 V, 6-Metal, 0.18 μm CMOS Process
Target devices	CMOS RFICs, LNA's, Mixers, Power amplifiers, PLLs,etc.
Area	1.0 mm^2
Area without pads	0.455 mm^2
Test frequency range	1.0 MHz-2.7 GHz
Sampling clock resolution	< 10 ps
Peak to peak sampling clock jitter at Fin= 1.1 GHz	2.5 ps
Sampling module SNDR at Fin=100 MHz	53 dB
Sampling module SNDR at Fin=2.5 GHz	43 dB

Table 9: Performance Parameters of the Tester

and the nominal values rises rapidly. This can be explained by noting that the nonlinearity of the LNA becomes significant when the input power level is increased. Table 9 summarizes the performance of the tester core and its major specifications.

6.3 Summary

In this chapter simulation results were presented. In the first part, the operation of the embedded tester in the self-test and calibration mode was explained. Then the measurement capabilities of the tester were evaluated using an RF oscillator and a low noise amplifier as circuits under test. Simulation results obtained using Cadence SpectreS simulation tool were also presented. The results showed that the proposed test methodology can successfully be employed to measure relative performance metrics of fast analog/RF circuits via a low speed external controller.

CHAPTER VII

EXPERIMENTAL RESULTS

This chapter deals with the experimental measurements that were performed to evaluate the characteristics of the embedded tester. Sine wave and step signal tests [73] were performed to determine the parameters of the tester. First, measurements were taken to evaluate the combined effect of clock jitter and track and hold accuracy. The second measurements were made to evaluate the bandwidth of the T/H circuit.

7.1 Low Frequency Sampling Accuracy Test

The purpose of this test is to determine the sampling accuracy of the T/H circuit. The basic procedure is to apply a sine wave as an excitation signal and measure the samples captured by the T/H circuit to calculate parameters both in frequency and time domains. The signal path for sine wave test is shown in Figure (96). The self-test switches, SW1, Sw2 and SW3, are set to directly apply the input sine wave to the T/H circuit.

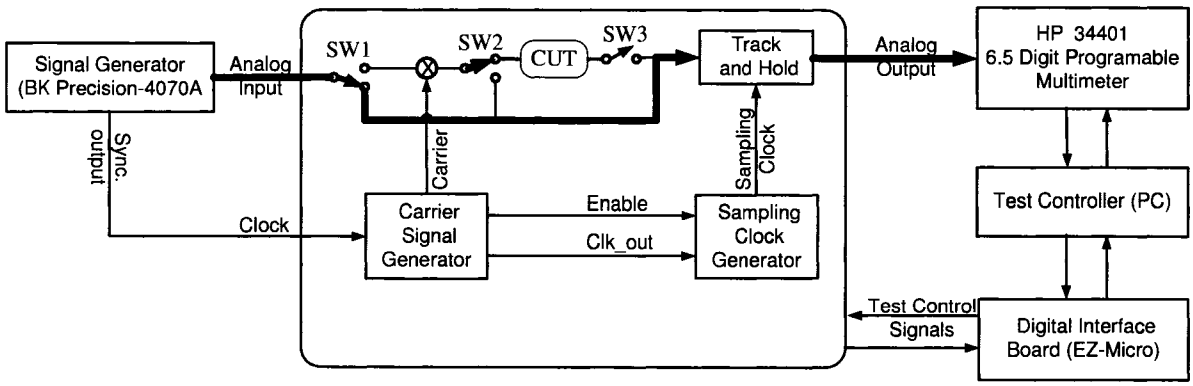

Figure 96: (a) Setup for sine wave testing

The external signal generator was programmed to generate an input signal of $V_{in} = 0.02sin(2\pi 20 \times 10^6 t)$ and the resultant waveform was verified using an oscilloscope. The carrier signal generator was programmed to provide a signal of 1.28 GHz (64 times faster than V_{in}) that was used to synchronize the sampling clock frequency. A sample set, consisted of 64 samples taken over one period of V_{in}, was obtained by subsampling. To evaluate the measurement repeatability, five sample sets were compared. The measured samples and the equipments used are given in Appendix II.

The input signal and the mean value of the five measured sample sets are shown in Figure 97. The sample sets were compared and the resulting mean values and standard deviations were computed. The relative measurement error computed from $error = Average\frac{V_{in}-V_{measured}}{V_{amplitude}}$ was less than 5.3%. $V_{measured}$ represents the mean value of the five measured sample sets and $V_{amplitude}$ denotes the amplitude of the input signal. The resulting standard deviations shown in Figure 97(b), which indicate less than 2 mV RMS error, are considered as stringent measure of the noise associated with the combined effects (that are not separable) of clock jitter, T/H accuracy, self-test switches, power supply regulation and measurement accuracy.

The power spectrum of the average of the five sample sets, plotted in Figure 97, was computed using the Matlab FFT function. The resulting amplitude spectrum is shown in Figure 98(a) where the 20 mV amplitude of the input signal is readily apparent. The corresponding power spectrum shown in Figure 98(b) indicates that the sampling noise artifacts are all at least 38.7 dB below the power of V_{in}. To calculate the SNDR, first the power of the signal was determined from the power spectrum. Then, the signal was removed and the total power of remaining components was computed using Matlab "SUM" function. The measurement results show 31.3 dB signal to noise and harmonic distortion ratio.

To determine the effect of the input signal level on the SNDR, a new set of experiments was carried out with an input signal of $V_{in} = 0.5sin(2\pi 20 \times 10^6 t)$. The

measurement results for this case indicate 53.7 dB SNDR. The dependency of the noise and distortion on the input signal level was calculated for both the 20 mV and 500 mV input signal levels. In the case of 20 mV, the noise and distortion power was -68.3 dB and for the 500 mV case was -62.7 dB. This result is attributed to increased distortion caused by the combined nonlinear properties of the CMOS switches and the T/H circuit.

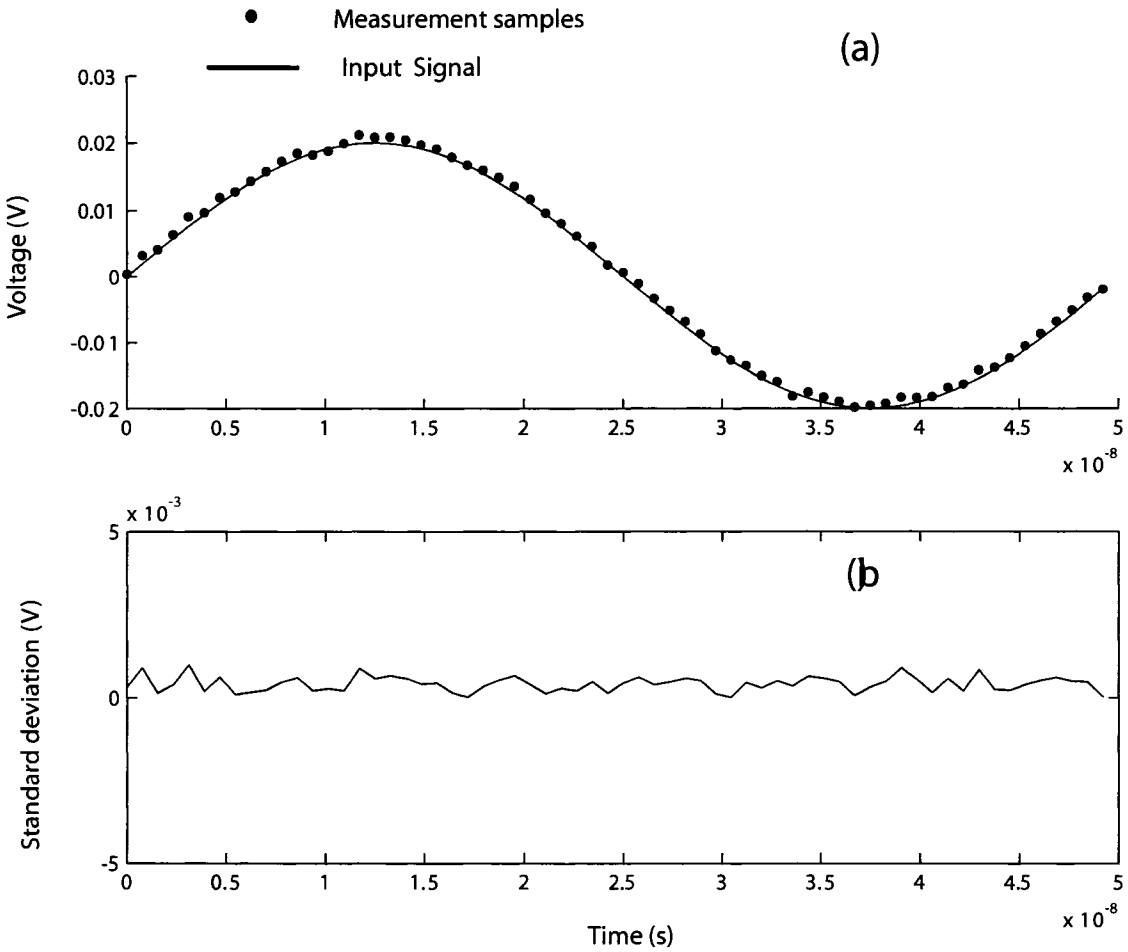

Figure 97: (a) Measured samples of the applied sinusoidal input. (b) Standard deviations of the samples.

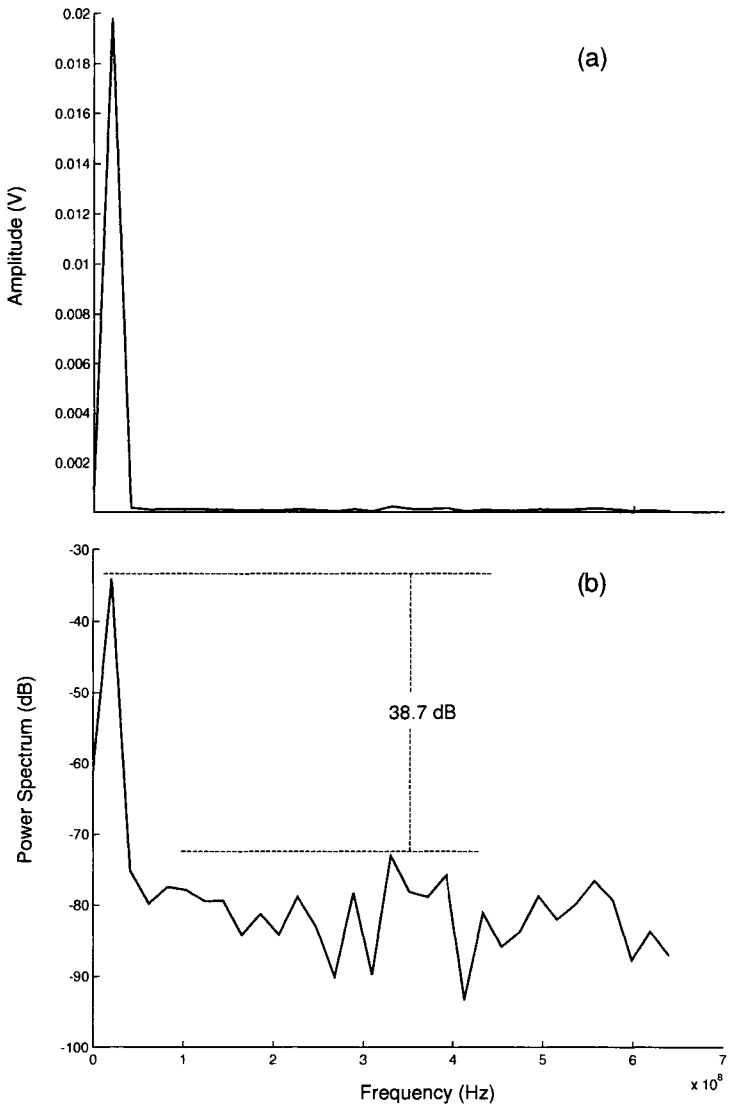

Figure 98: Single-sided spectrum(a) Amplitude. (b) Power.

7.2 High Frequency Sampling Accuracy Test

To calculate the SNDR at different frequencies, the configuration of the internal self-test switches were changed (Figure 99) to apply high frequency stimulus signals of 1.8 V_{pp} to the T/H circuit. $V_{in} = 0.9sin(2\pi 20 \times 10^6 t)$ was generated by the external.

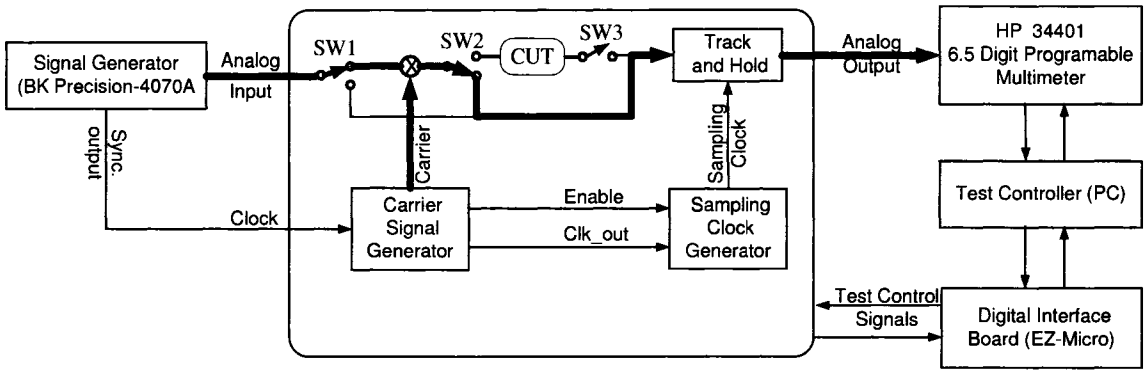

Figure 99: (a) Test setup for SNDR measurement

signal generator. The carrier signal generator was programmed to generate signals ranging from 100 MHz to 2.2 GHz. For each test case, a total number of 128 samples of the T/H input signal were taken by subsampling and the signal to noise was calculated using Matlab functions as specified in previous section.

Figure 100 shows the measured and the simulated SNDR versus input signal frequency. It can be observed that the measurement scheme supports over 44.3 dB SNDR up to an input signal frequency of 1.6 GHz which corresponds to over 7.0 effective bits linearity. From Figure 100 it can be seen that the SNDR drops off at high frequencies due to the increased distortion associated with the nonlinear properties of the signal path. The difference between the simulated and measured results is attributed to the model accuracy in modeling noise, parasitic effects and process variations.

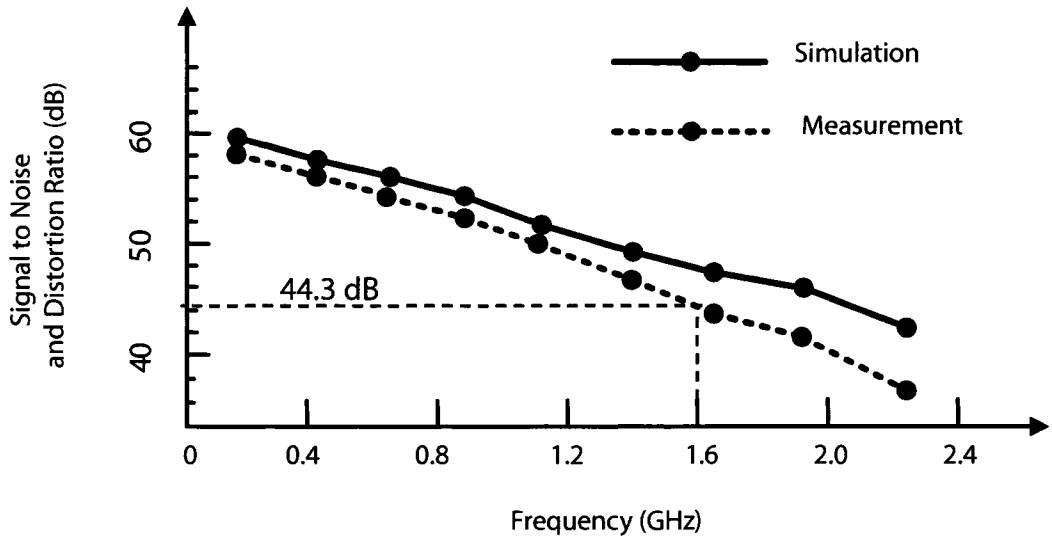

Figure 100: Simulated and measured SNDR versus input signal frequency

7.3 Step Response Testing

To determine the bandwidth of the employed T/H circuit, the test setup presented in Figure 96 was employed to perform a step signal test. To perform the test, a squarewave of 20MHZ was used to excite the T/H circuit. The coupled PLL and DLL module was programmed to provide sampling clocks of 9 ps resolution. A total number of 32 samples of the response were collected in different cycles of the input signal through subsampling.

Figure 101(a) shows the measured and simulated T/H step response. From the step response, the impulse response was computed using the DIFF function in Matlab (Figure 101(b)). It is recognized that differentiating the step response of a linear system to obtain the impulse reponse is an ill conditioned numerical method. However, the DIFF function used in Matlab represents the most robust method available. Defining the aperture time as the peak of the impulse response where 80 % of the power is contained [74], the impulse response yields an aperture time of 55 ps. The frequency response of the sampling scheme obtained from the Fourier transform of the impulse response is also shown in Figure 101(c). It can be seen that the -3dB

bandwidth of the proposed T/H scheme lies at 4.8 GHz. The measured step response, as indicted in Figure 101(a), exhibits overshot which can be explained by the effect of bonding pad wires.

Table 10: Measurement Results Summary

Parameter	Measured Value
Relative track and hold sampling error for $Vin = 0.02sin20 \times 10^6 t$	<5.3%
Standard deviations of the samples for $Vin = 0.02sin20 \times 10^6 t$	< 2mV
Sampling module's SNDR at 100MHz	58dB
Sampling module's SNDR at 2.7GHz	35dB
-3dB bandwidth of the track and hold circuit	4.8GHz

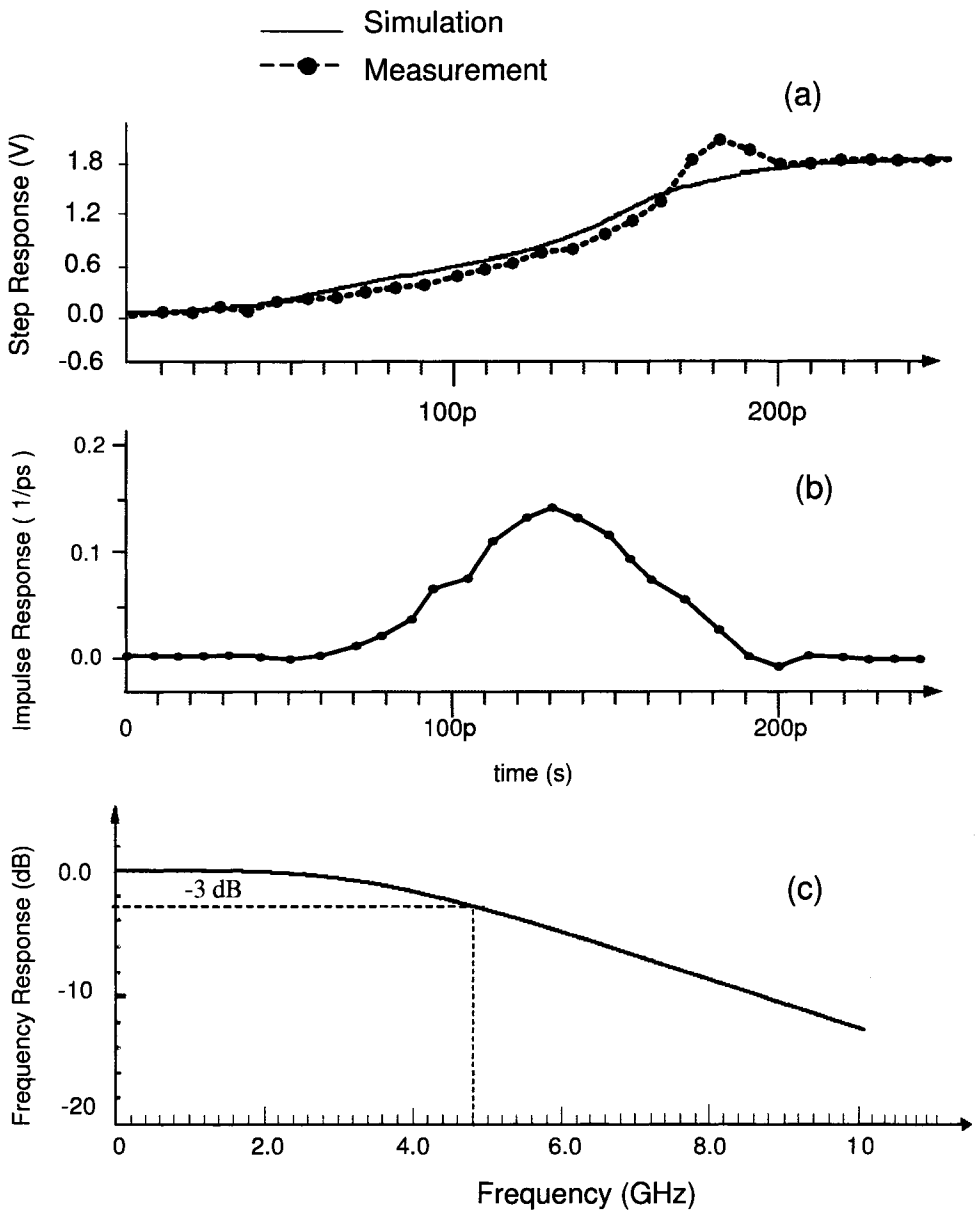

Figure 101: (a) Measured and simulated samples of T/H the step response. (b) Impulse response of the sampling scheme determined from the measured step response. (c) Frequency response of the sampler obtained from the impulse response.

7.4 Summary

The measured sampling error for $V_{in} = 0.02sin(2\pi 20 \times 10^6 t)$ has a mean error value of 1.05 mV which represents 5.25% of the peak value of the input signal. The amplitude and power spectrum of the output of the T/H circuit were computed and SNDR and Spurious Free Dynamic Range (SFDR) were found to be 31.3 dB and 38.7 dB respectively. Experiments were repeated for various frequencies in the range of 100MHz-2.2GHZ. For an input signal of 1.8 V_{pp} the measurement scheme supports over 44.3 dB SNDR up to an input frequency of 1.6 GHz which corresponds to over 7.0 effective bits linearity. It was concluded that the distortion increases with higher input amplitude and frequency.

The step response of the T/H circuit was measured and used to determine the corresponding impulse response. From the impulse response the frequency response of the T/H circuit was computed by taking the FFT. The frequency response of the T/H circuit shows -3dB bandwidth of 4.8 GHz.

CHAPTER VIII

CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

A test methodology utilizing an embedded tester core that enables the testing of analog/RF circuits in a mixed-signal System-on-Chip implementation has been developed. The proposed method uses coherent modulation and subsampling techniques to provide a high frequency testing capability that overcomes the inherent bandwidth limitations of SoC I/O signal paths, including the I/O pads. The test methodology eliminates the need for a complex test interface required to minimize transmission line effects and does not require the use of advanced external automatic test equipment to perform tests on the internal analogue RF cores.

Extensive simulations were carried out to ensure the validity of the proposed test methodology and the design of the embedded tester core. Simulation examples to demonstrate the test methodology and the expected results were provided for an RF oscillator and a low noise amplifier. It was shown that the embedded tester core can be employed to carry out advanced test functions such as a two-tone test that is used to locate the third order intercept point (IP3) of RF circuits.

A prototype of the embedded tester core has been designed and fabricated in CMOS 0.18 μm technology. The resulting embedded tester core has an area of 1 mm^2 of silicon. A test fixture for the embedded tester implementation has been obtained from CMC Microsystems to facilitate making the experimental measurements.

The measurement results performed on the prototype show that the tester was able to coherently subsample a sinewave input of 20 mV peak amplitude with less than 2 mV RMS error from the ideal simulated values. From the signal to noise plus distortion measurements, it was concluded that the tester supports 44.3 dB SNDR for input signals of 1.8 V peak-to-peak up to a maximum frequency of 1.6 GHz. This value of SNDR corresponds to over 7.0 effective bits linearity. The frequency response obtained from the step response of the sampling circuitry showed that the -3dB bandwidth of the CMOS T/H circuit and associated signal paths lies at 4.8 GHz.

8.2 Future Work

To test a CUT in a mixed-signal SoC environment, in addition to resources for stimulus generation and response evaluation, a test access mechanism is required to carry stimulus signals to multiple CUTs and receive their responses. The focus of this research work was to develop on-chip resources to carry out at-speed testing of RF/analog cores. It is assumed that the stimulus signals are applied directly to the CUT and responses are captured by the tester without any significant degradation. However, the transmission path, if poorly designed, can undermine the signal integrity. Using a dedicated signal path for each CUT is labor intensive and can cause routing problems if the number of CUTs becomes large. To deal with this problem the IEEE P1500 standard, developed as BIST for mixed-signal devices, can be used to establish the connectivity between the tester and the CUT. The effect of the IEEE P1500 transmission paths on high speed signals and the embedded tester's interaction with the CUT through IEEE P1500 architecture can be an attractive topic for future research.

Appendix I

RTL Codes Representing Digital Modules

//16-to-1 MULTIPLEXER

‘timescale 100ps/10ps

module MUX16To1 (sel,in,out);

input [3:0] sel;

input [15:0] in ;

output out;

reg out;

always @(sel)

begin

case (sel)

4’b0000: out = in[0];

4’b0001: out = in[1];

4’b0010: out = in[2];

4’b0011: out = in[3];

4’b0100: out = in[4];

4’b0101: out = in[5];

4’b0110: out = in[6];

4’b0111: out = in[7];

4’b1000: out = in[8];

4’b1001: out = in[9];

4’b1010: out = in[10];

```
4'b1011: out = in[11];
4'b1100: out = in[12];
4'b1101: out = in[13];
4'b1110: out = in[14];
4'b1111: out = in[15];
endcase
end
endmodule
```

// 10-BIT COUNTER

```
'timescale 100ps/10ps
module RippleCounter(q, clk, N, out);
output [9:0] q;
output out;
reg out;
input clk;
wire reset;
input [9:0] N;
assign reset=out;
TFF tff0(q[0], clk, reset);
TFF tff1(q[1], q[0], reset);
TFF tff2(q[2], q[1], reset);
TFF tff3(q[3], q[2], reset);
TFF tff4(q[4], q[3], reset);
TFF tff5(q[5], q[4], reset);
TFF tff6(q[6], q[5], reset);
```

```
TFF tff7(q[7], q[6], reset);
TFF tff8(q[8], q[7], reset);
TFF tff9(q[9], q[8], reset);
always @ (posedge clk)
if ( q==N ) out¡=1; else out¡=0;
endmodule

    module TFF(q, clk, reset);
output q;
input clk, reset;
wire d;
DFF dff0(q, d, clk, reset);
not n1(d,q);
endmodule

   module DFF(q, d, clk, reset);
output q;
input d, clk, reset; reg q;
always @ (posedge clk)
if (reset)
q<= 1'b0;
else
q¡= d;
endmodule
```

// COMPARATOR

```
'timescale 100ps/10ps
module Compare(In1, In2, out, clock);
output out;
input [9:0] In1,In2;
input clock;
reg out;
always @(posedge clock)
begin
if (In1 == In2) out <= 1;
else out <= 0;
end
endmodule
```

// SERIAL-TO-PARALLEL CONVERTER

```
'timescale 100ps/10ps
module SerConv(Sin, clk, Pout);
output [19:0] Pout;
reg [19:0] Pout;
input Sin,clk;
always @(posedge clk)
begin Pout <= Pout<<1;
Pout[0] <= Sin;
end
endmodule
```

Appendix II

Measured Samples and Experimental Equipments

The following equipments were used to setup the measurement environment according to the IEEE standard for ADC converters in order to perform a sine wave test.

1. DC power supply - BK precision 1760A
2. Signal Generator - BK precision 4070A DC to 21.5MHz waveforms
3. Digital Sampling Oscilloscope - Tektronix TDS 1002
4. Spectrum Analyzer- Tektronix 2710 10KHz- 1.8GHz
5. Fixture Interface Board - CFP80TF provided by CMC
6. HP 34401 Digital Multimeter
7. Digital Interface Board
8. Personal Computer

The measurement results for a test case in which a sinusoidal waveform of $V_{in} = 0.02sin(2\pi 20 \times 10^6 t)$ is applied to the tester core are shown below. A total number of 64 sample sets of the applied waveform are obtained through coherent sampling. Each sample point is determined by taking the average of five measurement readings for increased accuracy. All the measured samples shown below are expressed in Volt.

Sample Sets of $V_{in} = 0.02sin(2\pi 20 \times 10^6 t)$ ***Collected Over One Period***

Sample sets 1 through 7

	0.0011	0.0030	0.0051	0.0074	0.0084	0.0090	0.0117
	0.0016	0.0027	0.0035	0.0055	0.0080	0.0096	0.0109
	-0.0010	0.0027	0.0047	0.0066	0.0094	0.0096	0.0127
	-0.0003	0.0041	0.0032	0.0069	0.0088	0.0094	0.0119
	0.0008	0.0036	0.0040	0.0053	0.0106	0.0108	0.0128
Mean	0.0004	0.0032	0.0041	0.0064	0.0090	0.0097	0.0120

Sample sets 8 through 14

	0.0111	0.0156	0.0153	0.0172	0.0197	0.0179	0.0180
	0.0145	0.0126	0.0162	0.0160	0.0183	0.0170	0.0201
	0.0110	0.0154	0.0150	0.0178	0.0191	0.0188	0.0176
	0.0139	0.0151	0.0159	0.0191	0.0172	0.0180	0.0189
	0.0135	0.0131	0.0166	0.0164	0.0181	0.0193	0.0192
Mean	0.0128	0.0144	0.0158	0.0173	0.0185	0.0182	0.0188

Sample sets 15 through 21

	0.0180	0.0218	0.0194	0.0213	0.0218	0.0178	0.0211
	0.0206	0.0215	0.0196	0.0204	0.0195	0.0189	0.0186
	0.0204	0.0206	0.0214	0.0195	0.0209	0.0196	0.0185
	0.0214	0.0197	0.0231	0.0215	0.0202	0.0215	0.0205
	0.0191	0.0220	0.0205	0.0214	0.0197	0.0208	0.0168
Mean	0.0199	0.0211	0.0208	0.0208	0.0204	0.0197	0.0191

Samples of $V_{in} = 0.02sin(2\pi 20 \times 10^6 t)$

Sample sets 22 through 28

	0.0176	0.0152	0.0148	0.0140	0.0122	0.0112	0.0088
	0.0182	0.0172	0.0157	0.0160	0.0134	0.0127	0.0087
	0.0184	0.0184	0.0164	0.0148	0.0150	0.0125	0.0097
	0.0167	0.0163	0.0153	0.0149	0.0136	0.0104	0.0109
	0.0183	0.0162	0.0175	0.0148	0.0139	0.0116	0.0098
Mean	0.0179	0.0167	0.0159	0.0149	0.0136	0.0117	0.0096

Sample sets 29 through 35

	0.0082	0.0065	0.0047	0.0008	0.0008	-0.0021	-0.0036
	0.0096	0.0050	0.0042	0.0028	0.0003	-0.0006	-0.0027
	0.0085	0.0062	0.0051	0.0029	-0.0012	-0.0026	-0.0019
	0.0067	0.0066	0.0045	0.0008	0.0031	0.0003	-0.0047
	0.0074	0.0062	0.0044	0.0016	0.0000	-0.0004	-0.0039
Mean	0.0081	0.0061	0.0046	0.0018	0.0006	-0.0011	-0.0034

Sample sets 36 through 42

	-0.0061	-0.0069	-0.0109	-0.0113	-0.0134	-0.0156	-0.0152
	-0.0059	-0.0077	-0.0095	-0.0112	-0.0120	-0.0127	-0.0155
	-0.0049	-0.0048	-0.0072	-0.0113	-0.0125	-0.0125	-0.0129
	-0.0046	-0.0062	-0.0078	-0.0112	-0.0123	-0.0134	-0.0164
	-0.0043	-0.0086	-0.0082	-0.0113	-0.0130	-0.0133	-0.0153
Mean	-0.0051	-0.0068	-0.0087	-0.0113	-0.0127	-0.0135	-0.0151

Samples of $V_{in} = 0.02sin(2\pi 20 \times 10^6 t)$

Sample sets 43 through 49

	-0.0166	-0.0184	-0.0165	-0.0178	-0.0177	-0.0209	-0.0193
	-0.0146	-0.0183	-0.0191	-0.0183	-0.0193	-0.0198	-0.0187
	-0.0149	-0.0183	-0.0176	-0.0184	-0.0176	-0.0193	-0.0201
	-0.0162	-0.0187	-0.0171	-0.0194	-0.0208	-0.0197	-0.0199
	-0.0173	-0.0170	-0.0176	-0.0176	-0.0193	-0.0194	-0.0196
Mean	-0.0159	-0.0181	-0.0176	-0.0183	-0.0189	-0.0198	-0.0195

Sample sets 50 through 56

	-0.0186	-0.0190	-0.0172	-0.0184	-0.0183	-0.0170	-0.0127
	-0.0195	-0.0185	-0.0173	-0.0185	-0.0160	-0.0163	-0.0128
	-0.0193	-0.0178	-0.0195	-0.0174	-0.0171	-0.0156	-0.0162
	-0.0203	-0.0182	-0.0185	-0.0184	-0.0173	-0.0162	-0.0146
	-0.0183	-0.0184	-0.0194	-0.0186	-0.0155	-0.0166	-0.0151
Mean	-0.0192	-0.0184	-0.0184	-0.0183	-0.0168	-0.0163	-0.0143

Sample sets 57 through 64

	-0.0141	-0.0130	-0.0100	-0.0096	-0.0067	-0.0049	-0.0040	-0.0006
	-0.0147	-0.0126	-0.0111	-0.0080	-0.0077	-0.0052	-0.0029	-0.0024
	-0.0138	-0.0123	-0.0110	-0.0087	-0.0061	-0.0040	-0.0033	-0.0028
	-0.0128	-0.0116	-0.0109	-0.0086	-0.0069	-0.0060	-0.0033	-0.0025
	-0.0135	-0.0122	-0.0098	-0.0087	-0.0065	-0.0054	-0.0027	-0.0017
Mean	-0.0138	-0.0124	-0.0106	-0.0087	-0.0068	-0.0051	-0.0032	-0.0020

Appendix III

List of Abbreviations

ATE - Automatic Test Equipment. An automated, usually computer-driven, approach to testing semiconductors, electronic circuits, and printed circuit board assemblies.

ATPG - Automatic Test Pattern Generator - Tool-based approach to generate test pattern that relies heavily on the design database and
netlist.

BILBO - A BILBO is a multitalented logic circuit that can be a state register, a scan register, an LFSR, or a MISR depending on the state of it's mode pins. BILBOs are sometimes used to cascade large combinational logic blocks in a BIST engine.

BIST - (Built in Self Test) BIST essentially builds tiny tester models onto the integrated circuit so that it can test itself.

Boundary Scan - Generic term for IEEE 1149.1. It is a

methodology allowing complete controllability and observability of the boundary (I/O) pins via a standard interface.

CP - (Charge Pump) A circuit that consists of two switched current sources that pump charge into or out of a capacitance to increase or decrease the control voltage of a phase locked loop.

Channel - The tester functions and the path through a pin-group card and test fixture dedicated to one DUT pin.

CAD - Computer Aided Design

Crosstalk - A phenomenon in which one or more signals interfere with another signal.

Defect(s) - Term used to reference specific flaw(s); physical or chemical imperfection, on a manufactured device. Most defects can be detected and measured by a Failure Analysis group. Specific devices that do not perform as expected contain defect(s) or have Design flaws.

DFT - (Design For Test) Design For Test is the practice of adding hardware hooks to integrated circuits in order to facilitate effective, inexpensive testing.

Die - A piece of semiconductor with circuitry fabricated on it; one location on a wafer; compare chip.

DLL - (Delay-Locked Loop) A circuit similar to a phase-locked loop with a voltage controlled delay line instead of a voltage controlled oscillator.

DUT - (Device Under Test) This is the target device being tested. Less frequently referred to as "CUT" (circuit under test).

EDA - electronic design automation. EDA refers to the design tools and environment utilized to render the logic, schematics, insert scan, insert BIST, etc. for a new chip design.

FFT - Fast Fourier Transform

Fault(s) - This term is used in reference to classes, or concepts, of defect types. The most common of these is the stuck at type, or fault class. In the EDA and academic worlds, a fault is a software model of a defect, or class of defects.

Fault Coverage - Quality measure for a test or set of tests, based on the percentage of actually detected faults (defects) versus the total number of theoretically detectable faults,on a particular fault model. A coverage figure should be given for each model type tested. As the operator defines the nodes to be evaluated (in some cases this is done by defining lists of nodes not to be used in the task) the raw number has little meaning without a full analysis of the set up.

Functional test - A process that applies pattern vectors to a device and checks the output to determine that the device is operating according to its truth table.

Jitter - A slight movement of a transmission signal edges from their ideal location in time that can introduce errors and loss of synchronization.

Hard fault - A hard fault is a potential open or short circuit in the design modeling the effects of manufacturing defects on the network connects.

I/O channel - An input/output tester port that is capable of both stimulating a device pin and monitoring a response from the same pin.

IP3 - Third order intercept point is the point at which the linear extrapolation (as a function of input power) of linear output power and third-order distortion power level meet

JTAG - (Joint Test Action Group) Originally, the name of the team, the term has come to be associated with the output of the team. JTAG is now essentially synonymous with the IEEE 1149.1 standard for Test Access Port and Boundary Scan.

LNA - Low Noise Amplifier

LPF - Low Pass Filter

LFSR - (Linear Feedback Shift Register) LFSRs are shift registers with exclusive-OR gates that allow some bits in the register (usually referred to as a polynomial) to feed back into selected points within the register. LFSRs are often used in BISTed designs to form PRPGs and MISRs.

MISR - (Multiple Input Shift Register) Also known as Multiple Input Signature Register. MISRs are simply LFSRs configured as signature analyzers. MISRs are often used on the back end of BIST engines to capture and compress output sequences from a circuit under test.

P1500 - IEEE standard for test wrappers (common -scan like test structures "wrapped around SOC cores).

Parametric faults - These faults are caused by variations in component parameter values produced by process or environmental changes.

PFD - (Phase Frequency Detector) A device that compares the phase of two input signals. It has two inputs which correspond to two different input signals, usually one from a voltage-controlled oscillator (VCO) and another from some external source

Pin-Electronics- One of the main section of automatic test equipment, where the stimulus data are applied to the device under test and its responses are captured

PLL - (Phase Locked Loop) An electronic circuit t hat controls an oscillator so that it maintains a constant phase angle (ie, lock) on the frequency of an input signal.

SNDR (Signal to Noise and Distortion Ratio) indicates in dB the ratio between the powers of the converted main signal and the sum of the noise
and the generated harmonic spurs

Soft fault (parametric fault) - Any fault caused by a parametric or Scan Chain - Serial organization of scan elements such that the first element of the chain is at a device input and the last element of the chain is at a device output. Devices may use single or multiple scan chains to 'capture' all of the scannable nodes.

SoC - (System on a Chip) Practice of integrating one or more processor cores, embedded memories, peripheral interfaces, and sometimes mixed signal circuits onto a single chip to form a complete (or nearly complete) system.

Soft fault (parametric fault) - Any fault caused by a parametric or process variation outside of tolerance or nominal values is called a soft fault.

Stimulus - An input signal which imitates action or reaction in a circuit, such as voltage or current.

Structural Testing - Strategy of testing integrated circuits that focuses on detecting manufacturing defects. Unlike functional or behavioral testing, defects are targeted directly.

TAP - (Test Access Port - pronounced "tap") Part of the JTAG standard, the TAP is a 4 (or optionally 5) pin port to enable boundary scan.

T/H - Track and Hold

Test protocol - A sequence of control operations required to perform a test. At the lowest level a test protocol is just a series of logic 0 and 1 applied to specified test control ports. It will typically also contain symbolic references to the test data that is to be applied to or observed at specified test data or system data ports. Test protocols involve the activation of one or more test modes and may also contain pre-conditioning and post-conditioning functions or sequences.

VCO - (Voltage Controlled Oscillator) A circuit which can change its output frequency based on the voltage level applied to its input.

VCDL - (Voltage Controlled Delay Line) A circuit which can change its output delay based on the voltage level applied to its input.

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Ontario Graduate Scholarship in Science and Technology (OGSST)	Provincial	Research	University of Windsor	2004/09 - 2005/09
Tuition Fee Scholarship	Institutional	Academic	University of Windsor	2004/09 - 2005/09
Tuition Fee Scholarship	Institutional	Academic	University of Windsor	2003/09 - 2004/09
In Course Bursary	Institutional	Academic	University of Windsor	2002/09 - 2002/12
Kharazmi Award	National	Research	Iran Telecomm. Research Center (ITRC)	1998/06 - 1999/06

Teaching Experience

Guest Instructor

Course Code	Course Name	Nature	Date
88-433	Digital Integrated Circuit Design	Undergraduate	May-Aug. 2002

Teaching Assistant

Course Code	Course Name	Nature	Date
88-313	Electromechanical Systems1 Circuit Design	Undergraduate	Sep.-Dec. 2001
88-226	Electronics I	Undergraduate	Sep.-Dec. 2002
88-457	Digital Signal Processing	Undergraduate	Jan.-Apr. 2003
88-435	Microeletromechanical systems	Undergraduate	May-Aug. 2003
88-431	Control-II	Undergraduate	Jan.-Apr. 2004
88-327	Microprocessors	Undergraduate	May-Aug. 2004
88-217	Digital logic design	Undergraduate	Sep.-Dec. 2004
88-327	Microprocessors	Undergraduate	May-Aug. 2005
88-217	Digital logic design	Undergraduate	Sep.-Dec. 2005
88-327	Microprocessors	Undergraduate	May-Aug. 2006
88-217	Digital logic design	Undergraduate	Sep.-Dec. 2006

Professional Memberships

2004 - Present	Professional Engineers Ontario (PEO)
2003 - Present	Institute of Electrical and Electronics Engineers (IEEE)

Publications

Journal Papers

1. R. Rashidzadeh, M. Ahmadi, W. C. Miller, "On-Chip Measurement of Waveforms in Mixed Signal Circuits Using Segmented Sampling Technique," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 50, no. 2, pp. 105-113, Feb. 2007.

2. R. Rashidzadeh, M.Ahmadi, W. C. Miller, " Test and Measurement of Analog and RF Cores in Mixed-Signal SoC Environment," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (Accepted on Dec. 25, 2006).

Conference Proceedings

1. R. Rashidzadeh, W. C. Miller, M. Ahmadi, "A PLL Based Analog Tester Core", IEEE Canadian Conference on Electrical and Computer Engineering, Saskatoon, 2005, pp. 824 - 827.

2. R. Rashidzadeh, M. Ahmadi, W. C. Miller, "An IP Tester Core for SoC RF Circuits, " Proceedings of Micronet R & D Annual Workshop, Ottawa, 2005, pp. 69-70.

3. R. Rashidzadeh, M. Ahmadi, W. C. Miller, "An Embedded Tester Core For System-on-Chip," Proceedings of 4th IEEE International Workshop on System-on-Chip for Real-Time Applications, Banff, Canada, 2004, pp. 105-108.

4. R. Rashidzadeh, M. Ahmadi, W.C. Miller, "A Tester-on-Chip Implementation in 0.18μm CMOS Utilizing A MEMS Interface," IEEE International Symposium on Circuits and Systems, Bangkok, Thailand, 2003, vol. 5, pp. V561-V564.

Papers Presented at Special Workshops and Symposia

1. R. Rashidzadeh, M. Ahmadi, G.A. Jullien and W.C. Miller, "An Embedded Tester IP-Core For SoC Environment," Proceedings of Micronet R & D Annual Workshop, Aylmer, Canada, 2004, pp. 97-98.

2. R. Rashidzadeh, M. Ahmadi, W. C. Miller, G.A. Jullien, (2003) "A Tester-on-Chip and A MEMS Interface," Proceedings of Micronet R & D Annual Workshop, Toronto, Canada, 2003, pp. 100-101.

3. R. Rashidzadeh, W.C. Miller, M. Ahmadi, " A Digital Tester Architecture For a System-on-Chip Implementation," presented at Symposium on Microelectronics Research & Development in Canada, Montreal, June 18, 2003.

Chip Fabrications

1. An analog/RF tester core for mixed signal ICs operating in the range of 1.1GHz-2.7GHz, occupying $1mm^2$ in CMOS 0.18m technology.

2. Rail to Rail high speed OpAmp occupying $0.3mm^2$ in CMOS 0.35m technology.

Industrial Experience

Position: Senior Research Engineer

Institution: Iran Telecommunication Research Center (A major research institution with well over 600 engineers and researchers - www.itrc.ac.ir)

Period: 1995-Aug. 2000

Supervisor: Dr. A. Khademzadeh

- Actively participated in designing of an advanced Automatic Test Equipment (ATE) supporting test on mixed signal boards with automatic learning option for unknown ICs. The final project (Mizan 3000) received the Kharazmi award in 1998, which is the most prestigious national prize for outstanding accomplishments in engineering research and development presented annually, in person, by the president of Iran.

- Managed a group of 5-7 engineers designing a Private Automatic Branch Exchange (PABX) systems. Led the creation of a cost effective modular system, which lowered the cost of PABX manufacturing by more than 15%. This product is in the market now and serves over 200,000 telephone subscribers.

- Supervised and supported engineers working on subscriber line interface circuits (SLIC) for modem interface.

- Experienced working with advanced test and measurement equipment such as HP 8560EC spectrum analyzer, HP 16500 logic analyzer and Rohde & Schwarz network analyzer.

Position: Test Engineer

Institution: Iran Telecommunication Research Center

Period: Feb.1989-Aug. 1995

Supervisor: Mr. E. H. Nejad

- Designed embedded systems for various telecommunication systems using microprocessors, microcontrollers, reduced instruction processors and digital switch arrays.
- Improved the speed and economics of functional testing by automating some of the processes involved like test vector generation, fault detection, results analysis and reporting.
- Configured and programmed Teradyne board tester and trained users for board testing. Developed interface boards and test jigs for various communication modules.
- Board level testing, diagnosing and repairing of Digital/RF products.
- Prepared technical documents, diagrams and schematics of communication systems. Troubleshooting and repairing digital and or analog systems to the component level.