2004

A 12-bit, 40 msamples/s, low-power, low-area pipeline analog-to-digital converter in CMOS 0.18 mum technology.

Mani Mohajerin
University of Windsor

A 12-Bit, 40 Msamples/s, Low-Power, Low-Area Pipeline Analog-to-Digital Converter in CMOS 0.18 μm Technology

By
Mani Mohajerin

A Thesis
Submitted to the Faculty of Graduate Studies and Research
through the Department of Electrical and Computer Engineering
in Partial Fulfillment of the Requirements for
the Degree of Master of Applied Science at the
University of Windsor

Windsor, Ontario, Canada
2004

Your file Votre référence
ISBN: 0-612-92500-5
Our file Notre référence
ISBN: 0-612-92500-5

Abstract

With advancements in digital signal processing in recent years, the need for high-speed, high-resolution analog-to-digital converters (ADCs) which can be used in the analog front-end has been increasing. Some examples of these applications are image and video signal processing, wireless communications and asymmetrical digital subscriber line (ADSL). In CMOS integrated circuit design, it is desirable to integrate the digital circuit and the ADC in one microchip to reduce the cost of fabrication. Consequently the power dissipation and area of the ADCs are important design factors.

The original contributions in this thesis are as follows. Since the performance of pipeline ADCs significantly depends on the op-amps and comparators circuits, the performance of various comparators is analyzed and the effect of op-amp topology on the performance of pipeline ADCs is investigated. This thesis also presents a novel architecture for design of low-power and low-area pipelined ADCs which will be more useful for very low-voltage applications in the future. At the schematic level, a low-power CMOS implementation of the current-mode MDAC is presented and an improved voltage comparator is designed. With the proposed design and the optimization methodology it is possible to reduce power dissipation and area compared with conventional fully differential schemes.

Dedications

To my parents for their love and support.

Acknowledgements

It has been a real privilege to be a graduate student in the ECE department at the University of Windsor. One of the real assets of the ECE department is the standard facilities for research in the field of VLSI design. My experience here has been full of opportunities to learn from faculties and students.

I would like to express my sincere gratitude to my supervisors Dr. Chunhong Chen and Dr. Esam Abdel-Raheem who have guided and supported me throughout my research and for preparation of this thesis.

I also thank my committee members, Dr. Huapeng Wu and Dr. David Ting for their valuable comments and suggestions and for reviewing this thesis.

Table of Contents

List of Tables

List of Figures

List of Abbreviations

A	Amplitude, area, amplifier voltage gain
A/D	Analog-to-digital
ADC	Analog-to-digital converter
C	Capacitance
C_L	Load capacitance
CMFB	Common mode feedback
CMOS	Complementary metal oxide semiconductor
C_{out}	Parasitic output capacitance
C_{ox}	Gate-oxide capacitance
D	Differential
D/A	Digital-to-analog
DAC	Digital-to-analog converter
DNL	Differential nonlinearity
E	Error
ENOB	Effective number of bits
FFT	Fast Fourier transform
F_{in}	Input frequency
FOM	Figure of merit
F_S	Sampling frequency
g_m	Transconductance
i	Stage index
IC	Integrated circuit
I_D	Drain current

IF	Intermediate Frequency
INL	Integral nonlinearity
INL	Integral nonlinearity
k	Boltzmann's coefficient
L	Channel length
MDAC	Multiplying digital-to-analog converter
MSB	Most significant bit
μ	Carrier mobility
N	Number of bits
NMOS	n-channel metal oxide semiconductor
P	Power dissipation
PD	Pseudo-differential
PMOS	p-channel metal oxide semiconductor
R_{on}	Switch on-resistance
S	Single ended
SC	Switched capacitor
SFDR	Spurious free dynamic range
S/H	Sample-and-hold
SNDR	Signal-to-noise and distortion ratio
SNR	Signal-to-noise ratio
T	Absolute temperature,
THD	Total harmonic distortion
V_{DD}	Positive supply voltage
V_{ds}	Drain-source voltage

V_{gs}	Gate-source voltage
V_{in}	Input voltage
V_{LSB}	Voltage corresponding to the least significant bit
VLSI	Very large-scale integrated circuit
V_{pp}	Volts peak-to-peak
V_{TH}	Threshold voltage
W	Channel width

Chapter 1

Introduction

1.1 Motivation

The quality and performance of the modern electronics devices require extensive digital signal processing. High-definition television, multimedia systems, wireless communication systems, radar systems, modems, control systems are some examples where digital signal processing is mandatory.

Data converters are required for the interface between analog circuits and digital circuits. Figure 1.1 shows the general digital signal processing systems.

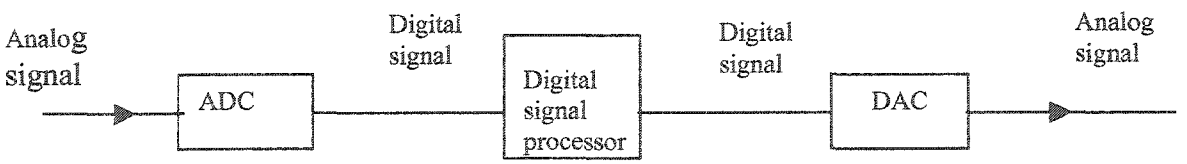


Figure 1.1: General Digital Signal Processing Systems

As CMOS technology enables manufacturing of battery-powered and portable devices by scaling down the size of transistors and supply voltage, the need for low-power design techniques becomes more demanding. Consequently design of high-speed and low-power

ADCs is vital for modern electronics devices. The pipeline ADCs are suitable for low-power and high-speed applications and therefore it is the natural choice for these applications.

1.2 Research focus

The tradeoff between speed, resolution and power dissipation makes the design of ADCs a multidimensional design and challenging. Although the conventional pipeline ADCs allow high conversion rate with high accuracy, the low-voltage design limitations bring new challenges. In fact it is known that reducing supply voltage will increase the power dissipation of pipeline ADCs when high signal to noise ratio is required [1]. Therefore developments of new low-voltage pipeline architectures, which allow power optimization is essential. In this thesis, the main focus is to develop such an architecture, which will lead to power optimization of pipeline ADCs.

1.3 Thesis organization

This thesis presents a theoretical study and design of a novel pipeline ADC architecture as well as circuit techniques developed during the course of this research.

Chapter 2 reviews applications of ADCs and conventional ADC architectures. The ADCs performance parameters and Figures of merit used to evaluate the overall performance of ADCs are also described.

Chapter 3 describes the general design considerations at the architecture level in pipeline ADCs such as effect of non-idealities, digital correction logic and redundancy.

Chapter 4 presents circuit level design of various building blocks used in pipeline ADCs. Also theoretical analysis is performed on performance of various building blocks such as comparators and op-amps.

Chapter 5 introduces a novel pipeline architecture and design and performance evaluation of a 12-bit, low-power and low-area pipeline ADC. Finally the conclusions and future works are given in chapter 6.

Chapter 2

Analog to digital conversion techniques

2.1 Introduction

As shown in Figure 2.1 an n-bit analog-to-digital converter, converts the input signal V_{in} to a digital binary output with respect to the reference voltage (V_{ref}). The reference voltage defines the input range of the ADC. Mathematically the relation between input and output is given by:

$$V_{in} \approx V_{ref}(Bit_1 2^{-1} + Bit_2 2^{-2} + \ldots + Bit_n 2^{-n}) \qquad (2.1)$$

The main requirements for ADCs are accuracy, speed, power dissipation and microchip area. Therefore there exist various conversion techniques for a given set of requirements. For example in some applications high speed and high accuracy are a must while the power dissipation is not an important design consideration. An example of such applications is some of the high-speed data acquisition systems [2]. On the other hand there are some devices, which require very low-power dissipation and reasonable accuracy, but the high conversion rate is not needed, such as hearing aids devices [3]. In this chapter various data conversion techniques and their applications are discussed.

In order to assess the performance and accuracy of analog-to-digital converters, a number of parameters are used. This chapter also presents the static and dynamic parameters. Finally, two of the well-known figure-of-merits (FOM) which are used to evaluate the overall performance of ADCs are given.

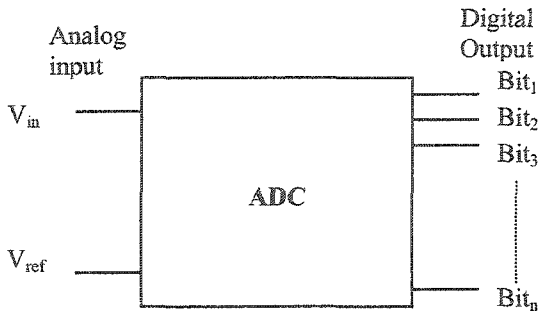


Figure 2.1: Block diagram of an n-bit ADC

2.2 Successive approximation

The successive approximation ADC works similar to a binary search algorithm [4]. The binary search begins with the most significant bit and goes toward the least significant bit. As shown in Figure 2.2, first the input signal is sampled and held. The output of the comparator is set to 1 if input is greater than the digital to analog converter's (DAC) output and 0 otherwise. The successive approximation register (SAR) will store the intermediate bits. The advantages of successive approximation ADCs are their high resolution, simple circuitry and small area and low power dissipation, however it is difficult to achieve high conversion rate due to the feedback. Also the accuracy is limited by performance of the comparator and DAC. The successive approximation is used often

in portable and battery powered devices, which do not require high conversion rate. The achievable resolution and speed are up to 20 bits and 10KHZ-1MHZ, respectively.

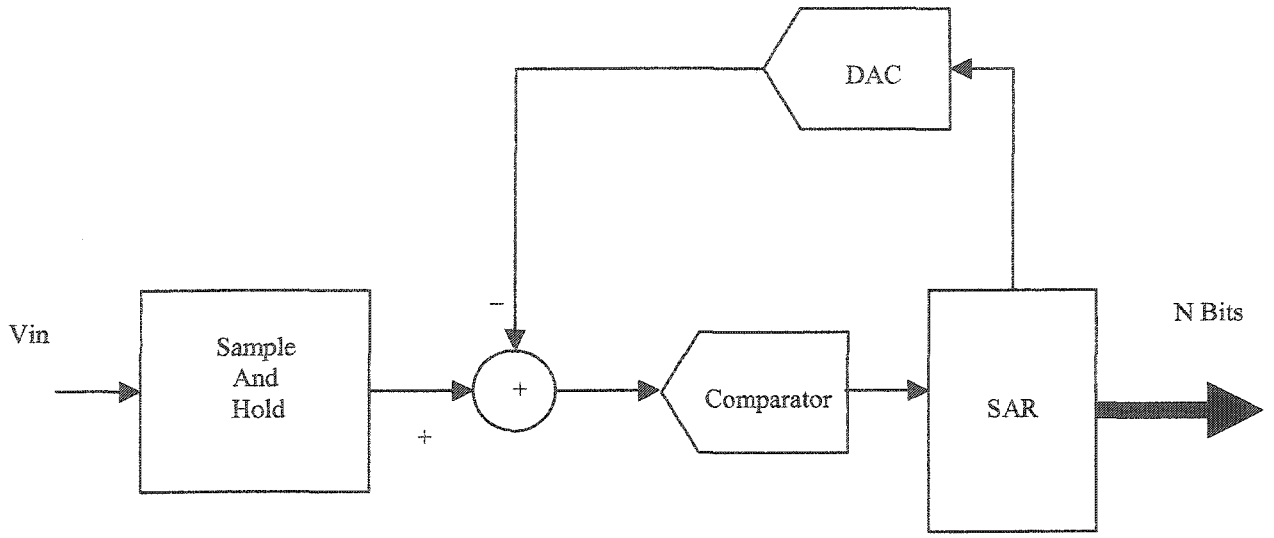


Figure 2.2: The successive approximation ADC architecture.

2.3 Sigma-delta ADC

The general architecture of sigma-delta ADCs is shown in Figure 2.3 [5]. The input signal comes into the difference amplifier and passes through integrator. The comparator compares the integrator's output with ground and produces a 1 or 0. Comparator's output is fed to a digital filter and to a 1-bit DAC. The feedback loop forces the average of the signal to be equal to the input signal. The purpose of the integrator is noise shaping which reduces quantization error. Using sigma-delta ADCs, very high resolution (up to 24 bits) can be achieved, however the speed of recent sigma-delta ADCs is limited to about 1-MHZ. Therefore they are used in high precision devices such as weight scales and some hearing aids devices.

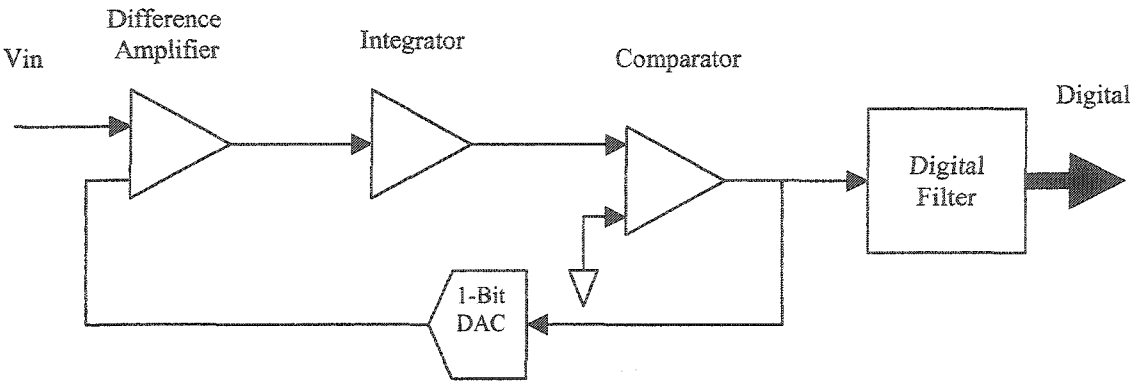


Figure 2.3: The general architecture of sigma-delta ADCs

2.4 Flash ADC

The flash architecture is the fastest possible way to convert analog signals to digital signals, due to its parallel architecture [4]. As shown in Figure 2.4, the input signal voltage is fed simultaneously to one of the inputs of each comparator which, their other inputs are connected to 2^N-1 equally spaced reference voltages. The outputs of all comparators are processed by a logic circuit to produce N bits at the output. Therefore to produce N bits, 2^N-1 comparators are required. The exponential relation between the resolution and number of comparators makes this architecture feasible for only low-resolution applications. Typical applications for flash ADCs are data acquisition and high-density disk drives with 4-8 bits, and up to 500MHZ sampling rate.

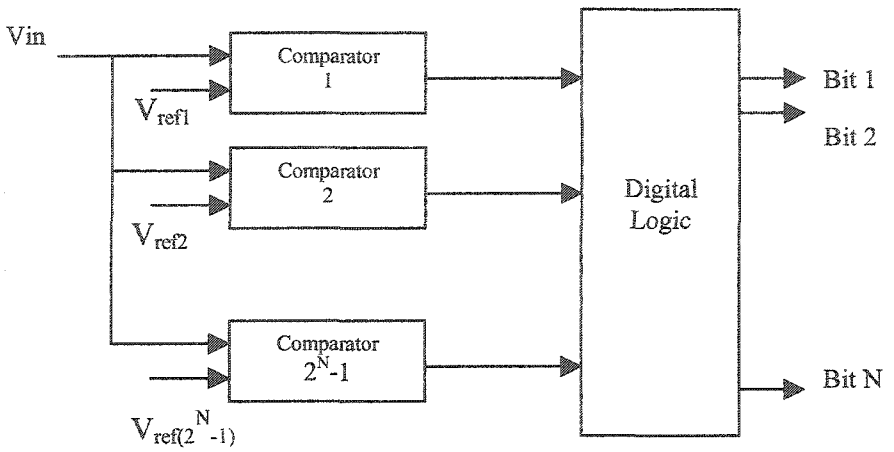


Figure 2.4: The flash architecture

2.5 Multi-step subranging ADC

The architecture of a 2N bit resolution subranging is shown in Figure 2.6. Input signal is sampled by the sample-and-hold (S/H) circuit. The first N-bit flash ADC produces the most N significant bits. Then the digital output is converted back to analog and subtracted from original input to produce a residue. The residue is amplified and is used by the second flash ADC to produce the other N least significant bits.

The advantage of the subranging ADC over the flash quantizer is the reduced number of comparators, therefore it consumes less power and area. However it requires high accuracy DAC, amplifier and subtracter. The performance of the subranging ADC is limited by the amplifier. Some of the applications are cellular phones, telecommunication and battery powered devices, however recently the pipeline ADCs are used more often

for these applications due to their superior performance. The speed of th the subranging ADCs is limited to100kHZ-10MHZ.

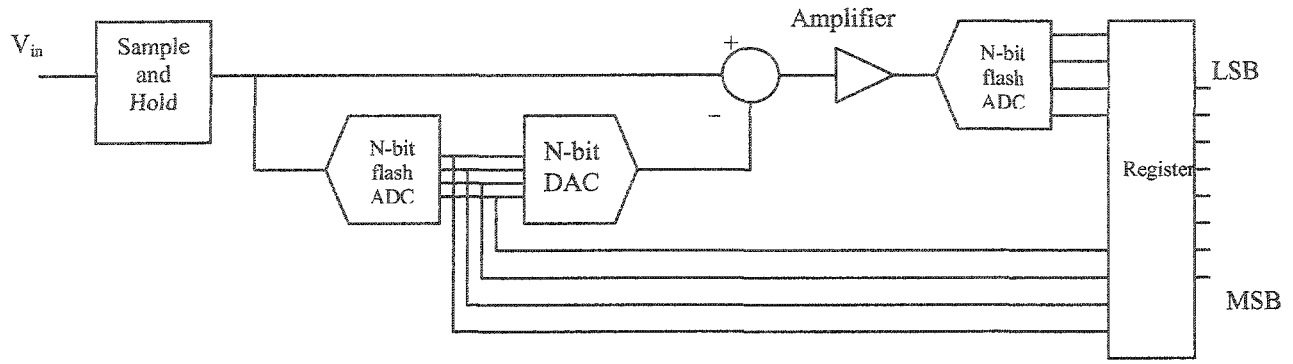


Figure 2.5: The architecture of a 2N-bit 2-step subranging ADC.

2.6 Pipelined ADC

The pipelined ADC is the same as the multi-step subranging with the difference that pipelining is applied to the architecture. Architecture of an N-bit pipeline ADC is shown Figure 2.6 [7]. The input is sampled and held by the S/H circuit. The sampled signal is processed by the first stage to produce digital outputs and the analog output. The digital output is stored in digital delay line and analog output is processed by the second stage. While the second stage is processing the analog output of the previous stage, the previous stage is processing a new sample. Each stage is in fact a low-resolution 2-step subranging ADC. Figure 2.7 shows the genetic architecture of the stages. The pipelining speeds up the conversion rate with relatively smaller power dissipation and area. Pipeline ADCs are used in a variety of applications, which require 1MHZ-100MHZ conversion rate with low power dissipation such as digital cameras, video recorders, ultrasonic, IF

digitization, asymmetrical digital subscriber (ADSL) and etc. In chapter 4 the architecture of pipeline ADCs will be discussed in greater details.

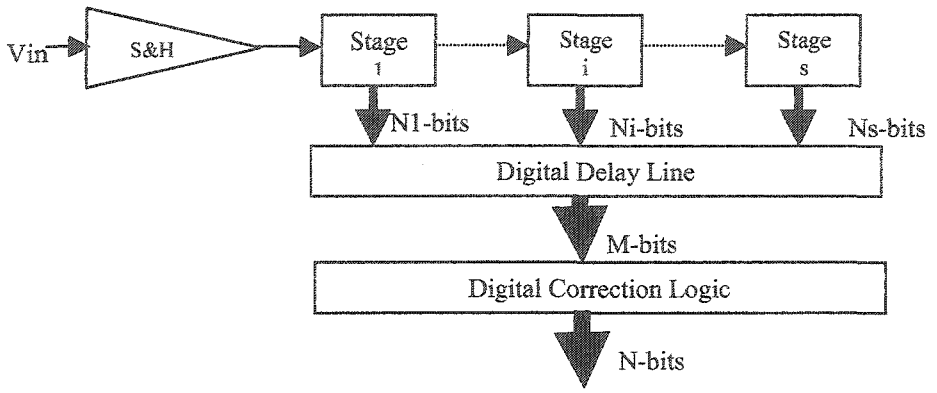


Figure 2.6: Generic architecture of pipeline ADCs

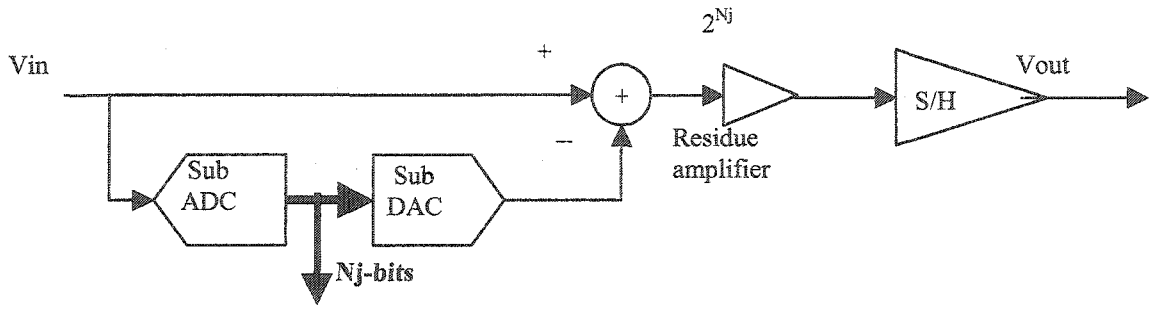


Figure 2.7: Generic architecture of stages.

2.7 Parallel pipeline ADC

Very high sampling rate and wide-band A/D conversion is required in wireless communication standards such as the Universal Telecommunication System (UMTS), Wireless Local Loop (WLL) and Local Multipoint Distribution Services (LMDS). By

applying parallelism to pipeline ADCs with equal resolution, the sampling rate can be increase [6]. Figure 2.8 shows the basic architecture for parallel pipeline ADCs. The sampling period is divided by the number of pipeline ADCs. At any given time, input signal is sampled and processed by one of the pipeline ADCs.

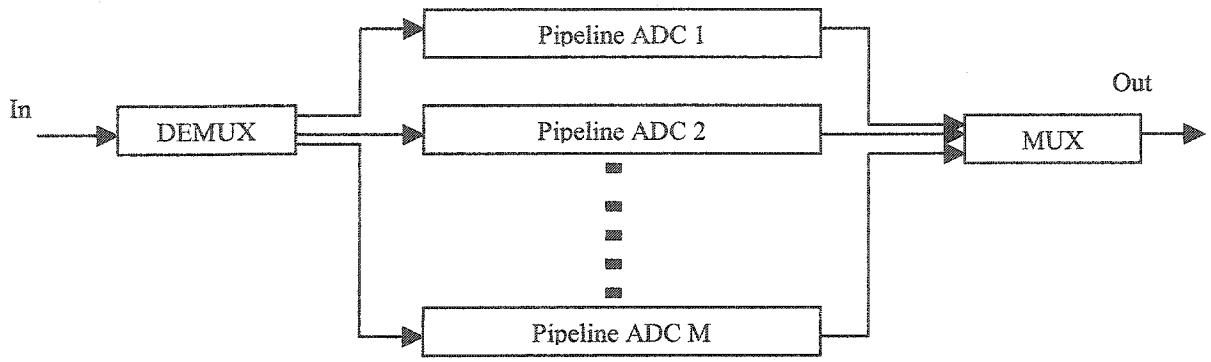


Figure 2.8: Parallel pipeline ADC with M channels.

2.8 Static parameters

In order to assess the static performance of the ADCs, a number of parameters are used. Figure 2.9 shows ideal and non-ideal input/output characteristics of a 3-bit ADC. For an ideal N-bit ADC with input range, $V_{in}=[0,V_{ref}]$, the transition voltages, V_{tn} are given by:

$$V_{Tn} = \frac{V_{ref}}{2^N}.n \qquad 1 \le n \le 2^N - 1 \qquad (2.2)$$

The quantization step, V_{LSB}, is the difference between any of the two successive transition voltages. The static parameters are directly measured by comparison between the ideal and actual output transitions [7].

2.8.1 Offset, full-scale and gain errors

The offset error is defined as deviation of the first transition voltage, V_{t1}' from the ideal transition V_{t1} and is expressed in LSB at N-bit level.

$$E_{Offset} = \frac{(V_{T1'} - V_{T1})}{V_{LSB}} \qquad 1 \le n \le 2^N - 2 \qquad (2.3)$$

The full-scale error is the deviation of the last transition voltage from ideal case and is expressed in LSB at N-bit level.

$$E_{FS} = \frac{V_{T(2^N-1)'} - V_{T(2^N-1)}}{V_{LSB}} \qquad (2.4)$$

The gain error is defined as ratio between slopes of straight lines connecting two endpoints of ideal and real characteristics and is expressed in %.

$$E_{Gain} = \left(\frac{V_{T(2^N-1)'} - V_{T1'}}{V_{T(2^N-1)} - V_{T1}} - 1 \right).100 \qquad (2.5)$$

2.8.2 Integral and differential non-linearity errors

The integral non-linearity (INL) is defined as deviation of each transition voltage of each code from the ideal transition voltage estimated from the straight line connecting the two endpoints.

$$INL(n) = \frac{V_{T(n)'} - (n-1).V_{LSB'} - V_{T1'}}{V_{LSB'}} \qquad 1 \le n \le 2^N - 1 \qquad (2.6)$$

The differential non-linearity (DNL) errors can be defined as the difference between a real quantization step and the ideal quantization step, after removing the gain error.

$$DNL(n) = \frac{V_{T(n+1)'} - V_{T(n)'}}{V_{LSB'}} - 1 \qquad (2.7)$$

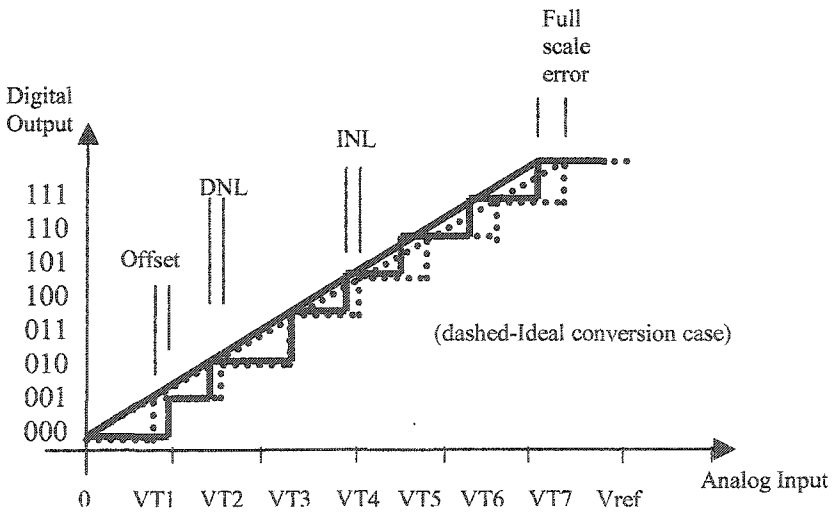


Figure 2.9: The ideal and non-ideal input/output characteristics of a 3-bit ADC

2.9 Dynamic parameters

The dynamic parameters show the performance of an ADC for a given input frequency at the sampling frequency [8]. In order to estimate the dynamic performance, a full-scale sine wave is applied and an FFT analysis is performed on the numbers at the output [9]. The spectral gives information about signal-to-noise ratio (SNR) and total harmonic distortion (THD). Figure 2.10 shows a plot of 2048 point FFT of a typical ADC.

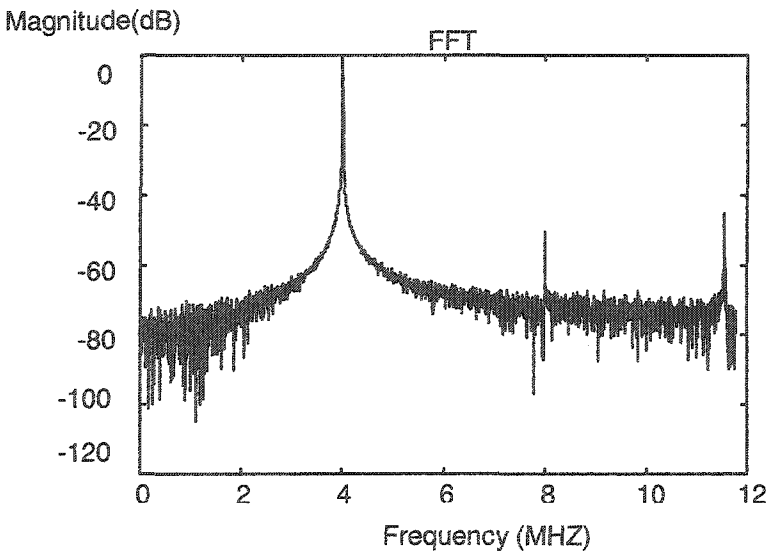


Figure 2.10: FFT spectrum of an ADC with 4 MHz input sine wave.

2.9.1 Signal-to-noise ratio:

Signal to noise ratio (SNR) is the ratio between the signal power and the summation of total noise power. It includes both the circuit noise and the quantization noise. The theoretical maximum achievable SNR of an N-bit ADC is given by:

$$SNR_{max} = 6.02.N + 1.76 \qquad (2.8)$$

The SNR of the Figure 2.10 is about 40 dB and is obtained by summation of the total power of noise excluding the total harmonics.

2.9.2 Total harmonic distortion

The total harmonic distortion (THD) is directly related to INL errors in the circuit [9]. By definition THD is expressed as:

$$THD = \frac{\sqrt{\sum_{n=2}^{(N_H+1)} A^2(n.f_{in})}}{A(f_{in})} \qquad (2.9)$$

Where N_H, A (f_{in}) and A ($n.f_{in}$) represent, respectively, the number of harmonics, the amplitude of the fundamental and the amplitude of the several harmonics.
The THD of the Figure 2.10 is about 44 dB.

2.9.3 Signal-to-noise plus distortion ratio

Signal-to-Noise plus Distortion ratio (SNDR) is the ratio between the signal power and the noise plus harmonic distortion power measured at the converter's output.

2.9.4 Spurious free dynamic range

The spurious free dynamic range (SFDR) is the ratio of signal to maximum amplitude of the noise or harmonics. It basically shows the overall purity of the spectrum at the output of ADC. The SFDR is always limited by one of the harmonics, since the magnitude of noise is always less than the harmonics.

2.9.5 Effective number of bits

Effective number of bits (ENOB) is a function of the input signal frequency and shows the effective resolution of the ADC.

$$ENOB(f_{in}) = \frac{SNDR_{dB}(f_{in}) - 1.76}{6.02} \tag{2.10}$$

Where, $SNDR_{dB}(f_{in})$ is the measured SNDR of the ADC for the input frequency.

2.10 Figures-of-merit

In order to evaluate and compare the performance of ADCs, Figures of merit must be used. Two of the most important design considerations for ADCs are power dissipation and microchip area against their overall performance. Power dissipation is important in

portable and battery-powered devices and area determines the cost of microchip fabrication. The following Figures of merit are used common for evaluation [10]:

$$FOM_1 = \frac{P}{2^{ENOB}.F_s} \tag{2.11}$$

$$FOM_2 = \frac{A}{2^{ENOB}.F_s} \tag{2.12}$$

FOM1 basically, determines the required power in order to achieve the given speed and accuracy. FOM2 expresses the cost of fabrication in terms of area for a given performance. In these Figures of merit, ENOB is used, since it is probably the parameter that describes the overall accuracy of the ADC.

2.11 Conclusions

In this chapter a number of well-known data conversion techniques and their applications were presented. The advantage of using pipeline architectures over others is high conversion rate with lower power and area consumption. Also, a number of parameters which are used to assess the static and dynamic performances of ADCs were presented. In order to compare the performance of various ADCs, two figure-of-merits were introduced. FOM1 describes the cost in terms of power dissipation and FOM2 describes the cost in terms of area, for a given performance.

Chapter 3

Design considerations for pipeline ADC architectures

3.1 Introduction

As explained in chapter 2, the advantages of the pipeline architectures are high throughput rate, low power dissipation and low hardware cost. The high throughput rate of the pipelined architectures stems from concurrent operation of the stages. As shown in Figure 3.1 [7], each stage is consisted of a low-resolution flash quantizer (SUB-ADC) and a multiplying digital to analog converter (MDAC). The flash quantizer produces a low-resolution digital output proportional to the input signal. The function of the MDAC is to convert the digital output to analog, subtract the result from the input signal to produce a residue and multiply the residue by 2^N, where N is the resolution of that stage. Mathematically, function of an ideal MDAC is described by [11]:

$$V_{out} = 2^N \times (V_{in} - DV_{ref}) \qquad (3.1)$$

Where D is digital output of the sub-ADC.

At any time, the first stage operates on the most recent sample, while the next stage operates on the amplified residue from previous sample. However due to non-idealities in circuits gain and non-linearity errors are introduced. In this chapter effect of non-idealities in the flash quantizer and the MDAC on the performance of the pipeline ADCs at the architecture level is analyzed.

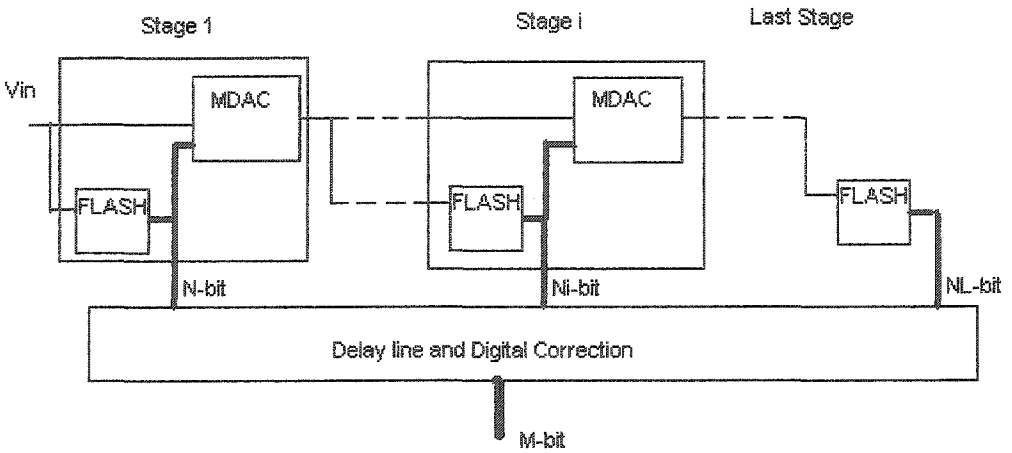


Figure 3.1: General architecture of an M-bit pipelined ADC

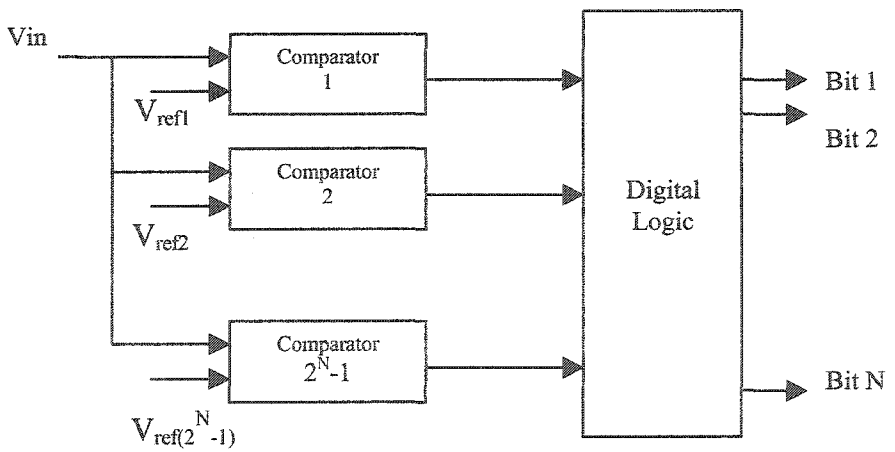


Figure 3.2: N-bit Flash quantizer

3.2 Non-idealities in the flash quantizers

Figure 3.2 shows typical architecture of an N-bit flash quantizer. Due to deviation of the reference voltages ($V_{ref1}...V_{refN}$) from their ideal values and the offset errors in the decision levels of the comparators, error is introduced in the flash quantizer. A 2-bit stage is considered as an example to analyze the effect of errors in the flash quantizer on performance of the stages. A 2-bit quantizer requires 4 comparators to define the operation region of the MDAC. The value of amplified residue to be processed by the next stage is given by:

$$Vout = \begin{cases} 4V_{in} + 3V_{ref} & ,if \quad -V_{ref} < V_{in} < -V_{ref}/2 \quad 00 \\ 4V_{in} + V_{ref} & ,if \quad -V_{ref}/2 < V_{in} < 0 \quad 01 \\ 4V_{in} - V_{ref} & ,if \quad 0 < V_{in} < +V_{ref}/2 \quad 10 \\ 4V_{in} - 3V_{ref} & ,if \quad +V_{ref}/2 < V_{in} < +V_{ref} \quad 11 \end{cases} \qquad (3.2)$$

Digital

Figure 3.3 shows the plot of input/output characteristics of an ideal 2-bit stage.

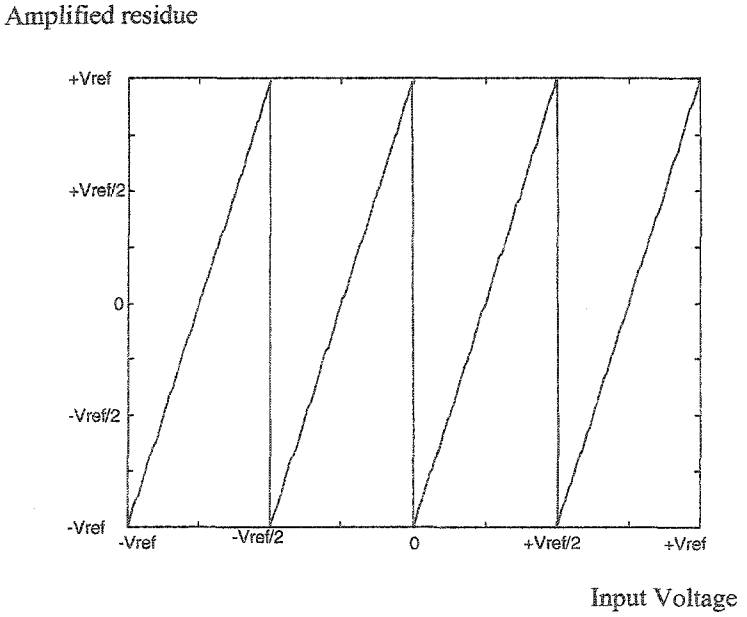


Figure 3.3: Residue amplification characteristic of the 2-bit stage.

With errors in the flash quantizer, the produced digital bits can be wrong. Therefore the analog input/output characteristic of the stage is changed. As shown in Figure 3.2, the errors cause the amplified residue to go out of the input range of the next stage. In this case the errors can not be corrected. A common practice to correct the effect of errors in the quantizer is to add redundancy in digital output bits of the stages [12, 13]. The redundancy is introduced by making the sum of the individual stage resolutions greater than the total resolution of the ADC. When the redundancy is eliminated by using a digital correction algorithm, the effect of the quantizers errors is eliminated. However it is necessary to keep the input signal of each stage within the correct range.

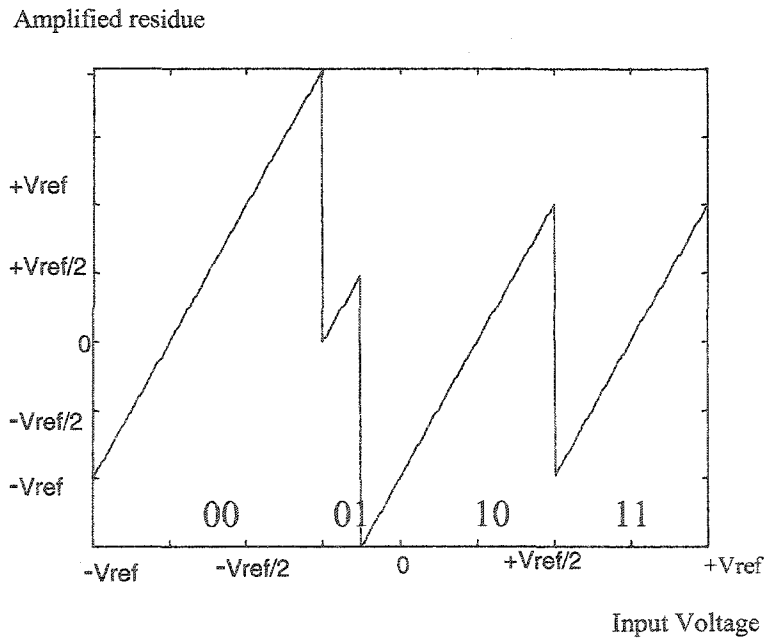


Figure 3.4: Effect of quantizer offset error on residue amplification characteristic

Figure 3.5 shows, the popular 1.5 bit stage characteristic [14, 15]. The decision levels of the comparators are shifted by Vref/4, while the stage gain is 2. The idea is to introduce offset such that, even with offset errors up to Vref/4 in the quantizer, the output range is still within the input range of the next stage. Another advantage of the 1.5 bit architecture is that only 3 comparators are used. Figure 3.6 shows the characteristic of a 1.5 bit stage with offset errors up to Vref/4. Clearly the amplified residue is still within the range. Therefore it can be corrected by digital correction logic. For the 1.5 bit architecture the input/output characteristic is given by:

$$Vout = \begin{cases} 2V_{in} + V_{ref} & ,if \quad -V_{ref} < V_{in} < -V_{ref}/4 \\ 2V_{in} & ,if \quad -V_{ref}/4 < V_{in} < +V_{ref}/4 \\ 2V_{in} - V_{ref} & ,if \quad +V_{ref}/4 < V_{in} < +V_{ref} \end{cases} \qquad \begin{matrix} Digital \\ 00 \\ 01 \\ 10 \end{matrix} \qquad (3.3)$$

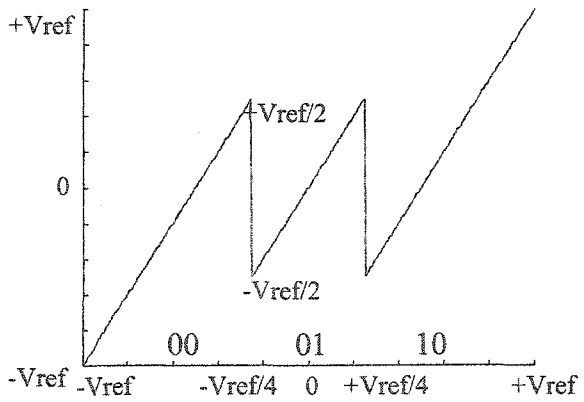


Figure 3.5: residue amplification of 1.5 bit stage

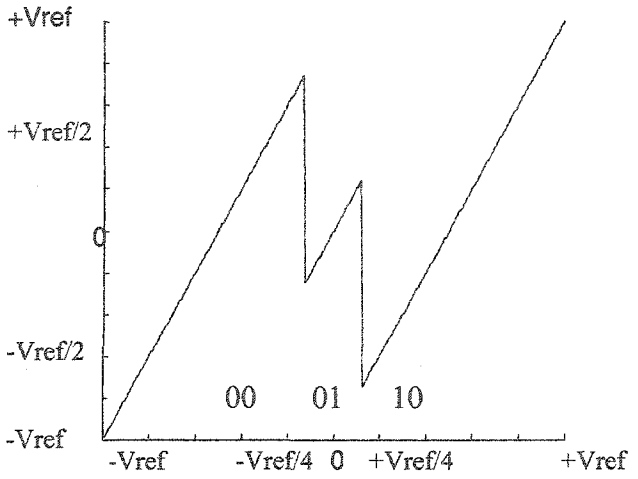


Figure 3.6: Effect of quantizer errors

Figure 3.7 shows a 10-bit pipeline ADC using the 1.5 bit architecture. The reference voltage is 1V and the input signal is -0.6V. The analog and digital output of each stage is also shown. The digital logic correction simply adds the most significant bits (MSB) of the stages to the least significant bits (LSB). Note that the most negative value corresponds to "000000000" and the most positive value corresponds to "1111111111".

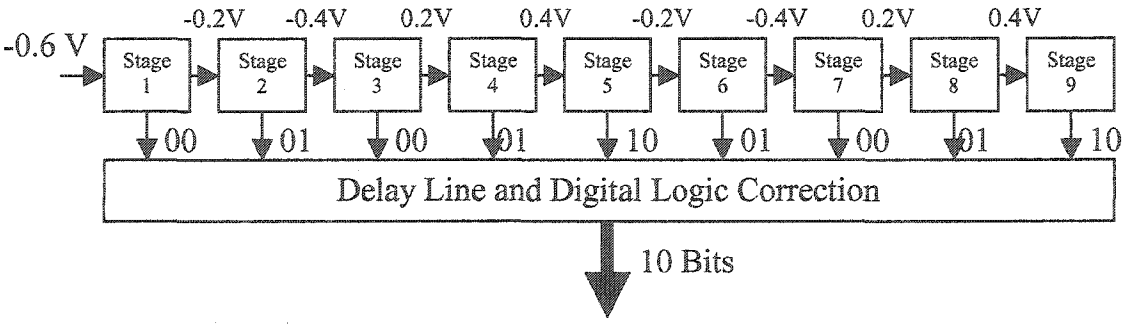


Figure 3.7: A 10-bit pipeline ADC with 1.5 bit stage resolution

The operation of the digital correction logic is as follows:

```
  000010001   MSB
+ 010101010   LSB
-------------------
  0011001100 = -0.6
```

Figure 3.8 shows the 10-bit pipeline with offset errors in its comparators as Figure 3.6. As a result the produced analog and digital outputs of the stages are wrong. With digital correction logic, the final result is corrected.

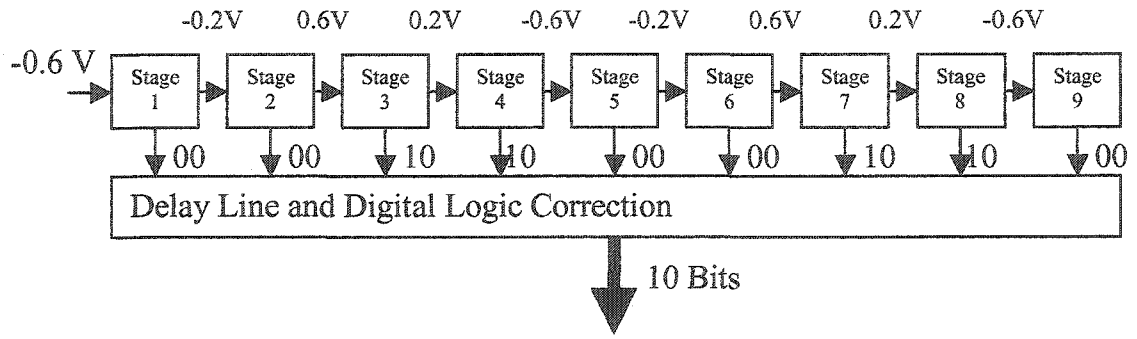


Figure 3.8: Produced errors in the stages due to errors in the quantizers.

```
  001100110   MSB
+ 000000000   LSB
-------------------
  0011001100 = -0.6
```

3.3 Non-idealities in the MDAC

Figure 3.9 shows the architecture of a 1.5-bit MDAC. The errors introduced in the MDAC are due to non-idealities in the residue-amplifier, sample-and-hold (S&H) and subtracter. Clearly the error in the residue amplifier produces gain errors, resulting the

output to be smaller or larger than input range of the next stage. Figure 3.10 shows the effect of error in the residue amplifier. The S&H and subtracter will also produce non-linearity errors as shown in Figure 3.11. To correct the errors in the MDAC analog or digital calibration algorithms are used which are more sophisticated than the digital correction logic used to correct the effect of errors in quantizers. A complete description of these calibration techniques are given in [16, 17].

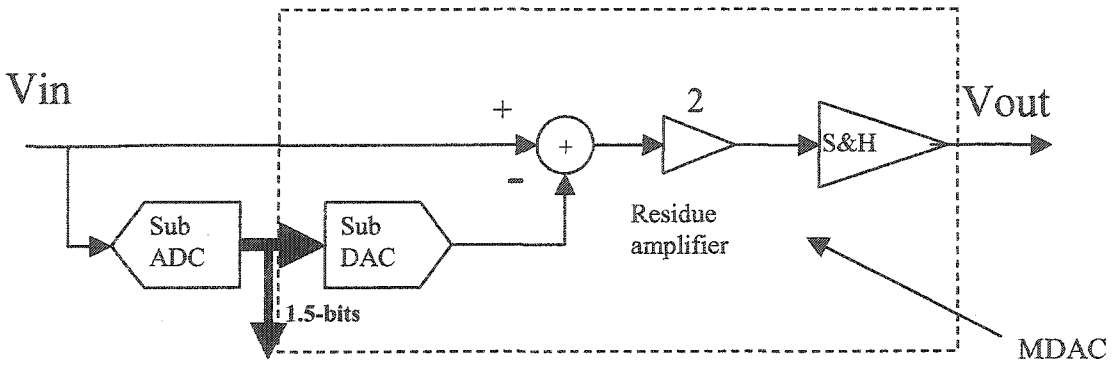


Figure 3.9: 2-bit MDAC

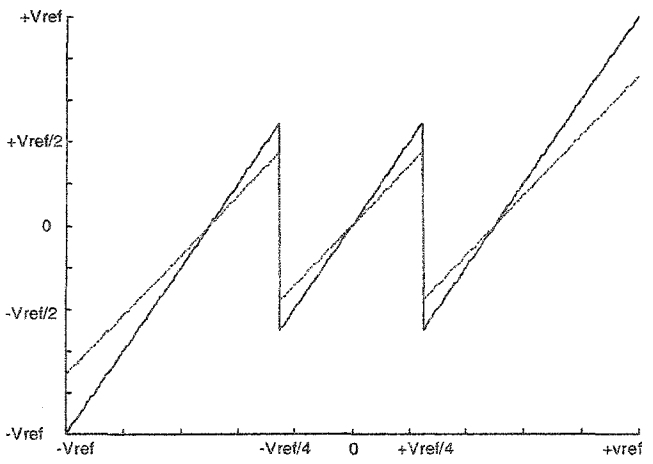


Figure 3.10: Effect of op-amp finite gain on output characteristic (Solid line is the ideal)

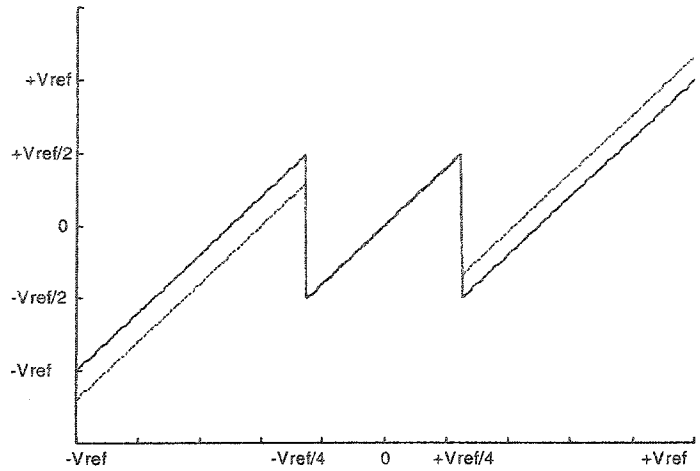


Figure 3.11: Effect of non-idealities of SUB-ADC on output characteristic

3.4 Conclusions

In this chapter, design considerations for pipelined ADCs at the architecture level was discussed. Effect of non-idealities in the flash quantizers and the MDACs on the pipeline ADCs appear as gain and no-linearity errors. The effect of errors in the flash quantizers can be completely corrected using the digital logic correction. The errors produced by the MDACs can be reduced by applying calibration techniques in analog or digital domain. Therefore it can be concluded that the accuracy of pipeline ADCs is limited by performance of the MDACs.

Chapter 4

Circuit design considerations for pipeline ADCs

4.1 Introduction

In this chapter, the design of the ADC's building blocks as well as design considerations with low supply voltage are discussed. As the CMOS technology continues to scale down the devices and the supply voltage, new circuit design techniques are required to cope with some of the limitations. As device dimensions shrink, the applied voltages will need to be proportionately scaled in order to guarantee long-term reliability and manage power density [18]. In general the analog circuits are designed either in voltage-mode or current-mode. The advantages and disadvantages of each design mode is another topic to discuss in this chapter.

4.2 Low-voltage design limitations

In conventional analog CMOS design the circuits are designed often in voltage mode. Specifically in pipeline ADCs, the switched-capacitor circuits are used in front-end S/H, multiplying digital to analog converters (MDAC) and preamplifiers for comparators. The switch capacitor circuits contain three components, namely, switches, op-amps and capacitors. Advances in CMOS technology, however, are driving the operating voltage

of integrated circuits increasingly lower. Consequently this will have an effect on reliability of CMOS switches and op-amps.

4.2.1 Effect of lowering voltage on switches

As the supply voltage is reduced, the Ron resistance of switches is increased. This will make the switches far from ideal. Although, by using transmission gate, the dynamic range of switches can be increased, as discussed in [18] transmission gates cannot be directly realized on a supply voltage below the sum of the two threshold voltages. Fortunately, for the technology that is used in this work, the threshold voltages of NMOS and PMOS are about 0.6 volts and the supply voltage is 1.8 volts. Therefore by increasing the width (W) of transistors, the Ron resistance can be reduced. However increasing the size of switches will also have two disadvantages. First, clock feed-through and charge injection will be increased, which can significantly degrade the accuracy of the ADC. This can be seen from expressions for the clock feed-through and charge injection given in the following equations respectively [19]:

$$\Delta V_{clock-feedthrough} = V_{ck} \frac{WC_{ov}}{WC_{ov} + C_H} \tag{4.1}$$

$$\Delta V_{charge-injection} = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H} \tag{4.2}$$

Where, C_{ov}, C_{ox} and C_H represent the overlap capacitance, the gate oxide capacitance and the sampling capacitor, respectively.

The second drawback is that the capacitive load on the op-amps is increased which increases the power dissipation. In some cases where the sum of threshold voltages is higher than the supply voltage, a common solution is to use a bootstrap circuit, which will increase the voltage for switches locally [20, 21].

4.2.2 Effect of lowering voltage on op-amps

Another design complication with low-voltage is the difficulty in biasing the op-amps. This is because, it is desirable to bias the transistors as to increase the output swing. This is necessary to achieve acceptable SNR in medium and high resolution pipeline ADCs. However this becomes difficult in low-voltage applications since reducing the overdrive voltage of transistors will degrade the surface mobility [22]. Using 2-stage topologies also requires compensation to avoid the instability problem. This will usually degrade the band-with, therefore reducing the speed of pipeline ADCs.

4.2.3 Voltage-mode versus current-mode design

In current-mode circuit design, the signals are represented by current rather than voltage. The main building block in current-mode circuits is the current mirror. The accuracy of the current mirrors depends on the matching accuracy of transistors. For this reason, it is difficult to design high accuracy circuits in current-mode since there is always mismatch between devices due to errors in VLSI fabrication process. However the current-mode VLSI design has several advantages over the voltage mode approach [23-25].

Firstly the current-mode IC design is compatible with digital IC design since it does not require high linear capacitors as opposed to switched-capacitor circuits. Secondly, the basic functions, such as scaling, summation and subtraction can be easily implemented without using op-amps. Thirdly, the voltage swing required in current-mode circuits is smaller than that in voltage-mode circuits due to the square I-V law of MOS transistors operated in saturation region. This advantage makes the current-mode approach suitable for low-voltage application. Fourthly, the current-mode approach usually results in low-power dissipation without sacrificing the speed.

4.3 Comparators

Low power and low voltage circuit design techniques are required for portable devices. Since analog-to-digital converters are the link between the analog and digital domain, it is essential to design these circuits with minimum amount of power. High conversion rate and low power is desirable in a number of applications, including visual-data processing systems, hard disk controllers, handy data terminals, and so forth [26]. The pipelined A/D converters are the preferred architectures in terms of speed and power dissipation [26-29]. The performance of A/D converters that have the pipelined architecture strongly depends on the performance of comparators.

In this section, performance of various comparators in terms of speed, power and resolution is analyzed and the simulation is performed using HSPICE models for 0.18 μm CMOS process.

In general, there are two classes of comparators [30]. The first class is amplifier type comparators, which utilize a number of amplifiers in series in order to obtain the overall gain. There is a trade off between bandwidth, resolution and power dissipation. For example, in order to obtain high resolution, high gain is required. However, high gain reduces the bandwidth of the comparators. One way to overcome this problem is to keep the gain in each stage low, while increasing the number of stages [33]. As a result, the power dissipation increases with the number of stages. The second class of comparators is latch type comparator. The essential part of the comparator is the regenerator latch. Due to zero static power and high speed of the latches, these comparators are very suitable for low power and high-speed A/D converters. In the following sections, both classes will be analyzed and simulated to show their advantages and disadvantages.

4.4 Amplifier type comparators

4.4.1 A two-stage comparator

A two-stage comparator is shown in Figure 4.1 [31]. It consists of a differential stage amplifier (M1 and M2), a current inverter M5-M6 (as the second amplifier) and the circuit to provide the bias current (M8-M11). The simulation predicts the instantaneous dc power dissipation of about 4 μW while the maximum bandwidth is 10 MHz. This speed is much lower than the required frequency for pipelined A/D converters.

The power dissipation in the differential pair is mainly static, since the differential pair only stirs the current that is supplied by the current mirror M7-M8. However, for the inverter, the relation for dynamic power ($P = 1/2\ C_p V_{dd}^2 f$, where C_p represents the capacitance at the output) is still valid. Therefore, the sizes of M5 and M6 are essential for dynamic power dissipation. To get the maximum bandwidth, the transistors size should be as small as possible to reduce the time-constant.

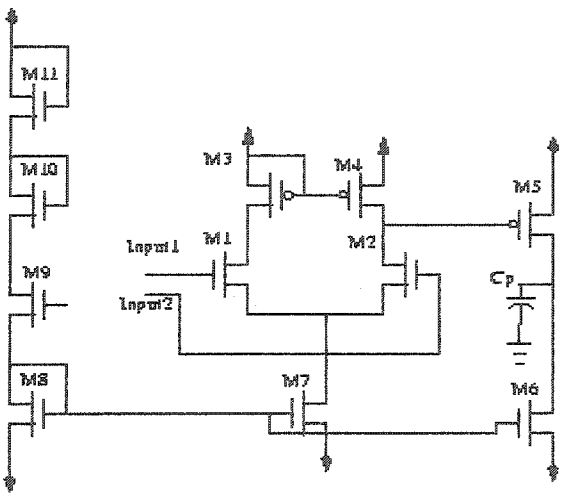


Figure 4.1: A two-stage comparator

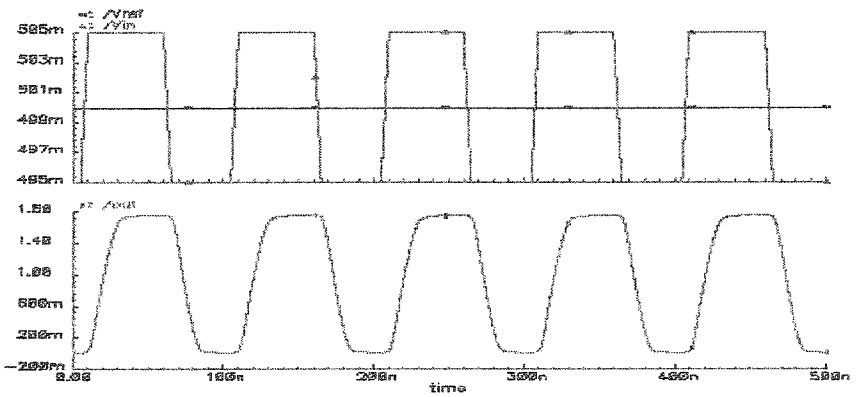


Figure 4.2: Simulation result for the two-stage comparator with the frequency of 10 MHz

4.4.2 A multi-stage comparator

In order to increase the bandwidth of the above comparator, the gain of each stage should be reduced. Therefore, many stages are required to increase the overall resolution, since the gain sets the smallest voltage difference that can be amplified to digital levels. Figure 4.3 shows a multi-stage differential pair [33]. Figure 4.4 shows the simulation results for 11 stages of differential pairs which are required to obtain 1mV resolution and 50 MHz bandwidth. The static power dissipation predicted by HSPICE is 18 μW. The disadvantage of the multi-stage comparator is its high power consumption, since the power is increased with every stage added. To produce TTL compatible signals, level shifters or an inverter is required at the output. Also, this comparator requires an accurate bias voltage, since the overall gain is very sensitive to the voltage.

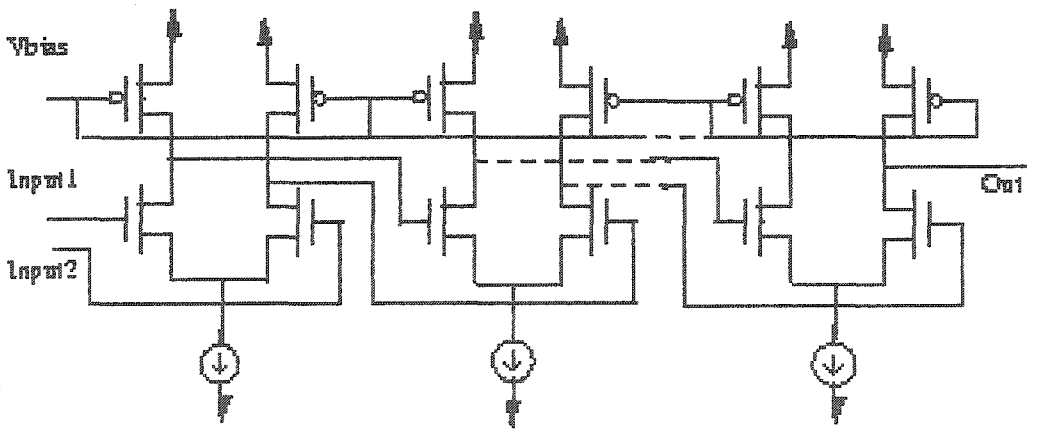


Figure 4.3: A multi-stage comparator

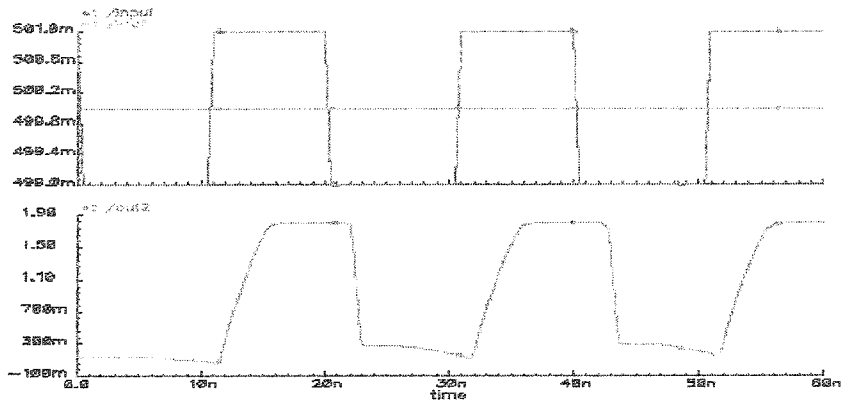


Figure 4.4: Simulation result for the multistage comparator with the frequency of 50 MHz

4.5 Latch type comparators

The advantage of a latch is that it dissipates no static power. The dynamic latch generates digital outputs, and only power dissipation is the charging current and short-circuit current from V_{dd} to ground during the transition to settling out. The regeneration time-constant, τ_{reg}, for this type of latch is given by [32]:

$$\tau_{reg} = \frac{C_p}{g_{m3} + g_{m5}} \tag{4.3}$$

Where C_p is the total capacitance at the output nodes and gm is the transconductance of the CMOS transistors. The power consumption is a function of transistor size. Figure 4.5 shows the circuit diagram for a dynamic latch comparator [26]. For the latch comparator, the speed is a function of transistor sizes and transconductace (g_m). To obtain lower regeneration time, smaller transistor's width should be used according to the above

equation. From the Figure, when the clock is low (reset phase), M7 and M8 are open, and the current cannot flow from V_{dd} to ground or from inputs to ground. When the outputs are settled, there is no static current, because either side of the latch has one of its transistors turned off. Figure 4.6 shows the simulation result with 200 MHz frequency. The current waveform is shown in Figure 4.7. Figure 4.8 shows the circuit diagram of a transconductance latch comparator [29]. The operation is based on the difference between the transconductances of M1 and M2, due to the difference of V_{in} and V_{ref}. In this comparator, the two inverters and two switches (M10-M11) are used to reduce the power consumption by cutting off the current when point A or B is at logic 1. Figures 4.9 and 4.10 show the simulation result with 25MHz frequency and the current waveform of the comparator, respectively.

The differential pair comparator as shown in Figure 4.11 [6] has a very high bandwidth, high resolution and still consumes relatively low power. It also has a relatively small input offset, since a differential amplifier is used at the input stage. The operation is based on the difference between the transconductances of the differential pair (i.e., M1 and M2). When the clock is low, the outputs are reset to V_{dd} through M7 and M8. At the same time, the gates of M5 and M6 are at V_{dd}, and no current can flow from the power supply to ground. When the clock is high, the difference between the transconductances of the differential pairs determines which side of the regenerator goes to logic 1 and which side goes to logic 0. Figures 4.12 and 4.13 show the simulation result with 200 MHz frequency and the current waveform for the circuit in Figure 4.11, respectively.

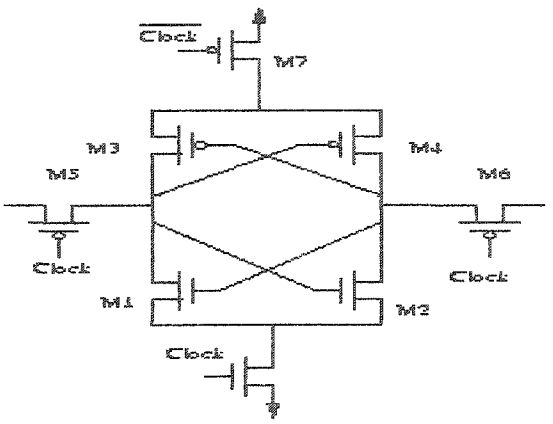


Figure 4.5: A dynamic latch comparator

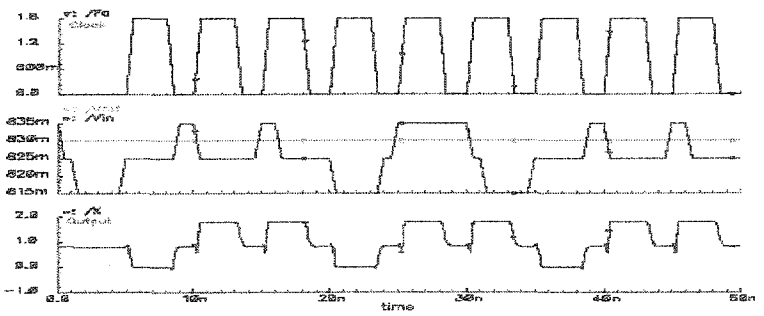


Figure 4.6: The simulation results at 200 MHz for Figure 4.5 (the comparison points are at the rising edge of the clock)

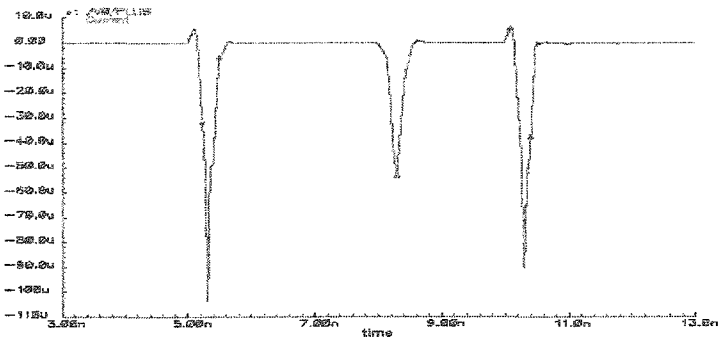


Figure 4.7: The waveform of current flowing from the power supply of Figure 4.5 (the power dissipation can be estimated from the area under the current curve to be about 15 μW)

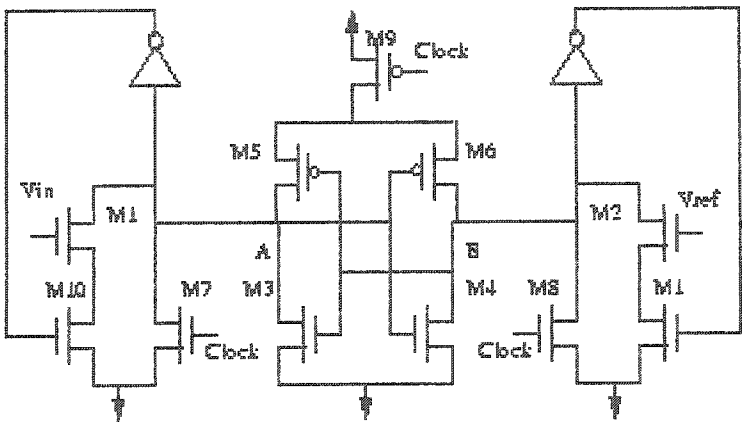


Figure 4.8: A transconductance latch comparator

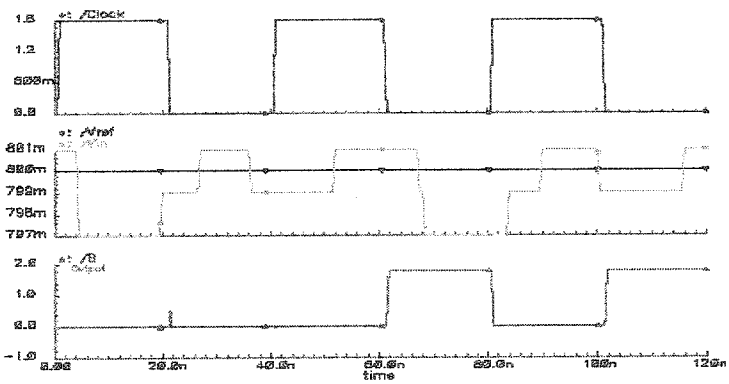


Figure 4.9: The simulation result for the transconductance latch comparator of Figure 8 at 25 MHz (the comparison point is at the falling edge of the clock)

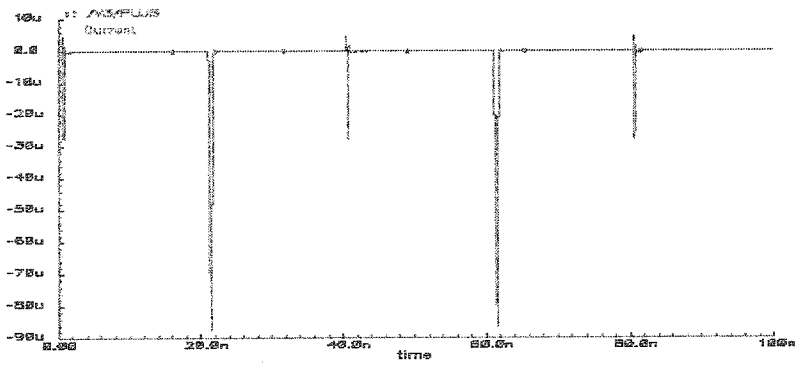


Figure 4.10: The waveform of current flowing from the power supply of Figure 4.8 (the dynamic power dissipation is estimated to be 2 μW)

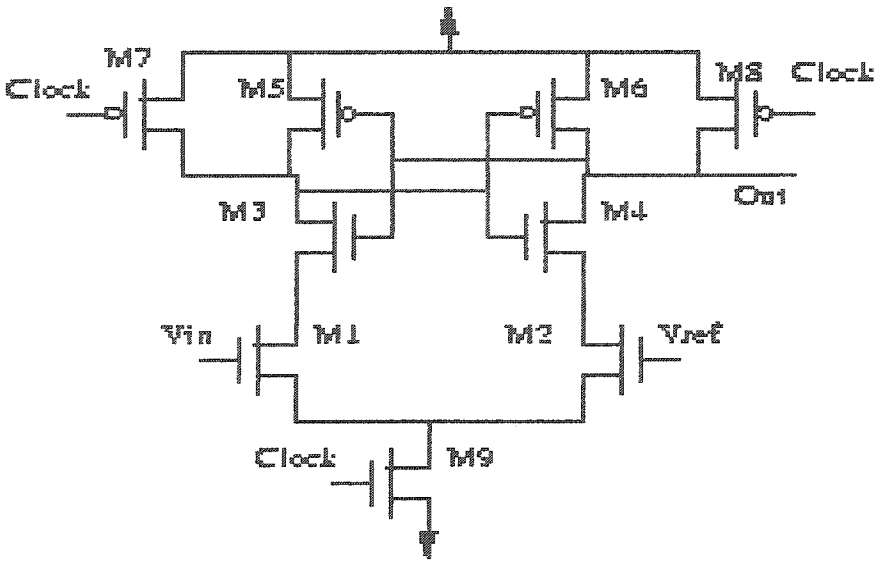


Figure 4.11: A differential pair comparator

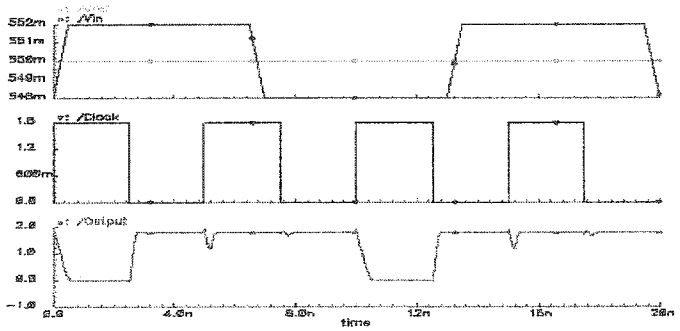


Figure 4.12: The simulation results for the differential pair comparator of Figure 4.11 at the frequency of 200 MHz

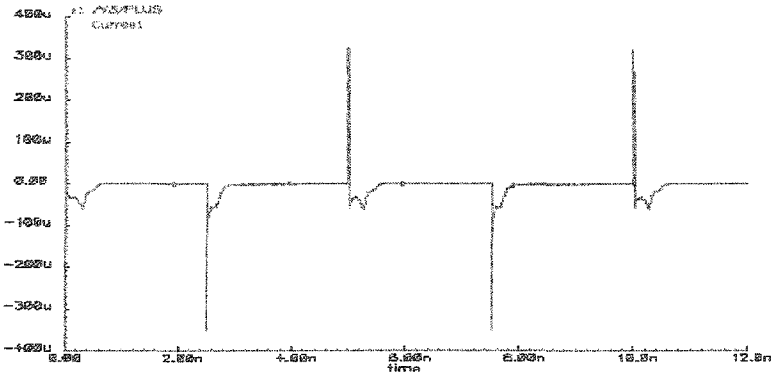


Figure 4.13: Current flowing from the power supply of Figure 4.11 at 200 MHz (the power dissipation estimated from the current curve is about 50 μW)

4.6 Sample-and-hold

Sample-and-hold (S&H) is required for the front end of the pipeline ADCs. Wide-band ADCs are required in wireless applications such as IF digitization. Without wide-band S&H circuit, it is not possible to achieve high accuracy at a high input frequency. The conventional S&H circuits are designed using switched-capacitor circuits. Figure 4.14 shows a fully differential S&H architecture [35] known as non-inverting amplifier. The circuit works in two phases. In the sampling phase (CK1) the input is sampled by the sampling capacitors (C1), while capacitors C2 are disconnected. Also the outputs are shorted together to reset the op-amp. In the hold phase (CK2), the inputs are disconnected from the sampling capacitors and capacitors C2 are placed around the op-amp. Therefore the stored charge on C1 is transferred to C2. The output of the S&H at the end of the hold phase is given by:

$$V_{out} = \frac{C1}{C2(1+\frac{1}{A})} . V_{in} \qquad (4.4)$$

Where A is the finite dc gain of the op-amp. With C1=C2=C, and sufficiently high dc gain, the input is sampled and held accurately. However the dependence on the matching accuracy of capacitors makes it difficult to sample the input signal accurately.

Figure 4.15 shows a slightly different S&H architecture known as unity gain sampler [19]. In the sampling phase the sampling capacitors are charged by the inputs while the inputs and outputs of the op-amp are shorted together to reset the circuit. In the hold phase the inputs are disconnected and the capacitors are placed around the op-amp to form an integrator. The output is given by:

$$V_{out} = \frac{V_{in}}{(1+\frac{1}{A})} \qquad (4.5)$$

Which does not require any capacitor matching. The unity gain sampler also is faster since its feedback factor is larger. Sometimes, the sampled input signal must also be amplified as to increase the signal-to-noise ratio of the ADC. In such applications the non-inverting amplifier is used to amplify the sampled input by the ratio of C1/C2.

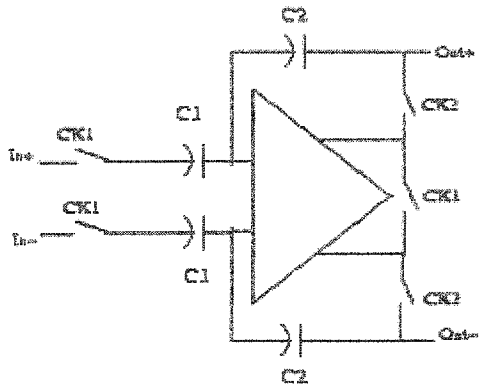


Figure 4.14: Non-inverting amplifier

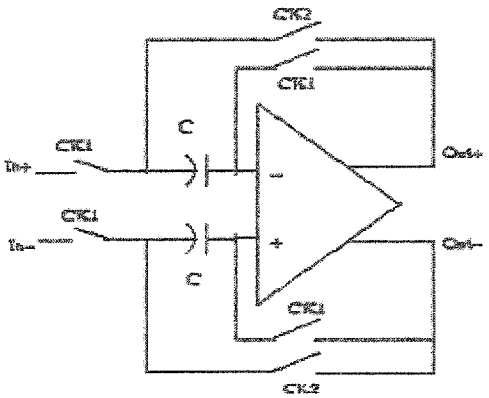


Figure 4.15: Unity gain sampler.

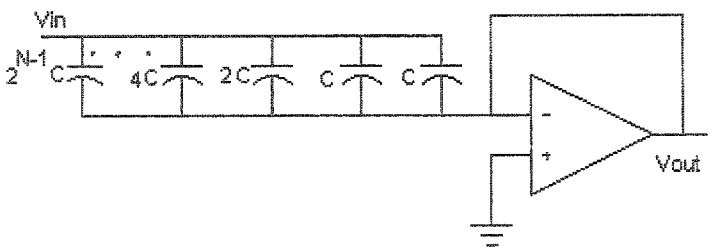


Figure 4.16(a)

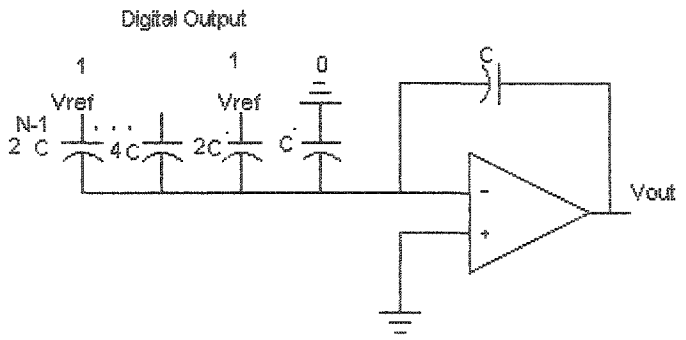


Figure 4.16(b)

Figure 4.16: N-bit MDAC, a: In sampling phase b: In residue amplification phase

4.7 Multiplying digital-to-analog converter

The MDAC operates on two clock phases. In the sampling phase (Figure 4.16a), the input signal is connected to the sampling capacitors through the switches to sample and hold the input signal. Also outputs and inputs are shorted together to keep the input voltages of the op-amp at the same level.

In the second phase (Figure 4.16b), the inputs are disconnected from the inputs by turning off the switches and capacitor C_I is placed around the op-amp to form an integrator. Also the left planes of the switching capacitors are connected to a voltage proportional to the output of the sub-ADC. At the end of amplification phase, assuming an ideal op-amp, the output is given by:

$$V_{out} = \frac{1}{C_0}(V_{in}(C_0 + \sum_{i=1}^{2^{N-1}} C_i) - \sum_{i=1}^{2^{N-1}} D_i C_i V_{ref}) \qquad (4.6)$$

Where N is the stage resolution, D_i is digital output bit of the sub-ADC and C_i is the capacitor in the capacitor-array:

$C_0=C$, $C_i=2^{i-1}C$

Due to non-idealities in the circuit, gain and non-linearity errors are introduced. The errors in MDACs are due to mismatch between capacitors, finite gain and offset of op-amps, R_{ON} resistance, charge injection and clock feed-through of switches. Non-ideality of switches appears as gain and non-linearity errors.

In order to analyze effect of mismatch between capacitors, the error in capacitors can be expressed as:

$$C_0=(1+\varepsilon_0).C, \quad Ci=(2^{i-1}+\varepsilon_i).C \quad , i=1,\ldots,N \tag{4.7}$$

With capacitors mismatch equation (4.6) becomes:

$$V_{out}=\frac{1}{(1+\varepsilon_0).C_0}(V_{in}(C_0+\sum_{i=1}^{2^{N-1}}C_i+\sum_{i=0}^{2^{N-1}}\varepsilon_i)-\sum_{i=1}^{2^{N-1}}D_iC_i(1+\varepsilon_i).V_{ref}) \tag{4.8}$$

Which shows that capacitor mismatch produce gain and non-linearity errors.

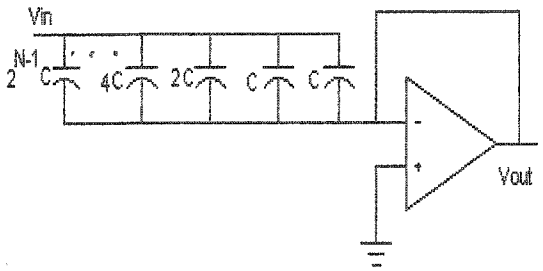
Assuming perfect matching between capacitors and a non-ideal op-amp, the output is given by:

$$V_{out}=\frac{2^N\times(V_{in}-D\frac{V_{ref}}{2})}{1+\frac{2^N}{A0}} \tag{4.9}$$

Where A0 is the finite DC gain of op-amp. Clearly the finite gain of op-amp produces gain errors.

4.8 Topology selection and design of op-amps in pipeline ADCs

In pipeline analog-to-digital converters (ADC), speed, power dissipation and resolution significantly depend on the op-amps used in the front-end sample-and-hold and multiplying digital-to-analog converters. Since the error in the SUB-ADCs can be corrected completely by the digital correction logic, the accuracy of pipeline ADCs is limited by the errors in the MDACs and S/H. The main sources of error in these circuits are mismatch between capacitors, clock feed-through and charge injection of switches, thermal noise of capacitors and finite gain of the op-amps. The input signal range of the ADCs depends on the maximum output swing of the op-amps used in the S/H and MDACs. Consequently as the supply voltage is scaled down in new CMOS technologies, the output swing of the op-amps is reduced. This will make the design of high-resolution pipeline ADCs more challenging since achieving high signal-to-noise ratio is more difficult when input signal range is reduced. In pipeline ADCs, the main portion of power is dissipated by the dc bias current of op-amps used in the front-end S/H and MDACs to meet the settling accuracy at a given sampling rate. If current is too low, then the output will not reach to the final voltage level during the half clock period, therefore producing error. On the other hand, if the current is too high, the output will reach to the final value earlier than the required time and too much power is wasted. Another requirement of the op-amps is the dc gain. Since the finite gain of the op-amps produces gain and non-linearity errors, the achievable resolution of each stage depends on the dc gain of the op-amp. In this section effect of op-amp topology on power-dissipation, area and speed is analyzed. The advantages and disadvantages of various op-amps are considered.



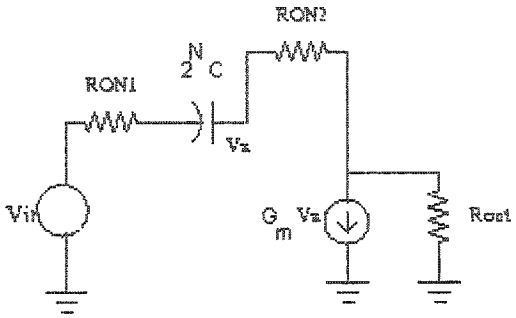
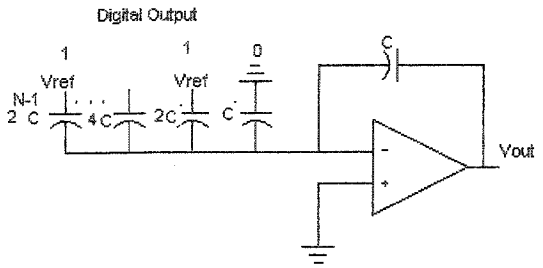


Figure 4.17 (a) Figure 4.17 (b)

Fig. 4.17: N-bit MDAC a: In sampling phase, b: Equivalent of the circuit in sampling phase.



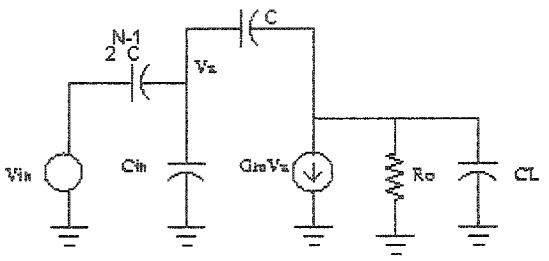


Figure 4.18 (a) Figure 4.18 (b)

Fig. 4.18: N-bit MDAC, a: In amplification phase, b: Equivalent of the circuit in amplification mode.

4.8.1 Speed considerations

The MDAC operates on two clock phases, sampling and amplification phases. Figure 4.17a shows the circuit in the sampling phase. From the equivalent circuit (Fig. 4.17b), the time-constant of the circuit in sampling mode is approximately given by:

$$\tau_{sam} = (R_{on1} + \frac{1}{G_m}) \times 2^N C \qquad (4.10)$$

Where $R_{on}1$ is the ON resistance of switch S1, G_m is Transconductance of the op-amp, C is the unit capacitance and N is the stage resolution.

The time-constant of the circuit in the sampling phase must be small enough to allow settling the input voltage across the capacitors. This is important for the S/H, if the input signal contains high frequency components. It is obvious that reducing time-constant requires reducing $R_{on}1$ and C, while increasing G_m.

Figure 4.18a shows the circuit in the amplification mode and the equivalent of circuit is shown in Figure 4.18b.

The time-constant of the circuit during the amplification phase is approximately given by:

$$\tau_{amp} = \frac{(C_L + C)((2^N - 1) \times C + C_{in}) + C_L C}{G_m C} \qquad (4.11)$$

Where C_{in} is the input capacitance seen at the input of op-amp and C_L is the total capacitance seen at the output of the MDAC. At the end of amplification phase, the output of the amplifier must settle to the required accuracy in order not to cause any error. This also depends on the time-constant in amplification phase. From (4.10) and (4.11), it can be concluded that in order to reduce the time-constant of the MDAC, the transcoductance of the op-amp G_m must be increased. For one-stage op-amps, this can be accomplished by increasing width of the input transistor [19], without increasing current, which will require reducing the overdrive voltage. This can be seen by considering the transconductance equations of CMOS transistors:

$$g_m = \sqrt{2\mu_n C_{ox}(\frac{W}{L})I_D} \tag{4.12}$$

$$g_m = \frac{2I_{bias}}{(V_{GS} - V_{th})} \tag{4.13}$$

Table 4.1: Performance of double cascode op-amp

Op-amp	Not Optimized	Optimized
Bandwidth	25.15 KHZ	24 KHZ
Unity Gain	330 MHZ	340 MHZ
DC Gain	82dB	83dB
Load	1.5 pf	1.5 pf
Settling time	8ns	8ns
Bias current	1.012mA	0.507mA
Width ($M_{1,2}$)	9μm	18μm
Power dissip. of A1	0.5mW	0.5mW
Power dissip. of A2	0.5mW	0.5mW
Total power	2.82mW	1.91mW

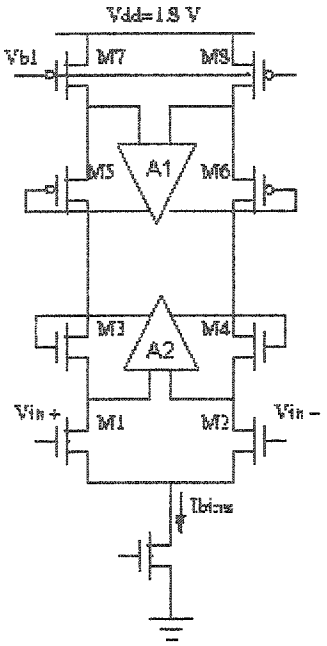


Figure 4.19 (a): a double cascode op-amp with gain-boosting.

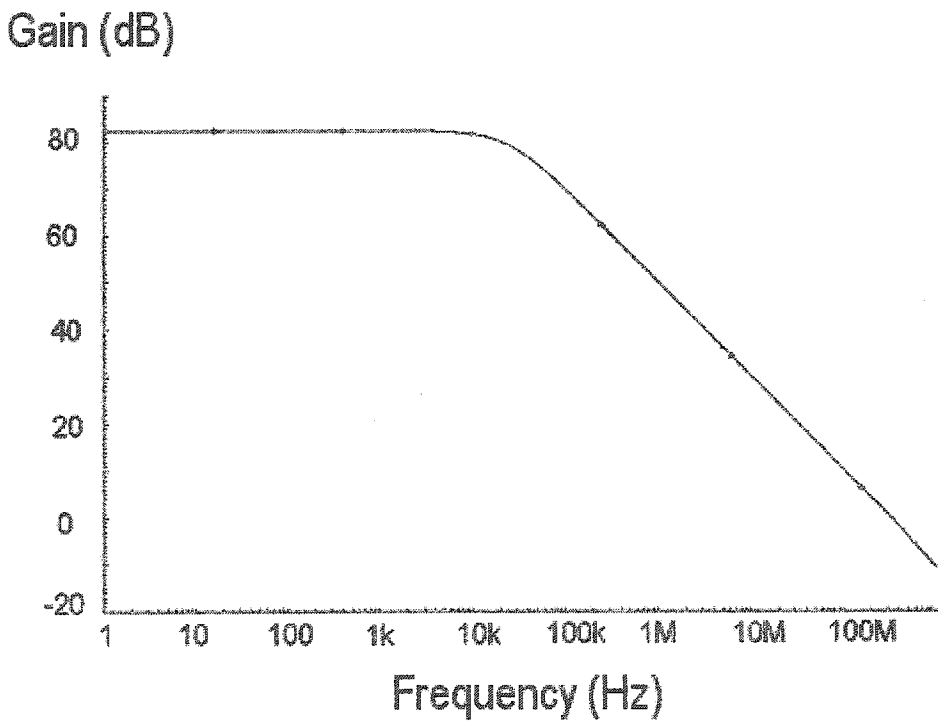


Fig. 4.19 (b): Magnitude response of the optimized cascode op-amp.

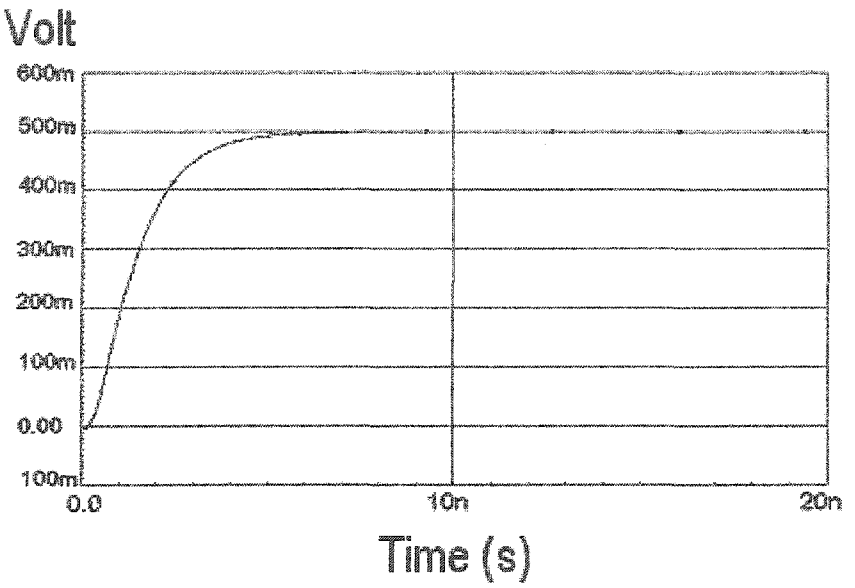


Fig. 4.19 (c): Settling behavior of the cascode op-amp

Figure 4.19a shows a gain-boosted double cascode op-amp. The magnitude response and the settling behavior are depicted in Figures 4.19b and 4.19c respectively. The gain-boosting op-amps, A1 and A2, are conventional n and p type folded cascode op-amps. The gain for a double cascode is given by $g_{m1}[(g_{m3}r_{o3}\ r_{o1}) \parallel (g_{m5}\ r_{o5}\ r_{o7})]$, which can only be a few hundred. This gain is not enough to be used for pipelined ADCs, with gain-boosting technique the gain is approximately given by: $g_{m1}[(A1g_{m3}r_{o3}\ r_{o1}) \parallel (A2g_{m5}\ r_{o5}\ r_{o7})]$.

Table 4.1 summarizes the performance of the op-amp in 2 cases. In the first case the main op-amp was biased with 1.012 mA. In second case, the bias current was reduced by about 50% while the width of M1 and M2 was increased by the same factor. Although the power dissipation was reduced, simulation predicts almost the same settling time and bandwidth since the transconductance is not reduced. Another consideration is output swing.

For a double cascode op-amp the output swing is $2(V_{DD}-V_{OD9}-V_{OD1}-V_{OD3}-|V_{OD5}|-|V_{OD7}|)$. With 1.8V supply voltage, in 0.18μm CMOS technology, and assuming 300mV across the PMOS and current source transistors and 200mV across the NMOS transistors, the output swing is $1V_{p-p}$. By using the well-known, folded cascode topology, the output swing can be increased by about 600mVp-p at the cost of higher power dissipation and lower speed.

Figure 4.20 shows a pseudo-differential double cascode op-amp with the output swing equal to that of the folded cascode. The power dissipation is reduced by a factor of about 3/5 and higher speed can be achieved comparing to the folded cascode topology [36].

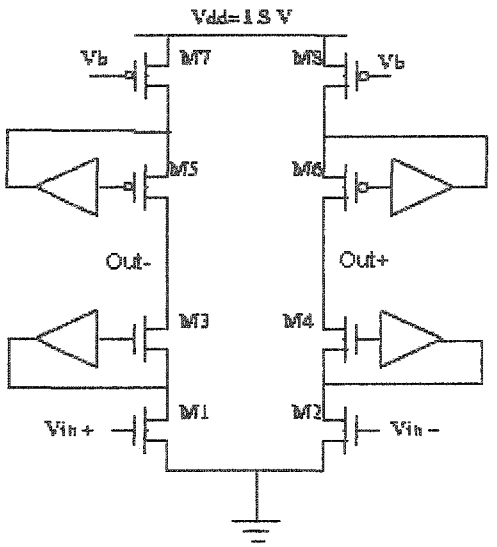


Figure 4.20: A gain-boosted pseudo-differential op-amp

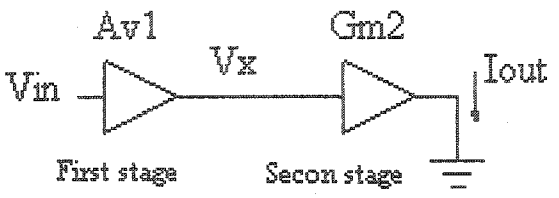


Figure 4.21: 2-stage op-amp topologies

In applications where a wide-band ADC is required, the transconductance of one-stage op-amps may not be high enough in the sampling mode. In these cases, 2-stage topologies will provide higher transconductance. As shown in Figure 4.21 the effective Gm of a 2-stage op-amp is given by:

$$G_m = \frac{\partial I_{out}}{\partial V_{in}} = \frac{\partial V_X}{\partial V_{in}} \cdot \frac{\partial I_{out}}{\partial V_X} = A_{v1}.G_{m2} \qquad (4.14)$$

Another way to reduce the time-constant is to reduce total capacitance. The capacitor units are chosen according to noise constraints. As shown in [7], for n bit resolution ADC with signal range of 2Vref, the value of capacitor unit in an N-bit MDAC must satisfy the following condition:

$$C >> \frac{3.K.T.2^{2n}}{2^N.V^2_{Ref}} \qquad (4.15)$$

Where K is the Boltzmann's constant, T is the absolute temperature.

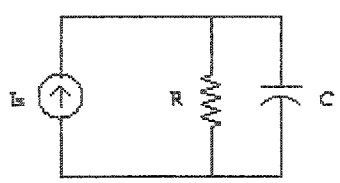


Figure 4.22: RC model to analyze step response

4.8.2 Power dissipation

In pipelined ADCs the main source of power dissipation is the dc biasing current of the op-amps to meet the settling time requirements. In order to analyze the step response of the circuit in each phase, a first order RC (shown in fig. 4.22) circuit is used. The step response of an RC circuit is given by:

$$V_C(t) = I_S R + (V_0 - I_S R)e^{-t/\tau} \qquad (4.16)$$

With R= 1/Gm. Solving the above equation for current gives:

$$I_{bias} = \frac{G_m (Vout - V_0 e^{-t/\tau})}{(1 - e^{-t/\tau})} \qquad (4.17)$$

Where V_0 is the initial voltage at the output. The time-constant τ in the above equation is either τ_{sam} or τ_{amp}. However I_{bias} corresponds to the greater value of the two.

Also I_{bias} given in the above equation is for half of the circuit, therefore minimum bias current is given by:

$$I_{min}=2Max(I_{sam},I_{amp}) \qquad (4.18)$$

Where I_{sam} and I_{amp} are the required bias current in the sampling and amplification mode, respectively. In the above equation, Imin is the minimum required current to charge the output from the initial voltage to Vref in a given time, t. From (4.17) it can be seen that

reducing the time-constant will result in reduction of power dissipation significantly. If signal range is large, the value of capacitors can be small, since this will relax the thermal noise constraints. In low voltage applications, the output swing can be increased by using 2-stage topologies. Although the extra stage has its own power dissipation, in low-voltage and medium to high resolution pipeline ADCs, the power dissipation may be even reduced comparing to the case of one-stage op-amps. This can also be explained by considering the gain requirement. Since gain of one-stage op-amps is too low to be used for pipelined ADCs, gain-boosting may be used which, also increases the power dissipation.

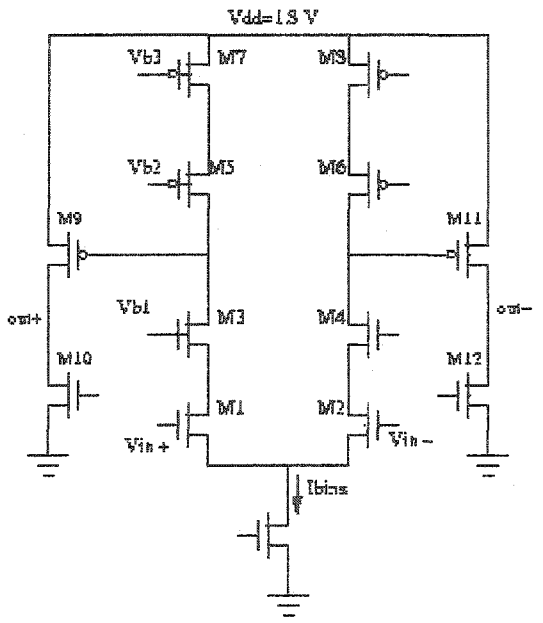


Figure 4.23: A 2-stage high-swing op-amp

Another way to increase the gain, is by using a 2-stage op-amp, which also improves transconductance and output swing. Nonetheless, 2-stage op-amps require compensation to become stable and their speed is limited.

Figure 4.23 shows a 2-stage op-amp with high output swing. The gain is approximately given by: $g_{m1}[(g_{m3}r_{o3}\ r_{o1}) \parallel (\ g_{m5}\ r_{o5}\ r_{o7})][g_{m9}\ (r_{o9} \parallel r_{o11})]$. The differential output swing is $2(V_{DD}$-

$|V_{OD9}|-V_{OD11}$). In 0.18μm CMOS technology and 1.8V supply voltage, the output range is about $2.4V_{p-p}$ (2(1.8-0.3-0.3)). Since the output swing is increased by a factor of almost 2 comparing to one-stage op-amps, the unit capacitance can be reduced by a factor of 4. Therefore it can be concluded that both power dissipation and area are reduced.

4.9 Conclusions

In this chapter design consideration for sub-circuits used in pipelined ADCs was discussed. In order to analyze performance of comparators, five comparators have been analyzed in terms of their advantages and disadvantages. It has been shown that in designing comparators, there is a trade off between their resolution, bandwidth and power consumption. As shown in the simulation results, the latch type comparators have better performance in terms of speed, resolution and power dissipation. The power consumption is only dynamic due to the charging/discharging of the output, which is a function of switching activity. Another issue with comparators is the input offset voltage. Unfortunately, the latch type comparators have high input offset. One way to reduce the offset is to use a preamplifier so that the input offset is divided by the amplifier's gain [26, 34]. This method, however, results in the increased power dissipation. Another way to overcome the input offset is to use a digital logic error correction circuit, which consumes less power compared to the first method.

In section 4.6 effect of op-amp topology on the overall performance of pipeline ADCs was analyzed. It was shown that increasing transconductance of op-amps, will reduce the power dissipation and improves the band-width of pipeline ADCs. In one-stage op-amps,

transconductance is improved by increasing the width of the input devices. In low-voltage applications, by using 2-stage topologies, both transconductance and output swing are increased, which can also result in lower power and area, however they achieve lower conversion rate. In general it may be concluded that for high conversion rate and medium resolutions, one-stage topologies, such as pseudo-differential architectures are suitable. If higher resolutions and lower conversion rate is required, 2-stage topologies may prove better performance. Also, parallel pipeline architectures may be used to increase the conversion rate [36].

Chapter 5

Design of a novel low-power, low-area, 12-bit 40Msamples/s pipeline ADC

5.1 Introduction

The conventional architecture of pipeline ADCs is shown in Figure 5.1. It is consisted of a few stages, and a digital logic correction. Each stage is consisted of a Multiplying digital to analog converter (MDAC) and a low resolution SUB-ADC.

In conventional voltage-mode pipeline ADCs, the MDACs are designed using fully differential switched capacitor circuits, which require high-gain, high-swing, fast settling time op-amps and large, high-linearity capacitors, which occupy large area. In these stages the main source of power dissipation is the biasing current of op-amps to meet the settling time requirements.

It is also possible to design these stages in current mode using simple current mirrors, which do not require the wide bandwidth op-amps and large capacitors to save their power dissipation and area [38, 39]. How ever because of their limited accuracy they can be only used in low-resolution applications. There have been also some current mode pipeline ADCs with high speed and medium resolution [40, 41], but they use more

complex circuits, which consume more power and area comparing to voltage-mode pipeline ADCs.

This chapter describes a novel pipeline architecture using combination of voltage-mode and current-mode stages. Section 5.2 presents the architecture and circuit design. Section 5.3 describes the optimization methodology. The simulation results and conclusion are given in section 5.4 and 5.5 respectively.

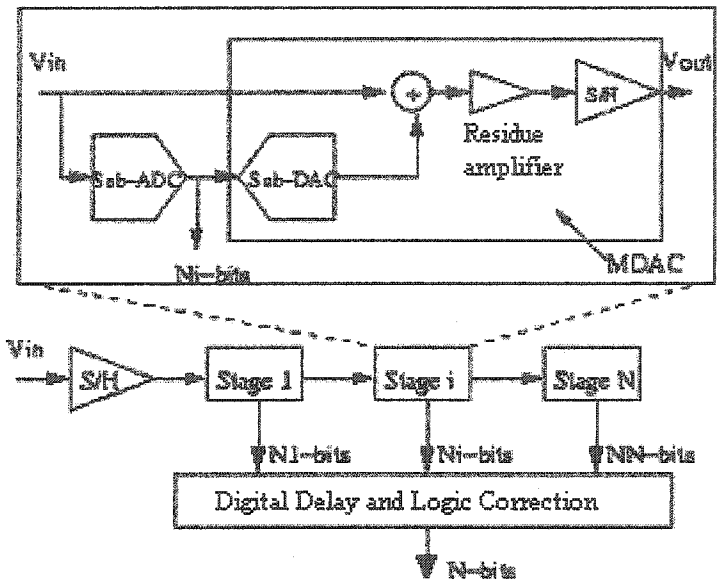


Figure 5.1: Conventional architecture for pipeline ADCs

5.2 Design

5.2.1 Architecture

The block diagram of the proposed architecture is shown in Figure 5.2. . It is consisted of a front-end sample and hold, N voltage-mode stages, a voltage-to-current converter

(VIC), M current-mode stages and a digital logic correction. The resolution of all stages is 1.5-bit [42] therefore 11 stages are required to obtain 12 bits output. Each stage is consisted of a 1.5-bit sub-ADC and a 1.5-bit MDAC, except the last stage, which is a 2-bit flash quantizer. In the following sections, design and optimization are described.

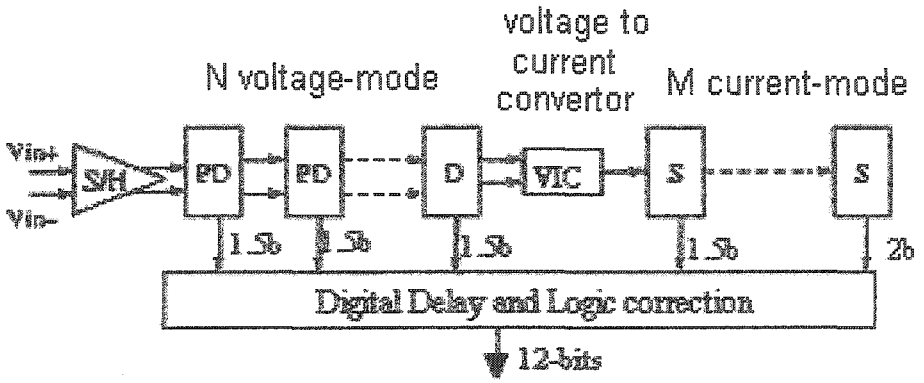


Figure 5.2: The proposed pipeline ADC. PD: pseudo-differential. D: differential. S: single-ended.

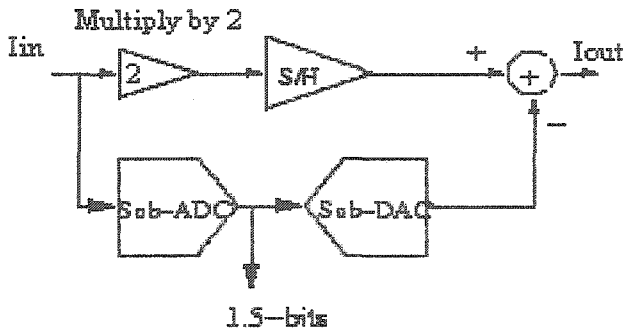


Figure 5.3: Current-mode stages architecture

5.2.2 Current-mode stages

Fig. 5.3 shows the architecture and fig. 5.4 shows the schematic design of the current mode stages. During CK1, the input current is multiplied by 2 and sampled. At the same time the output bits of the SUB-ADC are produced. During CK2 the sampled current is subtracted from appropriate current to produce 2Iin-I1, 2Iin-I2, or 2Iin-I3, depending on the output of the SUB-ADC (X, Y and Z). The current mode stages are single-ended, which are designed using simple low-voltage cascode current mirrors rather than the well-known regulated-cascode current mirrors. This is because the performance of regulated-cascode current mirrors is degraded at high sampling rates. To maximize the accuracy of current mirrors, parametric analysis is used to find the best size of transistors for the current range. In practice the mismatch between transistors will produce error in current mirrors, therefore analog layout techniques are important to reduce the mismatch between transistors. In order to sample current accurately, voltage-sampling technique is used. As shown in fig. 5.4, the gate voltage of M8a is sampled and applied to the gate of M8b, therefore ideally the same current flows through M8b. The op-amps used are regulated cascode and dissipate only 350μW, and their gain is designed to be 20000. To reduce the power dissipation, current is scaled in pipeline stages. In order to estimate the average error in the MDAC, the output was compared with an ideal MDAC for 100 cases. According to our simulation results, average error is about +/-0.3% of the full scale. Fig. 5.8a shows the latch type current comparator [30], with zero static power dissipation. To reduce the kickback noise the size of input transistors is minimized.

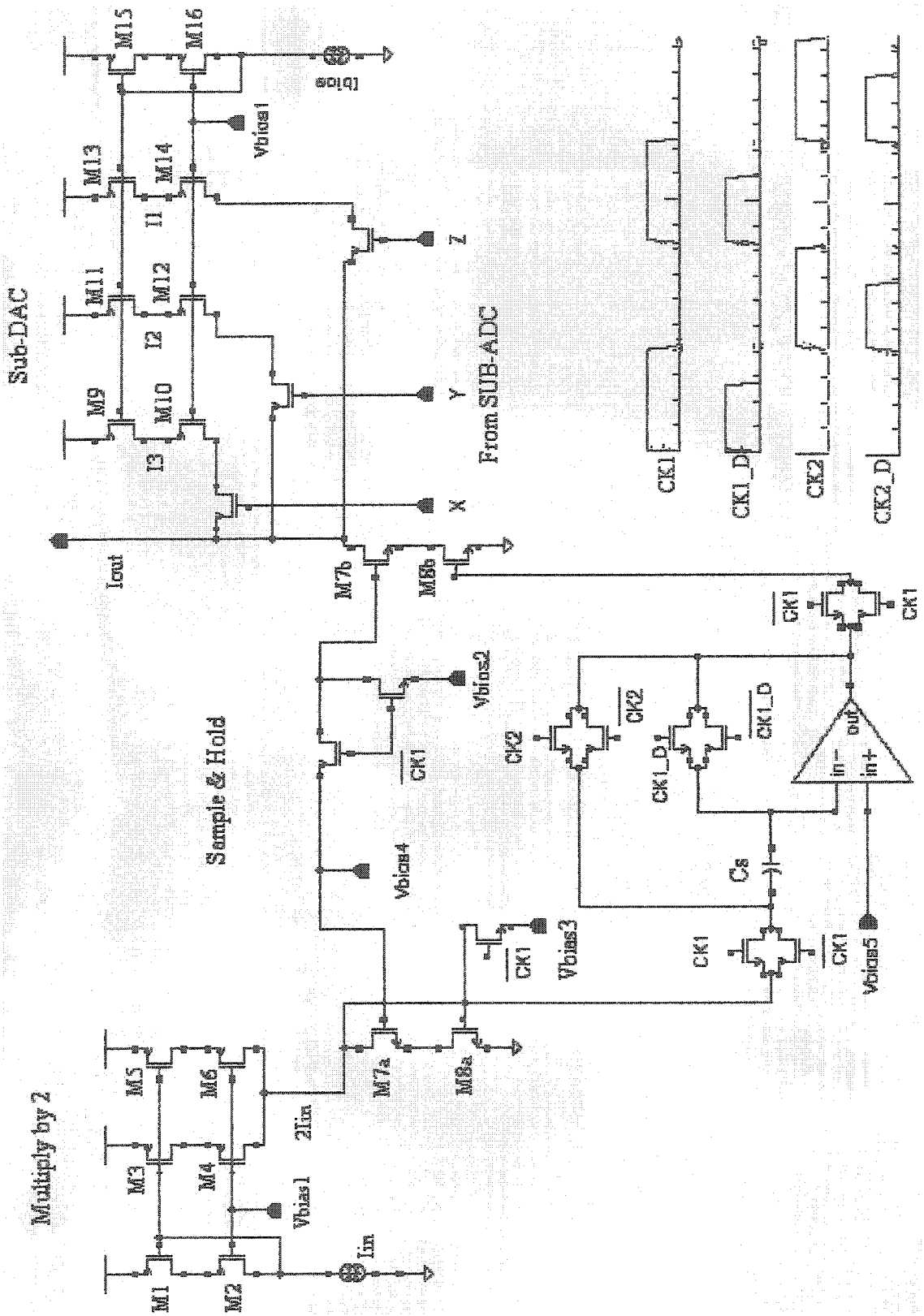


Figure 5.4: 1.5 bit current-mode MDAC and clock phases.

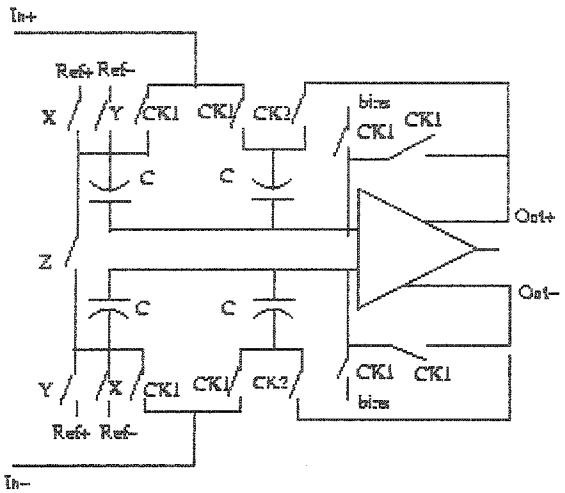


Figure 5.5: 1.5 bit voltage-mode MDAC architecture.

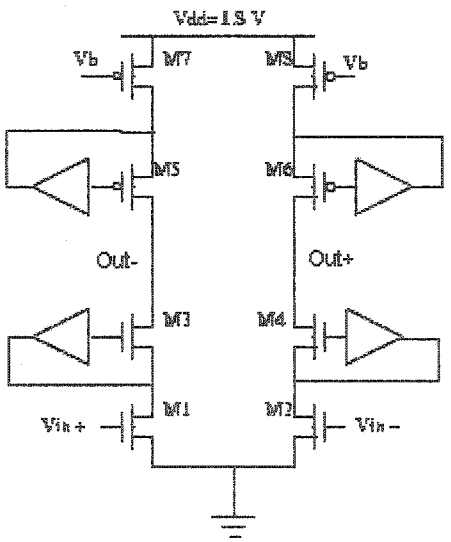


Figure 5.6 (a): Pseudo-differential op-amp.

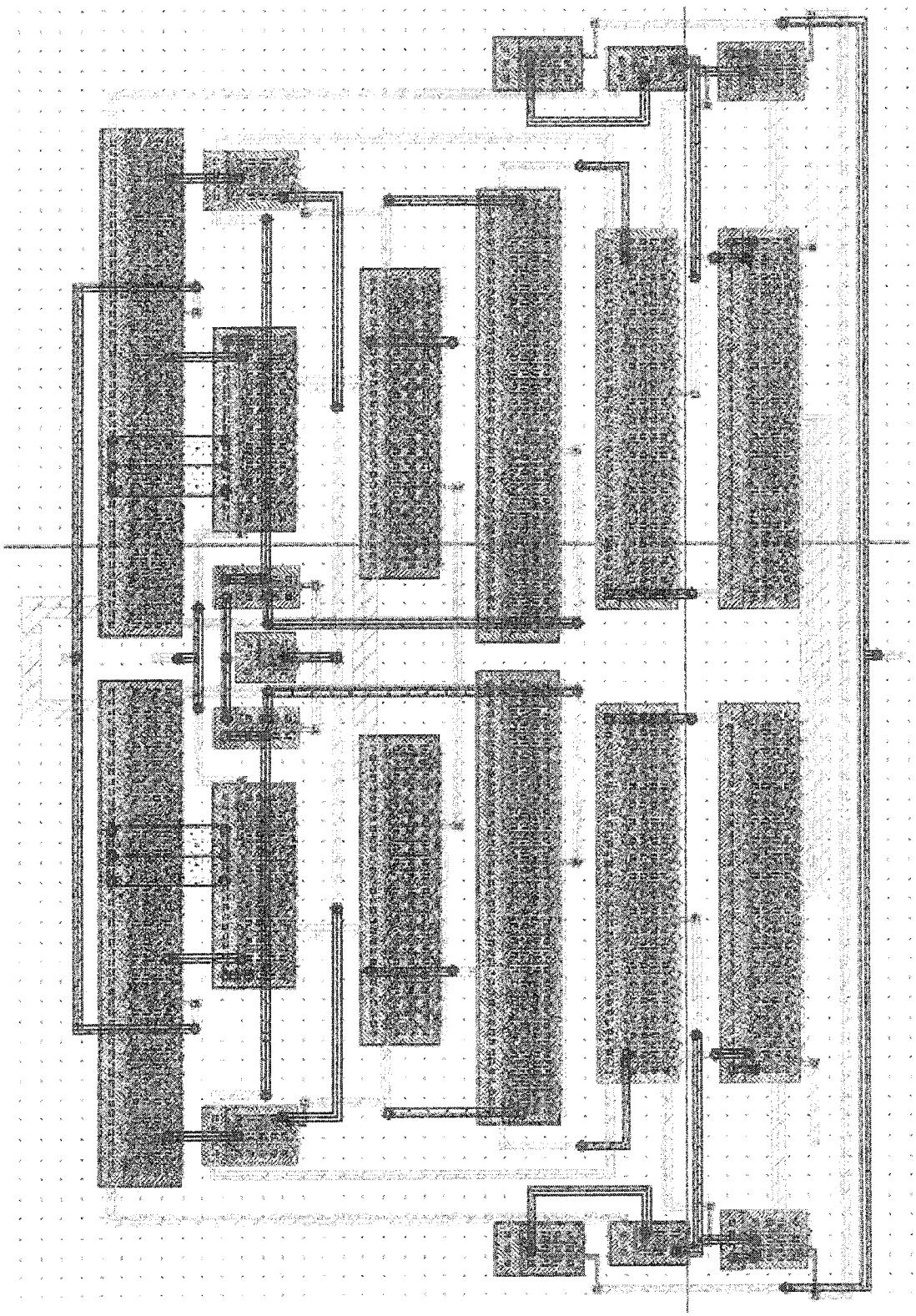


Figure 5.6 (b): Layout design of the pseudo-differential op-amp

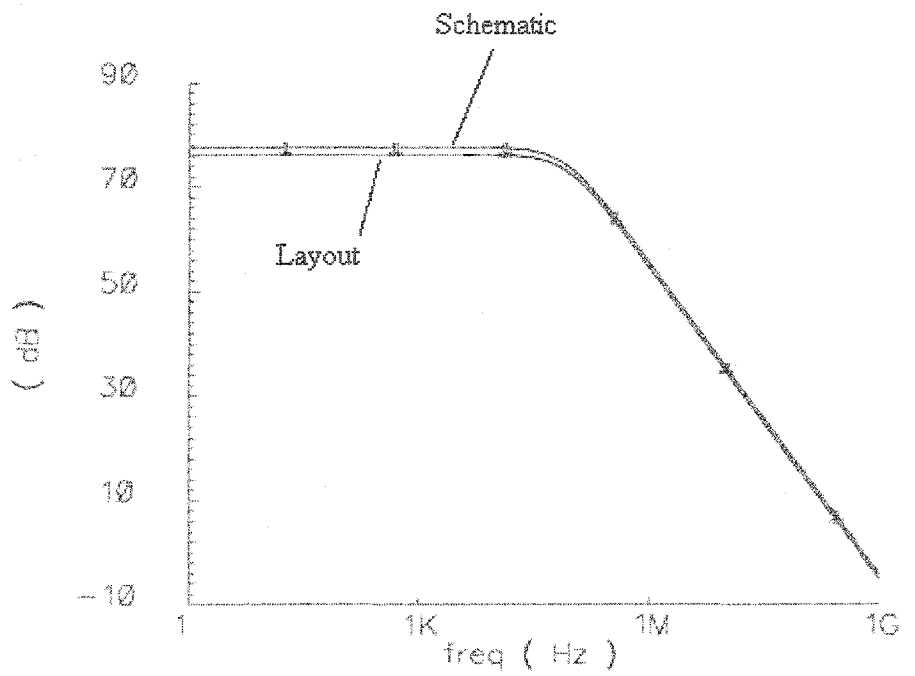


Figure 5.6 (c): Magnitude response of schematic versus post-layout.

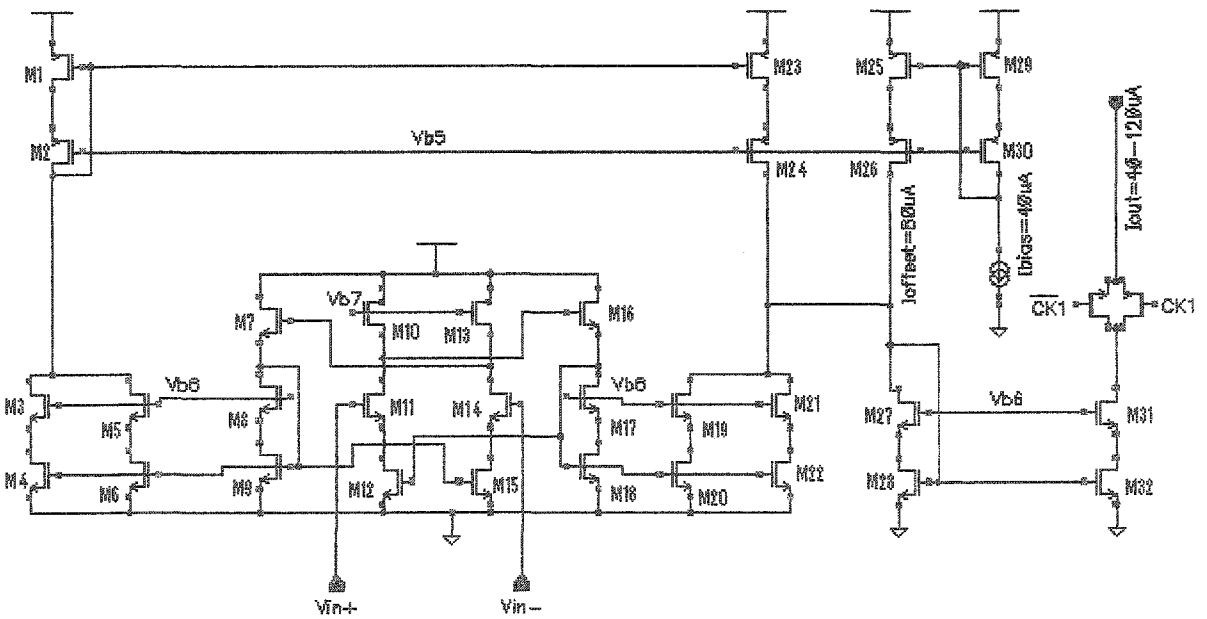


Figure 5.7: A Low-Power VIC with differential input and single-ended output.

5.2.3 Voltage-mode stages

The voltage-mode stages and S/H were designed in voltage-mode using switched capacitor circuit. Figure 5.5 shows the 1.5 bit MDAC architecture. In order to achieve high signal swing, fast settling time with low power dissipation, pseudo-differential cascode op-amps [36] with gain boosting are used. The schematic and layout design of the op-amp are shown in Figure 5.6a and 5.6b respectively. Figure 5.6c shows the magnitude response of schematic and layout. It can be seen there is only a negligible difference between their magnitude responses. Since the input common mode of the VIC must be accurately defined, the last voltage mode stage was designed using fully-differential folded cascode op-amp with common-mode feedback to control the input common-mode level of the VIC. The VIC requires accurate input common mode to produce the correct current range, which can not be defined by pseudo-differential op-amp. To convert voltage to current a low-voltage VIC with high linearity and low power dissipation is used. The schematic of the VIC is shown in fig. 5.7 [43], which is modified to provide single-ended output current from differential input voltage. The input and output ranges are -/+700mV and -/+40μA respectively. An offset current of 80μA is added so that the output current range is always positive from 40μA to 120μA. In order to reduce power dissipation, the output current is only available during sampling mode and is turned off on otherwise. The power dissipation of VIC is about 2.4mW. The total harmonic distortion (THD) of the VIC is about –38dB at 5MHZ full range sine wave and the non-linearity is about +/-0.2% of the full scale. Fig. 5.8b shows the voltage comparator [14]. In order to improve the resolution of the comparator, Nmos M3a and

M3b are added which work as pre-amplifiers. It is important to make sure that M3a and M3b operate in saturation region during the latch regeneration. Therefore transition analysis was used to find the required size of these transistors to operate in saturation region. According to our simulation results, the average error in the voltage mode MDAC is about +/-0.06%.

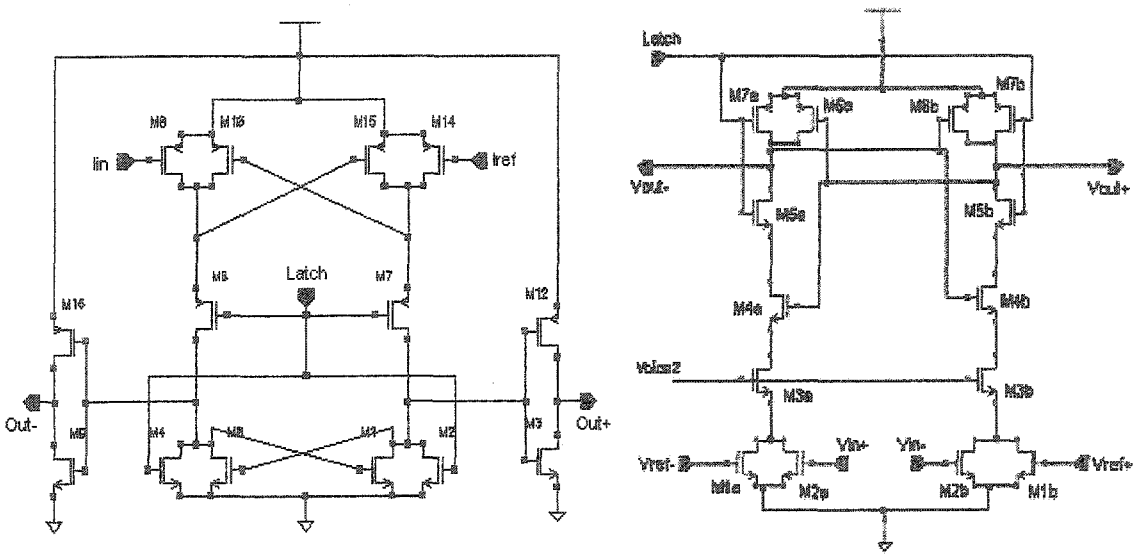


Figure 5.8: (a) Current comparator, (b) Voltage comparator

5.3 Optimization methodology

In order to optimize the pipelined ADC, the number of voltage-mode and current mode stages must be selected such that the total area, power dissipation and propagated error in the stages are minimized. In our analysis, the error of the sub-ADCs is not considered, because they are completely corrected by the digital logic correction. The MDACs in

each stage is modeled as an ideal MDAC plus a source of error which, is added at the output. Using this model the total output-referred error (E) is given by:

$$E = \sum_{j=1}^{M}\left[\sum_{i=1}^{N} G^{N+M-i-j+1}.e_i + G^{M-j+1}.e_{VIC} + G^{M-j}.e_j\right] \qquad (5.1)$$

Where, N is the number of voltage-mode stages, M is the number of current-mode stages, G is the gain of the stages which is 2, e_i is the error of the i^{th} voltage-mode stage, e_j is the error in the j^{th} current-mode stage and e_{VIC} is the error of the VIC. The total power dissipation and area of the pipelined stages are given by:

$$P = \sum_{i=1}^{N} P_i + \sum_{j=1}^{M} P_j + P_{VIC} \qquad (5.2)$$

$$A = \sum_{i=1}^{N} A_i + \sum_{j=1}^{M} A_j + A_{VIC} \qquad (5.3)$$

Where P_i, P_j and P_{VIC} are the power dissipation of voltage-mode, current-mode and VIC stages respectively. A_i, A_j and A_{VIC} represent the area of voltage-mode, current-mode and VIC stages respectively. Using the above formulation the following quantities (Q) are considered for minimization[1]:

$$Q_1 = P \cdot A \cdot E \qquad (5.4)$$

$$Q_2 = P \cdot A \cdot E^{0.5}$$

[1] Other formulations have been investigated and found not useful in the optimization procedure.

However it would be a difficult task to prove that power, area and error are linearly related to each other therefore the analysis is done experimentally. Figure 5.9a, 5.9b and 5.9c show the output-referred error, power and area versus different combination of stages respectively. Figure 5.9d and 5.9e show plot of Q1 and Q2 versus architecture configuration. Figure 5.9d shows that the most optimized configuration occurs when 5 voltage-mode and 6 current-mode stages are implemented. Figure 5.9e shows that the optimized configuration is achieved when 3 voltage-mode and 8 current-mode stages are implemented, however in this case the accuracy might be too low for most of applications according to the output referred error in Fig. 5.9a. In order to keep the accuracy as high as possible the optimization is done based on Q1 criteria.

In pipeline ADCs the required accuracy of stages is relaxed from stage i to stage i+1, as the remaining output bits is reduced from stage i to stage i+1 [44]. This allows optimizing each stage based on its required accuracy. Therefore the sampling capacitors are scaled down in pipelined stages which, allows reducing biasing current of the op-amps. Table I shows the estimated power dissipation and area of each stage. The power dissipation was estimated using cadence SpectreS simulator. The area was estimated by summing the area of each transistor and capacitor and adding 100% for interconnections spacing. Table II shows the estimated power and area for a conventional fully-differential pipeline ADC. It can be seen that both power dissipation and area are significantly reduced. This is because in conventional fully-differential pipeline ADC, the folded-cascode op-amps require large biasing current to achieve high bandwidth, however in the proposed design, only the third stage uses a differential folded-cascode op-amp. Also

voltage mode stages require 4 large capacitors, but the current-mode stages require only one capacitor, reducing the area.

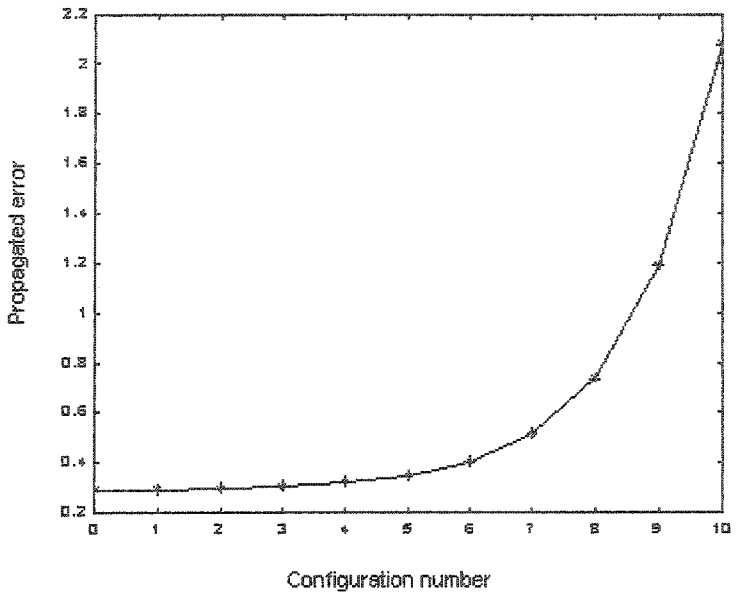


Figure 5.9a: Output-referred error versus configuration

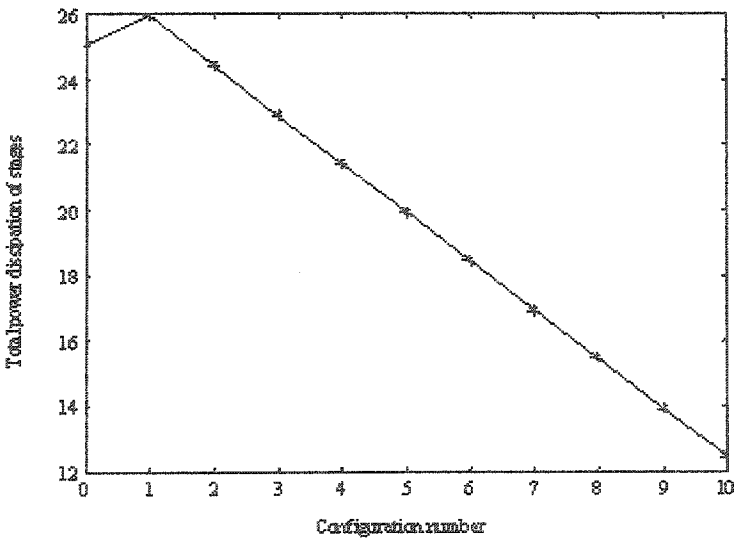


Figure 5.9b: Total power dissipation versus configuration

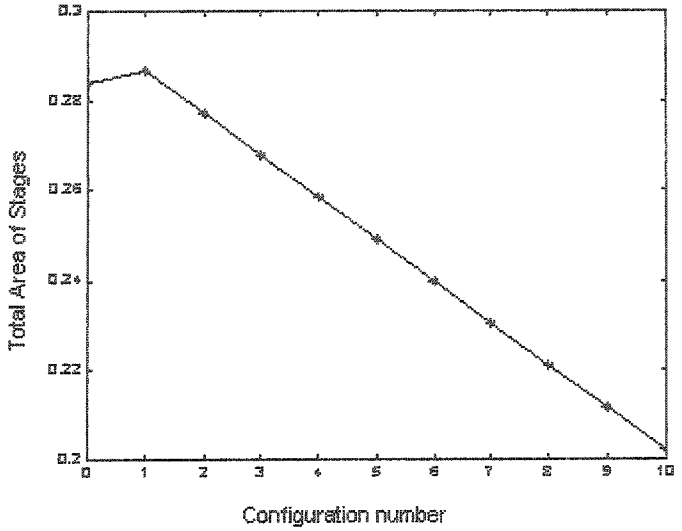


Figure 5.9c: Total area versus configuration

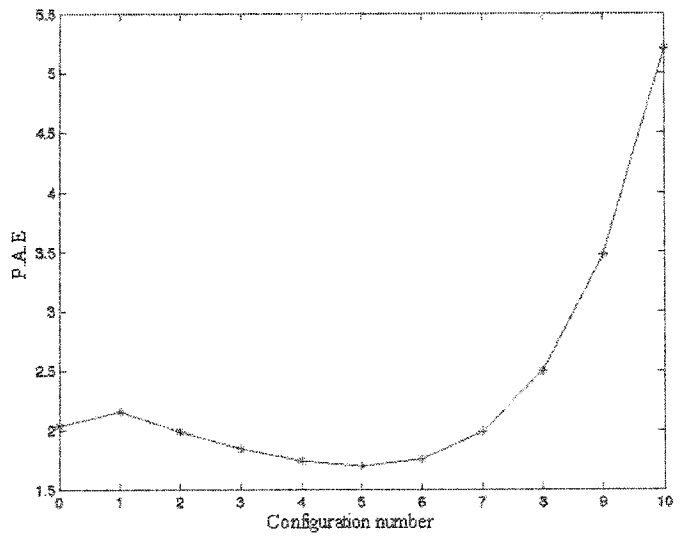


Figure 5.9d: Q1 versus configuration

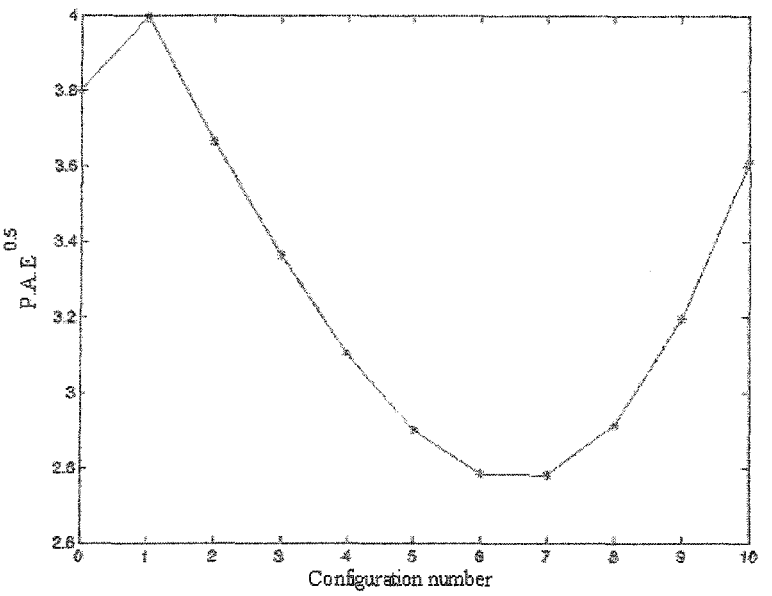


Figure 5.9e: Q2 versus configuration

Table 5.1: Estimated average power dissipation and area of the proposed pipeline ADC stages.

Stage	Type	Sampling Capacitance	Power dissipation	Area mm^2
S/H	PD	1.1 pF	2.2 mW	0.016
1^{st},2^{nd}	PD	0.5 pF	2.45 mW	0.0284
3^{rd},4^{th}	PD	0.4 pF	2.1 mW	0.027
5^{th}	D	0.3 pF	3.84mW	0.0315
VIC	S		2.4 mW	0.012
$6,7^{th}$	S	0.25 pF	1.1 mW	0.019
$8\text{-}10^{th}$	S	0.25 pF	0.8 mW	0.019
11^{th}	S		0.3 mW	0.004
Total			22.44 mW	0.2693

Table 5.2: Estimated average power dissipation and area of fully differential pipeline ADC stages.

Stage	Type	Sampling Capacitance	Power dissipation	Area mm^2
S/H	D	1.1pF	4.3mW	0.02
1^{st},2^{nd}	D	0.5pF	4.5mW	0.032
3^{rd},4^{th}	D	0.4pF	4mW	0.0315
$5,6^{th}$	D	0.3pF	3.84mW	0.03
$7,8^{th}$	D	0.25pF	2.15mW	0.025
$9,10^{th}$	D	0.25pF	2mW	0.025
11^{th}	D		0.3mW	0.006
Total			37.58mW	0.313

5.4 Results

Fig. 5.10 shows a plot of fast Fourier transform (FFT) of the output at 40Msamples/s with 4 MHZ input signal. The SFDR which shows the purity of the signal is 62.5 dB. The SNDR is 58.3dB. However SNDR is reduced to 56.2 dB at 5MHZ. A significant part of signal distortion is due to the sample and hold which, degrades the accuracy at higher input frequencies. Table 5.3 summarizes the specifications of the ADC.

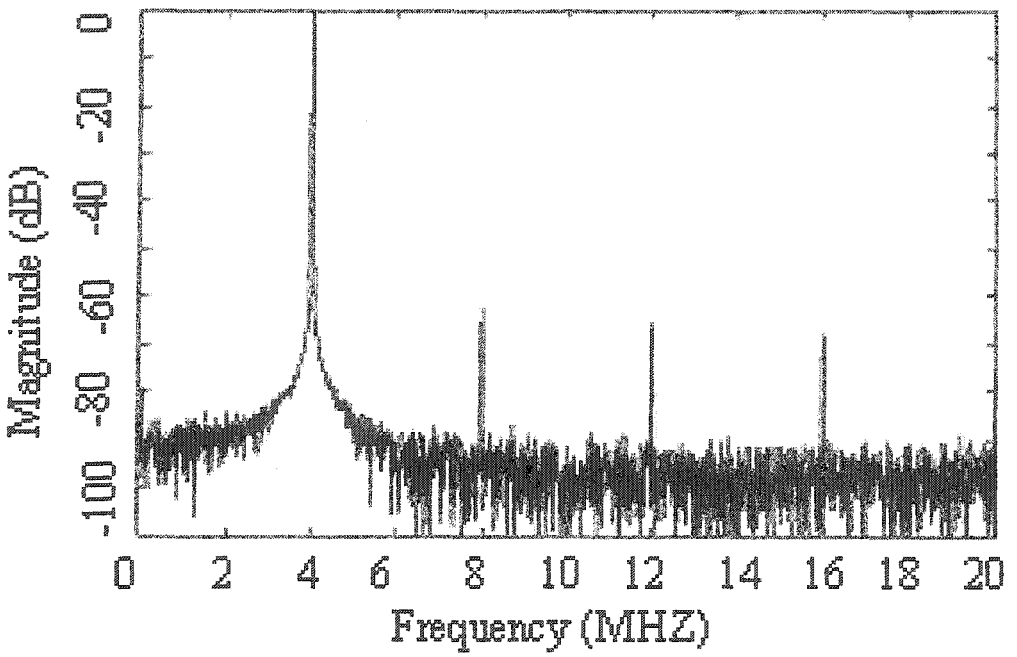


Figure 5.10: FFT spectrum at 40 MS/s and 4 MHZ input.

Table 5.3: ADC specifications

Technology	0.18-μm TSMC CMOS
Supply Voltage	1.8 V
Resolution	12-bits
ENOB	9.5-bits
Sampling Rate	40-Msample/s
Full Scale input range	1.4 V_{P-P}
SFDR@ 4MHZ (5MHZ)	+62.5dB (59.2 dB)
SNDR@ 4MHZ (5MHZ)	58.3dB (56.2dB)
SNR@ 4MHZ (5MHZ)	-63dB (-66dB)
Estimated Area of ADC	0.36 mm^2
Estimated Power dissipation of ADC	24.5mW

5.5 Conclusions

In this chapter design of a novel pipeline ADC was presented in details. It was shown that the proposed pipeline architecture using combination of current-mode and pseudo-differential voltage-mode is suitable for design of low power, low area and high speed ADCs. According to the simulation results, the accuracy of the designed pipeline ADC was limited by the performance of the front-end S/H and not but the ADC, therefore by improving the speed of the S/H, better accuracy can be achieved at high frequencies. . Table 5.4 shows various ADCs along with some of their performance parameters.

In order to compare this design with other published works, FOM1 and FOM2 are calculated and plotted (Figure 5.11 and 5.12). It can be concluded that using the described design, it is possible to reduce power dissipation and area comparing to conventional fully differential schemes. It is known that scaling down the voltage can actually result in higher power dissipation in conventional voltage-mode pipeline ADCs [1] therefore it is expected that the proposed design be more useful for future low-voltage CMOS technologies due to current-mode stages, since the power dissipation of current mode stages is reduced by scaling voltage.

Table 5.4: Summary of published works for pipeline ADCs.

ADC	Resolution	Speed	Power dissip.	ENOB	Area	Technology	Year
Miyazaki [36]	10-bit	30 MSPS	16mW	8.71	3.12mm^2	0.3 µm	2003
Aslanzadeh [45]	12-bit	25 MSPS	76mW	11.35	N/A	0.35 µm	2003
ADC10321 [46]	10-bit	20 MSPS	98mW	9.2	N/A	N/A	2003
ADC10030 [47]	10-bit	30 MSPS	125mW	9.1	N/A	N/A	2003
Blum [48]	10-bit	100 MSPS	180mW	8.83	0.43mm^2	0.12 µm	2002
Sang [49]	10-bit	120MSPS	208mW	9.37	3.6mm^2	0.25 µm	2002
Chang [50]	10-bit	25MSPS	21mW	7.68	2.24mm^2	0.35 µm	2002
Jamal [51]	10-bit	120MSPS	234mW	9.14	12.5mm^2	0.35 µm	2002
Thompson [52]	15-bit	20MSPS	380mW	14.66	13.76mm^2	0.5 µm	2001
Mikko [6]	10-bit	200MSPS	405mW	6.85	7.4mm^2	0.5 µm	2001
Hamedi [53]	10-bit	50MSPS	65mW	9.17	1.2mm^2	0.25µm	2001
Kwak [54]	15-bit	5MSPS	130mW	13.8	27.3mm^2	1.4 µm	1997
This work	12-bit	40MSPS	24.5mW	9.5	0.36 mm^2	0.18µm	2004

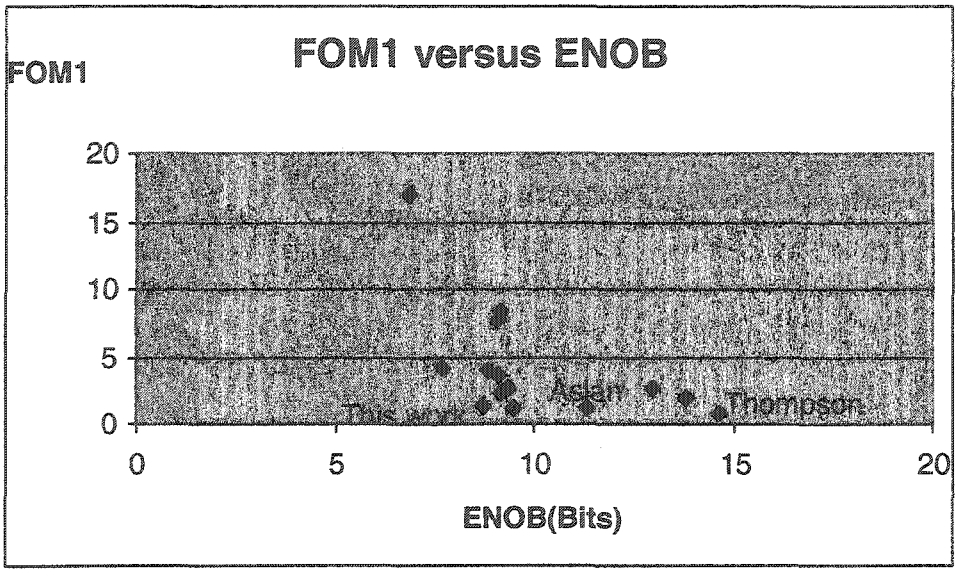


Figure 5.11: FOM1 versus ENOB

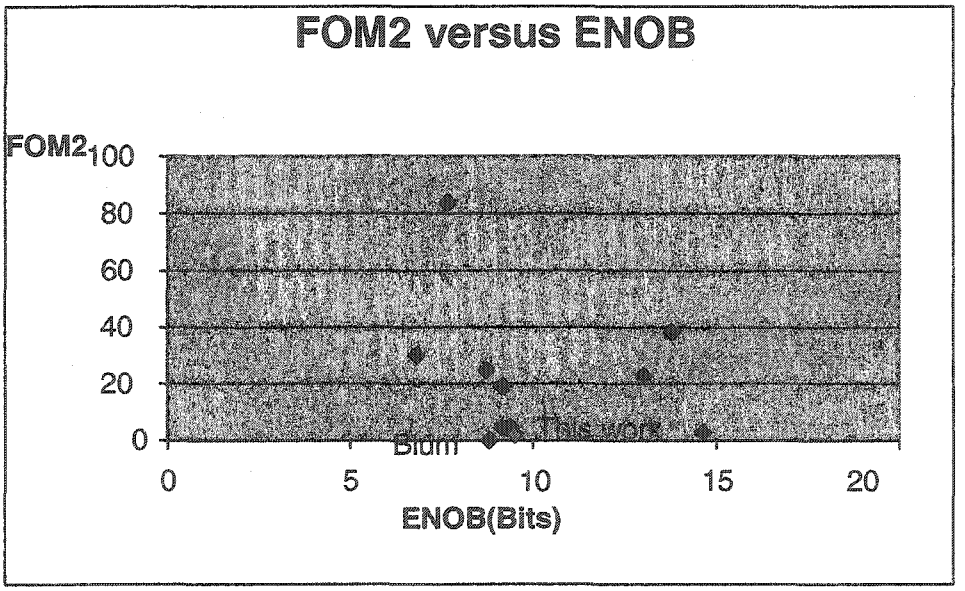


Figure 5.12: FOM2 versus ENOB

Chapter 6

Conclusions and future works

The focus of this thesis was optimization of pipeline ADCs in terms of power dissipation and area such that integration of analog and digital circuits in one microchip becomes more efficient.

In chapter 2, a number of well-known analog to digital conversion techniques and their applications were reviewed. For very high resolution and low-speed applications the successive approximation and sigma-delta architectures are feasible in terms of power dissipation. However if high conversion rate is required, pipelined ADCs have superior performance. It was also shown that the advantage of using the pipeline architecture over sub-ranging and flash architectures is the reduced number of comparators and high conversion rate with lower power dissipation. Also a number of parameters to evaluate static and dynamic performance of ADCs were given.

In chapter 3, design considerations for pipelined ADCs at the architecture level was discussed. Effect of non-idealities in the flash quantizers and the MDACs on the pipeline ADCs was analyzed. The effect of errors in the flash quantizers can be completely corrected using the digital logic correction. The errors produced by the MDACs can be

reduced by applying digital or analog calibration techniques. Therefore the accuracy of pipeline ADCs is limited by performance of the MDACs.

Chapter 4 focused on circuit design considerations for pipeline ADCs. The limitations of low-voltage design on switches and op-amps were discussed. Also current-mode and voltage-mode designs were compared and their advantages and disadvantages were analyzed. The main advantage of current-mode design is low power dissipation, however the trade off is less accuracy due to mismatch between transistors in the current mirror. Also effect of op-amp topology on the performance of pipeline ADCs was analyzed. It was shown that for high-speed and medium bandwidth, single stage topologies such as the pseudo-differential cascade op-amp are more efficient. If high bandwidth is required, 2-stage topologies can meet the requirements due to greater transconductance. The draw-back of using 2-stage op-amps is lower speed. By applying parallelism the speed of pipeline ADCs is increased.

In chapter 5, a novel pipeline architecture was proposed and a 12-bit 40Msamples/s pipeline ADC was designed. It was shown that by using voltage-mode stages in the front-end and current-mode stages at the back-end, more optimized design can be achieved compared to the conventional voltage mode schemes.

Although the designed ADC consumes low-power and area, its bandwidth is limited to about 5MHZ. This is mainly due to performance degradation of the front-end S/H circuit at higher frequencies. As explained in chapter 4, in applications which require wide-band ADCs (example: radio receivers), high transconductance op-amps such as 2-stage topologies in the S/H will improve the ADC bandwidth. However parallelism must be

applied to increase the sampling rate. For future work development of a wide-band pipeline ADC by using a parallel-pipeline architecture and wide-band S/H will be useful. Also development of calibration techniques in analog or digital domain is necessary to reduce the effect of errors in the MDACs and to improve linearity.

Bibliography

[1] Andrew M. Abo and Paul R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter", IEEE Journal of solid-state circuits, vol. 34, no. 5, may 1999

[2] Li Fanghui; Ren Lixiang; Long Teng; Tian Liyu, "High-speed data acquisition and digital signal processing of monopulse Doppler radar system", 2000. WCCC-ICSP 2000. 5th International Conference on Signal Processing Proceedings, Volume: 3, 21-25 Aug. 2000, pp:1876 - 1880 vol.3

[3] Amantia, P.J.; Kane, M.J.; Kimball, E.A.; Garverick, S.L., "A mixed-signal IC for a semi-implantable hearing aid", 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on Circuits and Systems, Volume: 1, 30 May-2 June 1999 pp:186 - 189 vol.1

[4] Adel Sedra and Kenneth Smith; "*Microelectronic Circuits*" Oxford, 1998.

[5] B.E. Boser and B.A. Wooly, "The Design of sigma-delta modulation analog-to-digital converters", IEEE J. Solid-State Circuits, vol. 23, pp.1298-1308, Dec. 1998.

[6] Lauri Sumanen, Mikko Waltario, Kari A.I. Halonen," A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter", IEEE J. of Solid-State Circuits, Volume: 36 , Issue: 7 , July 2001 pp:1048 – 1055.

[7] J. Goes, J. C.Vital."*Systematic Design for Optimization of Pipelined ADCs.*" Kluwer Academic Publishers, 2002

[8] Rudy Van De Plassche, "*Integrated Analog-To-Digital and Digital-To-Analog Converters*", Kluwer Academic Publishers, 1994

[9] Joey doernburg, Hae-Seung Lee and David A. Hodges, "Full-Speed Testing of A/D Converters", IEEE J. of Solid-State Circuits, Volume: 19, Issue: 6, Dec 1984 pp:820 – 827.

[10] Frank Goodenough, "Analog Technology of all Varieties Dominate ISSCC", Electronic Design, 1996.

[11] B.S Song, S.H. Lee and M.F. Tompset, "A 10-b 15-MHz CMOS Recycling Two-Step A/D Converter", IEEE Journal of Solid-State Circuits, Volume: 25, Issue: 6, Dec. 1990 pp:1328 - 1338

[12] E.G. Soenen and R.L. Geiger, "An Architecture and An Algorithm for Fully Digital Correction of Monolithic Pipelined ADCs", IEEE Transactions On Circuits and Systems, vol 42, 1995.

[13] S.H. Lewis, H.S. Fetterman, G.F. Gross Jr., R. Ramachandran and T.R. Viswanathan, "A Pipelined 9-Stage Video-Rate Analog-To-Digital Converter", IEEE 1991 Custom Integrated Circuit Conference 12-15 May 1991 pp:26.4/1 - 26.4/4

[14] T.B. Cho and P.R. Gray, "A 10b, 20Msample/s, 35mW Pipeline A/D Converter", IEEE J. of Solid-State Circuits, vol. 30, 1995.

[15] S.H. Lewis, R. Ramachandran and M. Snelgrove, "Indirect Testing of Digital-Correction Circuits in Analog-to-Digital Converters with Redundancy", IEEE Trans. On Circuits and Systems, vol 42, 1995.

[16] Y. Lin, B. Kim and P. Gray. "A 13-b 2.5-MHZ Self-Calibrated Pipelined A/D Converter in 3-μm CMOS." IEEE J. of Solid-State Circuit, Vol 26, pp. 628-636, 1991.

[17] L. Singer, S.Ho, M. Tikko, D.Kelly, "A 12b 65Msample/s CMOS ADC with 82dB SNDR at 120MHZ." ISSCC Digest of Technical Papers, pp. 38-39, 2000.

[18] Andrew Masami Abo, "Design for Reliability of Low-voltage, Switched-capacitor Circuits", PHD Thesis, University of California, Berkeley, 1999.

[19] B. Razavi, "*Design of Analog CMOS Integrated Circuits.*" 1999, MC Graw-Hill.

[20] B. Vaz, N. Paulino, J. Goes, R. Tavares and S. Garcao, "Design of Low-Voltage CMOS Pipelined ADCs using 1 Pico-Joule of Energy per Conversion", ISCAS, 2002. Volume: 1, 26-29 May 2002 pp: I-921 - I-924 vol.1

[21] M. Walttari, L. Sumanen, T. Korhonen and K. Halonen, "A Self-Calibrated Pipeline ADC with 200MHz IF-Sampling Frontend" Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. IEEE International, Volume: 1 , 3-7 Feb. 2002 pp:314 - 469 vol.1

[22] Klein, P.; Chladek, S. "A new mobility model for pocket implanted quarter micron n-MOSFETs and below", 2001. ICECS 2001. The 8th IEEE International Conference on Circuits and Systems, Volume: 3, 2-5 Sept. 2001 pp:1587 - 1590 vol.3

[23] C. Yu and Y. Liw, "High-speed CMOS current-mode wave-pipelined Analog-to-Digital Converter", The 7th IEEE International Conference on Circuits and Systems, 2000. ICECS 2000, Volume: 2, 17-20 Dec. 2000 pp:907 - 910 vol.2

[24] Edgar Sanchez-Sinencio and Andreas G. Andreou, "*Low-Voltage/Low-power integrated circuits and systems*" December 1998, Wiley-IEEE Press

[25] J.B. Hughes, N.C. Bird and I.C. Macbeth, "Switched currents- a new technique for analog sampled-data signal processing", Proc. of the 1989 IEEE Int. Symp. On Circuits and Systems. 8-11 May 1989 pp: 1584 - 1587 vol.3

[26] Koji Kotani, Tadashi Shibata, and Tadahiro Ohmi, "CMOS Charge-Transfer Preamplifier for Offset-Fluctuation Cancellation in Low-Power A/D Converters," Journal of Solid-State Circuits, vol. 33, May 1998.

[27] Christian Jesus, Gordon W. Roberts, and Mohamad Swan, "Low Power/Low Voltage High Speed CMOS Differential Track and Latch Comparator with Rail-to-Rail Input," Proc. of 2000 IEEE International Symposium on Circuits and Systems. Volume: 5, 28-31 May 2000 pp: 653 - 656 vol.5

[28] Rachelle Ockey and Marek Syrzycki, "Optimization of a Latched Comparator for High-Speed Analog-to-Digital Converters," Proc. of 1999 IEEE Canadian Conference on Electrical and Computer Eng. Volume: 1, 9-12 May 1999 pp:403 - 408 vol.1

[29] J. Terada, Y. Matasuya, F. morisawa, and Y. Kado, "8-mW, 1V, 100-MSPS, 6-Bit A/D Converter using a Transconductance Latched Comparator", AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Conference on ASICs, 28-30 Aug. 2000 pp: 53 - 56

[30] J. Ho and H. C. Luong, "A 3-V, 1.47mW, 120-MHZ Comparator for use in a Pipelined ADC.", IEEE Asia Pacific Conference on Circuits and Systems, 18-21 Nov. 1996

[31] Phillip E.Allen and Douglas R. Holberg, "*CMOS Analog Circuit Design*" 1987. New York.: Oxford University Press.

[32] B. Razavi, "*Principles of Data Conversion System Design*" New York, N.Y.: IEEE Press, 1995.

[33] Ara Hajjar and Gorden W. Roberts, "A Multi-Pass A/D Conversion Technique for Extracting On-Chip Analog Signals," Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, 1998. ISCAS '98., Volume: 2 , 31 May-3 June 1998 pp:280 - 283 vol.2

[34] Behzad Razavi and Bruce A. Wooley, "Design Techniques for High-Speed, High Resolution Comparators," Journal of Solid-States Circuits, December 1992. Volume: 27, Issue: 12, Dec. 1992 pp:1916 - 1926

[35] S. Mathur, M. Das, P. Tadeparthy, S. Ray, S. Mukherjee and Dinakaran B.L.,"A 115mW 12-Bit 50 MSPS Pipelined ADC.", ISCAS 2002. IEEE International Symposium on Circuits and Systems, Volume: 1, 26-29 May 2002 pp:I-913 - I-916 vol.1

[36] Daisuke Miyazaki, Shoji Kawahito and Masanori furuta, "A 10-b 30-MS/s Low-Power Pipelined CMOS A/D Converter Using a Pseudodifferential Architecture", IEEE J. of Solid-State Circuits, Volume: 38 , Issue: 2 , Feb. 2003 pp:369 – 373.

[37] K. Nagaraj, H.S. Fetterman, J. Anidjar, S.H. Lewis and R.G. Renneinger, "A 250-mW,8-b, 52-Msamples/s Parallel-Pipelined A/D Converter with Reduced Number of Amplifiers", IEEE J. of Solid-State Circuits, vol. 32, 1997.

[38] M. Gustavsson and N. Tan, "New Current-Mode Pipeline A/D Converter Architectures", IEEE International Symposium on Circuits and Systems, 1997. Volume: 1, 9-12 June 1997 pp:417 - 420 vol.1

[39] R.C.C Hui and H.C. Luong, "A CMOS Current-Mode Pipeline ADC Using Zero-Voltage Sampling Technique", IEEE International Symposium on Circuits and Systems, 1998. Volume: 1, 31 May-3 June 1998 pp:9 - 12 vol.1

[40] J.W Chung and K.S. Yoon, "Design of 3.3V 10Bit Current-Mode Folding/Interpolating CMOS A/D Converter with an Arithmetic Functionality", IEEE Asia Pacific Conference on ASICs, 2000. 28-30 Aug. 2000 pp:45 - 48

[41] Yu-Yee Liow and C. Wu, "The Design of High-Speed Pipelined Analog-to-Digital Converters Using Voltage-Mode Sampling and Current-Mode Processing

Techniques.", IEEE International Symposium on Circuits and Systems, 2002. ISCAS 2002, Volume: 3, 26-29 May 2002 pp:III-117 - III-120 vol.3

[42] S.H. Lewis, H.S. Fetterman, G.F. Gros, R. Ramachandran and T.R. Viswanathan, "A 10-b 20-MS/s analog-to-digital converter." IEEE J. of Solid-State Circuits, 1992.

[43] C.H. Lin, Tales Pimenta and Mohammed Ismail, "A Low-Voltage Low-Power CMOS V-I Converter with Rail-to-Rail Differential Input for Filtering Applications." 1998 IEEE International Conference on Circuits and Systems, Volume: 1, 7-10 Sept. 1998 pp: 165 - 168

[44] S.H. Lewis "Optimizing the Stage Resolution in Pipelined Multistage Analog-to-Digital Converters for Video-Rate Applications" IEEE Trans. On Circuits and Systems,1992, pp 516-523.

[45] H.A. Aslanzadeh, S. Mehrmanesh, M.B Vahidfar and A.Q. Safarian, "A Low power 25MS/S 12-bit Pipeline Analog to Digital Converter For Wireless Applications", Southwest Symposium on Mixed-Signal Design, 23-25 Feb. 2003 pp:38 - 42

[46] National Semiconductor, "10-bit, 20 MSPS, 98mW A/D Converter" Product Manual, 2003.

[47] National Semiconductor, "10-bit, 30 MSPS, 125mW A/D Converter" Product Manual, 2003.

[48] A.S. Blum, B.H. Engi, H.P. Eichfield, R. Hagelauer and A. Abid, "A 1.2V 10-b 100-Msamples/s A/D Converter in 0.12μm CMOS", Symposium on VLSI Circuits Digest of Technical Papers, 2002., 13-15 June 2002 pp:326 - 327

[49] Sang M. Yoo, T. Oh, J. Moon, S. Lee and U. Moon, "A 2.5V 10b 120 Msample/s CMOS Pipelined ADC with high SFDR" Proceedings of the IEEE Custom Integrated Circuits Conference. 12-15 May 2002 pp:441 – 444

[50] D.Y. Chang, Lei Wu and U. Moon, "Low-Voltage Pipelined ADC Using Opamp-Reset Switching Technique." Proceedings of the IEEE Custom Integrated Circuits Conference, 12-15 May 2002 pp:461 - 464

[51] S.M Jamal, Daihong Fu, P.Hurst and S.H. Lewis, "A 10b 120Msamples/s Time-Interleaved Analog-to-Digital Converter with Digital Background Calibration", IEEE Journal of Solid-State Circuits, Volume: 37 , Issue: 12 , Dec. 2002 pp:1618 - 1627

[52] D.U Thompson, and B.A. Wooley, "A 15-b Pipelined CMOS Floating-Point A/D Converter", IEEE J. of Solid-State Circuits, Volume: 36, Issue: 2, Feb. 2001 pp: 299 – 303.

[53] S. Hamedi-Hagh and C.A.T. Salama, "A 10Bit, 50Msample/s, Low Power Pipelined A/D Converter For Cable Modem Applications", ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems, Volume: 1, 6-9 May 2001 pp: 424 - 427

[54] S.U. Kwak, B.S. Song and K. Bacrania, " A 15-b 5Msample/s Low-Spurious CMOS ADC", IEEE Journal of Solid-State Circuits, Volume: 32, Issue: 12, Dec. 1997 pp:1866 - 1875

Vita Auctoris

Name: Mani Mohajerin

Place of Birth: Tehran, Iran

Year of Birth: 1974

Education: University of Windsor, Windsor, Ontario

1996-2000, B. A. Sc

University of Windsor, Windsor, Ontario

2002-2004, M. A. Sc