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A $\Sigma\Delta$ Modulator for Digital Hearing Instruments Using 0.18 μm CMOS Technology

by

Iman Yassin Taha

A Thesis

Submitted to the Facility of Graduate Studies and Research
through Electrical and Computer Engineering in Partial
Fulfillment of the Requirements for the Degree
of Master of Applied Science at the
University of Windsor

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Abstract

This thesis develops the design methodology for a low-voltage low-power $\Sigma\Delta$ Modulator, realized using a switched op-amp technique that can be used in a hearing instrument. Switched op-amp implementation allows scaling down the design to the latest CMOS technology. A single-loop second-order $\Sigma\Delta$ Modulator topology is chosen. The modulator circuit features reduced complexity, area reduction and low conversion energy. The modulator has a sampling rate of 8.2 MHz with an over-sampling ratio (OSR) of 256 to provide an audio bandwidth of 16 kHz. The modulator is implemented in a 0.18 μm digital CMOS technology with metal-to-metal sandwich structure capacitors. The modulator operates with a supply voltage of 1.8 V. The active area is 0.403 mm^2 . The modulator achieves a 98 dB signal-to-noise-and-distortion ratio (SNDR) and a 100 dB dynamic range (DR) at a Nyquist conversion rate of 32 kHz and consumes 1321 μW with a joule/conversion figure of merit equal to 161×10^{-12} J/s.

The design methodology is developed through the extensive use of simulation tools. The behaviour simulation is carried out using Matlab/ SIMULINK while circuits are simulated with Hspice using the Cadence design tools. Full-custom layout for the analog and the digital circuits is performed using the Cadence design tool. Post-processing simulation of the extracted modulator with parasitic verifies that results meet the requirements. The design has been sent to CMC for fabrication.

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Abbreviations

ADC	Analog-to-digital converter
CM	Common-mode
CMFB	Common-mode feedback
CMOS	Complementary metal-oxide semiconductor
DAC	Digital-to-analog converter
DR	Dynamic range
DRC	Design rule checker
FF	Flip-flop
FOM	Figure-of-merit
GBW	Gain bandwidth product
GUI	Graphical user interface
LVS	Layout versus schematic
MOSFET	Metal-oxide semiconductor field effect transistor
NMOST	Negative-channel metal-oxide semiconductor transistor
NTF	Noise transfer function
Op-Amp	Operational amplifier
OSR	Oversampling ratio
PMOST	Positive-channel metal-oxide semiconductor transistor
PSD	Power spectral density
RMS	Root mean square
RC	Resistance capacitor
SC	Switched capacitor
$\Sigma\Delta$	Sigma-delta
SNDR	Signal-to-noise and distortion ratio

SNR	Signal to noise ratio
SO	Switched op-amp
SOC	System on chip
SR	Slew rate
SR FF	Set-reset flip-flop
STF	Signal transfer function
VLSI	Very large scale integration

Chapter 1

Introduction

1.1 Motivation

Modern electronics systems in computers, communications, automotive and instrumentation are mostly mixed-signal systems. An analog to digital converter (ADC) is a standard building block, unavoidable as interface between the analog world and the digital signal processing hardware. The market for portable electronic systems and system-on-chip (SOC) such as wireless communications devices and hearing aids, is continuously expanding. Both low voltage and low power operation are of great importance for portable applications and SOC. Low voltage operation is demanded because it is desirable to use as few batteries as possible for size and weight considerations. Low power consumption is necessary to ensure a reasonable battery lifetime.

The $\Sigma\Delta$ converters are based on noise shaping and over-sampling. It has been known for nearly thirty years, but only recently has the technology of high-density digital VLSI existed to manufacture them as inexpensive integrated circuits. Without the CMOS technology, the digital filtering required in $\Sigma\Delta$ converters for decimation and interpolation makes these circuits too expensive. Low voltage low power design can be achieved as the CMOS technology is scaled down. $\Sigma\Delta$ converters have low sensitivity to the component mismatches at the price of extensive use of digital processing [1].

There are a lot of architectures available to implement $\Sigma\Delta$ converters, from single-loop [2] to the more sophisticated with multiple feedback loops, cascade connection or multi-bit quantization [3] [4] [5] [6] [7] [8]. Most of these architectures have been successfully implemented. CMOS $\Sigma\Delta$ converters with 20-bit effective resolution in instrumentation [9] [10] [11], 16-bit in audio and data acquisition [12] [13] [14] [15] [16] and 12-bit or more in communications are feasible [17] [18] [19] [20].

The first and probably largest application of $\Sigma\Delta$ converters is in the field of digital telephony [21]. Digital audio is the most obvious application that takes full advantage of

the inherent qualities of $\Sigma\Delta$ converters [22] [23] [24] [25] [26]. For digital-audio applications, the previous researches have already proven that switched-capacitor (SC) $\Sigma\Delta$ structure is a good candidate. However, these works either employ supply voltages as high as 5 V [27], or use out-of-date CMOS technologies with bigger transistor channel lengths [27] [28]. In the 0.18 μm technology, $\Sigma\Delta$ modulator is presented for digital-audio applications using a bootstrapped switch [29]. To the author's knowledge, there is a lack of papers on implementation of digital-audio $\Sigma\Delta$ modulators with guaranteed performance that is compatible with the latest CMOS technologies. The market does post a continuing demand to design $\Sigma\Delta$ modulators using technologies with channel length as small as 0.18 μm or even smaller to be compatible with the latest CMOS technologies and with less area-occupation, high-resolution, and low power.

1.2 Objectives

This thesis investigates the development of a switched op-amp (SO) $\Sigma\Delta$ modulator for digital-audio instrumentations to provide compatibility with the continuously decreasing CMOS technology feature size. The specific design objectives are:

1. To develop a top down design methodology in order to perform an analysis at the system architectural level before starting transistor level design. To use Matlab/ SIMULINK to implement the system architecture and model non-idealities.
2. To choose the proper topology to design the $\Sigma\Delta$ modulator for digital-audio instrumentations, while considering low-power and low-voltage design constraints.
3. To carry out the design of the individual building blocks using the 0.18 μm CMOS process. To integrate the building blocks. To verify the designed individual circuits and the whole modulator by simulation using Hspice in the Cadence design tools.
4. To implement the Layout considering the mixed-signal design requirements. To verify that the designed $\Sigma\Delta$ modulator meets the

required specifications thought post-simulation with parasitic and testing the fabricated chip.

1.3 Thesis Organization

Chapter 2 is an introduction to $\Sigma\Delta$ modulators. It includes discussing oversampling ADC, analyzing the behavior of $\Sigma\Delta$ modulators in the Z-domain and discussing the performance metrics. The motivation for top-down design methodology is discussed and the implemented methodology for this work is shown. In Chapter 3 different kinds of topologies are compared and the reasons for selecting the single-loop, second-order $\Sigma\Delta$ modulator for this work are discussed. Non-idealities issues associated with $\Sigma\Delta$ modulator design and modeling in MATLAB/ SIMULINK are given and the behavior simulation to optimize the system and building blocks parameters is then developed. In Chapter 4, the switch design constraint and low-voltage, low-power design techniques are addressed. Chapter 5 focuses on the implementation of each building block in the TSMC 0.18 μm CMOS technology with the simulation results from the analog environment of the cadence design tool. Chapter 6 deals with integrating the building blocks to implement the SO $\Sigma\Delta$ modulator and simulating the results. In Chapter 7, conclusion remarks and recommendations for future work are discussed.

Chapter 2

$\Sigma\Delta$ Modulator Basic Concepts

This Chapter introduces the concept of oversampling ADC, describes the basic function of the $\Sigma\Delta$ Modulator and explains how the $\Sigma\Delta$ Modulation is so beneficial for generating high-resolution data. The performance criteria that are necessary to measure the performance of the $\Sigma\Delta$ Modulator are defined. A top-down design methodology using SIMULINK for the design of $\Sigma\Delta$ modulator is discussed. The motivation and the benefits of the top-down optimization are presented, which featured a shorter design cycle, along with ease of implementation and reproducibility. The design steps for the SO $\Sigma\Delta$ modulator are summarized

2.1 Oversampling ADC

Analog-to-digital converters can be separated into two categories depending on the rate of sampling. The first category samples the input at the Nyquist rate, such that:

$$f_N = 2F$$

Where F is the signal bandwidth and f_N is the sampling rate. The second type samples the signal at a rate much higher than the signal bandwidth. This type is called the oversampling converter [30].

Figure 2-1 shows the typical process used in ADC. After filtering the signal, to help minimizing aliasing effects, the signal is sampled, quantized, and encoded using simple digital logic to provide the digital data in the proper format.

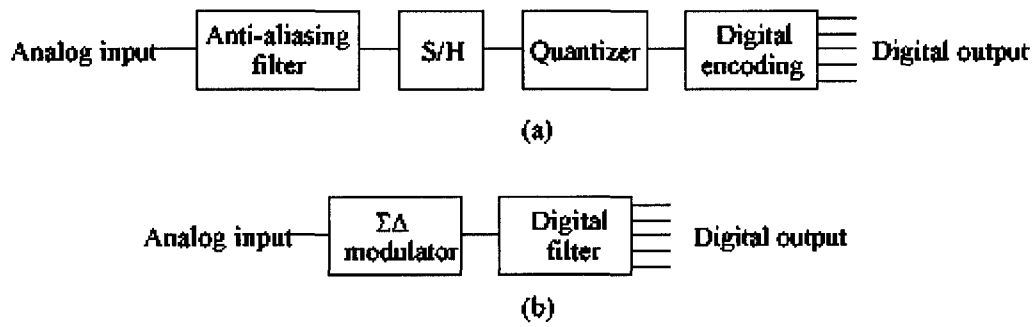


Figure 2-1. Typical ADCs block diagrams. (a) Nyquist rate ADC. (b) Oversampling ADC

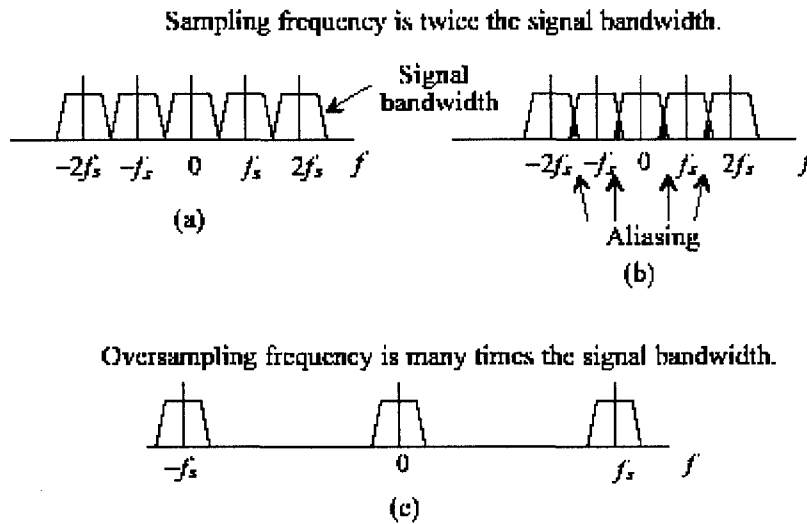


Figure 2-2. Nyquist rate and oversampling ADC. (a) Frequency domain for Nyquist rate ADC. (b) Aliasing effect for Nyquist rate ADC. (c) Frequency domain for oversampling ADC.

A sampled signal in the frequency domain appears as a series of band-limited signals at multiples of the sampling frequency. As the sampling frequency decreases, the frequency spectra begin to overlap causing aliasing effect. Figure 2-2a shows the frequency spectra, while Figure 2-2b shows the aliasing effect when using Nyquist rate converters. Complex filters are required to correct the problem. For oversampled ADC, aliasing becomes much less of a factor. Since the sampling rate is much greater than the bandwidth of the signal, the frequency domain representation shows that the spectra are

widely spaced, as seen in Figure 2-2c. Thus using oversampling ADC, little if any, anti_alias filtering is needed.

Oversampling converters typically employ SC circuit and therefore do not need sample-and-hold circuits. Quantization is provided in the form of a pulse-density modulated signal that represents the average of the input signal. The modulator is able to construct these pulses in real time, so it is not necessary to hold the input value and perform the conversion. Figure 2-3 illustrates the output of the modulator for the positive half of a sine wave input. For the peak of the sine wave, most of the pulses are high. As the sine wave decreases in value, the pulses become distributed between high and low according to the sine wave value.

Digital signal processing should be utilized for the oversampling ADC, which filter any out-of-band quantization noise and attenuate any spurious out-of-band signals. The output of the filter is then down sampled to the Nyquist rate so that the resulting output of the ADC is the digital data, which represents the average value of the analog voltage over the oversampling period. Figure 2-4 shows the block diagram and the frequency spectrum of the digital part.

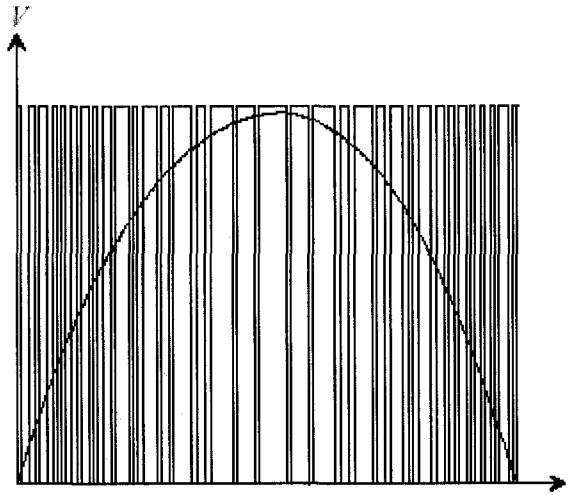


Figure 2-3. Pulse density output from a $\Sigma\Delta$ modulator for a sine wave input

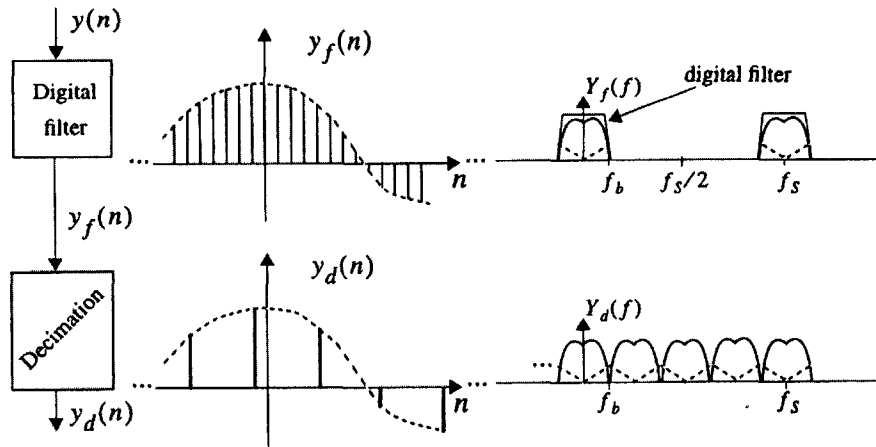


Figure 2-4. Digital and decimation filtering in the $\Sigma\Delta$ ADC

2.2 First Order $\Sigma\Delta$ Modulator

This section examines the time domain and the frequency domain behaviour to determine why $\Sigma\Delta$ Modulation is so beneficial for generating high-resolution data. Noise shaping, which is a powerful concept used within oversampling ADC, is explained.

2.2.1 Time Domain Behaviour

A basic first order $\Sigma\Delta$ modulator can be seen in Figure 2-5. An integrator and a 1-bit quantizer are in the forward path, and a 1-bit digital-to-analog (DAC) is in the feedback path of a single-feedback loop system. The 1-bit quantizer is simply a comparator that converts an analog signal into either a high or low. From the Z-domain representation shown in Figure 2-6, the input-output relation can be written in terms of a difference equation as [31]:

$$y(KT) = x(KT - T) + Q_e(KT) - Q_e(KT - T) \quad (2-1)$$

Where K is an integer. T is the inverse of the sampling frequency (f_s). Q_e is the quantization noise expressed as:

$$Q_e(KT) = y(KT) - u(KT)$$

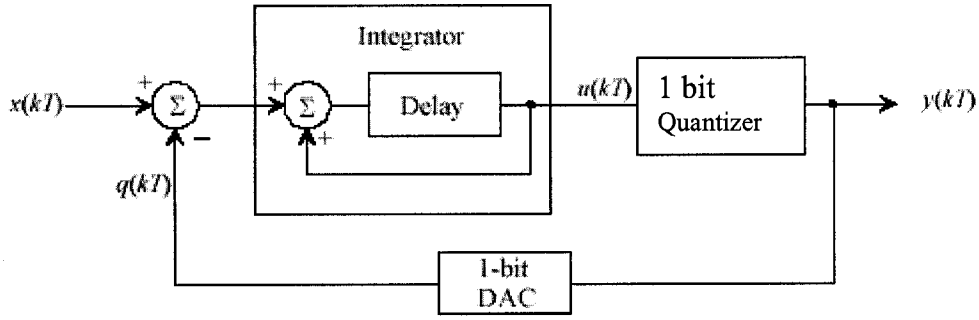


Figure 2-5. First-order $\Sigma\Delta$ modulator

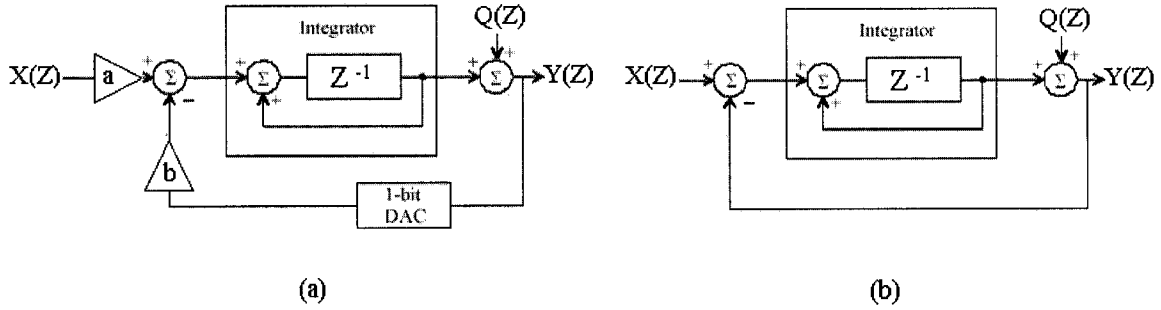


Figure 2-6. Z domain representation of the first-order $\Sigma\Delta$ modulator.

(a) Z-domain representation. (b) Conceptual representation.

Therefore, the output of the modulator consists of a quantized value of the input signal delayed by one sample period, plus a differencing of the quantization error between the present and previous values. Thus, the real power of the $\Sigma\Delta$ Modulator is that the quantization noise Q_e , cancels itself out to the first order.

2.2.2 Z-Domain Behaviour

Figure 2-6 shows the Z-domain model for the first order $\Sigma\Delta$ modulator. The ideal integrator is represented with the transfer function $\frac{Z^{-1}}{1 - Z^{-1}}$. The 1-bit quantizer is

modeled as a simple error source $Q(Z)$, and the DAC is considered to be ideal. The output can be expressed as:

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})Q(z) \quad (2-2)$$

Where $Y(z)$, $X(z)$ and $Q(z)$ are the z-transform of the modulator output, input, and the quantization error respectively.

The multiplication factor of $X(z)$ is called the signal transfer function (STF), whereas that of $Q(z)$ is called the noise transfer function (NTF). It can be noted that z^{-1} represents a unit delay, while the NTF has high pass characteristics, allowing noise suppression at low frequencies. The modulator has essentially pushed the power of the noise out of the bandwidth of the signal. This high-pass characteristic is known as noise shaping. The digital filter will then perform low pass filtering in order to remove all of the out-of-band quantization noise, which then permits the signal to be down sampled to yield the final high-resolution output

2.3 Second Order $\Sigma\Delta$ modulators

Second order $\Sigma\Delta$ modulator provides a greater amount of noise shaping. A second-order modulator is shown in Figure 2-7.

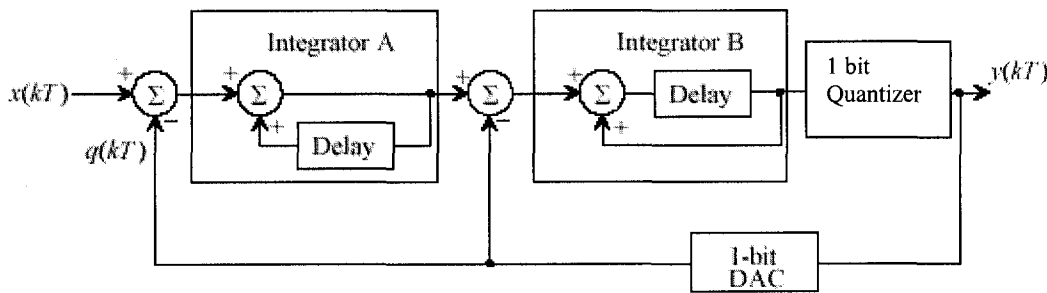


Figure 2-7. Second-order $\Sigma\Delta$ modulator

The output of the modulator can be expressed in the time domain as [31]:

$$y(KT) = x(KT - T) + Q_e(KT) - 2Q_e(KT - T) + Q_e(KT - 2T) \quad (2-3)$$

The output contained a delayed version of the input plus a second-order differencing of the quantization noise Q_e .

The z-domain equivalent is given by [32]:

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})^2 Q_e(z) \quad (2-4)$$

The NTF $(1 - z^{-1})^2$ has two zeros at dc, resulting in second-order noise shaping. In general L^{th} -order noise shaping can be obtained by placing L integrators in the forward path of a $\Delta\Sigma$ modulator. For L^{th} -order noise differencing, the noise transfer function (NTF) is given by:

$$NTF_Q(z) = (1 - z^{-1})^L \quad (2-5)$$

In the frequency domain, the magnitude of the noise transfer function can be written as:

$$|NTF_Q(f)| = |1 - e^{-j2\pi f T_s}|^L = (2 \sin \pi f T_s)^L \quad (2-6)$$

Figure 2-8 shows the noise shaping functions of the first, second, and third-order modulator. The crosshatched area under each of the curves represents the noise that remains in the signal bandwidth. As the order increases, more of the noise is pushed out into the higher frequencies, thus decreasing the noise in the signal bandwidth. Almost all of the noise is out of the signal bandwidth; it can be easily filtered, leaving only a small portion within the signal bandwidth. As the modulator order and/ or oversampling ratio increases, the portion of the quantization noise that falls into the signal band decreases.

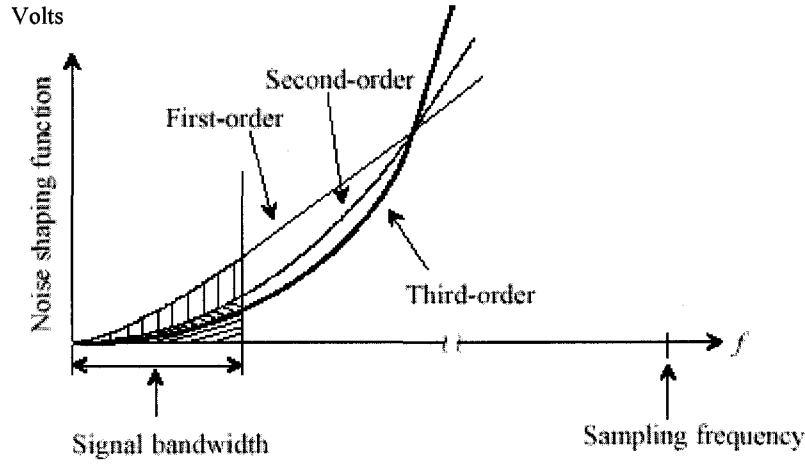


Figure 2-8. Comparison of noise shaping for the first, second and third-order $\Sigma\Delta$ modulator.

In practice, the single-loop modulator having noise-shaping characteristics in the form of $(1-Z^{-1})^L$ is unstable for $(L>2)$, unless an L-bit quantizer is used [33] [34]

2.4 Performance Criteria

The figures of merit used to characterize $\Delta\Sigma$ modulator are the signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), Dynamic range (DR), the effective resolution and the power dissipation.

2.4.1 Signal-to-noise ratio (SNR)

SNR is the ratio between the output power at the frequency of a sinusoidal input and the in-band noise power. Ideally with quantization noise only, the SNR results in:

$$SNR(dB) = 10 \log_{10} \left(\frac{A^2 / 2}{P_Q} \right) \quad (2-7)$$

Where A is the amplitude of the input signal and P_Q is the quantization noise power.

2.4.2 Signal-to-noise-and-distortion ratio (SNDR)

It is the ratio of the output signal power to the in-band noise power due to the non-idealities of the circuitry and the quantization noise. Then by definition, SNDR is given by:

$$SNDR(dB) = 10 \log_{10} \left(\frac{A^2 / 2}{P_Q + P_D} \right) \quad (2-8)$$

Where P_D is the harmonic distortion power due to the non-idealities.

Peak SNDR is a useful metric for evaluating the capability of a $\Sigma\Delta$ modulator for handling large in-band signals at acceptable linearity. It is especially important for applications such as digital audio applications. Peak SNDR is frequency dependant and can be used to measure the degradation of the modulator performance as the input signal increases in frequency. Since the output data is digital, discrete Fourier transform can be used to examine the data in the digital domain.

2.4.3 Dynamic range (DR)

The DR is defined as the ratio between the output power at the frequency of a sinusoidal input with full-scale range amplitude and the output power when the input is a sinusoidal of the same frequency, but of small amplitude, so that it cannot be distinguished from noise; that is, with SNR equals to 0 dB. DR is also called the useful signal range [35].

For a single-bit quantizer, DR is given by [32]:

$$DR^2 = \frac{3}{2} \frac{2L+1}{\pi^{2L}} M^{2L+1} \quad (2-10)$$

Where M is the OSR and L is the modulator order

2.4.4 Effective resolution

The number of bits (B) or effective resolution of the $\Sigma\Delta$ modulator as a function of its DR is [32]:

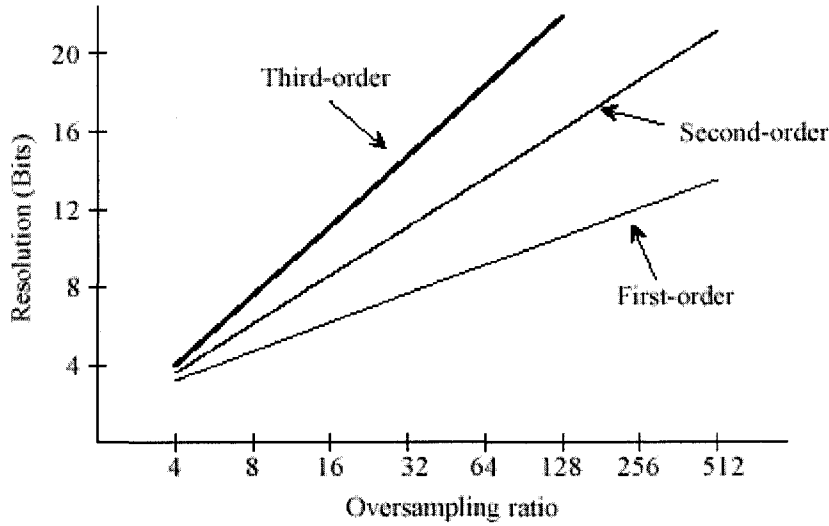


Figure 2-9. Oversampling ratio versus resolution for the first, second and third-order $\Sigma\Delta$ modulator.

$$B(\text{bit}) = \frac{DR(\text{dB}) - 1.76}{6.02} \quad (2-11)$$

Thus for 16 bit data conversion, one must design a circuit that will have DR of 98 dB. The resolution also increases as the order of the $\Sigma\Delta$ modulator and the oversampling ratio increases, as seen in Figure 2-9 [30]

It can be concluded from equation (2-10) and (2-11) that using a first-order modulator, DR increases by 9dB with every doubling of the oversampling ratio. This correlates to an approximate increase of 1.5 bits in resolution. The higher order modulators have even greater gain in resolution as 2.5 bit increase is attained with each doubling of the oversampling ratio using a second-order modulator, while the third-order modulator increases by 3.5 bits.

2.4.5 Power Dissipation

In low-voltage, low-power design, power dissipation is an important parameter. It is opposes a design constraint. Power dissipation is normally discussed as a trade off parameter with target metrics.

2.5 Top-Down Design Methodology Motivation

Despite a high tolerance for non-idealities of the $\Sigma\Delta$ Modulator, it is still governed by the limitations of its analog building blocks, especially at the input stage, where, no noise shaping has taken place. The design of an analog system consists of three obstacles:

1. Architecture selection.
2. Determining the specifications of the analog building blocks necessary to implement the chosen architecture.
3. Minimizing the effects of the circuit non-idealities.

If these obstacles are treated separately, the number of design iteration is big and consequently the design cycle will take too long to practically meet the market demands for the technology. Due to the uncertainty that arises with a change in technology, it is more amenable to consider a design process that can begin without a complete dependence on a specific technology. Some tools exist aimed at fully automating the design process, however they are limited to a small number of fixed schematic [36] [37]. These tools, which are not designed to be reproduced, remove the designer from the process, and do nothing to increase the designer's knowledge. Furthermore, the techniques used in these programs are hidden and cannot be applied to other designs.

2.6 Switched Op-Amp $\Sigma\Delta$ Modulator Design Methodology

To reduce the number of the design iteration and better explore the design options, it is beneficial to perform an analysis at the system architectural level before starting transistor level design. This allows for a feasibility analysis in which all the design considerations are treated at the highest level of abstraction. The ultimate goal is to have the low level circuit parameters dictated by the selected architecture and desired performance. High-level optimization geared design avoids the complete dependence on a specific technology and provide the designers with values for familiar parameters (such as g_m or r_{out} for an op-amp), which provide excellent guidelines for the construction of a device. A top-down design methodology is needed in conjunction with an optimization process for the creation of analog or mixed signal integrated circuits.

There is also a need to provide a mean of tackling the design problem by presenting a simple to implement methodology that makes use of widely used and available tools. This allows the procedure to be implemented and reused with little difficulty or expense [38]. SIMULINK is used to implement the system architecture and model non-idealities, while MATLAB [39] is used to create routines to optimize the circuit parameters. As a result, the requirements of the building blocks will be specified prior to the undertaking of transistor level simulation, saving valued design time. Top down design methodology is proposed to design $\Sigma\Delta$ modulator. The systematic design methodology that is followed in this work is shown in Figure 2-10.

Starting with the required specification, the topology required for hearing-aid application is investigated and the optimal architecture is chosen. The system behavior simulation is necessary to optimize the $\Delta\Sigma$ modulator topology parameters on the system level. SIMULINK is used for the behaviour simulation. The key parameters are isolated and the sub-circuits is modeled for non-idealities and the behaviour simulation is run again to derive the required circuit specification in order to ensure that the real system, with non-ideal components, reaches the intended performance. This methodology avoids estimation of the required circuit specifications; it is an important part of low power design. The building blocks are designed in 0.18 μm process at the circuit level such that they achieve the given specifications and hence ensure the overall system performance. All the sub-modules and sub-circuits are integrated and simulated. The simulation results are compared with the required specification. The system then enters the layout phase. Post-simulation is necessary to ensure that the parasitic effect is considered. Finally it is sent for fabrication.

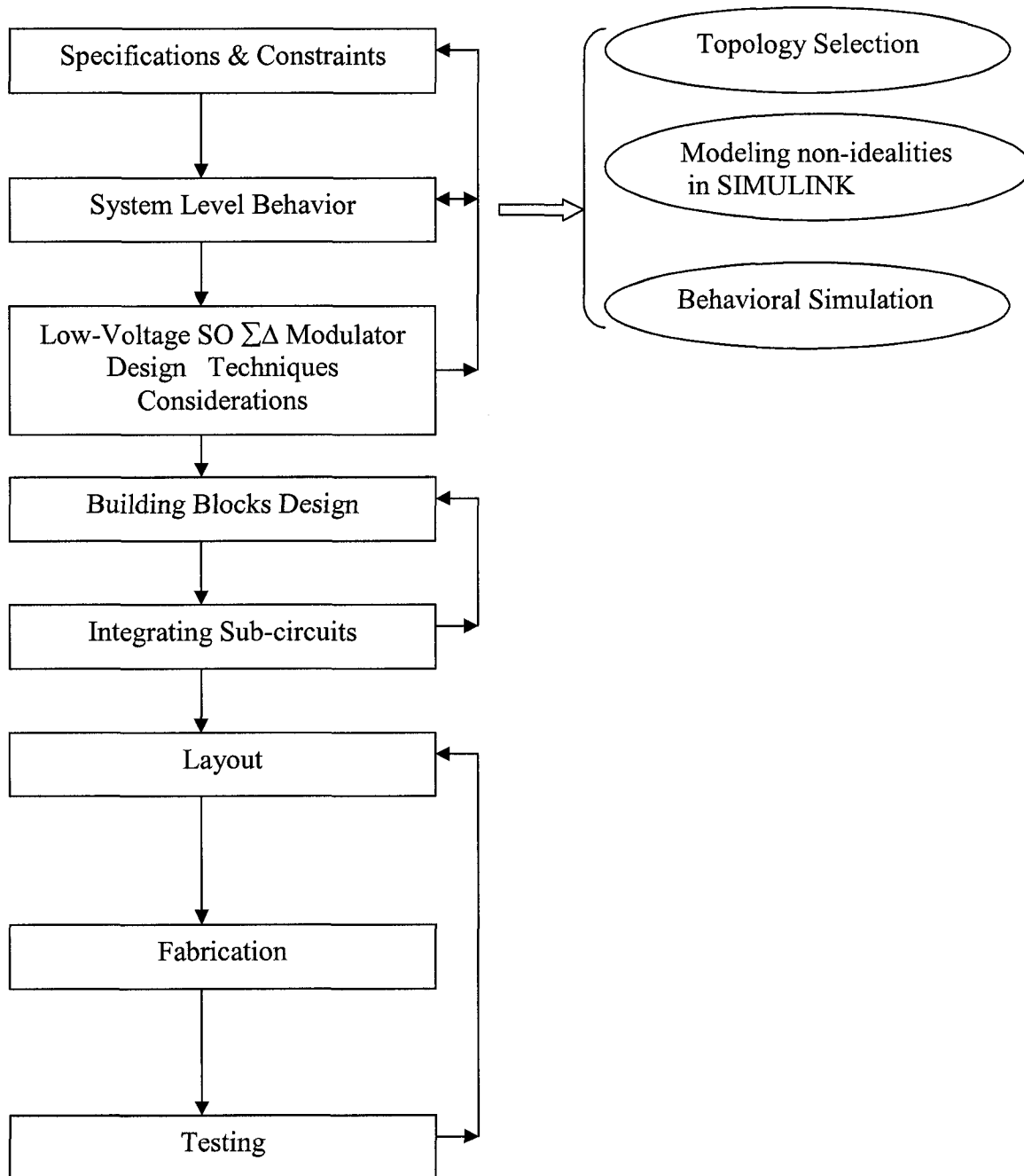


Figure 2-10. SO $\Sigma\Delta$ modulator design methodology

Chapter 3

System Level Behavior

A variety of $\Sigma\Delta$ modulator architectures have been explored recently. $\Sigma\Delta$ modulators can be classified in two primary groups, the single-loop and cascade. Each of which has its advantages and drawbacks. Among these, perhaps the most robust is a second-order $\Sigma\Delta$ modulator [34]. The second-order $\Sigma\Delta$ modulator is attractive for digital-audio signal acquisition for their stable operation and its tolerance to circuit non-idealities.

A complete set of SIMULINK models are needed to perform exhaustive behavioral simulation of the SC $\Sigma\Delta$ modulator taking into account most of the non-idealities, such as sampling jitter, KT/C noise and op-amp parameters (noise, finite gain, finite bandwidth (GBW), slew-rate (SR) and saturation voltages). The models, which simulate non-idealities, are utilized in the behavior simulation. The behavior model is presented and the results obtained with the modeled blocks for the second-order $\Sigma\Delta$ modulator are reported.

3.1 Comparison between Modulator Architectures

Different kinds of $\Sigma\Delta$ modulators exist. Depending on the number of quantizers, modulator can be classified as single-loop and cascade. They can also be classified as one-bit or multi-bit modulator according to the number of quantization levels employed by the quantizer. The advantage and disadvantage of these topologies are summarized in Table 3-1.

Table 3-1 Comparison between modulator architectures

Modulator Type	Advantages	Disadvantages
Low-order Single-loop Single-bit	<ul style="list-style-type: none">• Guaranteed stability• Simple loop filter design• Simple circuit design	<ul style="list-style-type: none">• High value of OSR for high SNR• More prone to noise pattern
High-order Single-loop Single-bit	<ul style="list-style-type: none">• High SNR for low OSR• Less prone to noise pattern• Simple circuit design	<ul style="list-style-type: none">• Difficult loop filter design• Stability is signal dependent• Maximum input range must be restricted to ensure stability
Multi-loop cascade	<ul style="list-style-type: none">• High SNR for low OSR• Stability guaranteed• Maximum useful input range	<ul style="list-style-type: none">• Requires near perfect matching between analog integrator and digital differentiator.• Complex SC circuits are required to ensure matching.
Multi-bit	<ul style="list-style-type: none">• High SNR for very low OSR• Stability is much easier to be achieved than for high-order loops.• Smaller noise pattern	<ul style="list-style-type: none">• More complex circuit design• Sensitive to DAC non-linearity

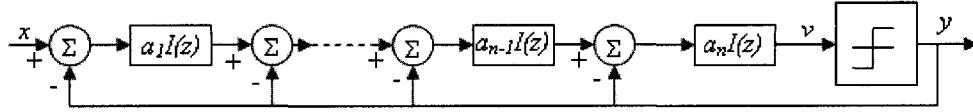


Figure 3-1. Classic n^{th} order single loop $\Sigma\Delta$ modulator topology.

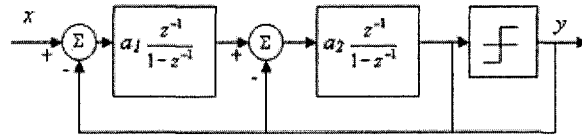


Figure 3-2. Second-order, single-loop $\Sigma\Delta$ modulator topology

3.2 Single Loop $\Sigma\Delta$ modulators using Half Delay Integrators

Single-loop $\Sigma\Delta$ modulators are extremely insensitive to circuit mismatches. Practically, second-order, third order, fourth-order, or even higher order $\Sigma\Delta$ modulators are used [40] [41]. Figure 3-1 shows the block diagram of an n^{th} order classic single bit modulator. The topology has been organized to have the minimum of independent parameters. It uses full delay integrators with a transfer function of:

$$I(z) = a \frac{z^{-1}}{(1 - z^{-1})} \quad (3-1)$$

Second-order $\Sigma\Delta$ modulator for audio applications was suggested by [40]. Figure 3-2 shows the second-order modulator topology. The output of this modulator in the frequency domain is given as follows:

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})^2 E(z) \quad (3-2)$$

In equation 3-2, the noise transfer function $(1 - z^{-1})^2$ works as a second-order shaping filter to the quantization noise

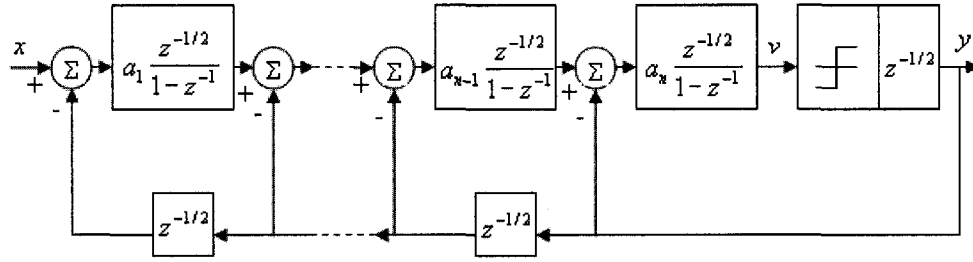


Figure 3-3. The n^{th} order single loop $\Sigma\Delta$ modulator topology using half delay integrators.

The basic SO integrator cell offers only and exactly a half delay to the signal, thus its transfer function is given by:

$$I_{\frac{1}{2}}(z) = a \frac{z^{-1/2}}{(1 - z^{-1})} \quad (3-3)$$

The half-delay integrator must be followed by an analog half-delay block to function as a full-delay integrator [42] [43]. This can be implemented by a SC amplifier with unity gain, deploying the SO technique. However, this requires an extra op-amp, and hence causes an increased power and area allocation. For the purpose of a $\Sigma\Delta$ modulator, these additional amplifiers can be avoided by making use of a rearrangement topology. In the architecture of Figure 3-3, the half-delay element has been shifted to the feedback path [44]. There they are in the digital domain. They can be implemented with a half-delay latch and their power consumption is now negligible as compared to the analog implementation. Furthermore, the properties of the modulator are identical to the full-delay implementation. The loop coefficients that optimize the SNR have not changed.

The power spectral density of the shaped quantization noise of an n^{th} -order oversampling $\Sigma\Delta$ modulators is calculated as [45]

$$S_Q(f) = S_E(f) \left| 1 - e^{-j2\pi \frac{f}{f_s}} \right|^{2n} = \frac{\Delta^2}{12 f_s} \cdot 2^{2n} \sin^{2n} \left(\pi \frac{f}{f_s} \right) \quad (3-4)$$

Where Δ is the separation between two consecutive levels

The in-band noise power is calculated by integrating the power spectral density of the quantization error expressed in equation 3-4, in the signal band $(-f_b, f_b)$:

$$N_Q = \int_{-f_b}^{f_b} S_Q(f) df = \frac{\Delta^2}{12} \cdot \frac{\pi^{2n}}{(2n+1) \cdot OSR^{(2n+1)}} \quad (3-5)$$

Where OSR is the oversampling ratio, expressed as:

$$OSR = 2f_b/f_s$$

Then the DR is calculated as:

$$DR = 10 \log \left[\frac{(\Delta/2)^2}{2N_Q} \right] = 10 \log \frac{(6n+3)OSR^{(2n+1)}}{2\pi^{2n}} \quad (3-6)$$

Equation 3-6 shows that the DR is a strong function of the OSR and the order (n) of the $\Sigma\Delta$ modulator. For each doubling of the OSR, an extra $(2n+1)/2$ bits can be obtained. Thus the designers can tradeoff between OSR and n to meet the required DR. On the other hand, the main constraints for single-loop modulators of an order greater than 2 is the stability problem. Increasing the loop parameters worsens the stability of the loop [46] as they become conditionally stable. Stabilizing a high-order modulator requires the use of deliberately chosen parameters and more complicated transfer functions than just a cascade of integrators and possibly the use of reset circuits in the integrators in case instability happens. All of these tend to reduce the DR well below the upper bound given by equation 3-6 for a single-loop modulator with orders higher than two.

The second-order modulator is widely used because it is simple to implement and insensitive to component mismatch. The NTF “ $(1-z^{-1})^2$ ” filters out the quantization noise out to the second-order. From equation 3-4, the power spectral density of the shaped quantization noise is deduced as:

$$S_Q(f) = S_E(f) \left| 1 - e^{-j2\pi \frac{f}{f_s}} \right|^4 = \frac{\Delta^2}{12f_s} \cdot 16 \sin^4 \left(\pi \frac{f}{f_s} \right) \quad (3-7)$$

From equation 3-5, the in band power of the second-order modulator is calculated as:

$$N_Q = \int_{-f_b}^{f_b} S_Q(f) df = \frac{\Delta^2}{12} \cdot \frac{\pi^4}{5 \cdot OSR^5} \quad (3-8)$$

Equation. 3-8 shows that doubling the OSR leads to decrease of 15dB/octave of the in-band noise power.

The DR can be calculated from equation.3-6 as:

$$DR = 10 \log \left[\frac{15 \cdot OSR^5}{2\pi^4} \right] = 50 \log OSR - 11.1354 \quad (3-9)$$

3.3 Cascade $\Sigma\Delta$ Modulator using Half Delay Integrators

To avoid the instability problem of higher order single-loop modulator, cascade architecture could be an alternative. Figure 3-4 shows a block diagram of a cascaded $\Sigma\Delta$ modulator. It uses combinations of inherently stable first and second-order $\Sigma\Delta$ modulators to achieve higher-order noise shaping. Outputs from all stages pass through a digital error cancellation logic to cancel the quantization errors except for that of the last stage.

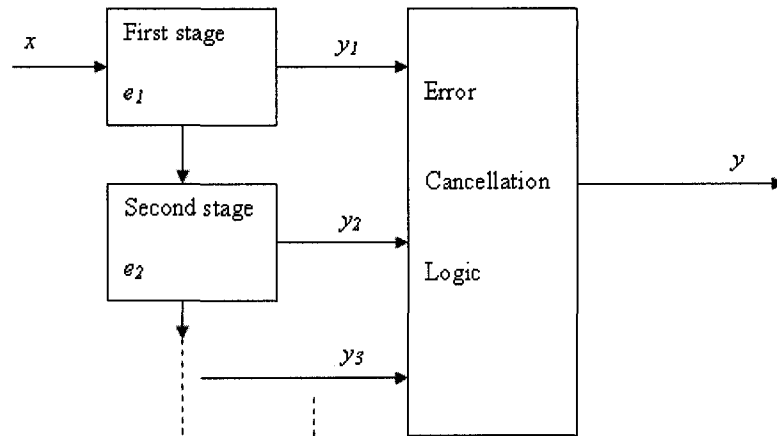


Figure 3-4. Block diagram of a cascaded $\Sigma\Delta$ modulator

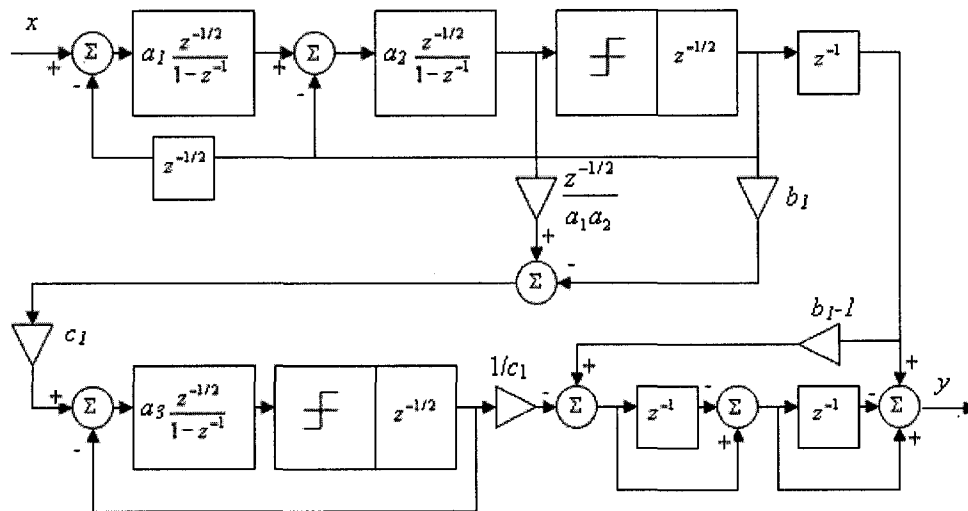


Figure 3-5. Cascaded 2-1 $\Sigma\Delta$ modulator with half delay integrators

It is also possible to implement cascade topologies using half-delay. Figure 3-5 shows a cascade 2-1 topology with half delay integrators. Linear analysis of these structures allows expressing the output signal as a combination of the input signal and the quantization noise of the last stage [43].

$$Y(z) = z^{-\frac{5}{2}} X(z) + \frac{1}{c_1} (1 - z^{-1})^3 E_2(z) \quad (3-10)$$

We can see that the output of this cascaded modulator is a third-order noise shaping. The in-band noise power is calculated by using a method similar to equation 3-5.

$$N_Q = \int_{-f_b}^{f_b} S_Q(f) df = \frac{\Delta^2}{12} \cdot \frac{\pi^6}{7 \cdot c_1^2 \cdot OSR^7} \quad (3-11)$$

Accordingly, the DR for the 2-1 cascade structure is calculated to be:

$$DR(dB) = 10 \log \left[\frac{(\Delta/2)^2}{2P_Q} \right] = 10 \log \left(\frac{21 \cdot c_1 \cdot OSR^7}{2\pi^6} \right) \quad (3-12)$$

Equation 3-12 shows that the DR increases by 21dB for every doubling of the OSR. It is clear that the scaling coefficient c_1 tend to reduce the DR.

Similarly, a stable higher-order multi-stage $\Sigma\Delta$ modulator can be obtained. In [47] a 2-1-1 fourth-order cascaded $\Sigma\Delta$ modulator can be realized with an OSR of 24 with 15 bits resolution. It can be concluded that the noise shaping of a cascaded architecture is comparable to, or even better than that of a single-stage modulator whose order is the sum of all the orders in the cascade.

3.4 Multibit Topology

The cascade architecture can be combined with multibit DAC converters to improve DR further. For example, a 2-1 cascade with a 3-bit DAC converter in the second stage achieves 12-bit resolution with an OSR of 24 and 2.1 MS/s Nyquist rate [48]. However, multibit DAC converter is constrained by linearity problem so calibration techniques are often needed to make the modulator designed works well. The common way to ease the linearity requirements is only using multibit DAC converter at the last stage rather than at the overall modulator input as shown in [48].

3.5 Topology Selection

For audio applications, both single-loop and cascade structures are published [27] [41] [49] [50] [51]. In comparing the single loop topologies with cascaded topologies, generally the former are always much worse than the later in term of PSNR. Therefore, if the main goal is high resolution, the cascaded topology offers a much better solution than single loop topologies. This, however, comes at the cost of much higher sensitivity to non-idealities of the building blocks [52]. Although cascade topology offers higher SNR and maximizes the input range, the SO technique do not make use of the maximum input range. This is because SO technique, only eliminate the need for rail-to-rail switching operation at the output of the integrator, however, the input switch for the input signal path remains, and it could be implemented as a single switch with limited signal range as will be explained in details in Chapter 5.

Single-loop architecture, as compared to cascade, is relatively insensitive to component mismatches. As an example, a fourth-order interpolative topology can tolerate up to 5% mismatch in its coefficients [53]. In contrast, a 2-2-cascade modulator requires about 1% between the analog and digital inter-stage gains to achieve 14-bit performance. For a second-order modulator, variation of $\pm 20\%$ in the gain of the first integrator has only a minor impact on the modulator's performance. This gain tolerance translates into tolerance for incomplete settling of the integrator outputs as long as the settling process is linear [40].

If the second-order modulator is used to implement a $\Sigma\Delta$ modulator of 16 bit resolution, the OSR needs to be 256 for the hearing aids application with a signal bandwidth of 16 KHz, the sampling rate (f_s) needed is 8.2 MHz. This frequency can be realized with 0.18 μm CMOS technology that is used to implement this work. Drawback for using such frequency is the need for higher SR and clock jitter requirements. With the help of the behavior simulation that consider non-idealities, SR can be estimated and a decision can be made if the figure is practical. Dynamic power dissipation doubles for every doubling of the sampling frequency, however if SO $\Sigma\Delta$ modulator is used, the duty cycle is 50% as will be explained in Chapter 7.

This design is exploring the possibly of using SO technique to implement a SO $\Sigma\Delta$ modulators using the latest IC technology with specified resolution and power

consumption requirement for a 16 bit hearing aid application with a bandwidth of 16 KHz. It was suggested in [40] that an ideal second-order $\Sigma\Delta$ modulator combined with oversampling ratio of 256 can be employed to realize a 16 dB resolution A/D converter. This discussion suggests that second-order single-loop architecture is favorable for this design, due to the inherent stability, simplicity and compatibility with SO technique for reduced power consumption and the constraint of the reduced input signal range.

Table 3-2 Non-idealities of the fundamental basic blocks

Basic Block		Non-ideality	Consequences
Clock		Jitter	Jitter noise
SC Integrator	Switches	Thermal noise	
	Op-Amp	Thermal noise	
		DC gain	Increases in quantization noise and harmonic distortion.
		BW and SR	Incomplete settling noise and harmonic distortion
		Saturation	Overloading and harmonic distortion
	Capacitors	Mismatching	Increase in quantization noise and harmonic distortion
Comparator		Hysteresis, Offset	Quantization noise increase

3.6 $\Sigma\Delta$ Modulators Non-Idealities

Table 3-2 compiles the fundamental basic blocks and the non-idealities considered.

3.7 Clock Jitter Model

The effect of clock jitter, on a SC $\Sigma\Delta$ modulator can be calculated based on the complete charge transfers during each of the clock phases. Once the analog signal has been sampled, the circuit is a sampled data system where variations of the clock period have no direct effect on the circuit performance. Therefore, the effect of clock jitter on the SC circuit is completely described by computing its effect on the sampling of the input signal. This means also that the effect of clock jitter on a $\Sigma\Delta$ modulator is independent of the structure or order of the modulator.

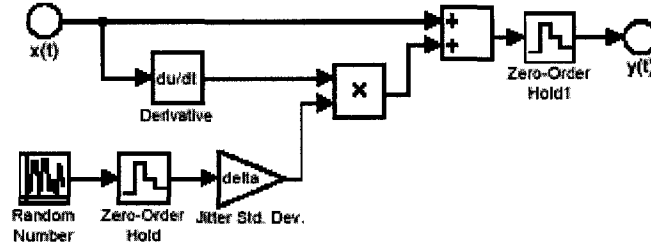


Figure 3-6. Modeling a random sampling jitter

Clock jitter results in a non-uniform sampling and increases the total error power in the quantizer output. The magnitude of this error is a function of both the statistical properties of the jitter and the input signal to the converter. The error introduced when a sinusoidal signal with amplitude A and frequency f_{in} is sampled at an instant, which is in error, by an amount δ is given by:

$$x(t + \delta) - x(t) \approx 2\pi f_{in} \delta A \cos(2\pi f_{in} t) = \delta \frac{d}{dt} x(t) \quad (3-13)$$

This effect can be simulated with SIMULINK by using the model shown in Figure 3-6, which implements equation 3-13. Here, it is assumed that the sampling uncertainty δ is gaussian random process with “delta” standard deviation. Whether oversampling is helpful in reducing the error introduced by the jitter depends on the nature of the jitter. The jitter is assumed to be white, so the resultant error has uniform power spectral from 0 to $f_s/2$, with a total power of $(2\pi f_{in} \delta A)^2 / 2$. In this case, the total error power will be reduced by the oversampling ratio [54].

3.8 Integrator Noise Model

While the performance of the theoretical $\Sigma\Delta$ modulator is only determined by the in-band quantization noise suppression, the physical implementation of the system with solid-state devices has to deal with other noise sources as well. The main additional noise sources of a silicon implementation are thermal noise and flicker ($1/f$) noise.

The circuit noise to be dealt with in a $\Sigma\Delta$ modulator is the noise injected into the input summing node of the first integrator, since it is added directly to the input signal and appears in the output spectrum without any filtering. White noises from the rest of the integrators are attenuated by different powers of the oversampling ratio, depending on the position of the integrator, and can be neglected.

The circuit thermal noise generated in an integrator has two main origins, the white noise due to the resistance of the MOS switches and the op-amp noise of the input stage. These noise sources originate a broadband and sampled noise component at the output of the integrator. These effects can be successfully simulated with SIMULINK using the model of a “noisy” integrator shown in Figure 3-7, where the coefficient b represents the integrator gain, which, referring to the schematic of a single-ended SC integrator shown in Figure 3-8, is equal to C_s/C_f . Each noise source and its relevant model will be described in the following sub-sections.

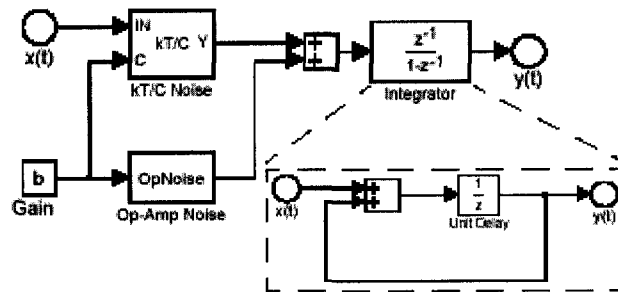


Figure 3-7. Noisy integrator model

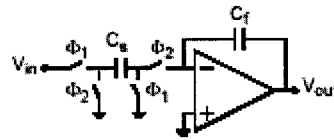


Figure 3-8. Single-ended SC integrator

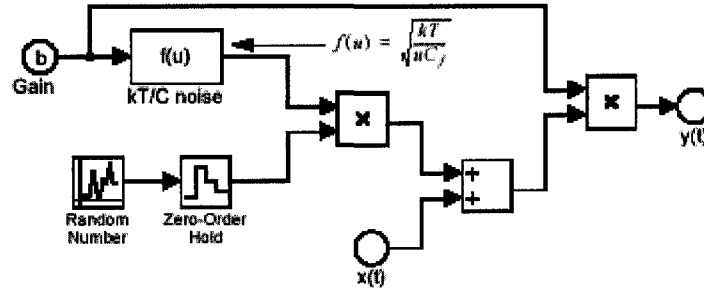


Figure 3-9. Modeling thermal noise (KT/C block)

3.8.1 Switch Thermal Noise (KT/C) Model

A critical source of noise in the system is the KT/C noise injected into the first stage integrator of the modulator. As a result, the input capacitor must be large enough to counter the additive noise effect that results. Therefore the first key parameter is the input sampling capacitor of the first integrator (C_s).

Thermal noise is caused by the random fluctuations of carriers due to thermal energy and presents even at equilibrium. Thermal noise has a white spectrum and wide band limited only by the time constant of the SCs or the bandwidths of the op-amps. Therefore, it must be taken into account for both the switches and the op-amps in the SC circuits. For instant, the sampling capacitor C_s in the single-ended SC integrator shown in Figure 3-8, is in series with a switch, with finite resistance R_{on} that periodically opens, sampling a noisy voltage onto the capacitor. The switch thermal noise voltage e_T (usually called KT/C noise) can be found by evaluating the integral [27]:

$$e_T^2 = \int_0^{\infty} \frac{4KTR_{on}}{1 + (2\pi f R_{on} C_s)^2} df = \frac{kT}{C_s} \quad (3-14)$$

Where K is the Boltzman constant and T is the absolute temperature

The switch thermal noise voltage e_T is superimposed to the input voltage $x(t)$ leading to:

$$y(t) = [x(t) + e_t(t)]b = \left[x(t) + \sqrt{\frac{kT}{bC_f}} n(t) \right] b \quad (3-15)$$

Where $n(t)$ denotes a gaussian random process with unity standard deviation and b is the integrator gain expressed as:

$$b = C_s/C_f$$

Equation (3-15) is implemented by the model shown Figure 3-9

Since the noise is aliased in the band from 0 to $f_s/2$, its final spectrum is white with a spectral density:

$$S(f) = \frac{2kT}{f_s C_s} \quad (3-16)$$

The first integrator will have two switched input capacitor, one carrying the signal and the other providing the feedback from the modulator output, each of them contributing to the total noise power.

3.8.2 Op-Amp Noise Model

Figure 3-10 shows the model used to simulate the effect of the op-amp noise. Here V_n represents the total RMS noise voltage referred to the op-amp input. Flicker ($1/f$) noise, wide-band thermal noise and dc offset, contribute to this value. The total op-amp noise power V_n^2 can be evaluated, through circuit simulation, on the circuit of Figure 3-8 during Φ_2 , by adding the noise contribution of all the devices referred to the op-amp input and integrating the resulting value over the whole frequency spectrum.

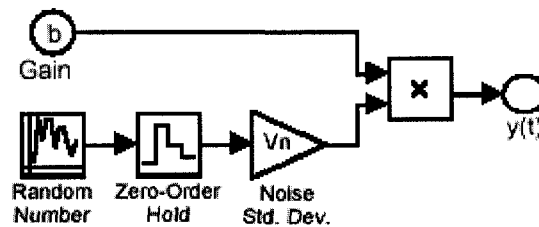


Figure 3-10. Op-amp noise model

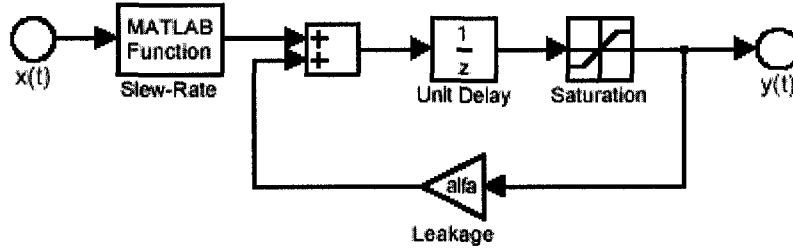


Figure 3-11. Real integrator model

3.9 Integrator Non-Idealities Model

The op-amp is the most critical component of the modulator, as its non-idealities causes an incomplete transfer of charge, leading to non-linearities. Key parameters that govern its behaviour are the noise, finite gain, finite bandwidth, SR, and saturation voltages. The SIMULINK model of an ideal integrator with unity gain is shown in the inset of Figure 3-2. Its transfer function is expressed as:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (3-17)$$

Analog circuit implementation of the integrator deviate from this ideal behaviour due to several non-ideal effects. One of the major causes of performance degradation in SC $\Sigma\Delta$ modulators, indeed, is due to incomplete transfer of charge in the SC integrators. This non-ideal effect is a consequence of the op-amp non-idealities, namely finite gain and bandwidth, SR and saturation voltages. These will be considered separately in the following subsections. Figure 3-11 shows the model of the real integrator including all the non-idealities.

3.9.1 DC Gain

The dc gain of the integrator described by equation 3-17 is infinite. In practice, however, the gain is limited by circuit constraints. The consequence of this integrator

leakage is that only a fraction of the previous output of the integrator (α) is added to each new input sample. The transfer function of the integrator with leakage becomes:

$$H(z) = \frac{z^{-1}}{1 - \alpha z^{-1}} \quad (3-18)$$

Therefore the dc gain H_0 becomes:

$$H_0 = H(0) = \frac{1}{1 - \alpha} \quad (3-19)$$

The limited gain at low frequencies increases the in-band noise.

3.9.2 Bandwidth and Slew Rate

The finite bandwidth and the SR of the op-amp are modeled in Figure 3.11 with a building block placed in front of the integrator, which implements a MATLAB function. The effect of the finite bandwidth and SR are related to each other and may be interpreted as a non-linear gain [55]. With reference to the SC integrator shown in Fig (3.8), the evolution of the output node during the n th integration period (when Φ_2 is on) is:

$$v_o(t) = v_o(nT - T) + \alpha V_s \left(1 - e^{-\frac{t}{\tau}} \right), \quad nT - \frac{T}{2} < t < nT \quad (3-20)$$

Where α is the integrator leakage, τ is the time constant of the integrator expressed as:

$$\tau = 1 / (2\pi \text{ GBW})$$

V_s is defined as:

$$V_s = V_{in}(nT - T/2)$$

The slope of this curve reaches its maximum value when $t = 0$, resulting in:

$$\left. \frac{d}{dt} v_o(t) \right|_{\max} = \alpha \frac{V_s}{\tau} \quad (3-21)$$

Two separate cases will be considered:

1. The value specified by equation 3-21 is lower than the op-amp SR. In this case there is no SR limitation and the evolution of v_o fits equation 3-20.
2. The value specified by equation 3-21 is larger than SR. In this case, the op-amp is in slewing and, therefore, the first part of the temporal evolution of v_o (for $t < t_0$) is linear with the slope SR. The following equations hold (assuming $t_0 < T$):

$$v_o(t) = v_o(nT - T) + SRt; \quad t \leq t_0 \quad (3-22)$$

$$v_o(t) = v_o(t_0) + (\alpha V_s - SRt_0) \left(1 - e^{-\frac{t-t_0}{\tau}} \right); \quad t > t_0 \quad (3-23)$$

Imposing the condition for the continuity of the derivatives of equation 3-22 and 3-23 in t_0 , we get:

$$t_0 = \frac{\alpha V_s}{SR} - \tau \quad (3-24)$$

If $t_0 \geq T$ only Equation.3-22 holds.

The MATLAB function in Figure 3-11 implements the above equations to calculate the value reached by $v_o(t)$ at time T , which will be different from V_s due to the gain, bandwidth and SR limitations of the op-amp. The SR and bandwidth limitations produce harmonic distortion reducing the total SNDR of the $\Sigma\Delta$ modulator. Appendix A.1 shows the MATLAB function.

3.9.3 Saturation

The dynamic of signals in a $\Sigma\Delta$ modulator is a major concern. It is therefore important to take into account the saturation levels of the op-amp used. It can simply be done in SIMULINK using the saturation block inside the feedback loop of the integrator, as shown in Figure 3-11

3.10 Capacitor Mismatching

One of the main advantages of SC circuits is that high precision can be obtained as the integrator coefficients are realized with capacitor ratios. However, fabrication process still results in capacitor mismatching and causes error to the values of these coefficients [56]. Consequently the quantization noise increases. In [53], it is shown that single-loop $\Sigma\Delta$ modulator can tolerate this type of error to as large as 5%. This is one of the advantages for selecting single-loop, second-order topology, rather than the cascaded topology.

3.11 Comparator

The principle design parameter of a comparator include speed, input offset, input-referred noise, and hysteresis. Owing to its position in a $\Sigma\Delta$ modulator, the offset and input-referred noise are subjected to noise shaping by feedback loop so can be neglected. For digital-audio design, speed is also not a problem. The sensitivity of an A/D converter performance to comparator hysteresis can be modeled quite well by an additively white noise. This noise also undergoes the same spectral noise shaping as the quantization noise. Thus the design requirement for the comparator is usually quite relaxed.

3.12 Behavioral Simulation for the Ideal $\Sigma\Delta$ modulator

Behavioral simulation can be accomplished using SIMULINK tool, as it provides a GUI tool so the designer can easily build block diagram, perform simulation, and view the simulation results at each point. The necessary functions and programs can be written in MATLAB to measure the performance of the modulator. Figure 3-12 shows the block diagram of a second-order $\Sigma\Delta$ modulator that is built in SIMULINK for behavioral simulation. All of the blocks are predefined in SIMULINK and are ideal. These

fundamental blocks are the ideal integrator, single-bit quantizer, adders and multipliers. Through adequate connections of these few blocks, a full $\Sigma\Delta$ modulator can be obtained. Scopes are used to monitor all of the critical points. Figure 3-13 shows the input sinusoidal, the outputs of the integrators and the modulator output superimposed on the input and the second integrator output. Figure 3-14 shows the normalized power spectral density at the output with 0.23 V input sinusoidal signal. By setting the different integrator coefficients and performing simulation, it is possible for the designer to choose the integrator coefficients that maximize the integrator output swing. However, owing to the use of ideal building blocks for the modulator, the simulation results cannot be very accurate and need to be fine-tuned by further behavioral simulation by using the blocks that model non-idealities in Chapter 5.

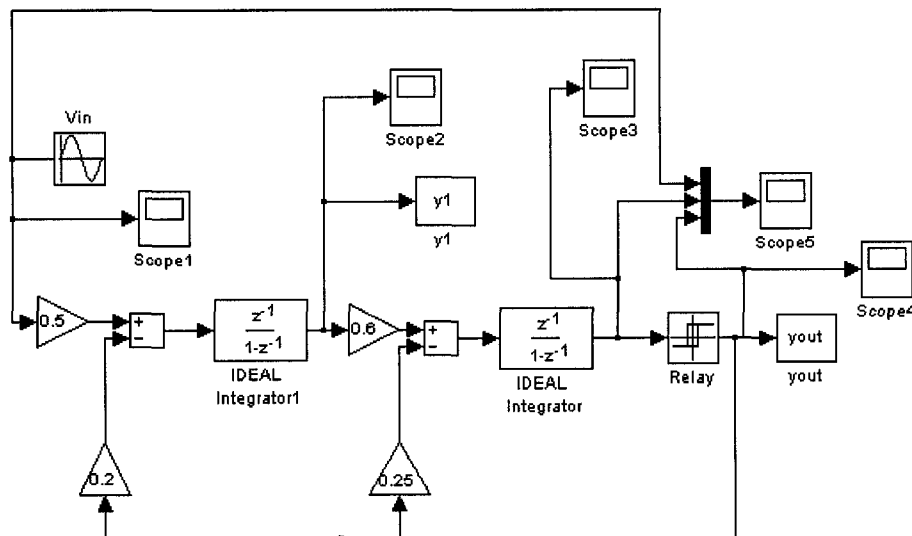


Figure 3-12. SIMULINK model for an ideal second-order $\Sigma\Delta$ modulator

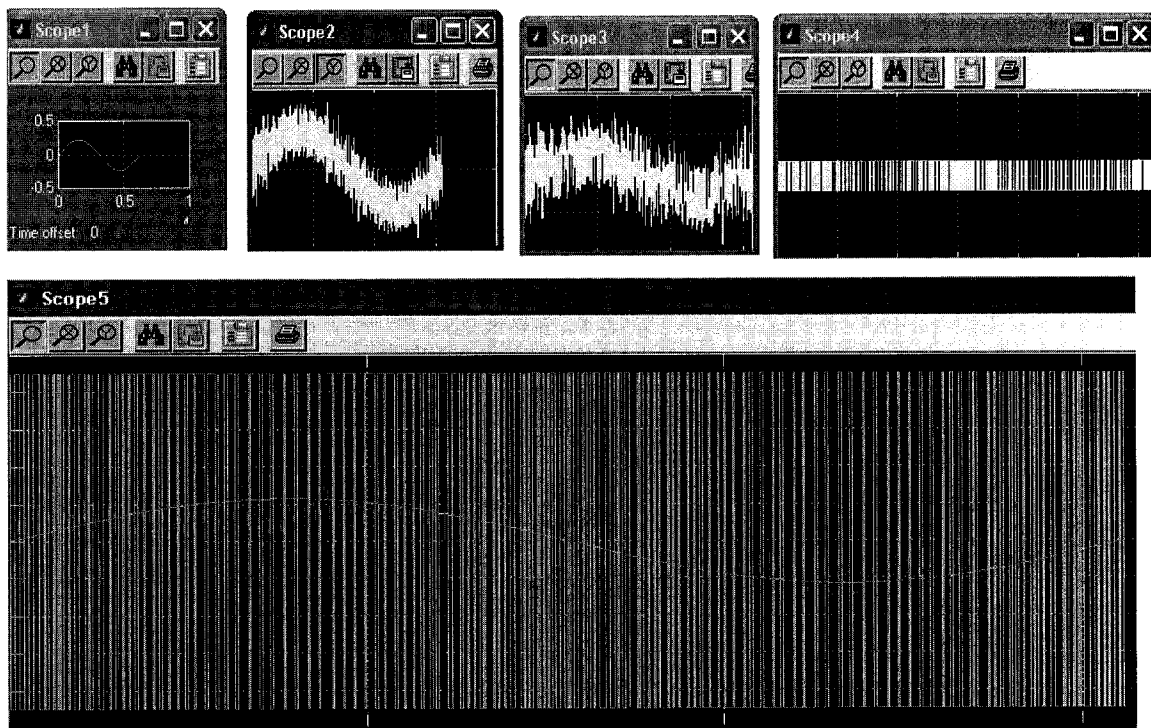


Fig. 3-13 SIMULINK simulation scope's results for the input, first and second integrator and the modulator output

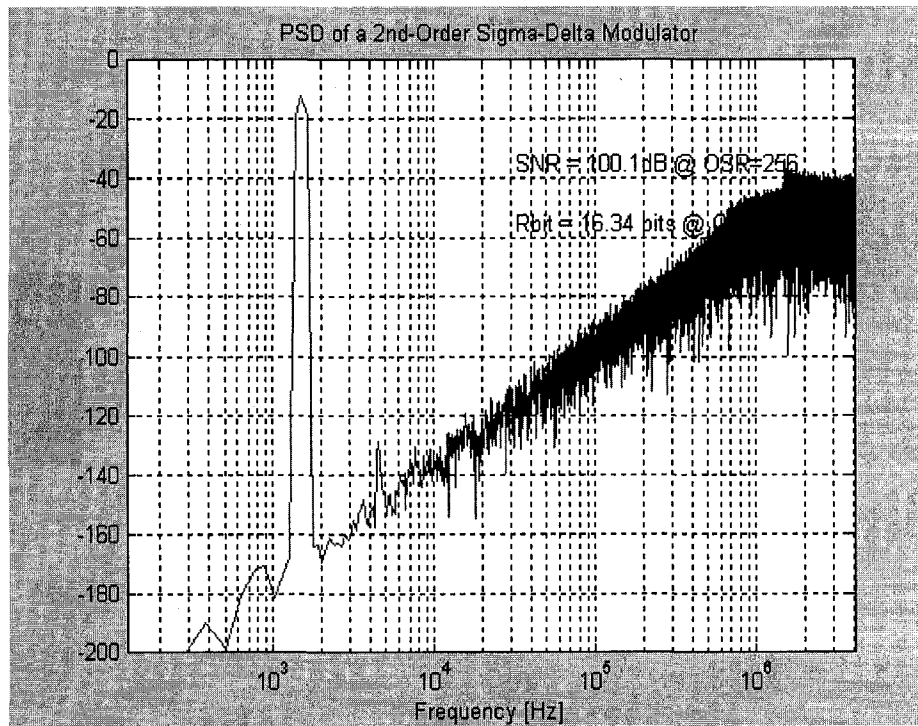


Figure 3-14. Simulated output spectra with -2 dB input sinusoidal for the ideal second-order modulator

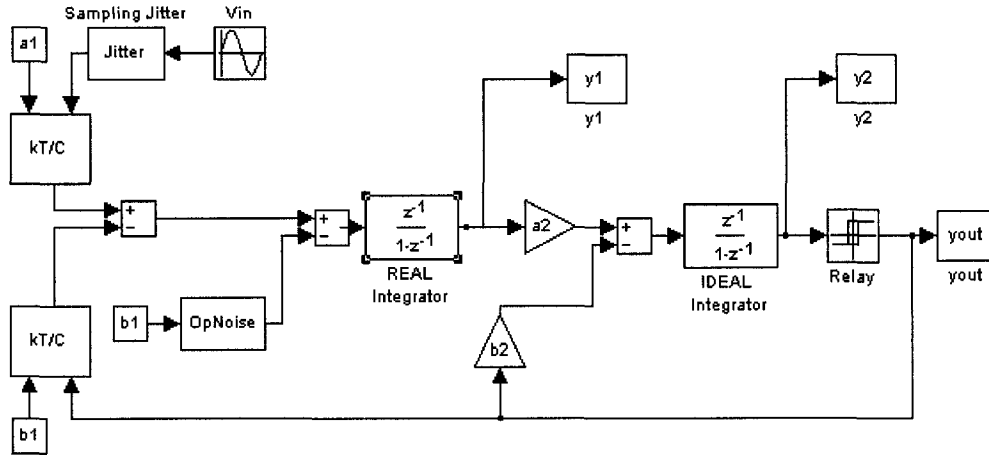


Figure 3-15. SIMULINK model for the non-ideal second-order $\Sigma\Delta$ modulator

3.13 Behavioural Simulation for the Non-Ideal $\Sigma\Delta$ modulator

The behavior of $\Sigma\Delta$ modulator can be affected by errors. The integrator is a fundamental block within a $\Sigma\Delta$ modulator. Its non-idealities, however, largely affects the operation of the modulator. The non-ideality for the first integrator only is considered, since their effects are not attenuated by the noise shaping. A single-bit quantizer is implemented with a comparator, which is a perfectly linear block and does not introduce any non-linearity error. Though linear block, comparators are subject to non-idealities such as input offset, comparator hysteresis, etc. However, due to its position in the $\Sigma\Delta$ modulators, the impact of the comparator non-idealities in the operation of $\Sigma\Delta$ modulators is much smaller than of integrators as these errors are subject to the same treatment as quantization noise.

Figure 3-15 shows the blocks used to simulate the behavior of the second-order SC $\Sigma\Delta$ modulator with a non-ideal first integrator [57]. To validate the models of the various non-idealities affecting the operation of the SC $\Sigma\Delta$ modulator, several simulations are performed with SIMULINK on the second-order modulator of Figure 3-15

Analysis such as power spectral density (PSD) analysis and SNR analysis are performed on the output. All the functions and programs in MATLAB are listed in Appendix B. From these analyses, it is possible for the designer to optimize the

integrator coefficients and building block parameters so as to design a $\Sigma\Delta$ modulator with the best possible performance.

For this design, after intensive simulation with SIMULINK and running the necessary programs, the SNDR curve that is believed to be the best outcome is shown in Figure 3-15. Within which, a 96 dB peak SNDR and 98 dB DR are achieved. The simulated PSD is shown in Figure 3-17 with -2 dB input sin signal. Fig 3.17 shows that the noise floor is well under -100 dB for an input signal as big as -2 dB and the modulator is thermal noise dominated. The corresponding modulator coefficients and building blocks parameters that result in the above performance are listed in Table 3-3 and 3-4.

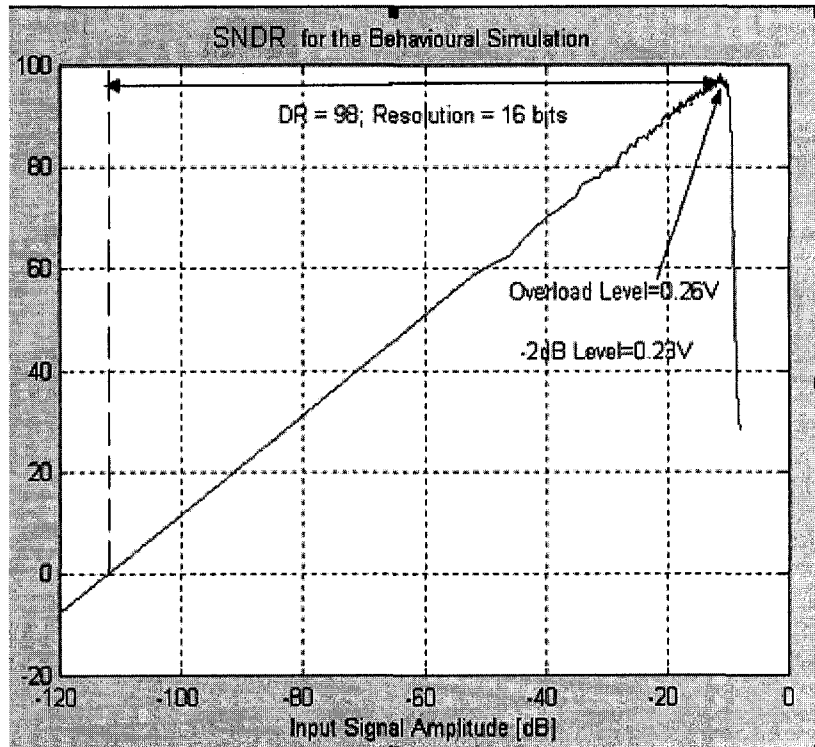


Figure 3-16. SNDR versus input amplitude

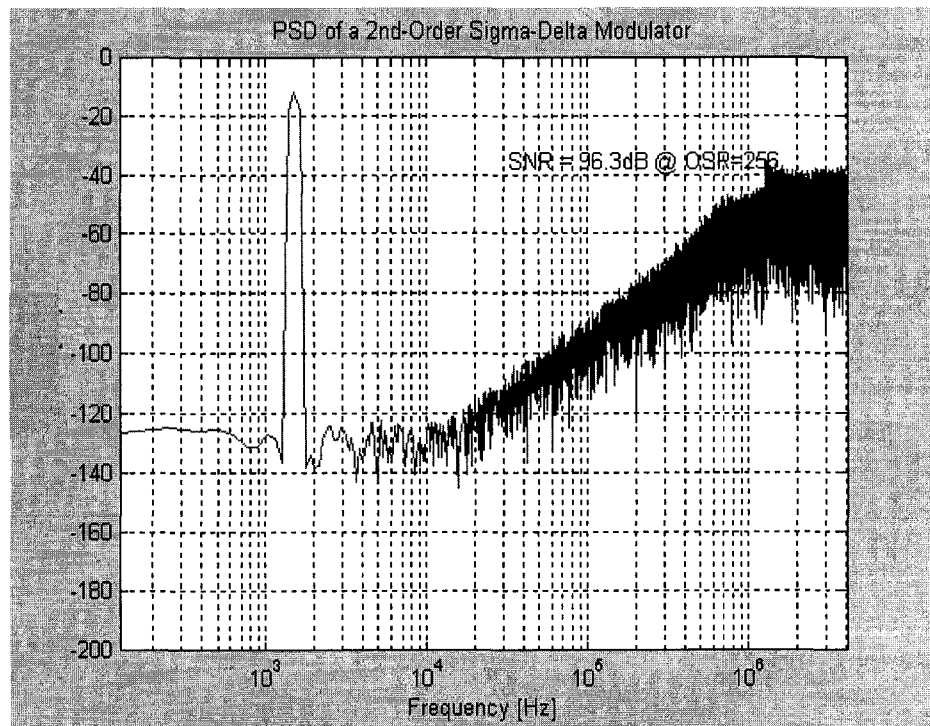


Figure 3-17. Simulated output spectra with -2 dB input sinusoidal for the non-ideal second-order $\Sigma\Delta$ modulator

Table 3-3 Second-order modulator coefficients and parameters

Parameter	Value
BW	16 KHz
Sampling frequency	8.192 MHz
OSR	256
DR	16 bit
Number of samples	65536
Gain of the first and second integrator	$a_1 = 0.5$; $a_2 = 0.6$
Feedback gain for the first and second integrator	$b_1 = 0.2$; $b_2 = 0.26$
Supply voltage	1.8 V
Coefficient mismatch	<10%

Table 3-4 Building block requirements

Block	Parameter	Value
Op-Amp	Gain	>55 dB
	GBW	>40 MHz
	SR	>16V/us
	Output swing	0.1-1.7V
Comparator	Output swing	0-1.8V

Chapter 4

Low- Voltage Low-Power Design Considerations

When an analog integrated circuit is needed at low supply voltage levels, the SC technique is the only technique in CMOS that can be used in practice to achieve good quality circuit. Probably the most robust way to implement a $\Sigma\Delta$ modulator is with SC technique. Their robustness and inherent linearity are the reasons why SC techniques have become as widespread as they are nowadays. It would be a great advantage if the high-quality SC properties could be kept for low voltage operation. However, when designing SC circuits for lower voltages, quite quickly a severe difficulty is encountered due to the switch-driving problem. The low supply voltage does not allow enough overdrive to turn on the transistors used as switches anymore, and SC circuits at low voltages could only be realized either in a special process with extra low threshold voltage transistors or by using an on-chip voltage multiplier. The SO technique, derived from the standard SC technique, is based on the replacement of critical switches with op-amps, which are turned on and off. This technique results in a true very low-voltage operation and can be used in a standard CMOS process.

It is plausible that a circuit with a higher frequency of operation requires a higher power. It is also plausible that performing analog signal processing with increased accuracy requires increased power consumption. So if a certain performance requires certain power consumption, altering the performance through a redesign should change the necessary power consumption. The proper way to think about low power consumption is to define it as a trade off between contradictory specifications, such as accuracy, frequency of operation or signal bandwidth and power consumption. Lowering the power supply at first looks like it lowers the power consumption because the product of voltage and current is smaller. However, lowering the power supply voltage has a number of consequences that on the contrary cause the power consumption to increase, as will be shown and illustrated further on.

In this Chapter the SO technique is treated. As a starting point the problem of low voltage SC signal processing circuits are considered. The key problem is the driving of

the switches. The existing solutions for it are briefly covered. Then the original SO principle is introduced. Next the evolution in this field is described. The endpoint is the differential modified SO integrator cell. Low-voltage, low-power considerations are then discussed in the context of the single loop $\Sigma\Delta$ modulator.

4.1 Switch Behavior

SC circuits are built up of three basic building blocks. An op-amp or an operational transconductance, a switch and a capacitor. Figure (4-1) shows a non-inverting integrator cell. The switches S1 through S6 are clocked with two non-overlapping phases $\phi 1$ and $\phi 2$. C_S is the input sampling capacitor, C_I is the integrating capacitor and C_{Load} is the load capacitor. Lowering the supply voltage of such a circuit has implications on the operation of some of the building elements. The functional property of a capacitor, namely its capacitance is independent of the supply voltage. Op-amps and switches, however, are strongly affected. The former need to cope with much less available voltage drop over each transistor. The later always need a minimal overdrive voltage in order to assure a certain on-resistance. It is possible to design op-amp with quite low supply voltage [58]. The most problematic issue, however, in low voltage SC circuits design is the switching driving problem. About $(V_{tn} + V_{tp} + 0.5 \text{ V})$ is the practical minimal power supply voltage for the switch still has rail-to-rail switch input range [59] [60].

In classic SC circuits a complementary switch is preferably used. Figure 4-2 shows the complementary switch designed using $0.18 \mu\text{m}$ technology. The NMOS and PMOS switch on-conductance in this configuration and in settled condition is given by equation 4-1 and 4-2 [59], where all are referred to ground

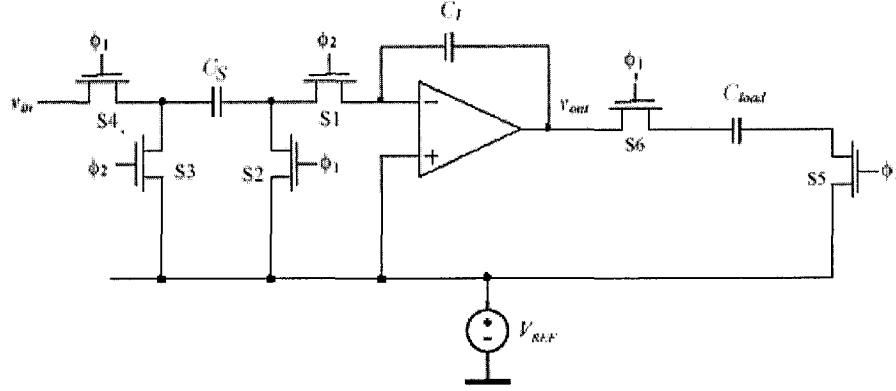


Figure 4-1. Non-inverting SC integrator

$$G_{sw,n} = \left[kP_n \left(\frac{W}{L} \right)_n (V_{dd} - V_{in} - V_{tn}) \right] \quad (4-1)$$

$$G_{sw,p} = \left[kP_p \left(\frac{W}{L} \right)_p (V_{in} - |V_{tp}|) \right] \quad (4-2)$$

Where G_{sw} is the switch conductance.

Assuming that $V_{dd} > (V_{tn} + V_{tp})$, the N-type switch conducts for an input signal from ground on up to V_{tn} below V_{dd} . The p-type conducts from V_{tp} on up to V_{dd} . Figure 4-3a shows the simulated switch conductance for a 1.8 power supply and for a switch W/L dimensions of $0.5 \mu\text{m}/0.18 \mu\text{m}$ using the 0.18um process. The simulated conductance shows that there is no overlapping between G_n and G_p , and that G_n dominates the total conductance, while Figure 4-3b shows the total R_{on} resistance, which varies by 400% for the full input range. Thus rail-to-rail operation is impossible under the $0.18 \mu\text{m}$ technology.

Equation 4-1 and 4-2 indicate that lower switch resistance and thus fast settling can be achieved by up-scaling the device. In trying to increase the size of the P-type to obtain a symmetrical total on-resistance response, Figure 4-4 shows the simulation results after increasing the size of the P-type twelve times the N-type. In the middle region both transistors conduct in parallel. The conductivity for the N and P type overlapped, as

shown in Figure 4-4a, to allow rail-to-rail operation. But the conductivity of the P-type never matches the N-type. The total on-resistance is nearly symmetrical Figure 4-4b, however, the total resistance variation is 170%, thus it is impossible to yield a reasonably a rail-to-rail constant on-resistance. On the other hand, larger switches give rise to a larger clock feed through, an unwanted effect. Also if the minimum desired conductivity for the matched complementary switch is $600 \mu\text{G}$ (Equivalent to $2.1\text{K}\Omega$), then the N and P switches never overlap, and there exists an input range for which neither of the complementary type switches is turned on or conducting anymore as shown in Figure 4-5. From these simulation results, it can be concluded that realization of complementary switch in the $0.1 \mu\text{m}$ technology is not possible.

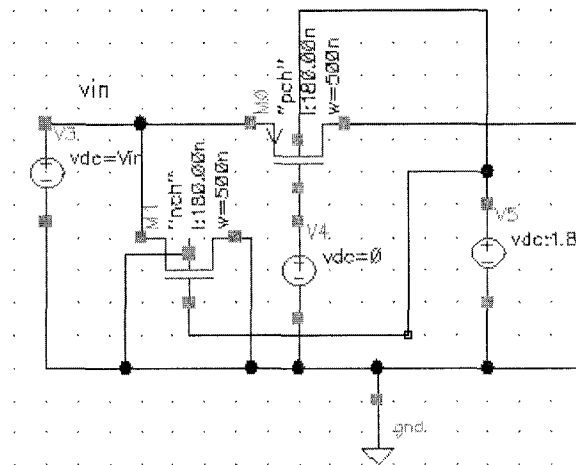


Figure 4-2. Complementary switch

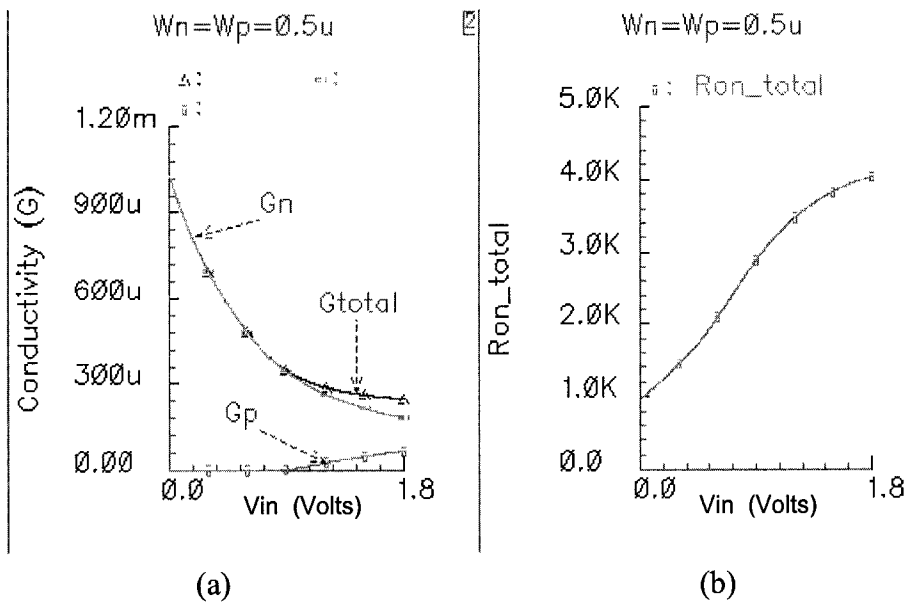


Figure 4-3. Complementary switch simulation results in 0.18 μm process.
(a) Single switch and total conductivity.
(b) The total on-resistance.

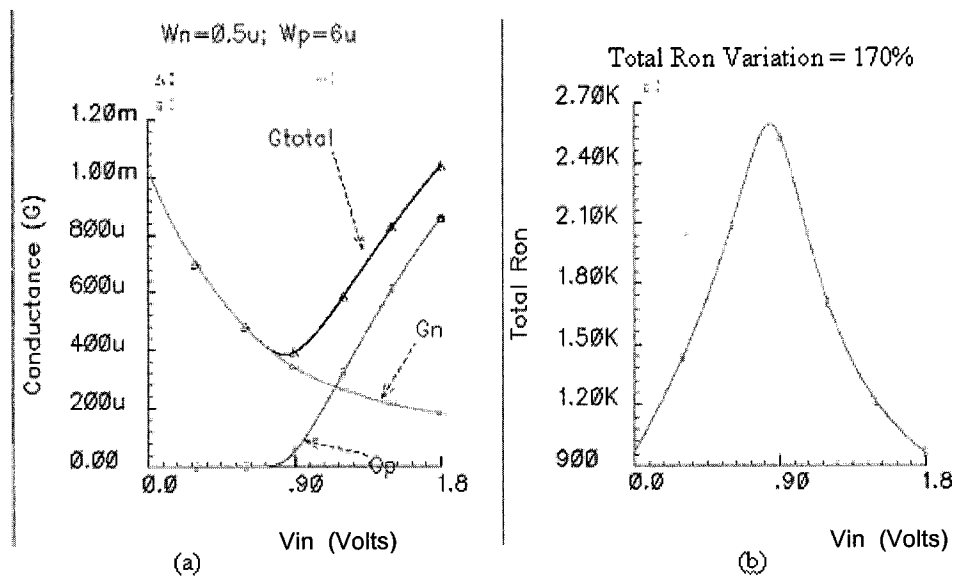


Figure 4-4. Complementary switch with symmetrical on-resistance simulation results in 0.18 μm technology. a) Single switch and total conductivity.
(b) The total on-resistance.

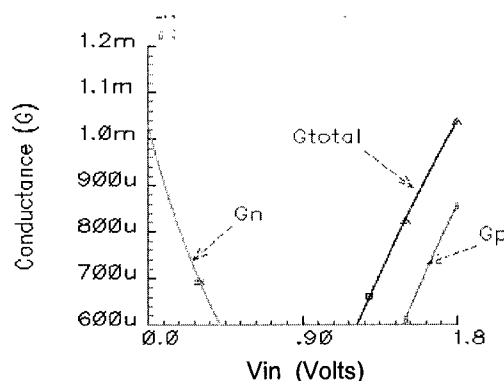


Figure 4-5. Simulation results of the symmetrical on-resistance complementary switch if the minimum conductivity desired is 600 μG (equivalent to an on-resistance of 2.1 $\text{K}\Omega$)

4.2 Single Switch Behavior

The reduced signal range can still be switched if the signal is located in a range where one of the N or P switches is conducting. The best device to choose for applications as a single switch is that the one showing lowest on-resistance. Applying the maximum overdrive voltage on an N-type switch, the on-resistance is 1.63 $\text{K}\Omega$ (Figure 4-6) as compared to 4.8 $\text{K}\Omega$ (Figure 4-7) of the P-type switch with ten times more width and with maximum overdrive voltage as well. Therefore it is safe to say that the NMOST makes the best single transistor switch.

The on-resistance of the switch together with the sampling capacitor defines an RC time constant. Referring to Figure 4-1 again, the input is first sampled onto the sampling capacitor C_S . Assuming a zero internal resistance of the signal source, the settling of the sampling is completely determined and limited by the RC time constant. In the subsequent integration phase the settling process can only go slower than this due to the finite GBW of the op-amp [43].

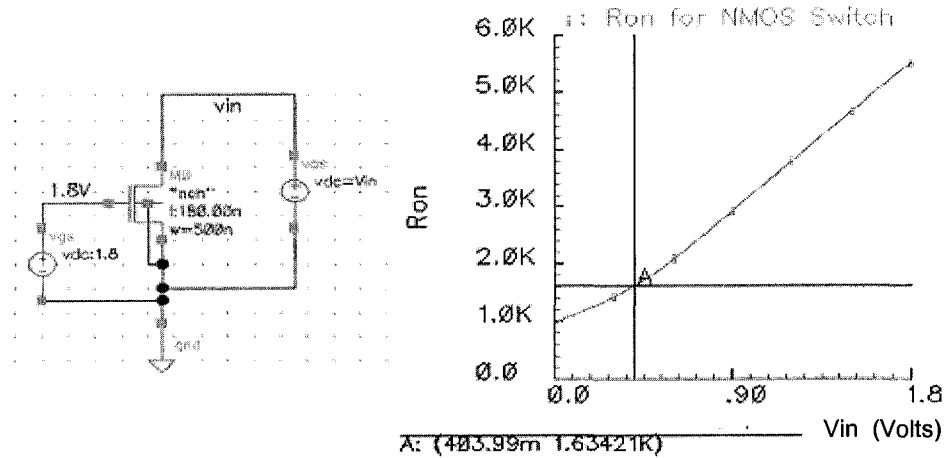


Figure 4-6. Simulation of the N-type switch in 0.18 μm technology. (a) The schematic. (b) The simulated on-resistance.

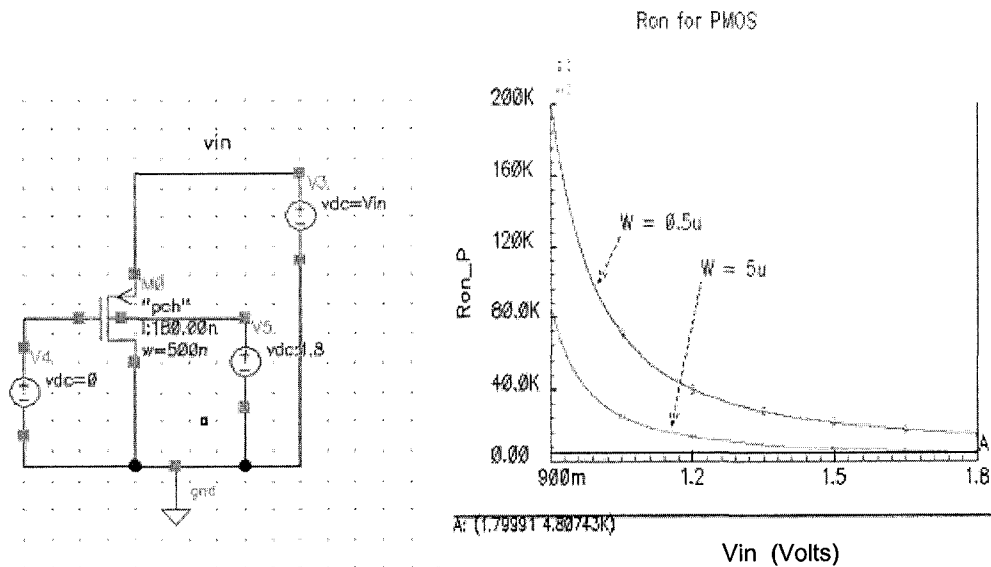


Figure 4-7. Simulation of the P-type switch in 0.18 μm technology. (a) The schematic. (b) The simulated on-resistance with $W_p = 0.5\mu\text{m}$ and $W_p = 5\mu\text{m}$.

4.3 Existing Solutions

It is difficult to realize the complementary switch in 0.18 μm technology, as illustrated above. Four techniques have been developed to overcome the switch limitation. The first one is to use a multi-threshold process, which has low threshold voltage, at least for the NMOST device [61]. This technique has some drawbacks. The switch-off leakage is much higher than in the case of a high threshold voltage. This leakage causes the charge on the integrator capacitor to leak away. This leakage is signal dependent and consequently causes harmonic distortion. Another drawback is the high cost of dedicated low threshold voltage process.

The second technique is to employ voltage multipliers to generate a higher supply voltage on-chip. This method has been particularly useful in the past when an application calls for low-voltage external power source (e.g. 2.4 V battery) but the integrated circuit is fabricated via a high-voltage process (e.g. 5 V for 2 μm CMOS process). Typically all circuit components, excluding the switches and clocks voltages driving them, are designed for operation in low voltage. A few low voltage $\Sigma\Delta$ modulator based on this idea have recently been presented [62] [63]. This technique provides an easy, quick and reliable way of designing low-voltage SC circuits. It is very similar to classic SC circuits, of which the design procedure is well established and well known. Furthermore, it has the advantage that it cuts away an important part of the power dissipation by having the op-amp to work with the low supply voltage. This technique, however, still has some disadvantages. Although the high on-chip generated voltage is only used to drive switches, the voltage multipliers remain area and power consuming. The most important disadvantage is that the recent deep sub-micron technologies are operating with low power supply and will not sustain higher voltages [60].

The third solution to overcome the switch-driving problem is to use the bootstrapping technique [29][64][65][66]. However, the first drawback is that it imposes an instantaneous higher voltage glitch across the thin gate oxide before the inversion takes place under the gate and a channel forms in the MOSFET switch. The second possible drawback is the circuit complexity involved in the implementation of a good bootstrapped switch.

4.4 Original SO Technique

The fourth solution to overcome the switch-driving problem is the SO. This technique allows the design of true low-voltage SC circuits (filters, $\Sigma\Delta$ modulator, etc.) in deep sub-micron technologies [60]. The SO technique would not violate the maximum voltage restrictions of a low-voltage CMOS process. Looking at the SC integrator of Figure 4-1, it can be concluded that there are two types of switches:

1. Switches that have one terminal fixed to a reference level V_{ref} . This connection is either physical as in is the case for switches S2, S3 and S5 connected to V_{ref} , or via virtual ground as for the switch S1.
2. Switches are not connected to the reference voltage but to a signal source. These are the switch S6 connected to the output of the amplifier, and the switch S4 at the very input of the system.

The first type of switch can always be turned on if the switch driving voltage is at least V_t plus an overdrive voltage (V_{ov}) higher than the reference voltage. The second type of switch, however, needs to be able to pass the entire signal range. Because the condition under which the operation is being considered here is for a supply voltage too low to have proper complementary switch operation, these switches present the bottleneck.

The core idea of the original SO technique boils down to eliminate the switch itself at the output of the op-amp. So the switch S6 in Figure 4-1 is plainly replaced by a short as can be seen in Figure 4-8. Leaving S6 out has a few consequences. During the integration phase of the second integrator, the output of the first integrator is shorted to V_{ref} . This calls for inactivation of the first integrator by switching it off; hence the nomenclature of the technique. A second consequence is that the basic SO integrator cell now has a half delay.

The original SO technique further makes the implicit choice to take the dc input level of the op-amp equal to the output level, and both are at the reference level V_{ref} . As a consequence, the output signal swing is less than the available swing, and the switch overdrive voltage is less than maximally possible [44].

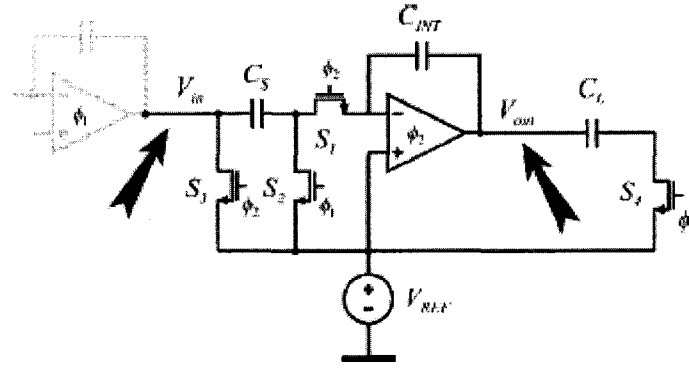


Figure 4-8. The SO integrator preceded by another integrator.

4.5 Modified SO Technique

The modified SO technique enhances output signal swing of the op-amp [67]. The dc level at the op-amp output is taken in the middle of the full output swing, in practice it is taken to $(V_{dd} + V_{ss})/2$. Furthermore, the dc level at the op-amp input is set at V_{ss} . This implies a reference level V_{ref} , (that is equal to the dc level of V_{in}) equals to V_{ss} . These choices are illustrated by Figure 4-9. Due to the mentioned modifications, the modified SO technique allows one to reduce the power-supply voltage. The dc offset that exists on a sample taken of the op-amp output signal should be removed before being applied to next op-amp. This is done by C_{CM} in the modified SO integrator cell, which is shown in Figure 4-10 in differential form. The idea is to remove it with an equal charge injection of the opposite polarity that is performed with a capacitor. The proper scaling of C_{CM} is $C_S/2$ [60]. The capacitors C_S and C_{INT} are the sampling and integrating capacitors. Proper operation also requires a high reference level, taken to V_{dd} . The output of the op-amp must be shorted to V_{dd} during its off phase because shorting it to V_{ss} would forward bias the junction diodes of the switches connected to the op-amp input nodes. Since two reference levels are now present, they are distinguished by the terminology $V_{REF,hi}$ and $V_{REF,lo}$, taken equal to V_{dd} and V_{ss} , respectively. These two reference voltages can in principle be chosen differently from V_{dd} and V_{ss} . [44].

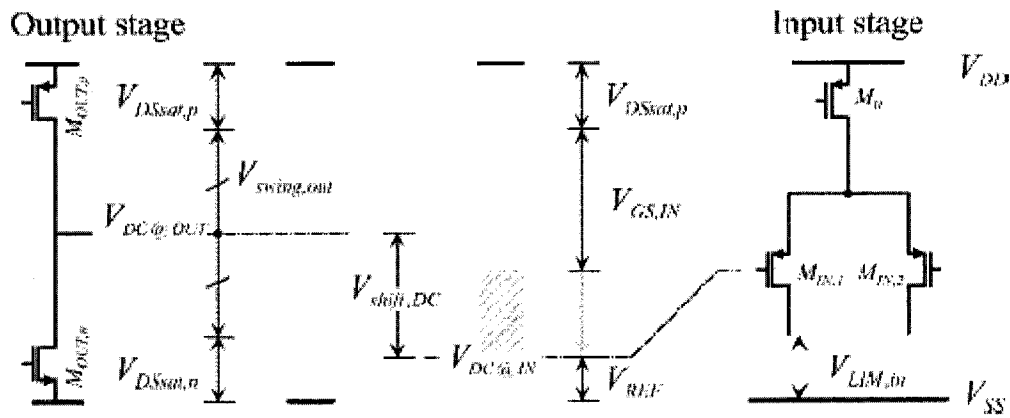


Figure 4-9. The signal swings in the modified SO technique.

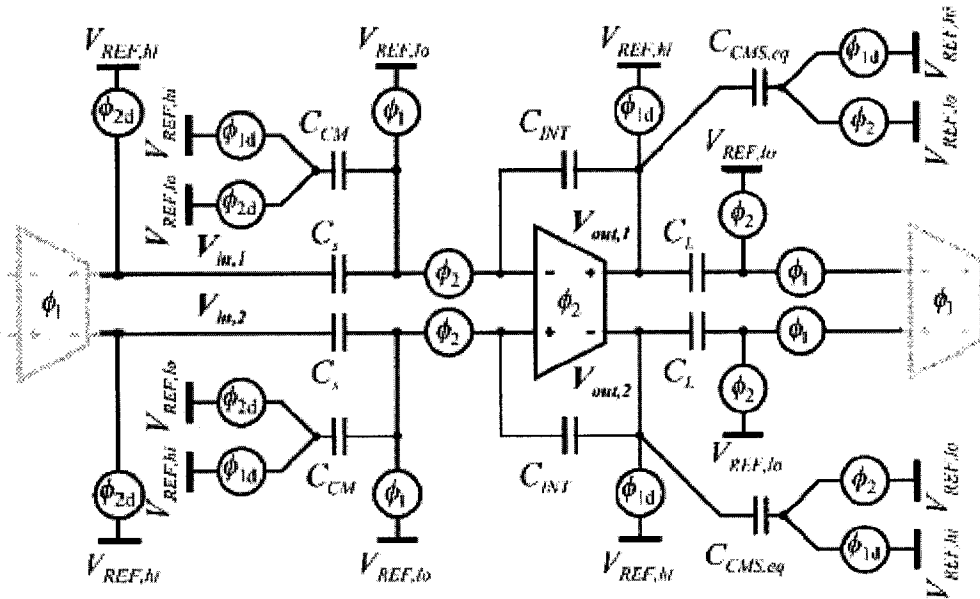


Figure 4-10. The differential modified SO integrator cell

4.6 Quantization and Circuit Noise

The theoretical $\Sigma\Delta$ modulator is only determined by the in-band quantization noise suppression. The in-band quantization noise for an n th-order oversampling $\Sigma\Delta$ modulator is given by [45]:

$$N_Q = \frac{\Delta^2}{12} \frac{\pi^{2n}}{(2n+1)OSR^{(2n+1)}} \quad (4-3)$$

Where Δ is the separation between consecutive levels in the quantizer, OSR is the oversampling ratio and n is the order of the modulator.

While the performance of the theoretical $\Sigma\Delta$ modulator is only determined by the in-band quantization noise suppression, the physical implementation of the system with solid-state devices has to deal with other noise sources as well. The main additional noise sources of a CMOS implementation are thermal noise and the flicker noise ($1/f$ noise).

The circuit noise to be dealt with a $\Sigma\Delta$ modulator is the noise injected into the input summing node. The noise generated in the internal nodes of the loop is suppressed by the high loop gain. In a sampled data $\Sigma\Delta$ modulator, the noise is generated by the on-resistance of the switches in the sampling and integrating process. An approximate expression for the in-band thermal white noise power is

$$N_T = \alpha \frac{kT}{C_s OSR} \quad (4-4)$$

Where α depends on the specific way of performing the feedback, k is the Boltzman constant, T is the absolute temperature, C_s the sampling capacitance, and OSR is the oversampling ratio

Noise from the switches is the sum of the sampled noise in the sampling phase and in the integration phase. It is band limited by the RC time constant during the sampling phase and by a combination of this and the amplifier's time constant during the

integration phase. There is a noise contribution associated with each capacitor in parallel with the sampling capacitor. Equation 4-5 and 4-6 holds for the case of the modified SO integrator (Figur.4-10) including feedback capacitors (C_{FB}), which besides the sampling capacitor C_s and the C_{FB} capacitor also has a common-mode adjust capacitor C_{CM}

$$P_{N,sw} = P_{N,sw,samp} + P_{N,sw,int} \quad (4-5)$$

$$P_{N,sw} \approx \frac{2kT}{C_s \cdot OSR} \left(1 + \frac{C_s}{C_{FB}} + \frac{C_s}{C_{CM}} \right) \quad (4-6)$$

Equation 4-5 and 4-6 reveal that the noise is increased by the addition of capacitors at the input. The switch noise is directly increased. C_{CM} plays a large role, since it is only half the size of C_s .

For this particular realization (second-order modulator), the complete expression for the in-band circuit noise is [11]:

$$N_c = \frac{2kT}{C_s \cdot OSR} \left(1 + \frac{C_I}{C_s} \right) + \left(\frac{kTR_{eq,opamp}GBW}{OSR} + 4k_{opamp} \ln(f_b) \right) \left(1 + \frac{C_I}{C_s} \right)^2 \quad (4-7)$$

The first term of equation 4-7 can be replaced by equation 4-6 for the modified SO integrator of Figure 4-10. While the second term in equation.4-7 represents the white and flicker noise generated in the op-amp, where $R_{eq,opamp}$ is the hypothetical equivalent resistor for the op-amp white noise, k_{opamp} is a coefficient for the op-amp's flicker noise, and f_b the signal bandwidth. C_s is the sampling capacitance and C_I is the integrating capacitance.

A schematic representation of the different noise types is shown in Figure 4-11. The SNR of a $\Sigma\Delta$ modulator is determined by the ratio of the signal power (S) and both the circuit and quantization noise (NC and NQ, respectively):

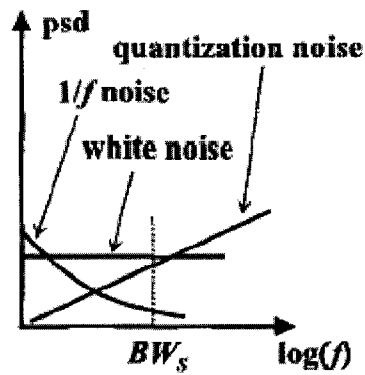


Figure 4-11. The noise power spectral densities

$$SNR = \frac{S}{N_c + N_q} \quad (4-8)$$

Diminishing the quantization noise can be done by choosing a higher OSR or a higher modulator order. If the modulator order is greater than two, stability needs to be discussed. Stabilizing then requires the use of deliberately chosen parameters and more complicated transfer functions than just a cascade of integrators and possibly the use of reset circuits in the integrators in case instability happens.

Diminishing the thermal noise is done by choosing a larger sampling capacitor and larger OSR. All of these operations require an extra power allocation. A higher OSR require all the integrators to settle faster, thus SR and GBW must increase. In a first-order estimation, the extra power consumption is equal to the relative OSR increase: doubling the OSR causes double power consumption. A higher modulator order requires an extra integrator for each additional order in a classical SC circuits and the modified SO case. Because the SO system have a duty cycle of 50%, the power consumption for the second-order SO is half of the corresponding one in SC circuits.

The first integrator needs to drive the input sampling capacitor. In order to reduce the thermal noise power by a factor of two, the input sampling capacitor must be increased with a factor of two.

4.7 Intrinsic Constraint of Power Consumption

Generally Low supply voltage in analog circuit causes higher power consumption. This is not awkward. A small input voltage must be used. A certain DR requirement puts a specification on the thermal noise level. This later requires a minimum sampling capacitor size. The smaller the input voltage, the larger the capacitor must be. The capacitor is a load to the op-amp in the integrator. The integrator must settle to an error set by the DR. Due to the higher load, a higher transconductance is needed, which is set by the bias current; hence the higher power consumption. This process is given by the following expression [66].

$$P \propto kTDR^2 BW \frac{V_{ov}}{V_{DD}} \quad (4-9)$$

Where BW is the signal bandwidth, DR is the dynamic range, and V_{ov} is the $V_{GS}-V_T$ of the input stage transistors.

The proportionality expression for the power consumption of an integrator Equation 4-9 reveals that lowering the supply voltage increase the power consumption due to the fact that the input signal must scale down at the same time. This fact might be called the low voltage low power consideration. Low voltage SC circuits are thus expected to show a less favorable power–resolution-bandwidth trade-off. It also suggests that lower supply voltage favored by digital circuits and required by deep sub-micron CMOS process will have an adverse effect on power dissipation for analog circuits.

The proportionality (equation 4-9) also tells something about the region of operation of the transistors as well. For low power the over-drive voltage should be minimized. When lowering V_{ov} for a constant current, the transistor width increased, and so does C_{GS} . The latter is a parasitic load capacitance to the amplifier in the integrator that is seen in parallel with the sampling capacitor. In many low voltage applications such large C_s is required that for the required speeds of operation, the parasitic C_{GS} is negligible. Hence for low voltage and low power operation the over-drive voltage is best reduced as much as necessary, but not more. If the supply voltage is not too low a bias in the transition region between weak and strong inversion is recommended.

4.8 Practical Constraints of Power Consumption

The settling speed of an integrator is determined by its GBW. The GBW of the modified SO integrator (Figure 4-10) is given by [44]

$$GBW_{\text{int}} = \frac{g_{\text{meff}, \text{opamp}}}{C_{L, \text{eff}}} \quad (4-10)$$

With:

$$C_{L, \text{eff}} = C_s + C_{CM} + C_{FB} + \frac{C_L + C_{CMS, eq}}{F_{dc}} \quad (4-11)$$

$$F_{dc} = \frac{C_{INT}}{C_S + C_{FB} + C_{CM} + C_{INT}} \quad (4-12)$$

Capacitance C_{FB} is the feedback capacitor in a modulator. These expressions show that all the capacitors cause a largely increased capacitive load. There are more capacitors and the feedback factor becomes smaller, which increases the effective load capacitance. The increased effective load capacitance increases the power consumption.

4.9 Suppression of Noise Generated Inside the Loop

An important property of a $\Sigma\Delta$ modulator that must be made use of in order to save power is the reduction of noise sources inside the loop. The reduction of the noise on node K in a single-loop $\Sigma\Delta$ modulator with integrator coefficient a_i and for oversampling ratio OSR is quantified by the factor [44] [60]

$$F_{\text{sup}, K} = \frac{OSR^{2K}}{\pi^{2K}} (2K + 1) \left(\prod_{i=0}^K a_i \right)^2 \quad (4-13)$$

So, noise injected at the internal summing nodes is reduced so much by the large gain of the preceding integrators that it can be neglected. The thermal noise sources internal to the loop are strongly suppressed. Therefore the size of the capacitors inside

the loop can be made much smaller than the input sampling capacitors. The corresponding op-amps need lower transconductance. The output stage of the op-amp is scaled down, and with it, its power consumption. For low power operation it is thus imperative that the integrators are scaled down progressively.

4.10 System Level Power Saving

There is basically only one option for power saving in a SO integrator and it is on the system level. The intrinsic SO integrator is a half delay integrator. It is off during 50% of the time. This means that a power saving of almost 50% is possible without any drawback.

Chapter 5

Building Block Design

This Chapter describes the design of the SO $\Sigma\Delta$ modulator building blocks implemented in the TSMC 0.18 μm single-poly, six-metal CMOS process with 1.8 V power supply voltage. Details of the SO and feedback circuit design are discussed. Digital part is designed. It includes the design of the non-overlapped clock generator; half-delay circuit and set reset FF.

5.1 Switched Op-Amp

The low supply voltage prevents from using stacked structures at the amplifier output. A two-stage amplifier is needed to guarantee the desired gain. To avoid the power supply noise a practical SO circuit has to be differential, which demands a common-mode feedback (CMFB) to be included in the amplifier [54] [47]. The designed SO is similar to the one presented in [68]. It consists of an input stage, class A (or common source) output stage, the common-mode feedback (CMFB) stage and the switching circuit to realize the SO operation.

Figure 5-1 shows the input and the output stage. The input stage consists of a PMOS input pair (M1,2) and a folded load consisting of four equal sized PMOS transistors (M4,5,6,7). The differential signal, between n3 and n4 nodes, sees high load impedance since the transconductance of M4 and M5 are cancelled by the transconductance of the cross coupled devices named M6 and M7. However, for a common mode (CM) signal, the impedance is low and thus the CM voltage in the first stage output is stable enough without a common mode feedback (CMFB).

The class A output stage consists of the common source connected gain transistors (M12 and M13), and the current source loads (M14 and M15). The current flow in the output stage is interrupted by the switches Ms5 and Ms6 in order to realize the SO principle. When the op-amp is off, they switch the output stage to the high impedance state and pull Vo+ and Vo- to Vdd. Ms1 is on, thus n1 and n2 are shorted to

prevent the input stage from saturating. The compensation capacitors c_0 and c_1 are connected to the cascode node of the input stage (n_1 and n_2), which provides faster settling than the classic Miller-compensation. The capacitors are disconnected when the op-amp is in the off state by the switches M_{s2} and M_{s3} . This brings two advantages. The charge in the capacitors is preserved which speeds up the turn on if the subsequent output values do not differ much. In addition the compensation capacitors also boost the common mode feedback during the turn on by injecting current in the nodes n_1 and n_2 .

Due to the switching operation of the amplifier as it is turned off for one half of the clock cycle and its outputs are forced to either ground or V_{dd} . Fast recovery from the off state need to be insured and the CMFB circuit has to be fast and capable of providing large current to the output. Typically the common-mode level of the two stages needs adjustment. In [69], the need for CMFB in the first stage is eliminated and the fully differential two-stage amplifier needs CMFB only for the second stage, and thus a fast a simple passive CMFB circuit may be used. The CMFB circuit is shown in Figure 5-2. When the op-amp is in the off state, V_{o+} and V_{o-} are connected to V_{dd} and the node n_0 of the CMFB circuit to V_{ss} . At the same time the capacitors c_3 is reset. When the op-amp is turned on, the output CM voltage ($V_{dd}/2$) is sensed with a capacitive divider formed by the capacitors c_1 and c_2 . The capacitor c_3 is switched to V_{dd} restoring the operating point of node n_0 to V_{ss} . The capacitor c_4 is used to shift the DC level of the sensed CM signal to the proper level for the op-amp CMFB input. The offset voltage in the capacitor is refreshed during the amplifier off phase. The diode-connected transistor provides this voltage M_6 that together with the dummy switch M_7 forms a replica of the current source in the op-amp output stage. The PMOS switch M_4 has a relatively small overdrive, thus its on-resistance is high. However, since the purpose of the switch is to maintain the constant percentage in c_4 , the poor conductivity is not a problem.

The op-amp is designed for an input CM voltage of 0 V and an output CM voltage of $V_{dd}/2$. The requirements for the op-amp for the first integrator are much stringent than that of the second integrators. This is due to scaling down the integrating capacitor. Thus output stage of the second op-amp is scaled down.

Table 5-1 gives the dimensions of the transistors and capacitors for the integrators. The second op-amp differs from the first op-amp by the size of the output

devices and is given between parentheses in the Table. The simulated op-amp performance is shown in Figure 5-3 and 5-4. The specifications for the first op-amp are summarized in Table 5.2, while the specification of the second is given in Table 5-3.

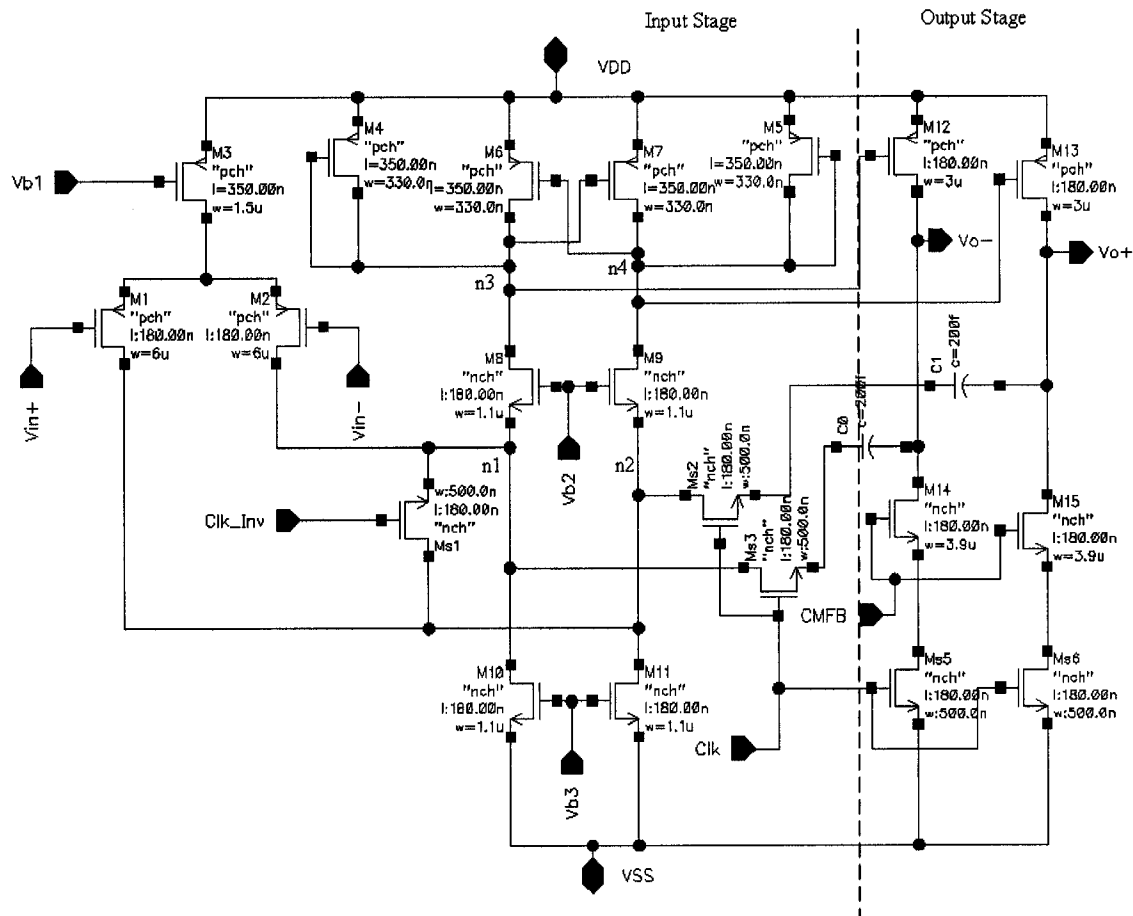


Figure 5-1. Folded cascode two stage op-amp

Table 5-1 Cell values for the op-amps

Element	Width/Length	Element	Width/Length
M1, M2	6 μm /0.18 μm	M12, M13	3 μm (1.3 μm)/0.18 μm
M3	1.5 μm /0.35 μm	M14, M15	3.9 μm (0.5 μm)/0.18 μm
M4, M5, M6, M7	0.33 μm /0.35 μm	C0, C1	200 fF
M8, M9, M10, M11	1.1 μm /0.18 μm	Ms1, Ms2, Ms3, Ms4, Ms5	0.5 μm /0.18 μm

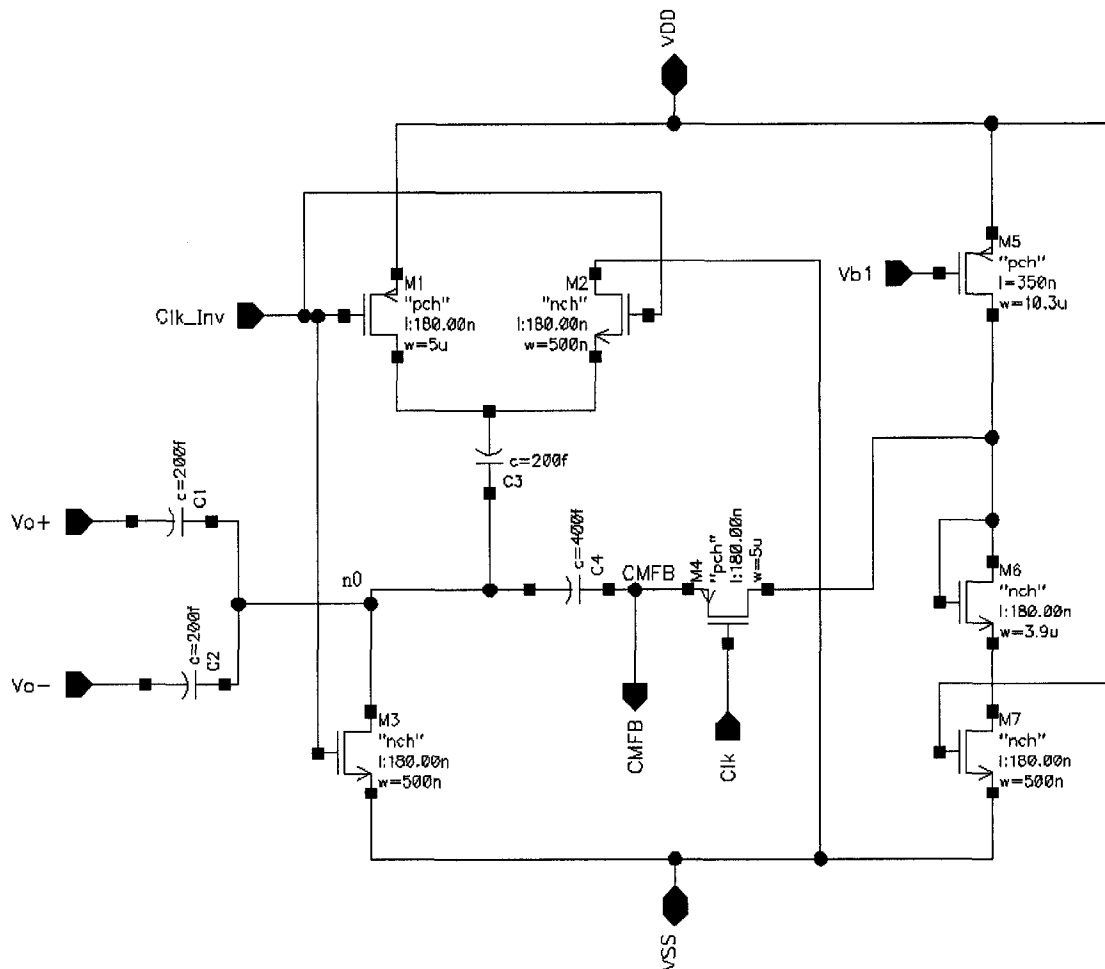


Figure 5-2. The common-mode feed back circuit

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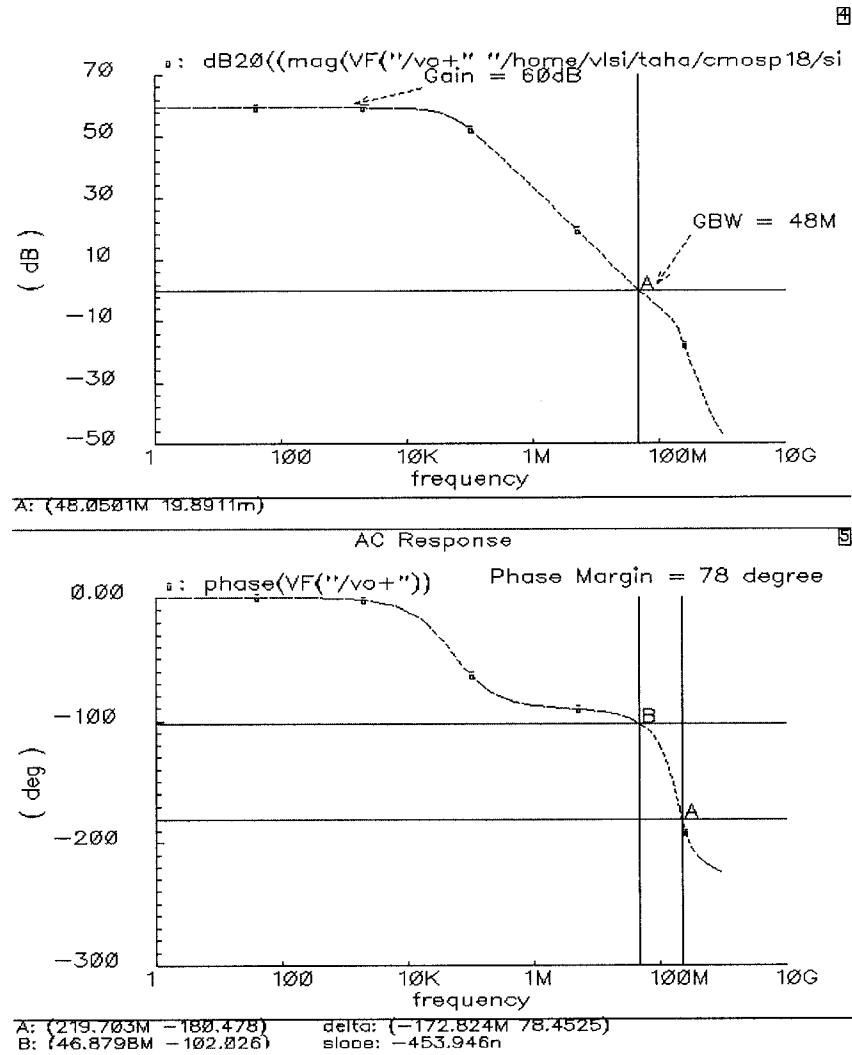


Figure 5-3. The ac response of the op-amp

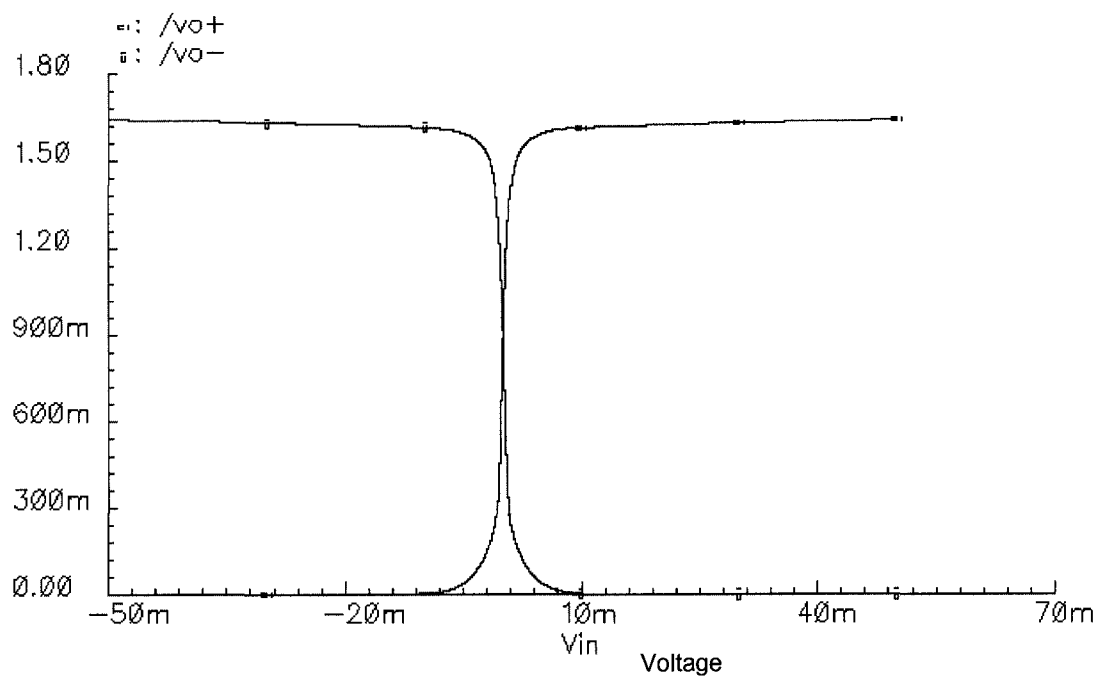


Figure 5-4. The DC response of the op-amp

Table 5-2 Simulated performance of the first and second op-amp

Parameter	1 st Integ.	2 nd Integ
DC gain	60 dB	59 dB
GBW (CL = 5pF)	48 MHz	45 MHz
Phase margin	78°	75°
Output swing	0-1.7 V	0-1.7 V
SR	21 V/ μ s	16 V/ μ s
Input common-mode range	-100m V-500 mV	-100 mV-500 mV
Output common-mode	0.9 V	0.9 V
Current (on/off)	374 μ A/274 μ A	250 μ A/145 μ A
Power Consumption (on/off)	674 μ W/274	450 μ W/261 μ W

5.2 Switched Op-Amp Integrator

The SO integrator is implemented using the designed SO in section 8.1. Figure 5-5 shows the circuit implementation of the SO integrator. Figure 5-6 is the simulation result showing the output CM of 900 mV that is obtained applying zero input. It reset to 1.8. Figure 5-7 show the transient simulation results applying step input.

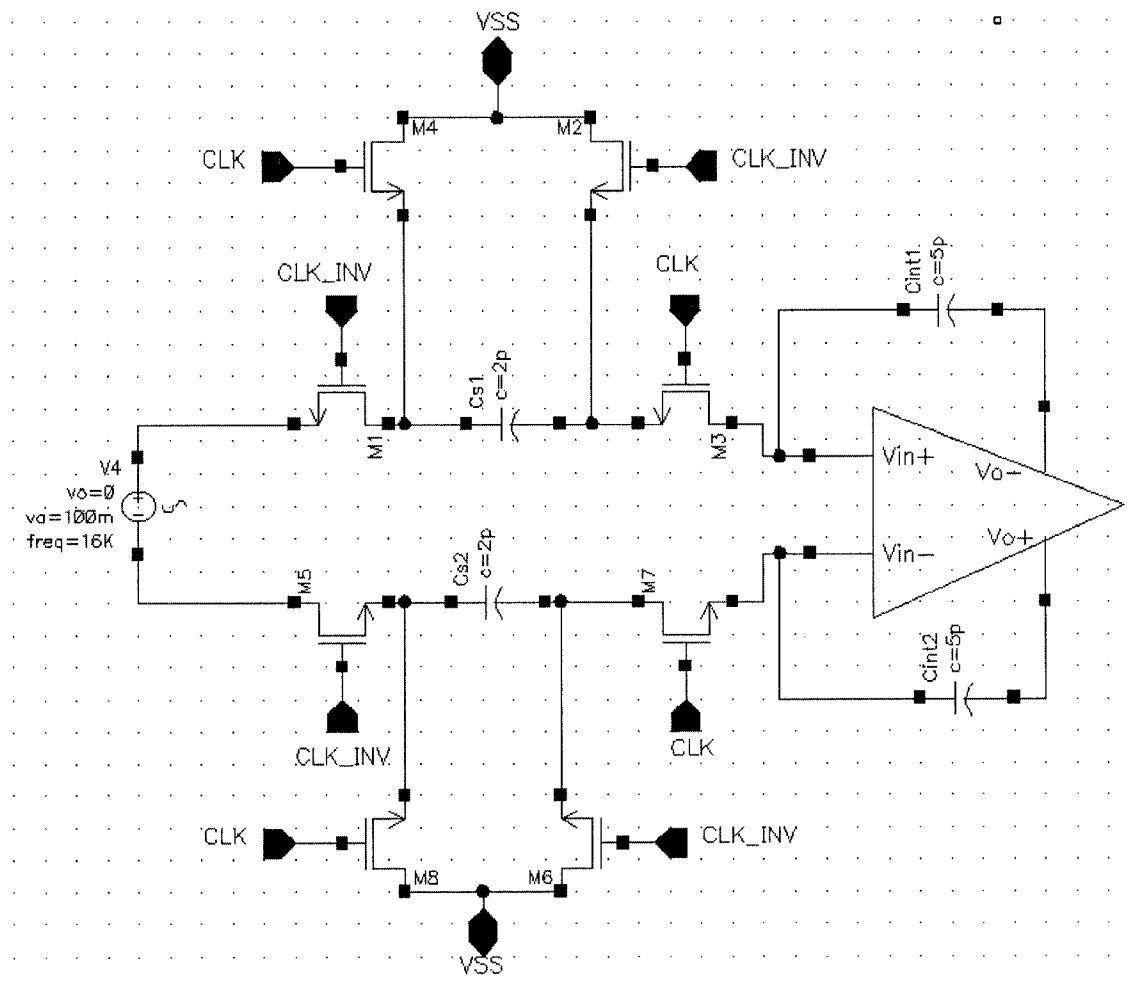


Figure 5-5. SO integrator

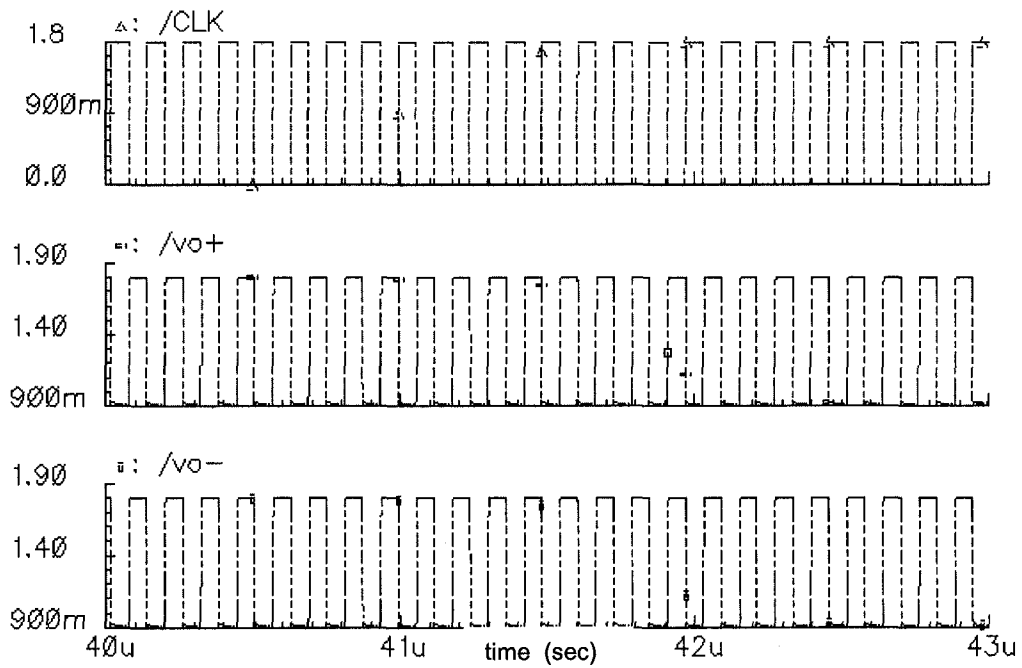


Figure 5-6. Output CM simulation result

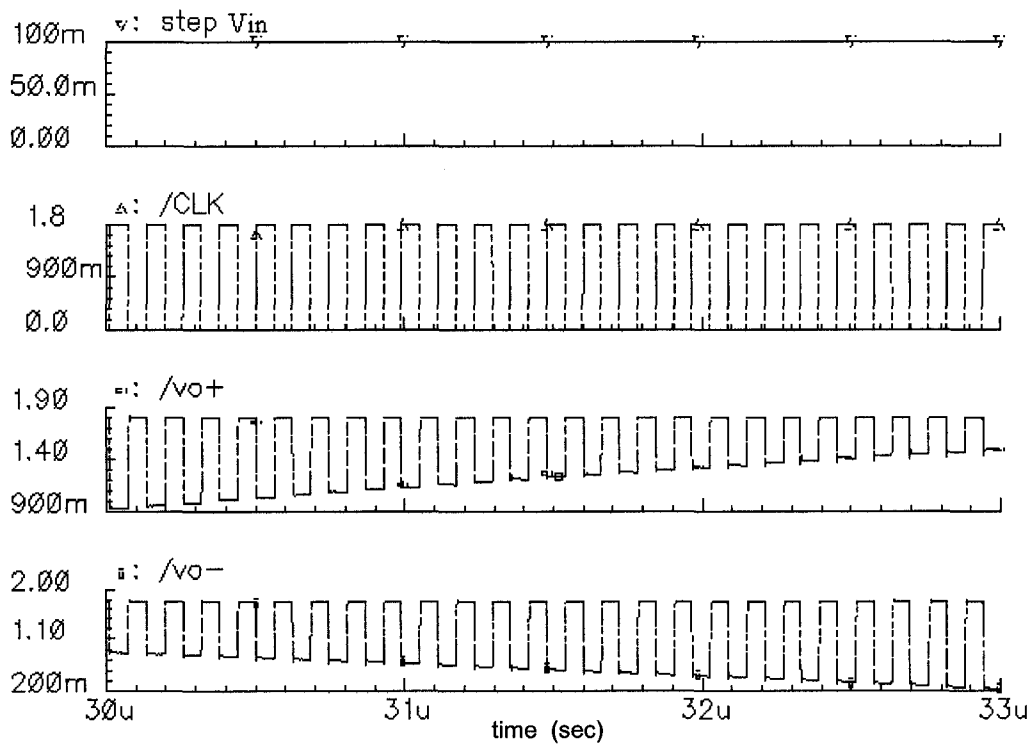


Figure 5-7. Transient response to a step input

5.3 Comparator

A high speed, high resolution CMOS comparator is designed. The topology is shown in Figure 5-8. It consists of three stages, namely the input stage, a positive feedback or decision stage (regenerative latch), and an output stage. The input stage amplifies the input stage to improve the comparator sensitivity and isolates the input of the comparator from switching noise coming from the positive feedback stage (decision stage). The positive feedback stage is used to determine which of the input signals is larger. The first set of inverters at the output stage work as buffers, amplify this information, recover signal levels and output a digital signal. The second set of inverters is added to obtain the reset to zero operation.

The input stage and the decision circuit are similar to the circuit presented in [30]. The comparator is designed for an input CM voltage of 900 mV. The decision stage is designed with some hysteresis for the use in rejecting noise on a signal. M7, M8 are cross-gated so the positive feedback increases the gain of the decision stage. Before design with hysteresis, M7,8,11,12 are of the same size. When $V_{in} = V_{ref}$, the drain currents of M7 and M8 equals and all transistors are in saturation. If V_{in} increases more than V_{ref} , such that the drain current of M9 is much larger than that of M10, then M7,12 are on and M8,11 are off. If V_{in} decreases such that the drain current of M10 increases and the drain current of M9 decreases, switching takes place when the drain-to-source voltage of M7 equals the threshold voltage of M8. At this point, M8 starts to take current away from M12. This decreases drain-to-source voltage of M12 and thus starts to turn M7 off. Switching takes place such that M12 and M7 are off when the gate-to-source voltages of M7,12 are less than the threshold voltage of the devices. Hysteresis is designed by having W/L of M7,8 more than that of M11,12. The switching point voltage is given by [30]:

$$V_{switching} = V_{in} - V_{ref} = \frac{I_{D,M2}}{gm_{1,2}} \frac{\frac{\beta_{M7,8}}{\beta_{M11,12}} - 1}{\frac{\beta_{M7,8}}{\beta_{M11,12}} + 1} \quad \text{for } \beta_{M7,8} > \beta_{M11,12} \quad (5-1)$$

M37, M38 are the switches used. The input stage does not contain any switches; as a result no clock feed through is injected to the input nodes. When the switch is closed, out_1, out_2 are low, and the comparator outputs, out+ and out- reset to 0.

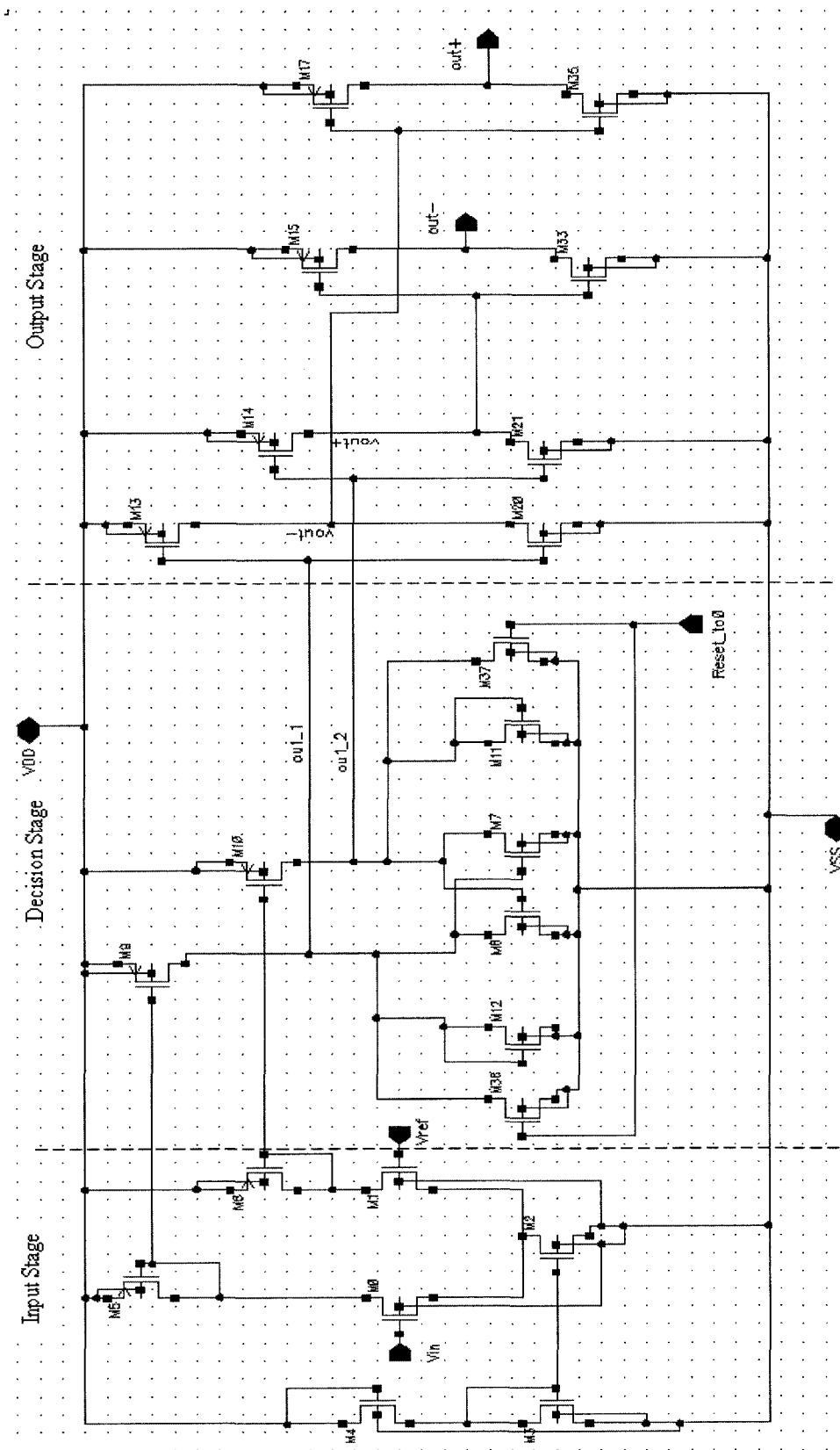


Figure 5-8. Three stage comparator

Simulated comparator performance is shown in Figure 5-9 to Figure 5-2. Table 5-3 gives the dimensions of the transistors. The specifications are summarized in Table 5-4

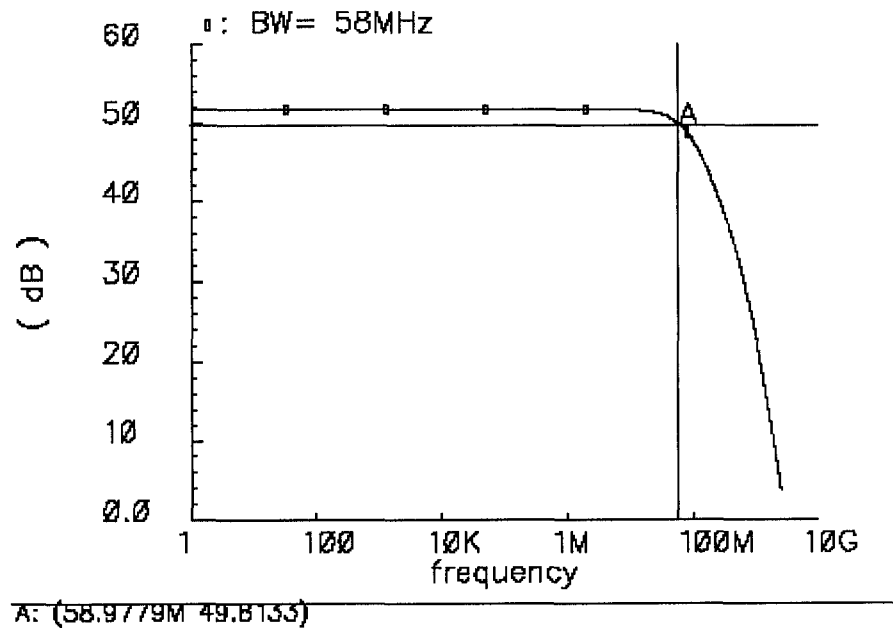


Figure 5-9. The ac response of the comparator

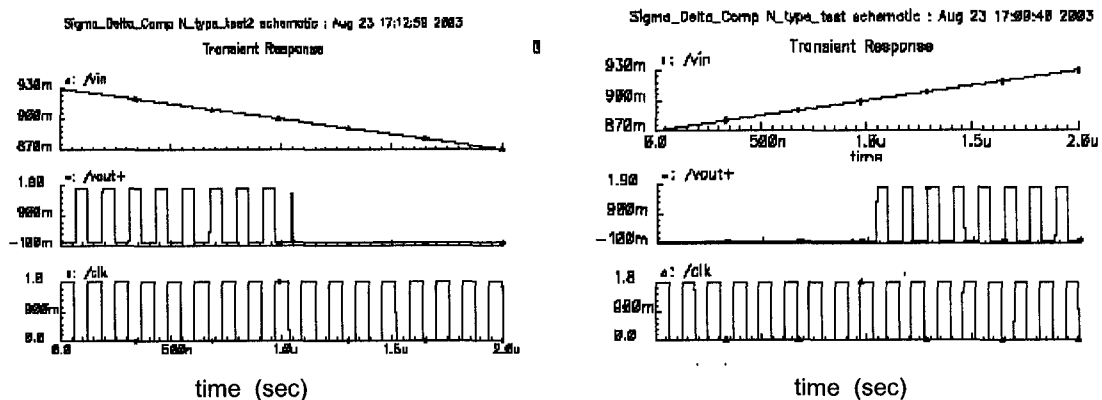


Figure 5-10. Comparator response to a ramp input.

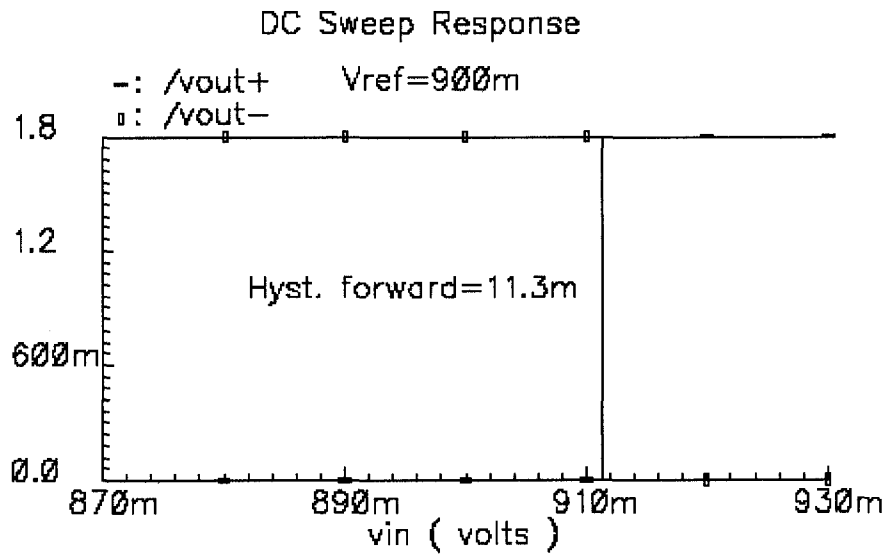


Figure 5-11. Simulating hysteresis in the forward direction

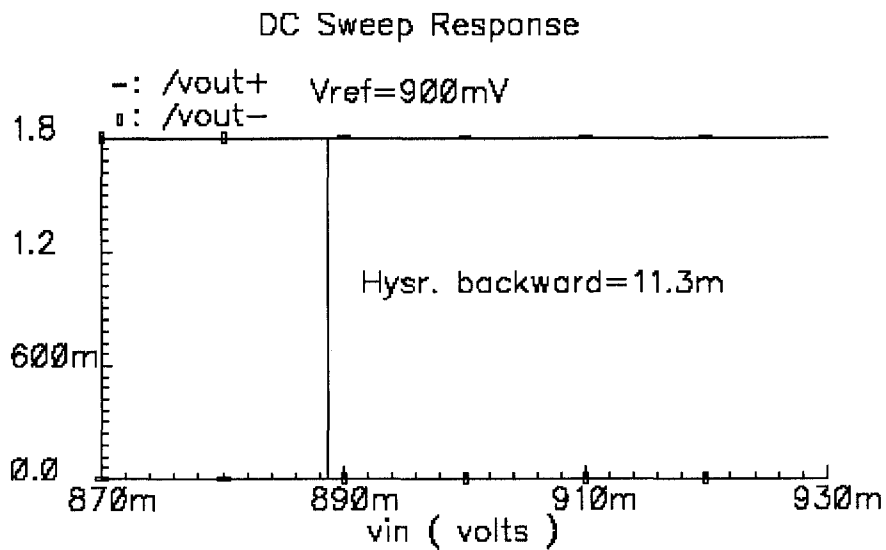


Figure 5-12. Simulating hysteresis in the backward direction

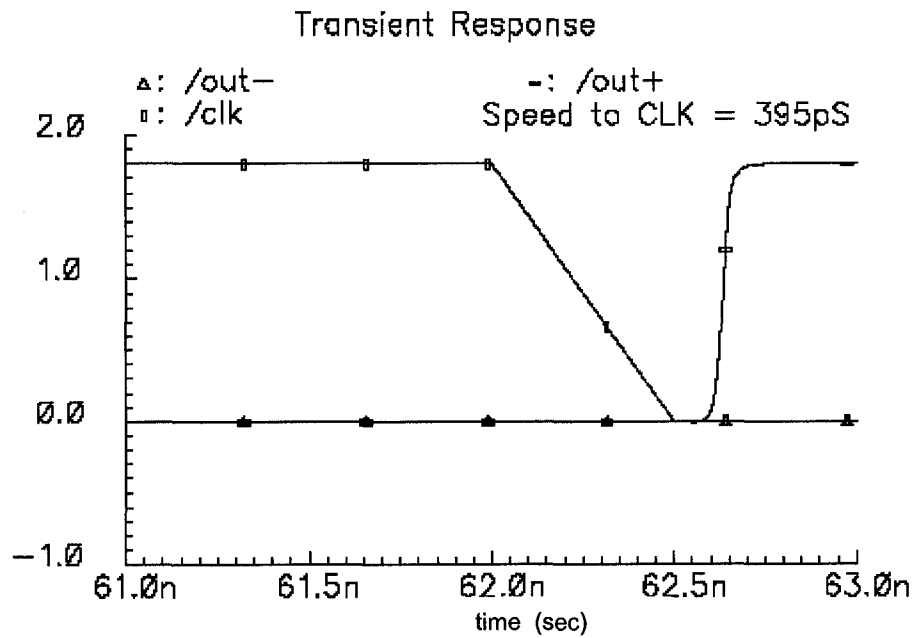


Figure 5-13. Simulating the comparator speed

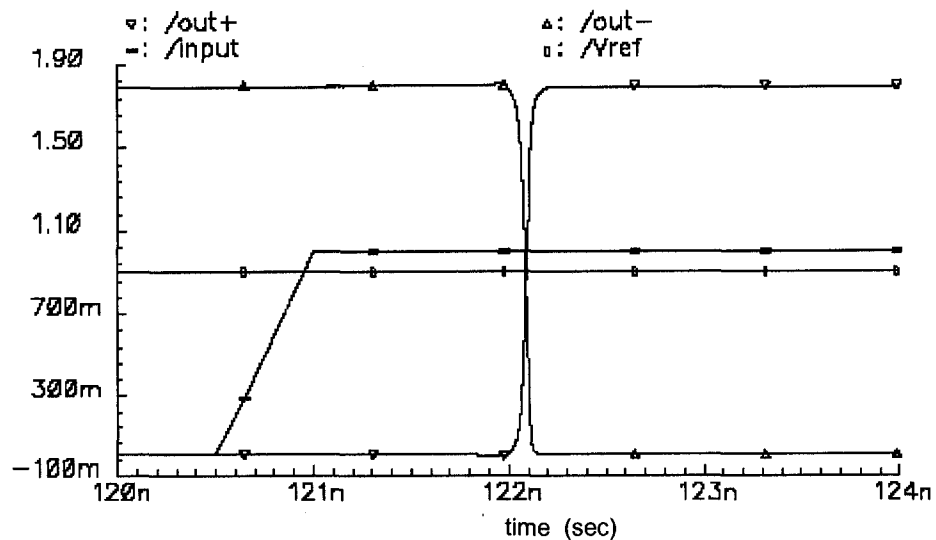


Figure 5-14. Simulating the comparator propagation delay

Table 5-3 Cell values of the comparator

Element	Width/Length	Element	Width/Length
M0, M1	1.4 μm /0.18 μm	M37, M38, M33, M35	0.5 μm /0.18 μm
M2	0.7 μm /0.35 μm	M5, M6, M9, M10	0.5 μm /0.35 μm
M7, M8	0.5 μm /1 μm	M13, M14, M15, M17	2 μm /0.18 μm
M11, M12	0.5 μm /1.21 μm	M20, M21, M33, M35	0.5 μm /0.18 μm

Table 5-4 Comparator Specifications

Propagation delay	1.2 ns
Hysteresis	11.3 mV
Current (on/off)	34 μA /14 μA
Power consumption (on/off)	61 μW /25 μW
Bandwidth	58 MHz
Vref	900 mV
Speed to clock	395 ps

5.4 Biasing Circuit

The biasing required for the op-amps and the comparator are designed with all CMOS voltage divider and shown in Figure 5-13. The values of the transistors are listed in Table 5-5

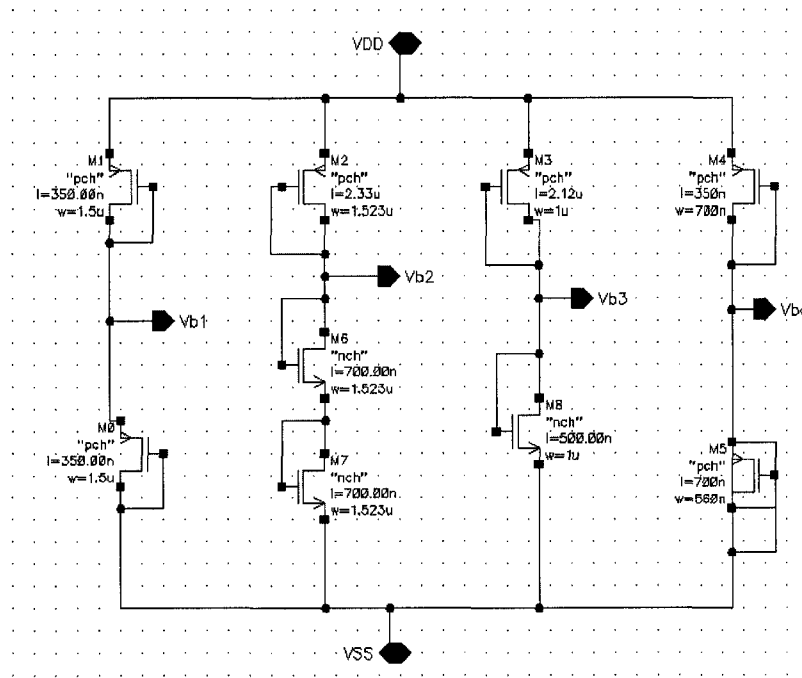


Figure 5-15. The biasing Circuit

Table 5-5 Cell values for the biasing circuit

Element	Width/Length	Element	Width/Length
M0, M1	1.5 μm /0.35 μm	M5	0.56 μm /0.7 μm
M2	1.523 μm /2.33 μm	M6, M7	1.523 μm /0.7 μm
M3	1 μm /2.12 μm	M8	1 μm /0.5 μm
M4	0.7 μm /0.35 μm		

5-5 Half Delay Circuit

Half clock period delays, required in the modulator feedback loop, are realized using D and S bar R bar FFs. The gates and the FFs are realized using static logic design. Figure 5-15 shows the designed circuit and Figure 5-16 shows the simulation result.

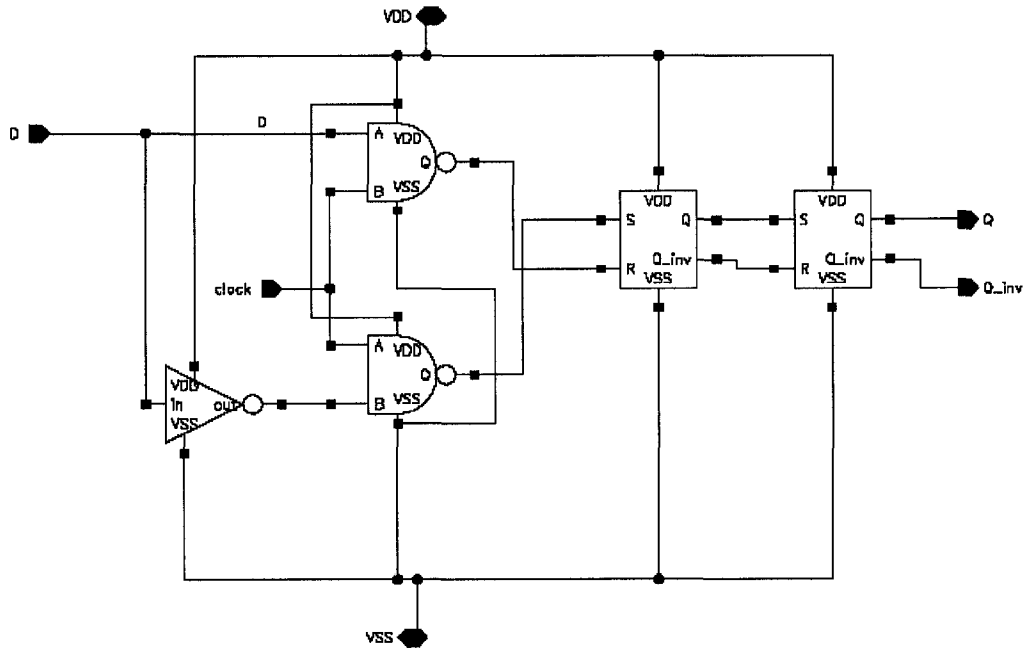


Figure 5-16. Half delay circuit

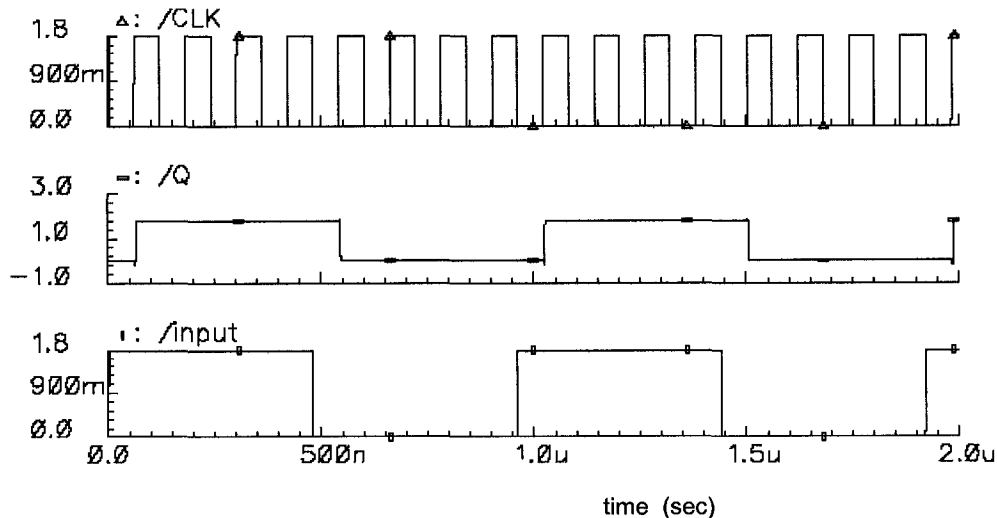


Figure 5-17. Half delay circuit simulation result

5.6 Clock Generator

Two-phase non-overlapping clocks are required in a SC circuit to reduce the signal dependent charge injection. A timing block, shown in Figure 5-17, generates a non-overlapping two-phase clock “CLK” and “CLK_INV”. In addition two slightly delayed versions are also generated. The timing block is controlled by an external master clock. The clock driver is formed using inverters and two NOR gates. One input terminal of both of the two-input NOR gates is driven by a cross-feedback which guarantees the non-overlap feature of the clock phases. Figure 5-18 shows the timing diagram.

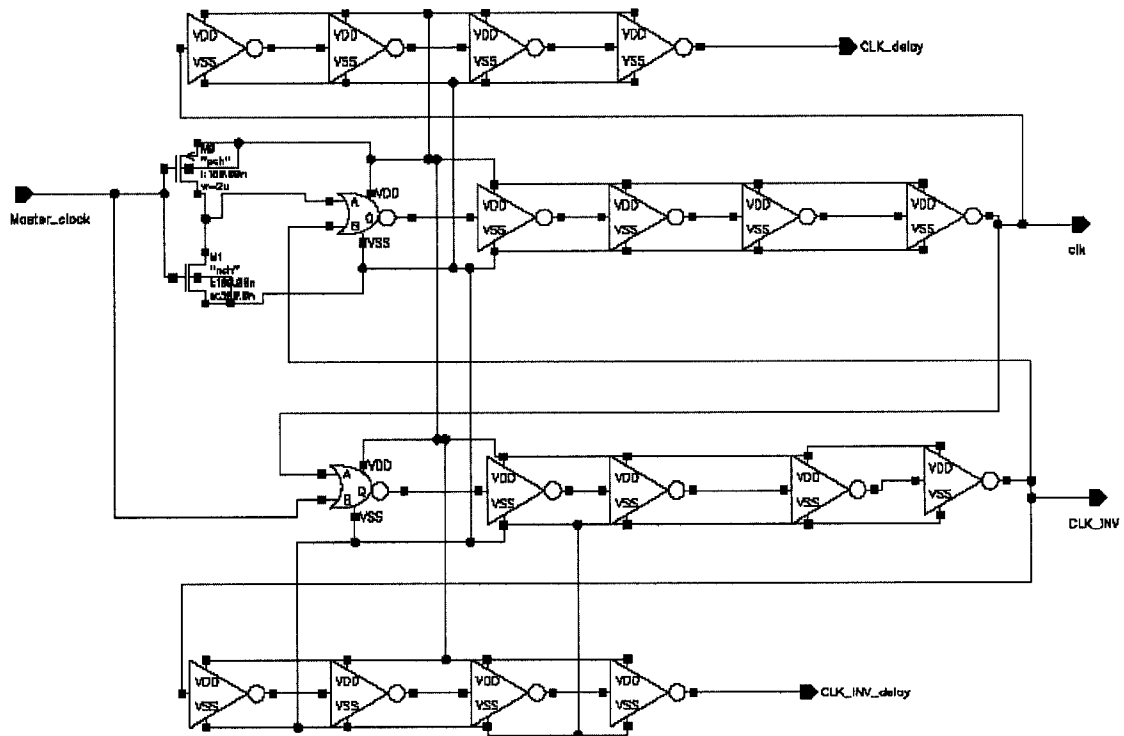


Figure 5-18. Clock generation

Sigma_Delta_Modulator first_order schematic : Aug 23 17:50:52 2003

Transient Response

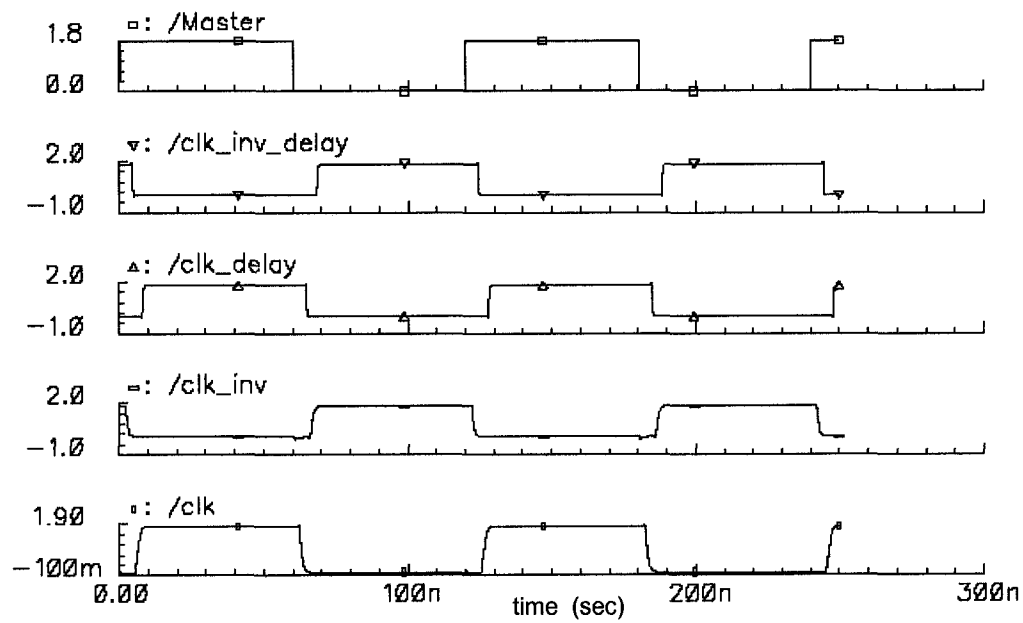


Figure 5-19. Timing diagram

Chapter 6

System Implementation

This Chapter describes the implementation of a simulated prototype second-order single-loop $\Sigma\Delta$ modulator in TSMC 0.18 μm single-poly, six-metal CMOS process with 1.8 V power supply voltage. The simulated results are presented. The discussion starts by integrating the sub-blocks to implement the second-order single-loop $\Sigma\Delta$ modulator. Layout issues are then addressed. Finally, simulated results are presented.

6.1 Modulator Schematic and Implementation

In the modified SO topology [60], the input and output common-mode voltages of the op-amps are set independently and the dc offset that exits at the output of each integrator is removed using a SC circuit. In this work the topology is further modified to save area and decrease the complexity. The DC CM voltage at

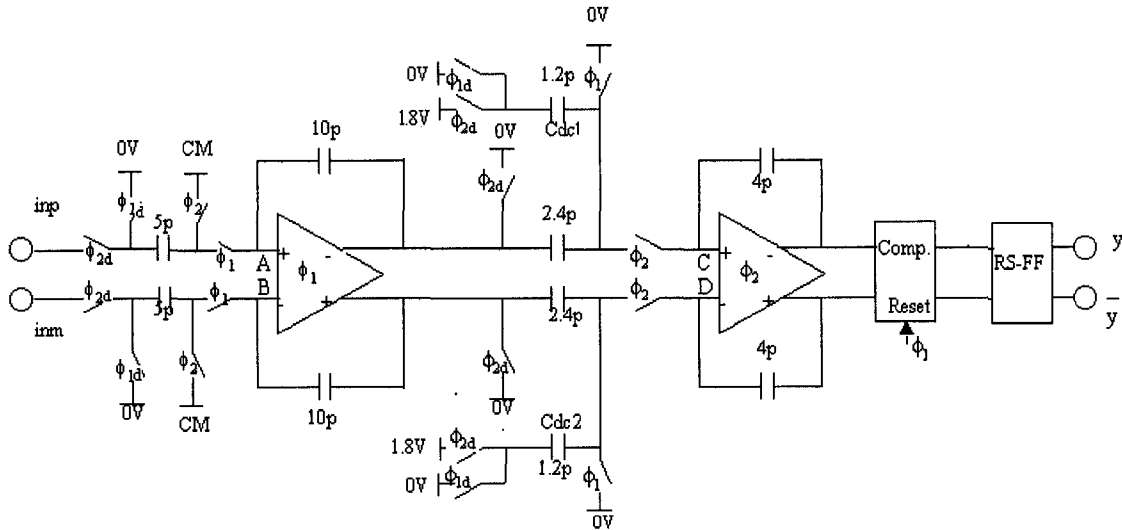


Figure 6-1. Circuit schematic of the second-order single-loop $\Sigma\Delta$ modulator

the output of the second integrator is not removed. Thus the SC circuitry after the second integrator is eliminated to save 13% of the area required for the capacitors. However,

this requires the next stage (the comparator) to withstand this DC level. Thus, the input stage of the comparator for this work is designed with N-type MOS.

The circuit schematic without the feedback network is shown in Figure 6-1. It is obtained by connecting the two SO integrators and the comparator designed in Chapter 5. The input and output common-mode voltages are set independently in this design. The dc level at the op-amp input (input common-mode voltage) is set to zero while the dc level at the op-amp output (output common-mode voltage) is set to half of the supply voltage, in this case, 900 mV. The dc offset that exists on a sample taken of the input and the op-amp output signal is to be removed. This is done in SC. For instance, the DC CM voltage of 900 mV at the output of the first integrator is removed by setting the value of C_{dc1} , C_{dc2} to be half of the second integrator's sampling capacitor. Proper operation also requires a high reference level, taken to VDD. Since two reference levels are now present, they are taken equal to the VSS and VDD. The first integrator in the system features the low voltage sampling solution. The input is sampled with reference to its CM voltage, which is 0.23 V.

The modulator is scaled according to what was discussed in Chapter 4. That is, the actual capacitor values are scaled based on white noise considerations. The sampling capacitors for the first integrator are chosen to provide a noise floor low enough for 16-bit resolution with some margins for quantization noise and other noise sources. The value of this sampling capacitor is 5 pF, while the integration capacitor is 10 pF, which implements an integrator coefficient of 0.5. The 5 pF sampling capacitor is chosen to provide a noise floor of 103 dB, which is low enough for 16-bit resolution, with some margins for the first op-amp noise and quantization noise. The sampling capacitor for the second integrator is 2.4 pF. The modulator is controlled by two non-overlapping clock phases (CLK and CLK_INV) together with delayed versions of these clock cycles.

The schematic for the differential feedback network is shown in Figure 6-2. The feedback signal is produced by using four AND gates that control the operation of the inverting and non-inverting SC feedback circuit mechanisms. Only one reference voltage is used. The reference voltage is taken to be 400 mV. The reference voltage is sampled by the inverting and non-inverting configuration under the control of the feedback output and applied to the inputs of the integrators, where A and B are the inputs of the first

integrator and C and D are the inputs of the second integrator. Figure 6-3 shows the implemented Feedback circuit for the first integrator. Figure 6-4 shows the implemented modulator.

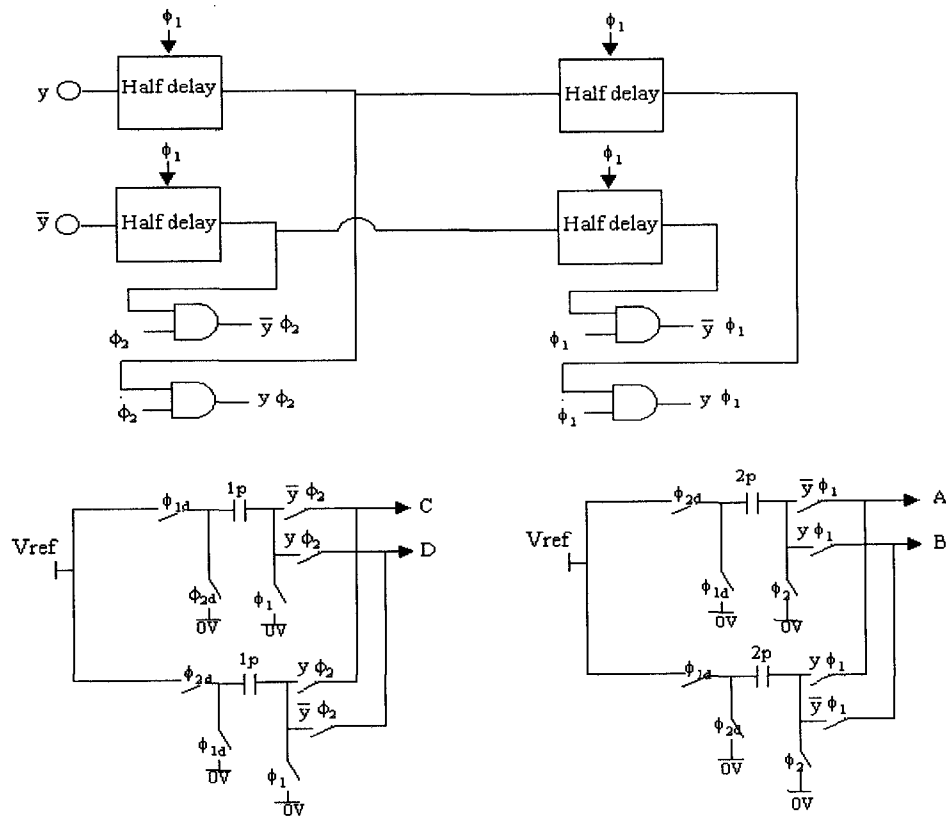


Figure 6-2. Feedback network

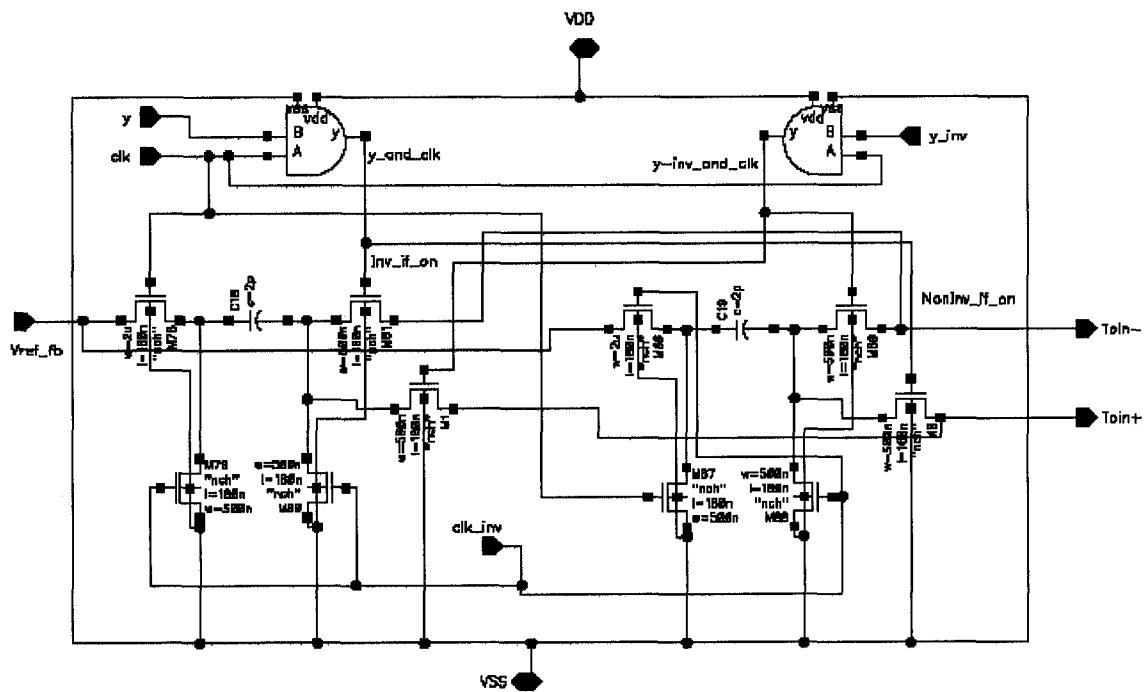


Figure 6-3. Feedback circuit implementation

6.2 Modulator Layout Methodology

The objective is to produce a design methodology to implement the design and assure the layout quality through post-simulation with parasitic. Figure 6-5 shows the different phases of the layout methodology that are followed to build the layout of this work. The successful layout of the mixed-signal design minimizes the effect of the digital switching on the analog circuits. Mixed signal layout strategies are developed throughout all phases. The strategies are implemented at the system level, down to the device level and ending at the interconnect level.

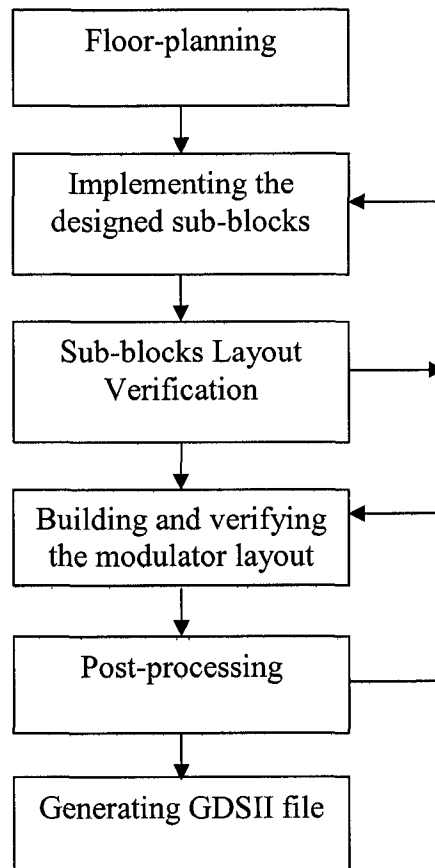


Figure 6-5. Layout methodology

6.3 Floor-planning

It involves documenting the general areas where all components and signals will go in order to minimize the area and maximize the performance. Figure 6-6 shows the activities involved in floor planning.

6.3.1 Power Supply Strategy

Whenever analog and digital circuit reside together on the same die, danger exists of injecting noise from the digital system to the sensitive analog circuitry through the power supply and ground connections. One way to reduce the interference is to prohibit the analog and digital circuit from sharing the same interconnect. The routing for the supply and ground for both the analog and digital should be provided separately to eliminate the effect of parasitic resistance. The resistance associated with the analog connection to ground or supply can be reduced by making the power supply and ground as wide as feasible. This reduces the overall resistance of the metal run, thus decreasing the voltage spikes that occur across the resistor. Separate VDD and VSS are provided in this layout for an analog and digital cells and devices.

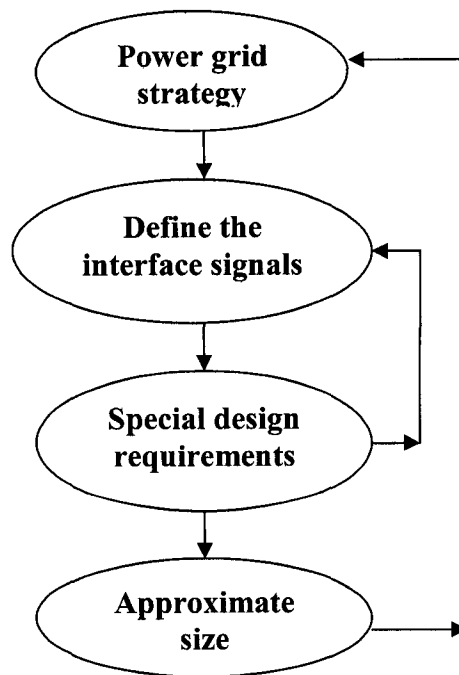


Figure 6-6. Floor-planning steps

6.3.2 *Interface Signals Definition*

In this stage, all the input and output interface signals are listed and assigned a position on the sub-blocks. Signals with special design requirements are identified.

6.3.3 *Special Design Requirements Consideration*

To minimize the effect of crosstalk, mismatch and noise in mixed signal environment, special design requirements at this system level need to be considered. Symmetry and symmetrical environment is very important in the design of the op-amp. Input signals to the first integrator should be placed as close as possible to the input pads. High-swing analog circuits such as comparators and output buffer amplifiers should be placed between the sensitive analog and the digital circuitry. Since the digital output buffers are designed to drive capacitive loads at very high rates, they should be kept farthest from the sensitive analog signal.

6.3.4 *Size Approximation*

With size constraint, there is a need to know the feasibility of meeting such constraint. Therefore size should be estimated. Size can be estimated from previous knowledge about older design of the same complexity and process design rules and from the number of transistors and the layout design rules.

6.4 Sub-block Implementation

Based on floor planning, each sub-block is implemented. Figure 6-7 shows the steps to be followed in this phase.

6.4.1 Component Placement

Sub-blocks may be redesigned if specifications are not achieved through post-simulation. The ability of the design to be completely routed is usually limited by the placement of the components. Labeling signals is advised to avoid connection errors.

6.4.2 Special Design Requirements

Different special design requirements are implemented such as fingering and increasing noise immunity. Noise immunity is increased by paying attention to the matching of the fully differential design, using guard rings and shielding the analog signals.

6.4.2.1 Matching of Fully Differential Design

The common-mode rejection inherent in the fully differential op-amps eliminates most or all of the noise from the digital circuitry coupled through the parasitic stray capacitors, if equal amount of noise are injected into the differential amplifiers. This is dependent on the symmetry of the amplifier and the matching of the transistors in the op-amp. Layout techniques should be used to improve matching. Common-centroid techniques ensure matching of transistors. Figure 6-8 shows the p-type input transistors of the op-amp implemented as common centroid. Figure 6-9 shows the op-amp layout where a complete environment matching is considered.

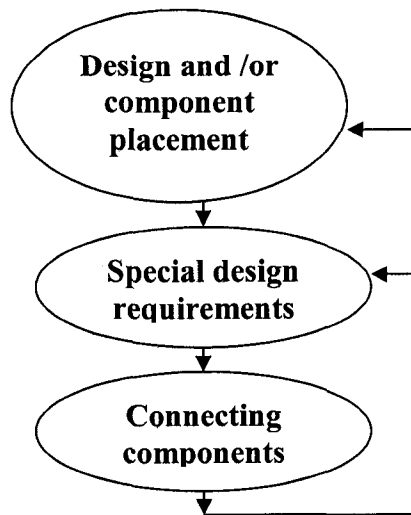


Figure 6-7. Implementing the designed sub-blocks

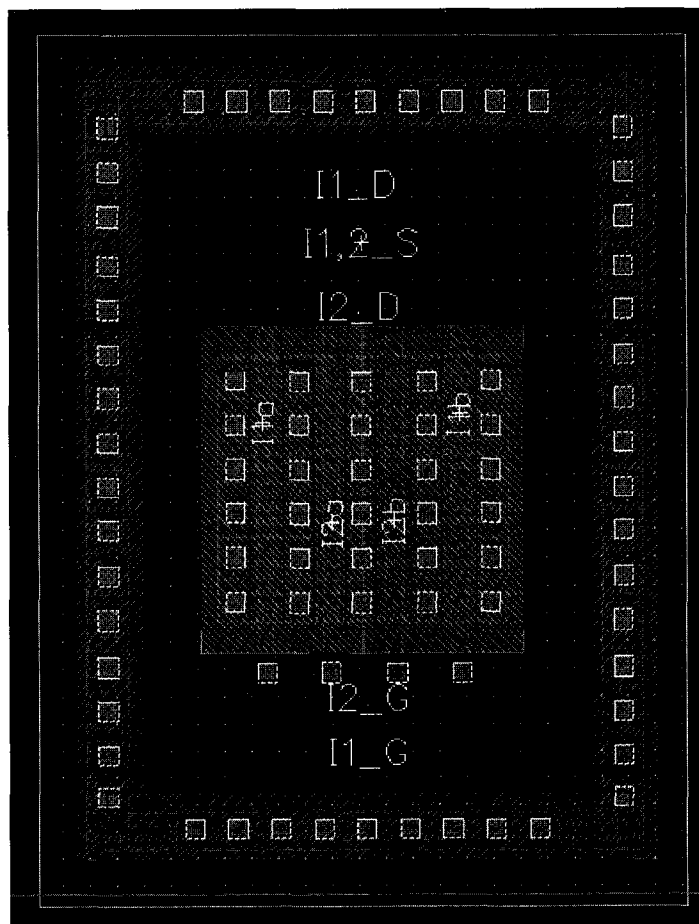


Figure 6-8. Common centroid input stage transistors

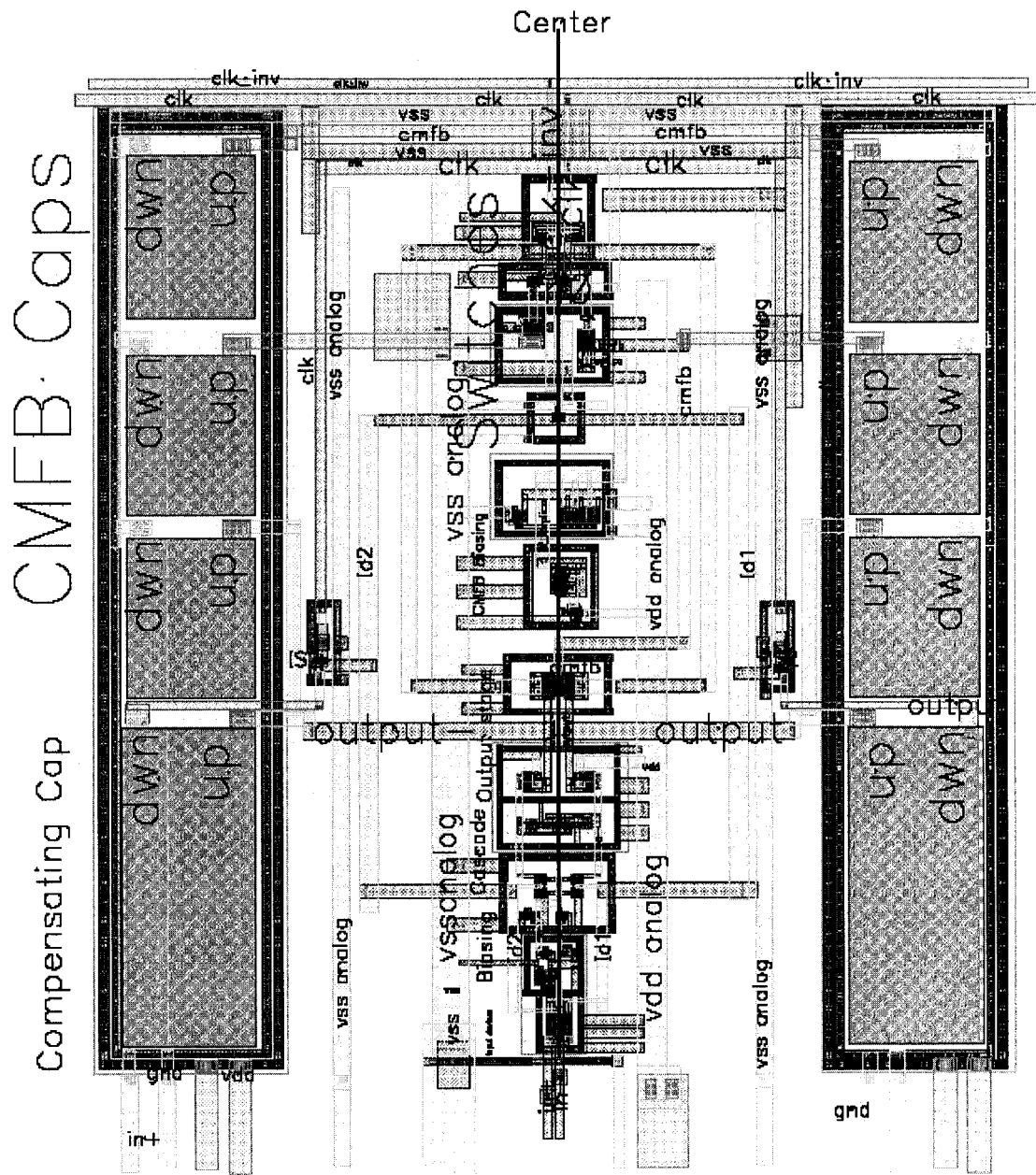


Figure 6-9. Op-amp layout

6.4.2.2 *Guard Rings*

Guard rings should be used throughout a mixed signal environment. Circuits that process sensitive signals should be placed in a separate well with guard rings attached to the analog VDD supply. The n-type devices outside the well should have guard rings attached to the analog VSS. Digital circuits should be placed in their own well with guard rings attached to the digital VDD. Guard rings placed around the n-type devices will also help to minimize the amount of noise transmitted from the digital devices.

Guard rings are used around the SCs to avoid coupled substrate noise. The capacitor is laid out over an n-well; the n-well is tied to analog VDD through an n+ implant in the n-well and metal. Surrounding the n-well is a ring of p+. This ring is tied to an analog ground. The idea is that the p+ will provide a sink for any current injection from the surrounding circuitry. Since the ground is the lowest potential in the circuit, the noise will terminate on the p+ and may not penetrate the area under the capacitor and then not coupled into the capacitor. Noise current that may still move deep under the capacitor will sweep out through VDD and not coupled into the capacitor because the n-well is held at the most positive potential in the circuit. Figure 6-10 shows the implementation.

6.4.2.3 *Shielding*

The shield implemented for this layout takes the form of a layer tied to analog ground placed between two other layers, one carrying the sensitive analog signal and the other carrying the digital signal. It is the case when such crossing is unavoidable. Figure 6-11 shows an example, where the sensitive analog signals exist on metal 2; the crossing digital clocks are carried by metal 3, while a grounded metal 3 is used as a shield. This shield is used for isolation providing a termination plane for the electric fields resulting from the voltages on both the digital and analog signals.

It should be avoided to run interconnects carrying sensitive analog signals parallel and adjacent to any interconnect carrying digital signals. If this situation cannot be avoided, then an additional line connected to analog ground should be placed between the two signals.

6.4.2.4 Capacitor Layout

This application requires linear and high precision capacitors, thus metal capacitors are needed. A multi-metal sandwich of conductive layers can be formed in CMOS technology. The 0.18 μm CMOS technology offers six metal layers, thus five capacitors can be formed on the same area. Capacitors in the modulator are implemented using the sandwich structure. Metal 1, metal 3 and metal 5 form the negative plate of the capacitor, while metal 2 and metal 4 make the positive plate of the capacitor.

6.4.2.5 Multi-Finger Transistors

Wide transistors need to be folded so as to reduce the source-drain junction area and the gate resistance. Figure 6-12 shows an example.

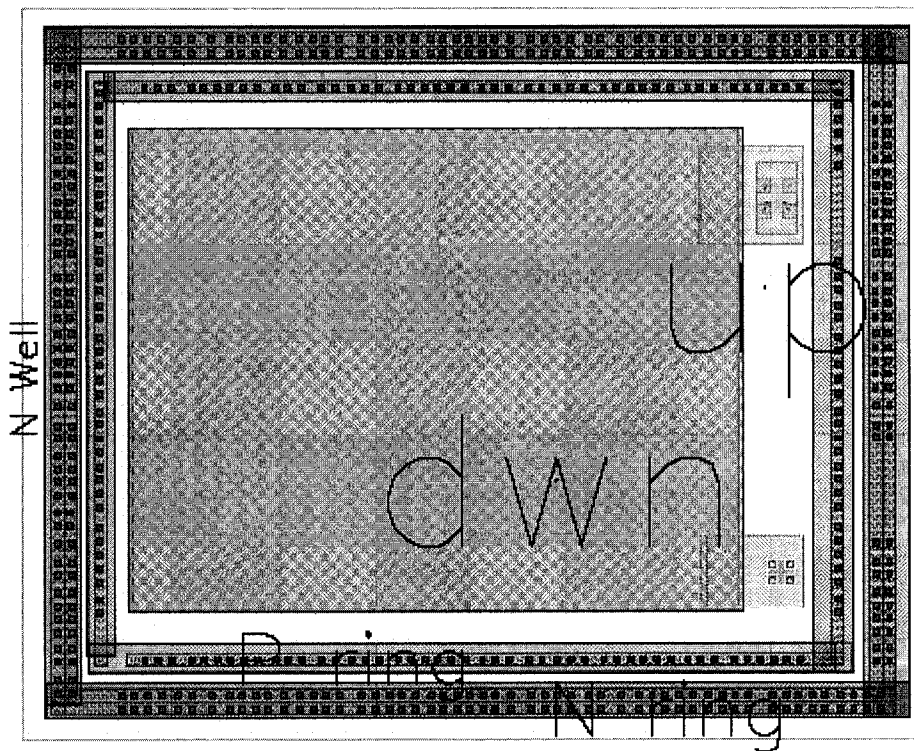


Figure 6-10. Capacitor layout with guard rings

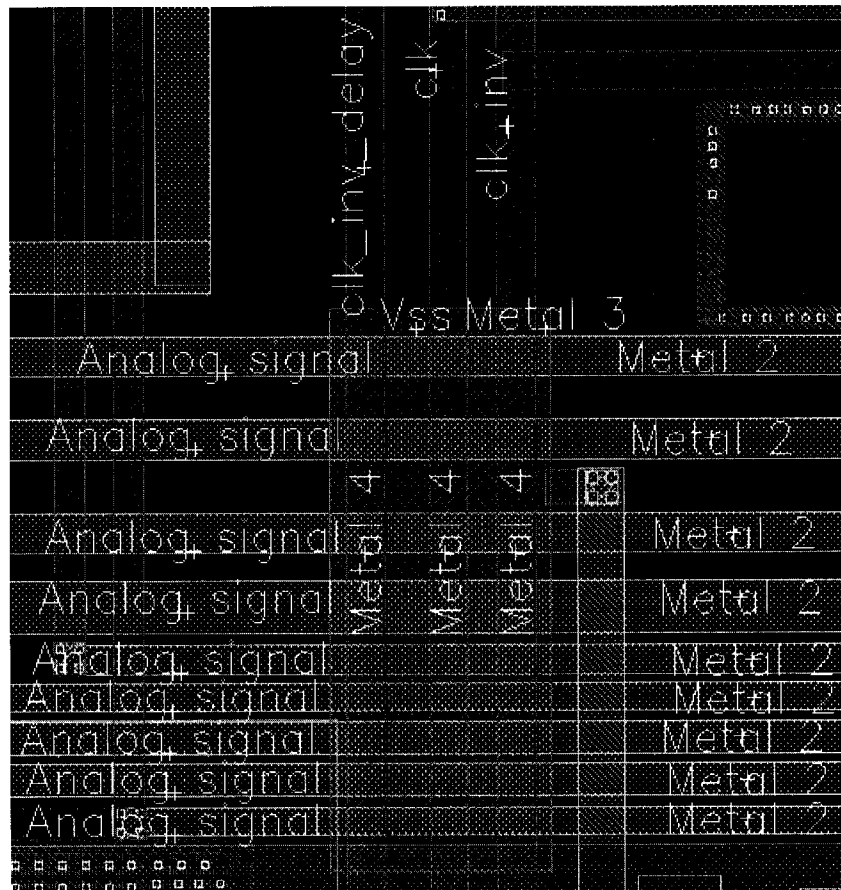


Figure 6-11 Shielding the sensitive analog signals

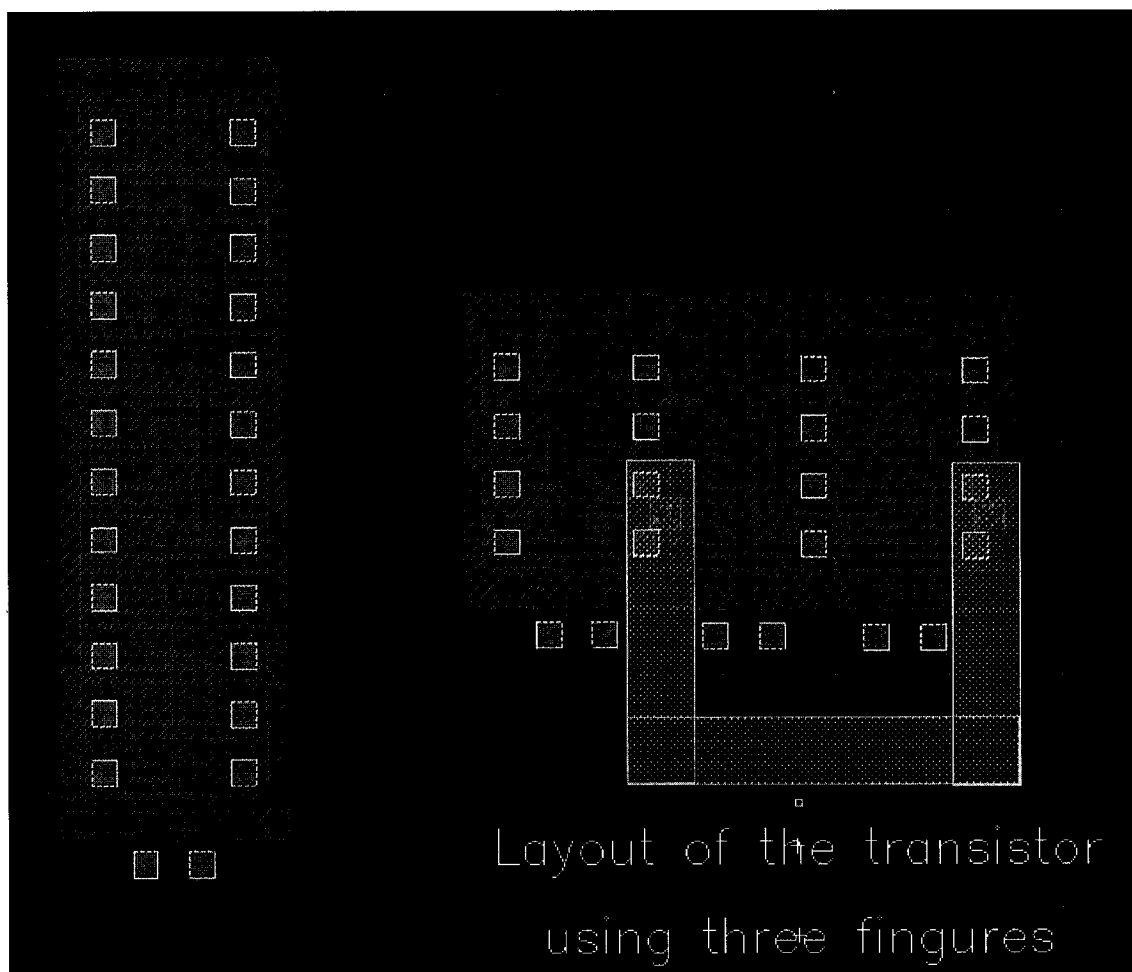


Figure 6-12. Multi-fingering

6.4.3 Component Connection

With good floor planning and placement of components, this step becomes easy. Otherwise, completing interconnect routing while respecting special design requirements is usually difficult and time consuming. When routing the analog circuitry, the lengths of the current carrying paths need to be minimized. This will reduce the amount of voltage drop across the path due to parasitic resistance. Minimizing the routing of the signals within the design is also important to reduce the input capacitance for signal. Contacts should also be used very liberally whenever changing layers to improve the fabrication reliability. Using the minimum design rule line may width as routing width may not be practical, because connection points may require via or contacts, and the space required for vias or contacts is generally wider than the minimum width rule for routing. For the digital part, consistent routing direction with specific metal layers should be maintained to assure that the layout is routable. However for an analog part, the use of minimum number of metal layers is better to increase the noise immunity. Labeling all the important signals simplifies error diagnosing in the layout versus schematic activity.

6.4.4 Sub-Block Layout Verification

Figure 6-13 shows verification steps that should be done for each sub-block. Design rule check (DRC) step verifies that all polygons and layers of the layout meet the 0.18 μm CMC process, such as width and space rules. Netlist is generated through the extraction step that is compatible for simulation. Once the layout versus schematic (LVS) is succeeded then it is assured that electrical connectivity, device sizes and nets are correct. The layout is then extracted with parasitic and post-simulation is performed to ensure that each sub-block is functioning as expected and that the specifications meet the requirements. Figure 6-14, 6-15, 6-16, 6-17 and 6.18 show the layout for the comparator, clock generation, half-delay, and the set-reset FF respectively.

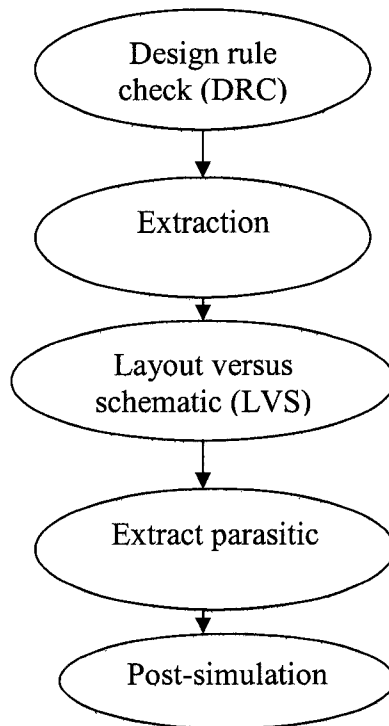


Figure 6-13. Building block layout verification steps

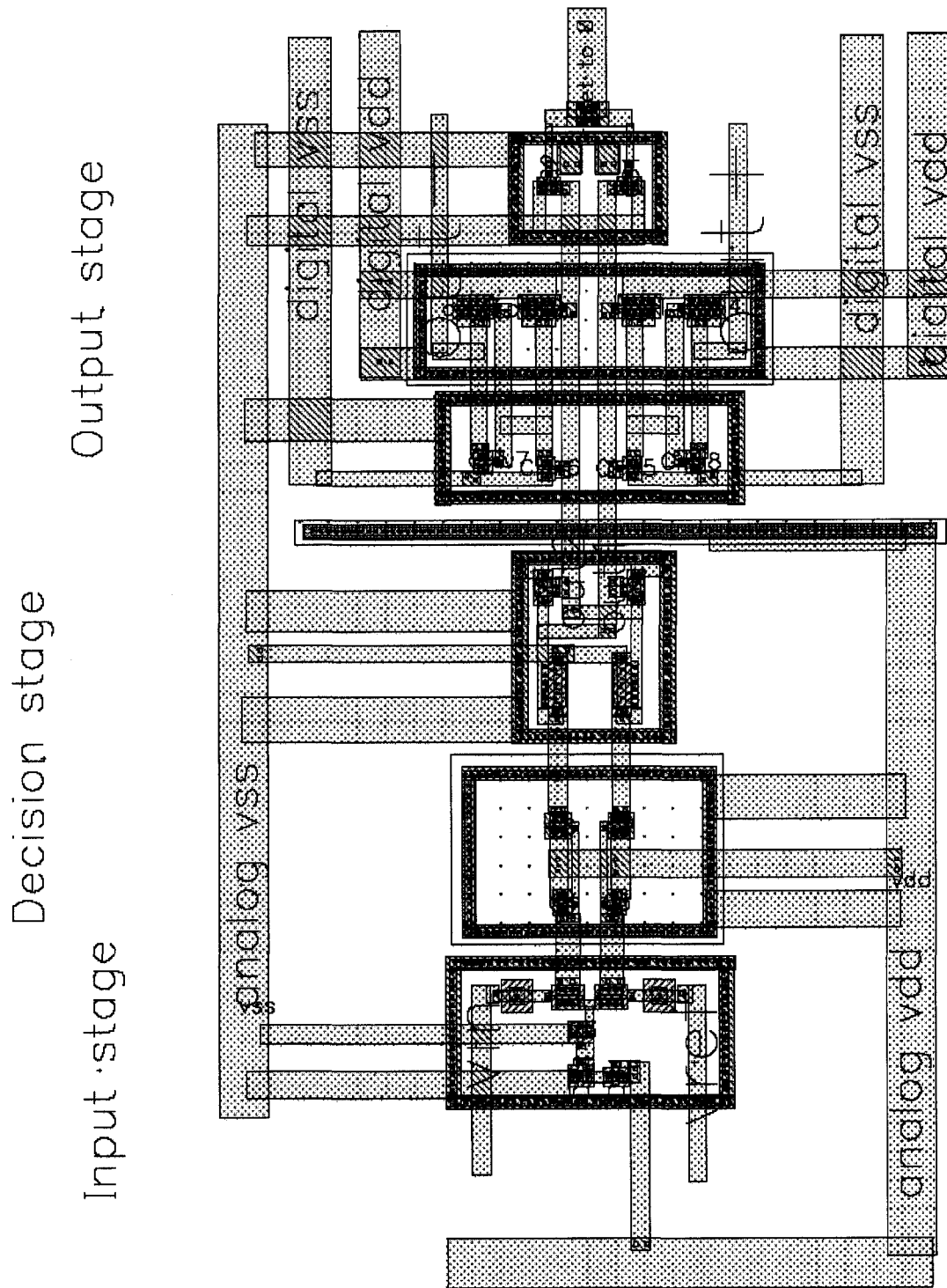


Figure 6-14. Comparator layout

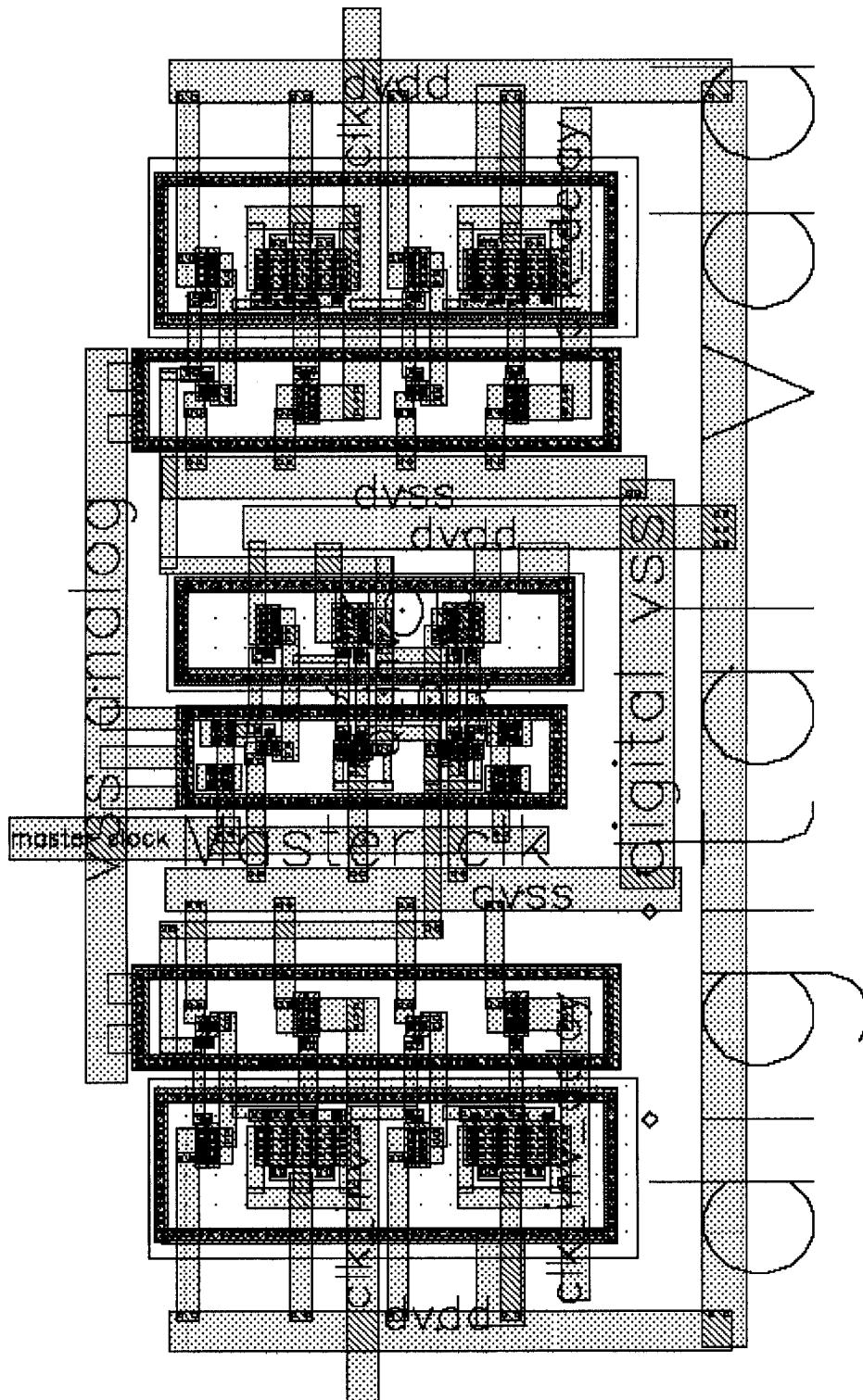


Figure 6-15. Clock generation layout

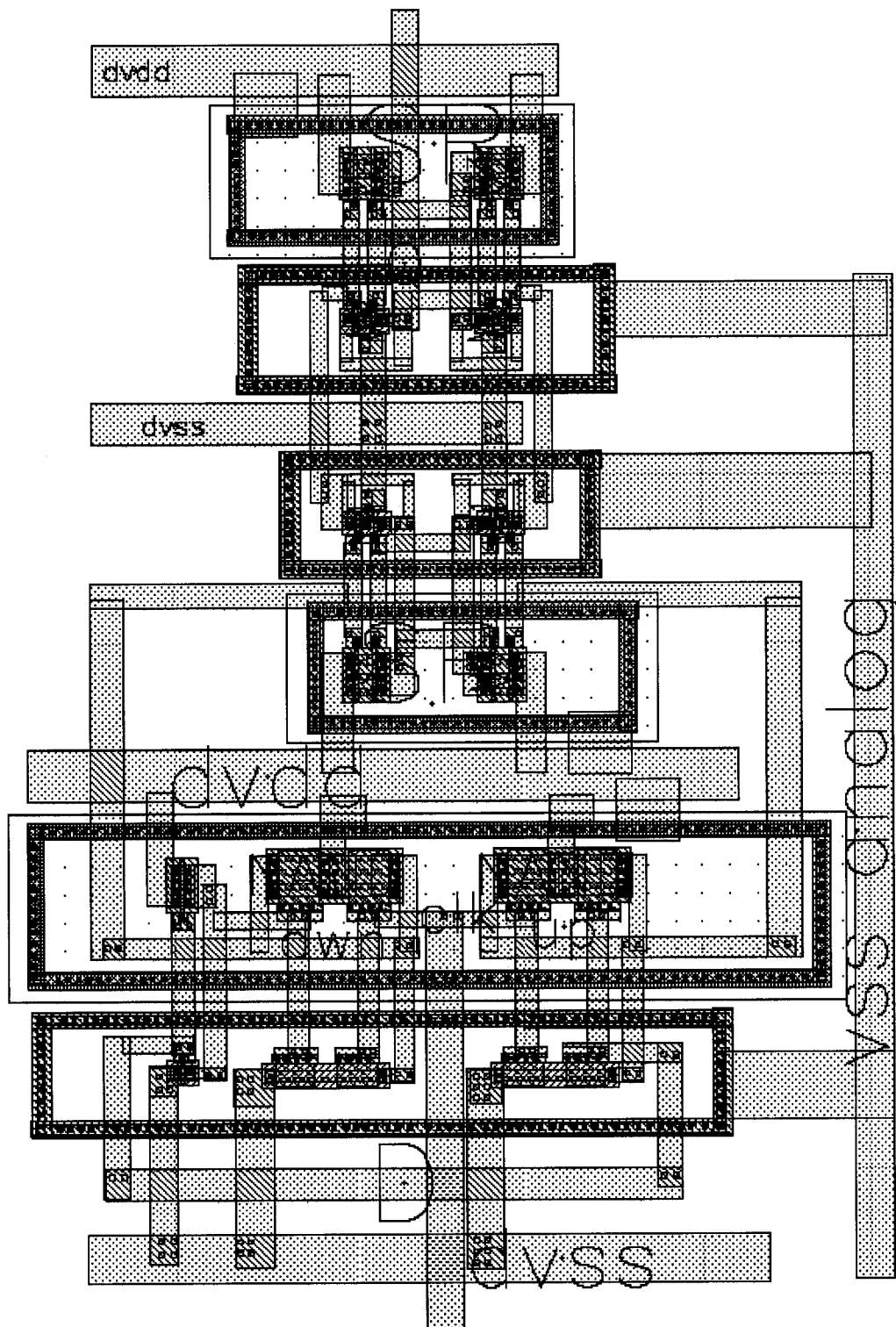


Figure 6-16. Half-delay circuit layout

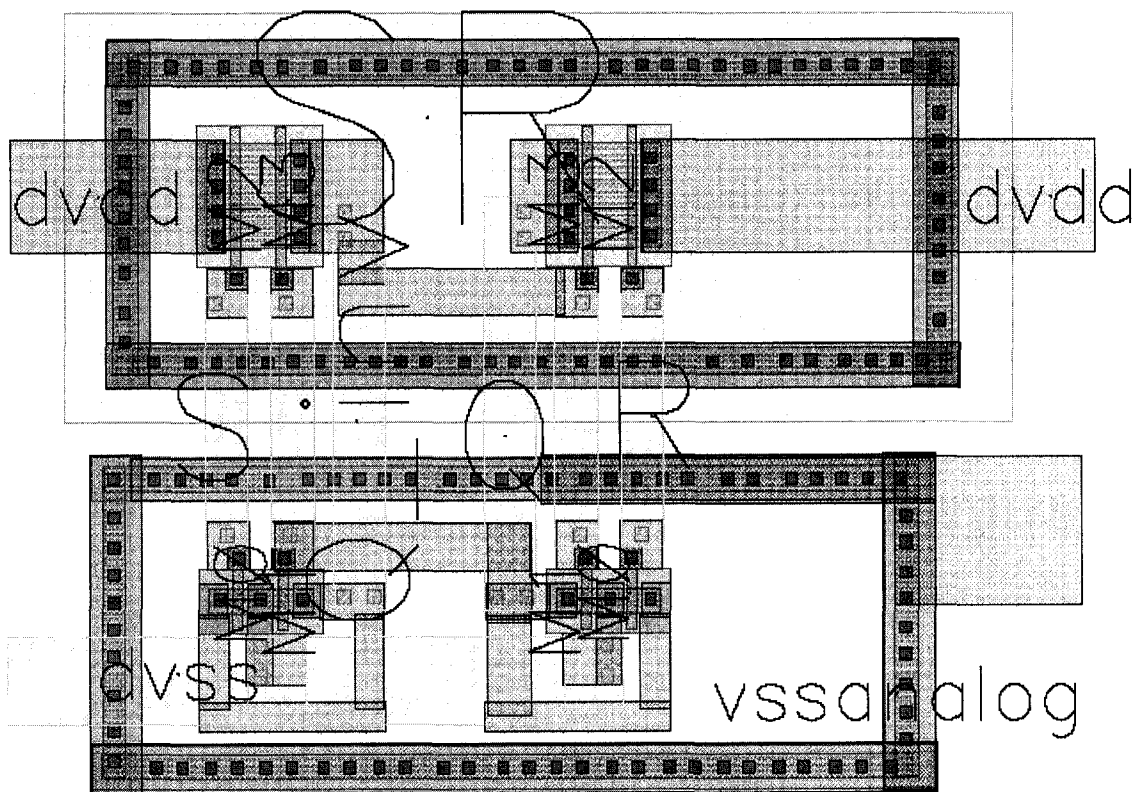


Figure 6-17. Set-reset flip-flop layout

6.5 Building and Verifying the Modulator Layout

All sub-blocks are integrated based on floor planning. The modulator is verified through DRC, LVS and post-simulation with parasitic extraction. Figure 6-18 shows the layout of the modulator chip. The chip dimension is 995.6 μm X 985.6 μm . The die area is 650 μm X 620 μm .

6.6 Post Processing

Figure 6-19 shows the generated bitstream of the extracted modulator with parasitic. The input applied is a differential sin wave of amplitude of 125 mV and frequency of 16 KHz.

The output bitstream for a differential sinusoidal input of 5 KHz for 8195 samples is then post-processed in MATLAB to calculate the SNDR. To calculate the dynamic-range (DR), the SNR is calculated while changing the amplitude for the applied input sinusoid. Figure 6-20 shows the achieved SNDR of 98 dB and Figure 6-21 shows the DR of 100 dB. The post-simulation verifies that results meet the requirements.

The simulated modulator performance is summarized in table 6.1, which demonstrates the success of the design methodology. A figure-of-merit (FOM) based on joule/conversion was computed to compare this work with other designs. The proposed $\Sigma\Delta$ Modulator has the best FOM moreover; the area is also the minimum as shown in Table 6.2

6.7 Generating the GDSII file

The GDSII file is generated and the chip is sent for fabrications

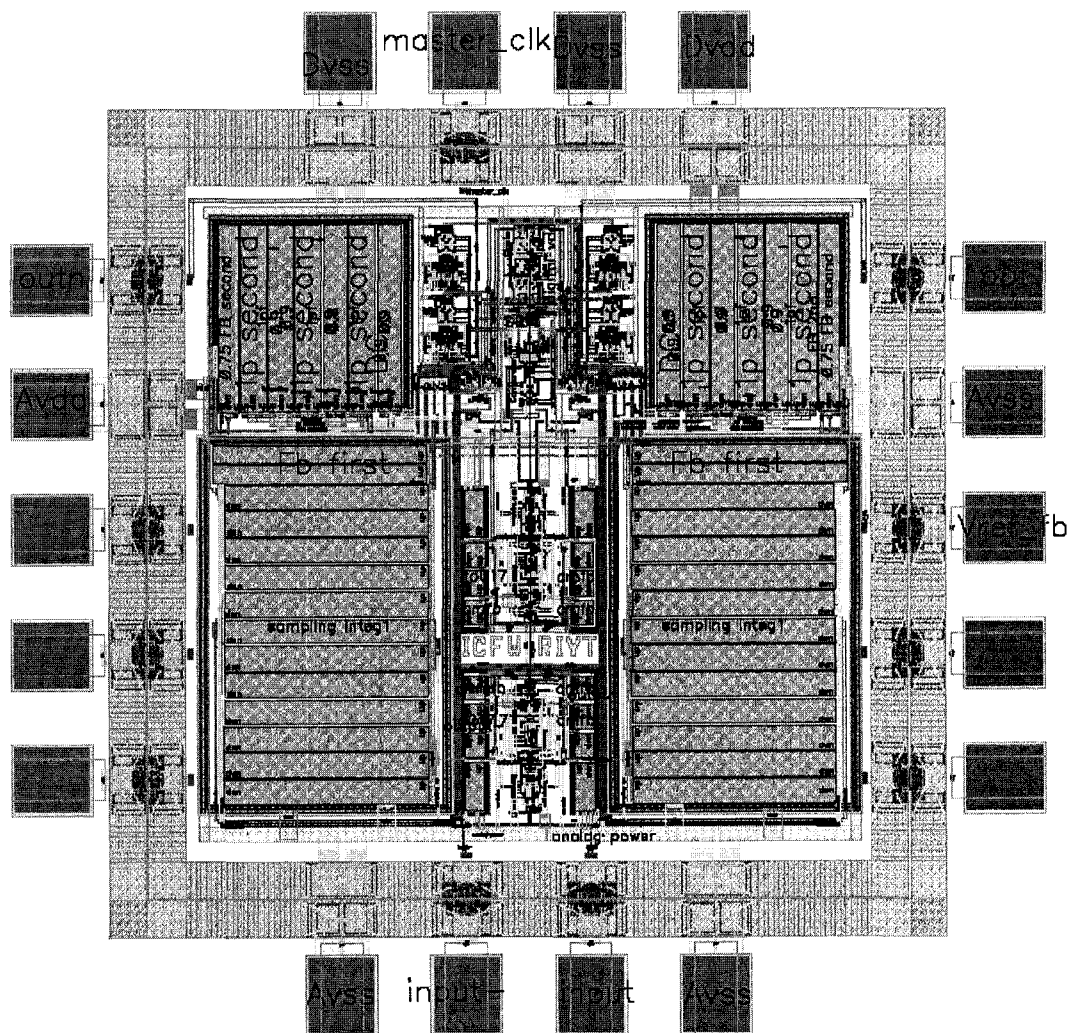


Figure 6-18. The implemented $\Sigma\Delta$ modulator

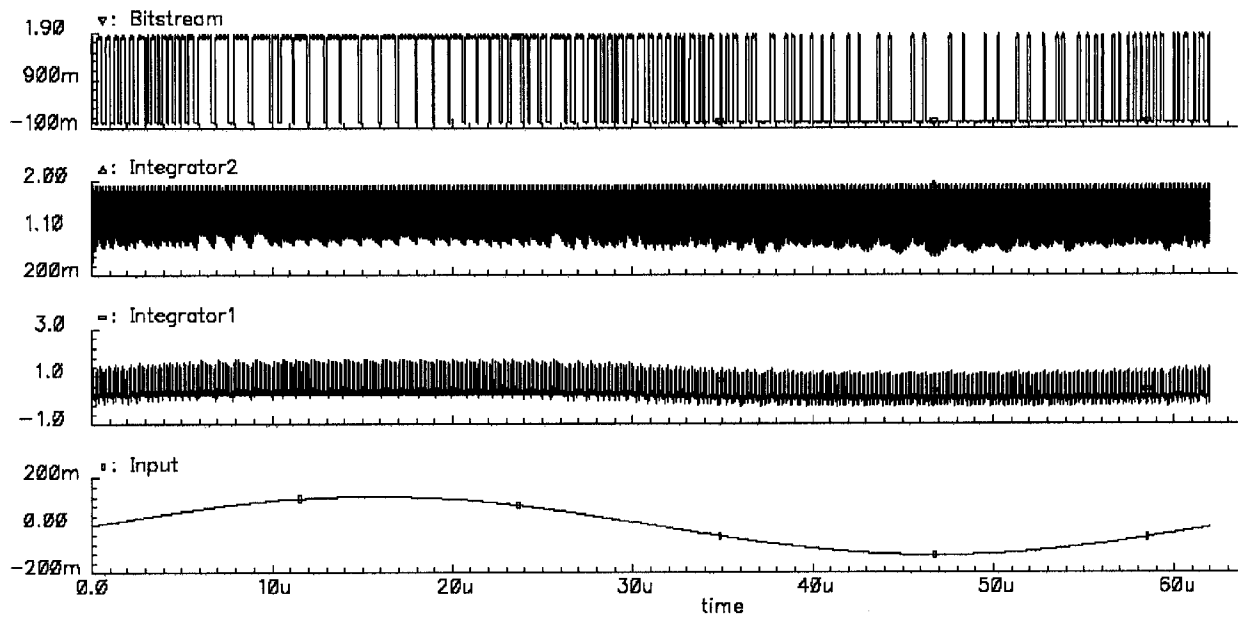


Figure 6-19. The generated bitstream

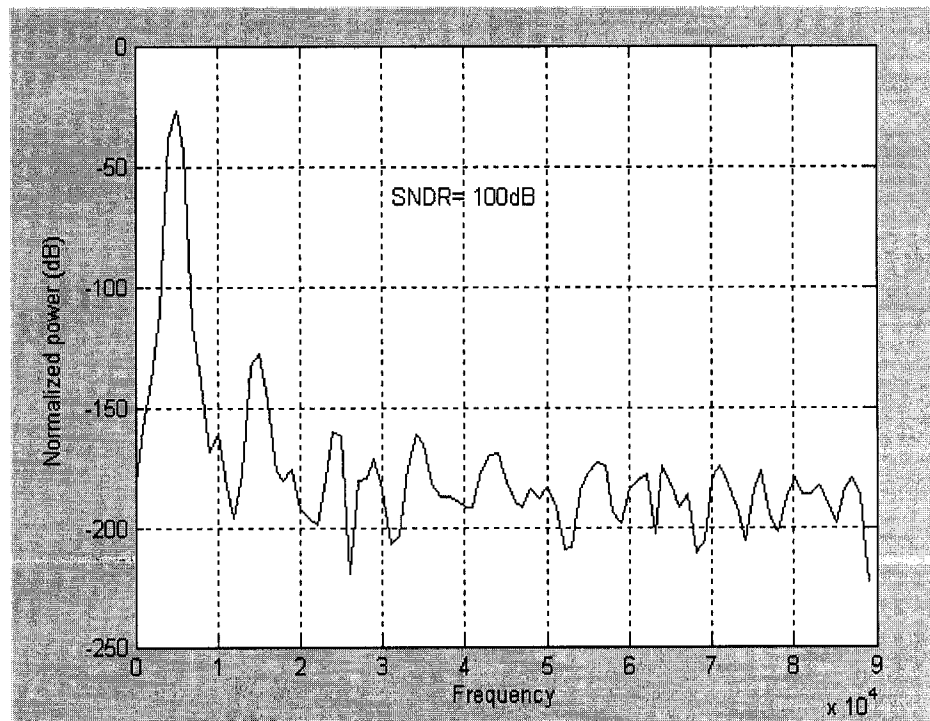


Figure 6-20. The output spectrum

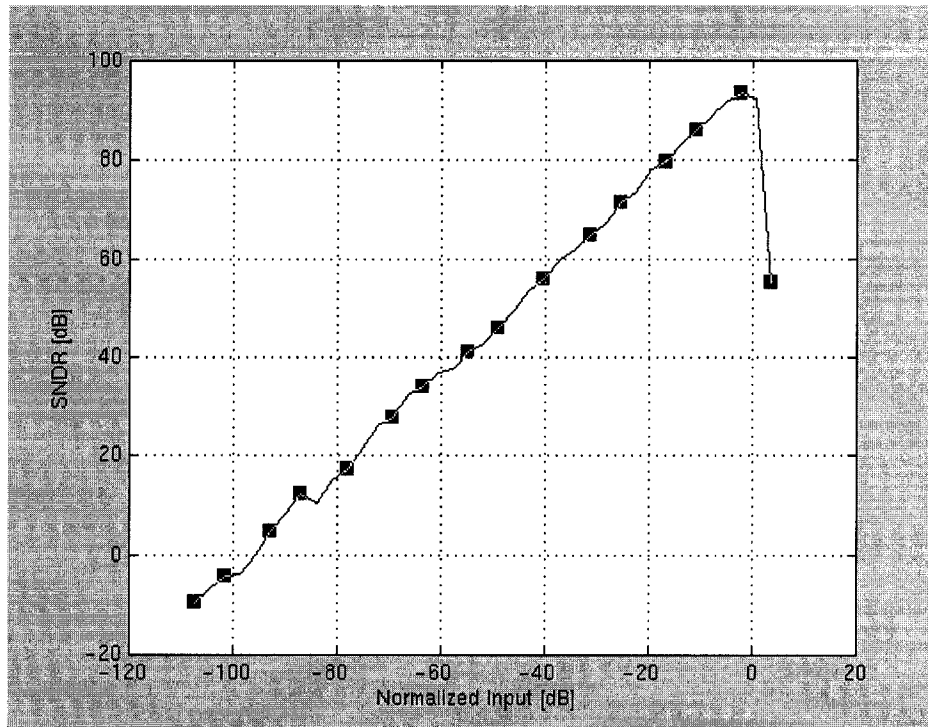


Figure 6-21. SNDR versus signal amplitude

Table 6-1 Modulator specifications

Sampling rate	8.2 MHz
OSR	256
BW	16 KHz
Supply voltage	1.8 V
SNDR	98 dB
DR	100 dB
Die Area	0.403 mm ²
Power consumption	1321 μ W
Process	0.18 μ m TSMC

Table 6-2 Comparison between this work and previous designs

Ref.	Type	VDD	DR [dB]	BW [KHz]	Power [μ W]	Area [mm ²]	Sampling Rate [MHz]	Figure of merit Joule/second [10 ⁻¹²]
This work	SO	1.8	100	16	1321	0.403	8.2	161
[50]	SC	1	88	25	950	0.63	5	190
[28]	SC	1.8	99	25	2500	1.5	4	625
[29]	SC	1.8	102	25	2350	1.426	3.2	734
[51]	SC	5	104	25	47000	5.2	6.4	7344
[27]	SC	5	111	22	520000	25.8	5.632	92329

Chapter 7

Conclusions and Recommended Future Work

7.1 Conclusions

A 1.8V modulator for an audio hearing-aid application has been designed using a SO technique and a 0.18 μm digital CMOS process. The single-loop, second-order topology proposed in this work saves approximately 70% of the required area in [29]. The use of a SO based $\Sigma\Delta$ modulator allows the design to be readily scaled to the latest CMOS technologies. In the proposed circuit one DC offset switching capacitor circuit was eliminated and this reduced the required area for the capacitors by 13%. The overall complexity of the $\Sigma\Delta$ modulator was simplified to increase the robustness of the low-voltage low-power design. Simulation results indicated a SNDR of 98 dB and DR of 100 dB with a 16 kHz signal bandwidth, as required for this hearing-aid application. A figure-of-merit based on joule/conversion was computed to compare this work with other designs. The proposed $\Sigma\Delta$ modulator has the best figure-of-merit and the minimum area when compared to the existing state-of-the-art designs. The modulator circuit features reduced complexity, area reduction and low conversion energy. It is the only modulator designed based on a SO technique that is compatible with the continuously decreasing feature sizes associated with the latest CMOS technology. A research paper based on this work has been accepted for publication in the proceedings of the Fourth International Workshop on System-on-Chip (IWSOC'2004), Banff, Alberta, July, 2004.

7.2 Recommended Future Work

The results presented and values used to determine specifications and evaluate performance metrics are based on simulation results only. The $\Sigma\Delta$ modulator was submitted for fabrication to the Canadian Microelectronics Corporation (CMC) and the layout passed all the design-rule-checks (DRC). The delivery of the fabricated chip was delayed due to packaging problem and this has prevented the author from testing the physical implementation of the chip. It is hoped that the author will be able to test the

chip in the future at her new place of employment. In any event, an outline for testing methodology that will verify specifications and support the evaluation of performance metrics has been developed and left with the author's research supervisor.

This research has dealt with the design of a $\Sigma\Delta$ modulator for use in an ADC. In order to complete the design for the $\Sigma\Delta$ ADC the associated decimation filter needs to be developed. Since the designed $\Sigma\Delta$ modulator as it is based on SO, the same topology and design methodology can be applied to implement the design in the newest technology, such as 0.09 μm CMOS technology. An $\Sigma\Delta$ ADC could also be developed in the form of an intellectual property (IP) core for use in a system-on-chip (SOC) implementation.

Appendix A

MATLAB functions

A.1 Slew Rate Modeling

```
function out = slew(in,alfa,sr,GBW,Ts)
% Models the op-amp slew rate for a discrete time integrator
% in: input signal amplitude
% alfa: effect of finite gain (ideal op-amp alfa=1)
% sr: slew rate in V/s
% GBW: gain-bandwidth product of the integrator in Hz
% Ts: sample time
% out: output signal amplitude
tau=1/(2*pi*GBW); % Time constant of the integrator
Tmax = Ts/2;
slope=alfa*abs(in)/tau;
if slope > sr % Op-amp in slewing
    tsl = abs(in)*alfa/sr - tau; % Slewing time
    if tsl >= Tmax
        error = abs(in) - sr*Tmax;
    else
        texp = Tmax - tsl;
        error = abs(in)*(1-alfa) + (alfa*abs(in) - sr*tsl) * exp(-texp/tau);
    end
else % Op-amp in linear region
    texp = Tmax;
    error = abs(in)*(1-alfa) + alfa*abs(in) * exp(-texp/tau);
end
out = in - sign(in)*error;
```

A.2 PSD Plotting

```
*****

% 2nd Order Sigma-Delta A/D Modulator
% The modulator structure is simulated using SIMULINK
% Post-processing of the results is done with Matlab.
% 1. Plots the Power Spectral Density of the bit-stream
% 2. Calculates the SNR
*****

clear;
t0=clock;
*****

% Global Variables
*****

bw=16.05e3;           % Base-band
R=256;
Fs=R*2*bw;           % Sampling Rate
Ts=1/Fs;
N=R*R;               % Samples number
nper=12;
Fin=nper*Fs/N;       % Input signal frequency (Fin = nper*Fs/N)
Ampl=0.23;           % Input signal amplitude [V]
Ntransient=0;
*****

% kT/C noise and op-amp non-idealities
*****

echo on;
k=1.38e-23;          % Boltzmann Constant
Temp=300;            % Absolute Temperature in Kelvin
Cf=10e-12;           % Integrating Capacitance of the first integrator
alfa=(1e3-1)/1e3;    % A=Op-amp finite gain
Amax=0.8;            % Op-amp saturation value [V]
sr=10e6;             % Op-amp slew rate [V/s]
GBW=45e6;            % Op-amp GBW [Hz]
noise1=8e-6;         % 1st int. output noise std. dev. [V/sqrt(Hz)]
delta=4e-9;          % Random Sampling jitter (std. dev.)
echo off;
*****

% Modulator Coefficients
*****

echo on;
a1=0.5;
a2=0.6;
b1=0.2;
b2= 0.25;
Vref=0.9;
```

```

finrad=Fin*2*pi;                                % Input signal frequency in radians
*****

% Open Simulink diagram first
*****

options=simset('InitialState', zeros(1,2), 'RelTol', 1e-3, 'MaxStep', 1/Fs);
sim('second', (N+Ntransient)/Fs, options); % Starts Simulink simulation
*****

% Calculates SNR and PSD of the bit-stream and of the signal
*****

w=hann(N);
echo on;
f=Fin/Fs;                                % Normalized signal frequency
fB=N*(bw/Fs);                            % Base-band frequency bins
yy1=zeros(1,N);
yy1=yout(2+Ntransient:1+N+Ntransient)';
echo off;
ptot=zeros(1,N);
[snr,ptot]=calcSNR(yy1(1:N),f,fB,w,N,Vref);
Rbit=(snr-1.76)/6.02; % Equivalent resolution in bits
*****

% Output Graphs
*****

figure(1);
clf;
plot(linspace(0,Fs/2,N/2), ptot(1:N/2), 'r');
grid on;
title('PSD of a 2nd-Order Sigma-Delta Modulator')
xlabel('Frequency [Hz]')
ylabel('PSD [dB]')
axis([0 Fs/2 -200 0]);

figure(2);
clf;
semilogx(linspace(0,Fs/2,N/2), ptot(1:N/2), 'r');
grid on;
title('PSD of a 2nd-Order Sigma-Delta Modulator')
xlabel('Frequency [Hz]')
ylabel('PSD [dB]')
axis([0 Fs/2 -200 0]);

figure(3);
clf;
plot(linspace(0,Fs/2,N/2), ptot(1:N/2), 'r');
hold on;
title('PSD of a 2nd-Order Sigma-Delta Modulator (detail)')
xlabel('Frequency [Hz]')

```

```

ylabel('PSD [dB]')
axis([0 2*(Fs/R) -200 0]);
grid on;
hold off;
text_handle = text(floor(Fs/R),-40, sprintf('SNR = %4.1f dB @ OSR=%d\n',snr,R));
text_handle = text(floor(Fs/R),-60, sprintf('Rbit = %2.2f bits @ OSR=%d\n',Rbit,R));

s1=sprintf(' SNR(dB)=%1.3f',snr);
s2=sprintf(' Simulation time =%1.3f min',etime(clock,t0)/60);
disp(s1)
disp(s2)

```

A.3 SNR Calculation

```

function
[snrdB,ptotdB,psigdB,pnoisedB,input_extracted,norm_input_extracted,stot,ssignal,snoise
,input] = calcSNR(vout,f,fB,w,N,Vref)
% vout: Sigma-Delta bit-stream taken at the modulator output
% f: Normalized signal frequency (fs -> 1)
% fB: Base-band frequency bins
% w: windowing vector
% N: samples number
% Vref: feedback reference voltage
% snrdB: SNR in dB
% ptotdB: Bit-stream power spectral density (vector)
% psigdB: Extracted signal power spectral density (vector)
% pnoisedB: Noise power spectral density (vector)
fB=ceil(fB);
input_extracted=sinusx(vout(1:N).*w,f,N)
x(n)*Wn()
norm_input_extracted=(N/sum(w))*sinusx(vout(1:N).*w,f,N);
signal=norm_input_extracted;
noise=vout(1:N)-signal; % Extracts noise components
input= vout(1:N).*w;
stot=((abs(fft((vout(1:N).*w))))).^2); % Bit-stream PSD
ssignal=(abs(fft((signal(1:N).*w))))).^2; % Signal PSD
snoise=(abs(fft((noise(1:N).*w))))).^2; % Noise PSD
pwsignal=sum(ssignal(1:fB)); % Signal power
pwnoise=sum(snoise(1:fB)); % Noise power
snr=pwsignal/pwnoise;
snrdB=dbp(snr);
norm=sum(stot)/Vref^2; % Normalization
%if nargout > 1
ptot=stot/norm;
ptotdB=dbp(ptot);
%end

```

```

%if nargout > 2
    psig=ssignal/norm;
    psigdB=dbp(psig);
%end

%if nargout > 3
    pnoise=snoise/norm;
    pnoisedB=dbp(pnoise);
%end

```

A.3.1 Extraction of a Sinusoidal Waveform from a Bitstream

```

function outx = sinusx(in,f,n)
% extract a sin wave from a bitstream using hartely transform
sinx=sin(2*pi*f*[1:n]);
cosx=cos(2*pi*f*[1:n]);
in=in(1:n);
a1=2*sinx.*in;           % for hartley transform
a=sum(a1)/n;             % for the inverse hartley transform
b1=2*cosx.*in;
b=sum(b1)/n;
outx=a.*sinx + b.*cosx;  % the completed inverse hartley transform

```

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