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Low power CMOS analog multipliers.

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Low Power CMOS Analog Multipliers

by

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ABSTRACT

CMOS analog multiplier is a very important building block and programming element in analog signal processing. Although high-performance multipliers using bipolar transistors have been available for 40 years, CMOS multiplier implementation is still a challenging subject especially for low-power and low-noise circuit design.

Since the supply voltage is normally fixed for analog multiplier structures, we use the total current to represent the power dissipation. Our basic idea for low power design of analog multipliers is to fit most of the transistors into the linear region, while at the same time keeping the drain-to-source voltage as low as possible to decease the drain current. And also, we use PMOS transistors for the devices working in the saturation region to further decrease the drain current and improve the linearity performance.

Two low power CMOS analog multiplier designs have been proposed in this thesis. We gave detailed performance analysis and some design considerations for these structures. Cadence Hspice simulation verified our analysis.

To ensure a fair comparison, we also simulated the performance of a previous multiplier structure, which was considered to be one of the best multiplier structures with low power and low noise performance. Extensive experiments and comparison for these structures show that the proposed CMOS analog multipliers have much less power dissipation than that of previous structures, while at the same time, satisfying other performance requirements.

The proposed analog multipliers would be good choices in the applications where low power dissipation is an important consideration.

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CHAPTER 1

INTRODUCTION TO ANALOG INTERGRATED CIRCUIT DESIGN

With the development of VLSI (very large scale integration) technology, digital signal processing is proliferating and penetrating into more and more applications. Many applications that have been traditionally implemented in analog domain have been moved to digital field. However, as we will see later, even though digital signal processing techniques have been introduced in more applications, analog circuits are still required.

Actually analog circuit designers are still in strong demand today. Even though many signal processing functions have been implemented in digital, some functions can not be replaced by digital signal processing, such as analog-to-digital and digital-to-analog conversion, anti-alias and reconstruction filtering and so on. These functions are fundamentally required to implement in analog domain, independent of technology improvement.

1.1 Why is Analog Signal Processing Required?

While many types of signal processing have indeed moved to the digital domain, analog circuits have proved fundamentally necessary in many of today's complex, high-performance systems. Let's consider a few applications where it is very difficult or even impossible to replace analog functions with their digital counterparts regardless of advantages in technology [52].

Processing of Natural Signals: Naturally occurring signals are analog-at least at a

macroscopic level. Since all of these signals must eventually undergo extensive processing in the digital domain, we observe that these systems consist of an analog-to-digital converter (ADC) and a digital signal processor (DSP). The design of ADCs for high speed, high precision, and low power dissipation is one of the difficult challenges in analog design.

Digital Communication: When binary data generated by various systems, this signal must often be transmitted over long distances. Therefore, the signal would experience some attenuation or distortion. We need multi-level receiver to improve the quality of communication. Utilized extensively in today's communication systems, multi-level signal necessitates a digital-to-analog converter (DAC) in the transmitter to produce the multi-levels and an ADC in the receiver to determine which level has been transmitted.

Disk Drive Electronics: When the data stored in the hard disk is read by a magnetic head, the noise content is quite high, and the bits experience substantial distortion. Therefore, the analog filter and amplifier are needed to remove the distortion. The design of these building blocks poses great challenges as the speed of computers and their storage media continues increase every year.

Wireless Receivers: The signal picked up by the antenna of a radio-frequency (RF) receiver exhibits small amplitude and the signal is accompanied by large interferes. Some analog circuit is needed to amplify the low-level signal with minimal noise and withstand large unwanted components.

Optical Receivers: For high-speed data transmission, optical receivers are needed, where the data is converted to light and transmitted over an optical fiber. The receiver must process low-level signal at very high speed, requiring low-noise, broadband analog

circuit design.

Microprocessors and Memories: Today's microprocessors and memories draw upon a great deal of analog design expertise.

Basically, we need analog-to-digital converters (ADC) to digitize the input signal, and digital-to-analog converters (DAC) to reproduce the analog signal after digital signal processing. And also, analog pre-processing (before the ADC) and post-pressing (after the DAC) are needed, such as amplification, filtering and equalization.

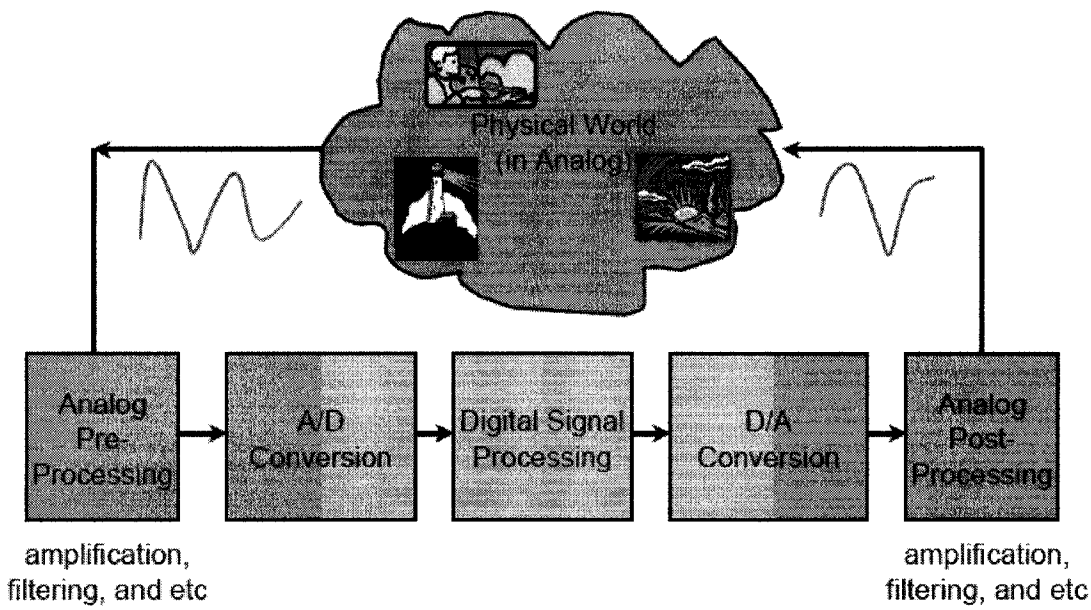


Fig. 1.1 ADCs, DACs, and pr-/post- processing analog circuits are required to interface the DSP core and the physical world

1.2 The Difference of Digital Circuits and Analog Circuits

Table 1.1 The difference of digital circuits and analog circuits

Analog Circuits	Digital Circuits
Signals are continuous in amplitude and can be continuous or discrete in time	Signal are discontinuous in amplitude and time - binary signals have two amplitude states
Designed at the circuit level	Designed at the systems level
Components must have a continuum of values	Component have fixed values
Customized	Standard
CAD tools are difficult to apply	CAD tools have been extremely successful
Requires precision modeling	Timing models only
Performance optimized	Programmable by software
Irregular block	Regular blocks
Difficult to route automatically	Easy to route automatically
Dynamic range limited by power supplies and noise (and linearity)	Dynamic range unlimited

We use the table above as a summary of the difference between the analog and digital circuits [57].

1.3 Integrated Circuit Technologies

Integrated circuits were invented in late 1950s, at Texas Instruments, Inc. In 1970s, Gordon Moore, one of the founders of Intel, predicted that the number of transistors per chip doubles every one and half years. The minimum channel length of MOS transistors dropped from 25um in 1960s to 90nm in the year of 2002, with the benefit of much higher complexity, smaller volume and higher speed. Without integrated circuit

technologies, computers might still be as huge as ENIC, and mobile phones would be as big as suitcases [56].

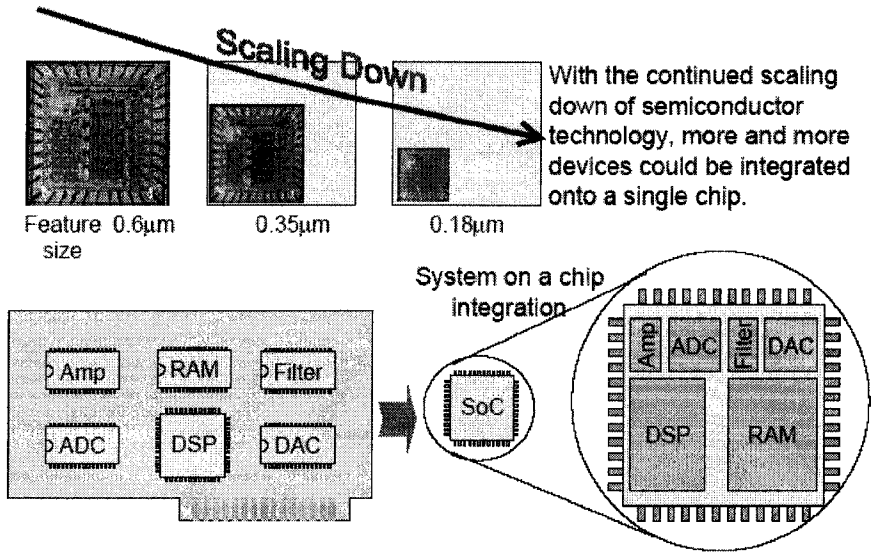


Fig. 1.2 Mixed-signal system-on-chip integration

Nowadays, most of the integrated chips have both analog and digital circuits. This is called mixed-signal integration, which penetrating into every corner of our everyday life, from supercomputers, space probes and medical diagnostic equipment, to printer, DVD players, cellular phones and children's toys. Digital circuit design is mostly automated from logic synthesis to placement and routing, while analog circuit design remains as an almost all-handcrafted art.

1.4 CMOS, Bipolar and BiCMOS Technologies

CMOS and Bipolar in silicon are the two mainstream semiconductor technologies. BiCMOS is the combination of the above two, which has both CMOS and Bipolar transistors.

CMOS technologies have the advantages of [56]

- Very large scale integration of both high-density digital circuits (such as DSP and memory) and analog circuit (including amplifiers, filters and A/D-D/A converters) for low cost.
- Ideal properties of MOS switches for high accuracy sample-data circuits, such as switch-capacitor filters and A/D-D/A converters.
- New CMOS technologies with smaller feature sizes (such as 0.25um and 0.18um) can operate at increasingly high speed (5GHz) comparable to some bipolar technologies.

Bipolar silicon technologies have the advantages of [56]

- Bipolar transistors can operated at higher frequencies than CMOS with relatively smaller power consumption.
- Suitable for pure analog integration with relatively high operating speed (such as RF circuits) or relatively high power (such as ADSL line drivers) applications.
- Digital circuits in bipolar are power hungry, prohibiting very larger scale integration.

BiCMOS technologies have most advantages of both CMOS and Bipolar technologies but at the expense of higher manufacturing cost due to required extra processing steps.

Thus CMOS technologies become mainstream technologies for mixed-signal integration due to the advantages of low cost and high integration density.

1.5 The Analog IC Design Process

The analog circuit design would be a very complex work, which requires deep understanding of the transistor models, experience and kinds of talents. While, most of

the design work should follow the process as below [57]:

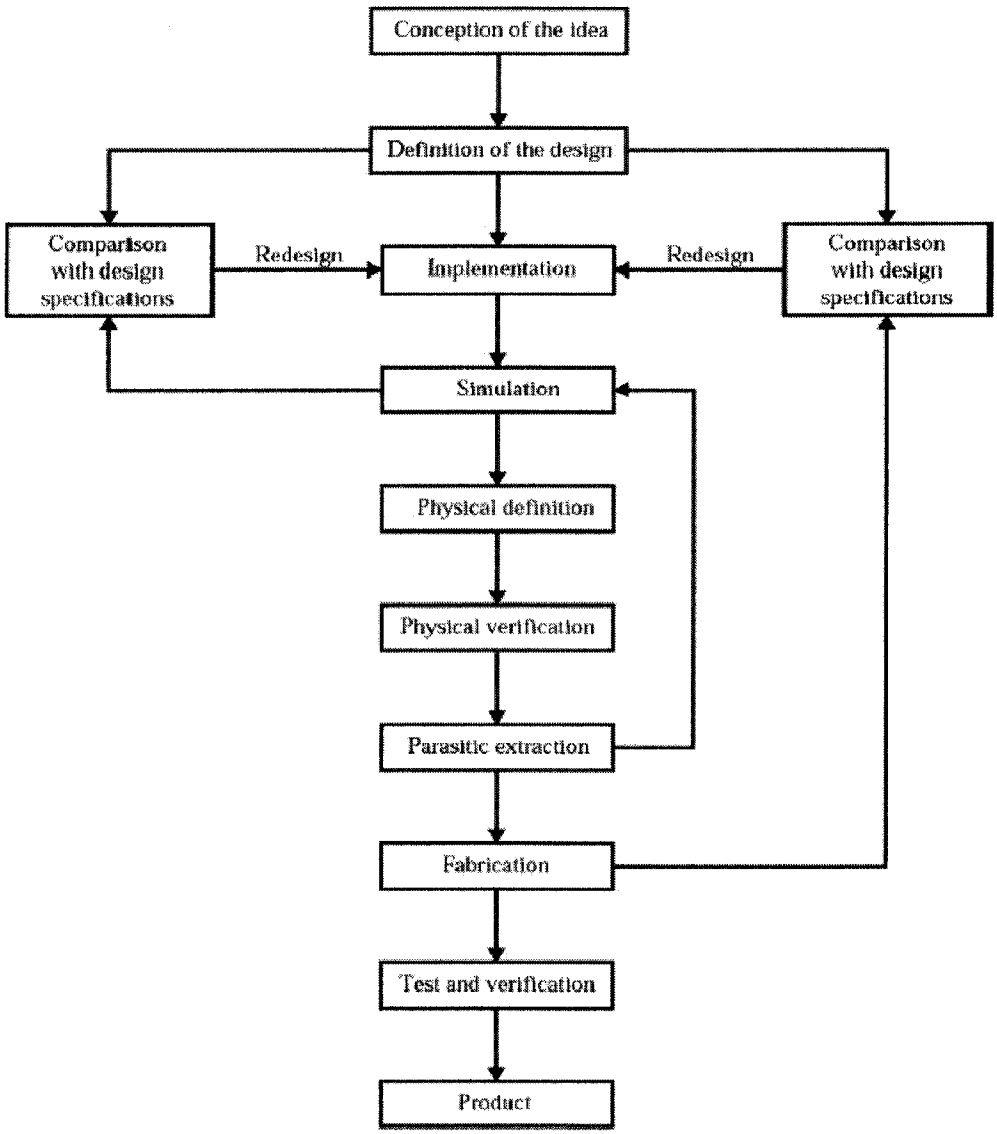


Fig. 1.3 The analog IC design process

CHAPTER 2

FUNDAMENTAL TO CMOS ANALOG MULTIPLIERS

Real-time analog multiplication of two signals is one of the most important operations in analog signal processing. The multiplier is used not only as a computational building block but also as a programming element in systems such as filters, neural networks, and as mixers and modulators in a communication system. Although high performance bipolar junction transistor multipliers have been available for a long time, the CMOS multiplier implementation is still a challenging subject especially for low-power and low-noise circuit design. Despite the large number of papers proposing new MOS multipliers, they can be roughly grouped into a few categories. This chapter will provide a complete survey of previous CMOS multipliers, and use it as the basis of our research work in this field.

2.1 Analog Multiplier Introduction

Multipliers perform linear products of two signals x and y, yielding an output as z=Kxy, where K is a multiplication constant with suitable dimension. Multipliers are often categorized as single-quadrant (x and y are uni-polar), two-quadrant (where x or y can be bipolar), and four-quadrant (where both x and y can be bipolar). Modulator and mixer are particular cases of multipliers that are designed with noise and frequency constraints. The history of the analog multipliers is originated from its use as a mixer and as an amplitude modulator that involves a multiplication of two signals.

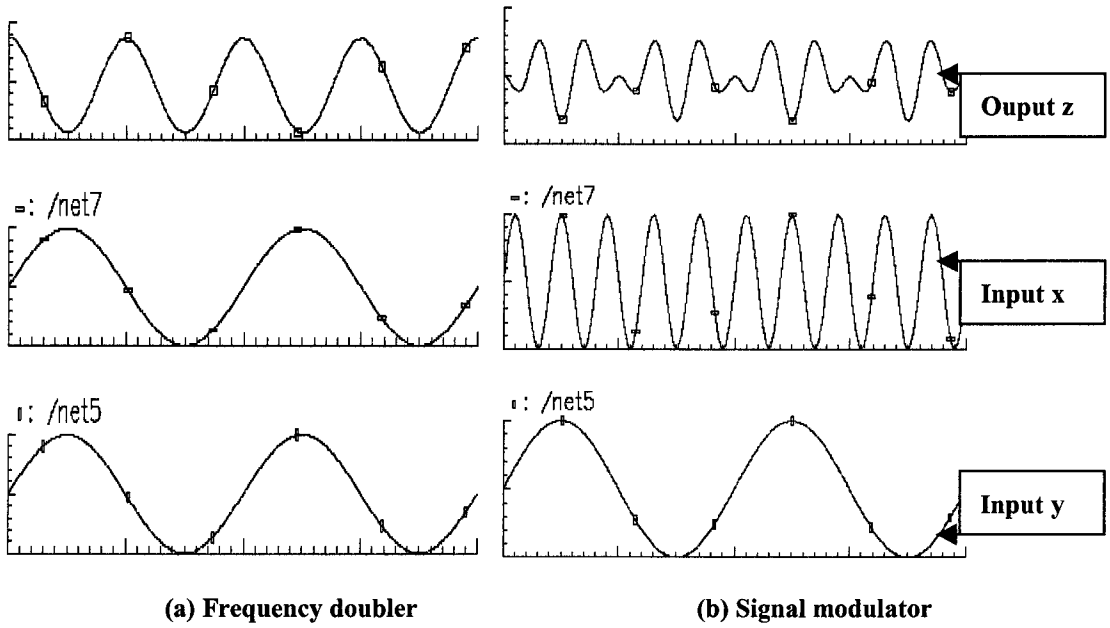


Fig. 2.1 The example of analog multiplier application (a) frequency doubler and (b) signal modulator

The basic idea of the multiplier implementation is illustrated in Fig 2.2. Two signals $v_1(t)$ and $v_2(t)$, are applied to a nonlinear device, which can be characterized by a high-order polynomial function. This polynomial function generates terms like $v_1^2(t)$, $v_2^2(t)$, $v_1^3(t)$, $v_2^3(t)$, $v_1^2(t)v_2(t)$ and many others besides the desired $v_1(t)v_2(t)$. Then it is required to cancel the undesired components. This is accomplished by a cancellation circuit configuration.

A multiplier could be realized using programmable transconductance component. Considering the conceptual transconductance amplifier of Fig 2.3, where the output current is simply given by $i_o = G_{m1}v_1$ and

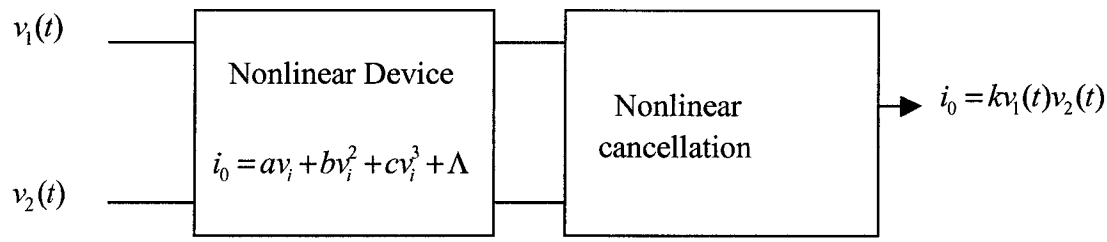


Fig 2.2 Basic idea of multiplier implementation (i=1,2....n)

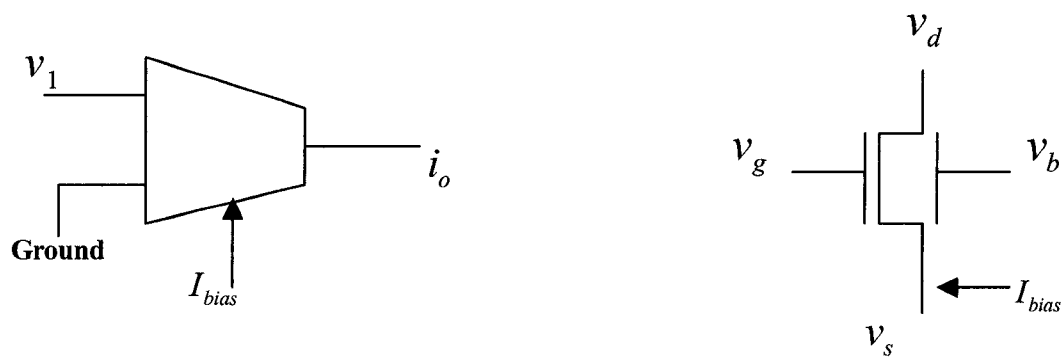


Fig. 2.3 Transconductance model

$G_{m1} = G_{m1}(I_{bias})$ for bipolar tranconductance, we have

$G_{m1} = \dfrac{I_{bias}}{2V_t}$ where V_t is the thermal voltage (kT/q).

Next, a small signal i_2 is added to the bias current. The second input signal v_2 can be converted in to a current $i_2(t) = G_{m2}v_2(t)$. Then, the output current yields [52]

$$i_o(t) = G_{m1}v_1 = \frac{I_{bias1} + G_{m2}v_2(t)}{2V_t}v_1 = \frac{I_{bias2}v_1(t)v_2(t)}{2V_t 2V_t} + \frac{I_{bias1}v_1(t)}{2V_t} \tag{2.1}$$

or $\quad i_o(t) = k_1 v_1(t)v_2(t) + k_2 v_1(t)$

Thus, $i_o(t)$ represents the multiplication of two signals $v_1(t)$ and $v_2(t)$, and an

unwanted component $k_2 v_1(t)$. This component can be eliminated by some cancellation structure. This is the basic operation principle of a Gibert Cell [1-2]. Operational transconductance amplifier based implementations are reported in [3-4].

As the digital technology dominates in modern electronics, analog circuits are required to share the same standard CMOS process for low-cost fabrication. Thus, the popular BJT Gibert Cell is not suitable in a standard digital process, and the designers must address low power supply voltage requirements. One problem the designers often encounter is how to select the best multiplier architecture for their application. Here, in this chapter, we will talk about the existing multiplier structures, and also their cons or pros.

2.2 Operation Modes and Circuit Topologies

Despite of many reported circuits, all cancellation methods can be categorized as two groups (single-quadrant multipliers and square law device) [52]. Since the single-ended configuration cannot achieve complete cancellation of nonlinearity and has poor supply rejection ration (PSRR), a fully differential configuration is necessary in a sound multiplier topology. The multiplier has two inputs, therefore there are four combinations of two differential signals, i.e., (x,y), (-x,y), (x,-y), and (-x,-y).

The topology of Fig 2.4(a) is based on single-quadrant multipliers, while Fig 2.4(b) is based on square law device. These topologies achieve multiplication and simultaneously cancel out all the higher order and common-mode components (X and Y) based on the following equalities

$$[(X+x)(Y+y)+(X-x)(Y-y)]-[(X-x)(Y+y)+(X+x)(Y-y)=4xy \qquad (2.2)$$

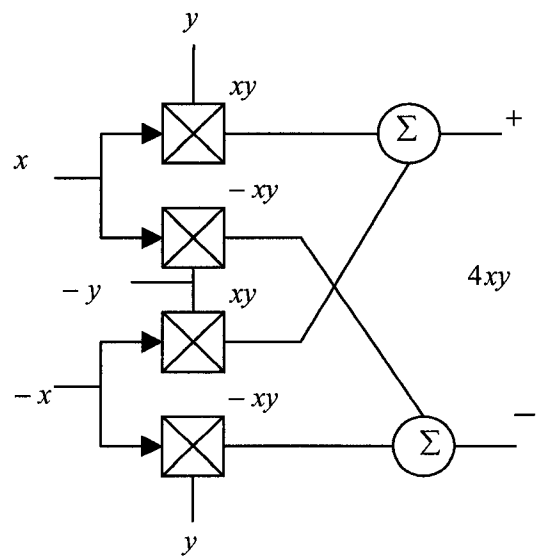


Fig. 2.4(a) Multiplier topology based on single-quadrant

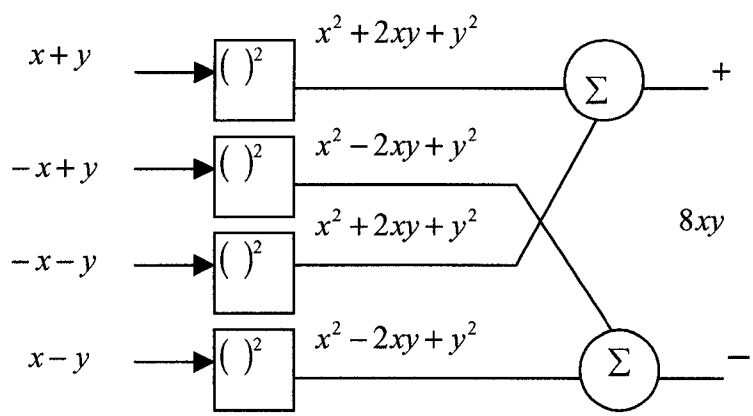


Fig. 2.4(b) Multiplier topology based on square law device

or

$$\left\{[(X+x)+(Y+y)]^2+[(X-x)+(Y-y)]^2\right\}-$$

$$\left\{[(X-x)+(Y+y)]^2+[(X+x)+(Y-y)]^2\right\}=8xy \tag{2.3}$$

respectively. Note that, lower case letters represent small signals and higher case letters represent DC bias (common-mode components).

MOS transistors can be used to implement these cancellation schemes and the

fundamental operation in transconductance multiplier because the MOS FET is a transconductance device. The simple MOS transistor model is expressed as

$$I_d = K[V_{gs} - V_T - \frac{V_{ds}}{2}]V_{ds} = K[V_{gs}V_{ds} - V_T V_{ds} - \frac{V_{ds}^2}{2}] \tag{2.4}$$

when $V_{gs} > V_T$, $V_{ds} < V_{gs} - V_T$

$$I_d = \frac{1}{2}K[V_{gs} - V_T]^2 = \frac{K}{2}[V_{gs}^2 - 2V_{gs}V_T - V_T^2] \tag{2.5}$$

when $V_{gs} > V_T$, and $V_{ds} > V_{gs} - V_T$

for NMOS transistors in its linear and saturation regions, respectively. Here, $K = \mu_0 C_{ox}\frac{W}{L}$ and V_T are the conventional notation for transconductance parameter and the threshold voltage of the MOS transistors, respectively.

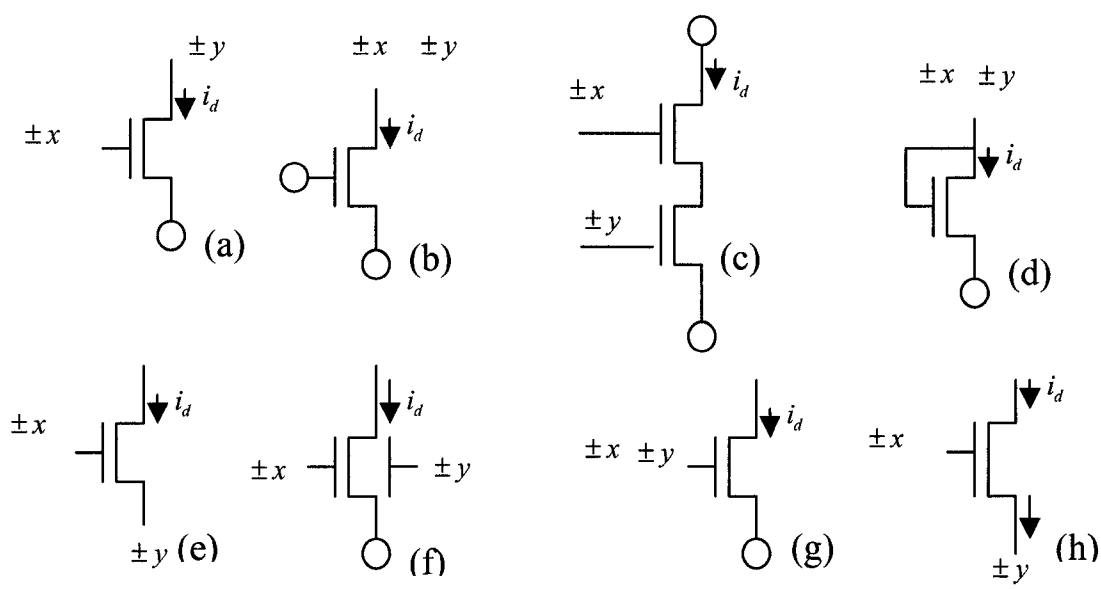


Fig. 2.5 Voltage signal injection methods

Fig 2.5 shows the application methods of two signals (x and y) in a MOS FET. The small circle on the transistor terminal represents a fixed biasing voltage. x and y are

time-variable voltage signals, disregarding the bias. The first three methods are used for operation in their linear region and the rest are for transistors working in the saturation region. The signal injection methods (b), (d) and (g) in Fig 2.5 require a voltage summing circuit, but this extra circuit could affect the total power consumption.

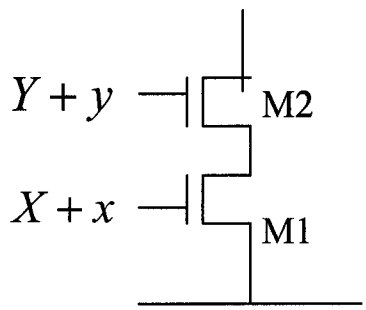
We use the following table 2.1 as a summary of all 8 kinds of signal injection methods.

Table 2.1 Summary of operation modes

Operation region	Signal injection method	Active term	Cancellation method	Comment
Linear	Fig 2.5 (a)	$v_{gs}v_{ds}$	Single-quadrant	Practical
Linear	Fig 2.5 (b)	v_{ds}^2	Square device	Not practical
linear	Fig 2.5 (c)	$v_{gs}v_{ds}$	Single-quadrant	Not practical
Saturation	Fig 2.5 (d)	v_{gs}^2	Square device	Not practical
Saturation	Fig 2.5 (e)	v_{gs}^2	Square device	Practical
Saturation	Fig 2.5 (f)	$v_{gs}V_{TH}$	Single-quadrant	Not practical
Saturation	Fig 2.5 (g)	v_{gs}^2	Square device	Practical
Saturation	Fig 2.5 (h)	v_{gs}^2	Square device	Practical

2.3 Multipliers Operation in the Linear Region

We can cluster all transconductance multipliers into two groups based on the MOS operation region, linear [5-21] and saturation [22-49].



$$i_{ds} = g_m v_{gs2}$$

$$v_{ds1} = R_{on} i_{ds}$$

Fig. 2.6 Linear transconductance

Linear transconductance:

First we introduce a programmable linear transconductance and show how it can be used to yield a multiplier. In Fig 2.6 [5], M1 works in the linear region while M2 operates in the saturation region when proper bias voltage X and Y are provided. For small signal model, we have the relationship as follow:

$v_{ds1} = R_{on} i$ and $i = g_{m2} y$

Therefore, we have $v_{ds1} = R_{on} g_{m2} y$

We could use signal y to control v_{ds} of transistor M1. That is the basic idea of linear transconductance.

Using $v_{gs}v_{ds}$:

There are different structures to implement the multipliers operating in linear region based on the linear transconductor in Fig 2.6. The structure below is an example [14].

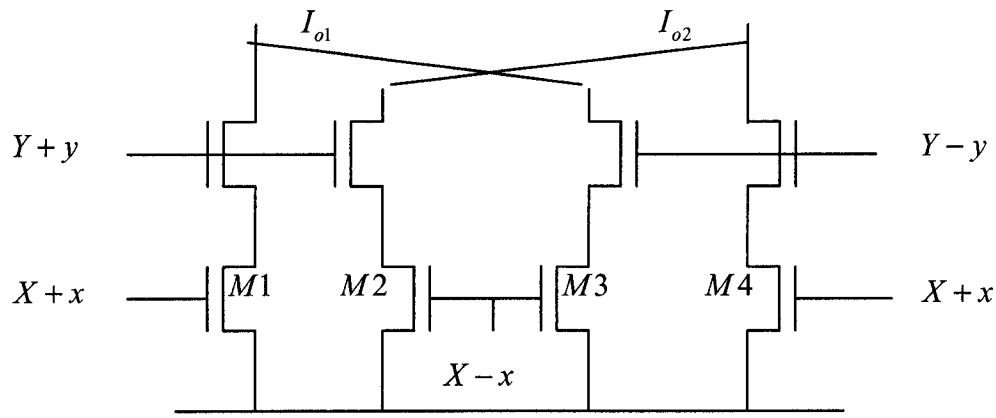


Fig. 2.7 Four-quadrant analog multiplier using $v_{gs}v_{ds}$

In Fig 2.7, we combine two linear transconductance to implement the multiplier. For the 4 columns currents, we have

$$I_1 = K(X + x - V_{TH} - \frac{y}{2})y$$

$$I_2 = K(X - x - V_{TH} - \frac{y}{2})y$$

$$I_3 = K(X + x - V_{TH} + \frac{y}{2})(-y)$$

$$I_4 = K(X - x - V_{TH} + \frac{y}{2})(-y)$$

Then, we have $$I_o = (I_1 + I_3) - (I_2 + I_4) = 4Kxy \qquad (2.6)$$

which is the multiplication of two signals, where K is a constant. Some work has been done to optimize the current-efficiency with this kind of multipliers [55].

Using v_{ds}^2

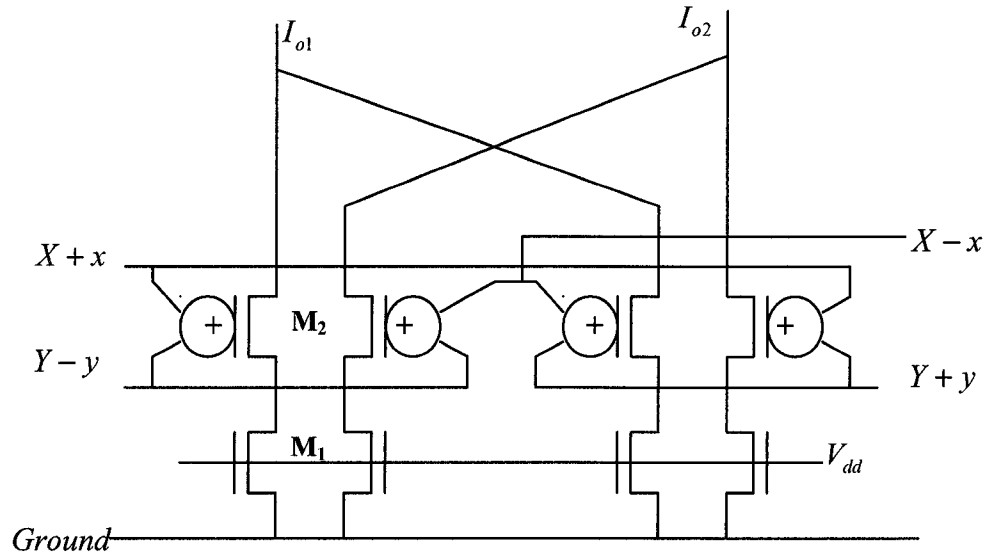


Fig. 2.8 Multiplier using v_{ds}^2

The MOS transistors working in the linear region has a square term v_{ds}^2. This term can be used to realize the cancellation method in (2.2). In Fig 2.8, sum and difference of two input signals are applied to the gate of source followers M2 and they control the drain voltage of M1 that operates in the linear region [50]. However, the linearity of this configuration is poor.

2.4 Multipliers operation in the saturation region

Using v_{gs}^2 with gate and source injection:

A four-quadrant multiplier working in the saturation region can be implemented by four cross-coupled transistors as shown in Fig 2.9 [22-23]. The output current I_o yields

$I_o = I_{o1} - I_{o2} = 4Kxy$ based on (2.3) and (2.5).

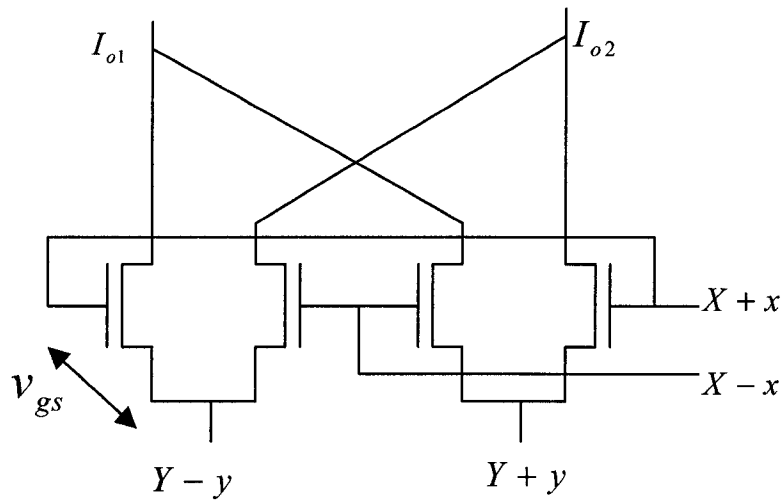


Fig. 2.9 Multiplier using v_{gs}^2 with gate and source injection

Using v_{gs}^2 with voltage adders:

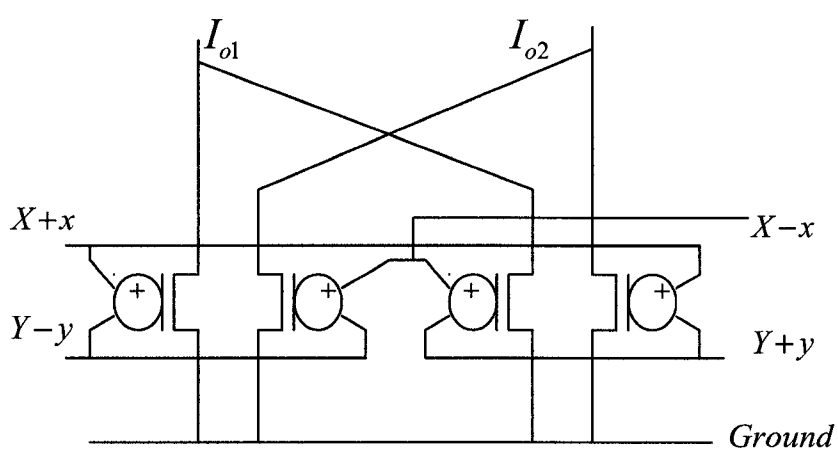


Fig. 2.10 Multiplier using v_{gs}^2 with voltage adders

This multiplier architecture is based on the nonlinearity cancellation of Fig 2.4 (b) and

voltage summing circuits. Four cross-coupled transistors with voltage summer realized a four-quadrant multiplier as shown in Fig 2.10. The output current can be obtained based on (2.3) and (2.5). Reference [41] provides a summary of this multiplier type. A recent paper [54] provides a couple of structures that use low supply voltage. As they require additional transistors, they do not have any advantage over other types.

Using $v_{gs}V_{TH}$ with substrate terminals:

The substrate of MOS transistors can be used as an additional input terminal as long as the substrate-source junction is kept reverse biased. The substrate potential controls the threshold voltage for the NMOS transistor as

$$V_{TH} = V_{THO} + \gamma[\sqrt{2|\Phi_F| - V_{bs}} - \sqrt{2|\Phi_F|} \tag{2.7}$$

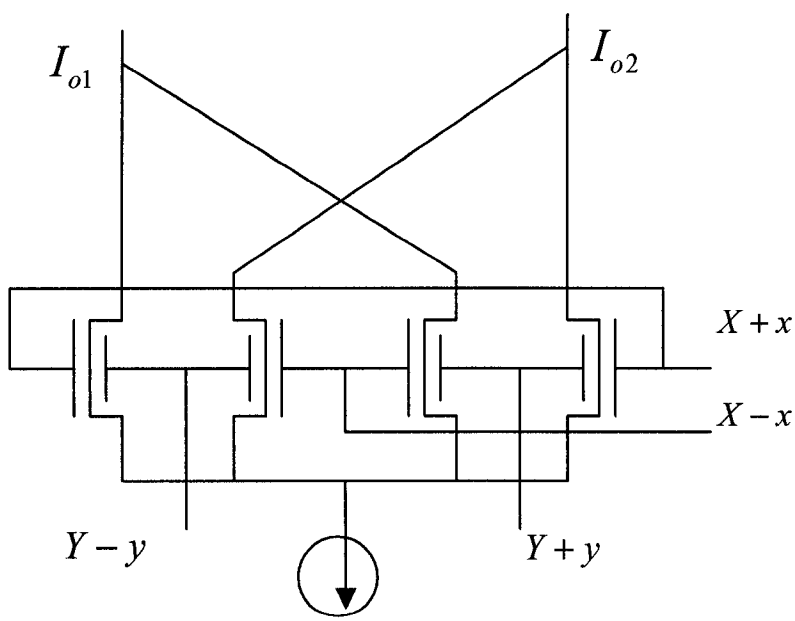


Fig. 2.11 Using $v_{gs}V_{TH}$ with substrate terminals

where V_{THO} is the threshold voltage when V_{bs}=0, γ is the body effect coefficient and Φ_F is the Fermi potential [52]. Substitute V_{TH} in (2.5) with (2.7), the configuration shown in Fig 2.11, based on (2.3), gives

$$I_o = \frac{4K\gamma}{2|\phi_F|-Y+s}[y\sqrt{2|\phi_F|-Y+s}+(\frac{y}{2|\phi_F|-Y+s})^3+\mathrm{A}]x \approx \frac{4K\gamma}{2|\phi_F|-Y+s}xy$$

The approximation is valid only if $2|\Phi_F|-Y+s$ >>y. This kind of analog multipliers is shown in Fig 2.11. However, the linearity of this configuration is poor.

Using MOS Gilbert Cell:

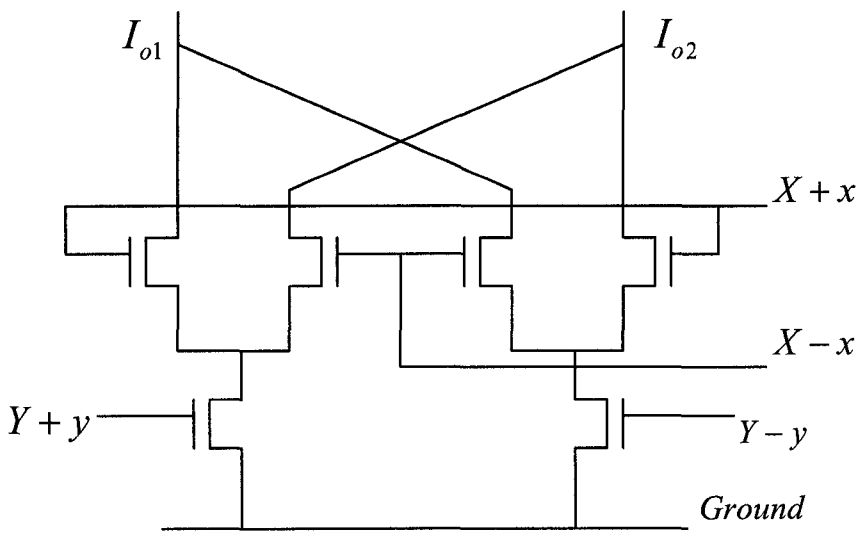


Fig. 2.12 MOS Gilbert Cell multiplier

MOS Gilber Cell comes from the Bipolar Gilbert Cell [1], and it is the earliest implementation of multiplier with CMOS technology. The differential output currents from two differential pairs are subtracted, yielding

$$I_o = I_{o1} - I_{o2} = 2\sqrt{K}x[\sqrt{I_{y1}} - \sqrt{I_{y2}}]$$

The output current, $\sqrt{I_{y1}} - \sqrt{I_{y2}}$ is generated by another differential pair as $\sqrt{I_{y1}} - \sqrt{I_{y2}} = \sqrt{2K_3 y}$. Thus, the MOS Gilbert multiplier shown in Fig 2.12 yields $I_o = I_{o1} - I_{o2} = 2\sqrt{2KK_3}xy$ where x and y are both voltage signals. As its linearity is poor, several modified versions have been reported [44-49].

2.5 Comparison of Different Multiplier Structures

Some limited qualitative comparisons are summarized in table 2.2. From this table, we could observe that the circuits in Fig 2.7 and Fig 2.9 have the properties above the "average multipliers". Therefore, we try to do some simulation for these two structures about the linearity, power dissipation and noise in order to find a topology with the best average performance as a reference for our future research work.

Table 2.2 Comparison of different multiplier structures

Structure	Worse than	Remark
Fig 2.7		Good linearity Low supply voltage
Fig 2.8	Fig 8	Require additional circuitry Poor linearity
Fig 2.9		Good linearity
Fig 2.10	Fig 10	Require additional circuitry
Fig 2.11	Fig 10	Poor linearity
Fig 2.12	Fig 8	Poor linearity High supply voltage

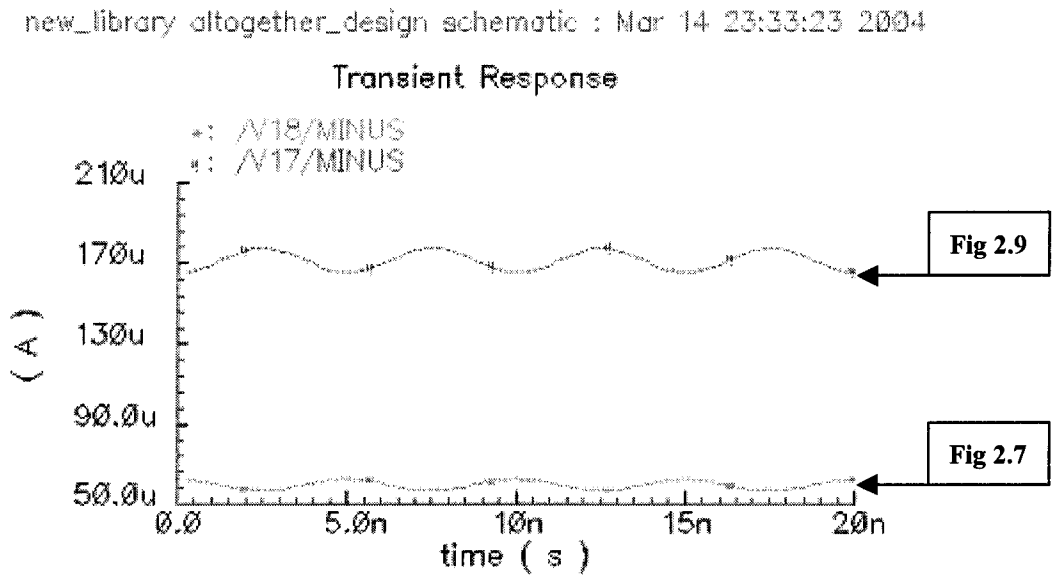


Fig. 2.13 The comparison of total current for Fig 2.7 and Fig 2.9

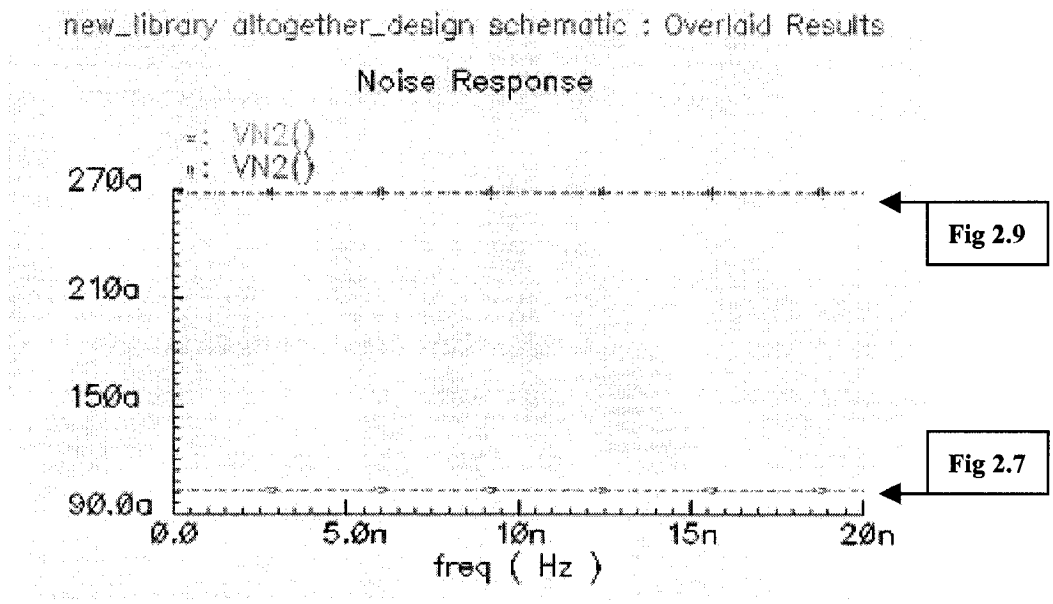


Fig. 2.14 The comparison of input noise for Fig 2.7 and Fig 2.9

We compare these two structures with simulation result. The linearity of x signals in Fig 2.7 is better than that in Fig 2.9. The linearity of signal y in Fig 2.9 is better than that in Fig 2.7. The power supply current can be explained as power consumption supposing the same supply voltage. The total current in Fig 2.7 is lower than the total current in Fig 2.9 (see Fig. 2.13). The input noise of Fig 2.7 is much lower than that of Fig 2.9 (see Fig. 2.14). We can see, that from our analysis, the circuit in Fig 2.7 has best performance.

Although a large number of analog multipliers are reported, they fall into eight categories described in this chapter and summarized in Table 2.1. Several multiplier architectures do not have any clear advantage over others. As the current trend of circuit design is low power and low noise, the circuit in Fig 2.7 seems to be the one of the most attractive high-performance multiplier structure [51], which provides us a basis for our further research.

CHAPTER 3

BASIC IDEA OF ANALOG MULTIPLIER DESIGN

In this chapter, we talk about our basic idea for the CMOS analog multiplier design. This idea comes from our deep research over 70 multiplier structures in the literature survey. And also, we talk about the basic performance metrics that we have to consider during our design of structures.

3.1 The Performance Metrics of Analog Multipliers

Linearity: As we know, the basic building block of analog multipliers is the transconducance amplifier. The input-output characteristic of transconductance amplifier is generally a nonlinear function that can be approximated by polynomial over some signal range:

$$i(t) \approx a_0 + a_1 x(t) + ... + a_n x^n(t) \tag{3.1}$$

For a sufficient of narrow range of x, we could have

$$i(t) \approx a_0 + a_1 x(t) \tag{3.2}$$

where a_0 can be considered the operating (bias) point and a_1 the small signal gain. So long as $\alpha_1 x(t) << \alpha_0$, the bias point is disturbed negligibly. The higher order terms are insignificant. In other words, $\Delta i = a_1 \Delta x$ indicating a linear relationship between the input and output.

For an analog multiplier, which is the combination of some amplifiers, there should have some linear relationship between the input and output as

$$z = Kxy$$

This relationship can be gotten from equation (3.1) for all working transconductance amplifier by canceling the higher orders and bias voltages. We could see that the linearity between the input and output is the most important performance and it is the basis of analog multiplier design. As this linear relationship is gotten from the approximation in (3.1), sometimes, in order to get accurate relationship, we have to infer to the large-signal analysis.

Input Range: We hope the analog multipliers we designed can be used in different environment, that is, the input signal could have very large magnitude or very small magnitude. But on the other hand, in order to keep the transistors in the suitable working region (linear or saturation), we have to limit the magnitude of the input signal. In general, the linearity would be degraded if the input range increases. Therefore, the input range (voltage swing) is one of the important performance metrics we have to consider.

Power Consumption: With the nowadays' trend to the low voltage and low power design in the analog field, we try to decrease the power consumption in our design, which is the main aim of our research work presented in this thesis.

Noise Performance: Noise is also an important consideration in analog multiplier design, especially for the small-signal application. Noise limits the minimum signal level that a circuit can process with acceptable quality.

Analog signals processed by integrated circuits are corrupted by two different types of noise: device electronic noise and "environmental" noise. In this thesis, we will focus on the electronic noise. The electronic noise consists of thermal noise and flicker noise mainly.

MOS transistor exhibits thermal noise, which is because of the resistor component in the transistors. It can be proved [52] that for long-channel MOS devices operating in the saturation, the channel noise can be modeled by a current source connected between the drain and source terminals as: $\overline{I_n^2} = 4KT\gamma g_m df$. Here the coefficient γ is derived to be equal to 2/3 for long-channel transistors and may need to be replaced by a larger value for small size transistors. For transistors working in the linear region, we have $\overline{I_n^2} = 4KTg_{ds}df$ [53].

Flicker noise is another important source of electronic noise for MOS transistors. When charge carriers move at the interface between the gate oxide and the silicon substrate, some are randomly trapped and later released, introducing "flicker" noise in the drain current. The flicker noise is more easily modeled as a voltage source in series with the gate and roughly given by $\overline{V_n^2} = \frac{K}{C_{ox}WL}\frac{1}{f}$ [52], that is, the noise spectral density is inversely proportional to the frequency.

The natural approach to measure the noise is to set the input to zero and calculate the total noise at the output due to various sources of noise in the circuit. While intuitively appealing, the output–referred noise does not allow a fair comparison of the performance of different circuits because it depends on the gain. To overcome the above quandary, we usually specify the "input-referred noise" of circuits. The idea is to represent the effect of all noise sources in the circuit by a single source, $\overline{V_{n,in}^2}$ at the input such that the output noise is equal to the input-referred noise times the gain.

In addition, speed, gain, input and output impedance may be important for specific applications. In practice, most of these parameters trade with each other, making the

design a multi-dimensional optimization challenge. Illustrated in the "analog multiplier design octagon" of Fig 3.1, such tradeoff provides many challenge in analog design, requiring intuition and experience to arrive at an acceptable compromise.

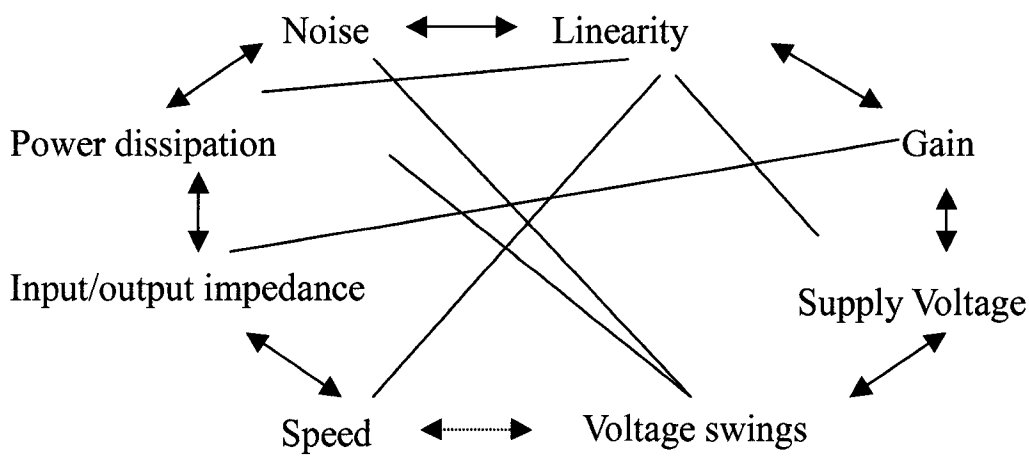


Fig. 3.1 Analog multiplier design octagon.

3.2 Differential Structure

The differential structure is among the most important circuit inventions, and has become the dominant choice in today's high-performance analog and mixed-signal circuits.

A single-ended signal is defined as one that is measured with respect to a fixed potential, usually the ground. A differential signal is defined as one that is measured between two nodes that have equal and opposite signal excursions around a fixed potential. In the strict sense, the two nodes must also exhibit equal impedances to that potential. Fig 3.2 illustrates the two types of signals conceptually.

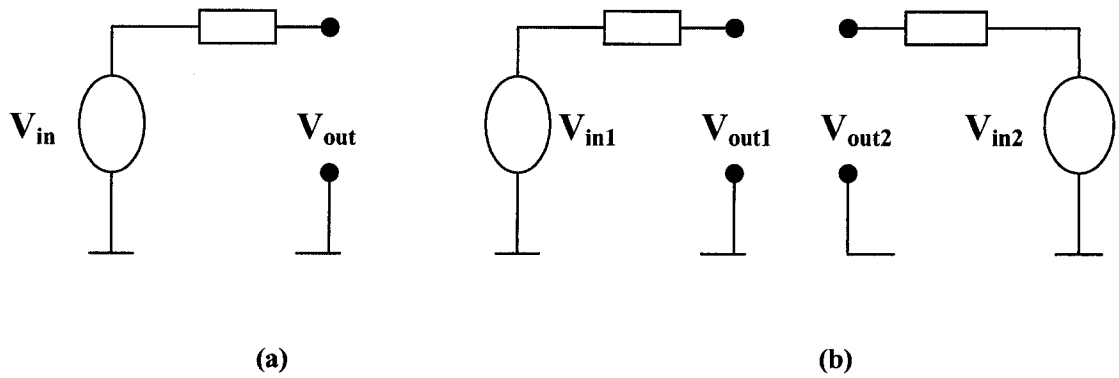


Fig. 3.2 (a) single-ended signals and (b) differential signals

An important advantage of differential operation over single-ended signaling is higher immunity to "environmental" noise. Supposing that two adjacent lines in a circuit carry a small, sensitive signals and a large clock waveform, transitions on one line will corrupt the other line. If we use the differential structure, and the clock line is placed midway between the two, the transition disturbs the differential phase by equal amount, leaving the difference intact.

Another useful property of differential signaling is the increase in maximum achievable voltage swings. Other advantage of differential circuits over single-ended counterparts includes simpler biasing and higher linearity.

While it may seem that differential circuits occupy twice as much area and power consumption as single-ended alternatives, the advantage it brings us outweighs the disadvantage we suffer. Therefore, we will use the differential structure in our analog multiplier design.

3.3 The Basic Idea of Low Power Design

For previous CMOS analog multiplier design, most transistors are biased to operate in the

saturation region where the drain current I_D of the device is given by [52]

$$I_D = \frac{1}{2}K(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{3.3}$$

where $K = \mu_o C_{ox} W/L$ and V_{TH} are the transconductance parameter and the threshold voltage of the device, respectively, and λ represents the channel-length modulation effect for long channel devices.

Because the power consumption of an analog circuit can be expressed as

$$P = V_{\sup ply} * I_{total} \tag{3.4}$$

while supply voltage is normally fixed for a certain circuit, we could use the total current to represent the power consumption. It can be seen that in the saturation region, the low power consumption requires a small V_{GS} that leads to the reduced input range. A simple example is shown in Fig. 3.2 where two signals are injected to the two transistors in series (see Fig. 3.2 (a)) or in parallel (see Fig. 3.2 (b)). The series structure has less power consumption, but with a smaller input range since V_{GS} must satisfy $0 < V_{GS} - V_{TH} \leq V_{DS}$ for the transistors to operate in saturation region. In contrast, the parallel structure as shown in Fig. 3.2 (b) has a bigger input range while the two devices would draw more current from the power supply.

Therefore, there is a tradeoff between the input range and the power consumption, which provide a real challenge to the analog multiplier designers.

At the same time, we realized that by biasing the transistors to operate in the linear region, we could reduce the drain current while keeping a relatively large input range. The drain current in linear region is given by [52]

$$I_D = K[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2] \tag{3.5}$$

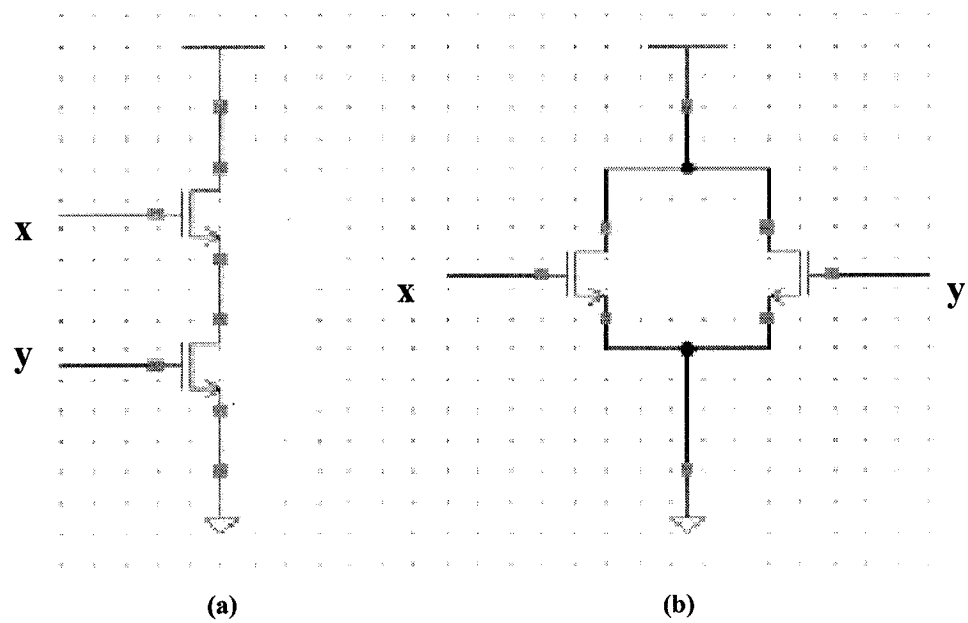


Fig. 3.3 Power consumption and input range for (a) series structure and (b) parallel structure

Since $V_{GS} - V_{TH} > V_{DS}$ in the linear region, the overdrive voltage can be biased to increase the input range. The drain current could remain a proper value by decreasing the V_{DS}, keeping the power dissipation at the same level.

Our basic idea for low power design of analog multiplier is to fit most of the transistors into the linear region, and also keep the V_{DS} as low as possible to decease the drain current. Actually, some of designers have tried to design the analog multipliers with most transistors working in the linear region, but nobody has given the basic design idea for this type of analog multipliers. And another problem we have to solve is that the multipliers in this type have worse linearity compared with most multipliers working in the saturation region. We try to design some multipliers with less total current, thus less power consumption, and with less noise, if applicable, while at the same time, keep good linearity.

The basic design flow of our structure can be shown as below in Fig 3.4. We should do the theoretical computation and analysis first to find an analog multiplier with good performance. Then we do the simulation by Hspice simulator in the schematic level about the performance of power consumption, noise and linearity, to verify our analysis before. After that, we transfer to the layout level to implement the circuit with more details. In order to help us to do good job in this level, we should make the layout verification by the DRC, LVS and Extraction. And also, we have to do the simulation in this level by Hspice to verify that the performance has no big change in this level. When all of this work has been done, we would send the design data to CMC to get the circuits fabricated and after we get the chip we will do the test to give the final verification.

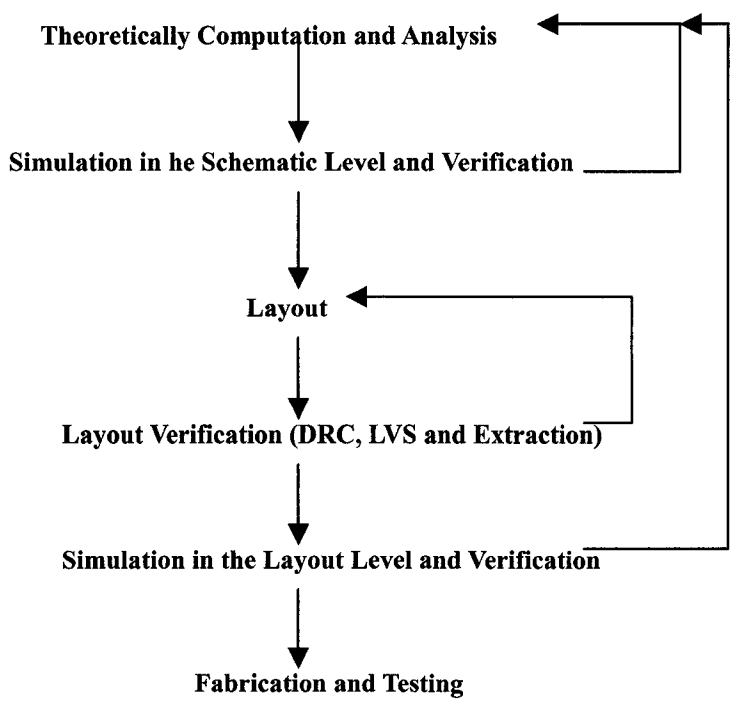


Fig. 3.4 Design flow of our structures

CHAPTER 4

FIRST ANALOG MULTIPLIER STRUCTURE

In this chapter, we present a low power and low noise analog multiplier operating with 1.5V supply voltage. The core structure consists of only 6 transistors and brings in the benefits in terms of power consumption, noise performance and linearity. Some design considerations are also provided. The extensive experiments with Hspice simulation show that this new structure is particularly attractive for low power and low noise applications. We hope we could summarize our design idea by the practice of this design.

4.1 Circuit Topologies and Theoretical Analysis

Fig 4.1 shows the proposed CMOS analog multiplier structure, which consists of 4 NMOS transistors (M1-M4) operating in the linear region and 2 NMOS transistors (M5-M6) working in the saturation region. The drain current I_D of the NMOS transistors in the linear region is expressed as [52]

$$I_D = K[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$$

Assuming that all transistors in Fig 4.1 are biased to operate in a proper (linear or saturation) region, we show, in the following, that this topology achieves multiplication. We suppose that (a) all transistors in Fig 4.1 have same threshold voltage V_{TH}, (b) the M1-M4 have same transconductance parameter K_l (i.e., $K_1=K_2=K_3=K_4=K_l$) and (c) the M5-M6 have the same transconductance parameter K_u (i.e., $K_5=K_6=K_u$), we have

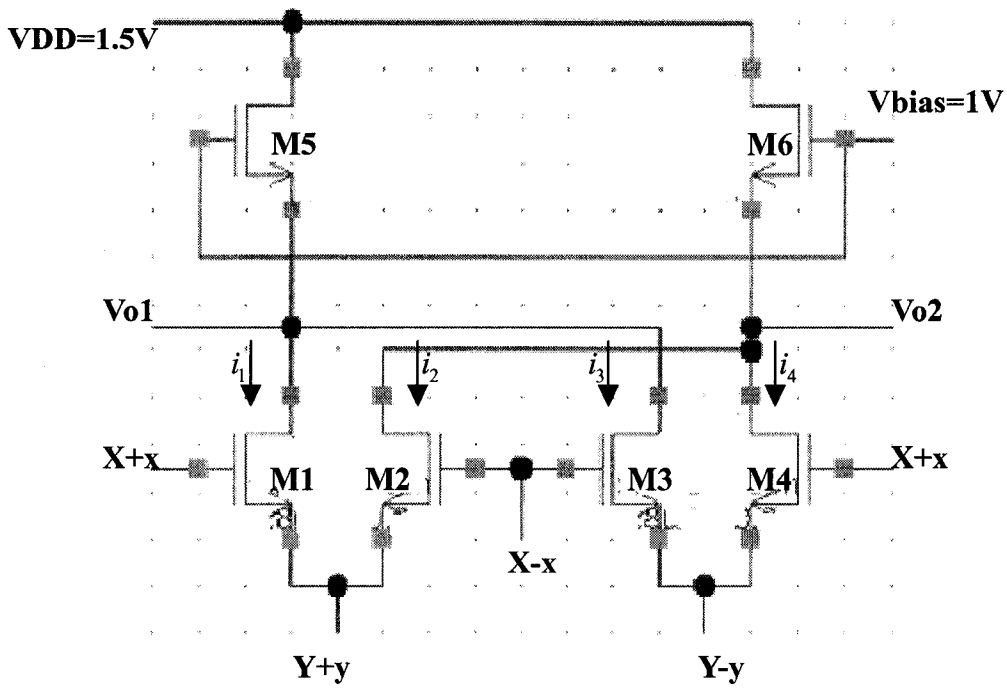


Fig. 4.1 Our first multiplier structure

$$i_1 = K_l[X - x - Y - y - V_{TH})V_{DS1} - \frac{1}{2}V_{DS1}^2] \tag{4.1}$$

$$i_2 = K_l[X + x - Y - y - V_{TH})V_{DS2} - \frac{1}{2}V_{DS2}^2] \tag{4.2}$$

$$i_3 = K_l[X + x - Y + y - V_{TH})V_{DS3} - \frac{1}{2}V_{DS3}^2] \tag{4.3}$$

$$i_4 = K_l[X - x - Y + y - V_{TH})V_{DS4} - \frac{1}{2}V_{DS4}^2] \tag{4.4}$$

where

$$v_{DS1} = v_{o1} - Y - y \tag{4.5}$$

$$v_{DS2} = v_{o2} - Y - y \tag{4.6}$$

$$v_{DS3} = v_{o1} - Y + y \tag{4.7}$$

$$v_{DS4} = v_{o2} - Y + y \tag{4.8}$$

The drain current in the saturation region can be shown as

$$I_D = \frac{1}{2}K(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{4.9}$$

Ignoring λ in (4.9) since it is very small, the drain current of M5 and M6 are

$$i_1 + i_3 = \frac{1}{2}K_u(V_b - V_{o1} - V_{TH})^2 \tag{4.10}$$

$$i_2 + i_4 = \frac{1}{2}K_u(V_b - V_{o2} - V_{TH})^2 \tag{4.11}$$

respectively. By solving the above equations for small signals x and y, the differential voltage V_{o1}-V_{o2} can be approximated as

$$V_{o1} - V_{o2} \propto \frac{K_l}{K_u}xy \tag{4.12}$$

which represents the multiplication of two signals. Thus, for a given DC bias, the input range of the multiplier can be influenced by $\frac{K_l}{K_u}$. However, there is a minimum value of $\frac{K_l}{K_u}$ in order to keep M1-M4 operating in the linear region. While it exhibits a strong ability of canceling nonlinearity, the approximation in (4.12) still introduces a linearity error if: (a) the difference of V_{TH} for transistors in saturation region and in linear region has to be considered, (b) the higher-order effects of the devices (such as body effect and channel-length modulation) need to be taken into account, or (c) other issues such as temperature and possible device mismatch are not ignored.

To realize multiplication, proper bias arrangements for all transistors in Fig 4.1 are required. The bias condition can be written as:

$$\begin{cases} Y \pm y < V_{o1}(or V_{o2}) < V_b - V_{TH} \le V_{DD} - V_{TH} \\ V_{o1}, V_{o2} < X \pm x - V_{TH} \\ 0 \le Y \pm y < X \pm x - V_{TH} \end{cases} \tag{4.13}$$

where V_{o1} and V_{o2} are determined by (4.1) – (4.11). If K_l / K_u increases, V_{o1} (or V_{o2}) would decrease, leading to the increased input range for x and reduced input range for y since V_{o1} (or V_{o2}) must meet: $Y + y < V_{o1}, V_{o2} < X - x - V_{TH}$. However, increasing X-Y can improve the input range for both x and y. Typical values to be used are: V_{DD}=1.5V, X=1.3V, Y=0.2V, V_{TH}=0.6V, and $V_{o1}=V_{o2} \approx 0.22$V (when x=y=0, V_b=1.0V and $K_l=K_u$).

One disadvantage with the structure in Fig 4.1 is that the input range for signal y is limited. To solve this problem, one can add two signal attenuators at the input terminals of y, as shown in Fig 4.2. The signal attenuators consist of 4 NMOS transistors (i.e., M7-M10) operating in the linear region. The aim of the attenuators is to transfer the large signal in the input terminals into a small signal for increased input swing. The M7-M10 should be biased properly such that z=cy, where c is a constant (c<1).

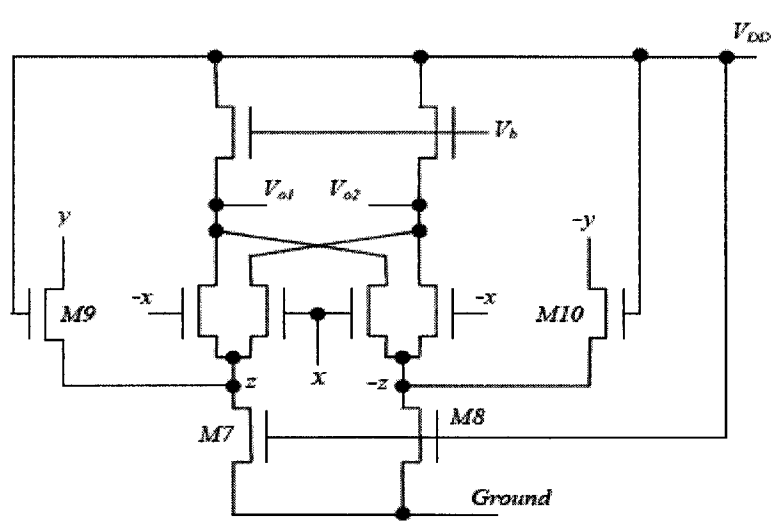


Fig. 4.2 Multiplier structure with signal attenuators

However, the use of attenuators introduces more power consumption and device noises. Therefore, this structure can be used in the application where the input range is an important consideration while the power and noise are not. In the following, we will present the performance analysis and discussion on the core structure in Fig 4.1 only.

4.2 Performance Analysis

The performance metrics for the multipliers include the linearity, input range, chip area cost, power consumption, frequency range, and noise. Some of them can be more important than others, depending upon applications. It is not uncommon that some measurements are contradictory. When this happens, a reasonable tradeoff has to be made.

In this section, we give a quantitative analysis on power dissipation and noise for the proposed multiplier. The other metrics will be discussed together with experiments in the next section.

Power Dissipation: As we have talked before, normally the supply voltage for certain circuit is fixed. Therefore, we could use the total current in the structure to represent the power consumption. For the proposed structure in this chapter (Fig 4.1), the total current is given by

$$I_{total} = i_1 + i_2 + i_3 + i_4$$

from (4.1)-(4.4) and (4.10)-(4.11), we have

$$i_1 + i_3 = 2K_l(X - Y - V_{TH})(V_{o1} - Y) + 2K_l(x + y)y = \frac{1}{2}K_u(V_b - V_{o1} - V_{TH})^2 \qquad (4.14)$$

$$i_2 + i_4 = 2K_l(X - Y - V_{TH})(V_{o2} - Y) + 2K_l(-x + y)y = \frac{1}{2}K_u(V_b - V_{o2} - V_{TH})^2 \qquad (4.15)$$

and

$$I_{total} = 2K_l(X - Y - V_{TH})(V_{o1} + V_{o2} - 2Y) + 4K_l y^2 \tag{4.16}$$

This implies that the power dissipation can be reduced if any of X-Y, K_l or y decreases. But too low values of X-Y and K_l could negatively affect the input range. Note that even though (4.16) is not directly related to K_u, the increased K_u could raise both V_{o1} and V_{o2}, resulting in more power dissipation. Also, the output current is less sensitive to x, suggesting that the smaller signal of the two inputs be applied to y for more power savings.

Noise Performance: Noise is another important consideration in designing multipliers, especially for small-signal applications. The total output noise of Fig 4.1 is given by

$$\overline{i_{n;o}^2} = 4\overline{i_{n;lin}^2} + 2\overline{i_{n;sat}^2} = 16KT(g_{ds} + \frac{1}{3}g_m)df \tag{4.17}$$

where

$$g_{ds} = K_l(X - V_o - V_{TH})$$

$$g_m = 2\sqrt{K_l K_u (X - Y - V_{TH})(V_o - Y)}$$

It can be shown from (4.1)-(4.11) that the transconductance of the multiplier is $4K_l$, and hence the input-referred noise voltage is

$$\overline{v_n^2} = \frac{\overline{i_n^2}}{16K_l^2} \propto \frac{kT}{K_l}[(X - V_o - V_{TH}) + \frac{2}{3}\sqrt{\frac{K_u}{K_l}(X - Y - V_{TH})(V_o - Y)}] \tag{4.18}$$

This suggests that K_u / K_l should be increased to improve the noise performance. We should make a tradeoff between power dissipation and noise by selecting a proper value of K_l.

4.3 Experiment and Discussions

In order to estimate the performance of the proposed structure, we used the Cadence Hspice simulator to conduct the experiments on linearity, power dissipation and noise etc. We simulate the circuit in Fig 4.1 using standard 0.35um CMOS technology with supply voltage 1.5 V. Unless otherwise specified, all transistors use the identical size W/L=0.7u/0.35u. Circuit is biased to have the typical values (i.e. X=1.3V and Y=0.2V) with input range of ± 0.2 V for signals x and y (i.e. 2x=2y=0.4V).

Linearity: First we take a look at the DC transfer characteristics of $V_{o1} - V_{o2}$ versus x and y for this structure with X=1.3V and Y=0.2V. The results are plotted in Fig 4.3 (a) for signal x and (b) for signal y. Comparing this two graphs, the linearity of signal x is better than that of signal y, because it has a more linear curve by the DC response.

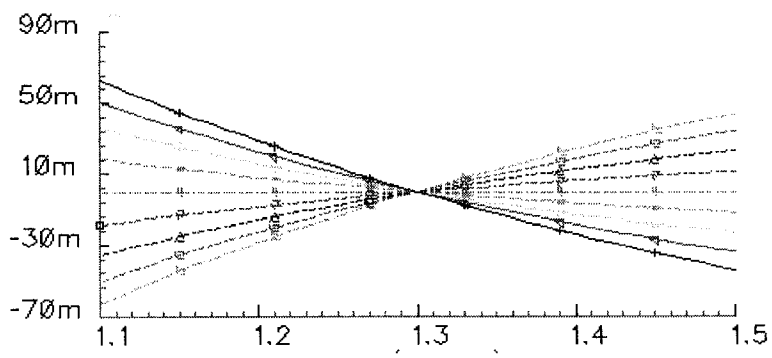


Fig. 4.3 (a) DC response for signal x (with body effect)

When we talk about the linearity, we have to consider the body effect, which is because that the substrate of the MOS transistors is not tied to the source.

Actually, the threshold voltage of the transistor is a function of the total charge in the depletion region (Q_d) as the gate charge must mirror the charge Q_d before the inversion

layer is formed. Thus, as V_B, the substrate voltage drops and Q_d increase, V_{TH} also increase. It can be proved [52] that with body effect, we have

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}) \tag{4.19}$$

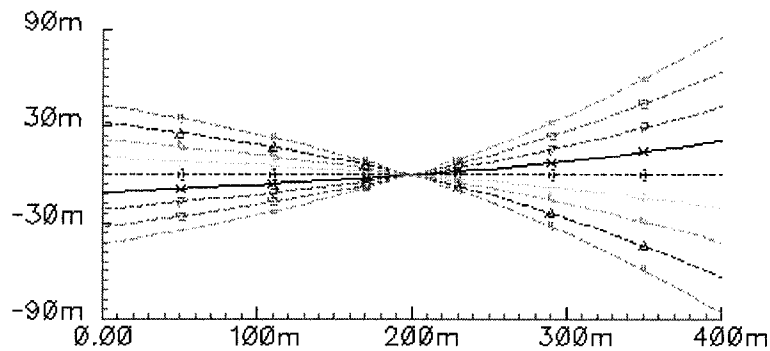


Fig. 4.3 (b) DC response for signal y (with body effect)

Therefore, because of the body effect, the linearity would become worse. Fig 4.4 shows the linearity error of signal x and signal y with and without body effect when the measured signal increased from 0 to 0.2V. And also, from the two graphs, we see that the linearity error of y is more than that of x.

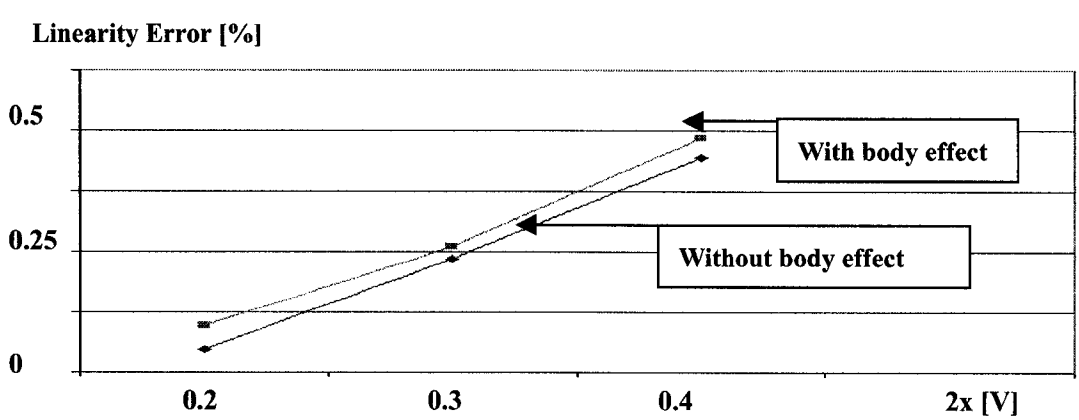


Fig. 4.4 (a) The linearity error of signal x with and without body effect.

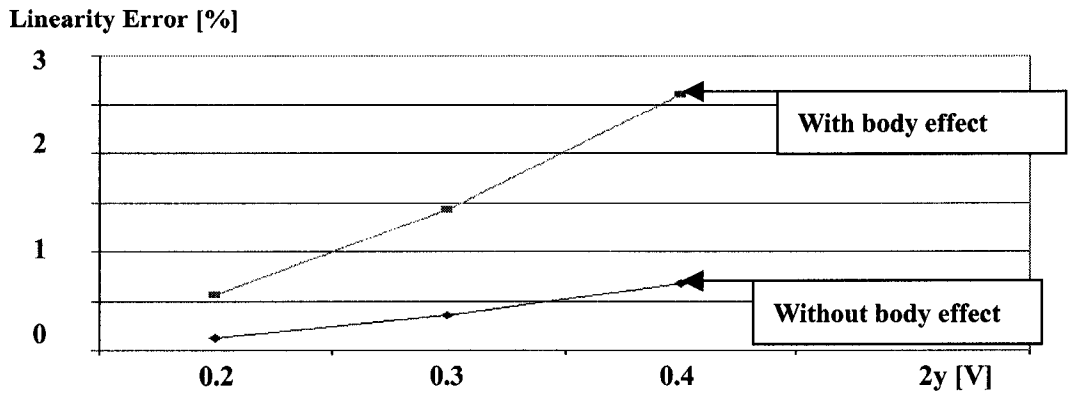


Fig. 4.4 (b) The linearity error of signal y with and without body effect.

Power Consumption: As we know that we could use the total current to represent the power consumption, we do the simulation with different parameters and see what happens about the total current. In Fig 4.5 (a), with the increase of the DC bias of (X-Y), the total current increased, which verifies our analysis in the power performance analysis in section 4.2, equation 4.16.

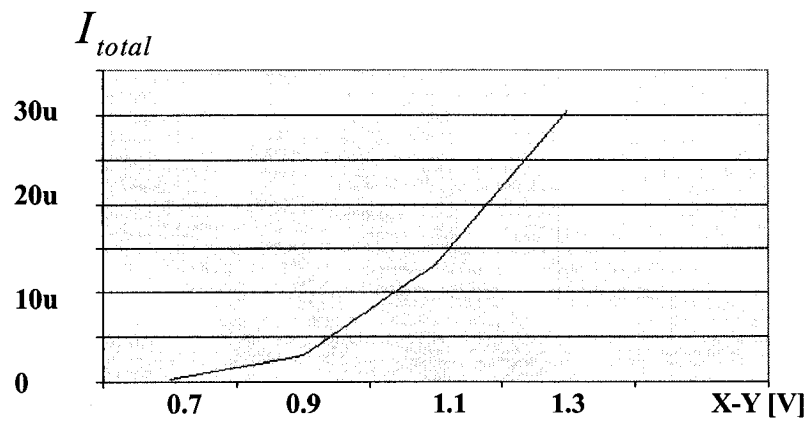


Fig. 4.5(a) Total current versus X-Y

From the Fig 4.5 (b), with the increase of transconductance of the NMOS transistors in the low level, K_l, the total current also increased. Supposing that we have two input signals which have different magnitudes, how do we distribute them, that is, which is

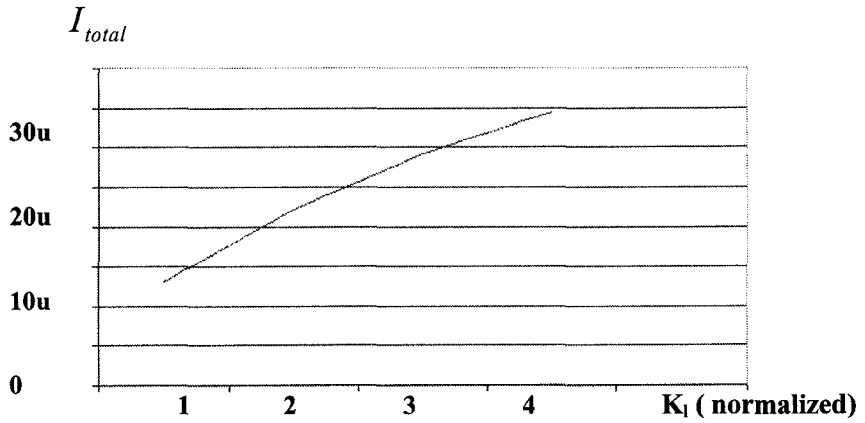


Fig. 4.5(b) Total current versus K_l

used as x and which is y? From the analysis in the last section, we know that the total current has no relationship with signal x, so we could use the signal with bigger magnitude as x and the other as y (distribution 1) in order to decrease the total current. Fig 4.5 (c) shows us this characteristic by different distribution.

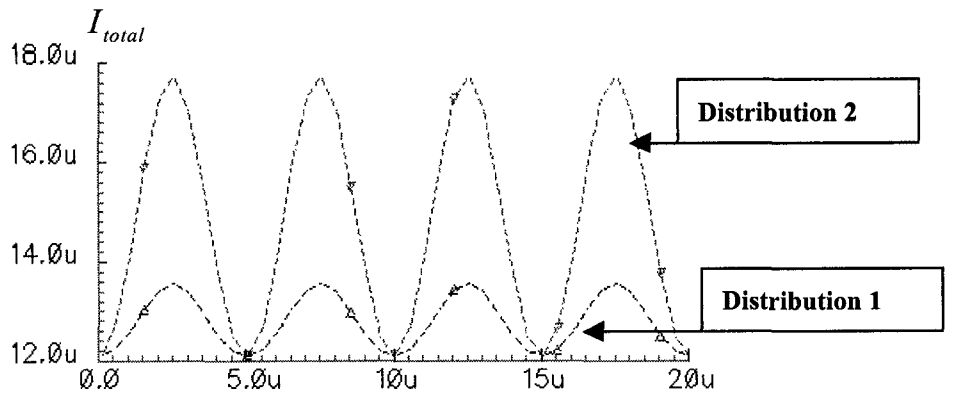


Fig. 4.5(c) Total currents for different signal distribution

Noise Performance: From our previous discussion, we know that the input-referred noise have relationship with the DC bias of (X-Y) and the ratio of parameters K_u / K_l. By the simulation of noise analysis, we find that in Fig 4.6(a), with the increase of (X-Y),

the input-referred noise increased. And also, in Fig 4.6(b), the noise response increased if we increase the ration of K_u / K_l.

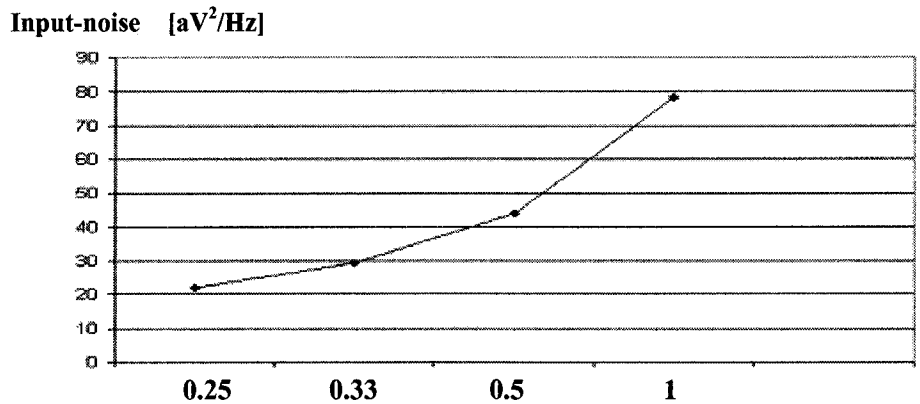


Fig. 4.6(a) The input-referred noise voltage of Fig. 4.1 versus K_u/K_l

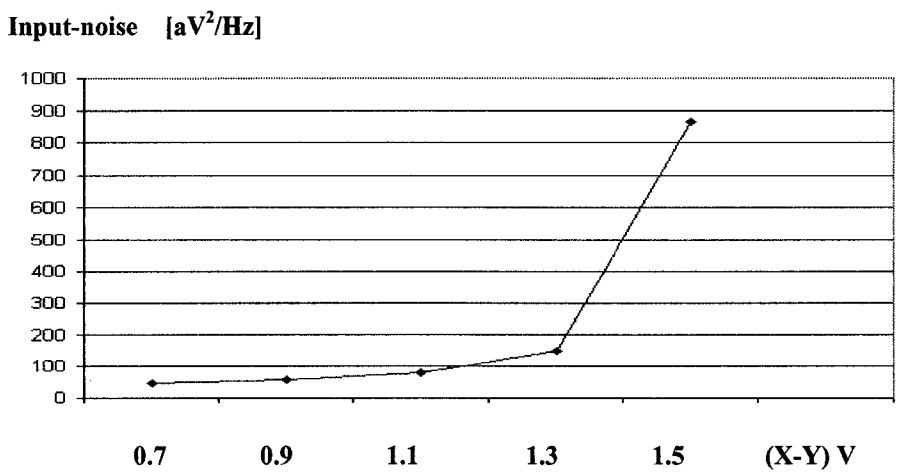


Fig. 4.6(b) The input-referred noise voltage of Fig. 4.1 versus X-Y

4.4 Layout and Extractions

Today's analog circuit design is heavily influenced by layout. The layout of an analog multiplier circuit defines the geometries that appear on the masks used in fabrication. The

geometries include n-well, active, polysilicon, n^+ and p^+ implants, interlayer contacting windows, and metal layers.

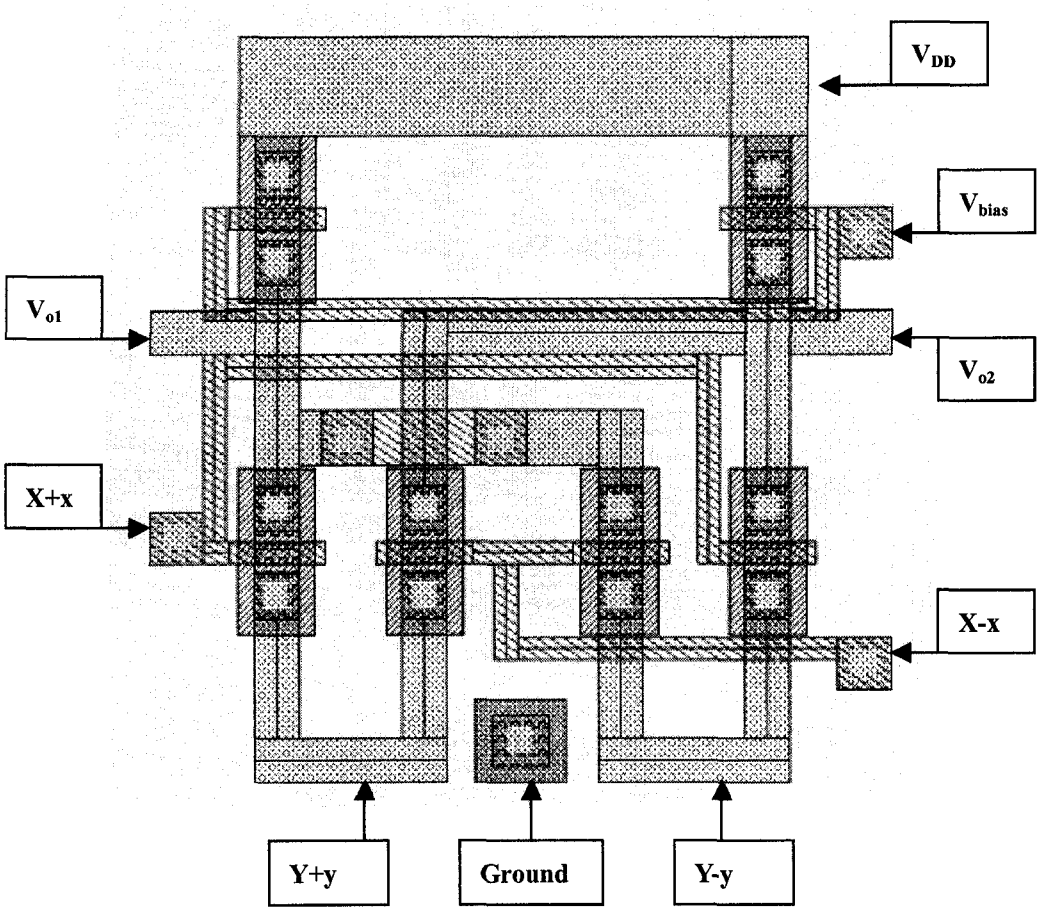


Fig. 4.7 The layout of structure Fig 4.1

For general layout consideration of multiplier structure, we note that: (a) the n-well surrounds the device with enough margin to ensure that the transistor is contained in the well for all expected mislignments during fabrication; (b) each active area (S/D regions and n^+ contact to the well) is surrounded by a proper implant geometry with enough margin; (c) from the fabrication steps, the gate requires its own task; (d) the contact

windows mask provides connection from active and poly regions to the first layer of metal.

For the layout of the structure in Fig 4.1, we consider to (1) decrease the distance among the transistors as long as we could pass the DRC; (2) try to decrease the length of the metal or polysilicon to decrease the parasitic resistors and capacitors involved; (3) for the differential structure, try to make involved parasitic resistors and capacitors symmetric.

We use 0.35um CMOS technology for our layout design. 6 nfet cells from the pcell library are used as transistors. The estimated area cost is only 12u*12u. The substrate of the circuit is connected to the ground. The total layout of this structure is shown above in Fig 4.7.

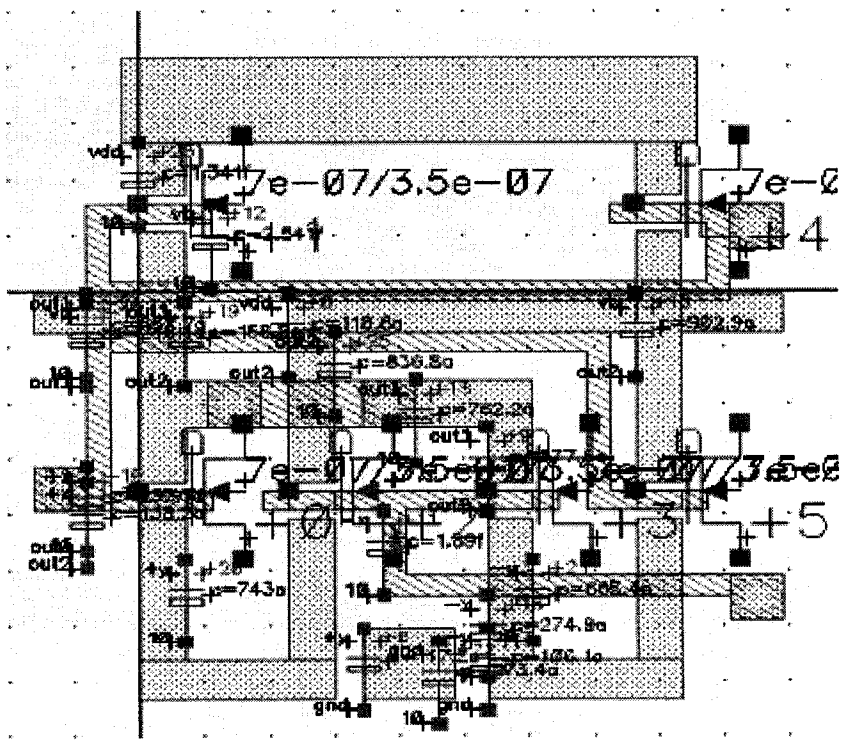


Fig. 4.8 The extracted structure of Fig 4.1

When we design the layout of the structure, we have to do the DRC (design rule check) at every step of the design to guarantee that our design comforts the design rules for CMOS 0.35u technology. In the schematic level, we only consider the devices that we used in the structure, and we suppose that there are no involved resistors or capacitors due to the connection. But in the layout level, we use all kinds of metals and polysilicons to connect devices in the circuit, which will apparently change the performance of the circuit. We would get different result in the layout level from that in the schematic level. By the extractor tool in cadence, the computer can find the involved resistors and capacitors for us automatically and we could get a new model of the circuit in the layout level and have more accurate simulation result.

Fig 4.8 is the extracted structure of Fig 4.1. We could find that, after the extraction, more resistors and capacitors are added to the previous layout structure. We have to use this changed structure to do the simulation for different performance analysis to see what is the difference.

The difference of total current has been shown in Fig 4.9. We could see that after the layout and extraction, the total current increased because of the involved resistors and capacitors.

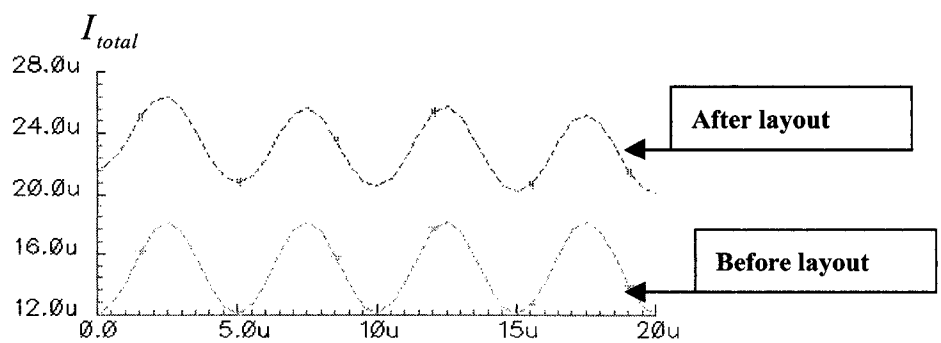


Fig. 4.9 The comparison of total current before and after layout

And also, when we do the simulation of AC analysis after layout. We find that the bandwidth of AC response decreased a little bit. That is the result of the parasitic capacitors from the polysilicons and metals for connection in the layout level. We could find this characteristic from Fig 4.10.

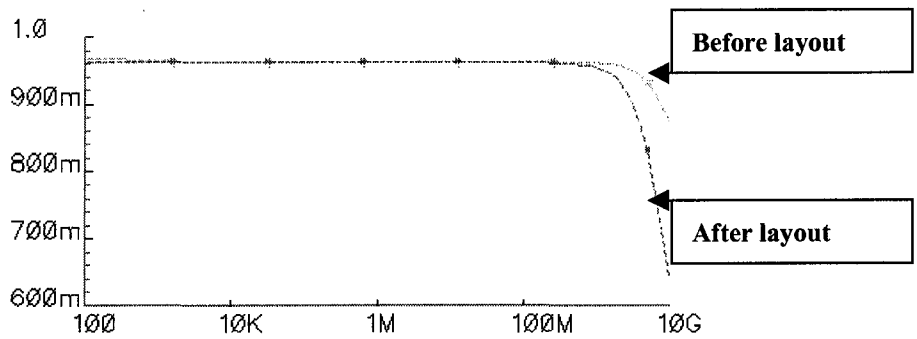


Fig. 4.10 The comparison of AC response before and after layout

Now we talk about a very important performance parameter, THD (total harmonic distortion). THD is the ratio of the sum of the powers of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency. We use it to calculate the distortion of AC signal not only for the DC linearity, but also for the AC linearity. Fig 4.11 (a) shows the THD of signal x with the increase of frequency before layout and after layout, while Fig 4.11 (b) is for the THD of signal y with the increase of frequency before layout and after layout. We find that, after the layout and extraction, the THD increases for both input signals. But we realized that this increase has no influence for low frequencies (0-100K) and has no big influence for middle frequencies (100K-10M). However, in the high frequency region, the THD deteriorates apparently after the layout, which make this multiplier structure a bad choice for high frequency application.

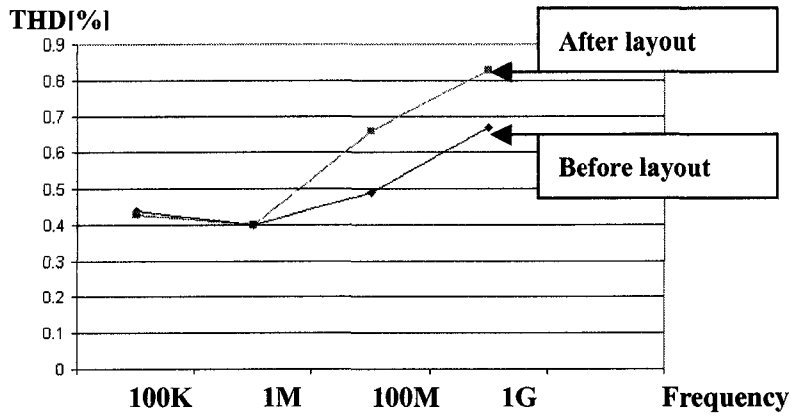


Fig. 4.11 (a) The comparison of THD for signal 2x=0.4V before and after layout with frequencies.

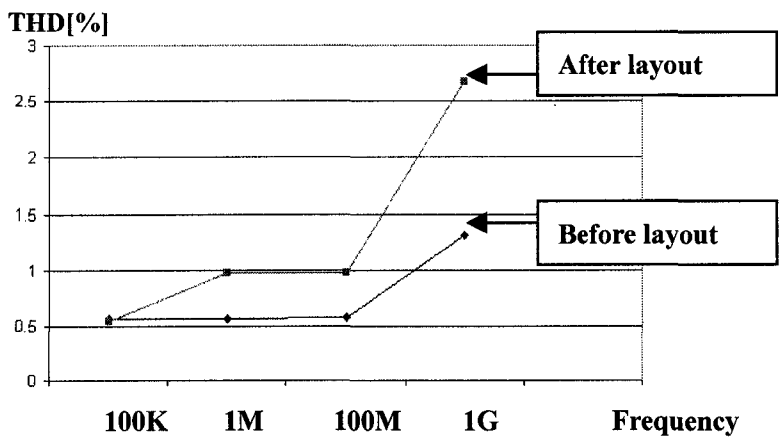


Fig. 4.11 (b) The comparison of THD for signal 2y=0.4V before and after layout with frequencies

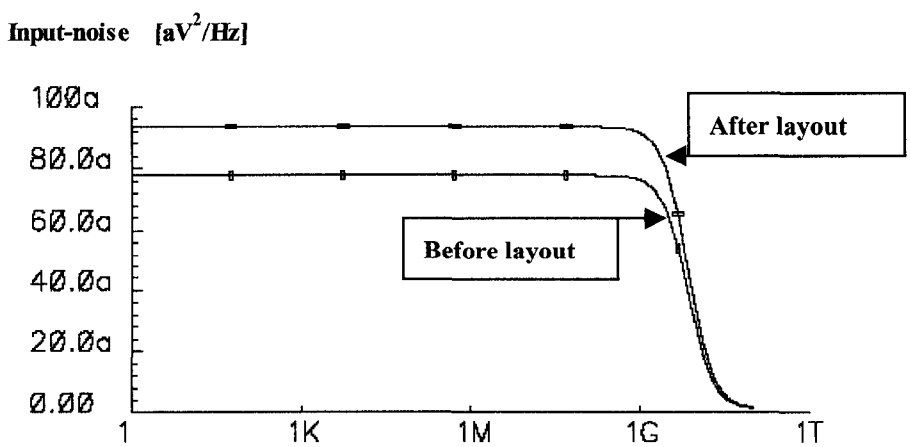


Fig. 4.12 The comparison of input-noise before and after layout with frequencies

For the input-noise simulation, we find that the noise increased after layout, which is shown in Fig 4.12. That is because in the layout level, we have to consider the involved resistors and capacitors due to the connection, which deteriorates the noise performance. But the increase of input-noise in the layout level has no big influence on the circuit performance since normally the input signals could not be very small.

Generally, after the layout, most performance of circuit might be degraded. But from our simulation and experiments, the performance of our circuit in the layout level still satisfies our expectation.

CHAPTER 5

SECOND ANALOG MULTIPLIER STRUCTURE

In chapter 4, a low power and low noise analog multiplier was introduced. We only use 6 NMOS transistors for that structure, which guaranteed very small area for the fabrication. But from the simulation result, we found that the linearity error of signal y was as high as 2.6 % maximum when y=0.2V, Y=0.2V with body effect considered. The high linearity error involved would be a problem, especially in the application where high accuracy is needed.

That high linearity error, as we found from our analysis, is because of the body effect. With the change of signal y, the threshold voltage V_{TH} also changed, which deteriorates the linearity of signal y.

And also, we try to do more work to decrease the total current, as the low power design is the latest trend. We realized that the transconductance parameter of PMOS transistors is much smaller than that of NMOS. Therefore, with the same input range, if we use the PMOS transistors, we could have much smaller total current. But the use of PMOS also brings us the worse linearity, which verified the tradeoff between the power consumption and linearity again. Since the MOS transistors working in the saturation region can bring more current compared with the transistors operating in the linear region, we consider to use the PMOS transistors, when saturation region operation is needed, while put others in the linear region, in order to get a good equilibrium between linearity and power dissipation.

5.1 Circuit Topologies and Theoretical Analysis

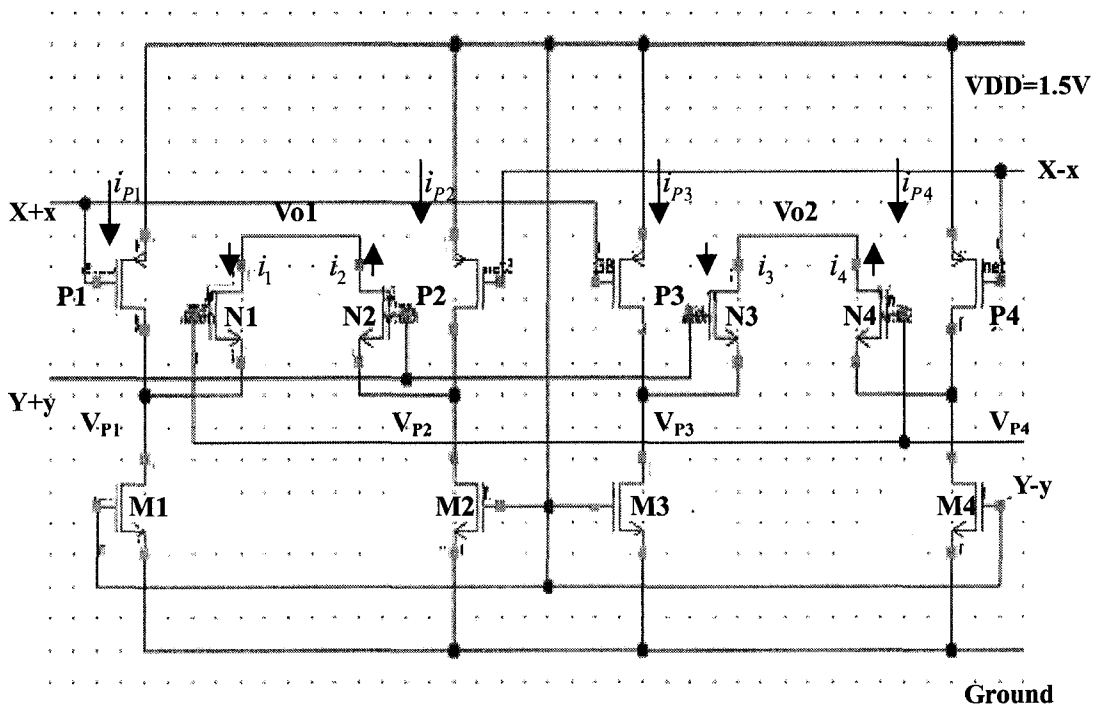


Fig. 5.1 Our second CMOS analog multiplier

In this chapter, we talk about a new analog multiplier structure. Fig. 5.1 shows the proposed CMOS multiplier structure, which consists of 4 PMOS transistors (P1-P4) operating in the saturation region and 8 NMOS transistors (N1-N4 and M1-M4) in their linear region. Assuming that all transistors in Fig. 5.1 are biased to operate in a proper (linear or saturation) region, we show in the following that this topology achieves multiplication.

Assuming that (a) the transistors in Fig. 5.1 have same threshold voltage, i.e., V_{THN} for NMOS and V_{THP} for PMOS, and (b) the P1-P4, N1-N4, and M1-M4 have transconductance parameter K_P, K_N and K_M, respectively, we have

$$i_1 = K_N[(Y+y-V_{P1}-V_{THN})(V_{O1}-V_{P1})-\frac{1}{2}(V_{O1}-V_{P1})^2] \tag{5.1}$$

$$i_2 = K_N[(Y-y-V_{O1}-V_{THN})(V_{P2}-V_{O1})-\frac{1}{2}(V_{P2}-V_{O1})^2] \tag{5.2}$$

$$i_3 = K_N[(Y - y - V_{P3} - V_{THN})(V_{O2} - V_{P3}) - \frac{1}{2}(V_{O2} - V_{P3})^2] \tag{5.3}$$

$$i_4 = K_N[(Y + y - V_{O2} - V_{THN})(V_{P4} - V_{O2}) - \frac{1}{2}(V_{P4} - V_{O2})^2] \tag{5.4}$$

For the 4 PMOS transistors, we have

$$i_{P1} = \frac{1}{2}K_P(V_{DD} - X - x - |V_{THP}|)^2[1 + \lambda(V_{DD} - V_{P1})] \tag{5.5}$$

$$i_{P2} = \frac{1}{2}K_P(V_{DD} - X + x - |V_{THP}|)^2[1 + \lambda(V_{DD} - V_{P2})] \tag{5.6}$$

$$i_{P3} = \frac{1}{2}K_P(V_{DD} - X - x - |V_{THP}|)^2[1 + \lambda(V_{DD} - V_{P3})] \tag{5.7}$$

$$i_{P4} = \frac{1}{2}K_P(V_{DD} - X + x - |V_{THP}|)^2[1 + \lambda(V_{DD} - V_{P4})] \tag{5.8}$$

The transistors M1-M4 can be considered as the resistors with resistance approximately equal to

$$R_{ON} \approx \frac{1}{K_M(V_{DD} - V_{THN})} \tag{5.9}$$

This leads to an almost linear relationship between the drain current and voltage for the M1-M4. And also, we have

$$i_{P1} + i_1 = i_{M1} \tag{5.10}$$

$$i_{P2} - i_2 = i_{M2} \tag{5.11}$$

$$i_{P3} + i_3 = i_{M3} \tag{5.12}$$

$$i_{P4} - i_4 = i_{M4} \tag{5.13}$$

Solving the equations above with $i_1 = i_2$ and $i_3 = i_4$ gives the following approximate result:

$$V_{O1} - V_{O2} \propto \frac{K_P}{K_N K_M} xy \tag{5.14}$$

which is a multiplication of two input signals, x and y.

The advantage of this structure is that only PMOS transistors operate in saturation region. Therefore, we can achieve a larger input range. In other words, given same input range, a

lower supply voltage can be applied. The transistors P1-P4 in saturation region push the V_{P1}-V_{P4} down, increasing the input ranges for the signal y.

For a given DC bias, the output range of the multiplier is influenced by $K_P/(K_N K_M)$. However, there is a maximum value for $K_P/(K_N K_M)$ in order to keep M1-M4 and N1-N4 operating in the linear region. While the circuit exhibits the ability of canceling nonlinearity, the approximation in (5.9) introduces a linearity error. The body effect of transistors N1-N4 has been ignored in the above analysis. Other issues such as temperature and possible device mismatch are also a contributing factor to the linearity error.

To realize multiplication, proper bias arrangements for all transistors in Fig. 5.1 are required. The bias conditions for Fig. 2 can be written as:

$$V_P - |V_{THP}| \le X \pm x \le V_{DD} - |V_{THP}| \qquad \text{for P1-P4} \qquad (5.15)$$

$$Y \pm y \ge V_O + V_{THN} \qquad \text{for N1-N4} \qquad (5.16)$$

The bias voltage of M1-M4 is chosen to be V_{DD} in order to make V_P as low as possible, allowing P1-P4 for a higher input range. Typical values to be used are: V_{DD} = 1.5 V, X =0.5 V, Y = 1.5 V, V_{THP} = 0.7 V and V_{THN} = 0.6 V . When all transistors use the same size of W/L=0.7μm/0.35μm with $x = y = 0$, V_{O1} and V_{O2} turn out to be 16.1 mV.

5.2 Performance Analysis

In this section, we give a quantitative analysis on power consumption and noise for the proposed multiplier. The other metrics will be discussed in next section.

Power Consumption: Given a constant supply voltage, power consumption of Fig. 5.1 can be estimated by looking at the total output current which is given by $\mathbf{i}_{total} = i_{P1} + i_{P2} + i_{P3} + i_{P4}$. It is interesting to see that the currents i_1-i_4 have nothing to do with the total output current. From equations (5.5)-(5.8), we have

$$i_{total} = \frac{1}{2}K_P(V_{DD} - X - x - |V_{THP}|)^2[1+\lambda(V_{DD} - V_{P1})] + \frac{1}{2}K_P(V_{DD} - X + x - |V_{THP}|)^2[1+\lambda(V_{DD} - V_{P2})]$$
$$+\frac{1}{2}K_P(V_{DD} - X - x - |V_{THP}|)^2[1+\lambda(V_{DD} - V_{P3})] + \frac{1}{2}K_P(V_{DD} - X + x - |V_{THP}|)^2[1+\lambda(V_{DD} - V_{P4})]$$

(5.17)

Since V_{P1}~V_{P4} is very small compared with the input signals (when the circuit is properly biased), we have the following approximate result:

$$i_{total} \propto 2K_P[(V_{DD} - X - |V_{THP}|)^2 + x^2]$$

(5.18)

We see that the power dissipation has nothing to do with the signal y and DC bias Y for transistors N1-N4. But if K_P increases, the current would increase. A large value of y, however, will degrade the linearity, as can be seen in the next section.

Noise Performance: Noise is another important consideration in designing multipliers. The total output noise of Fig. 5.1 is given by

$$\overline{i_{n;o}^2} = 8\overline{i_{n;lin}^2} + 4\overline{i_{n;sat}^2} = 16kTg_{ds1}df + 16kTg_{ds2}df + \frac{32}{3}kTg_m df \qquad (5.19)$$

where we notice that

$$g_{ds1} = K_N(Y - V_O - V_{THN})$$

$$g_{ds2} = K_M(V_{DD} - V_P - V_{THN})$$

$$g_m = K_P(V_{DD} - X - |V_{THP}|)$$

Then, the total input noise would be

$$\overline{v_{n;o}^2} = 8\overline{v_{n;lin}^2} + 4\overline{v_{n;sat}^2} \propto 16kT\frac{K_P^2}{K_M^2}g_{ds1}df + 16kT\frac{K_P^2}{K_N^2}g_{ds2}df + \frac{32}{3}kT\frac{K_P^4}{K_M^2K_N^2}g_m df \qquad (5.20)$$

This suggests that K_M, K_N should be increased and K_P should be decreased to improve the noise performance. Also, we realized that if we increased the difference of DC bias (Y-X), because the value of g_{ds1} and g_m changed, the input -referred noise would also be changed.

5.3 Experiment and Discussions

In order to estimate the performance of the proposed structure in Fig 5.1, we used the Cadence Hspice simulator to conduct the experiments on linearity, power dissipation and noise etc. We simulate the circuit by using standard 0.35um CMOS technology with supply voltage 1.5 V. Unless otherwise specified, all transistors use the identical size W/L=0.7u/0.35u. Circuit is biased to have the typical values (i.e. X=0.5V and Y=1.5V) with input range of ±0.2 V for signals x and y (i.e. 2x=2y=0.4V).

Linearity: First we look at the DC transfer characteristics of $V_{o1} - V_{o2}$ versus x and y for this structure with X=0.5V and Y=1.5V. The results are plotted in Fig 5.2 (a) for signal x and (b) for signal y.

Fig 5.3 shows the linearity error of signal x and signal y with and without body effect when the measured signal increased from 0 to 0.2V. We notice that there is no body effect for signal x. Therefore, the linearity of signal x keep in a good level. But for signal y, the linearity error increased because of the body effect.

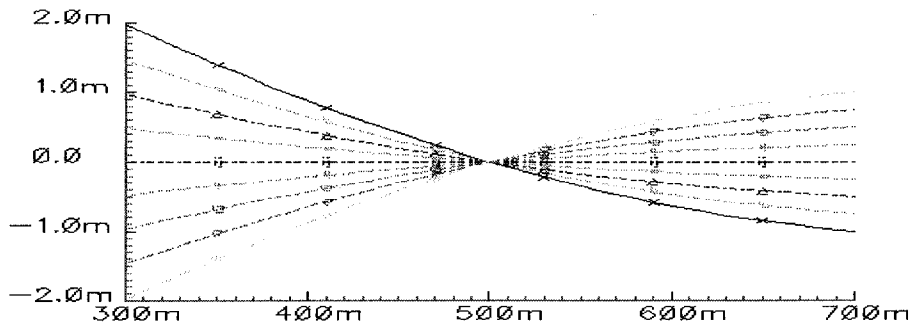


Fig. 5.2 (a) DC response for signal x (with body effect)

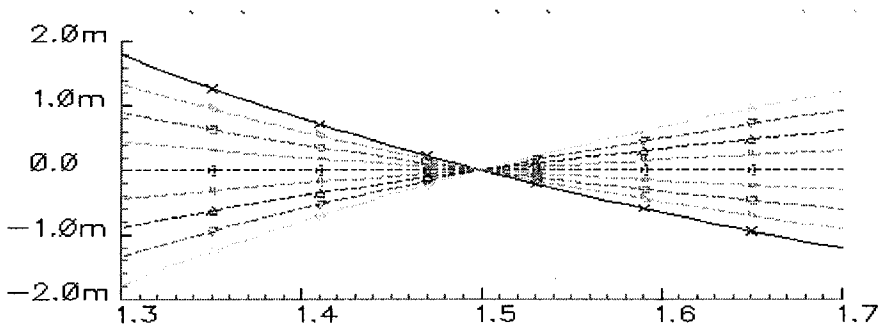


Fig. 5.2 (b) DC response for signal y (with body effect)

Fig 5.3 shows the linearity error of signal x and signal y with and without body effect when the measured signal increased from 0 to 0.2V. We notice that there is no body effect for signal x. Therefore, the linearity of signal x keep in a good level. But for signal y, the linearity error increased because of the body effect.

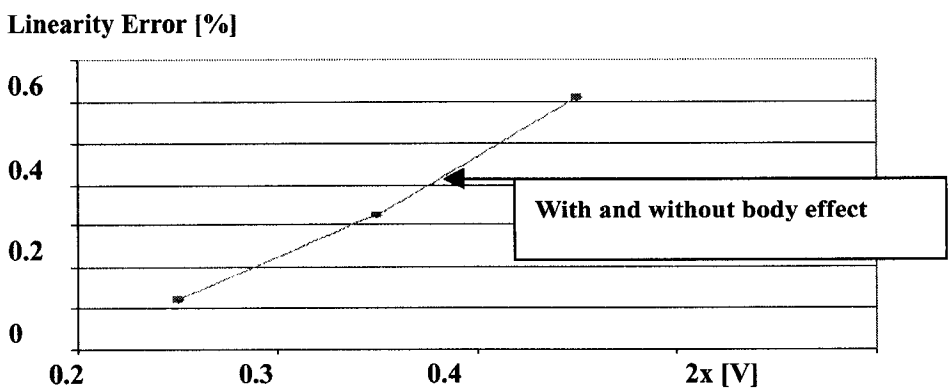


Fig. 5.3(a) Linearity error of signal x with 2y=0.4V (with and without body effect)

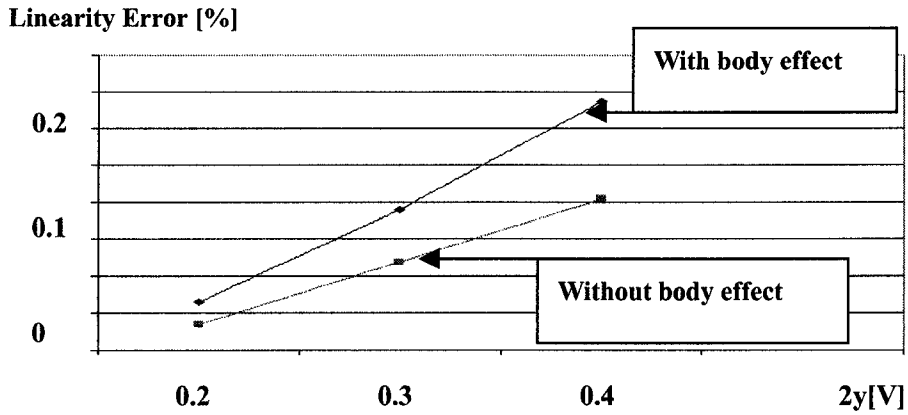


Fig. 5.3(b) Linearity error of signal y with 2x=0.4V (with and without body effect)

Power Dissipation: From our previous analysis about the total current, we know that the I_{total} would increase if the size of K_p (the transconductance parameter of PMOS transistors) increases. And also, the total current will decrease if we increase the DC bias of signal x. Fig 5.4 and Fig 5.5 show us these characteristics.

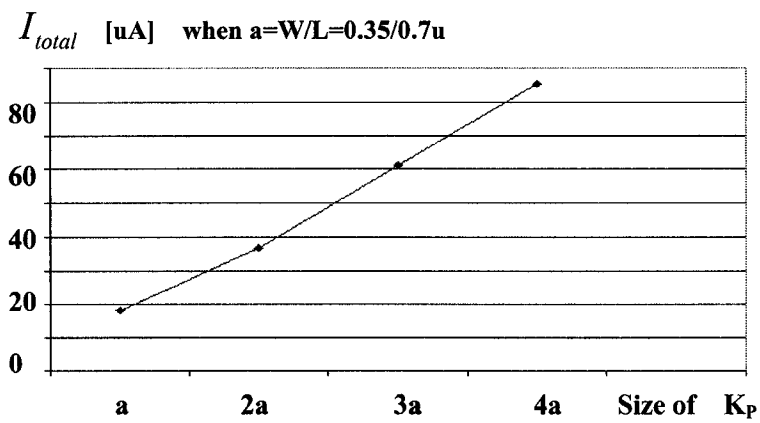


Fig. 5.4 The total current versus K_P

But on the other hand, as we can see from the equation (5.18), the total current has no relationship with DC bias Y (see Fig 5.6) and signal y (see Fig 5.7). This is a very important characteristic for this structure. If, because of the requirement of specific

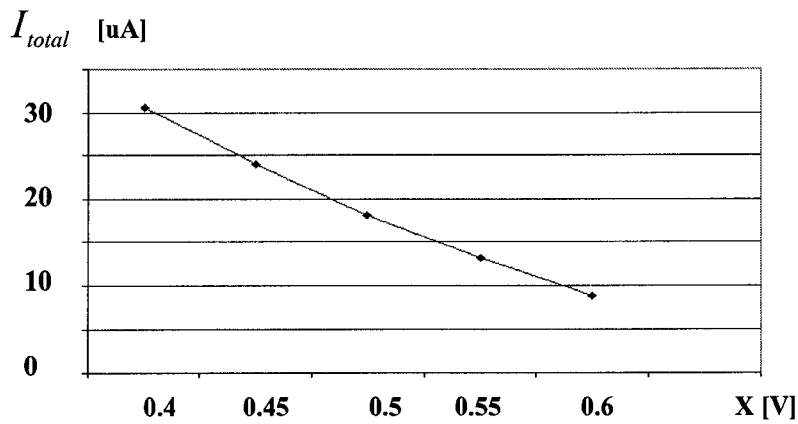


Fig. 5.5 Total current versus X

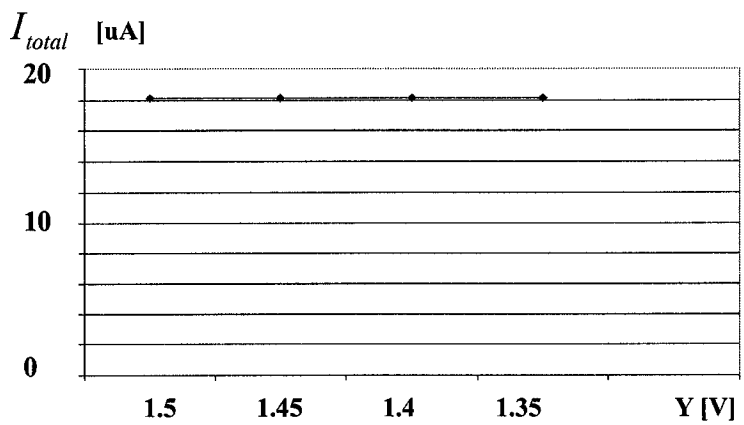


Fig. 5.6 Total current versus Y

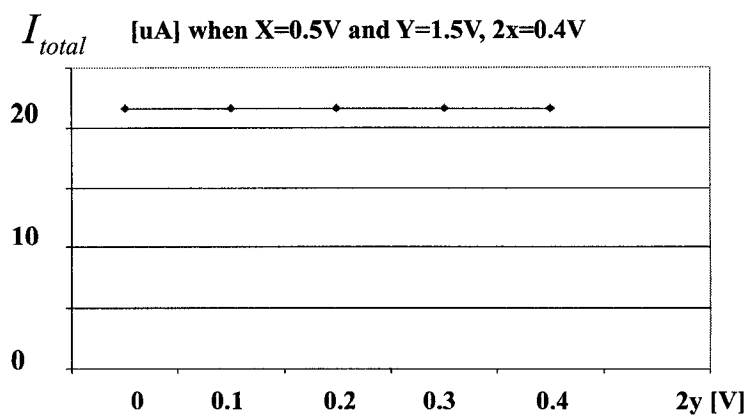


Fig. 5.7 Total current versus 2y

application, we have to change some parameters to get good performance, we could change the DC bias of Y or even the magnitude of signal y, but this change will not deteriorate the performance of total current, which give us more freedom for our design in different application.

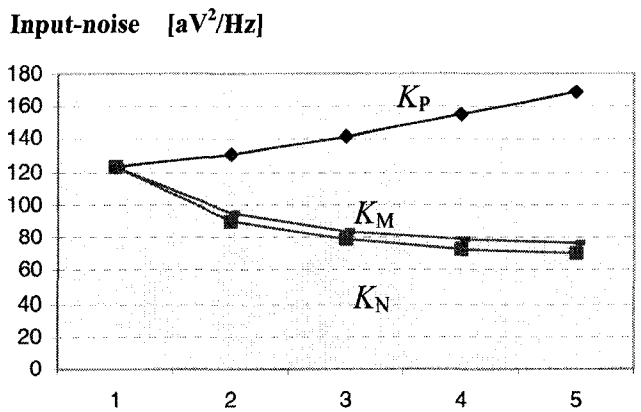


Fig. 5.8 The input-referred noise voltage of Fig. 5.1 versus K_P, K_M and K_N

Noise Performance: As we know from our analysis in last section, if we increase K_P (when keep K_M and K_N the same), the input-noise will increase; however, if we increase K_M or K_N when keeping other sizes unchanged, we could decrease the input-referred noise. Simulation results of noise analysis in Fig 5.8 verified our analyses.

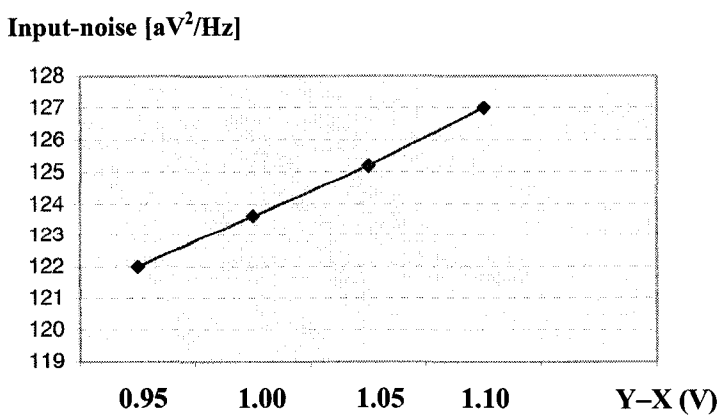


Fig. 5.9 The input-referred noise voltage of Fig. 5.1 versus Y-X

Fig 5.9 tells us that if we increase (Y-X), the input-referred noise increase, which is exactly what we predicted in last section's analysis.

5.4 Layout and Extractions

The layout of Fig 5.1 is shown in Fig 5.10. 4 PMOS are put in the n-well and other 8 NMOS are put in the substrate directly. 4 input terminals are connected to the edge of the circuit by polysilicon. The substrate of the PMOS is connected to the supply voltage (V_{DD}), while the bodies of NMOS are connected to the ground.

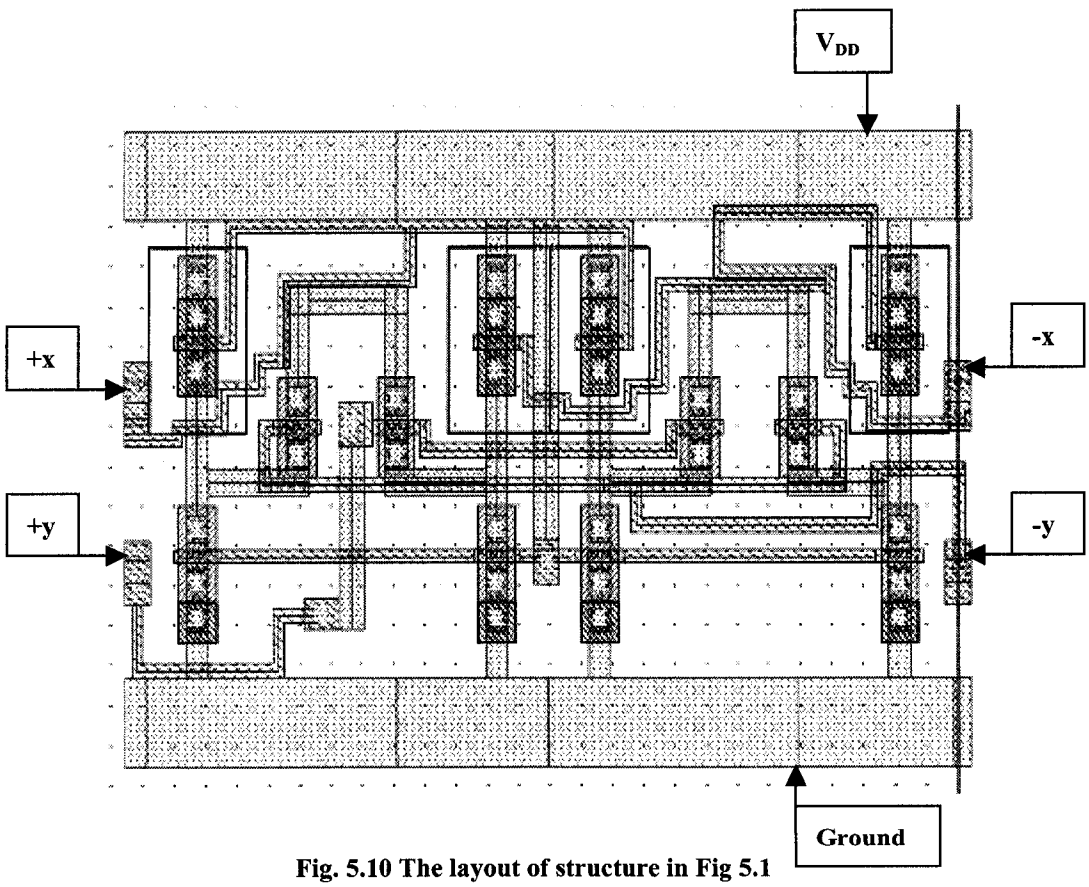


Fig. 5.10 The layout of structure in Fig 5.1

After the extraction, we find that more parasitic resistors and capacitors added to the circuit. Therefore, the performance of the circuit in the layout level could be different

from the circuit in the schematic level, where we suppose all the parasitic devices from the connection is zero. Fig 5.11 shows us the extracted circuit.

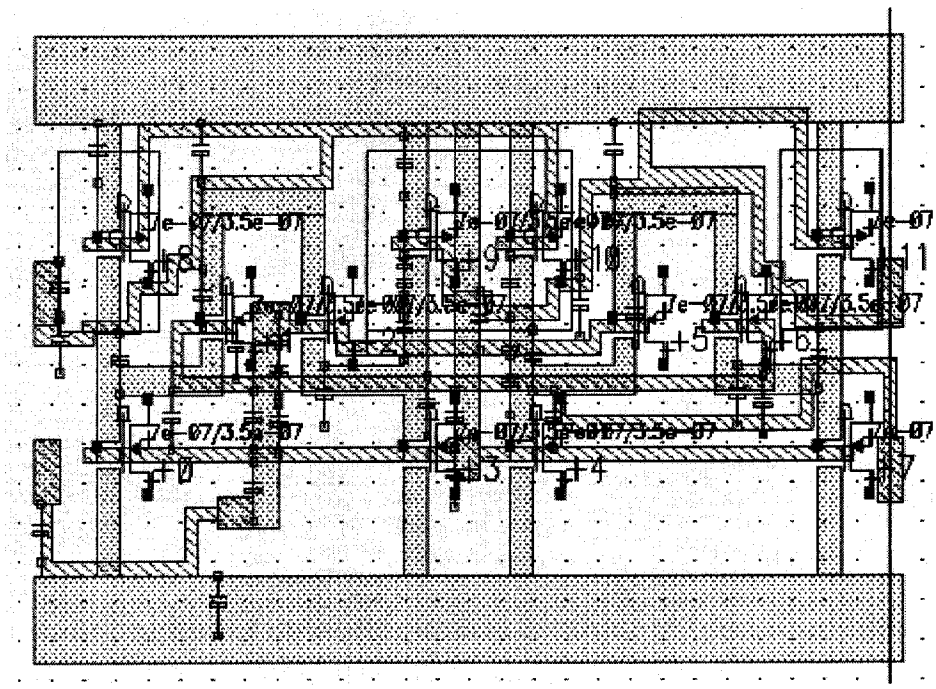


Fig. 5.11 The extracted circuit of our second analog multiplier

Now we give the comparison of total current before layout and after layout by Hspice simulation in Fig 5.12. There is no remarkable increase of the total current, as the increase of parasitic resistors has no big influence to the whole circuit.

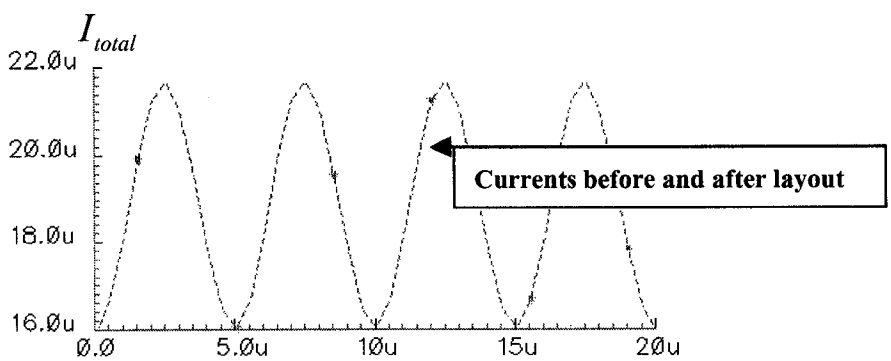


Fig. 5.12 The comparison of total currents before and after layout

In Fig 5.13, the AC response of the circuit changed after the layout compared with the circuit before layout. And also, after the layout, the bandwidth decreased a little bit.

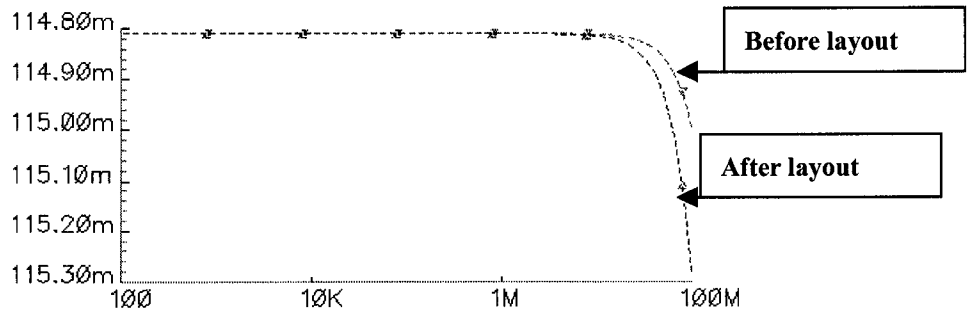


Fig. 5.13 The comparison of AC response before and after layout

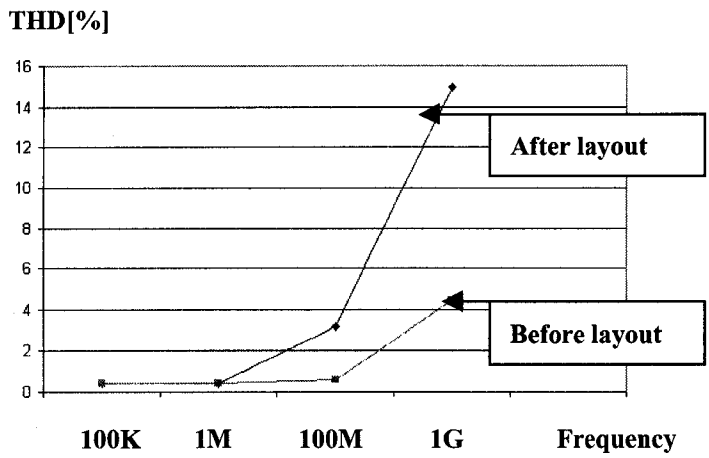


Fig. 5.14 (a) The comparison of THD for signal 2x=0.4V before and after layout with frequencies

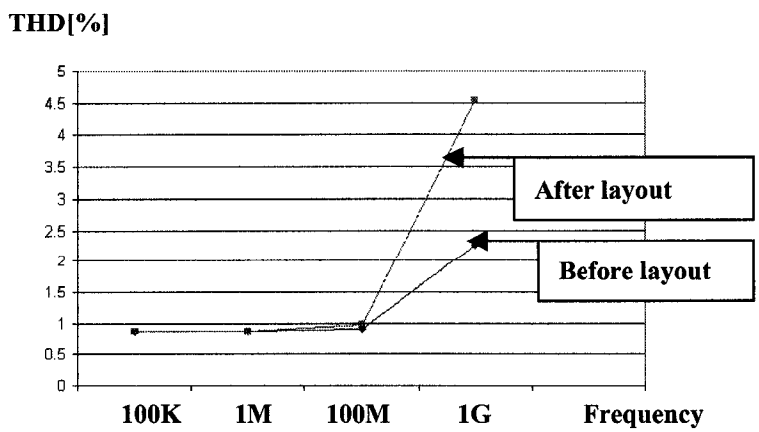


Fig. 5.14 (b) The comparison of THD for signal 2y=0.4V before and after layout with frequencies

For the total harmonic distortion (THD), we find from Fig 5.14 (a) and (b), that the linearity error increased in the high frequency domain, make the structure unsuitable for HF application when high accurateness is needed.

For the input-noise simulation, we find that the noise increased after layout, which is shown in Fig 5.15. That is because in the layout level, we have to consider the involved resistors and capacitors due to the connection, which deteriorates the noise performance. But the increase of input-noise in the layout level has no big influence on the circuit performance since normally the input signals could not be very small.

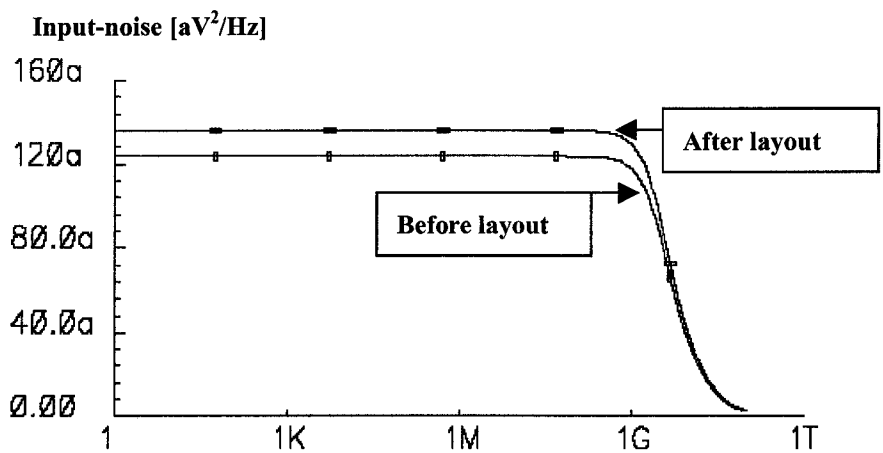


Fig. 5.15 The comparison of input noise before and after layout with frequencies

Generally speaking, after the layout, most performance of circuit might be degraded. But from our simulation and experiments, the performance of our circuit in the layout level still satisfies our expectation.

CHAPTER 6

PERFORMANCE COMPARISON OF DIFFERENT STRUCTURES

In order to estimate the performance of the proposed two structures, we have used *Cadence*'s *HSPICE* simulator to conduct the experiments on linearity, power consumption and noise etc. To ensure a fair comparison, we also simulated the most recommended structure of eight multipliers provided in [51], which was considered to be one of the best multiplier structures as low power and low noise design.

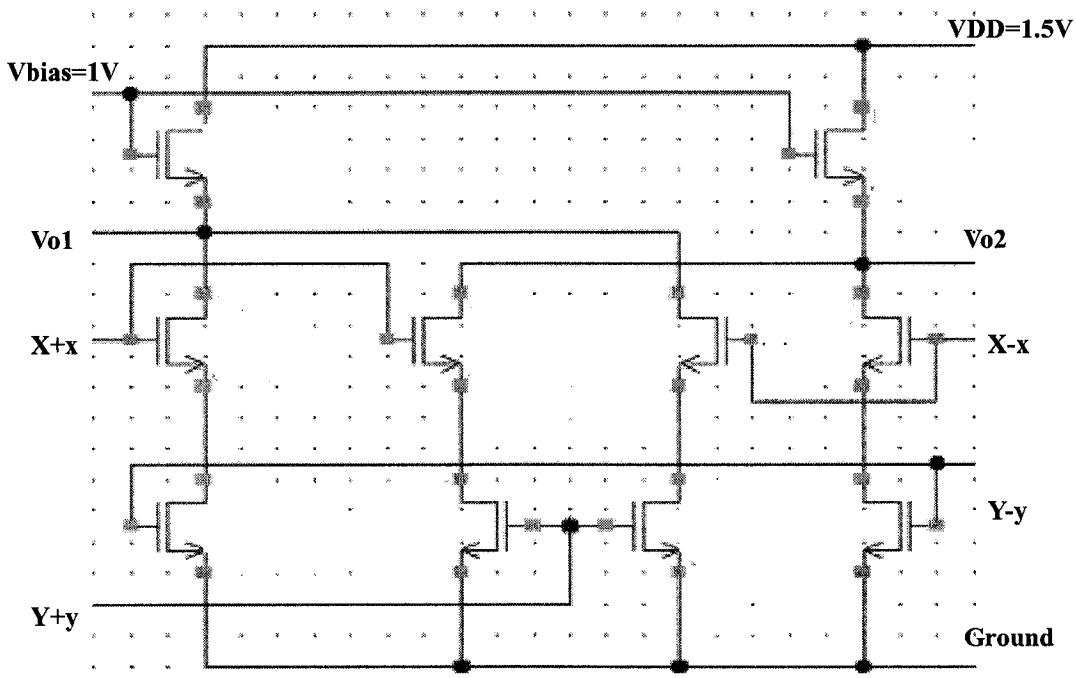


Fig. 6.1 The most recommended multiplier structure by [51]

Actually, we have talked about this structure in section chapter 2, section 3 (Fig 2.7). According to our comparison of most previous structures in this field, we believe this structure is one of the most attractive high-performance multiplier and can be the reference of our research work. For convenience, this structure is redrawn in Fig. 6.1,

where we use 10 NMOS transistors to constitute an analog multiplier. 4 transistors work in the linear region, while another 4 transistors operate in the saturation region and 2 NMOS transistors working in the saturation region in order to get output voltages. For all three circuits in Fig. 4.1, Fig. 5.1 and Fig 6.1, a standard 0.35μm CMOS technology was used with the supply voltage of 1.5 V. Unless otherwise specified, all transistors use the identical size with W/L = 0.7μm/0.35μm. The circuit is biased to have the typical values (in Fig. 6.1, X = 1.3 V and Y = 1.0 V were used) with the input range of ± 0.2 V for both x and y (i.e., $2x = 2y = 0.4$ V).

Linearity Error: First we look at the linearity error of signal x for all the three structures (Fig 4.1, Fig 5.1 and Fig 6.1) in Fig 6.2(a). We find that the linearity error increase with the increase of input range of signal x. Structure in Fig 4.1 and Fig 5.1 have smaller linearity error compared with the structure in Fig 6.1, which is the most recommended one by paper [51]. From this comparison, we could say that our two proposed multiplier structures have less linearity error of x than that one in Fig 6.1.

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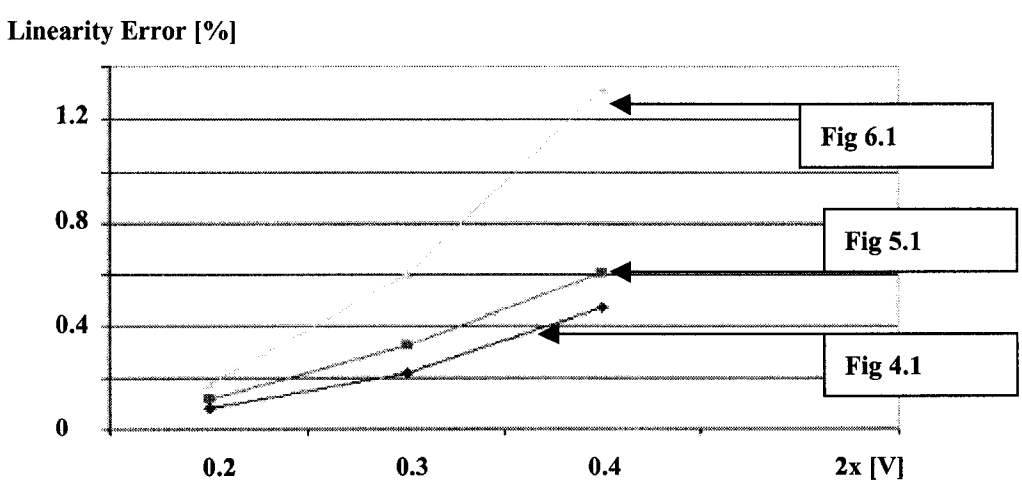


Fig. 6.2(a) The comparison of 3 structures for signal x

However, for the linearity error of signal y of the 3 structures, we have different result.

Fig 6.2(b) shows that our first proposed structure (Fig 4.1) has the worst linearity error of signal y. But our second proposed structure (Fig 5.1) still has better performance of linearity than that of the most recommended one in Fig 6.1

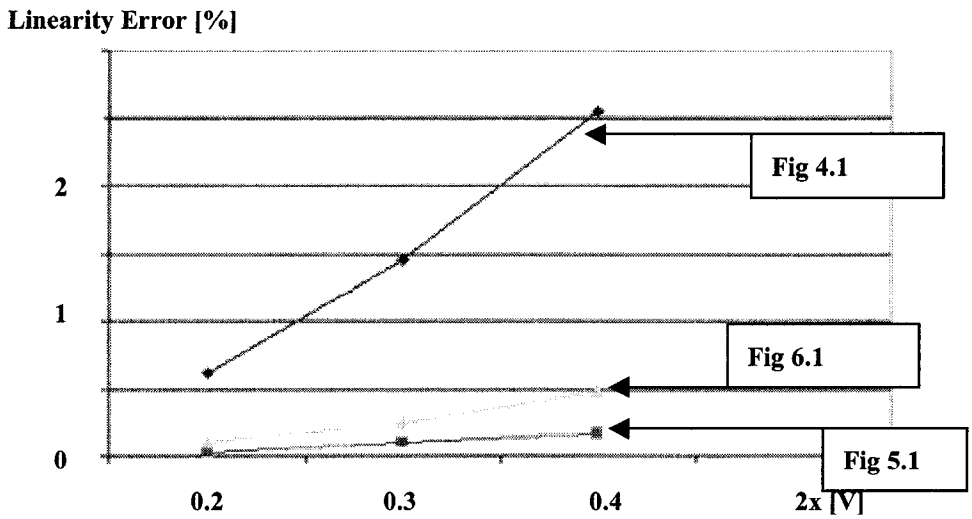


Fig. 6.2(b) The comparison of 3 structures for signal y

Total Harmonic Distortion (THD): Fig 6.3 (a) and (b) show that with the increase of frequency, the THDs of signal x and y increase and deteriorate the linearity. For signal x, the 3 structures have the similar values and trends in low and middle frequency region. While for signal y, our two structures have less THD than the structure in Fig 6.1.

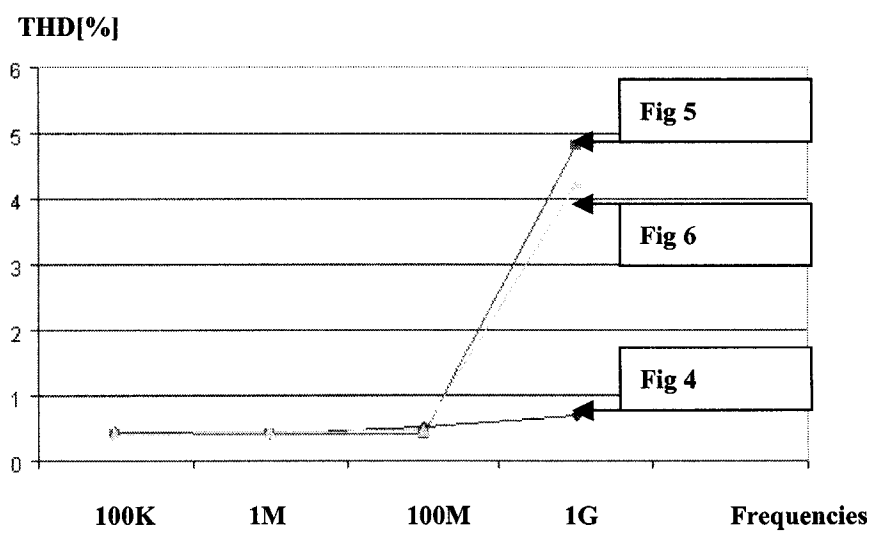


Fig. 6.3(a) The comparison of 3 structures for signal x

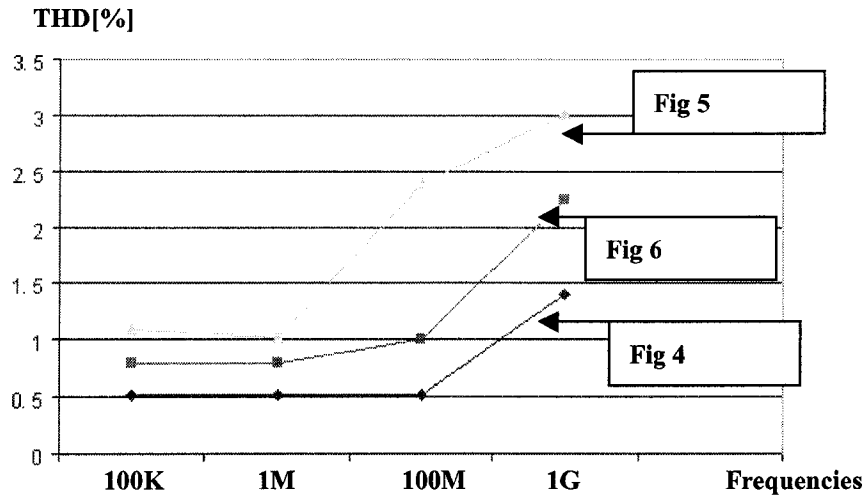


Fig. 6.3(b) The comparison of 3 structures for signal y

Total current: We do the simulation of the total currents of the 3 structures with appropriate bias voltage and input signal x=y=0.2V sine wave in frequency 100K. The result in Fig 6.4 shows us that our proposed 2 structures (Fig 4.1 and Fig 5.1) have only one third of total current of the most recommended one in Fig 6.1. That means if we use the same supply voltage, our 2 structures have much less power dissipation than the structure in Fig 6.1. Therefore, our two structures are low power analog multipliers.

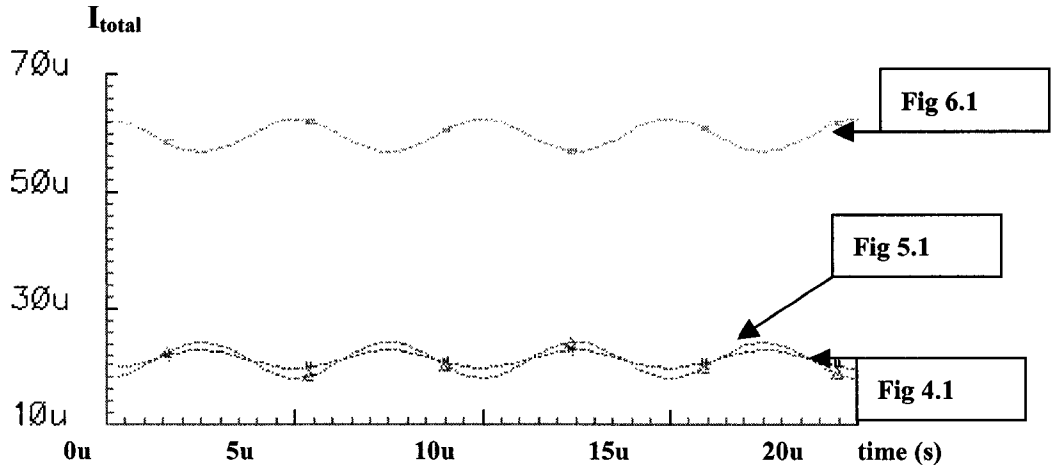


Fig. 6.4 The comparison of total current of 3 structures

Noise Performance: We also do the noise analysis by the *Cadence Hspice*. From Fig 6.5, we find that the structure in Fig 4.1 has less input-referred noise than the other two structures, so it is low noise design of analog multiplier. However, the input-referred noise of structure in Fig 5.1 is more than that in Fig 6.1. I hope I could do more to improve the performance of noise for this structure in the future.

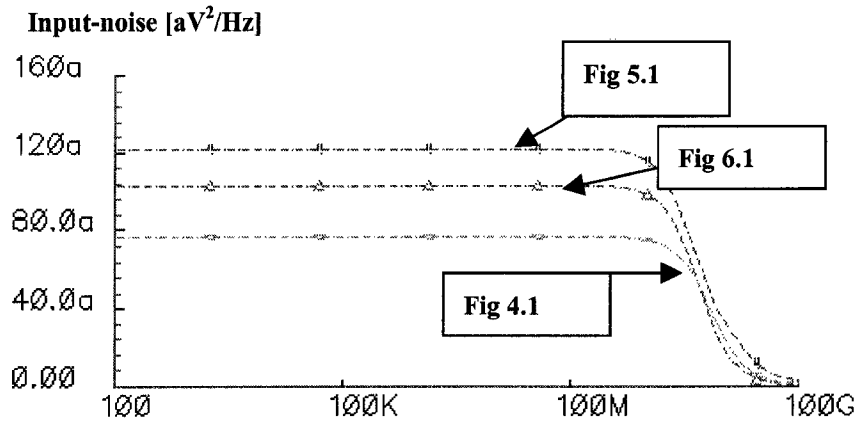


Fig. 6.5 The input -referred noise for 3 structures in different frequencies

We use table 6.1 as a summary of comparison of the 3 structures.

Table 6.1 The different performance comparison of 3 structures

	Our first structure	Our second structure	Recommended by [52]
Linearity error of x	0.5%	0.6%	1.3%
Linearity error of y	2.6%	0.23%	0.5%
THD of x	0.43%	0.4%	0.4%
THD of y	0.51%	0.8%	1.1%
Power dissipation	22.65uW	27.15uW	68.31uW
Input-referred noise	76aV*V	128aV*V	109aV*V
Band width	4.22G	1.98G	1.86G
Number of transistors	6	12	10
Estimated area	12u*12u	27u*16u	
Technology	CMOS 0.35	CMOS 0.35	CMOS 0.35

CHAPTER 7

CONCLUSIONS AND SUGESTIONS FOR FUTURE WORK

In this thesis, we talked about our design work of two analog multiplier structures. Hspice simulator was used to do the simulation about several performance metrics. The simulation results have shown that our multipliers have better performance in terms of power consumption. With the same input range and relatively small input-referred noise, the power dissipation of our two structures is only one third of that of the structure, the most recommended by [51]. Further power reduction could be achieved by fine-tuning design parameters. Therefore, we can say that our two structures are very suitable for application where low power is important consideration.

Throughout the whole design process, we have gotten some experience for analog multiplier design:

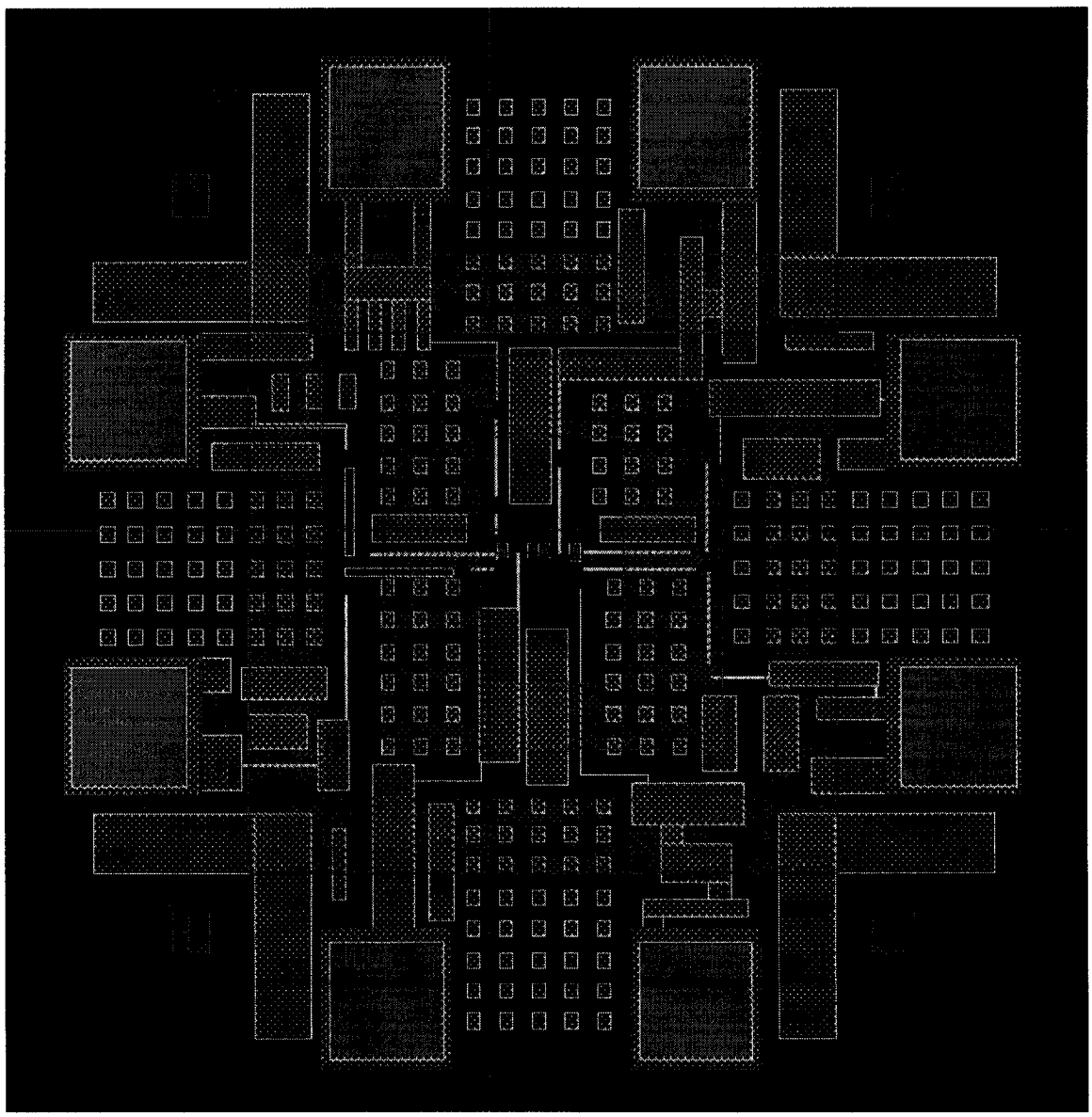
- By Biasing the transistors in the linear region and decreasing the drain-source voltage, we could get low current while at the same time, keeping a relatively wider input range. This is the basic idea of our low power design.
- Proper use of the PMOS transistors can help us decrease the body effect, therefore improve the linearity performance, and bring us less drain current as the transconductance parameter of PMOS are much smaller than that of NMOS.
- Body effect is an important second-order effect which we have to consider for good linearity.
- In the layout level, for the differential structure, try to make involved parasitic resistors and capacitors symmetric.
- Post-layout simulation is important for performance verification.

As we have found from our simulation results, our first proposed structure (Fig 4.1) has more linearity error of signal y, which degrades it from the excellent analog multiplier. Therefore, it is not recommended that we use it in the application where good linearity is the most important consideration.

Our second proposed structure has better linearity and lower power dissipation compared to others. We realize that its noise performance is not as good as the most recommended one in [51]. But considering 20% high input-noise has no remarkable influence on the total performance of multiplier in the actual application, we used it as our most proposed structure and sent the design of this circuit to the CMC for fabrication. The complete physical layout graph can be seen in the appendix (next page). Physical testing will be done when manufacture of this circuit has been finished.

APPENDIX

The design as ICDWRAMR sent to CMC for Fabrication
(The Second Proposed CMOS Analog Multiplier)



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