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Low Power Demodulator Design for RFID Applications

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by

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Low Power Demodulator Design for RFID Applications

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DECLARATION OF CO-AUTHORSHIP / PREVIOUS PUBLICATION

I. Co-Authorship Declaration

I hereby declare that this thesis incorporates material that is result of joint research, as follows:

The primary contributions, experimental designs, data analysis and interpretation were performed by the author under the supervision of Dr. Chunhong Chen. Besides supervision, Dr. Chunhong Chen also provided the author with the project idea, guidance, and financial support.

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Thesis chapter	Publication title	Publication status
Chapters 3-4	Mario Mendizabal and Chunhong Chen, "Low Power Demodulator Using Sub-threshold Design," 2012 IEEE International Symposium on Circuits and Systems	Submitted for publication

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ABSTRACT

Power consumption is a key issue in today's digital and analog design for various portable devices. Radio frequency identification (RFID) is a technology which requires very low power and it uses electromagnetic waves in the radio frequency to transmit the ID of objects. It has a broad range of uses although inventory management and tracking are the most common.

A low power demodulator, part of a RFID transponder operating in the 900 MHz range, is presented using sub-threshold design. Using this technique and working with 90 nm complementary metal-oxide-semiconductor (CMOS) technology, the circuit can operate with a supply voltage as low as 0.3 V, consuming a very small amount of power compared to other demodulators in the literature, making it suitable for ultra-low power applications.

ACKNOWLEDGEMENTS

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CHAPTER I
INTRODUCTION

This chapter is about the radio frequency identification (RFID) standards and its applications. Section 1.1 introduces the RFID system and its operation. Section 1.2 covers the different types of transponders. Section 1.3 shows the frequency range and uses for RFID. Section 1.4 deals with the different modulation schemes that can be used in RFID. Section 1.5 provides a description of the seven major components of a RFID transponder. And finally, Section 1.6 details the objective of this thesis.

1.1 Introduction to RFID Systems

RFID is a technology that uses electromagnetic waves in the radio frequency range to transmit the ID of objects, and can be thought of as a smart barcode system. RFID has been around since the early 1970s, but it hasn't been until recently due to technology advancement in integrated circuits and radios that it's been feasible, mostly because of the size and cost going down drastically. This has made it useable on a large scale, and with increased interest from the industry and government, has made it gain widespread popularity [1].

The whole system consists of three main blocks:

- Transceiver or reader
- Transponder or tag
- Host system or data processing system

Figure 1.1 shows a RFID system and how it operates is as follows. The transceiver, which consists of an antenna, sends periodic signals to inquire about any transponders in the vicinity. The transceiver detects the transponders in the working range and identifies their ID signals, and then passes this information on to the host system.

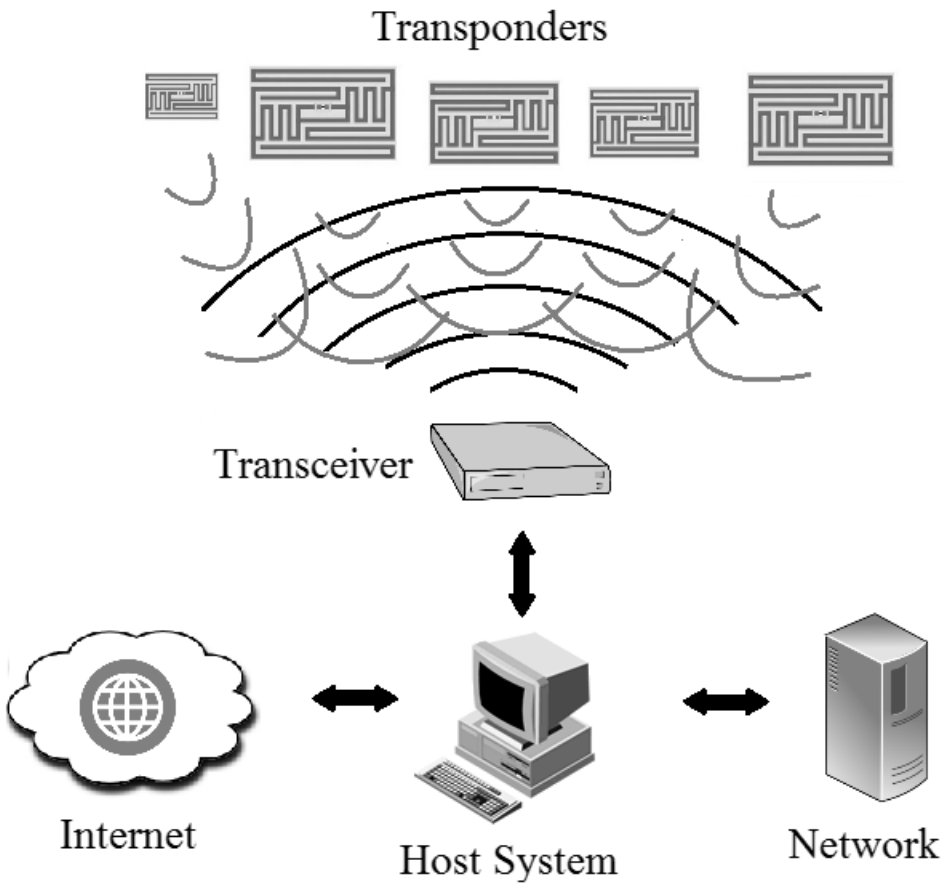

Figure 1.1. RFID system.

The host system provides the means of processing and storing the data, and this can then be further connected to a network, the internet, or some other system were additional processing and analyzing of the data can be done.

The transponders consist of an antenna and a microchip combined in a small package, and they are attached to the item or object that is going to be tracked. Once they get within range of the transceiver, they send the signal back to it to let it know that they're within range.

1.2 Types of Transponders

There are three types of transponders:

- Passive
- Semi-passive
- Active

Passive transponders are transponders that have no internal power supply in the chip and the power is then supplied by the transceiver. The transponder draws power from the magnetic field generated by the antenna. This in turn energizes the circuits, making the transponder backscatter the signal to the transceiver.

Semi-passive transponders have a small battery that allows the circuit to be constantly powered and it removes the need for power recovery circuits that are found in passive transponders.

Active transponders have their own battery and they broadcast their own signal. The batteries can either be replaceable or completely sealed, and some can even be connected to an external power source.

The advantages of active transponders are that they can be read at much longer distances of about 100 metres, they have higher bandwidth and data storage, and don't require much signal strength from the reader. Also they may be able to initiate communications or do independent monitoring. The disadvantages are that they are going to be larger and more expensive, and their lifetime is shorter because it depends on the battery.

As for passive transponders, advantages and disadvantages are basically the opposite. They can be much smaller, cheaper, require no maintenance, and their lifetime is much greater. On the other hand, they work at shorter distances going from a few inches to about 10 metres, have smaller read/write data storage, and they might remain readable for a long time, even after the item or product is no longer being tracked.

Semi-passive transponders are somewhere in between the two other types when it comes to distance, cost and lifetime.

Table 1.1 summarizes and compares the major differences between the three types of transponders [2].

Table 1.1 RFID Transponder Comparison

Transponder Type	Passive	Active	Semi-Passive
Power source	External Electromagnetic antenna field	On-board battery	On-board battery for internal circuitry Electromagnetic field for external transmission
Range	Measured in feet	Thousands of feet	Measured in feet
Size	Small	Large	Large
Data storage	Low	High	High
Cost	Low	High	High
Operational life	High	Low	Low

1.3 Frequency Range and Uses

RFID transponders operate on a very broad range, usual frequencies going from 135 kHz to 5.8 GHz. Frequency is one of the many factors that determine the range of operation of the system, and one of the most important characteristics [3].

Close coupling systems operate at very low frequencies up to 30 MHz, and require the transponder to be inserted into the transceiver or to be in extremely close proximity to it. These systems use capacitive and inductive coupling in order to communicate with each other. Capacitive coupling, as the name says, uses the plate of

the capacitors to provide the required coupling. Inductive coupling is when energy is transferred from one circuit to the other via their mutual inductance, meaning both transceiver and transponder need antenna coils. When they're close enough to each other, their fields will couple and a voltage will be induced into the transponder.

Remotely coupled systems use inductive coupling to communicate, operating at frequencies below 135 kHz and up to 13.56 MHz.

In the ultra-high frequency range (UHF), frequencies can vary from 433 MHz to 2.45 GHz. These systems use backscatter coupling, which means that the power transmitted by the transceiver into the transponder is reflected back to the transceiver, but after changing some of its properties, allowing the system to work at greater distances. A problem for UHF is that water and other materials absorb these waves, so tagging some objects may prove difficult. As for the difference in frequency, it depends on location; for example, 868 MHz is only used in Europe, while 900 to 928 MHz is used in the United States and Canada.

Other systems that use backscatter coupling are in the super high frequency (SHF) range using 5.8 GHz, allowing for ever longer ranges.

Table 1.2 summarizes some of the most common frequencies that are used and some of their applications [4].

Table 1.2. Common RFID Frequencies and Applications

Frequency Range	Typical Applications
< 135 kHz	Access control systems Alarm and theft prevention Animal identification Vehicle immobilizers
13.56 MHz	Item level management Parcel monitoring National identity card / passports Secure access control
443 MHz 860 – 960 MHz	Baggage sorting and monitoring Container monitoring Source coding Supply chain management
2.45 GHz 5.8 GHz	Road tolls Labels Real-time location systems

1.4 Modulation Schemes

Modulation is the process required to transmit information by varying a parameter, such as the amplitude, frequency, or phase, of an electromagnetic wave. It is used in a RFID system for both the forward link (transceiver-to-transponder) and reverse link (transponder-to-transceiver). There are many different modulation schemes, and the most common ones used for RFID will be covered.

Frequency shift keying (FSK) modulates the signal by changing the frequency of the carrier wave. This means that two frequencies for each binary state are used for the data transfer, one for the 1 or ON and one for the 0 or OFF. Even though FSK allows for

a simple transceiver design, it is rarely used in RFID because it has greater bandwidth, suffers from a slow data rate, and consumes more power compared to other modulation schemes [5].

Phase shift keying (PSK) is the process of changing the phase of the signal for each binary state. The shift is generally done by 180 degrees to differentiate between the two values, and it can be done at any 0 or at any data change. PSK provides faster data rate than FSK, but it is more complex so it requires more components and a larger area, and also consumes a great amount of power [6].

Amplitude shift keying (ASK) changes the amplitude of the signal and involves the simplest form of radio frequency detection. Two different amplitudes can be used, and in the simplest form of ASK one is usually picked as zero, which is what on-off keying (OOK) is. Nonzero amplitude represents a 1, while zero amplitude represents a 0. OOK is simpler to implement compared to other modulation schemes, but it loses the power up signal for the whole symbol period [7].

Pulse width modulation (PWM) is an OOK signal with different duty cycles, so it doesn't lose power during the 0 signal. It also has the advantage of simple clock extraction and detection circuits because it moves more of the system functionality to the RFID transceiver side, making it ideal for low power design.

That’s why in this thesis a 900 MHz ASK-PWM signal has been chosen for the forward link, as it allows for less power consumption, therefore increasing the operating range of the transponder.

1.5. Transponder Architecture

There are seven major components or blocks that make up the transponder as shown in Figure 1.2.

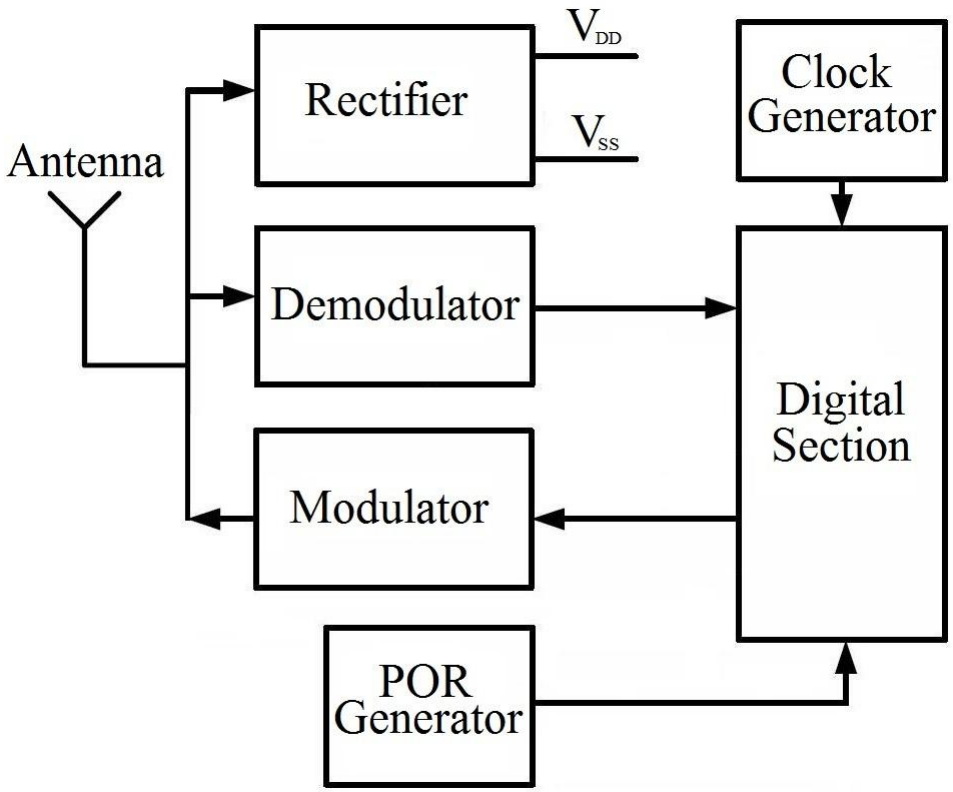

Figure 1.2. RFID Transponder Block Diagram.

1.5.1 Antenna

An antenna is a conductive structure designed to send or receive electromagnetic waves, so it is responsible for communication between the transceiver and transponder. Depending on the frequency range, the transponder can be either in the near field or far field of the transceiver antenna. At low frequencies in the near field, the power and signals are transferred by coupling, while at high frequencies in the far field, they are

transferred by electromagnetic waves in free space. The four major considerations when choosing an antenna are type, impedance, nature of the tagged object, and vicinity of structures around the tagged object [8].

In far field systems a wide variety of antennas are possible, although modified dipoles are most commonly used. For the transponder to operate effectively, it must receive enough power to turn on and it has to be capable of providing sufficient modulation for the transceiver to detect it. The power received by the transponder antenna is given by [9]

$$P_R = \left(\frac{\lambda}{4\pi d}\right)^2 P_T G_T G_R |\tau|^2 \chi \tag{1.1}$$

where λ is the wavelength, d is the distance between the transmitting and receiving antennas, P_T is the transmitted power, G_T and G_R are the gains of the transmitting and receiving antennas, $|\tau|^2$ is the mismatch efficiency, and χ is the correction factor for the effect of polarization misalignment.

The distance between the transceiver and transponder can be determined by

$$d = \frac{\lambda}{4\pi}\sqrt{\frac{P_T G_T G_R |\tau|^2 \chi}{P_{CHIP}}} \tag{1.2}$$

where P_{CHIP} is the power required to energize the transceiver. From this equation it can be clearly seen that in order to increase the range, the power to energize the transceiver must be minimized.

1.5.2 Rectifier

The rectifier or voltage generator is the circuit that provides power to the transponder, so its most important parameter is the output voltage V_{DC}. Most rectifier circuits are based on a diode attached to a capacitor that is added to smooth the rectified output and to remove any high frequency ripples [10].

An efficient rectifier called the 4-transistor cell structure using normal metal-oxide-semiconductor (MOS) transistors has been shown to perform better than diode-based rectifiers when Schottky diodes with low turn-on voltages are not available and is shown in Figure 1.3 [11].

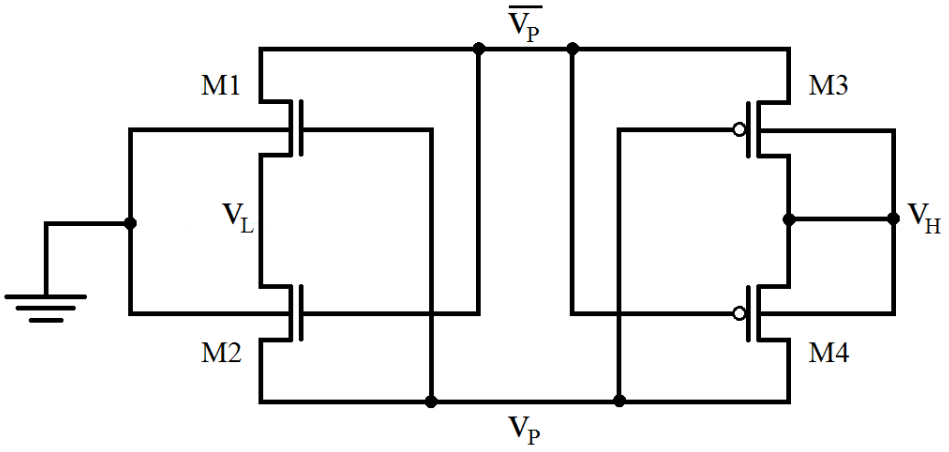

Figure 1.3. 4-transistor cell rectifier.

In this structure, if V_P and $\overline{V_P}$ are assumed to be high enough then the transistors will behave as switches, so a DC voltage will develop across a load connected between V_H and V_L. Generally, $V_{DC} = (V_H - V_L) = (2V_{RF} - V_{DROP})$, where V_{RF} is the AC voltage amplitude of V_P or $\overline{V_P}$ and V_{DROP} represents losses due to switch resistance and reverse conduction.

The maximum V_{DC} value that can be obtained with this structure is limited to $2V_{RF}$. In order to obtain larges values the cells can then be cascaded in series by coupling them with capacitors, allowing V_{DC} to build up at the output. This cascading in turn makes the circuit behave as a charge pump voltage multiplier.

1.5.3 Demodulator

The demodulator, which will be discussed in further detail in Chapter III, detects the signal sent from the transceiver and passes it on to the digital section. Since a 900 MHz ASK-PWM signal is assumed to be used in this project, the demodulator consists of an envelope detector to detect the gaps in this signal. The envelope detector is followed by an inverting Schmitt trigger for the purposes of both inverting the signal, as well as generating a more accurate envelope of the input signal. An integrator is next and it is what differentiates the bit parts of the signal, so the 1 and 0 gaps will have different outputs. Finally, the signal goes to the comparator, which will determine the correct output that will be fed into the digital section. The block diagram of the demodulator is shown in Figure 1.4.

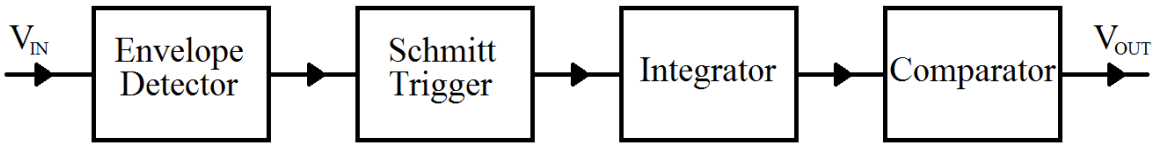

Figure 1.4. ASK-PWM demodulator block.

1.5.4 Modulator

The modulator is the block responsible of sending the signal back to the transceiver through backscattering. ASK backscattering is usually preferred because it makes the design simpler and has low power consumption. Using this approach, the modulator basically acts as a switch (S) parallel to the resonant circuit of the RFID transponder, either shorting the input impedance of the circuit (Z_{IN}) or leaving it matched with the antenna (Z_{ANT}), as shown in Figure 1.5 [12].

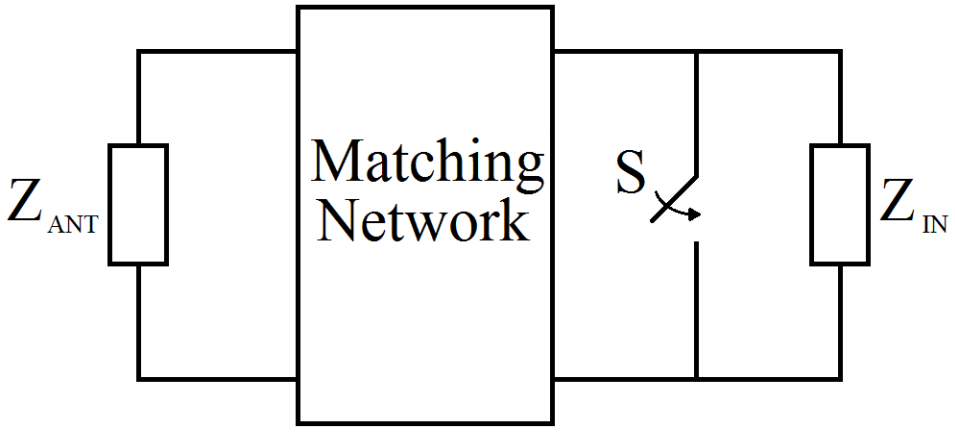

Figure 1.5. ASK backscattering modulator.

1.5.5. Power-on Reset Generator

The power-on reset (POR) circuit is responsible of generating the reset signal for the digital section, as well as disconnecting the transponder to avoid malfunction once the required power falls below a certain level.

Simply put, it has to measure the power supply voltage level and compare it with a certain threshold or reference voltage. If the power supply voltage is lower than the

reference voltage, the POR circuit has to release control of the baseband processor. If the power supply voltage level is higher than the reference voltage, the POR circuit has to generate the signals to reset and initiate operation of the digital synchronous baseband processor. Therefore, it needs a pulse in order to reset the circuit [13].

1.5.6 Clock Generator

The clock generator or oscillator is needed for the digital section to run and to decode the data. Depending on the system, the clock can either be generated on chip or it can be extracted from the incoming carrier signal.

There are different topologies that can be used to generate the internal clock such as current starved ring oscillators, relaxation oscillators, and phase locked loop (PLL), although the latter consumes too much power so it is normally not recommended for RFID. Relaxation oscillators are based on the charging and discharging of capacitors.

Ring oscillators can have different amount of stages, with the output of the last stage fed into the input of the first stage. They have the advantage of being able to operate without bulky passive components such as capacitors, resistors and inductors, making them the preferred topology as they consume less power and take up less area, which are the most important factors when it comes to clock generators [14].

1.5.7 Digital Section

The digital or baseband section of the transponder can have many different structures depending on the application of the RFID system being used. Typical and

most common parts are the anticollision circuit, the memory or EEPROM, and the mode selector or data encoder.

The anticollision circuit is what allows several transponders to be read simultaneously without interfering with each other. There are many anticollision protocols that can be implemented such as the query tree, binary tree, and dynamic slot allocation, just to name a few [15].

The memory or EEPROM is used to save the transponder ID and any other information that may be important such as the expiration date, location, or product number.

The mode selector or data encoder is what determines the mode of operation of the digital section, whether it's to read the data from the demodulator, or to address the memory array.

1.6 Objectives

The objective of this thesis is to design a low power demodulator, meaning we want to minimize its power consumed without affecting the performance of the circuit. As mentioned earlier, an ASK-PWM signal at 900 MHz will be used. The demodulator will be designed using 90 nm complementary metal-oxide-semiconductor (CMOS) technology and it will be used to complement other blocks for a low power RFID transponder. The main reason behind designing a transponder for low power is that it increases the operating range in case of a passive transponder, and in case of an active one, since it consumes less power, it increases the lifetime of the battery and system.

Chapter 2 explains the basic operation of a MOS transistor and its operation in the sub-threshold region. Chapter 3 shows the proposed design of the low power demodulator and its simulations. Chapter 4 provides additional simulation results along with the power consumed by the demodulator, comparing it with other circuits in the literature. Finally, Chapter 5 concludes the thesis and provides ideas for future work to be done.

CHAPTER II
MOS TRANSISTOR AND OPERATION

This chapter deals with the analog design basics of a MOS transistor. Section 2.1 introduces the MOS transistor and Section 2.2 its operation.

2.1 MOS Transistor

The structures of an n-channel metal-oxide-semiconductor (NMOS) and a p-channel metal-oxide-semiconductor (PMOS) transistor are illustrated in Figure 2.1.

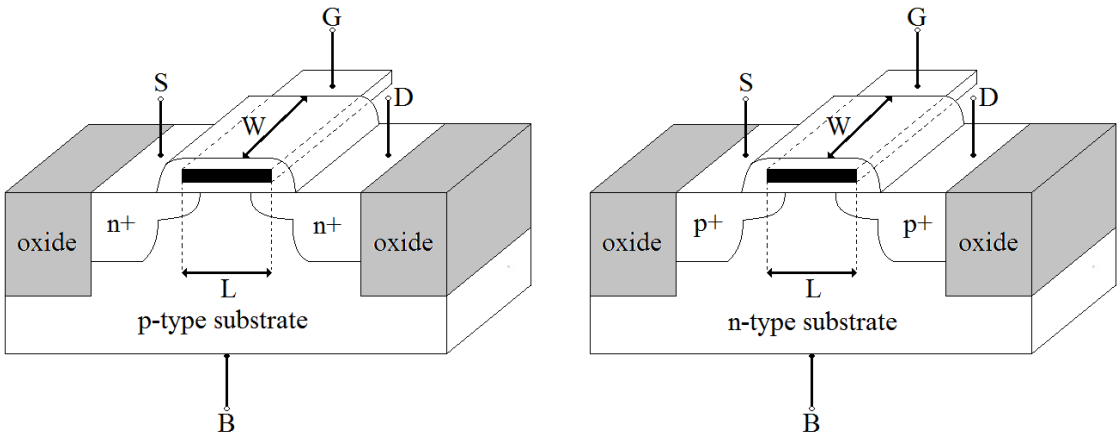

Figure 2.1. Physical structures of an NMOS and a PMOS transistor.

The NMOS transistor is formed with two heavily doped n^+ regions diffused into a lighter doped p^- material called the substrate or bulk (B). The two n^+ regions are called drain (D) and source (S) and are separated by a distance called the channel length (L). The channel width (W) is the distance in the direction normal to the channel length. At

the surface between the drain and source lies a gate (G) electrode that is separated from the silicon by a thin layer of silicon dioxide that acts as an insulator. Similarly, the p-channel is formed with two heavily doped p^+ regions diffused into a lighter doped n^- region. It also has the polysilicon gate terminal created in the same way as in the n-channel. For a CMOS process both NMOS and PMOS are built on the same wafer. So both transistors are essentially four terminal devices as shown in Figure 2.2 [16].

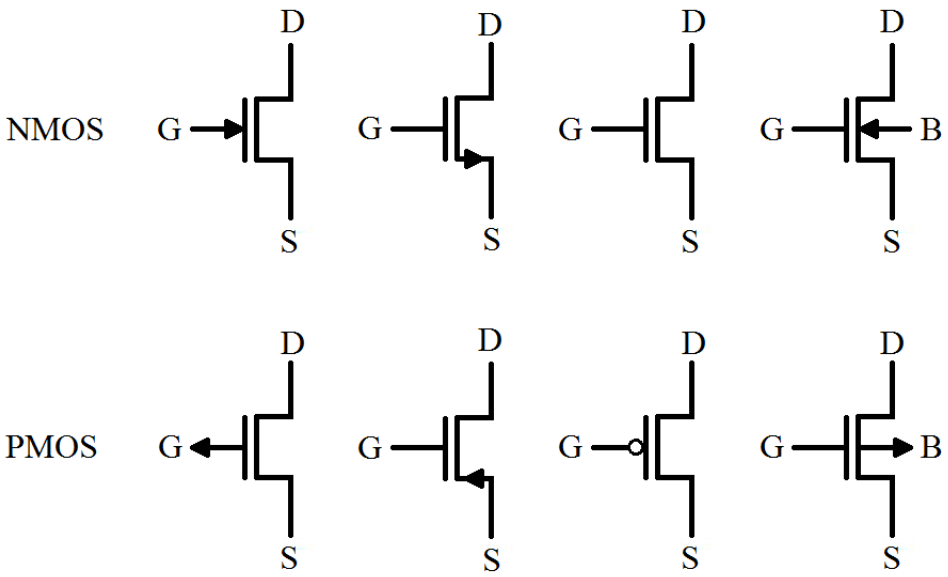

Figure 2.2. MOS transistor symbols.

2.2 MOS Operation

When a certain voltage is applied to the gate terminal, an inversion layer is formed between the drain and source to conduct current. In an n-channel device the current is carried by electrons, while in a p-channel device the current is carried by holes. The critical gate voltage at which an inversion layer is formed is called the threshold voltage (V_{TH}).

Depending on the bias voltage that is applied to the drain for fixed gate, source and body biases, a MOS transistor may operate in the linear, saturation, or breakdown regions. Furthermore, depending on the bias voltage that is applied to the gate for fixed drain, source, and body biases, a MOS transistor may operate in the strong, moderate, or weak inversion regions [17].

2.2.1 Strong Inversion Region

When the gate-to-source (V_{GS}) voltage applied is larger than the threshold voltage, the device operates in the strong inversion region ($V_{GS} > V_{TH}$). Depending on the magnitude of the drain-to-source (V_{DS}) voltage, the device may fall into different regions of operation.

The linear or triode region is when $V_{DS} < (V_{GS} - V_{TH})$, making the inversion channel act like a simple resistor. The drain current I_D increases linearly as V_{GS} increases and is given by [18]

$$I_D = \mu C_{OX} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \tag{2.1}$$

where μ is the mobility of charge carriers, C_{OX} is the gate oxide capacitance per unit area, and W/L is the effective width to length ratio of the transistor.

Saturation or active region is when $V_{DS} > (V_{GS} - V_{TH})$, which makes the excess voltage drop across the pinched-off region and the drain current remains approximately constant. The drain current in this case can be modeled as [18]

$$I_D = \mu C_{OX} \frac{W}{L} (V_{GS} - V_{TH})^2. \tag{2.2}$$

When V_{DS} is much larger than the saturation voltage, the device may enter into the breakdown region. This makes the current increase drastically as V_{DS} increases, and it is caused by the breakdown of the drain-body p-n junction.

2.2.1 Weak Inversion or Sub-threshold Region

The weak inversion or sub-threshold region, as the name suggests, is when the gate-to-source voltage is lower than the threshold voltage ($V_{GS} < V_{TH}$). When this happens, the transistor is supposedly off because no channel has been created. But in reality there is a small leakage or sub-threshold current that flows through the transistor that is much smaller than the current in strong inversion. Conduction in the sub-threshold region is dominated by diffusion current, unlike conduction in the strong inversion region where drift current dominates. This makes design in the sub-threshold region advantageous for implementing MOS transistors in analog circuits, especially in CMOS technology [19].

The current increases exponentially as the gate bias increases in the sub-threshold region and can be defined as [20]

$$I_D = 2n\mu C_{OX}\frac{W}{L}U_T^2 e^{\frac{V_{GS}-V_{TH}}{nU_T}} \tag{2.3}$$

where n is the sub-threshold slope factor given by $n = 1 + C_D/C_{OX}$, C_D is the depletion capacitance per unit area, U_T is the thermodynamic voltage given by $U_T = kT/q$, k is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge.

Assuming room temperature, most of these parameters are fixed and depend on the technology being used, while the length is kept at a minimum to obtain the lowest power dissipation. So the main parameters that can be controlled and changed to ensure the transistor operates in the sub-threshold region are the gate to source voltage along with the width of the transistor.

The drawbacks of sub-threshold operation include poor current matching, a maximum noise content of the drain current, and low speed [21]. Therefore, it is not recommended for high-performance systems where speed is a critical factor. However, in extremely low energy systems such as RFID, it can help reduce the power without affecting the overall performance.

2.2.2 Moderate Inversion Region

The moderate inversion region exists between the strong inversion and sub-threshold regions, as the transistor doesn't switch immediately from an exponential sub-threshold region behaviour to a quadratic strong inversion region behaviour. In moderate inversion, both the drift and diffusion currents are comparable and significant with neither effect dominating [22]. For this reason, compact modeling in this region becomes very difficult.

CHAPTER III
LOW POWER DEMODULATOR DESIGN

In this chapter the demodulator architecture that was presented in Section 1.5.3 is described in further detail, focusing on low power design. Section 3.1 presents the envelope detector, followed by the Schmitt trigger in section 3.2. This leads to the integrator in Section 3.3, and finally Section 3.4 deals with the comparator.

3.1 Envelope Detector

An envelope detector is a circuit that takes a frequency signal as input and provides an envelope of the signal as output. Figure 3.1 shows an image of the most basic envelope detector, which consists of a diode between the input and output of a circuit that is connected to a capacitor and resistor in parallel from the output of the circuit to ground.

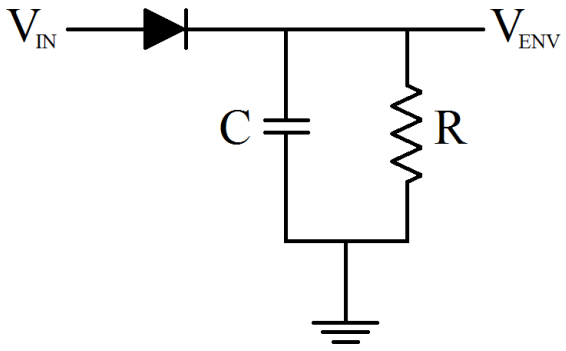

Figure 3.1. Basic envelope detector.

It is essentially a half-wave rectifier that charges the capacitor to the peak voltage of the input signal [23]. When the input wave's amplitude increases, the capacitor voltage is increased through the diode. When the input wave's amplitude decreases, the diode is then cut off because the capacitor voltage is greater than the input signal voltage and it causes the diode to open. This makes the capacitor discharge through the resistor slowly until it reaches a half cycle. When the input signal becomes greater than the output across the capacitor, the diode conducts once more and the cycle starts all over again.

The basic envelope detector only serves as a starting point for the design, as this circuit is too simple and inefficient, and diode based envelope detectors have known high distortion problems [24]. The circuit used, however, does consist of a rectifier section along with a resistor.

As it was stated earlier, the input wave in this project is an ASK-PWM signal operating at 900 MHz with an amplitude of 1.2 V. The job of the envelope detector is not only to track the envelope of the signal, but also to reduce the output signal low enough so that the rest of the components of the demodulator receive a voltage that is lower than their threshold voltage, making them operate in the sub-threshold region. However, the output voltage has to be reduced accurately, because if it is reduced too much and the voltage is too low, the signal won't be enough to drive the rest of the circuits. The lowest the signal could be reduced to was 0.3 V in order to ensure sub-threshold operation while keeping the demodulator operational.

The rectifier section is used to track the peak of the signal, and a particular voltage doubler cell was chosen for this section because it has the advantage that it's easy

to be cascaded [25]. Also it has been shown that the voltage doubler cell yields better results than conventional NMOS and low threshold transistors [26]. The voltage doubler cell is shown in Figure 3.2. As the amount of stages increases, the voltage is clamped and reduced more. Therefore, three stages were needed in order to reduce the signal as low as 0.3 V. One or two stages and the voltage would not be lowered enough, while four or more stages and the voltage would have been reduced too much making the rest of the circuit nonoperational.

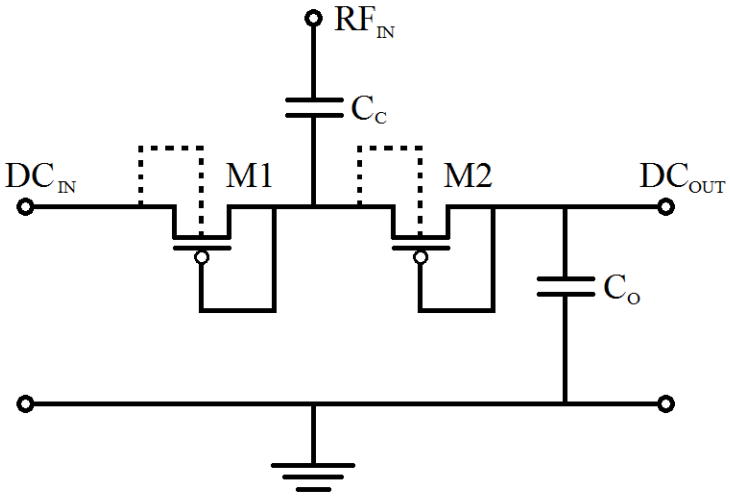

Figure 3.2. Voltage doubler cell.

The voltage doubler cell components control different parameters of the envelope detector. The width of the transistors help control the output voltage, so the value has to be carefully chosen to reduce the voltage to 0.3 V, considering three stages are used. If the widths are not properly chosen, the output voltage will be either too large or too small.

The capacitances control the output curve and the transition from a high voltage to a low voltage, and vice versa. The top capacitances (C_C) help keep track of the input signal. If they are too high, the output becomes distorted, while too low and the output becomes zero.

The bottom capacitances (C_O) control the shape of the output wave. If the capacitances are too high, the output wave will lose shape and it will go from being a square wave during transition to a curve. If the capacitances are too low, the peaks don't get tracked, so the output wave would be similar to the input wave.

After the three voltage doubler cells, a resistor is still needed just like in the basic envelope detector, or the signal will just get rectified and not track the envelope of the input signal, making the output signal a constant value after a certain period of time. The resistor, just as the amount of stages and the widths of the transistors, also helps control the magnitude of the output voltage. So if its value is too low or too high and is not chosen correctly, the output voltage will not be what is needed for the rest of the circuits in the demodulator.

Figure 3.3 shows the envelope detector circuit used and Table 3.1 the parameters of the components. Figure 3.4 displays the outputs of the envelope detector for the two cases of 1 and 0 inputs, and Figure 3.5 presents the layout of the envelope detector.

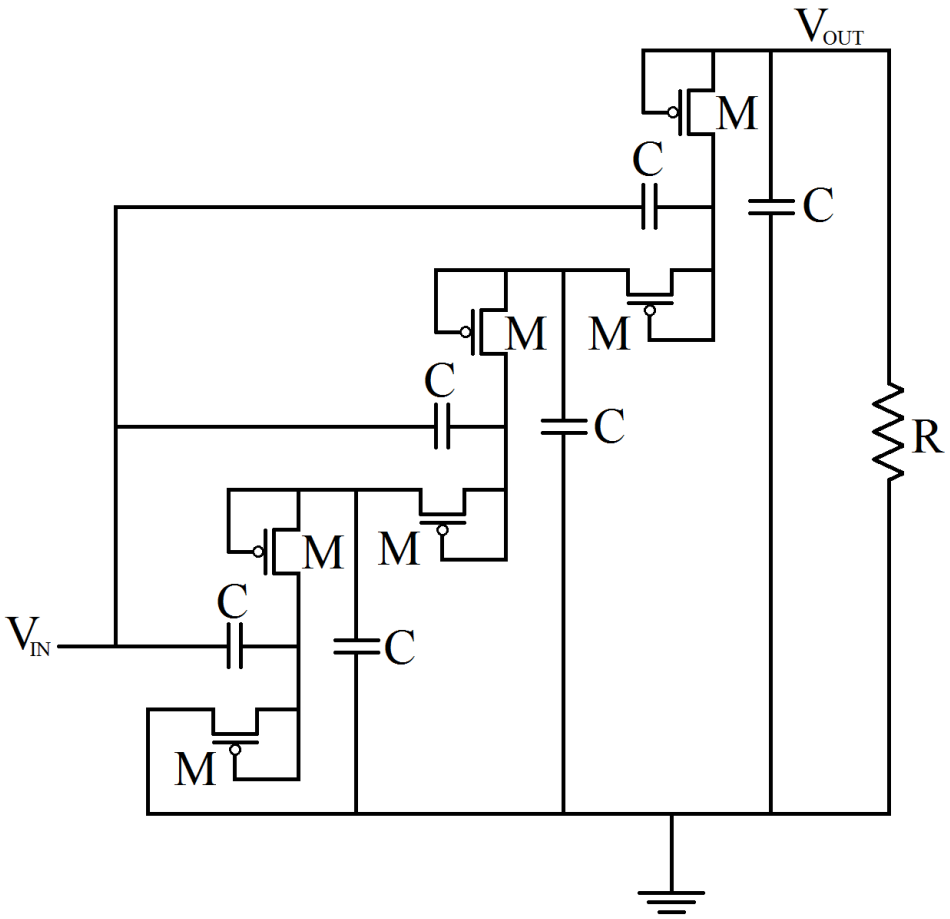

Figure 3.3. Envelope detector circuit.

Table 3.1. Envelope Detector Component Values

M	PMOS, 5 µm / 0.1 µm
C	400 fF
R	30 kΩ

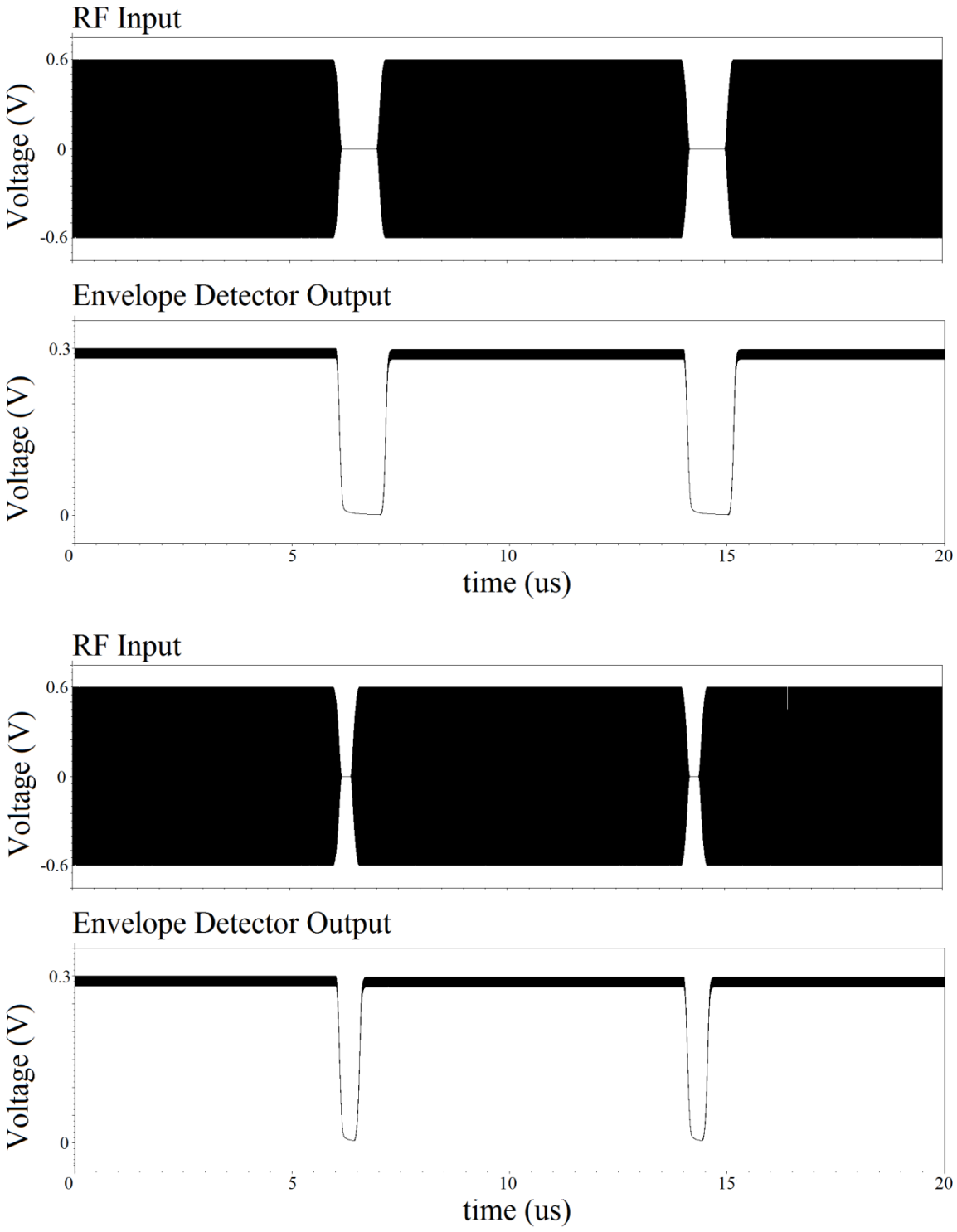

Figure 3.4. Envelope detector input and output for 1 and 0 signals.

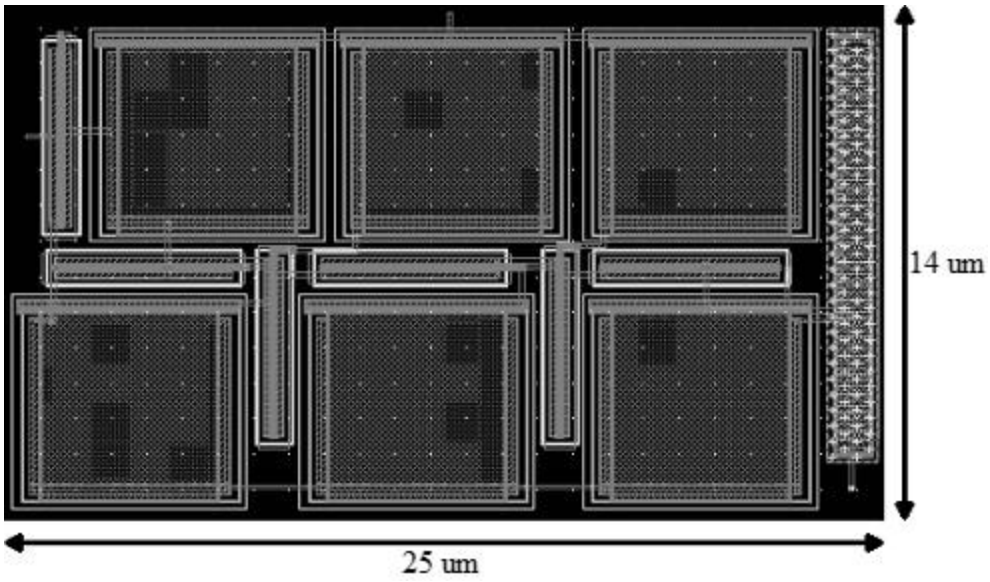

Figure 3.5. Envelope detector layout.

3.2 Schmitt Trigger

The next block in the demodulator is a Schmitt trigger, which is a type of comparator with two different threshold voltages. It is mainly used to reduce the effect of noisy inputs or signals, and it can be inverting or non-inverting. How it works is that when the input voltage goes over the high threshold voltage (V_H), the output is switched high, and it will stay high as long as the input doesn't go below the low threshold voltage (V_L), with the same behaviour occurring in the reverse situation. The difference between the two threshold voltages is what is called the hysteresis or hysteresis width (V_{HW}).

Figure 3.6 demonstrates exactly what hysteresis is and how it works by showing a noisy real life communication signal, as well as the outputs with and without a Schmitt trigger [27]. Without the Schmitt trigger and just using one value in the center for switching, every time the signal crosses the midway line there would be a switch in the output. However, with the Schmitt trigger, the signal stays low as long as it doesn’t go

over the high trigger value, and stays high as long as it doesn't go over the low trigger value. As illustrated, the outputs are two very different signals, so the Schmitt trigger protects against spikes and noise in the input signal.

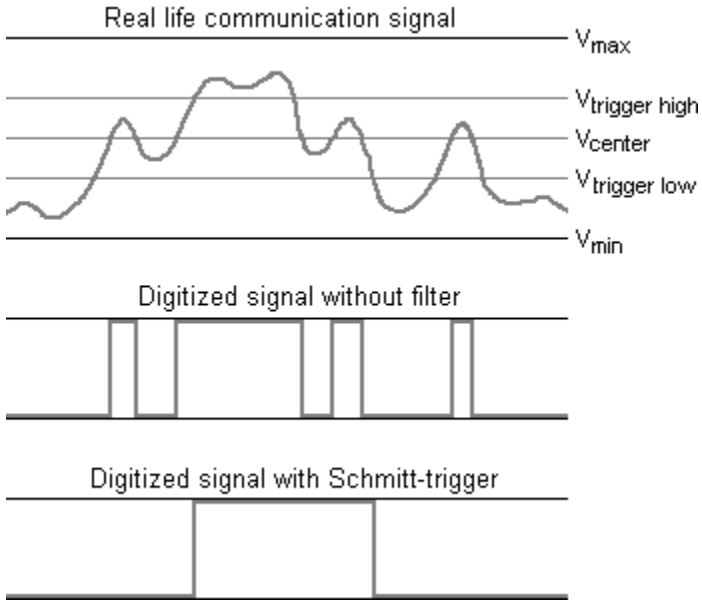

Figure 3.6. Signal with and without Schmitt trigger [27].

The traditional inverting Schmitt trigger consists of three PMOS and three NMOS transistors and is shown in Figure 3.7. Its standard operation is simply as follows. When the input voltage is low (V_{in} = 0 V), the two stacked NMOS M2 and M3 will be off while the two stacked PMOS M0 and M1 will be on, causing the output voltage to be high (V_{out} = V_{DD}). This will also cause M4 to turn off and M5 to turn on, which will then pull the node between M2 and M3 to V_{DD}. So when the input voltage increases, it will eventually turn M2 and M3 on and M0 and M1 off. But since the source of M2 was charged high by M5, only after that voltage is lowered enough by M3, or if the input voltage is high enough, can M2 be turned on, producing a low output voltage (V_{out} = 0 V). Since the

circuit is horizontally symmetrical, a similar process occurs when the input voltage changes from high to low. The voltage transfer characteristics of the hysteresis behaviour of the Schmitt trigger are shown in Figure 3.8 [28].

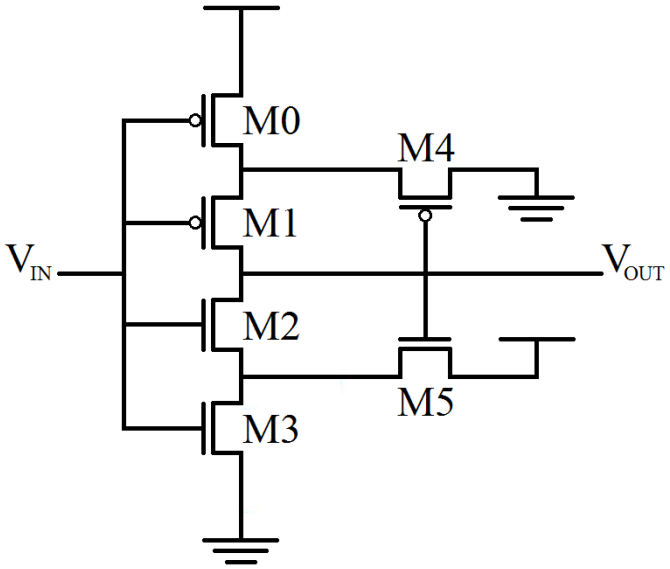

Figure 3.7. Schmitt trigger circuit.

There are many versions and types of Schmitt trigger circuits that have been implemented, but it hasn't been until recently where low power has been a concern. In [29] a low power prototype CMOS Schmitt trigger is presented using a different transistor arrangement and using a supply voltage of 3 V. Another one is presented in [30] using asymmetric double gates and four transistors. Reference [31] shows two CMOS Schmitt trigger using the dynamic threshold technique, which allows for the voltage to be reduced as low as 0.4 V. Reference [32] presents a simple CMOS Schmitt trigger well suited for low voltage and high speed applications that allows the construction of a very compact window comparator with only eight transistors.

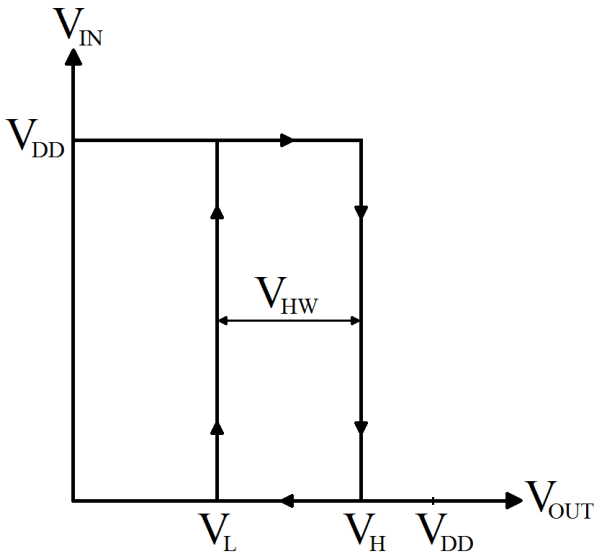

Figure 3.8. Schmitt trigger voltage characteristics.

The Schmitt trigger used for this project is based on the traditional Schmitt trigger shown above, with the exception that this one is made to operate in the sub-threshold region. The input to this circuit is the output from the envelope detector, and this voltage, which oscillates between 0.3 and 0 V, is lower than the threshold voltages of all the transistors and will make them operate in the sub-threshold region. The supply voltage V_{DD} was also reduced as low as it could to 0.3 V while keeping the circuit functional, guaranteeing that the output will not increase past this voltage and keep the rest of the circuit operating in this region.

In order to reduce the power consumed by this circuit even more than by just reducing the supply voltage, a model had to be created and analyzed extensively to see how changing the different transistor sizes would affect the drain current, power consumption, hysteresis width, area, and other metrics of the circuit. Certainly there are

equations that can be used to calculate some of these values such as the high to low or low to high thresholds, but they don't apply when the transistors are operating in the sub-threshold region.

From Equation 2.3 it was determined that the main controllable factors that affect operation in the sub-threshold region are the gate-to-source voltage and the width of the transistor. Since we're working with 90 nm CMOS technology and assuming room temperature and minimum transistor channel length (0.1 μm), all other values can be calculated and are basically fixed because of the technology. The gate-to-source voltage is what is being fed from the envelope detector, so proper care has to be maintained in order to calculate the width and to make sure the drain currents are low enough for sub-threshold operation.

It was found that by increasing the width size of M0, most of the drain currents were left unaffected, but the drain currents of M0 and M4 increased considerably, therefore increasing the power consumed as well. Increasing M1's width slightly increased the drain currents of M3 and M5 while leaving the others mostly unchanged. However, it decreased the hysteresis width of the circuit. Increasing the width of M3 and M5 slightly decreased M0 and M4's drain currents and left M1 and M2's current alone, but it had a drastic effect on M3 and M5's drain currents as it increased them substantially, so the trade-off wasn't worth it. Finally, changing the width of M2 and M4 increased M0 and M4's drain currents on a small scale, left M1 and M2's currents unchanged, and it decreased M3 and M5's currents to a large extent.

Based on these outcomes, it was found that changing the sizes of transistors M2 and M4 yielded the best results when it came down to reducing the overall drain currents and power consumption, while keeping the hysteresis width at a proper level.

The hysteresis width of the circuit used was 52 mV, with the high-to-low threshold at 83 mV, and the low-to-high threshold at 135 mV.

The component parameters of the Schmitt trigger are presented in Table 3.2. The input of the Schmitt trigger and its outputs for a 1 and 0 input signals are shown in Figure 3.9. The input is the output of the envelope detector, and the output of the Schmitt trigger is similar, but backwards, because it is an inverting Schmitt trigger. The layout is presented in Figure 3.10.

Table 3.2. Schmitt Trigger Component Values

M0, M1	PMOS, 0.12 µm / 0.1 µm
M2	PMOS, 0.3 µm / 0.1 µm
M3, M5	NMOS, 0.12 µm / 0.1 µm
M4	NMOS, 1 µm / 0.1 µm

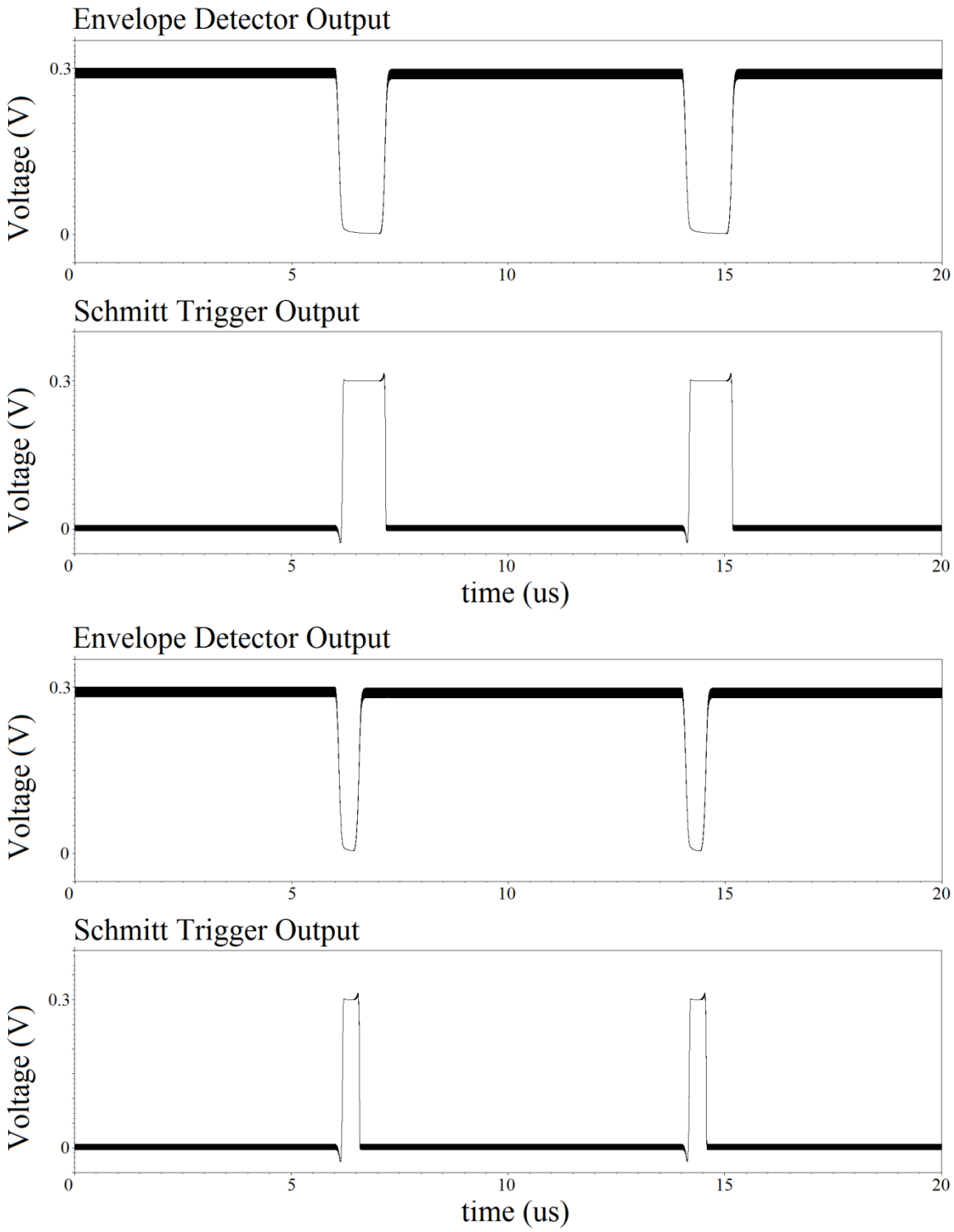

Figure 3.9. Schmitt trigger input and output for 1 and 0 signals.

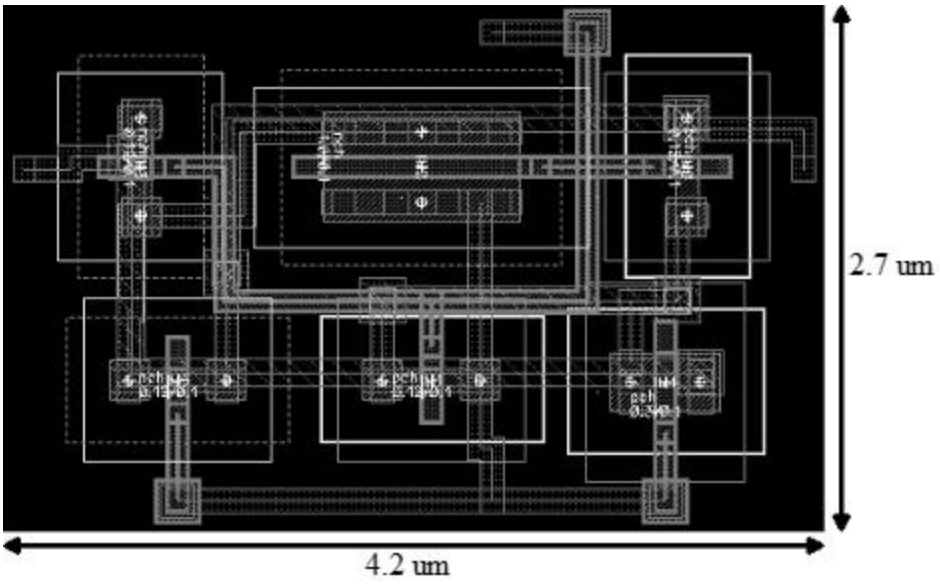

Figure 3.10. Schmitt trigger layout.

3.3 Integrator

An integrator, as the name says, is a circuit that integrates a signal. In this case the integration is done to differentiate the gaps from each other, so the 1 and 0 gaps will be different after going through it. Figure 3.11 shows an integrator implemented using an operational amplifier (op-amp) [33].

In this circuit, the output voltage (V_{OUT}) is determined by the length of time a voltage is present at the input (V_{IN}). The resistor is used to develop a current that will be proportional to the input voltage. This current will flow into the capacitor, whose voltage is proportional to the integral of the current with respect to time. Since the output voltage is equal to the negative of the capacitor voltage, the output is proportional to the integral of the input voltage with respect to time.

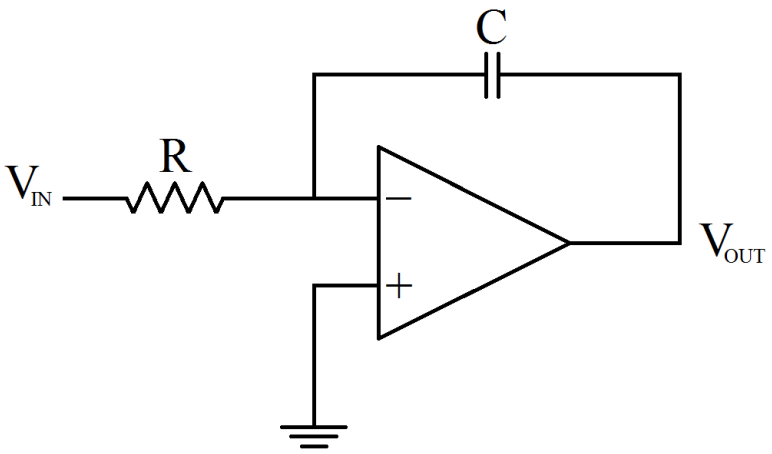

Figure 3.11. Integrator with operational amplifier.

The integrator for this project is implemented with a current source and a capacitor and is shown in Figure 3.12. A model was also created for this circuit and the transistors were sized and varied in order to see which would yield the least amount of power consumed, although the parameters were more constrained due to the capacitor, as it has to be able to discharge and differentiate between the two different gaps for logic 1 and logic 0. Special attention had to be paid also to the component values so the next block in the demodulator would be able to differentiate the integrations correctly.

The PMOS transistor determines how fast or slow the integration is done, while the two NMOS transistors determine the peak of the integration, meaning the output voltage. The capacitor in turn affects both of these settings. The supply voltage and the bias voltage (V_B) for the lower transistor M2 were kept at 0.3 V to guarantee the output voltage wouldn't rise above this value.

The parameters for the integrator are presented in Table 3.3 and the input and outputs for a 1 and 0 signals are shown in Figure 3.13. The layout of the integrator is presented in Figure 3.14.

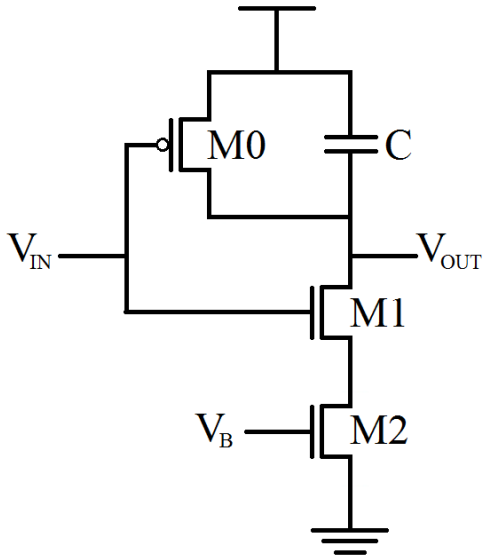

Figure 3.12. Integrator circuit.

Table 3.3. Integrator Component Values

M0	PMOS, 1 µm / 0.1 µm
M1, M2	NMOS, 0.12 µm / 0.1 µm
C	700 fF

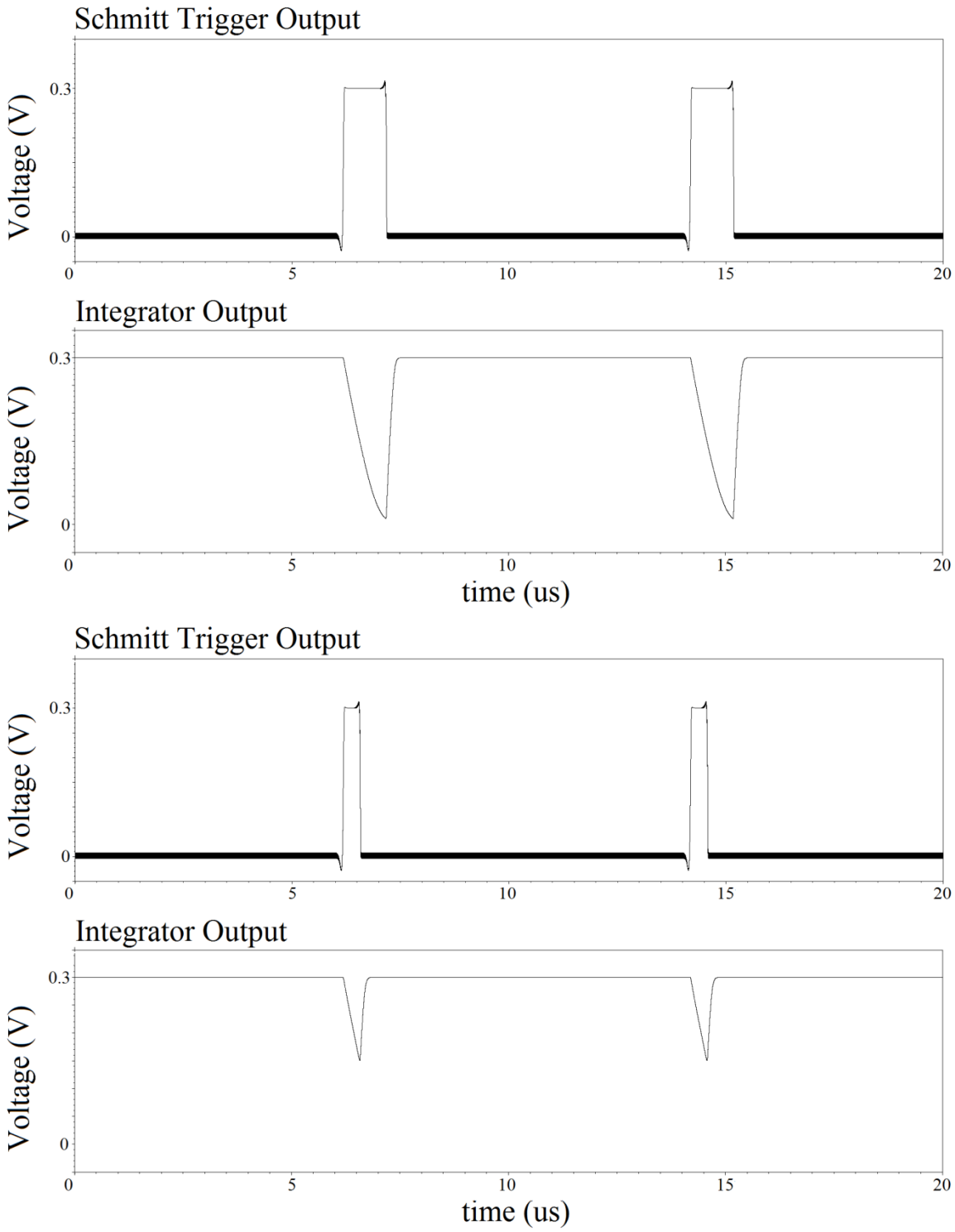

Figure 3.13. Integrator input and output for 1 and 0 signals.

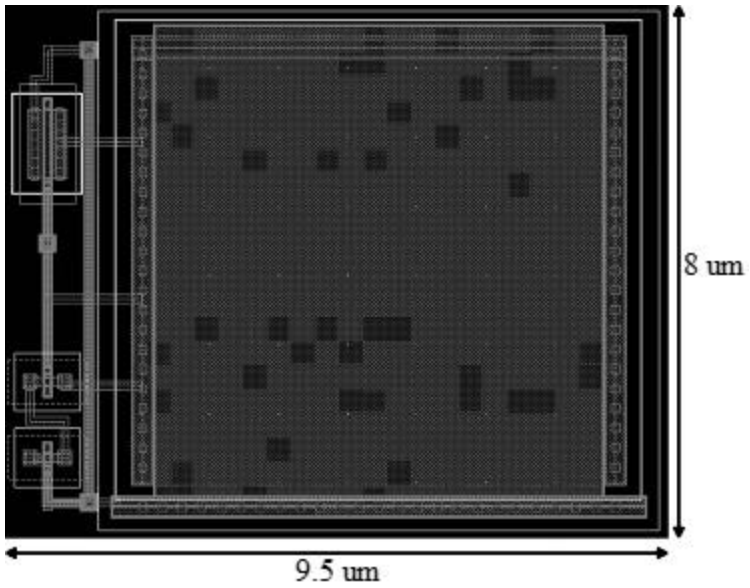

Figure 3.14. Integrator layout.

3.4 Comparator

The final block in the demodulator is a comparator, and just as the name says, it compares two input voltages and switches its output to indicate which is larger. Different comparator circuits were tested and simulated but they were either not working correctly in the sub-threshold region, or they were consuming too much power, making all the previous effort to reduce the power in the Schmitt trigger and integrator useless. Also, after the comparator, an inverter was needed to buffer the output to the digital section.

So it was decided that for this demodulator design, the comparator and inverter would be replaced by an inverting Schmitt trigger which was already optimized. Because after all, a Schmitt trigger is a comparator with different threshold voltages. Doing this helped reduce the power consumed significantly and it is something that to our knowledge hasn't been suggested in the literature.

The inverting Schmitt trigger used was the same one that has already been mentioned in Section 3.2 with the same values in order to differentiate the results of the integrator and feed the correct signal into the digital section. It wasn't coincidence that the same Schmitt trigger would work correctly with its two threshold voltages to differentiate the signals, but thoughtful planning when designing both the Schmitt trigger and integrator to get the correct output that was needed.

The input and outputs for a 1 and 0 signals for the comparator are shown in Figure 3.15. The output is the final output that will then go into the digital section of the transponder.

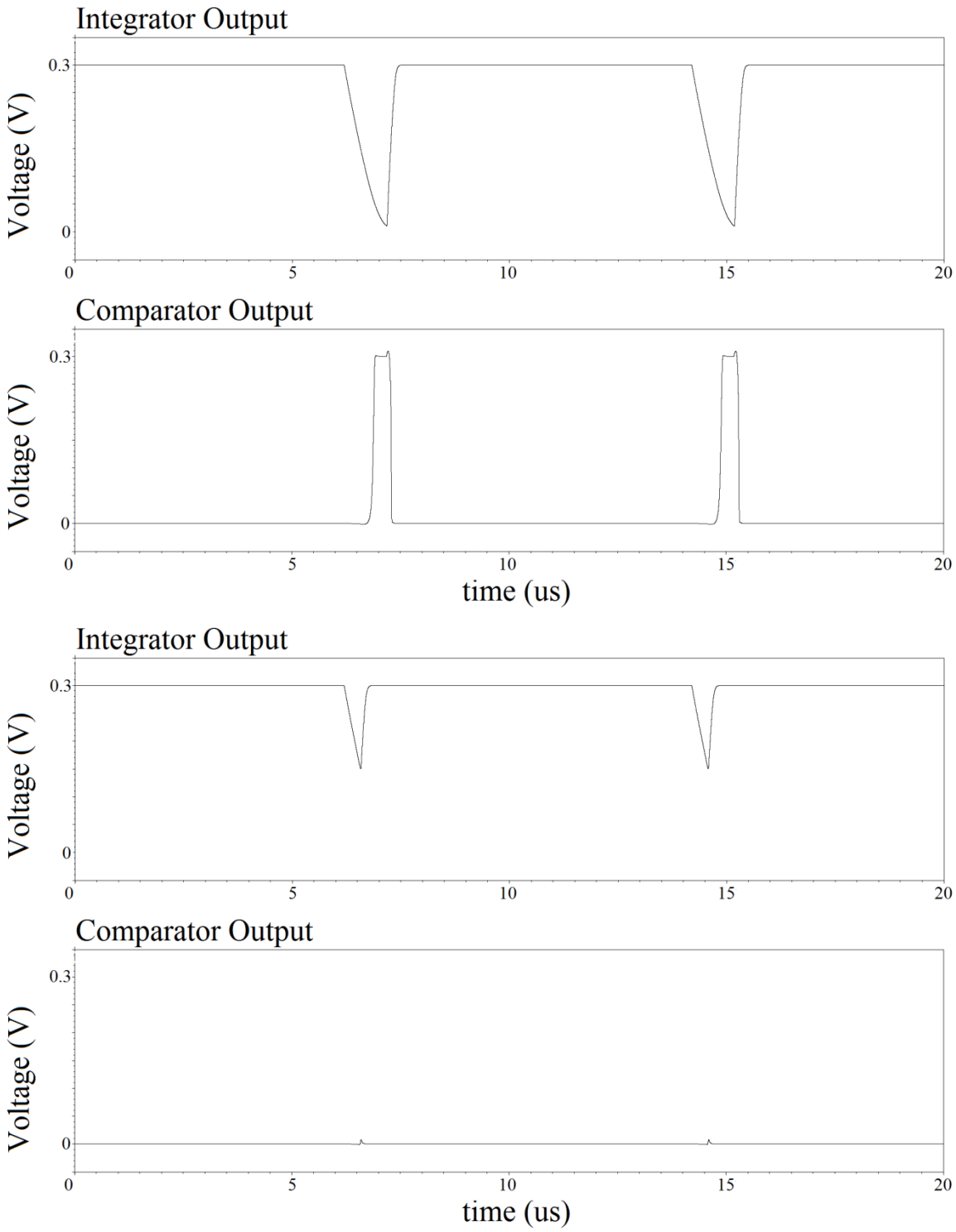

Figure 3.15. Comparator input and output for 1 and 0 signals.

CHAPTER IV
ANALYSIS OF RESULTS

4.1 Simulation Results and Analysis

The proposed circuit was designed in Cadence design tools using 90 nm CMOS technology, and all simulations were done using the Spectre simulator.

The input wave used was a 900 MHz ASK-PWM signal with a period of 8 µs with different gap lengths for logic 1 and logic 0. Figure 4.1 shows the output characteristics of the simulation. The input signal is '1 1 0 1 0 0 1' and the output is shown after each stage of the circuit.

The total power consumption for the whole circuit is only about 15 nW on average, which is by far lower than any result published already in the literature, when compared to 755 nW in [7] and 380 nW in [34]. These findings didn't use 90 nm technology as the process, so of course that by using a newer process the power consumption will improve. But we went further and compared what the consumption would go from by just using the standard sizing and operation in strong inversion with the same circuits and compared it to the optimized sizing using sub-threshold design and the results were remarkable, as the power consumed went down about twelve times from 180 nW to 15 nW. Table 4.1 shows the summary of these results.

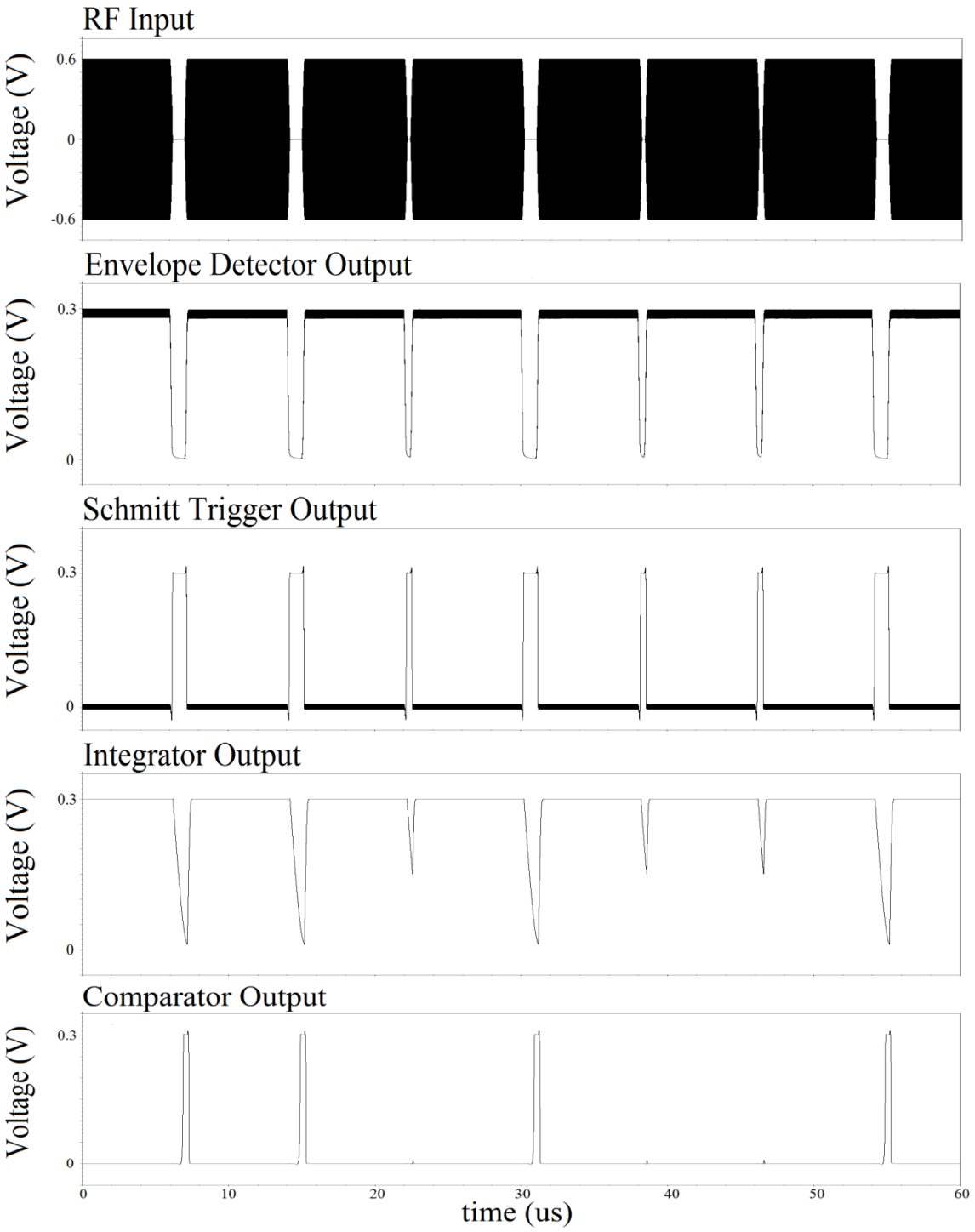

Figure 4.1. Demodulator simulation results.

Table 4.1. Demodulator Comparison

Literature	Frequency	Technology	Power Consumption
[7]	2.4 GHz	0.13 µm	755 nW
[33]	902 - 928 MHz	0.18 µm	380 nW
This work – standard operation	900 MHz	90 nm	180 nW
This work – sub-threshold	900 MHz	90 nm	15 nW

Other results worth mentioning are for papers that showed power consumption for the whole transponder getting results of 1 µW [35] and 1.2 µW [36]. These papers didn't specify exactly how much power was consumed by each block of the transponder, but from what we've gathered from other results, the demodulator consumes between 30-40% of the whole transponder power. Even if we were to consider and make a wild assumption that the demodulator consumed 20% of the power in those papers, it would still be around 200 nW, a result that is much higher than the one achieved in this project.

As for the drawbacks of designing in the sub-threshold region, as stated earlier, the delay of the circuit increased and it was much larger, going from a few picoseconds using strong inversion design, to a few hundred nanoseconds using sub-threshold design. But since RFID doesn't require high response and fast speed, this delay doesn't affect the performance of the demodulator so it is completely acceptable.

Another issue that comes into play is the operating temperature, as the circuit becomes more susceptible to it when working in the sub-threshold region. Even though

room temperature was assumed when designing and simulating the demodulator, different temperatures were also tested to see how they would affect the performance. The result from this was that the temperature affects the output pulse width in an almost linear fashion, increasing it as the temperature increases, and decreasing it as the temperature decreases. Still the demodulator performs well under most circumstances, and it isn't until the temperature is lowered below 5 ºC that the circuit stops working correctly.

4.2 Layout of the Demodulator

The layout of the whole demodulator circuit is shown in Figure 4.2, occupying a total area of 14 µm by 33 µm.

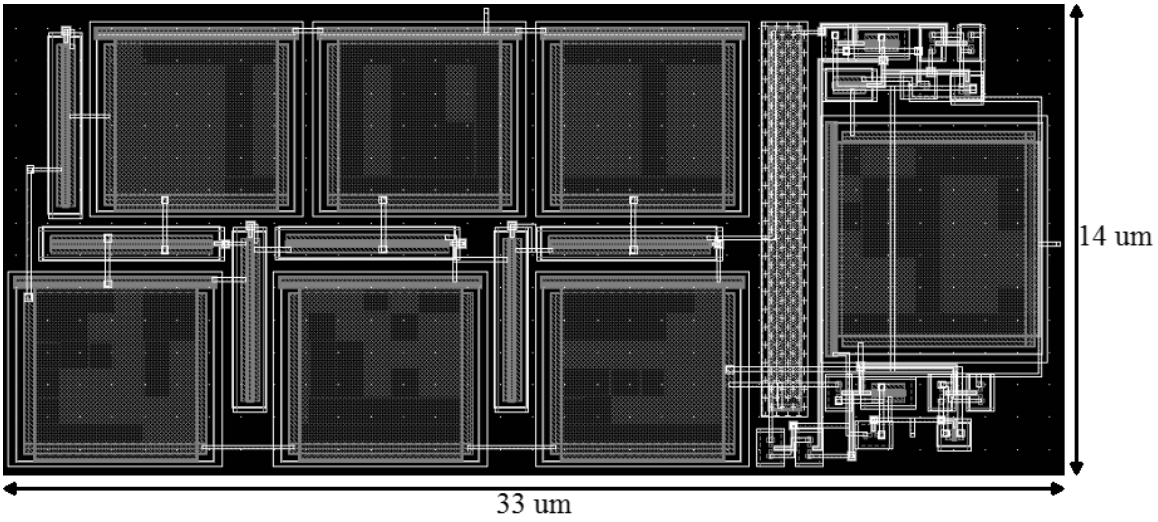

Figure 4.2. Demodulator layout.

CHAPTER V
CONCLUSION AND FUTURE WORK

5.1 Conclusion

A low power demodulator for a RFID transponder using a 900 MHz ASK-PWM signal has been designed using 90 nm CMOS technology. The envelope detector used was modified from existing ones based on a rectifier section and a resistor. The Schmitt trigger and integrator circuits were made to operate in the sub-threshold region with a power supply of 0.3 V, while the comparator and inverter used were replaced by an already optimized inverting Schmitt trigger. These components had to be carefully analyzed and sized correctly to ensure that they deliver the lowest amount of power possible while keeping the circuit fully functional. All of these steps taken helped reduce the power consumed substantially to only 15 nW on average, making this demodulator ideal for RFID, where low power is absolutely essential for the transponder to work at longer distances from the transceiver.

5.2 Future Work

There are many possibilities and options that could be done as future work for this project, such as working with different frequencies, or modulation schemes, or working with the other components of the transponder. At different frequencies the circuit would definitely change so a new challenge would be created.

Certainly the final goal would be to design all of the components of a transponder and make sure they all work together correctly in order to get it fully working.

APPENDIX A

PERMISSION FROM CO-AUTHOR

In this section a letter that permits the author of this thesis to use the paper that was co-written by Dr. Chunhong Chen is attached.

Permission to Use Submitted Paper

Dr. Chunhong Chen gives permission to Mario Mendizabal to include the following paper into his Master's thesis.

Paper submitted to 2012 IEEE International Symposium on Circuits and Systems, March 2012, Seoul, Korea, entitled:

M. Mendizabal and C. Chen, "Low Power Demodulator Using Sub-threshold Design."

Sincerely,

Dr. Chunhong Chen

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