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CMOS Optoelectronics

Implementation and Application

by

Guangxia Liang

A Thesis

Submitted to the Faculty of Graduate Studies
through the Department of Electrical Engineering
for the degree of Master of Applied Science
at the University of Windsor

November 1993

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Canada

Canada

Name *GUANGXIA LIANG*

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To my mother and father

ABSTRACT

An investigation of three different photo sensitive devices (PSD) that can be fabricated by using Northern Telecom's 1.2 and 3.0 micro CMOS technology is described in the thesis. A MOSFET has been optimized to enhance the photocurrent and use a parasitic photodiode formed between the source and substrate as a PSD. A conventional BJT structure with a small emitter area has been optimized to enhance the photocurrent and utilize the parasitic photodiode formed at the base-collector junction as a PSD. In addition, a field effect modified (FEM) vertical BJT with a collector-connected annular ring around a small emitter area has been used to create a more sensitive and faster responding parasitic photodiode at the base-collector junction that can be used as a PSD.

Each of the three distinct structures has been fabricated in both 1.2 and 3.0 micro technology in a number of different geometries as part of a parameter optimization study. A number of experiments have been carried out on the test cells to measure photocurrent as a function of light intensity using incandescent and LASER light sources. The most sensitive PSD was formed using a 3.0 micro FEM BJT design. The device is being used to create a photo sensitive array that will act as input nodes for an artificial neural network that is being employed as an intelligent sensor for process control based on non-contact measurement. As the array will be used to image LASER generated patterns formed by object-oriented beam steering, high sensitivity is not necessary, whereas a structure that can be readily integrated into a regular array is most important.

Acknowledgements

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CHAPTER 1

INTRODUCTION

1.1 THE MOTIVATION OF THE THESIS

In everyday life, various information is available in visible form. A great number of applications are related to image and vision, such as:

- image capture   remote sensing, event recording, etc.
- computer input automation   document scanning.
- robotics   machine vision.
- pattern recognition   optical-electric signal conversion.
- image processing   edge measuring, deblurring.
- optical communication   optical signal receiving.
- automatic control of machinery   position sensing, image processing.

The common generic element used in these applications is the Photo Sensitive Device (PSD), which is nothing but an electronic device that can convert optical variations into electrical variations.

The light sensitivity of silicon was discovered a long time ago. Diverse PSDs have been developed over the past several decades. Si photodetectors show the highest sensitivity in the

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wavelength range of 0.8-0.95μm. With the advance of the Very Large Scale Integrated (VLSI) technology, the 3μm and 1.2μm Complimentary Metal Oxide Semiconductor (CMOS) technologies are now available and are widely used due to their low power dissipation, simple process, MOS and BJT compatibility in the same wafer, scaling down potential, and so forth. Therefore, more interest is placed on the PSDs made by using CMOS processes.

1.2 CMOS 3μm AND 1.2μm TECHNOLOGY

In CMOS technology, the use of the well, made by low doping, opposite type silicon material as "surrogate" substrate diffused into the substrate, makes it possible that both n-channel and p-channel devices can be constructed on a single silicon substrate, as illustrated in Fig. 1.1. and Fig. 1.2.

Fig. 1.1 CMOS 3μm Technology

Fig.1.2 CMOS 1.2μm Technology

2
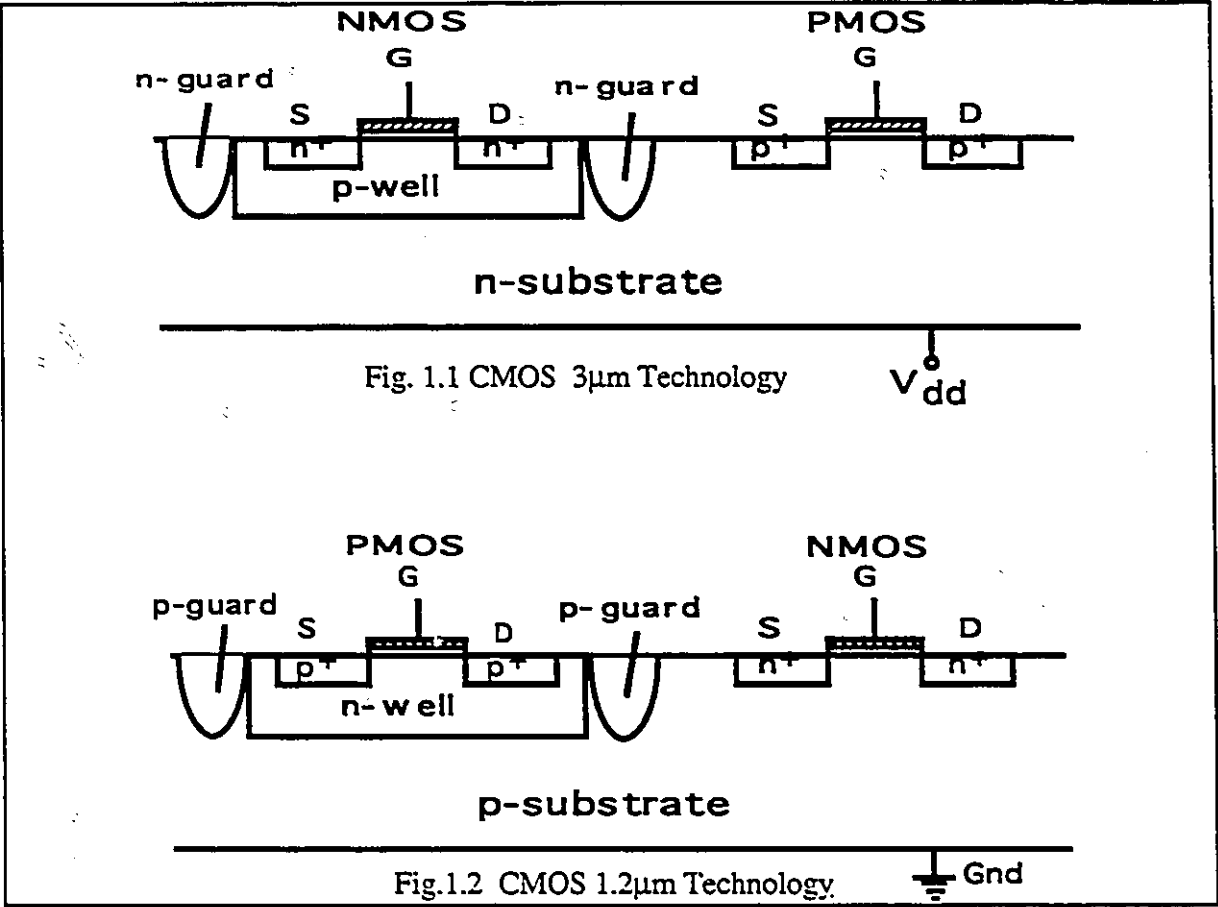
Although the CMOS process is essentially developed for the digital circuits, it can also be used to realize the Bipolar Junction Transistor (BJT). From Fig.1.3, it may be seen that the emitter, the base and the collector within the same well constructs a lateral BJT.
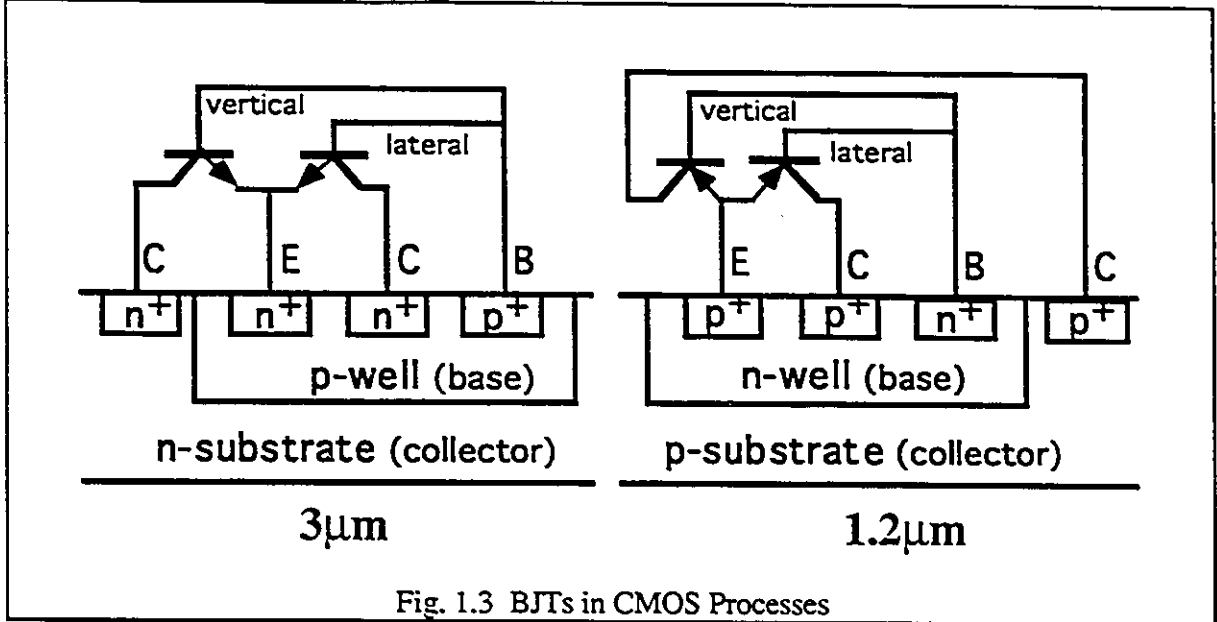
Fig. 1.3 BJTs in CMOS Processes

Due to the introduction of the well, a parasitic BJT is unexpectedly formed within the source (emitter), the well (base) and the substrate (collector) in the case of MOS, seen in Fig.1.1 and Fig.1.2, or within the emitter, the well (base) and the substrate (collector) in the case of lateral BJT. This is called the vertical BJT, as illustrated in Fig. 1.3. It is always accompanied by the lateral BJT.

Since the mobility of the electron is three times that of the hole, the NMOS is often adopted as a primary circuit. In a 3μm CMOS case, seen in Fig.1.2, the parasitic NPN BJT will become dominant and degrade the performance of MOS and increase the chances that latch-up will occur if the source area is quite large. However, the vertical NPN BJT characteristically has excellent gain with a corresponding low noise. Since the vertical BJT is bulk controlled, in most situations, it is more reliable than surface-controlled MOS or BJT transistors. [1.1]

For preventing the diode between the well and the substrate from forward biasing, which will result in substrate shunt current and degrade the performance of the MOS, the substrate is usually connected to the Vdd (highest potential of the power supply) for 3μm CMOS

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technology, seen in Fig.1.1, or connected to the ground (lowest potential of the power supply) for 1.2μm CMOS technolopgy, seen in Fig.1.2. Therefore, only the NPN BJT in a 3μm process or the PNP BJT in a 1.2μm process is possible. In summary, the NMOS, PMOS and NPN BJT can be made by using a CMOS 3μm process, the NMOS, PMOS and PNP BJT can be made by using a CMOS 1.2μm process.

1.3 THE LIGHT SENSITIVITY OF THE FLOATING WELL

It was found that a CMOS-fabricated MOSFET in a floating p-well on a semiconducting n-type substrate is optically sentsitive[1.2]. It is held true in an n-well in a p-type substrate.

The p-well potential is determined by the voltage drop of the source-substrate diode. The connection between that voltage drop and the current is given by the forward characteristics (source connected to ground, substrate connected to Vdd, p-well floating).

Fig.1.5 MOS mode and vertical BJT mode
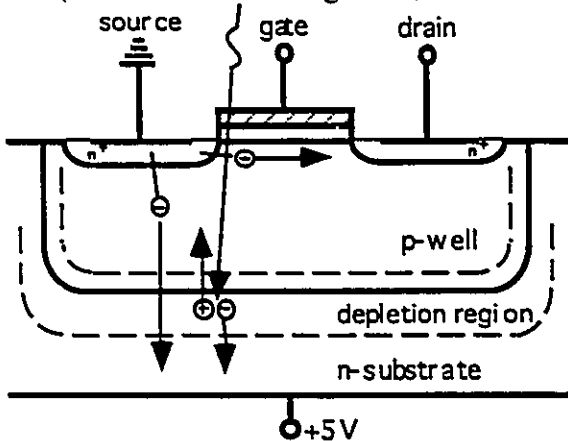
a) At low drain voltage

The channel field is not strong. Only a nearly constant leakage current is flowing through the diode. It produces a voltage U1 which works as the p-well bias, resulting an effective threshold voltage. The threshold voltage thus affects the drain current [1.3-1.4]. As illumination with light results in a higher leakage current, yielding a higher p-well potential, the threshold voltage connected with that potential will get lower so that the current will be increased. This is the photo sensitive mechanism of the PSD made in the CMOS process.

The relationship between the p-well-source induced current flow I_{ind} and the junction barrier potential (p-well potential) is given by the diode equation below:

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$$V_{p-well} = \frac{kT}{q}\ln(\frac{I_{ind}}{I_0} - 1) \cong \frac{kT}{q}\ln(\frac{RP_{opt}}{I_0}) \qquad (1.1)$$

where I_0 is the junction reverse-bias saturation current, proportional to the junction area.

P_{opt} is the light power in micro watts.

R is the responsivity

$$R = I_{ind}/P_{opt} = \eta q\lambda/hc$$

where λ is wavelength of light source.

    h is Planck's Contant.

    c is the speed of light.

    η is the quantum efficiency.

$$\eta = (1 - R_f)[1 - \exp(-\alpha w)]$$

Here, R_f is the surface reflectivity.

    α is the absorption coefficient.

    w is the width of depletion region.

An increase in p-well potential results in decreasing threshold.

$$V_T = V_{T0} + k_1(\sqrt{2\Phi_F - V_{p-well}} - 2\sqrt{\Phi_F}) \qquad (1.2)$$

As the threshold voltage drops, the channel current increases.

$$I_D = \beta[(V_G - V_T)V_{DS} - \frac{V_D^2}{2}] \qquad (1.3)$$

Substituting (1.2) to (1.3), a relation between the drain current and the incident light power is obtained:

$$I_D = \beta\{[V_G - V_{T0} - k_1(\sqrt{2\Phi_F - V_T\ln(1 + RP_{opt}/I_0)}$$
$$- \sqrt{2\Phi_F})]V_D - V_D^2/2\} \qquad (1.4)$$

Therefore, I_D will vary approximately as $\ln(P_{opt})$, as illustrated in Fig.1.5. The channel current of the MOSFET is logrithmically varied with light power.

b) For large drain voltage, (Vds>4V),

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The hole current generated by impact ionization (avalanche) at the drain exceeds the current generated by photons. This leads to dominance of the drain current,. Exceed holes also accumulate in very large quantities in the floating p-well near the source, causing positive voltage backbiasing to occur. As the drain current abruptly changes (kink), this effect is evidently indicated, as illustrated in Fig. 1.6.
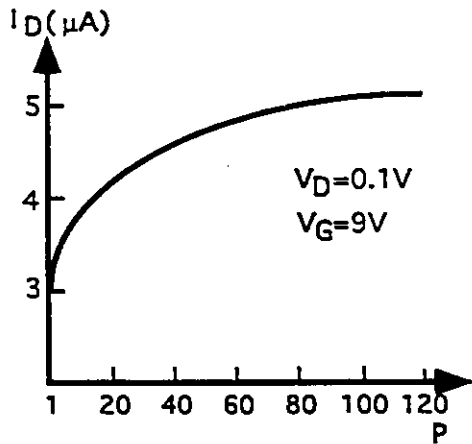
Fig 1.5 Drain current as a function of normalized light intensity
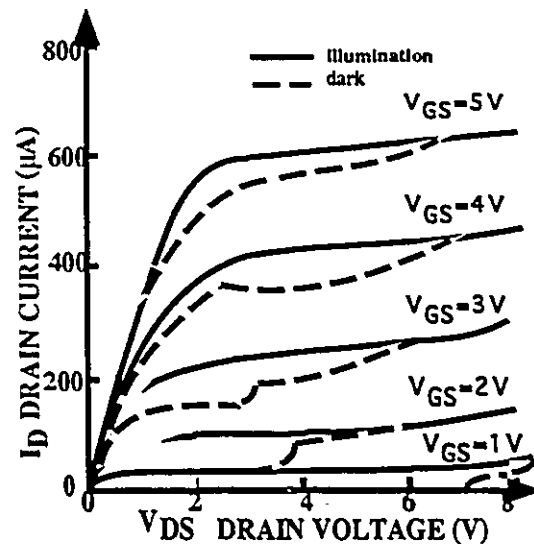
Fig.1.6 $I_D - V_{DS}$ curves for dark and illumination cases

When the transistor is illuminated, the kink smooths out as the p-well achieves a relatively uniform potential over the range of Vd values. For values of Vds greater than the kink voltage, impact ionization becomes the dcmonant effect, and there is very little photo induced change in the drain current. A Vds value chosen judiciously in the range below the kink voltage will lead the MOSFET to respond to light with the maximum current swing possible.

With a large source area, many electrons emitted from the source might not be captured by the channel field but cross the p-well into the n-substrate. Hence, a parasitic BJT can become dominant and create a large current flow through the substrate and into the source. This forms the phototransistor operation mode. The sourse current of the MOSFET with a large source area is linearly increased with respect to light power, reflecting a characteristic of a BJT photoresponse. It may be seen that there is no large channel between the photo MOS and photo BJT.

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1.4 THE OPERATION MODE OF PSD

The photocurrent is very small, usually the order of pA-μA, and is difficult to measure. It is often converted to the photovoltage. There are two approaches to convert photocurrent into photovoltage. One is to let the photocurrent flow through a load with huge resistance value. In this case, the PSD is operated in the photovoltaic mode. Another is to accumulate the charges generated by the incident light over a period of time then output the voltage. In this case, the PSD is operated in the photon flux integrating mode.

1.4.1 Photovoltaic mode (Steady-State mode)

o The light is projected onto the surface of the PSD, the photo-generated current (voltage) will be yielded in the output terminal of the PSD, continuously, just like the solar cell.

o This mode is usually operated in an intensive illumination case.

o The p-n junction of the PSD is essentially forward-biased so that it can not be integrated with the MOS circuits on the same chip.

o Area dependency (a large area generates a high photocurrent).

o It is very simple.

1.4.2 Charge-Storage Mode (Photon Flux Integrating Mode)

o The light is projected onto the surface of the PSD. The output of the PSD, either photo-generated current or photo-generated voltage, is periodically sampled. The peak output voltage of the PSD is independent of phototransistor current gain but proportional to :

- photo-generated charge amount.

- integration time.

$$V(t) = [V_0^{2/3} - \frac{2}{3} I_0 H (\frac{12}{q \alpha \varepsilon^2})^{1/3} t]^{3/2} \tag{1.6}$$

where H is the light density,

t is the integration time.

o This mode may be used at a very low illumination level by using a long integration time

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and in the case of nonrecurrent flash of high light by using short integration time. A dynamic range of about six order of magnitude of illumination level could be detected using this mode. And this range may be extended by the addition of external capacitance in parallel with junction capacitance.

o The p-n junction is reverse-biased so that it is possible to be integrated with MOS circuits on the same chip.

o The peak output signal is independent of the current gain of the PSD and the area of the PSD.

o Integrated arrays of charge-storage mode detectors are suitable for applications as image detectors.

o Many features can be easily added to the PSD, such as the light detection, the information enhancing, holding and reading out, the sensitivity, the wide dynamic range of linearity, the noise reduction, anti-blooming, etc.

1.5 THE LITERATURE SURVEY

There are a number of various PSDs, which can be divided into three categories in terms of the types of their output.

a) **Analog output**

Photoconductor, photo APD (Avalanche Photo Diode), photo JFET (Junction Field Effect Transistor), photo MOSFET, photo BJT. [2.3, 1.5-1.12].

b) **Digital output**

Photo flip-flop, the Lambda phototransistor. [1.13-1.15]

c) **Either analog or digital**

CCD (charge-couple device). [1.16-1.17]

The requirements of selecting PSD as the photocell of image array are:

o The output of the PSD is the analog signal which can be converted into either binary value (digital) or the grey levels, depending on different applications.

o The PSD can be used to construct an imager with high sensitivity, low noise.

o The PSD can be realized by using available standard CMOS processes such as 3μm or 1.2μm technology.

Literature survey summation:

o Due to the requirement of the imager, the devices with analog output are considered.

o The CCD has excellent performance in the imager application. Unfortunately, it can not be realized by using the standard CMOS processes.

o Of the other six PSDs, only photo diode, photo MOS and photo BJT will be carefully investigated, because:

- The photoconductor is not operated in the vision region but in the infrared region.

- The photo APD has large noise and needs high biasing voltage as well as a special process.

- The photo JFET has very low transconductance, responsivity dependent of area, and needs an epitaxial silicon process.

1.6 THESIS ORGANIZATION

This thesis consists of six chapters:

Chapter 1 is the introduction to the PSD.

Chapter 2 gives a review of the theory of the PSD..

Chapter 3 is focus on the simulation of photo BJT.

Chapter 4 involves the measurement and comparison of the PSD.

Chapter 5 introduces an intelligent imaging system using the best PSD as photo cell.

Chapter 6 concludes the thesis with a summary and suggestion for future research.

The main contribution of the author is that :

o the investigation of the CMOS PSD including literature survey, PSD layout using 3μm and 1.2μm CMOS technology, chip testing and PSD comparison.

o the development of a simulation method of the vertical BJT's photocurrent effect based on PSD measurement results, and the modification of the simulation model parameter of the PSD.

o the development of a simple PSD test method.

o the PSD application design involving an imaging system BSIIS.

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CHAPTER 2

THE THEORY OF
THE PSD

2.1 THE CONCEPT OF THE PHOTON

The photo-electric phenomenon is based on the electromagnetic radiation. On the basis of Planck's assumption of discrete energy, Einstein derived his famous photoelectric effect formula in 1905, which demonstrated that **electromagnetic energy is not distributed continuously in space but quantized in small bundles called photons** [2.1]. The energy of a photon E_p is directly related to its frequency and inversely proportional to its wavelength:

$$Ep = hv = hc/\lambda \qquad (2.1)$$

where

$h = 4.136 * 10^{-15} eVs$ is the Planck's constant.

v is the frequency of the electromagnetic radiation in Hz.

$c = 2.998 * 10^8 ms^{-1}$ is the speed of light in vaccum.

λ is the wavelength of the electromagnetic radiation in meter.

Transforming Eq(2.1), we get

$$\lambda = \frac{c}{v} = \frac{hc}{E_P} \qquad (2.2)$$

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The band gap energy of silicon is 1.1eV. The photo effect is not possible unless the photon energy is larger than or equal to E_g. Substituting 1.1eV into Eq.(2.2), the maximum wavelength of the visible light is found to be λ_{max}=1.127μm.

Electromagnetic energy is characterized by its wavelength, photon energy, and intensity. In the visible range of the light spectrum, electromagnetic energy is also characterized by its colour. The larger the E_P of incident light, the shorter the wavelength of the light.

2.2 THE CONCEPT OF ENERGY LEVEL IN ATOM

On the basis of an assumption that the angular momentum of the electron orbit is quantized, in 1913, Neiels Bohr proposed an atomic model which stated that it is only possible for an eletron to orbit the nucleus of an atom in discrete orbits with discrete values of energy [2.2]. The bound electron energies are depicted by discrete energy lines or levels, as illustrated in Fig.2.1. A free electron energy is zero electron volt (eV).
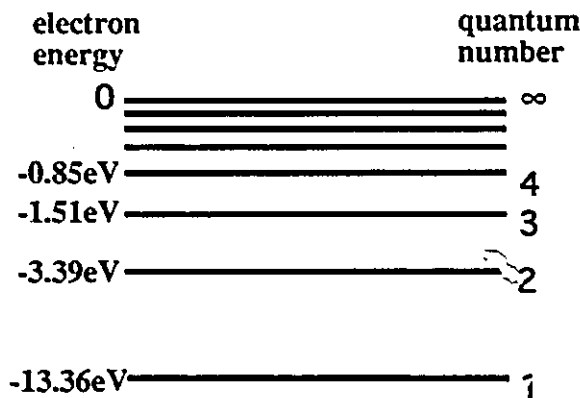
Fig. 2.1 Electron energy level
for hydrogen
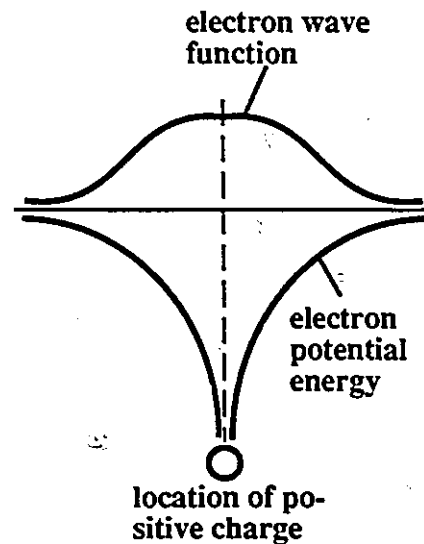
Fig.2.2 Electron potential energy & quantum mechnical wavefunction for one dimension potential well.

The theory was modified by applying quantum mechanism principles that electrons do not occupy fixed circular orbits of the atom but are spread out in three dimensions. The elec-

tron temporal and spatial position is described by a wave function which is defined as the probability density for spatial distribution of the electrons, as illustrated in Fig. 2.2.

As two potential wells are brought close to one another, there will be an increasing interaction between the bound electrons and the combined potential energy function. Two electrons (both initially in the ground state) can reside in either of two energy levels, one of lower energy level (corresponding to the wave function without the zero crossing) and one of higher energy (the resultant wave function with the zero crossing), as illustrated in Fig. 2.3. Thus, a single energy level is split into a band of levels, as a result of reducing the spacing between atoms in the crystal.

+1 +2

-1 -2

+1 -2

-1 +2
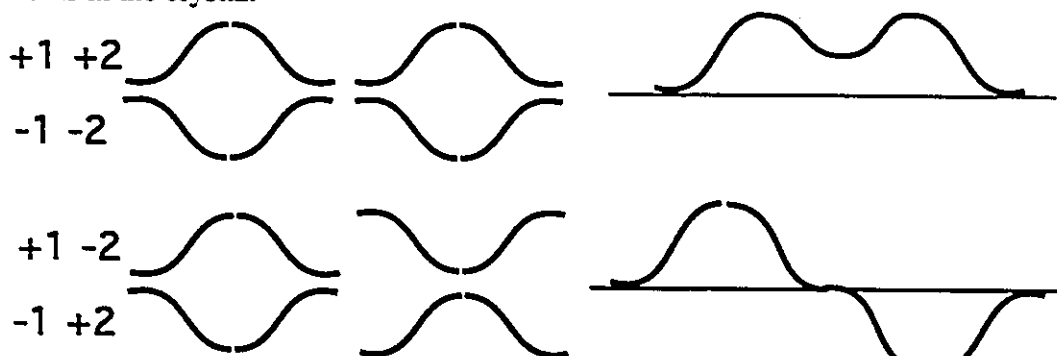
Fig.2.3 Splitting of an energy level into two energy levels due to the strong interaction of two electron wave functions

energy

conduction band

E_g

valence band

atomic spacing
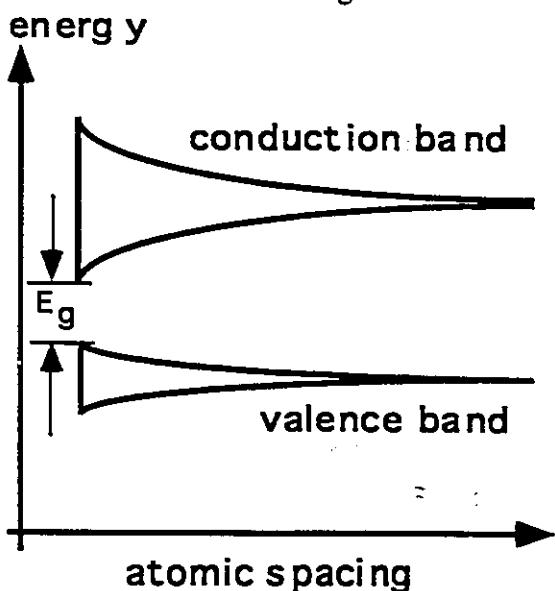
Fig.2.4 Energy band & gap in semiconductor

For the case of a semiconductor, a gap in available electron energy level exists between the occupied valence band of electron energies and the next highest unoccupied level. **The energy gap (Eg) is defined as the energy difference between the top of the valence band and the bottom of the conduction band (empty), as illustrated in Fig.2.4. The Eg of the semiconductor is** smaller as compared to that of the insulator.

The electron can absorb the energy to initially jump from a valence band state into the conduction band state gaining from a variety of sources such as light. When an electron in a semiconductor is elevated in energy to the conduction band, it leaves a hole, an empty electron state in crystal, which contributes to current conduction. Thus, electron-hole pairs are thermally generated.

The density of electron states function and the free electron concentration in the conduction band is a function of energy in an intrinsic material.

The Probability Density Function (PDF) $Pe(E)$ for the electron occupation of conduction band states is the Fermi-Dirac distribution function:

$$Pe(E) = \frac{1}{1 + \exp[(E - EF)/kT]} \qquad (2.3)$$

The probability function appropriate for holes occupying hole states at the top of the valence band is the probability that the associated electron state is unoccupied.

$$Ph(E) = 1 - Pe(E) = \frac{1}{1 + \exp[(EF - E)/kT]} \qquad (2.4)$$

The energy value EF is called the Fermi energy which is defined to be the maximum energy of electrons at 0 K. In an intrinsic semiconductor, the EF is approximately equidistant between the conduction band and the valence band, E_C and E_V respectly.

Due to the exponential decrease in the probability function with increasing energy, a slight change in the Fermi energy reference level (e.g. 100meV) results in a tremendous change in the free carrier concentration and the material conductivity.

In an intrinsic material, the free carrier concentrations are much less than the volume density of states. The probability of occupation of a conduction band state by an electron (or a valence band state by a hole) is much less than one half, i.e. the EF is very small. The number of occupied conduction band states will be small.

Assuming the $(E - EF)$ is much greater than kT :

$$Pe(E) = \frac{1}{1 + \exp[(E - EF)/kT]} \approx e^{EF/kT} * e^{-E/kT} \qquad (E - EF \geq kT) \qquad (2.5)$$

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As a result, the conduction band electrons are essentially independent.

$$Pe(E) \propto \exp(\frac{-E}{kT}) \qquad (2.6)$$

Assuming that most of the free electrons will occupy states very close to the lower edge of the conduction band (free hole will occupy only those states very close to the top of the valence band). The reference to the conduction and valence band of energies has been collapsed simply to refer to the edges of the bands Ec and Ev are separated by an energy gap E_g.

Quantitatively, the number of holes and electrons that are thermally generated is derived using the relationships

$$n = Nc * \exp[\frac{-(Ec - EF)}{kT}], \qquad p = Nv * \exp[\frac{-(EF - Ev)}{kT}] \qquad (2.7)$$

The free electrons and holes thermally generated in an intrisic material (no impurities present) are equal in number: $n = p = ni$ (intrisic carrier density). The product of the two carrier concentrations is given by

$$n * p = n_i^2 = Nv * Nc \exp[\frac{-E_g}{kT}] \qquad (2.8)$$

Eq.(2.8) indicates that the greater the density of unoccupied states Nc or occupied states Nv, the greater the likelihood of the transition of an electron from an occupied state to an unoccupied one, and therefore the greater the free carrier density. However, the greater the amount of energy involved in making the transition (relative to the energy kT), the less likely such a transition will occur. In other words, the rate of thermal generation of free electron-hole pairs is exactly equal to the rate of the capture (recombination) of free holes and electrons in an intrinsic material.

The free carrier densities can be modified by the introduction of impurities with a volume density much larger than the intrinsic carrier density ni, or, equivalently, by changing the position of the Fermi energy (the probability function) relative to the conduction and valence band edges.

The positioning of the Fermi energy closer to the conduction band edge than the valence band edge correlates to the case where the density of the free electrons (occupying states

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in the conduction band) is greater than the density of unoccupied states (holes) in the valence band. A Fermi energy value close to the valence band implies a greater density of free holes than electrons, as illustrated in Figure 2.5.

E_C ——————————— E_C ———————————
E_F ———————————

                                          E_F ———————————
E_V ——————————— E_V ———————————

n-type material   **p-type material**
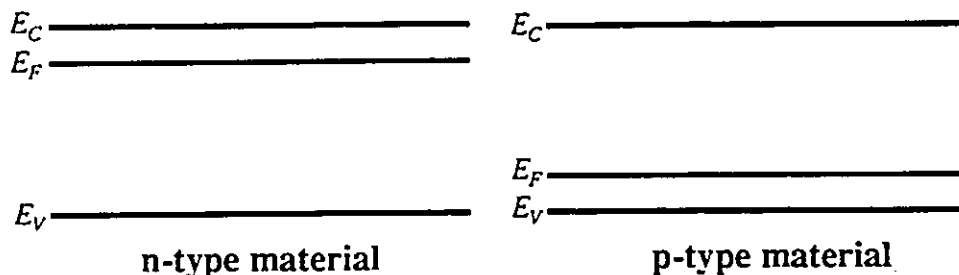
Fig.2.5. Energy band diagram for an n-type material (electrons are in the majority)

and a p-type material (holes are the majority carriers)

2.3 THE ENERGY LEVEL STATE IN A P-N JUNCTION

The principles of diffusion state that <u>free mobile electrons and holes tend to move from regions of high concentration to regions of low concentration</u>. Diffusion is a consequence of random thermal motion of the carriers.

With the two materials in contact, as electrons diffuse from the n-type region leave behind positively charged donor impurity ions N_D^+ and holes diffuse from the p-type region leave behind negatively charged acceptor impurity ions N_A^-, an electric field is formed. The direction of the electric field opposes the further diffusion of holes from p-type to n-type regions and the further diffusion of electrons from n-type to p-type regions. Therefore, every p-n junction acquires a built-in field and built-in contact potential, which opposes the further equilibrium diffusion of holes and electrons.

Since the n-type and p-type were each initially charge neutral, the resulting system of contacted regions is charge neutral overall.

built-in electric field
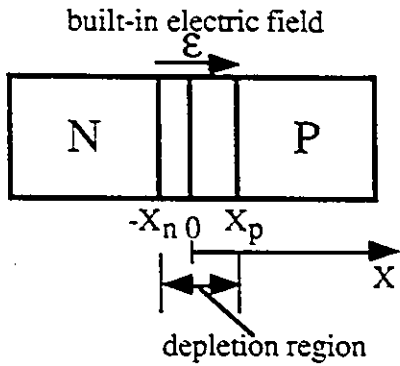
Fig.2.6.p-n junction

The region between $-x_n$ and x_p is assumed to be completely depleted of mobile holes and electrons due to the presence of the built-in field, seeing Fig.2.6.

The built-in field and contact potential will reach a magnitude such that the depletion region current produced by the diffusion flow of carriers from their majority to minority regions is exactly balanced by the depletion region drift current of carriers (electric field driven) from their minority into majority regions. **The net junction current is exactly zero.**

The total built-in voltage V_B is dependent only on the carrier concentration in the bulk region (zero electric field).

$$V_B = \frac{-kT}{T} * \ln(\frac{N_D * N_A}{n_i^2})$$

(2.8)

The built-in electron potential energy is

$$\Delta E = -q * V_B$$

Electron potential energy increases in an upward direction, hole potential energy increases in a downward direction. The energy gap E_g is constant throughout the material, only the relative potential energy changes, as illustrated in Fig.2.7.

built-in potential energy

$$\Delta E = -Q * V_{built-in}$$
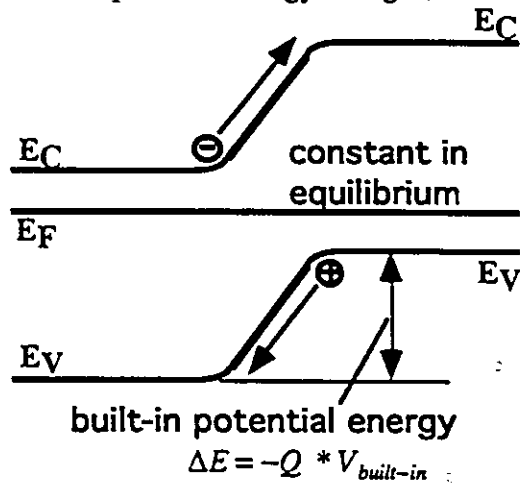
Fig.2.7. Energy band diagram for a p-n junction in equilibrium

If a voltage with the same polarity as the built-in voltage is applied to the p-n junction, the peak magnitude of the electric field x_n and x_p will all increase, the band-bending will increase.

If a voltage with the opposite polarity as the built-in voltage is applied to the p-n junction, the peak electric field x_n and x_p will all increase.

In the normal case, the p-n junction is reverse biased. The Fermi energy on two sides of the junction will separate further thus increasing the energy band bending. The applied reverse bias V_A increases the width of the depletion region and strengthen the built-in electric field in the depletion region so that the photo-generated free carriers will be easily created and swept quickly across the junction, as illustrated in Fig.2.7. The magnitude of the generation current roughly increases as the square root of the sum of the built-in and applied reverse bias voltage.

Fig.2.7. Energy-band diagram of a p-n junction with a reverse-bias voltage V_A

2.4 THE PRINCIPLE OF PHOTON DETECTION AND EQUATION

When a photon of an incident light at the speed of light strikes an atom, part or all of its energy is transferred to that atom. If its energy $E_P = E_{initial} - E_{final}$ exceeds the semiconductor's band-gap value E_g, i.e. $(hv > E_g)$, absorption of the photon can take place through the excitation of a valence electron into the conduction band, resulting in the creation of an electron-hole pair. The free electron and hole then become excess carriers and are free to contribute to the conductivity of the material.

Those photo carriers produced at (or within a diffusion length of) the p-n junction will be swept away by the depletion region field, the electrons into the n-type, and the holes into the p-type region before separation can occur. These photo carriers represent a negative current flow.

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To minimize the effects of the diffusion current, it must be ensured that the light penetrates the p-type region first and makes the width of the depletion region sufficiently wide that most photo electrons are generated in it.

The photo-generated current consists of two components as follows:

$$I = I_0[\exp(\frac{eV}{kT} - 1)] - I_{ph} \qquad (2.9)$$

where the first part represents the dark current (non-illumination case). The dark current is the difference of the following two current components. Both are statistically independent.

- $I_0 \exp(\frac{eV}{kT})$, a forward current due to majority carrier current flow across the junction.

- I_0 , the reverse current due to minority carrier flow in the reverse direction.

The second part $-I_{ph}$ is directly related to the photon flux.

According to [1.8], the photocurrent I_{ph} is given by

$$I_{ph} = \frac{q\lambda\eta P_o A}{hc} \qquad (2.10)$$

where   q is the electronic charge, $1.6021892 * 10^{-19} C$.

λ is the wavelength of the incident light, m.

η is the quantum efficiency.

P_o is the light intensity/unit area, w/m^2.

A is the light projected area, m^2.

h is Plank's constant, $6.626176 * 10^{-34} Js$.

c is the light speed in vaccum, $2.998 * 10^8 m/s$.

From Eq.(2.10), it can be seen that the photocurrent is affected by four factors. I_{ph} is proportional to λ, η, P_o, and A, respectively.

The photo effect is caused due to the absorption of photon energy. The absorption coefficient α , which is defined as the relative rate of decrease in light intensity along its propagation path[2.3], depends on the absorbing material and the photon wavelength. It is a function of incident photon energy. Generally, α is decreased strongly with an increase in light .

Those creating a diffusion length outside the depletion region must first diffuse to this

wavelength. The wavelength dependence of the absorption coefficient also makes the quantum efficiency a function of wavelength.

When the energy of incident photon is significantly larger than the band gap ($hv >> E_g$) the device will have a much larger quantum efficiency, as hv/ε electron-hole pair will be creased for each incident photon of energy hv, where ε is the ionization energy, the average energy necessary to create an electron-hole pair (3.6eV in Si). The larger the E_p of incident light, the shorter the wavelength of the light and the larger the absorption coefficient α, thus the larger the quantum efficiency η. The controllable factors are the material and the area.

By using Eq.(2.10), photocurrent can be calculated if the values of the above four factors are known. The calculation result of photocurrent can be used to determine the magnitude of the photocurrent source for photo effect simulation.

For example, if the spot size of laser beam is observed roughly 80x80 $(\mu m)^2$, identical to the area of the PSD, the maximum light power through the attenuator and the microscope is 0.36mw, this corresponds to a light intensity of:

$$0.36 * 10^{-3} / 80 * 10^{-6} * 80 * 10^{-6} = 0.05625 w / (mm)^2$$

This value can be used as the upper limit of light intensity. The value of quantum efficiency η lies between 0 and 1, assuming 0.2, and $\lambda = 623.8nm$. The upper limit photocurrent will be:

$$I_{ph-max} = \frac{(1.602 * 10^{-19})(6.328 * 10^{-7})(0.2) * 56250 * (64 * 10^{-10})}{6.63 * 10^{-34} * 3 * 10^8} = 36.7 \mu A$$

For the lower limit, a measurement is made with a photometer in a dark room. The value measured was around 10 lux which is roughly $1 w/m^2$, the photocurrent can be calculated to be:

$$I_{ph-min} = \frac{(1.602 * 10^{-19})(6.328 * 10^{-7})(0.2) * 1 * (64 * 10^{-10})}{6.63 * 10^{-34} * 3 * 10^8} = 0.652 pA$$

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CHAPTER 3

THE SIMULATION
OF THE PSD

3.1 PHOTOCURRENT EFFECT SIMULATION IN HSPICE

3.1.1 The modeling of diode photocurrent in HSPICE

Photo diode is the simplest and the most primary photo sensitive device. Even thouth it has the low current transfer ratio (CTR=0.2%), it is still a widely used PSD due to its simplicity, broad band characteristic, low idle noise, fast responsivity as well as the response linearity. It forms a basis of other PSD such as photo BJT, photo MOS and so forth.

There are several kinds of photo diode, the p-n junction diode, pin diode, Schottky diode, heterojunction diode and avalanche photodiode (APD). They are essentially all a p-n junction.

In non-illumination case, there is a low junction reverse current called dark current (leakage current) corresponding to the electrically or thermally generated carriers. Under illumination, the diode reverse current includes two portions, one corresponding to the electrically generated carriers, another corresponding to the optically generated carriers.

As we know, photons generate excess electron-hole pairs in a junction. Minority carriers crossing the junction build up a negative charge in n-region, a positive charge in a

p-region, generating a less than 1 volt voltaic voltage. If the junction is short-circuited, the photo-generated current will flow in the same direction as the thermogenerated leakage current.

Recall the equation (2.9), the photo-generated current is given by

$$I = I_0[\exp(\frac{ev}{kT} - 1)] - I_{ph}$$

where the first term represents the electrically or thermally generated dark current or leakage current while the second term I_{ph} stands for the photo-generated current corresponding the optically generated carriers.

For deriving the photocurrent equation of a p-n junction, assumptions are made in HSPICE [3.1], as follows:

o The radiation is penetrating, i.e., it is sufficiently energetic so it is not attenuated. This provides a constant carrier generating rate through the active region of the semiconductor, in other words, providing a constant independent current source. The assumption is not true to optical radiation as light can only penetrate a short distance.

o The junction voltage is fixed.

In practical devices, this is impossible because the radiation will induce a photocurrent which flows through the parasitic resistance of the device. The voltage across the junction will droop by the resistive voltage drop of the photocurrent. Hence, only when photocurrent is in low level and the parasitic resistance is small, the assumption of a constant junction voltage is approximately correct.

o The radiation pulse is square

It simplifies the time response of the photocurrent due to neglecting the rise and fall time of the light pulse so that it is unnecessary to do the convolution of the time function of the photocurrent generating rate with time.

o The junction is abrupt and one sided with a constant and doped semiconductor.

It allows the simple one-dimension model of minority carrier flow in a semicon-

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ductor.

Under the above four assumptions, the photocurrent in HSPICE can be expressed as:

$$I_{pp} = qrg_rAF\{ \underbrace{w}_{\substack{prompt \\ component}} + \underbrace{L_d erf[\sqrt{\frac{t-t_s}{\tau}}]}_{\substack{delayed \\ component}}\}u(t-t_s)$$

$$-qrg_rAF\{ \underbrace{w}_{\substack{prompt \\ component}} + \underbrace{L_d erf[\sqrt{\frac{t-t_s-t_p}{\tau}}]}_{\substack{delayed \\ component}}\}u(t-t_s-t_p)$$

(3.1)

where

I_{pp}	primary photocurrent (A)	L_d	diffusion length (m)
r	radiation dose rate (Rads/sec)	erf	error function
q	electronic charge (1.602E-19 Coulombs)	t	time (s)
g_r	carrier generation constant	τ	radiation minority carrier
	$(4.0E19m^{-3}$ in $S_i)$		time constant (s)
F	user scale factor (dimensionless)	t_s	dose rate pulse start time (s)
A	junction area (m^2)	t_p	dose rate pulse width (s)
w	depletion layer width (m)	$u(t)$	unit step function

In Eq. 3.1, the first term serves for the turn on and buildup of the photocurrent during the irradiation pulse, while the second term is responsible for the turnoff and decay after the pulse. Each term contains both a prompt component and a delayed component.

The prompt component yields from carrier pairs generated within the depletion layer of the p-n junction. These carrier pairs are immediately accelerated by the electric field inside the depletion layer and appear as photocurrent. The prompt photocurrent is therefore proportional to the depletion layer width, w, which is inversely proportional to the applied voltage dependent depletion capacitance, C. The higher the applied reverse voltage, the larger the prompt component of the photocurrent.

The delayed photocurrent arises from carriers generated outside the depletion layer. Some of these carriers move into the depletion layer after diffusing for a period of time which accounts for the delay and buildup of the response. When the dose rate pulse ends, the prompt component disappears immediately, but the delayed component will remain for a short time and decays slowly to zero.
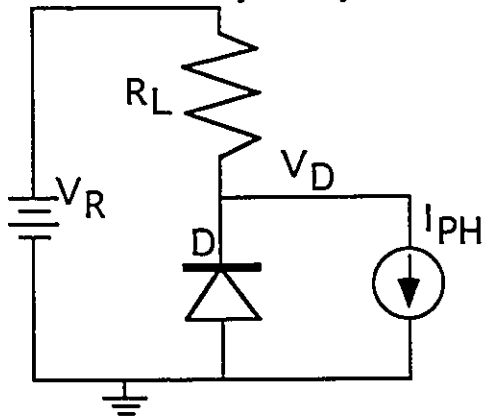
Fig.3.1 Simulation for Photocurrent in a pn Junction

In HSPICE, the simulation of the photocurrent is carried out by placing a new photocurrent source I_{ph} in parallel with the p-n junction, as illustrated in Fig.3.1.

This photocurrent source obeys the photocurrent equation 3.1. The direction of the photocurrent source is in consistance with that of the reverse biasing voltage.

Hence, the diode current consists of the reverse junction current (leakage current) and the photocurrent as separate entities. Under such conditions as the resistance R_L is small and the junction remains reverse-biased during the photocurrent pulse, the photocurrent entity will be dominant when light is projected onto the p-n junction.

3.1.2 The modeling of BJT photocurrent in HSPICE
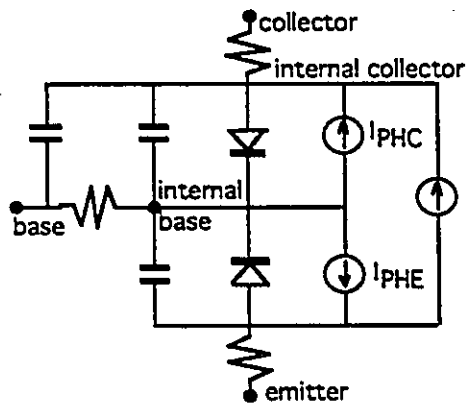
Fig.3.2 BJT equivalent circuit for transient analysis.

A BJT is merely a pair of opposite connected diodes sharing the same base region. The e-b junction is forward-biased and b-c junction is reverse-biased.

To this extent it is possible to re-present the photocurrent sources in a manner similar to the diode. Add two independent current sources connected in parallel

with their corresponding diode. as illustrated in Fig.3.2. However. in the case of the min. size emitter, the small emitter photocurrent source is often negligible compared to the large collector photocurrent source I_{PHC}.

The BJT model is required for simulation. The BJT model parameters may be obtained by measuring the input characteristic of BJT as well as its output characteristic. Then, the parameter values are input to a nonlinear regression optimization program as the initial values. When the convergent condition is satisfied, the running of the program stopped, the BJT model parameters are extracted.

3.1.3 Summary of photocurrent effect in HSPICE

o The assumptions in HSPICE are distinguished from the optical radiation case. Therefore, there will be a deviation between the HSPICE photocurrent effect simulation results and the measurement results.

o The BJT model in HSPICE is based on the epitaxial process which differs from the CMOS process.

o Even though some assumptions are made in HSPICE, the device measurement is still needed to extract the model parameters.

o Only transition analysis of photocurrent in HSPICE is offered.

## 3.2 THE PSD SIMULATION BASED ON MEASURE-MENT RESULTS

Due to above reasons as well as unaccessible of HSPICE photocurrent effect, the PSD simulation using HSPICE is restricted. The purpose of the device simulation is to use computer computing capability to emulate the device electric behavior. Any kinds of simulation results should match the actual device measurement results, or at least be close to the

measurement results as much as possible. Is there any way to use normal HSPICE model to do the photocurrent effect simulation? Since the diode photocurrent effect is emulated by using an independent current source connected in parallel with the diode, and the photocurrent source is dominated in diode current, compared with the diode leakage current, if the relationship of diode photocurrent vs. light power is known, the diode photocurrent value at a certain level of light power can be used as the magnitude value of the photocurrent source. This is the method of PSD simulation based on measurement results described below.

3.2.1 Photo diode and its simulation

The same schematic of photo diode as that in HSPICE is used, seen Fig.3.1. The reverse characteristic of the diode, as illustrated in Fig.3.3, should be carefully measured by using a digital volt-meter and an electrometer.

Fig.3.3 The reverse characteristic of photo diode
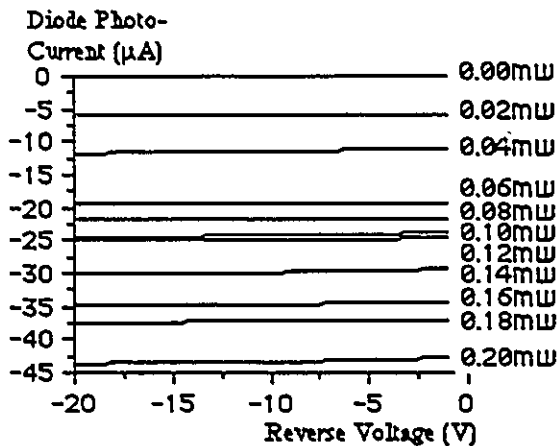
From Fig.3.3, it can be seen that the reverse diode current is almost a horizontal line with the change of applied voltage at a certain level of light power, in other words, the current is a constant. Every line represents a certain diode photocurrent level corresponding to a certain light power level.

This characteristic is a foundation of the PSD simulation. Different IC process requires its own model card deriving from the measurement results. Hence, this method can meet the needs of different process and eliminate the deviation deriving from assumptions.

A diode model card is provided below for reference.

```
.MODEL       DI01   D(LEVEL=1
+IS=1.732E-12      CJO=5.8p    N=1.49      BV=50       RS=0.5
+EG=1.11    IBV=1.0E-03    GAP1=7.02E-4      GAP2=1.11E+03
```

3.2.2 Photo BJT and its simulation

1. The photo BJT equivalent circuit for simulation

1.2μm BJT   3μm BJT

Fig.3.4 Photo BJT equivalent circuit
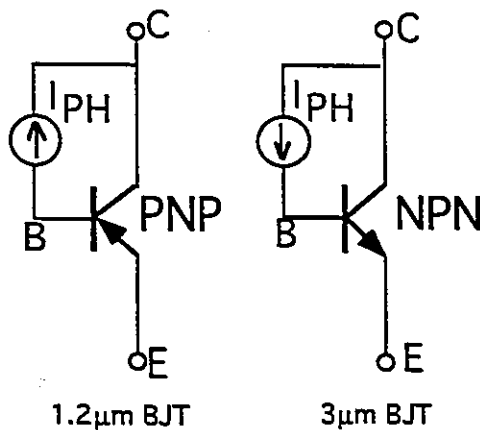
As mentioned in Chapter 1, the vertical BJT is always adopted in CMOS process. The 3μm NPN BJT and 1.2μm PNP BJT are all the substrate BJTs. The diode between p-well and n-substrate as well as the diode between n-well and p-substrate construct the major photo element of a CMOS photo BJT. In terms of the comparison of the testing result, the emitter is better used in minimum size, $9 \times 9 \mu m^2$ in 1.2μm case, compared with the b-c diode size, $(100 \times 100-9 \times 9) \mu m^2$. The e-b diode is negligible. Therefore, the photo BJT equivalent shown in Fig.3.4 may be employed to do the simulation.

2. Two CMOS BJT model cards

The BJT model cards are obtained by measuring the BJT dc characteristic and keeping modification of the model in the device simulator (Bipole and PdFab) until the simulation plot closely resembled the measured results.

The parameter I_{KF} and I_{KR} affect the prompt down portion. The parameter VAF and VAR affect the flat portion. The gap between two I_c lines is affected by I_b (photocur-

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rent source).

Since the substrate BJT is adopted, the substrate BJT model is needed.

Two CMOS substrate BJT models are provided below.

a. The 3μm substrate BJT model

.MODEL   QSUBNPN NPN

+ BF=250   BR=18   IS=46f   RB=2.5k   RC=2k   RE=10

+VAF=140   TF=5NS   TR=15NS   CJE=58.7f   VJE=.7   MJE=.5

+CJC=21.5F VJC=.7   MJC=.5

b. The 1.2μm substrate BJT model

.MODEL   QSUBPNP   PNP

+IS=1.53E-17   ISE=7.09E-13   ISC=6.77E-12

+IKF=2.93E-05   ISR=6.17E-01   TF=6.91E-04

+RB=1.43E+02   RBM=1.16E+02   IRB=7.78E-06

+RE=1.10E+01   RC=1.00E+03   PTF=5.74E+01

+CJE=1.27E-14   CJC=5.99E-14   CJS=1.15E-13

+VJE=7.78E-01   VJC=6.59E-01   VJS=7.00E-01

+MJE=4.66E-01   MJC=4.97E-01   MJS=5.00E-01

+FC=5.00E-01   XCJC=6.18E-02   TR=1.47E-06

+TF=6.94E-09   VTF=2.81E+02   XTF=6.11E+00

+BF=3.55E+01   VAF=1.00E+02   XTB=0.00E+00

+BR=2.08E-01   VAR=3.87E+01   NE=2.00E+00

+NC=2.00E+00   NEPI=1.00E+00   QCO=1.55E-13

3. The HSPICE netlist for photo BJT simulation


```
.options sda=2
vdd vdd! gnd! dc 5
ioptical 0 2 -34.4u
vc /vc gnd!
ve /ve gnd! 5v
.dc vc 0v 5v 0.1v
.print v(/vc) i(r2)
.plot v(/vc) i(r2)
* net 1 = vdd!
* net 0 = gnd!
* net 2 = /vb
* net 3 = /q7.e
* net 4 = /q7.c
* net 5 = /ve
* net 6 = /vc
```

```
.model          sub_pnp        pnp
+is=1.53E-17        ise=7.09E-13        isc=6.77E-12
+ikf=2.93E-05       isr=6.17E-01        tf=6.91E-04
+rb=1.43E+02        rbm=1.16E+02        irb=7.78E-06
+re=1.10E+01        rc=1.00E+03         ptf=5.74E+01
+cje=1.27E-14       cjc=5.99E-14        cjs=1.15E-13
+vje=7.78E-01       vjc=6.59E-01        vjs=7.00E-01
+mje=4.66E-01       mjc=4.97E-01        mjs=5.00E-01
+fc=5.00E-01        xcjc=6.18E-02       tr=1.47E-06
+tf=6.94E-09        vtf=2.81E+02        xtf=6.11E+00
+bf=3.55E+01        vaf=1.00E+02        xtb=0.00E+00
+br=2.08E-01        var=3.87E+01        ne=2.00E+00
+nc=2.00E+00
+nepi=1.00E+00
+qco=1.55E-13
```

```
* pnp(0) = /q7
q/Q7 /Q7.c /vb /Q7.E sub_pnp
* resistor(1) = /r1
```
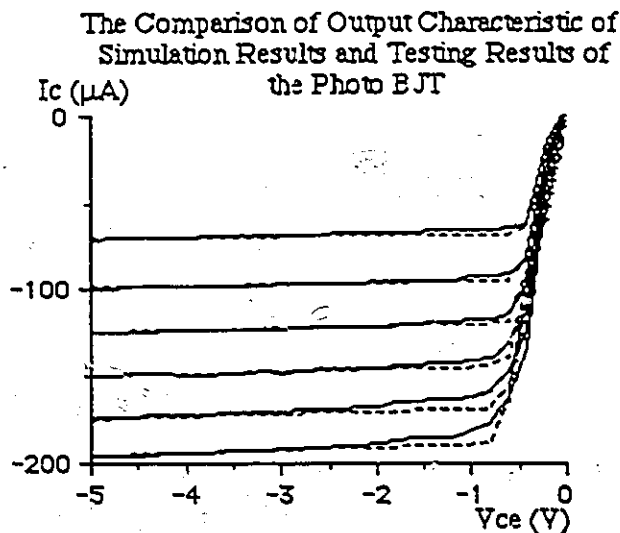
r/R1 /Q7.c /vc 1k
* resistor(2) = /r0
r/R0 /vc /Q7.E 1k

.end

4. The comparison of simulation results and measurement results

The Comparison of Output Characteristic of
Simulation Results and Testing Results of
the Photo BJT

Fig.3.5 Plot of simulation and testing results of BJT

The simulation results of the photo BJT under illumination and the measurement results are shown in Fig.3.5. It can be seen that they match quite well except the transition region between the prompt down portion and the flat portion of the characteristics.

3.3 SUMMARY OF SIMULATION BASED ON MEASUREMENT RESULTS

o The BJT model parameters should be modified by using measured data to let simulation rsults match measurement results as much as possible.

o In the photo BJT equivalent circuit, the e-b diode can be neglected for simplification due to the adoption of minimum size emitter. Therefore, only the b-c diode is considered as a major photo element in a photo BJT.

The neglection simplifies the question without affecting the simulation accuracy.

o Using this method, either DC or transition analysis can be proceeded, depending on the selection of assumed photocurrent source (DC source or pulse source).

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CHAPTER 4

THE MEASUREMENT
AND COMPARISON
OF THE PSD

4.1 THE MEASUREMENT OF THE PSD

The fundamental function of the photo sensitive devices is to convert optical signal into electrical signal. Therefore, an optical system will be involved.

The measurement of the PSD is rather critical because:

o The optical system is very sensitive.

Any minor dust particle will cause a large variation of light power projected onto the PSD, resulting in a large measurement error. A reliable optical system is indispensable for accurate measurement of the PSD.

o The size of the PSD is quite small.

It is very difficult to a project light beam onto the surface of a certain PSD cell. The size of the light beam dot should be small enough to project onto only one single PSD cell. The light beam dot should be able to move cell by cell. Hence, a

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precise measurement system is required.

o The photocurrent of the PSD is extremely low, around pA - μA order.

The very weak photocurrent will be drowned out by any electrical-magnetic inter-ference so that not only a sensitive measurement instrument but also the proper shielding and grounding are needed.

A good photocurrent testing method should have the following features:

1) simplicity.

The test equipment or instruments should be popular, commercially available and inexpensive.

2) enough accuracy.

The test results should be accurate enough, reasonable and match the theoretical analysis.

3) reliability.

The test method should possess good repeatability.

As mentioned above, the conversion from optical signal to electrical signal is the fundamental function of the PSD. The conversion efficiency is represented by the quantum efficiency which is defined as the generated electron-hole pair by each photon. The photo-current is the integration of the photo-generated carriers with respect to the integration time. It is the basic attribution of the PSD. The larger the photocurrent, the higher the quantum efficiency of the PSD, the better the PSD.

4.1.1 The test methodology of the photocurrent

In terms of the features of the PSD measurement mentioned above, a simple PSD test method is designed, as illustrated in Fig. 4.1. The test system consists of:

1) A He-Ne laser light source.

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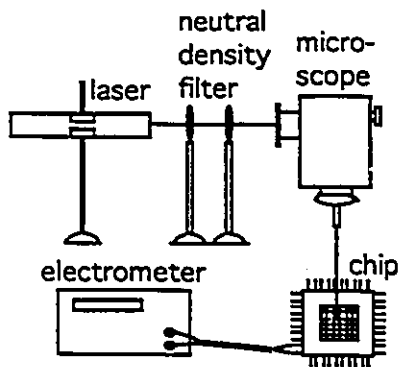2) A set of neutral density filters used as the light attenuator.

3) A microscope used to position the individual photo cell.

4) An electrometer used to measure the weak level photocurrent of the PSD.

neutral
density micro-
laser filter scope

Power Meter

Probe

Step 1: Calibration

neutral
density micro-
laser filter scope

electrometer chip
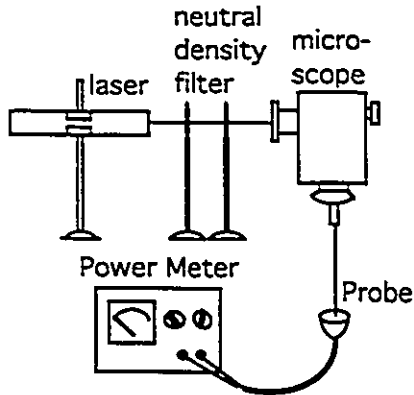
Step 2: Measurement

Fig. 4.1. The diagram of the PSD measurement

5) A power meter used to measure the light power instead of light intensity of the laser beam.

The He-Ne laser is selected as the light source because:

o It is a monocolor light source (mono-frequency, monowavelength) so that the power meter can be easily calibrated at the same wavelength as that of the laser beam, thereby reducing the measurement error.

o It is a very intensive light so that the wide range of intensity is likely obtained by means of an attenuator.

o It is a quite stable light source which ensures a stable generation rate of the electron-hole pairs.

The neutral density (ND) filter sets make possible the attenuation or combining of beams in a wide range of irradiance ratios with no significant dependence on wavelength. Beams can be attenuated to levels at which photometers or radiometers are more accurate and linear. Initial beam irradiances can then be calculated from accurately known filter densities [4.1].

The selection of the ND filter instead of an adjustable attenuator is due to its good repeatability. The adjustable attenuator is found to have the sharp attenuation characteristic at some intensity levels caused by dust, mildewy dot on the aluminum film surface of the

attenuator, resulting in a large variation of light power whenever the test is repeated by looking at the same scale of the attenuator.

By using ND filter set, each of the three chips was tested three times respectively and the same results were obtained for each of them. The results in Table 4.1 show that the good test repeatablility can be obtained by using the ND filter set.

Table 4.1

ND filter	light power	chip 1.2μm_3	chip 1.2μm_4	chip 1.2μm_5
Dark	0.0 mw	0.0263 pA	0.0157 pA	0.0532 pA
ND4 + ND8	0.01 mw	112.70 μA	112.04 μA	110.47 μA
ND8	0.055 mw	127.97 μA	128.85 μA	128.37 μA
ND4	0.12 mw	130.42 μA	131.19 μA	130.86 μA
Nothing	0.50 mw	137.86 μA	139.62 μA	138.31 μA

The adoption of the microscope enables the light dot to move from one PSD cell to the another.

4.1.2 The measurement of the forward characteristic of the photo BJT

The forward characteristic of a photo BJT, which can be used to extract the BJT model parameters, can be measured by using the HP4145B Semiconductor Parameter Analyzer, easily and quickly. However, care should be taken in the low level current region as the interference will cause a large testing error. Proper shielding cable should be employed to eliminate the effect of the interference.

4.1.3 The measurement of the reverse characteristic of the photo diode

The photo diode is a basic PSD element, often applied in reverse voltage. The photo BJT is a PSD whose one junction between base and collector served as a photo diode. The

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diode between the source and the substrate of a photo MOS also served as a photo diode.

It was found that the photocurrent values of the photo diode, above or below zero volt, are identical by using HP4145B with the general wires. This conflicts the semiconductor theory. The problem is solved by the use of shielding cable. However, the photocurrent values below zero volt (reverse characteristic) are found to decrease linearly down to 32 mA by using HP4145B. This seems to be unbelievable as well. **The reverse saturation current of the diode should be a constant value** according to the semiconductor theory. The low input impedance of the HP4145B is probably the cause of the obvious error.

For measuring the reverse characteristic of the diode, a digital voltmeter and an electrometer with high input impedance are recommended for measuring weak current in the case of the high output impedance of the PSD.

4.1.4 The problems in measurement of the PSD

a) Shielding

Every test environment is surrounded by sources of stray currents. These current can originate from vibrating cables, electrostatic coupling. Stray currents add to the desired source current, producing inaccurate readings from the ammeter.
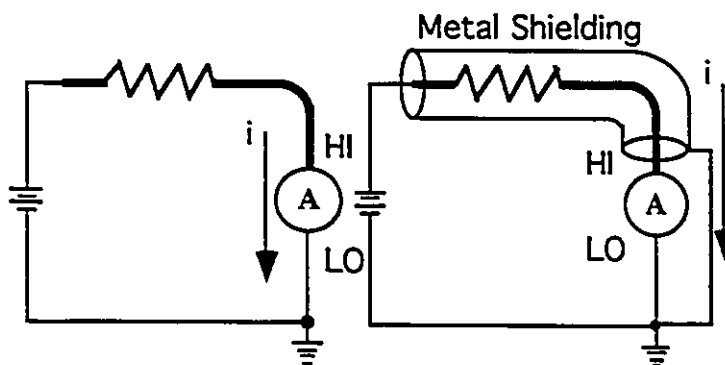

Fig.4.2 The diagram of shielding effect

Fig.4.2 illustrates a simple system. To determine where a stray current would flow, one should identify the system's high impedance lead where the path of least resistance flows through the mea-

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surement instrument. Shielding leads may prove helpful. By connecting the shield to the single ground, a low-resistance path around the meter will be created and the measurement error will be reduced.

Vibration will cause friction between cable conductors. This friction generates static charges, producing stray current.

The electromagnetic field is the main interference source. To reduce the effects of electromagnetic coupling, the test system has to be kept away from AC voltage sources or all charged objects including people. Do not walk around the test fixture, or use a large shielding case to get away with the operator. Also, the electromagnetic field can come from vibration and coupling between leads. The shielding cables and shielding case are recommended. The shielding cable has to be tied in place to avoid movement.

b). Grounding

Even though the shielding wire or cable is adopted, improper grounding can still produce the unexpected ground loop current which will add to the measured current, resulting in a measurement error.

A system is in either a floating or grounding case. When the signal source is floating, the receiving end should be connected to ground. Then, the shielding should be grounded at the receiving end. When the receiving end is floating, the shielding should be connected to the ground at the signal source end. If both signal source end and receiving end are grounded respectively, then the shielding should be connected to the ground.

When low current measurements are proceeded, guarding can be used to reduce the effects of leakage current. Voltage at the guard terminal is held at the same potential as the stimulate Measurement Unit output voltage. The guard terminal cannot be connected to the common terminal.

4.2 THE CHARACTERISTIS OF THE PSD PHOTO-CURRENT VS. LIGHT POWER

4.2.1 The diode reverse current vs. light power

The diode characteristic of the reverse current vs. light power is illustrated in Fig.4.3, which can be used to determine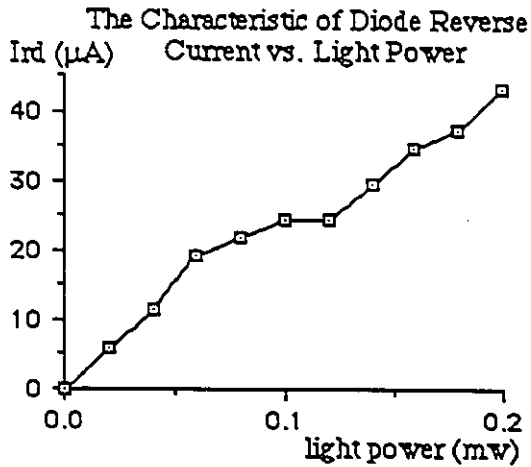 the magnitude value of the independent current source representing the photo effect, e.g., if the range of light power is known, the minimum and maximum values of the diode reverse current corresponding to the minimum and maximum values of the light power can be adopted as the magnitude values of the assumed photo current source for simulation. The measurement values of the diode reverse current vs. light power can be found in Appendix III.

The Characteristic of Diode Reverse
Ird (μA)   Current vs. Light Power

Fig.4.3 The diode characteristic of the reverse current vs. light power

4.2.2 The Comparison of the Photo BJT and Photo MOS in 3μm and 1.2μm Processes

Photocurrent of 3μm BJT and MOS
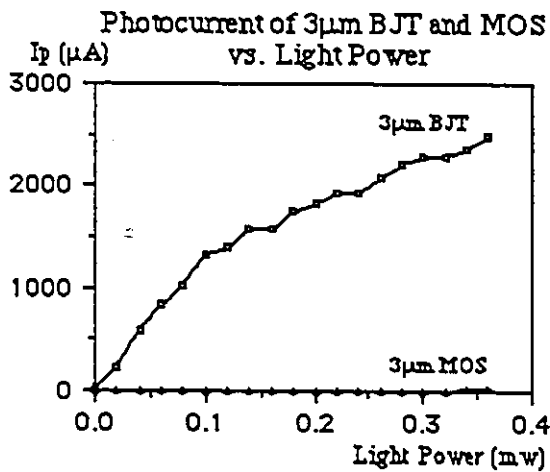Ip (μA)   vs. Light Power

Fig 4.4 Comparison of 3μm photo BJT and photo MOS

Photocurrent of 1.2μm BJT and MOS
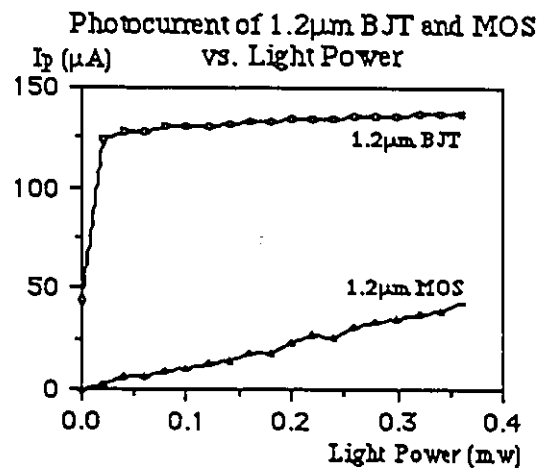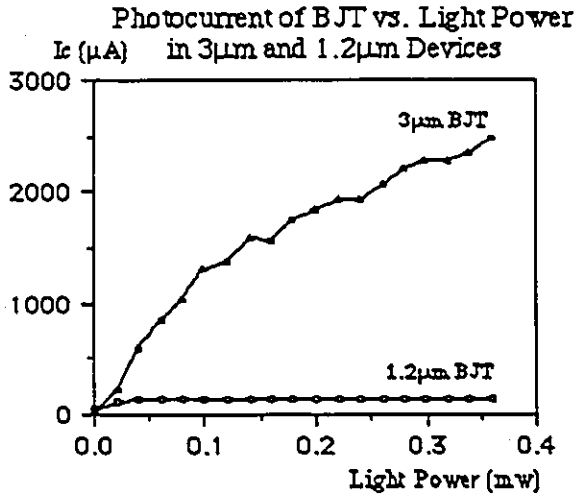Ip (μA)   vs. Light Power

Fig 4.5 Comparison of 1.2μm photo BJT and photo MOS

From Fig 4.4 and Fig 4.5, it can be seen that the photocurrent of BJT is always higher than that of MOS in either 3μm or 1.2μm process because BJT has higher current gain than that of MOS.

4.2.3 The characteristic of 1.2μm BJT Ip and 3μm BJT Ip vs. light power

Fig.4.6 Comparison of 3μm & 1.2μm BJT

The photocurrent of the 3μm BJT is larger than that of the 1.2μm BJT as seen in Fig.4.6.

The characteristic slope of 3μm BJT is almost 20 times that of the 1.2μm BJT so that the 3μm photo BJT is better than the 1.2μm BJT.

4.2.3 The 1.2μm MOS drain current vs. light power

Fig.4.7 Comparison of 3μm & 1.2μm MOS
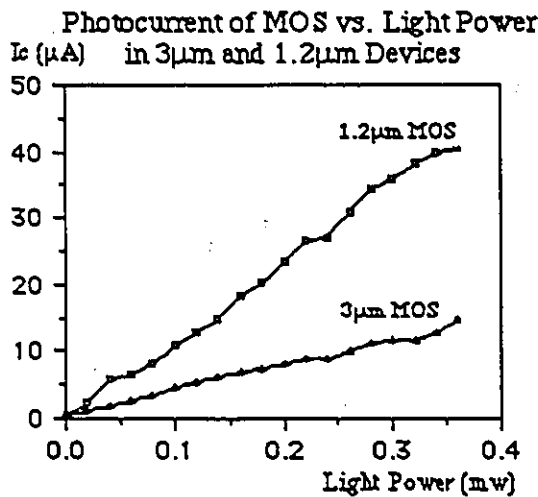
The photocurrent of the 1.2μm MOS is larger than that of the 3μm MOS as seen in Fig.4.7.

The characteristic slope of 1.2μm MOS is almost 2.5 times higher than that of the 3μm MOS so that the 1.2μm photo MOS is better than 3μm photo MOS.

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4.3 THE COMPARISON OF SOME PSD PARAMETERS IMPACT

4.3.1 The comparison of emitter size impact

Table 4.2

Light Power level	Photocurrent with small emitter	Photocurrent with large emitter
low (0.05mw)	15.33 μA	11.96 μA
medium (0.09mw)	28.92 μA	23.66 μA
high (0.16mw)	45.77 μA	38.47 μA

The data in the Table 4.2 show that the photocurrent with small emitter is higher than that with the large emitter. Because the major photo sensing portion of the photo BJT is the b-c diode, the increase of the emitter area will reduce the effective b-c diode area, eliminating the photocurrent.

4.3.2 The comparison of BJT size impact

Table 4.3

Light Power level	1.2μm BJT 50x50 μm²	1.2μm BJT 100x100 μm²	3μm BJT 50x50 μm²	3μm BJT 100x100 μm²
low	4.36μA	10.26μA	10.80μA	18.09μA
medium	8.63μA	19.35μA	23.94μA	29.11μA
high	14.24μA	20.29μA	39.72μA	43.48μA

It can be seen from the Table 4.2 that large size BJT generates higher photocurrent than small size BJT because the increase of the photocurrent is dependent on the b-c diode area.

4.3.3 The comparison of MOS size impact

Table 4.4

Light Power level	1.2μm BJT 50x50 μm²	1.2μm BJT 100x100 μm²	3μm BJT 50x50 μm²	3μm BJT 100x100 μm²
low	0.509 pA	0.783 pA	1.98 μA	3.57 μA
medium	0.932 pA	155.76 pA	4.26 μA	7.54 μA
high	120.2 nA	146.33 nA	7.72 μA	13.58 μA

Large size MOS yields a higher photocurrent than small size MOS from the Table 4.4.

4.3.4 The comparison of conventional BJT with FEM (Field-Effect Modified) BJT

Table 4.5

light power	50x50μm² BJT	50x50μm² FEM BJT	75x75μm² BJT	75x75μm² FEM BJT	100x100μm² BJT	100x100μm² FEM BJT
low	11.80 μA	14.39 μA	16.81 μA	20.09 μA	18.09 μA	23.25 μA
medium	23.94 μA	31.55 μA	32.54 μA	39.89 μA	29.11 μA	36.65 μA
high	39.72 μA	51.94 μA	47.55 μA	60.94 μA	43.48 μA	56.85 μA

The FEM BJT photocurrent is higher than that of the normal BJT (same size) from the Table 4.5.

4.4. SUMMARY

Through the comparison of the measurement results of various PSDs in both 3μm and 1.2μm technology, the following summary can be drawn:

o 3μm FEM BJT PSD is the best CMOS PSD among the tested cells.

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o The photocurrent of the BJT is always higher than that of the MOS.

o 3μm BJT is better than 1.2μm BJT.

o 1.2μm MOS PSD is a little bit better than 3μm MOS PSD.

o The characteristic of photocurrent vs. light power of diode can be used to determine the simulation range.

The value of the photocurrent at different light intensity level (light power) is different. However, if the range of the light power in a certain application is known, we only need to determine the magnitude values of assumed independent photocurrent source at minimum point and maximum point of the light power range and to do the simulation.

CHAPTER 5

A Base-Stored Intelligent Imaging System (BSIIS)

5.1 THE DESIGN OBJECTIVE OF BSIIS

Based on the measurement and comparison of the PSD, the best PSD is determined which is intended to apply to imaging application.

Charge-Coupled Device (CCD) and Photo Sensitive Device (PSD) such as photo diode, photo MOS, are widely used in the image capture or imaging application. Although CCD has excellent performance in this area, it suffers intrinsic image smear [5.1], reset noise, special request of fabrication process other than CMOS, area consuming for cell isolation as well as impossibility in random access of individual image cell which is requir-ed in the intelligent imaging application such as machine vision and neural network.

For the purpose of the intelligent scanning, the design of optical input is required to have the capability of random access. Each pixel can be addressed separately and indivi-dually. Some of them might be read more than once. Some of them might not be reached at all. This results in a non uniformly scanned image through selective data acquisition which is controlled by the algorithm of computer vision. Therefore, the X-Y addressed PSD array is chosen.

Most of area imaging systems are operated in the charge storage or charge integrated mode which is based on the period sampling of the charges generated by incident light. It can be operated in the low illumination level case. The charge storage operation mode is selected

for the Base-Stored Intelligent Imaging System (BSIIS), because it can easily realize the light detection, the information enhancing, holding and reading out. The sensitivity, linearity with broad dynamic range, blooming protection and noise reduction can be implemented by using the adequate circuitry in this mode. And it can eliminate the dependence of the output voltage on the current gain beta, thus reducing the non uniformity. The output voltage of BSIIS is analog signal which may be converted to the binary values (digital) whenever it is necessary for some applications.

A suitable photo site element for the image-sensing arrays should have high gain [5.1].The output reading of photo diode and photo MOS is in destructive mode due to with no or a little optical gain. The BJT has high transconductance than the MOS or diode, resulting in a very large S/N ratio and high sensitivity. There are two types of BJTs in standard CMOS process, the lateral BJT and the vertical BJT. The vertical BJT has larger h_{fe}, around 35, than h_{fe} of the lateral BJT, below 1 (1.2μm). It is more reliable than the lateral BJT as it is bulk-controlled [5.2]. The signal charges generated by light are stored in a control electrode region (base region). The attempt to use photo BJT as image cell was failed due to the large Fixed Pattern Noise (FPN) and random noise inherent in the amplification-type photo device. Recent development of the Base-Stored Image Sensor (BASIS) [5.3] overcomes these drawbacks This makes it possible that the BJT photo device is utilized in the BSIIS to obtain the excellent performance. However, the vertical BJT suffers large C_{bc}, resulting in the reduction of the spectral range. The FEM structure is utilized to provide a decade improvement in responsivity of the device operating in the charge storage mode by means of reducing effective C_{bc} without reducing the total primary photocurrent and no additional fabrication processing step is required [5.4]. This will be described later.

The noise reduction and the acquirement of linearity with wide dynamic range in the BSIIS is realized by using the hybrid operations of the Base reset and the Emitter reset as well as base forward-biasing, which will be analyzed later.

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The light sensing is periodical, reading can be carried out at any time. A pixel can be read more than once before it is sampled again. A buffer is employed to enable the multiple reading operation.

5.2 THE DESIGN CONSIDERATIONS

The design is to make a 2D array imager with random scan function for use in the intelligent scan systems. The main goal of this design is the availability of random access. Each pixel can be reached separately and independently. Some of pixels might be read at all. Some might be read more than once. The system can generate a regular picture or allow the selective data acquisition which is controlled by the algorithms of computer vision.

The system design has the following considerations:

o An X-Y addressed photo array should be adopted to enable the random access of individual pixel.

o The photo BJT is operated in the charge storage mode.

o The vertical photo BJT is selected due to its larger beta and reliability compared with lateral BJT. Furthermore, the unique FEM phototransistor is employed to reduce the effective base-collector capacitance without affecting the total primary photocurrent and no additional process steps are needed.

o The performance of the BASIS [5.5] is greatly improved by using the hybrid reset operation of base and emitter reset and deep forward-biasing reading operation of the photo BJT, resulting in the FPN and random noise reduction as well as the wide dynamic linear range of responsivity. This scheme is certainly adopted in the BSIIS.

o The use of a buffer keeps the voltage on the storage capacitor constant and separate the sampling operation from reading operation, enabling the multiple reading.

o The system must be implemented by using the standard CMOS technology such as 1.2µm CMOS process which can prevent the adjacent photo devices from crosstalk exist

ing in [5.6].

o The use of ploy layer capacitance other than MOS capacitance enables the stability of the storage capacitor and keeps the charges on it constant.

5.3 THE SYSTEM STRUCTURE OF THE BSIIS

Fig.5.1. The block diagram of the BSIIS
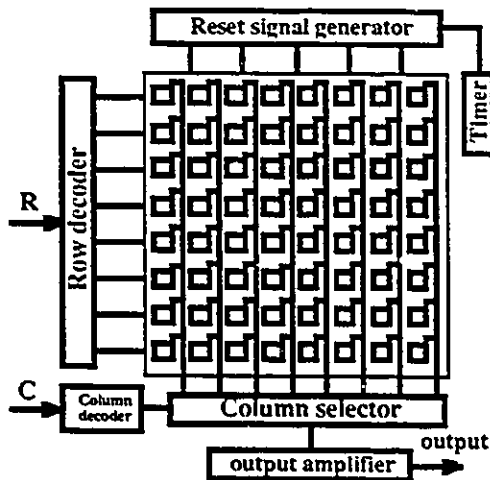
The chip of the BSIIS contains six portions, as illustrated in Fig. 5.1.

1) A two dimensional arrays of 8 rows and 8 columns of imaging cells (digital) converting optical signal into electrical signal.

2) A row decoder and a column decoder (digital) are used to access a particular pixel. The row decoder selects one of the 8 output lines. Each column bus is connected to one single output bus through the column selector. The input terminals of the row decoder and column decoder may be con-trolled by the vision algorithm through the interface.

3) The column selector consists of pass transistors controlled by a column decoder.

4) An output amplifier (analog) transfers the input analog signal coming from the column signal output bus to the output.

5) A reset signal generator (digital) yields the base reset, emitter reset, sampling, and storage capacitor reset signals.

6) A built-in timer (digital) creates the clock signal for whole system. Its frequency may be adjusted by the external resistor and capacitor network.

The advantage of this architecture is that the location of important video signal can

be immediately accessed and processed without wasting time on the other nonrelevant vedio signals. This configuration possesses two basic design features:

a) being able to access randomly to each pixel

b) separating the sensing section from the readout so that each pixel can be read at any time during the integrated period even multiple readings.

The integration time is selected to be the same for each individual pixel for simplifying the design.

5.4. THE PHOTO CELL DESIGN OF THE BSIIS

5.4.1. The circuit configuration of the photo cell

As illuastrated in Fig.5.2, the photo cell block diagram, the input signal of each pixel is the light intensity at the corresponding spot. The photo BJT converts the incident light into an analog voltage signal.

Each cell consists of light detection, photovoltage holding and reading out circuits, as illustrated in Fig. 5.3.
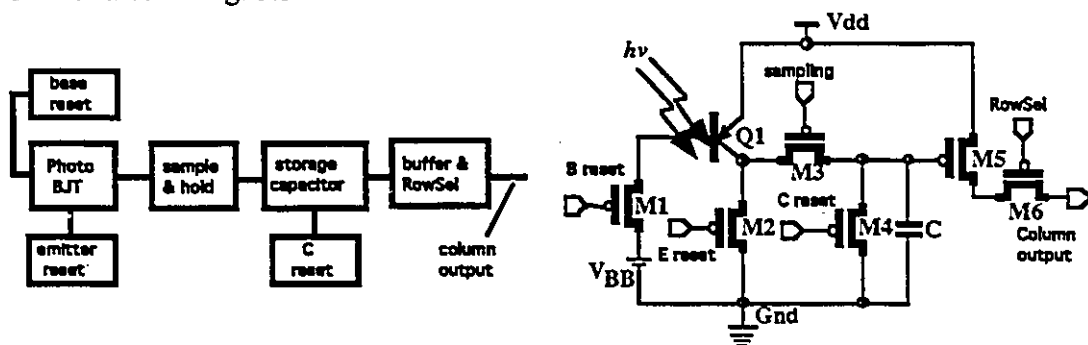

Fig.5.2 The block diagram of the photo cell   Fig.5.3 The schematic of photo cell in BSIIS

Q1 is a vertical PNP phototransistor which is used to detect the light intensity to yield the corresponding photocurrent. C is a capacitive load of Q1, which converts photocurrent into photovoltage and stores the photovoltage for multiple read out. Therefore, the circuit structure is virtually a capacitor-load emitter follower. The signal charges generated by light are stored in a control electrode region, i.e. the base region of Q1.

M3 is a sampling switch which is used to isolate the signal from the output and to separate the sampling from reading. When it is on, the charge stored in the base are amplified by Q1 due to the forward-biasing condition and charged to the storage capacitor C.

To prevent from the mixing of present period sampled signal with previous period sampled signal, which will cause image smear, the previous signal on C has to be discharged before it is recharged by new signal. M4 is required for discharging C.

For the same reason, a base reset operation is required for erasing the old stored charges in the base by discharging the base and for setting the base voltage to the initial state. M1 plays such a role. An alternative is to inject holes into the base from the emitter for recombining the photo-generated electrons. M2 is used for this aim.

For isolating the signal from the output line and keeping the voltage on C constant, M5 (buffer) is adopted. M6 is a switch realizing random access which can be controlled through row and column decoders by the algorithms of the computer vision.

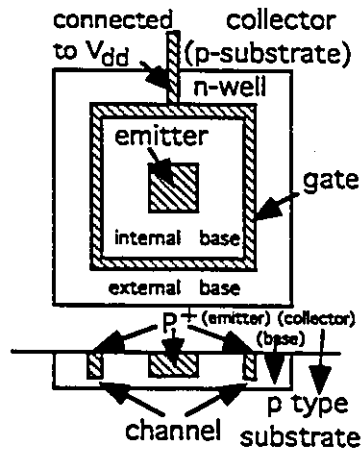## 5.4.2 The FEM Phototransistor

Fig.5.4 Top and central cross section of an FEM vertical phototransistor

The top and cross section of the FEM vertical phototransistor is illustrated in Fig.5.4.

The region inside the annular gate is the emitter of a vertical PNP BJT. The base region is divided by the annular P^+ region into two portions, internal base and external base. These two portions along with the annular P^+ gate form a n-channel junction FET with the gate connected to the BJT's collector. When collector (gate) junction is sufficiently reversed biased, say Gnd, the region under the gate becomes depleted and the

channel connecting the two portions of the base is pinched off so that the effective base-collector capacitance is only that of the internal region whereas the primary photocurrent includes both internal and external photocurrent. Hence, the responsivity of the FEM phototransistor may be increased by increasing the ratio of external to internal base area. The gate can be formed during the emitter diffusion so that no additional processing steps are required.

5.4.3. Analysis of the reset operation

In order to isolate light detection from reading out, the light sensing is periodical while reading can be proceed at any time. The signal stored on C can be read out more than once before it is sampled again. The operating timing chart is shown in Fig.5.5.

The operational sequence includes the steps of the C reset, Base reset, Emitter reset, forward- biased storage and read out operation.
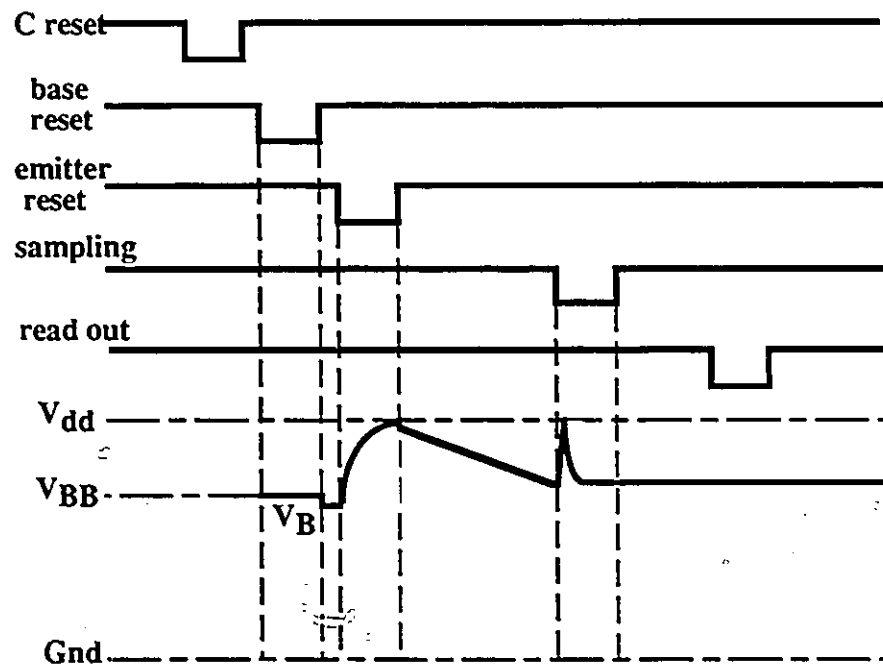

Fig.5.5. The operational timing chart of the BSIIS

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Step 1: The C reset operation

The capacitor C is discharged through M4 in C reset operation.

Step 2: The Base reset operation

The base voltage of Q1 is clamped to reset voltage V_{BB} through M1 in base reset operation while the emitter is in floating state. The value of V_{BB} should be set to the level higher than V_{BF}, the forward voltage drop of Q1, to keep the base-emitter junction forward-biased in the other reset operation, resulting in excellent linearity and no image lag. After the base reset, the base is floating state, keeping the reset potential.

Step 3: The emitter reset operation

The emitter is grounded through M2 in the Emitter reset operation to inject the holes into base from emitter for recombining with electrons generated by light in the previous period of storage time. After emitter reset operation, the emitter is in floating state too.

The emitter reset is the key factor to improve the performance of the BSIIS. The base voltage V_B is the function of emitter reset time t_E for various initial voltages. The various initial base voltages tend to converge to a single line when the initial base voltage is large than a certain value, e.g. $30\,kT/q = 774\text{mv}$. The fluctuations in the initial base voltage decrease drastically with the increase of emitter reset time. Even if there exists a large fluctuation in the initial base voltage, e.g. $30\,kT/q$ to $42\,kT/q$ (774 to 1084mv). The fluctuation (310mv) reduces to less than 2.26mv when the emitter reset time is 1μs. That is why the FPN and random noise are reduced by using emitter reset. Therefore, the hybrid reset combined by base reset and emitter reset is adopted to obtain the excellent performance of the BSIIS.

Step 4: The storage operation

When emitter reset is over, both base and emitter are floating. The base-emitter

junction is forward-biased. When Q1 is being illustrated, the emitter voltage increases linearly following the base voltage.

Step 5: The sampling operation

The emitter is connected to the storage capacitor C through M3. Since the base-emitter junction is forwarded, a large emitter current is allowed, resulting in a quick charge-up of C.

Step 6: The reading operation

The signal on C is transferred to the column bus through M5 and M6. M5 is a buffer which is in a source follower mode to isolate C from column bus, resulting in a constant signal voltage on C. Also, the use of M5 enables multiple readings after the sampling operation.

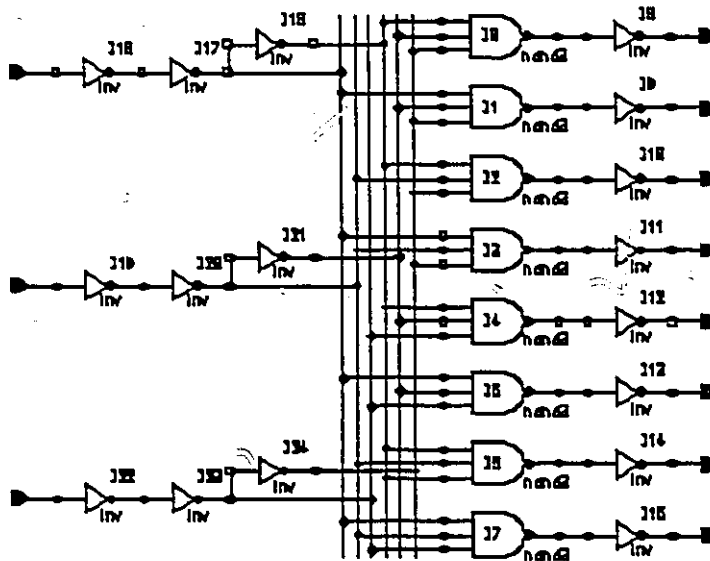# 5.5 THE CIRCUIT BLOCK OF THE BSIIS

5.5.1 Decoder

Fig.5.6. The schematic of the decoder

The row and column decoders used in the BSIIS are normal three input, eight output decoder, as illustrated in Fig.5.6, which are realized by using the CMOS 1.2μm library cell such as NAND3 and inverter (digital).

5.5.2. Column selector

The column selector is actually a large size NMOS pass transistor. Its gate voltage

is controlled by the output signal of the column decoder. It is a large width NMOS transistor. The ratio of width-length is at least equal to or large than ten.
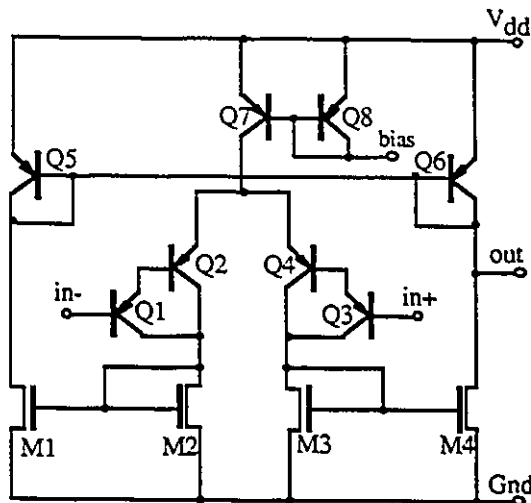
5.5.3. Output amplifier

Fig.5.7. The schematic of output amplifier

The output amplifier, shown in Fig.5.7, is a broad band, BJT, differential linear amplifier which is used to enhance the output voltage of the photo cell. It is a two stage BJT differential amplifier (analog).
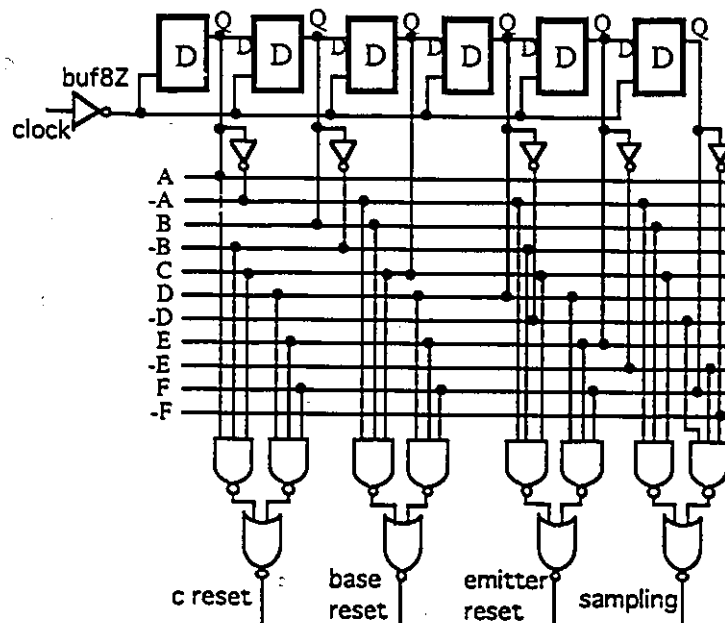
5.5.4. Reset signal generator

Fig.5.8. The schematic of the reset signal generator

The reset signal generator is used to generate the photo cell required reset signals such as the base reset, emitter reset, sampling and storage capacitor reset signals. The generator is a combinational and sequential logic which is composed of the D trigger, NAND3, NOR2 and buffer (library cells), as illustrated in Fig.5.8.

The reset signal generator is simulated. The simulation result matches the requirement of the timing chart in Fig.5.5.

5.5.5. Built-in timer

The first consideration of timer is the ring oscillator. Through simulation, it is found that its frequency is too high (several MHzs) and dependent of the size of the transistors constructing the inverter, thus, non-controllable from outside of the chip.

The period of the timer should be able to be adjusted through external means from the order of μs to the order of millisecond, matching the TV standard.

The built-in timer is simulated by using HSPICE. The simulation result can be seen in Fig.5.9.
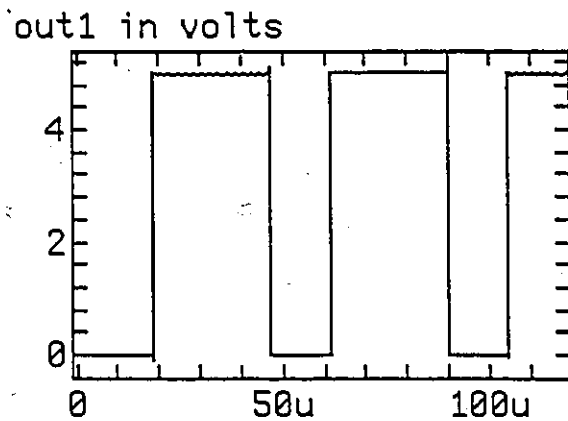

The timer is a clock signal oscillator which frequency can be adjusted through external resistor and capacitor network. It is composed of two comparators (analog), a voltage divider (analog), a novel flip-flop (digital), and a few output buffers (digital), as illustrated in Fig.5.10.

Fig.5.9. The simulation result of built-in timer

The voltage divider provides the two reference voltages (1.7 volt and 3.3 volt). The external RC network creates the linear increasing voltage as the input of two comparators. When the input of the comparator is equal or over 1.7 volt or 3.3 volt, the output of the comparator becomes high level, "1", which is used to trigger the novel flip-flop to generate

a square wave which can discharge the external capacitor through a transistor to form an input saw wave. The output buffer is adopted to enhance and modify the square wave.
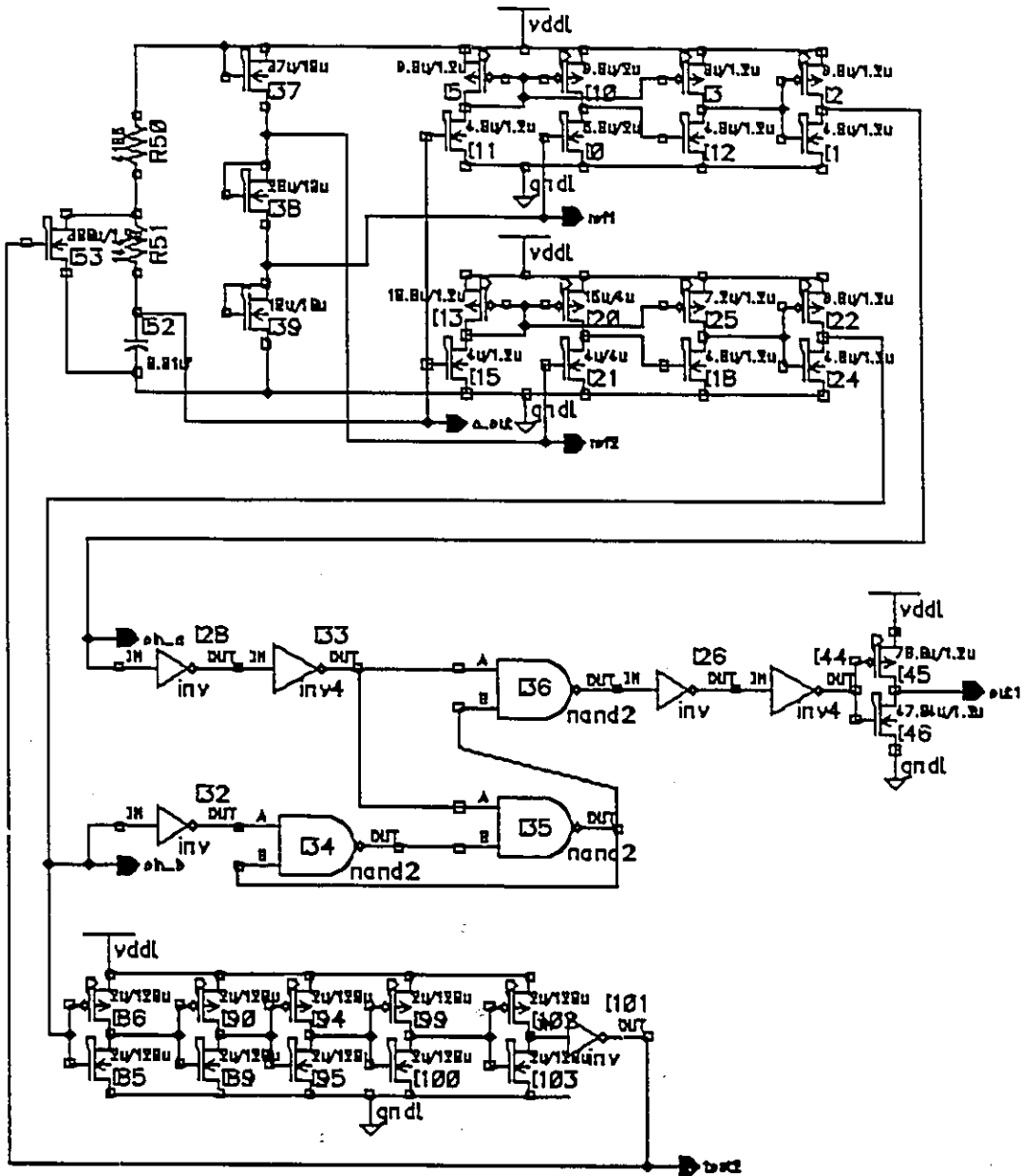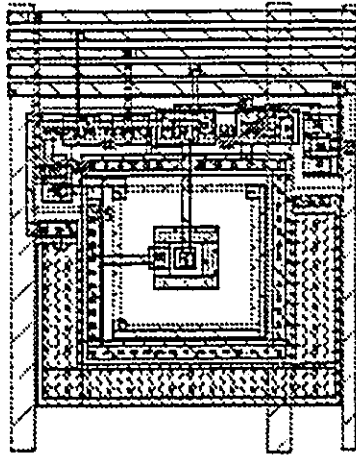

Fig.5.10. The schematic of the built-in timer

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5.6. THE LAYOUT OF THE PHOTO CELL

The photo cell layout of the BSIIS is shown in Fig. 5.11. The central portion is a FEM phototransistor. The upper portion of the phototransistor presents the reset MOS transistors. The surrounding portion of the phototransistor is the storage capacitor C.

Fig.5.11. The layout of the photo cell

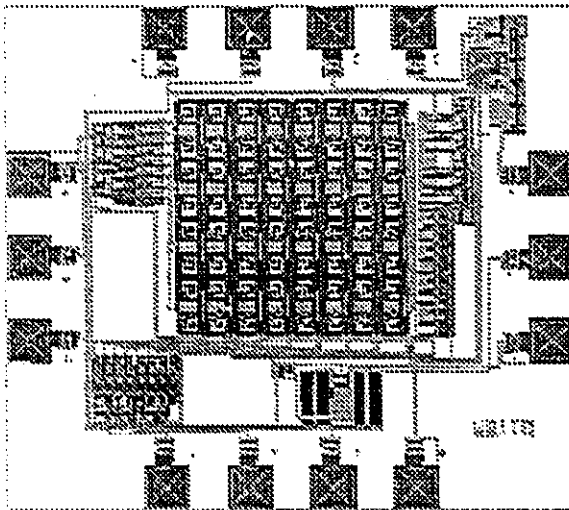# 5.7. THE LAYOUT OF THE BSIIS

The layout of the BSIIS is shown in Fig.5.12. The 8x8 photo BJT array is in the center of the chip. The row decoder is at the left of the array. Below it is the column decoder. An output amplifier is at the bottom of the chip. The reset signal generator is at the right of the array. At the right upper corner is the built-in timer.

Fig.5.12. The layout of the BSIIS

5.8. SUMMARY

On the basis of the latest literatures and our circuit simulation, the testing photo BJT cell and the BSIIS have been fabricated by using 1.2μm CMOS technology.

The BSIIS improves the responsivity comparing with the BASIS in [5.2-5.5], as well as the sensitivity, noise reduction, intercell crosstalk and stability of storage capacitor C comparing with the cell in [5.1].

The BSIIS can be used as the regular imager as well as the intelligent imager which can be applied to the applications such as character recognition, neural computing image processing, etc.

It is possible to incorporate the BSIIS with the processing unit on the same chip, resulting in high integration density, high processing speed and high reliability.

The BSIIS may be potentially scaled down with the evolution of the VLSI technology, resulting in increase of image resolution.

CHAPTER 6

Conclusion

6. CONCLUSION

The design, implementation and testing of three different photo sensitive devices that were fabricated using Northern Telecom's 1.2 and 3.0 micron CMOS technology is presented in the thesis. It can be concluded that:

1. A MOSFET structure can be optimized to enhance and use the parasitic photodiode that is formed between the source and substrate as a photo sensitive device.

2. A conventional BJT structure, with the exception of a much smaller emitter area, can be optimized to enhance and utilize the parasitic photodiode that is formed at the base-collector junction as a photo sensitive device.

3. A field effect modified (FEM) vertical BJT with a collector-connected annular ring around a small emitter area can be used to create a more sensitive and faster responding parasitic photodiode at the base-collector junction that can be used as a photo sensitive device.

4. Each of the three distinct structures can be fabricated in both 1.2 and 3.0 micron CMOS technology.

5. A number of experiments have been carried out on the test cells to measure photocurrent as a function of light intensity using incandescent and LASER light sources. The most sensitive photo sensitive device was formed using 3.0 micron FEM BJT design. Model parameters were extracted from the test results to provide an accurate

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simulation model. A FEM vertical BJT with a base-collector photodiode area of 50x50 microns and an emitter area of 9x9 microns in 1.2 micron CMOS technology is recommended for realizing individual photo sensitive elements.

6. A photo sensitive array, based on FEM BJT photo sensitive device, has been designed that is suitable for use as the input nodes to an artificial neural network that is being employed as an intelligent sensor for process control based on non-contact measurement.

Future work may include integrating individual photo sensitive elements or a complete photo sensitive array into an artificial neural network and improving the design of the photo sensitive array.

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APPENDIX I:

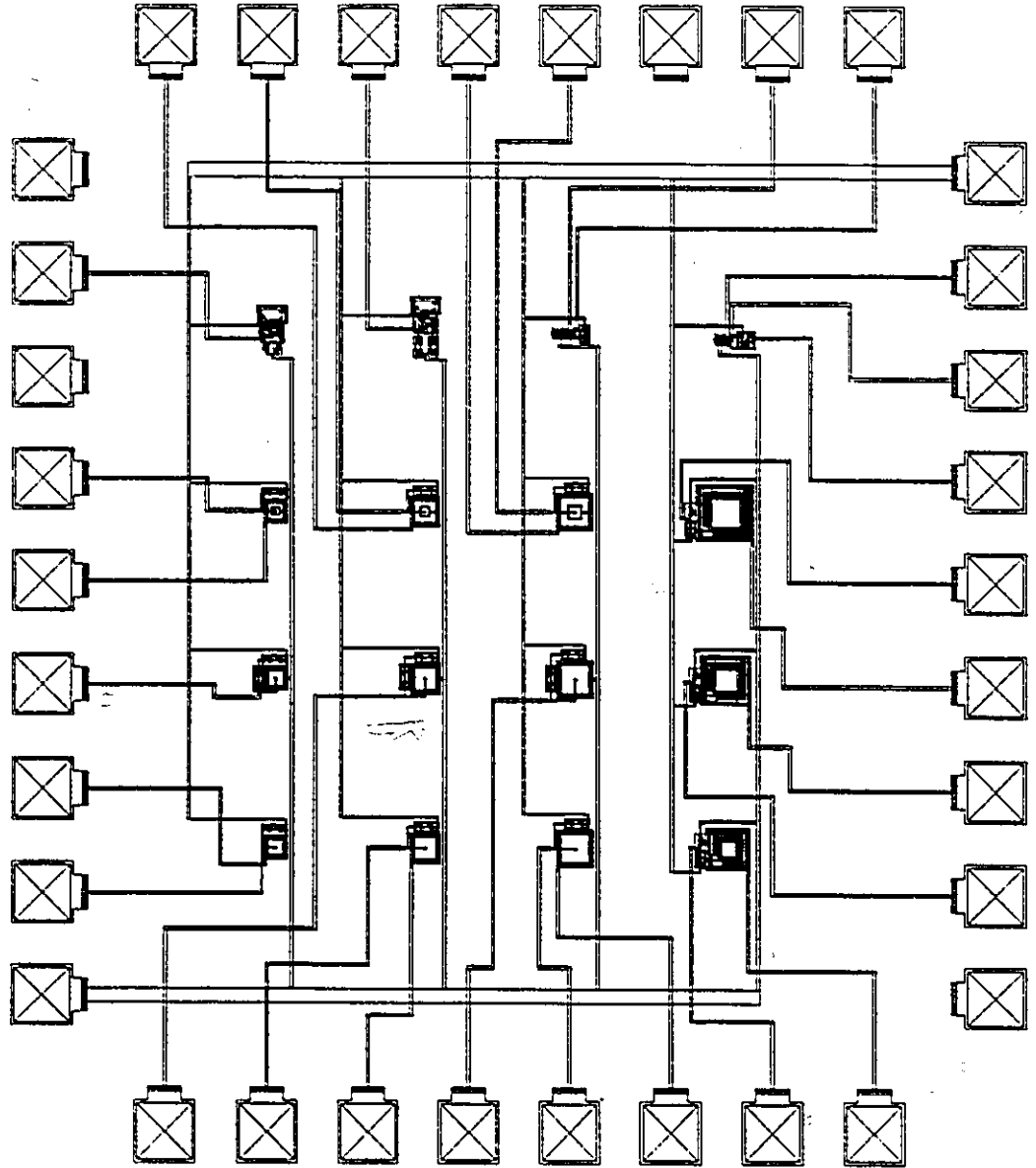## The Layout of Four Chips

PHOTO CELL TEST CHIP LAYOUT (3um)
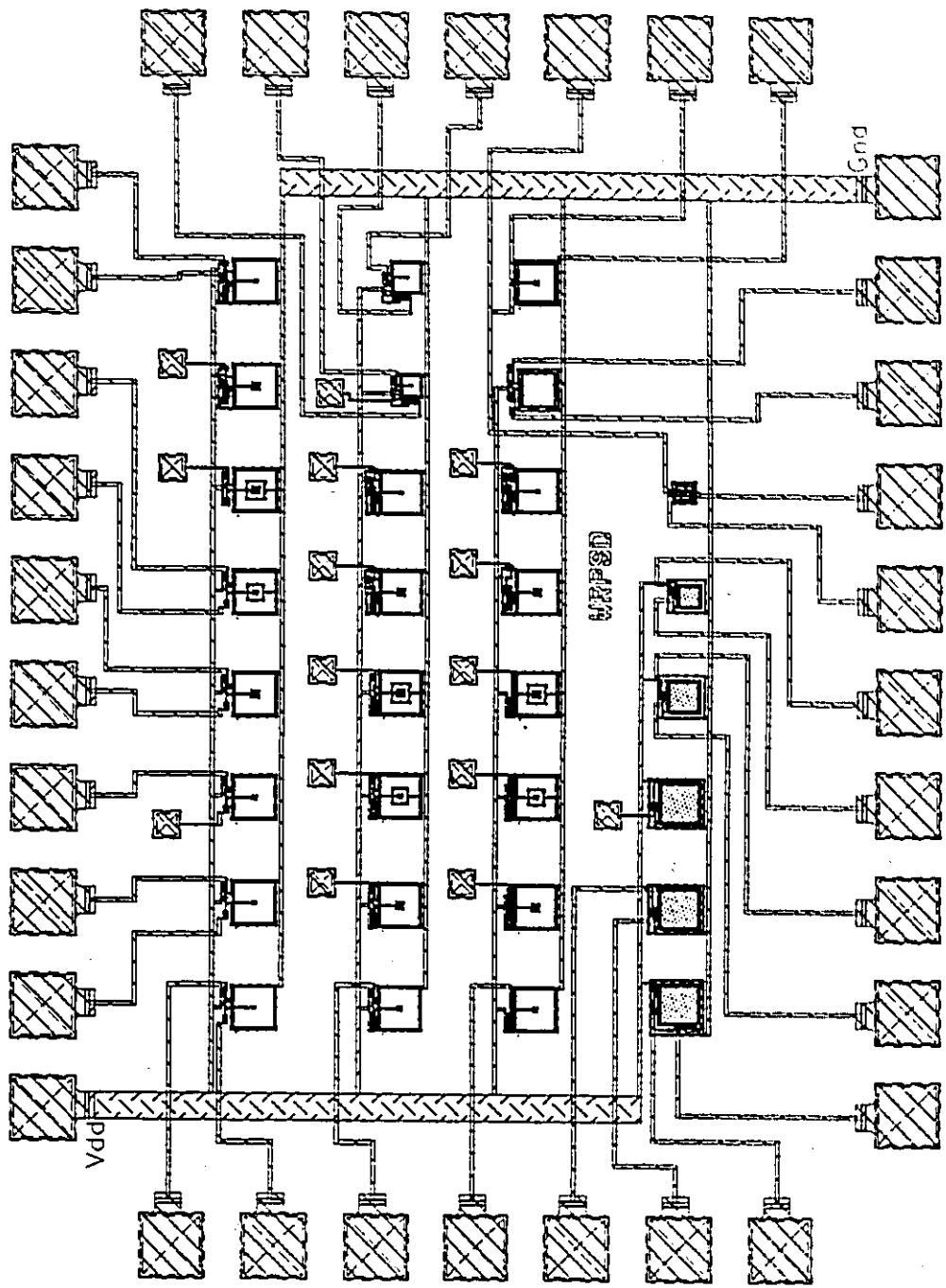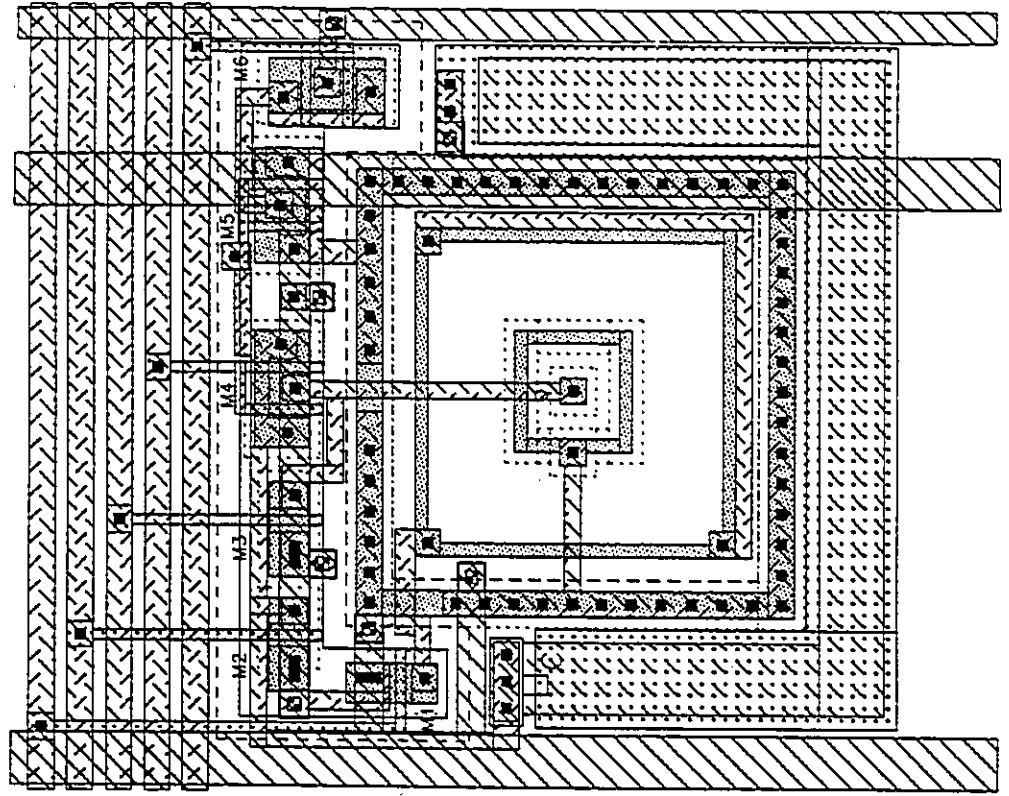
PHOTO SENSITIVE DEVICE TEST CHIP LAYOUT (1.2um)
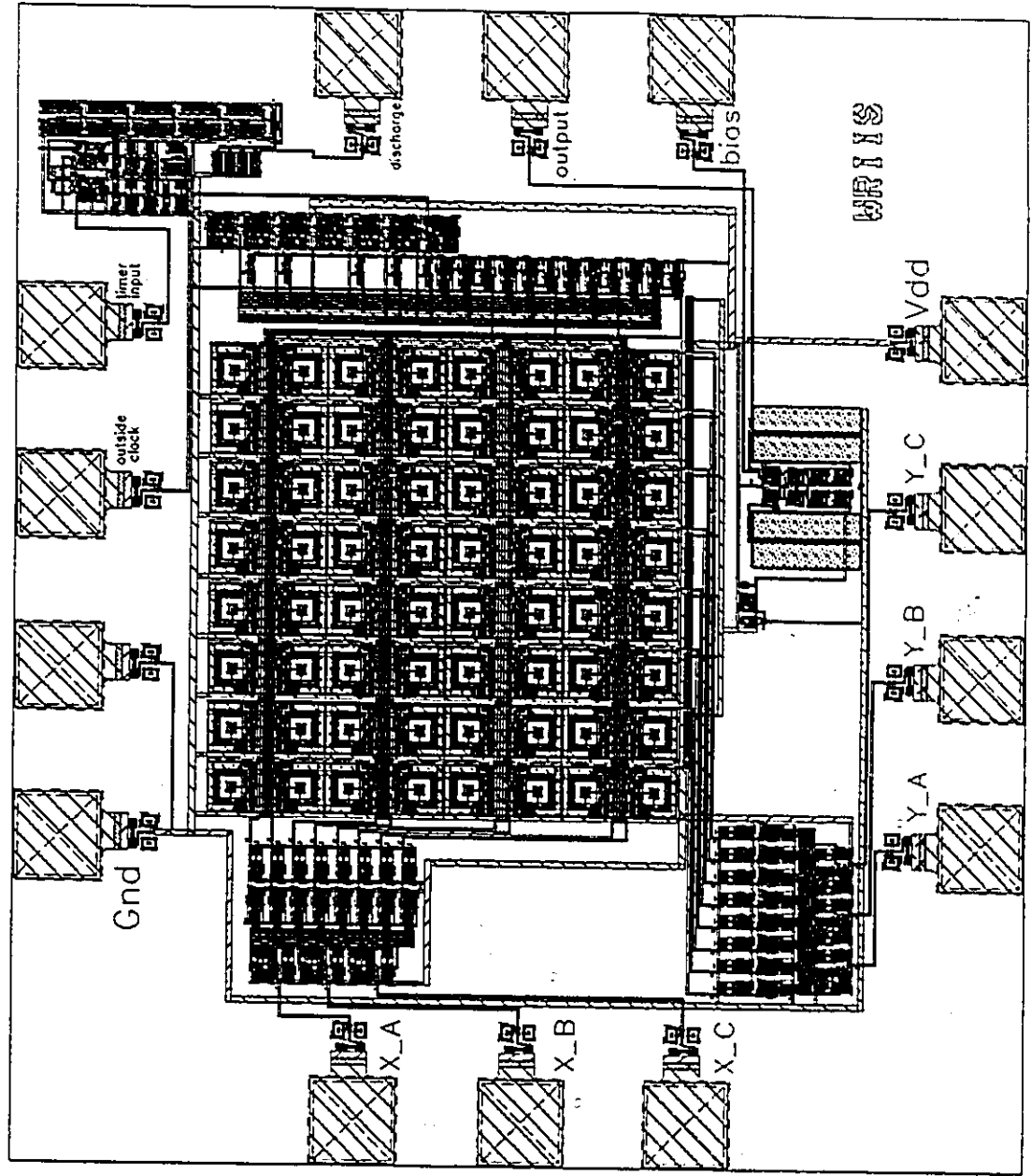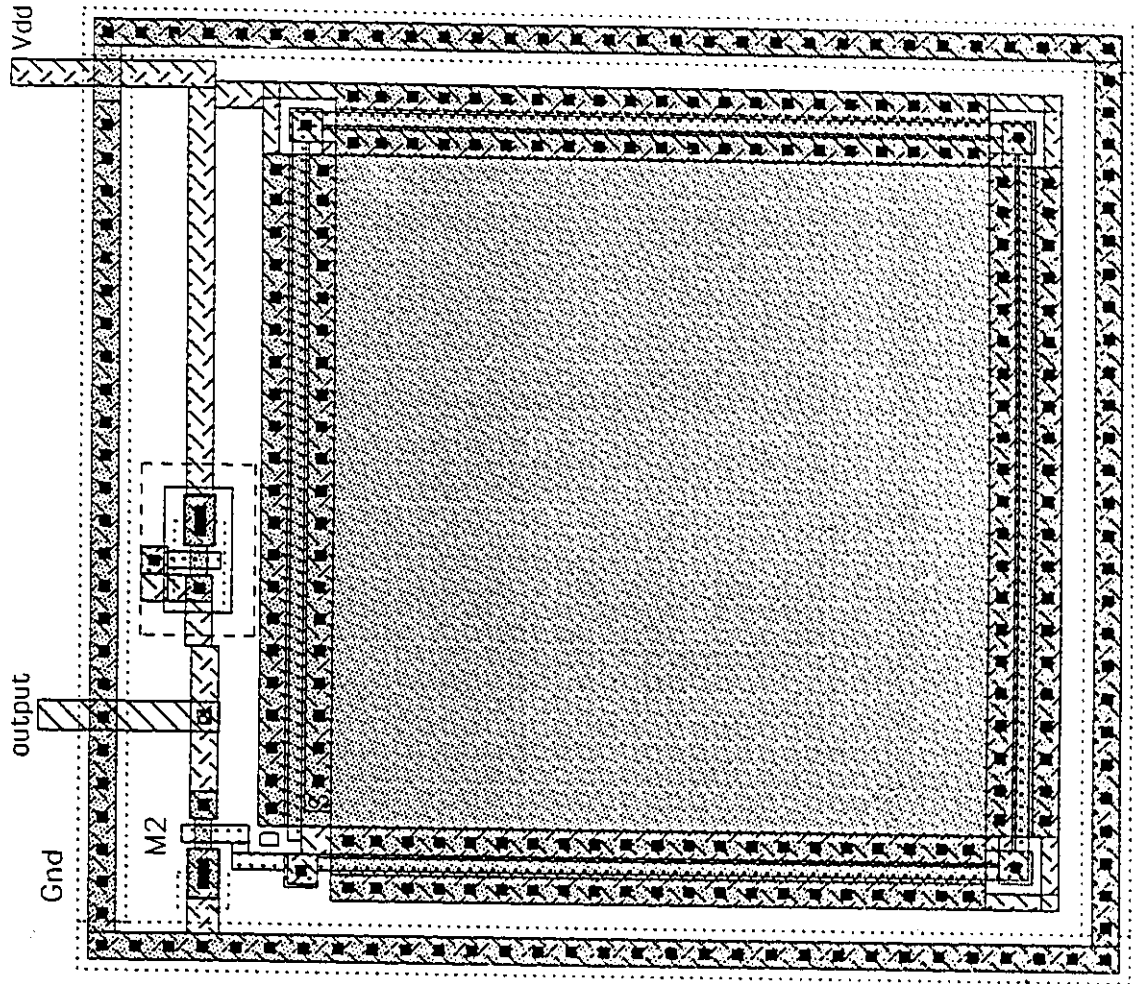
PHOTO CELL OF THE BSIIS

The Base-Stored Intelligent Imaging System (BSIS)

APPENDIX II:

The Layout of Photo BJT and Photo MOS
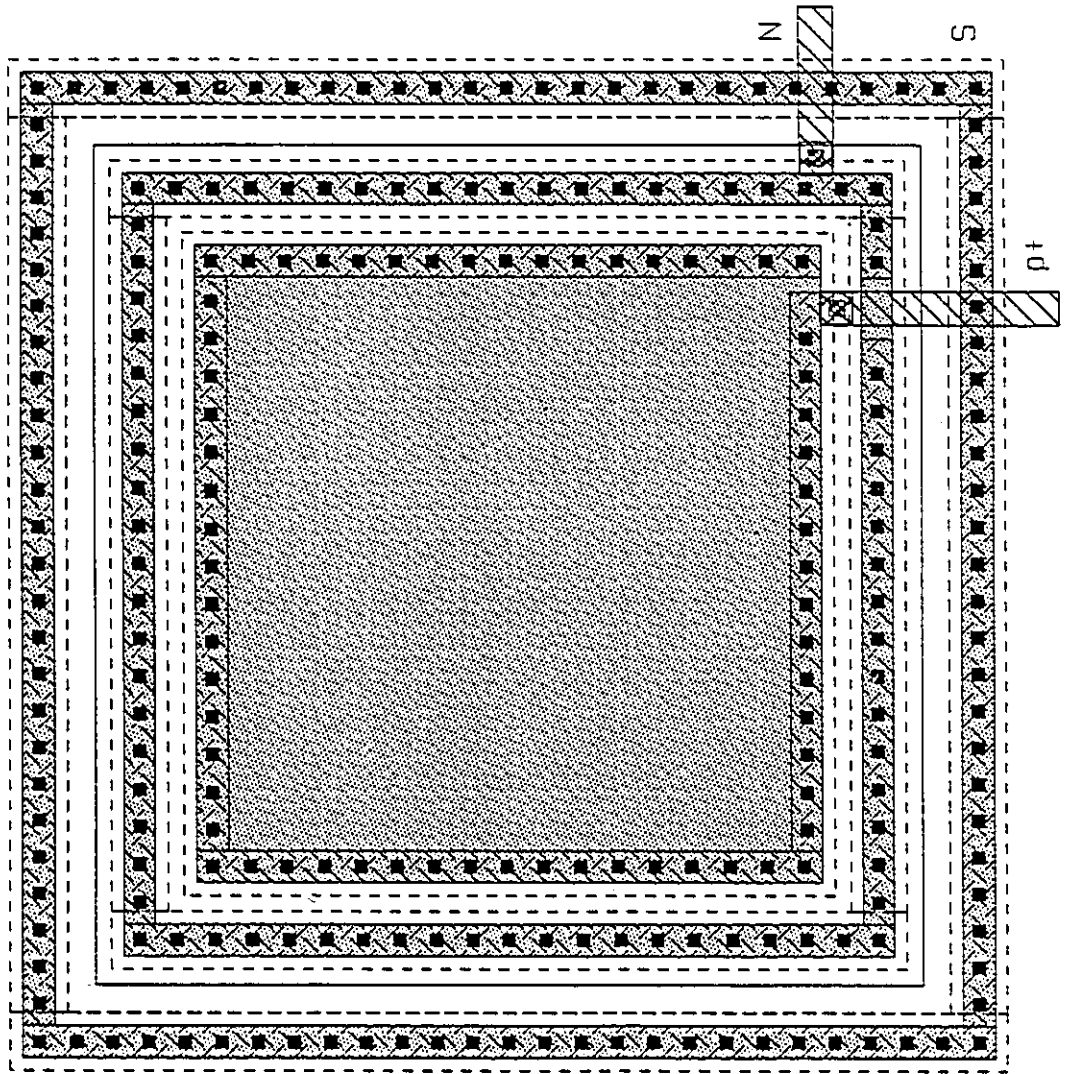
PHOTO NMOS WITH BUFFER (PMOS LOAD)
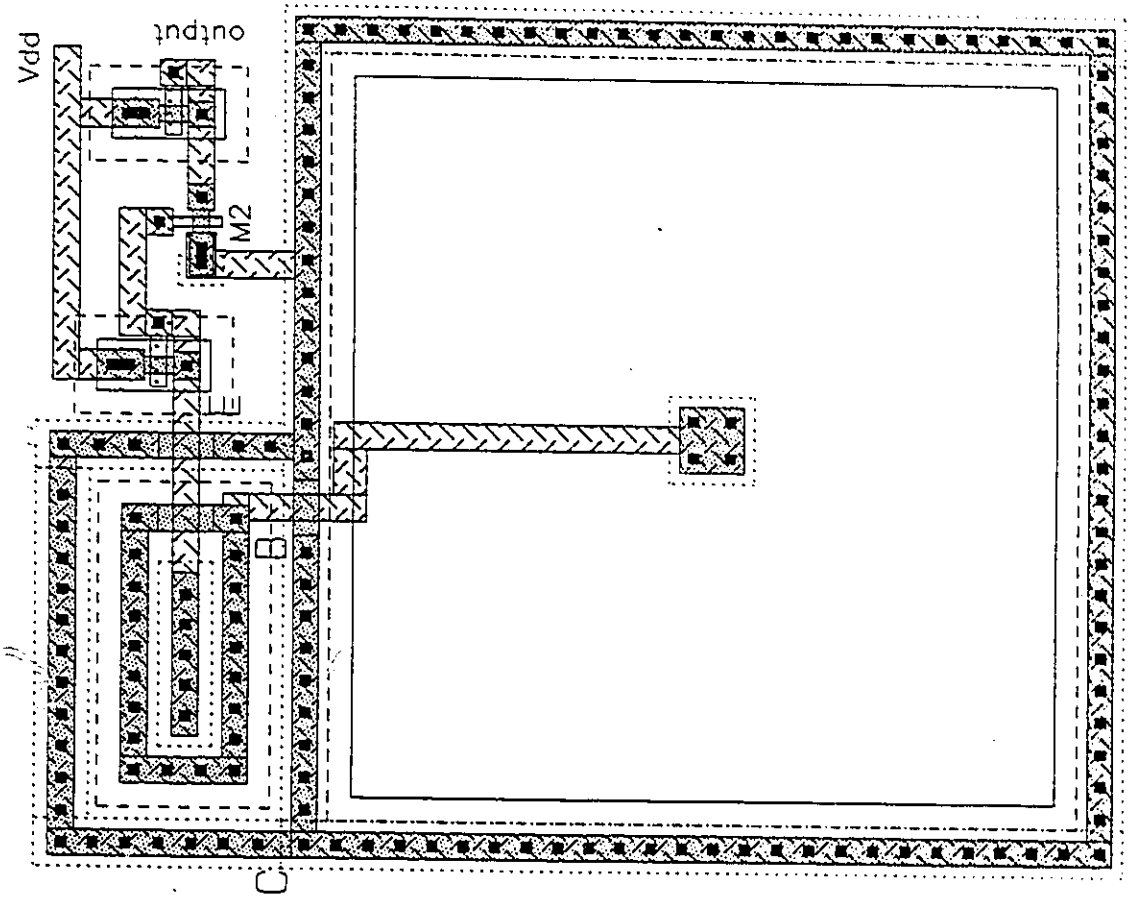
75*75 photo diode
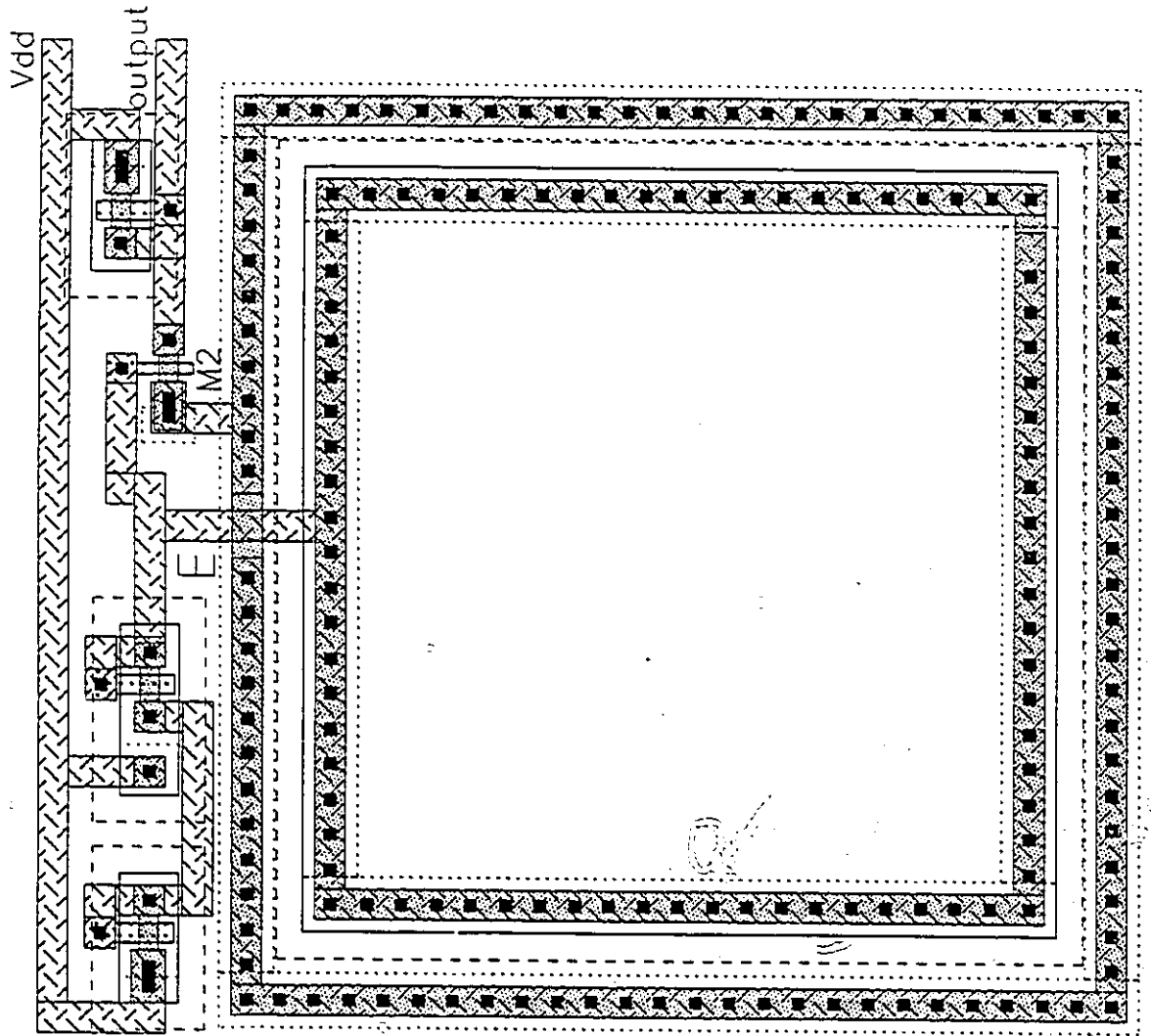
N

S

p+

PHOTO DARLINGTON WITH BUFFER

Vdd

output

M2

E

B

C

PHOTO PNP BJT WITH BUFFER
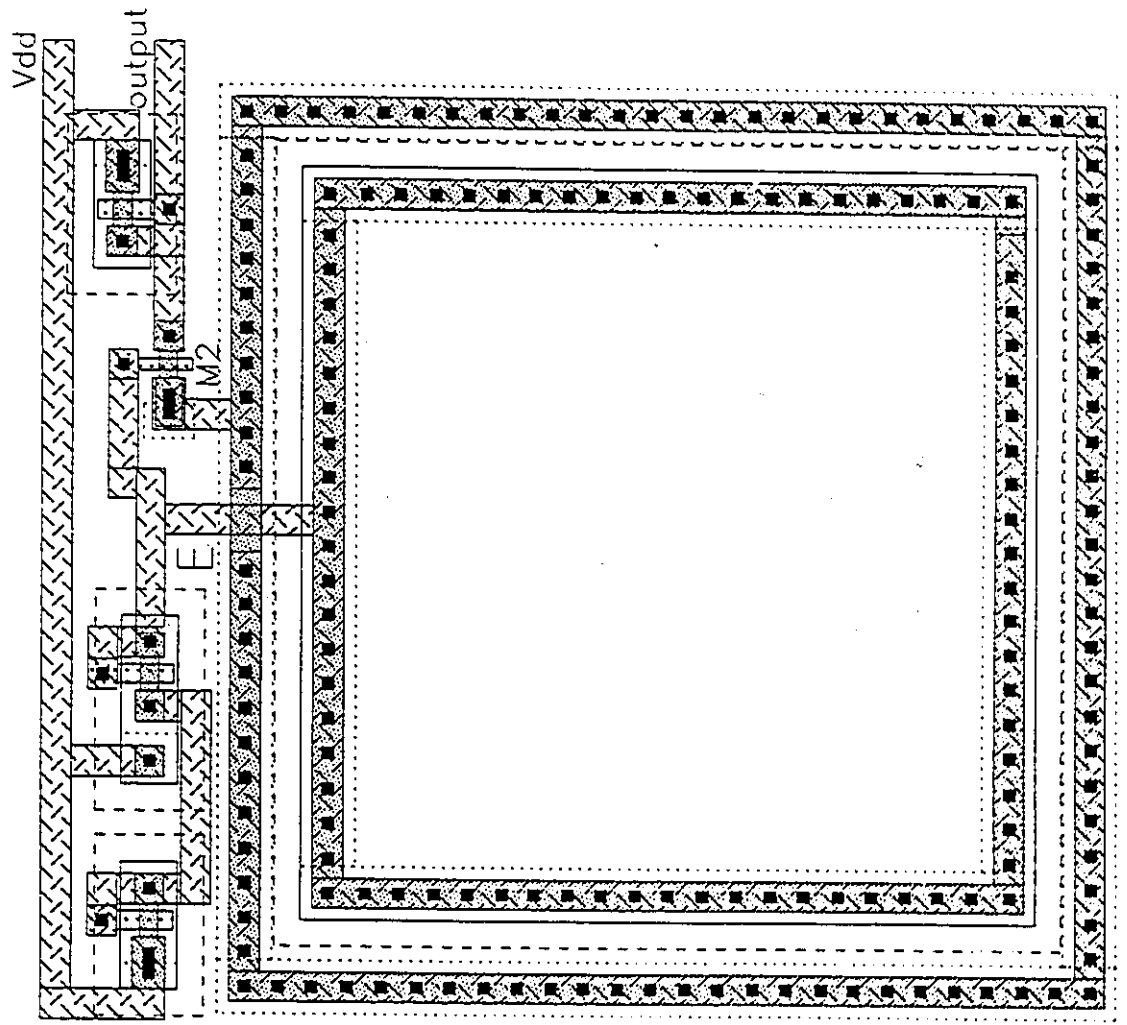
Vdd

Output

M2

E

PHOTO PNP EJT WITH TWO PMOS LOADS & AMPLIFIER

Vdd

Output

E

M2

APPENDIX III: The Measured Diode Photocurrent Data

reverse voltage (V)	reverse current(pA) dark	reverse current(µA) 0.02mw	reverse current(µA) 0.04mw	reverse current(µA) 0.06mw	reverse current(µ·) 0.08mw	reverse current(µA) 0.10mw
-1	-0.72	-5.83	-10.91	-19.15	-21.74	-23.64
-2	-0.93	-5.85	-10.99	-19.16	-21.75	-23.65
-3	-1.05	-5.88	-11.08	-19.20	-21.80	-23.66
-4	-1.21	-5.92	-11.18	-19.23	-21.80	-23.93
-5	-1.29	-5.93	-11.20	-19.24	-21.80	-24.04
-6	-1.41	-5.95	-11.22	-19.24	-21.81	-24.10
-7	-1.56	-5.97	-11.31	-19.25	-21.83	-24.13
-8	-1.78	-5.98	-11.37	-19.25	-21.84	-24.15
-9	-1.85	-5.98	-11.38	-19.25	-21.85	-24.17
-10	-1.96	-5.98	-11.40	-19.25	-21.86	-24.19
-11	-2.15	-5.98	-11.43	-19.25	-21.86	-24.22
-12	-2.25	-5.99	-11.48	-19.26	-21.86	-24.24
-13	-2.48	-5.99	-11.51	-19.26	-21.86	-24.26
-14	-2.65	-5.99	-11.53	-19.26	-21.87	-24.28
-15	-2.75	-5.99	-11.56	-19.26	-21.87	-24.30
-16	-2.98	-5.99	-11.60	-19.26	-21.87	-24.32
-17	-3.21	-5.99	-11.63	-19.26	-21.87	-24.35
-18	-3.64	-5.99	-11.64	-19.26	-21.87	-24.37
-19	-5/96	-5.99	-11.65	-19.26	-21.87	-24.38
-20	-9.22	-5.99	-11.66	-19.26	-21.87	-24.38

reverse voltage (V)	reverse current(µA) 0.12mw	reverse current(µA) 0.14mw	reverse current(µA) 0.16mw	reverse current(µA) 0.18mw	reverse current(µA) 0.20mw
-1	-24.47	-29.38	-34.24	-37.03	-42.57
-2	-24.55	-29.39	-34.26	-37.03	-42.70
-3	-24.64	-29.41	-34.32	-37.03	-42.83
-4	-24.69	-29.48	-34.38	-37.09	-42.97
-5	-24.74	-29.55	-34.43	-37.11	-43.04
-6	-24.78	-29.60	-34.49	-37.16	-43.13
-7	-24.80	-29.68	-34.52	-37.18	-43.19
-8	-24.83	-29.74	-34.57	-37.18	-43.23
-9	-24.84	-29.79	-34.57	-37.18	-43.28
-10	-24.87	-29.83	-34.59	-37.21	-43.33
-11	-24.88	-29.87	-34.61	-37.23	-43.38
-12	-24.91	-29.89	-34.61	-37.25	-43.43
-13	-24.93	-29.91	-34.63	-37.27	-43.47
-14	-24.94	-29.94	-34.65	-37.30	-43.51
-15	-24.96	-29.95	-34.67	-37.31	-43.53
-16	-24.98	-29.97	-34.67	-37.32	-43.55
-17	-25.00	-29.98	-34.71	-37.35	-43.57
-18	-25.02	-29.99	-34.77	-37.37	-43.61
-19	-25.04	-30.01	-34.82	-37.38	-43.64
-20	-25.06	-30.03	-34.82	-37.43	-43.67

APPENDIX IV: 3μm NPN BJT NETLIST

```
.options sda=2
vdd vdd! gnd! dc 5
ioptical 1 2
vce /vce gnd!

.dc vce 0 5v 0.2v ioptical 1u 10u 1u
.print i(r1) v(/vce)
*.plot i(r0) v(3)
*.tran 5ns 200ns

* net 1 = vdd!
* net 0 = gnd!
* net 2 = /vb
* net 3 = /vce
* net 4 = /q11.e
* net 5 = /q11.c
* resistor(0) = /r23
r/R23 gnd! /Q11.E 1k
* resistor(1) = /r20
r/R20 /Q11.C /vce 1k
.model model2 npn bf=250 br=15 eg=1.11 is=3e-15 isc=1.32e-15
+ise=5.2e-16 nc=2 ne=1.171136 vaf=70 var=18 ikf=0.1 ikr=2e-6
+rb=300 re=2 rc=50

* npn(2) = /q11
q/Q11 /Q11.C /vb /Q11.E model2

.end
```

APPENDIX V Neutral Density Filter (ND)

Neutral density filter sets make possible the fluctuation in a wide range of irradiance ratios with no significant dependence on wavelength. Beams can be attenuated to levels at which photometers or radiometers are most accurate and linear.

Initial beam irradiances can be calculated from accurately known filter densities. The definition of optical density is analogous to the definition of decibel as used in electronics. Optical density (D) is defined as the base 10 logarithm of the reciprocal of transmittance (T):

$$D=\log(1/T) \quad \text{or} \quad T=10^{-D}$$

where the reciprocal of the tranmittance, 1/T, is called the opacity.

Optical density is dimensionless, the notation 0.50D is used to mean 0.5 density units or simply a density of 0.50.

Neutral-density filters can be used in combinations of two or more at a time to achieve values of transmittance or density. In this case, densities of neutral-density filters are additive.

Nominal Density at 550nm (D)	Percent Transmittance (%T)
0.04	91.20
0.1	79.43
0.2	63.10
0.3	50.12
0.4	39.18
0.5	31.62
0.6	25.12
0.7	19.95
0.8	15.85
0.9	12.59
1.0	10.00
1.3	5.012
1.5	3.162
2.0	1.000
2.5	0.3162
3.0	0.1000
4.0	0.0100

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