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High Speed Test Interface Module Using MEMS Technology

By

Nabeeh Kandalaft

A Dissertation Submitted to the Faculty of Graduate Studies through the Department Electrical and Computer Engineering in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy at the University of Windsor

Windsor, Ontario, Canada 2012

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High Speed Test Interface Module Using MEMS Technology

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Declaration of Co-Authorship & Previous Publication

I. Co-Authorship Declaration

I hereby declare that this thesis incorporates material that is result of joint research with Dr. Rashid Rashidzadeh and Dr. Majid Ahmadi. I am aware of the University of Windsor Senate Policy on Authorship and I certify that I have acknowledged contribution of other researchers to my thesis, and have obtained written permission from each of the co-authors to include the above materials in my thesis.

I certify that this thesis, and the research to which it refers, is the product of my own work.

II. Declaration of Previous Publication

This thesis includes four original papers that have been previously published / submitted for publication in peer reviewed journals, as follows:

Thesis Chapter	Publication title/full citation	Publication status
Chapter 6	N. Kandalaft, R. Rashidzadeh, and M. Ahmadi, "High-Density Wafer Level Test Probe Card for 3D-ICs using MEMS Technology" Microelectronic Engineering, ID MEE-D-12-00353, under review, August, 2012.	Submitted
Chapter 3	N. Kandalaft, R. Rashidzadeh, and M. Ahmadi, "High Speed Test Interface Module Using MEMS Technology "IEEE Transactions on Very Large Scale Integration Systems (TVLSI), under-review, May, 2012.	Submitted
Chapter 6	N. Kandalaft, R. Rashidzadeh, and M. Ahmadi, "Testing 3D IC Through-Silicon-Vias (TSV's) by Direct Probing, "Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD). Under-review, Manuscript ID TCAD-2012, March, 2012.	Submitted
Chapter 3	N. Kandalaft, I. Basith, R. Rashidzadeh, "A MEMS Based Device Interface Board," IEEE International Test Conference ITC, Texas, USA, Oct. 2011.	Published

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Abstract

With the transient frequency of available CMOS technologies exceeding hundreds of gigahertz and the increasing complexity of Integrated Circuit (IC) designs, it is now apparent that the architecture of current testers needs to be greatly improved to keep up with the formidable challenges ahead. Test requirements for modern integrated circuits are becoming more stringent, complex and costly. These requirements include an increasing number of test channels, higher test-speeds and enhanced measurement accuracy and resolution.

In a conventional test configuration, the signal path from Automatic Test Equipment (ATE) to the Device-Under-Test (DUT) includes long traces of wires. At frequencies above a few gigahertz, testing integrated circuits becomes a challenging task. The effects on transmission lines become critical requiring impedance matching to minimize signal reflection. AC resistance due to the skin effect and electromagnetic coupling caused by radiation can also become important factors affecting the test results. In the design of a Device Interface Board (DIB), the greater the physical separation of the DUT and the ATE pin electronics, the greater the distortion and signal degradation.

In this work, a new Test Interface Module (TIM) based on MEMS technology is proposed to reduce the distance between the tester and device-under-test by orders of magnitude. The proposed solution increases the bandwidth of test channels and reduces the undesired effects of transmission lines on the test results. The MEMS test interface includes a fixed socket and a removable socket. The removable socket incorporates MEMS contact springs to provide temporary with the DUT pads and the fixed socket contains a bed of micro-pins to establish electrical connections with the ATE pin electronics.

The MEMS based contact springs have been modified to implement a high-density wafer level test probes for Through Silicon Vias (TSVs) in three dimensional integrated circuits (3D-IC).

Prototypes have been fabricated using Silicon On Insulator SOI wafer. Experimental results indicate that the proposed architectures can operate up to 50 GHz without much loss or distortion. The MEMS probes can also maintain a good elastic performance without any damage or deformation in the test phase.

Dedication

In the name of Allah, the Most Gracious and the Most Merciful

I might not know where the life's path will take me, but walking with You, God, through this journey has given me strength and patience. I am grateful to Allah. Indeed, without His help, nothing is accomplished.

I would like to dedicate this Doctoral dissertation to my late father. You constantly told me to "reach for the stars." I think I got my first one.

Mom, you gave me so much, thank you for teaching me that I should never surrender.

To my wife, without whom I would most certainly be lost, thank you.

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My deepest gratitude goes to my wonderful family for their encouragement, support and providing a loving environment throughout my life. Finally, and most important, I cannot find words to express my gratitude to my wife. Without her encouragement, sacrifice, and compassion I would not have finished the degree.

¹ www.cmc.ca.

² www. nserc-crsng.gc.ca.

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List of Abbreviations/Symbols

3D	Three Dimensional
3D-IC	Three Dimensional Integrated Circuits
AC	Alternating Current
ADS	Advanced Design System
ATE	Automatic Test Equipment
Au	Gold
Be-Cu	Beryllium Copper
BIST	Built-In Self-Test
BOE	Buffered Oxide Etchant
BOSCH	Time-Multiplexed Etching Named After Robert Bosch
С	Capacitance
C4F8	Perfluorocyclobutane
CAD	Computer Aided Design
CIRFE	Center for Integrated RF Engineering
Cm	Mutual Capacitance
CMOS	Complementary Metal-Oxide-Semiconductor
Cr	Chromium
Cu	Copper
DC	Direct Current
DDJ	Data Dependent Jitter
DI	Deionized Water
DIB	Device Interface Board
DRIE	Deep Reactive Ion Etching
DUT	Device Under Test
E	Young's Modulus of Elasticity
EMI	Electromagnetic Interference
FEA	Finite Element Analysis
FEM	Finite Element Method

FFT	Eight Effect There is the a
FEI	Field Effect Transistor
FPGA	Field-Programmable Gate Array
G	Conductance
GaAs	Gallium Arsenide
GHz	Giga Hertz
HF	Fluoric Acid
HFSS	High Frequency Structural Simulator
HMDS	Hexamethyldisiloxane
I/O	Input/output
IC	Integrated Circuit
ITRS	International Technology Roadmap For Semiconductors
KGD	Known Good Dies
L	Inductance
LCD	Liquid Crystal Display
Lm	Mutual Inductance
MEMS	Micro-Electromechanical Systems
MPa	Mega Pascal
NH4F	Ammonium Fluoride
PCB	Printed Circuit Board
PC-Switch	Photoconductive Switch
PE	Pin Electronics
PMU	Parametric Measurement Unit
R	Resistance
RAC	AC Resistance
RF	Radio Frequency
RIE	Reactive Ion Etching
RIO MGT	RocketIOTM Multi-Gigabit Transceivers
RX	Receive
S11	Return Loss
S21	Insertion Loss
SEM	Scanning Electron Microscope
SF6	Sulfur-Hexafluoride
SiO2	Silicon Oxide
S-N Curve	the magnitude of a cyclic stress (S) against the logarithmic scale of cycles
	to failure (N)
SOI	Silicon-On-Insulator
TEM	Thermo-Electro-Mechanical
TG	Timing Generators
TIM	Test Interface Module
Tpd	Time Delay
-	-

TSV	Through Silicon Vias
TX	Transmission
USB	Universal Serial Bus
UTS	Ultimate Tensile Strength
UUT	Unit Under Test
VIH	Input High Voltage
VIL	Input Low Voltage
VLSI	Very-Large-Scale Integration
VNA	Vector Network Analyzer
δ	Delta, Skin Depth
03	Permittivity Of Free Space
Er	Relative Permittivity of Dielectric Material
λ	Wavelength
σχ	Ultimate Strength
σy	Yield Point
Cair	Micro Air Voids Capacitors
Cmc	Micro-Contact Capacitors

Chapter 1

Introduction

As the semiconductor industry continues to evolve, complexity of microchip designs increases requiring strict manufacturing tests to verify their performance parameters. With the transient frequency of available CMOS technologies exceeding hundreds of gigahertz, it is now apparent that the architecture of current testers needs to be greatly improved to keep up with the formidable challenges ahead [1, 2]. The test requirements for modern integrated circuits (ICs) are becoming more stringent, complex and costly. These requirements include an increasing number of test channels, higher test-speeds and enhanced measurement accuracy and resolution [3, 4]. Semiconductor manufacturers are striving to find cost effective solutions to the problem of testing for new generation of ICs.

1.1 Testing Process

Generally, ICs have to pass through a refined process of design verification, development, and testing. The last of these can be considered the most important step of

creating profitable ICs. Testing is a process to detect fault free devices from defective ones to ensure proper operation of the devices released to the market.

A valuable indicator to evaluate the significance of test and fault detection at early stages in the VLSI industry is the rule of ten. The rule states that the cost of detecting a faulty IC increases by an order of magnitude in the production life cycle. If test is carefully planned at the beginning stages of the fabrication process, then faults could be identified, located and defective components can be removed from manufacturing process at a very low cost. Once the defective dies are soldered on a printed circuit board (PCB), the cost of detecting defective chips is multiplied by a factor of ten. Similarly, detecting faults at the system level cost as much as ten times more than the cost at the board level. IC manufacturing requires a significant amount of resources and time as shown in Fig.1.1. Before generating masks for the fabrication process, all semiconductor devices go through extensive design verification using simulation software tools to ensure that the process design rules are followed; and also to make sure that these devices meet the design specifications.

During fabrication, after deposition and etching of the first metal layer, in-line wafer test is performed to confirm the electrical properties associated with each completed fabrication step. Electrical parameters such as gate threshold, poly-silicon field threshold, and poly sheet resistance are tested and verified during this stage. In-line wafer tests use special test pattern structures located on the wafer or using scribe lines [5] which are usually patterned between dies. Nevertheless, in-line wafer tests might generate particles that can create additional defects.

Testing individual dies at the wafer level is known as wafer sort. The devices are subjected to standardized DC/AC parametric and functional tests. These test procedures are performed to verify die operation functionality; sort good dies, and provide yield information to enhance the overall fabrication process. Wafer sort is carried out by a wafer probing system where the electrical connectivity is established by small probes positioned on designated contact pads. The testing process is controlled by automatic test equipment to mark failed dies by an ink dot method. DC and AC parametric and functional tests are performed to identify Pass/Fail dies prior to packaging.



Fig. 1.1: Test Flow Chart Process.

1.1.1 Functional Tests

Functional tests verify that the devices under test perform its intended functions according to the design specifications. To validate this, test system supplies input data vectors to the DUT and verify the corresponding responses to guarantee proper operation. The expected output is stored in a vector memory and then compared to the expected and pre-calculated DUT outputs.

1.1.2 Parametric Tests

DC parametric's is the first test performed by Automatic Test Equipment (ATE) prior to any other manufacturing tests. During this stage, chips are tested for open, short, leakage, closed-loop gain, open loop gain, input high voltage (VIH), and input low voltage (VIL), faults [6, 7]. DC tests are performed on I/O signals to verify that they meet the current and voltage swing specifications. On the other hand, AC parametric tests are executed to identify transition faults of the DUT. They verify the frequency and timing parameters, such as rise/fall time, set and hold time, bandwidth, phase, distortion, noise, and propagation delay [8]. To perform these parametric tests, advanced measurement unit are required [8].

After identifying defective dies, fault free dies or Known Good Dies (KGD) are scribed, wired, and then packaged. Packaging of an IC is not the last phase of manufacturing. The packaged chips are tested again with the same or very similar test patterns to ensure that the device has been packaged properly and will continue to perform according to the nominal specifications.

Burn-in testing is also performed at this stage to detect and to eliminate early failures in semiconductor devices. It presumes that failure mechanisms can be accelerated by stressing the operating points where a burn-in cycle is equivalent to several years of normal operating conditions. Elimination of these devices improves the product quality and reliability significantly. For electronic components, burn-in tests are frequently conducted at elevated temperature, elevated voltage, and power cycling [10]. The time period required to conduct these tests varies from 10 to 1000 hours depending on the

failure mechanisms and the complexity of ICs. Burn-in tests are expensive and destructive [10].

There are two types of failure associated with burn-in tests:

- 1. Infant mortality failure tests
- 2. Freak failure test.

1.1.3 Infant Mortality Failures Tests

These failures are caused by sensitive designs and process variations. These defects can be detected by a short period of burn-in test (10-30 h) in a normal or slightly accelerated working environment. Normally, failures associated with infant mortality are caused by defects such as gate-oxide shorts, partial opens, resistive bridging, etc. These types of defects may not cause a functional error at the time of testing; yet, they can degrade the device lifetime and reliability [10, 11].

1.1.4 Freak Failures Tests

These tests are expensive and require long burn-in time of 100 to 1000 hours in an accelerated test environment [11]. Freak failure tests have the capability to stress more internal circuits, causing additional failure mechanisms verification.

In conclusion, testing is essential to deliver high-quality ICs and to ensure maximum operational reliability and safety. Testing is a complex, expensive process and must be planned at early stage of the design process.

1.2 Automatic Test Equipment

The complexity of testing ICs varies widely, ranging from simple manual test units to complex high speed Automatic Test Equipment (ATE) as shown in Fig. 1.2. It is a computer-operated instrument used to conduct IC verification tests.

The main building blocks of a typical ATE are:

- (1) Main Frame
- (2) Test Head
- (3) Computer Workstation



Fig. 1.2: FLEX automatic test equipment system from Teradyane [12].

1.2.1 The Main Frame

A main frame contains measurement units, interfaces connecting the workstation with the test head unit, power supplies, and control circuitry. It may also consist of a manipulator to position the test head precisely and a chiller unit to provide cooled liquid to control the temperature of the sensitive measurement electronics. The computerized workstation serves as an interface to control test programs and monitor the test results using different software tools provided by the ATE vendors.

1.2.2 Test Head

Test head is a physical structure where the wafer under test or the unit under test (UUT) is positioned to perform DC/AC parametric and functional tests during the test stage. The DUT is connected to the test head through an interface board known as the Device Interface Board (DIB) or a load board.

The test head consists of the most sensitive measurement units including programmable driver and receiver channels. It is a standalone movable part connected to the main frame through cables. In general, test heads are placed as close as possible to the devices under test in order to maximize the bandwidth and minimize the parasitic effects of transmissions lines.

The electronic circuitry of the test head boards consist [12] of

- ➢ Memories
- Timing Generators (TG)
- Test-pattern Generators
- Parametric Measurement Unit (PMU)
- Pin Electronics (PE)
- Functional Units
- Test Processor

The block diagram of a simple test head board in an ATE is shown in Fig. 1.3. The memories store the test vectors and the measured data collected from the DUT. The pin electronics circuitry adds the timing and format information to drive the DUT pin while

the programmable parametric measurement unit acquires the DC output signals from the DUT. A comparison takes place between the expected data and the actual DUT signals.

Many testers are equipped to handle two test heads that can share the main frame recourses. In this configuration, a device is tested on one test head while a handler sorts and loads devices for the second test head. Multisite capability is another feature which allows ATEs to simultaneously test multiple devices on the same test head to reduce the costs.



Fig. 1.3: Simple Test Head Architecture [6].

1.2.3 Computer Workstation

It is an interface to control the testing environment and measurement instruments. Test programs are controlled by software tools through the workstation. It simplifies the process of retrieving measurement data from measurement instruments.

Additional units are connected to ATEs to facilitate the testing process

- a) Test Handlers
- b) Wafer Probers

a) Test handlers

ATE systems, in general, interface with automated units for mass production known as test handlers to place the DUT on a test interface board. These handlers sorts good dies from defective ones based on the test outcome. Another important feature for test handlers is to provide a controlled thermal environment for units under test. This will improve the testing results as electrical parameters maybe shifted with temperature variation. There are two types of test handlers, gravity or electromechanical.

b) Wafer Prober

ATEs include a prober unit that moves across the silicon wafer and provides a physical access to test the dies at the wafer level. The wafer prober is mainly responsible for loading and unloading the wafers. It is equipped with automatic pattern recognition optics for aligning the wafer with high accuracy to ensure proper positioning between the probe tips and the contact pads on the wafer. Electrical probes are attached to a probe card and connected to ATE resources by a probe interface card to provide temporally electrical connections between the DUT and the ATE during the test stage.

1.3 Device Interface Board (DIB)

Current states of the art ATEs, in general, require a Device Interface Board (DIB) to perform test on ICs [4]. The DIB is a custom design interface board that provides temporary electrical connections between the DUT and measurement instruments resources within the tester; it is designed for a specific device or group of devices. Components on a typical test board assembly are resistors, inductors, capacitors and relays besides sockets which are required for proper DUT positioning. Bypass capacitors are usually used for noise reduction purposes. The DIB is responsible for routing signals to/from the DUT. A typical test board assembly and DIB are shown in Fig. 1.4.

The DIB also provides space for DUT-specific local circuits such as such as:

- Load Circuits
- Mixers
- Buffer Amplifiers
- ► FPGA.

The design of DIB for testing high-speed ICs is a major challenge [13]. High-speed test signals experience a broad range of nonlinearities associated with the signal paths due to relatively long traces of transmission lines between DUT and the tester [14-16]. The signal path from tester to the device under test is shown in Fig. 1.5. At the pin electronics side, the signal leaves the driver output with a certain rise time and overshoots properties. It faces impedance discontinuities and transmission line losses [4] before reaching the DUT I/O pins.

1.3.1 Impedance Discontinuities

In general, impedance discontinuity occurs at the following location

- Driver's output at the pin electronics side
- > DIB input
- > DUT input

Discontinuities cause reflections and alter the rising time of signals. Signal reflection reduces the data eye opening and the speed of communication [17]. The impact of reflections on the data eye opening is a function of electrical distance between the driver and the device under test. The problem of signal reflection can be minimized by matching impedances. The attenuation of signals due to matching impedances is taken into consideration in the calibration phase.



Fig. 1.4: a) Typical Test Board Assembly, b) Teradyne Device Interface Board (DIB) [12].



Fig. 1.5: A typical signal path from tester to the device under test.

1.3.2 Transmission line loss

The integrity of test signals is affected by various factors including:

- AC resistance due to skin effect
- Cross talk
- Electromagnetic coupling caused by radiation
- Dielectric loss
- Absorptive Loss
- Noise

1.3.2.1 Skin Effect

Skin effect is the tendency of current to flow at the outer edge or surface of a conductor at high frequency, instead of flowing uniformly over the full cross section. Electric current flows generally at the "skin" of the conductor, between the outer surface and a level known as the skin depth δ . The skin depth is defined as the depth below the surface of the conductor at which the current density decreases to 1/e (0.37) of the outer surface current. Skin effect increases the effective resistance. This effect becomes more obvious as the frequency increases.

1.3.2.2 Cross Talk

Cross talk is mostly due to electrical coupling of transmission line traces in close vicinity. Cross talk induces undesired effects from one line to another caused by capacitive or inductive coupling. Therefore, the amplitude, edge rate and jitter are affected. To minimize cross talk, transmission line traces have to be properly routed to minimize the coupling effects between neighboring wires.

1.3.2.3 Electromagnetic Coupling Caused By Radiation

Electromagnetic interference (EMI) is an interference that affects the electrical circuit performance due to electromagnetic induction or radiation of external sources. The Electromagnetic interference may disturb, obstruct, and degrade the behaviour of the device interface board. These effects vary from a simple degradation of the data to a total

loss of data [18]. The source of EMI is an artificial object, or natural, that radiates fast fluctuating electrical currents, such as electrical circuits, lights or radiating antennas.

1.3.2.4 Absorptive Loss

Absorptive loss is the amount of electromagnetic radiation absorbed by dielectric material. It is defined by loss tangent which determined by the angle in a complex plane between resistive and reactive components of the dielectric material.

1.3.2.5 Dielectric Loss

The absorption of electrical energy by a dielectric material that is exposed to alternating electric field where it is converted to heat is known as dielectric loss. Dielectric loss depends on the electric field frequency and the dielectric material which is also a function of frequency. At higher operating frequencies, the dielectric constant of material changes significantly.

1.4 Outline of the Thesis

The rest of this dissertation is organized as follows. Chapter 2 presents a review of literature. The recent studies in the area of test methodologies and the latest test architectures employed by semiconductor industry are also covered in this chapter. Chapter 3 begins with the description of the proposed solution and the architecture of the MEMS based Test Interface Module (TIM). The building blocks of the proposed module with the mathematical details have also been covered in this chapter. Chapter 4 presents the analysis, and simulation results. Chapter 5 discusses the fabrication process of the test interface module using a customized fabrication process. In chapter 6, experimental results of the fabricated prototype is presented and compared with the simulation results, and finally in chapter 7, conclusions are drawn and recommendations are made for future work.

Chapter 2

Review of Literature

2.1 Background

To reduce the effect of transmission lines between tester resources and the DUT, various techniques have been introduced in the literature. In [19-20], clamping diodes are added to the tester comparators to clamp the output signals ringing caused by reflections at the I/O pins. The efficiency of this method is reduced when the transition time of the output signals are less than the round trip delay. Therefore, although the magnitude of signal reflections can be reduced, the length of transmission line imposes a limitation on the maximum frequency of operation.

Another technique [20] uses series termination resistors at the outputs of the device under test to eliminate signal reflection. However, these resistors affect DC parametric measurements and output transition times. Compensation within the test program is required to isolate the effect of these resistors. This adds another level of complexity to the wafer level tests. Transmission line termination with 50 Ω resistors at the comparator side can eliminate reflections. This method, in general, is not feasible as the outputs of CMOS devices are not designed to drive 50 Ω loads.
2.2 Remote Driver to Reduce the Transmission Line Effects

Mydill [20] proposed a general purpose, high performance VLSI test system in which not only comparators, but also all critical pin electronics circuitry are within a short distance of the DUT as shown in Fig. 2.1. The basic approach is to reduce the distance between the device under test and the tester pin electronics board by placing required circuits close to the DUT. In this technique, most of the test head circuitry have been removed and located remotely in an attached mainframe chassis.

The circuits left in the test head include:

- Comparators
- Programmable Loads
- Drivers disconnect Switches

These circuits have been integrated on a low power monolithic chip to facilitate packaging and cooling requirements. The actual data drivers are located in the mainframe and connected to the pin-electronics through coaxial cables of 8-feet long. The designed PE board in this method reduces the total distance between the DUT outputs and the ATE drivers to approximately 2 to 3 inches for a typical packaged VLSI device.

To perform DC parametric test, the driver circuits are disconnected from the main frame, and the DC Parametric Measurement Unit (PMU) is connected to the DUT through a GaAs MMIC (Monolithic Microwave Integrated Circuit) driver switch.



Fig. 2.1: Remote driver and local driver circuits (Receiver, Driver Control, and Comparators) [24].

This method, for signals in the frequency range of 100 MHz generated by typical ATE drivers, performs well as the losses in the coax cable are insignificant in this frequency range.

Although the distance is reduced considerably in this method, the loss due to skin effect and dielectric material in the 8-foot cable becomes significant for high speed signals. Moreover, parasitic capacitances of typical field effect transistor FET switches can cause signal degradation. Furthermore, leakage current between gate and drain as well as between gate and source of transistors reduce the accuracy of DC current measurements. In [22], a special photoconductive switch (PC-switch) is proposed to replace FET switches in both the driver and the comparator paths to allow high speed I/O testing.

This configuration solves the signal path round trip delay problem for speeds up to about 100MHz. This technique is effective when the number of I/O pins is limited, but it cannot be readily used for high pin count devices where the complexity and cost of test fixture becomes substantially high.

2.3 Interleaving Method Using Single Matched Impedance Transmission Line

Dual-transmission line configuration for testing bidirectional pins has been proposed in [23]. This model uses a single transmission line for each driver and receiver terminated by 50 Ω loads to match the transmission line characteristic impedance. Transmission lines are configured by separate channels within the pin electronic board. A series resistor is included to minimize the load at the DUT output. In this configuration, both ends are terminated to minimize signal reflection. The advantages are enhanced signal integrity and eliminated dead time in the switching period. However, the main drawbacks of this method are the costs of channel resources used to compensate the effect of the resistive voltage divider at the comparator side.

In order to reduce the resources required for bidirectional transmission lines configuration, Keezer and Zhou proposed a method comparable to the dual line technique [24]. This method is implemented using only a single transmission line between the device under test and the ATE resources. To match the DUT output to 50 Ω transmission lines, a resistive divider is employed at the driver side as shown in Fig. 2.2. In this

method, similar to the dual line method, the driver provides the termination through a 50 Ω source resistor to match the transmission line impedance, therefore, signals arriving at the comparator side appear with full-amplitude at the I/O of the DUT without any reflection.

As the data arrives at the comparator side, a conflict arises if the driver is not quiet, causing signal degradation. Therefore, the driver must switch between logic zero and data bits. In this configuration drivers actively drive transmission lines to provide necessary termination through the 50 Ω source resistors.

It has to be noted that the transmission line delay T_{pd} must be correlated to the data bit rate. This is to ensure that the output data arrives at the comparator side when the driver is quiet. The data bits at the comparator side are attenuated because of the voltage resistive divider. Yet, no data conflict is occurred as shown in Fig. 2.3. To perform tests serial sequences of data have to be forwarded, followed by a serial output sequences. This requirement can be fulfilled by a single matched-transmission line as shown in Fig. 2.4.

The drawback of this method is the fact that it can operate only at fixed discrete frequencies determined by the transmission line delay, Tpd. The line delay must be designed to be a multiple of the operating frequency. In addition, for devices working on fixed clock rates, this method cannot be applied if the clock rate is not matched to the transmission line delay. Moreover, signal integrity issues at high frequency due to the transmission line length (2-3 feet) become critical and affect the test results.



Fig. 2.2: Interleaving method using single matched impedance transmission line [24].



Fig. 2.3: Timing for the interleaved method when the DUT alternates between input and output on switching cycles [24].



Fig. 2.4: Timing for the interleaved method when the DUT first receives input bits, then outputs serial bit stream [24].

2.4 Technology-Specific Transceiver Approach

Keezer and Zhou suggested an idea similar to these approaches presented in [21, 22] to locate the tri-state drivers and the high input impedance comparators as close as possible to the DUT I/O pins. Instead of using discrete switching elements, they proposed a solution to replace general purpose pin-electronics with technology-specific transceivers [24]. In this method, the transceivers are fabricated using the same technology as the DUT to precisely match the DUT I/O pin characteristics and thus eliminate the effects of signal reflection.

The buffer ICs are located next to the device under test or below the PCB text fixture as shown in Fig. 2.5. These ICs function as a local interface circuit reducing the distance between the DUT and the PE board. The data is directed through unidirectional lines to these buffer ICs using tri-state commands. The round trip delay is minimized and with such short distances, the transmission line effect is eliminated and matching resistors are not required. This method minimizes the round trip delay and by restricting the PE architecture to only a single technology, the power and the area overhead are also reduced. The main drawbacks are the limited range of voltage level adjustments. In addition, if mixed levels are required by the device under test, additional buffer ICs have to be added. In summary, this technique minimizes the transmission line effects but at the cost of restricting the flexibility of the general purpose pin electronics.



Fig. 2.5: General purpose pin-electronics with technology-specific transceivers [24].

2.5 Multi-Gigahertz Test Module

Majid and Keezer developed generic test modules that are connected to automatic test equipment through a device interface board (DIB) [25]. The DIB is designed to accommodate test enhancement modules and acts as a passive interface between the device under test and the ATE as shown in Fig 11. The test modules are designed using standalone mini-testers [26], [27]. They intercept signals generated by the ATE and then route them to the DUT. These test modules generate high-speed signals by precision multiplexing method using high-performance XOR gates. Each test module consists of two blocks, a core logic unit and an application specific logic block. The block diagram of the test module and how it connects to the DIB is shown in Fig. 2.6.

2.5.1 Core logic block

The core logic consists of FPGAs that control the testing environment; it also includes dedicated microcontrollers that are connected to a personal computer through a Universal Serial Bus (USB). Each Xilinx FPGA block consists of 4 RocketIOTM multi-gigabit transceivers (RIO MGT) [28] with 8 high speed TX and two RX channels as shown in Fig 2.7. A low-jitter timing reference is supported by an external RF clock source. The core logic also includes a flash memory to store the FPGA programming information.



Fig. 2.6: Multiple test modules connected to the top side of the DIB.



Fig. 2.7: Block diagram of test module design with DIB and ATE [25].

2.5.2 Application Specific Logic

Each of the transmitter TX channels passes through a 2:1 multiplexer to select the core signal or the application specific signal to pass it to an RF relay. The amplitude of these signals is then adjusted by SiGe buffer. The FPGA controls the test execution when the relay switches select the signal from the multiplexer; in this case the ATE is idle. DC parametric tests generated by ATE are selected by the RF relays switching through the device interface board; in this case, the signals from the core logic are bypassed. This mode allows the ATE to control test execution directly. In this case, standard ATE tests such as functional tests or DC-parametric tests can be performed.

In this approach signals are generated by ultra-precision buffers to improve their edge rates and then multiplexed to double their data rates using XOR gates. This method generates signals at 6.25 Gbps with 22ps jitter, and 10 Gbps at 32 ps jitter. Although theoretical results demonstrate a significant ATE performance enhancement, some timing errors are often generated in practice. XOR multiplexing gates are known for adding data dependent jitter (DDJ) that requires precise calibration at each frequency to compensate

the offset delays applied to the input signals. Moreover, the ATE DC-parametric test instruments and functional test channels must be connected via RF switches; which add some complexity to the test environment restricting the flexibility of the general purpose PE architecture.

To meet the test requirements for high-speed system-on-chip devices, leading ATE manufacturers offer additional extension instrumentation to generate high-speed signals. Verigy, for example, extends the performance of its scalable V93000 series with a Pin Scale HX extension card generating signals up to 12.8 Gbps [29]. The Pin Scale HX channel card combines the functionality of at-speed ATE channels with high-integrity loopback. A similar card is proposed by Credence that supports signal up to 6.4 Gbps with a jitter less than 30 ps peak-to-peak [30]. These cards are relatively expensive and they require a major capital investment.

2.6 ATE Interconnect Challenges

With the transient frequency of available CMOS technologies continuing to grow and increasingly complex IC designs, the design of automated test equipment faces formidable challenges. The test fixture and interconnects between the ATE pin electronics and the device under test remain as the main bottleneck affecting signal integrity at higher data rates [31].

ATE systems are required to have fast loading and unloading operations. They are also expected to connect to standard equipment such as probers, handlers, failure analysis equipment, etc. However, these requirements create mechanical and electrical constraints that can aggravate the signal integrity in large ATE system. For example, a large I/O pins count requires test fixtures with a large number of long traces of wires and coaxial cables which increases transmission line losses and undermines signal integrity and consequently affect the measurement accuracy at the DUT side.

2.6.1 Coax and Pogo Pins

ATE interconnects can be classified into two main categories: coaxial and pogo pins. Blind mate coaxial connector [32] presents less than 0.1 dB insertion loss at 18 GHz. This type of interconnect, which is shown in Fig 2.8, is commercially available. The downside of this technique is the limited pin count of the large area of the connectors, and the additional cost associated with this connector assembly.

Pogo pin assemblies can also be designed for very high bandwidth connection. Although pogo pins are not comparable with coax cable assemblies due to their physical structure, they do provide significant advantages over the coax cable assemblies such as density, cost and compatibility [33]. The mating structure on the PCB test fixture for these pogo pins is established by pogo via shown in Fig. 2.9 [31].



Fig. 2.8: ATE coaxial cable blind mate connector interface to the ATE pin Electronic [33].



Fig. 2.9: Automatic test equipment pogo pin assembly.

Through additional enhancements and various compensation techniques, it is possible to use a pogo pin assembly interface for high clock data rates without a significant modification in the current ATE architecture. This can work for low count I/O pins where the traces are in the range of 4 cm long. However, for current ATE solutions with high I/O pin count devices require large size test fixtures. This will imply longer signal traces, which in turn generates higher signal losses.

2.6.2 Test Fixture Design

ATE test fixture affect high-speed signal [31] due to the inherent loss of transmission lines and via interconnects [34]. For a limited number of I/O, the test fixture loss can be minimized by reducing the physical length of interconnects. However for high I/O pin count devices the test fixtures are large and require long traces of wires.

The performance of ATE text fixture can be improved by using low-loss dielectric materials such as ROGERS 4350 [35], however, it will always have a greater dielectric loss than standard coaxial cables made with PTFE (Polytetrafluoroethylene) materials. Moreover, the resistive skin effect becomes a significant factor for long traces of wires at high frequency. Since coaxial cables have a lower loss than traditional PCB traces, one approach is to exchange PCB signal traces with coaxial cables on the text fixture as shown in Fig. 2.10.



Fig. 2.10: Coaxial connectors and cables to solve the PCB loss challenge [33].

However, it is difficult to integrate the test fixture to a typical ATE handler. In addition, with discontinuities existing due to additional connector and vias, signal transitions must be carefully calibrated to guarantee proper operation.

2.5.3 Optical Interconnect

Optical interconnects have the potential to solve the signaling challenges of electrical wiring [36]. Optical waves have low losses; optical beams can touch, cross, and propagate close to each other without generating noise, signal coupling and jitter. Nevertheless, significant challenges must be solved before they replace the electrical wiring interconnects. One of the major limitations of optical interconnects is the operating voltage of the modulators. Both reflectivity and contrast ratio are deteriorated as operating voltages are lowered [37]. Moreover, complexity and the difficulty of producing high yield optoelectronic components add significant cost issues.

2.7 Summary

New generation of ICs poses numerous electromechanical challenges to the design and implementation of current ATE's. This chapter presented the complex challenges of testing CMOS ICs at high clock speeds. Various test methods and techniques have been proposed to address these challenges.

Test methodologies and the ATE architecture have to be significantly improved to support the test requirements of new generation of integrated circuits and systems.

Test fixture and interconnects between ATE pin electronics and the device under test are the main contributors to the signal integrity degradation at higher clock rates. The common approaches to address this problem are a) to reduce the transmission line length between the tester resources and the device under test, and b) to minimize signal reflections.

Technology-specific transceivers and test enhancement modules have also been presented in the literature. However, in these methods, higher test speeds are achieved at the cost of limiting the flexibility of general purpose PE architecture and ATE systems.

Chapter 3

Design and Methodology

3.1 Proposed Solution

The undesired effect of long traces of wires on signal integrity is significantly attenuated with the reduction of lengths of wires. Therefore, an effective solution is to reduce the physical separation between tester resources and the units under test.

MEMS technology can be used to reduce the length of the signal paths significantly. The characteristic impedance of transmission lines is a function of length; as a result, the undesired effects can be minimized with the length reduction.

A Test Interface Module (TIM) based on Micro-Electromechanical Systems (MEMS) offers a potential solution to minimize the physical separation between the device under test (DUT) and the ATE resources due to its micro-scale dimensions. As a result, the capacitive and inductive effects of the transmission line and AC resistance due to skin effect are significantly attenuated allowing the test channels to operate at higher clock speeds without considerable signal integrity degradation.

3.2 MEMS Test Interface Module Architecture

The architecture of the proposed MEMS test interface module, which is designed using IntelliSuite CAD tools, is shown in Fig. 3.1. The TIM consists of two interface sockets and a contact spring to provide temporary signal paths between the ATE resources and the DUT [38]. It includes:

- Fixed socket
- Removable socket
- Contact spring

The fixed socket acts as an interface between the removable socket and the ATE test channels. The removable socket provides the necessary means to support temporary connectivity between the device under test and the tester. It also provides a physical location for the device under test and includes contact springs for temporary connections. The removable socket can be customized based on the size of DUT and the number of I/O pins. In the test phase, a pressure mass is positioned on top of the die under test to keep it tightly pressed against the removable socket connecting the die to the tester.



3.2.1 Fixed Socket

The layout of the fixed socket is shown in Fig. 3.2. It includes solder pads on the bottom side to connect to ATE pin electronics. The electrical connections between the removable socket and the tester resources are established through a bed of micro pins located on the top side of the fixed socket. These micro pins are in fact the substitutes for the conventional pogo pins [39] commonly used in automatic test equipment.



(a)



Fig. 3.2: Layout of the implemented fixed socket, a) top side, b) bottom side.

3.2.2 Removable Socket

The removable socket incorporates cantilever type contact springs to provide temporary electrical connections between the DUT I/O pins and the ATE resources as indicated in Fig. 3.3. The die under test is positioned on top of the removable socket. Four circular alignment keys are integrated in the fixed and removable sockets to ensure proper positioning of the structure during the test stage as shown in Fig. 18b.







Fig. 3.3: Layout of the implemented removable socket, a) Top side, b) Bottom side.

3.2.3 Contact Spring

The cantilevered bridge-type contact spring in Fig. 3.4 provides temporary electrical connectivity between the DUT pads and the ATE resources. It has a square geometry of 100x100 μ m with a contact pad dimensions of 50x50 μ m and 10 μ m height. The contact surface is 10 μ m above the substrate plane to allow deflection in the test stage.



Fig. 3.4: Layout of the MEMS contact spring.

It is supported by eight beams of equal length to maintain symmetrical pressure around the contact pad. The connectivity between the top and bottom sides is established by two square beams within the removable sockets which are 500 μ m apart. Fig. 3.5 shows a three dimensional figure of the proposed module.

The contact spring is designed to satisfy the following objectives:

- Smooth and flat contact surface to maximize the contact area in order to achieve a lower contact resistance
- Reliable elastic performance to ensure reversible deformation of the structure
- Low contact force to reduce structural deformation
- Small area to support small-size contact pads



Fig.3.5: Signal path of a test channel on the removable socket.

In the test phase, the top contact pad retains negligible shear and maintains a reasonable flat top surface to provide greater contact area and to reduce the contact resistance [40, 41]. Fig. 3.6 shows the cross section of a contact spring and a DUT I/O pad in the steady state and after an induced pressure. The contact spring experiences a temporary elastic deformation due to the applied pressure mass load which keeps the contact pad tightly pressed to establish the electrical connection between the die I/O pads and the pin electronics resources. To avoid material stress deformation, the contact probe is designed to operate within the limits of material elasticity.

The proposed MEMS interface structure can be modified to accommodate test interface circuits usually required to perform functional tests on high speed analog and RF circuits [42]. MEMS TIM as compared to the currently used device interface boards provides necessary means for fault detection at the die level. This will enable manufacturers to detect faults before packaging. Thus, the cost of packaging which is now a major portion of the overall cost of fabrication is eliminated for faulty DUTs. Furthermore, MEMS TIM can readily meet the requirements of next generation of small pitch devices predicted in the International Technology Roadmap for Semiconductors (ITRS) [39]. It is implemented using the same fabrication process developed for ICs, thus it can be downscaled to meet the predicted small pitch requirements.



Fig. 3.6: Cross section of a contact spring and a die under test (a) before applying pressure, and (b) under pressure providing a temporary connection.

3.3 Circuit Model

A circuit model for the proposed MEMS TIM has been developed to predict its behavior at high frequencies. The effects of fixed socket can be compensated by proper ATE calibration. Thus, in practice, the signal path on the removable socket dominates the behavior of the entire MEMS interface module.

To develop a circuit model for the signal path, the transmission line between ATE test channels and device under test I/O pads and the discontinuity at the contact interfaces have been taken into consideration. The circuit model for the proposed MEMS TIM is shown in Fig. 3.7. It includes three distinct parts:

- Section 1: Top Contact: this is formed between a contact spring and an I/O pin of the die under test.
- Section 2: Conductive Path: this is the electrical path between the top and bottom contact springs through the removable socket structure.
- Section 3: Bottom Contact: this is formed between the contact spring and ATE pin electronics.

Due to the geometrical symmetry of the top and bottom contact pads, an identical model for both contacts has been employed.



Fig. 3.7: Transmission line model of the proposed MEMS test interface module between the die under test and pin electronics.

3.3.1 Circuit Model for Micro-Scale Contacts

3.3.1.1 Contact Resistance Rcont

On micro-scale level, all solid surfaces are rough. The existence of surface roughness between two contacting materials results in electrical contact resistance. The actual contact is created at distinct spots formed by the surface roughness at spots known as a-spots [43] shown in Fig. 3.8. Consequently, the electrical current lines cluster together to pass through microscopic contact areas. The constriction of electrical current at a-spots reduces the total electrical current passing through the bulk interface creating contact resistance. In the proposed model, a single circular a-spot is considered to derive the electrical contact resistance. Using Laplace's equation [44], [45], the constriction resistance for a circular a-spot in a cylindrical conductor with radius R is given by

$$R_{\text{cont}} = \frac{\rho}{2\alpha} \begin{bmatrix} 1 - 1.41581 \left[\frac{\alpha}{R} \right] + 0.06321 \left[\frac{\alpha}{R^2} \right] \\ + 0.15261 \left[\frac{\alpha}{R^3} \right] + 0.19998 \left[\frac{\alpha}{R^4} \right] \end{bmatrix}$$
 3.1



Fig. 3.8: Contact between two metal surfaces at distinct spots (a-spots), and the constriction current creating the contact resistance between the two surfaces [43].

Where ρ is the electrical resistivity, and α is the constriction radius. For $\alpha \ll R$, eq. (3.1) reduces to [46, 47]

$$R_{cont} = \frac{\rho}{2\alpha}$$
 3.2

The value of α is defined by the cluster around the *a*-spot and it is independent of the location of *the a*-spots within the nominal contact area [45]. For the first approximation, α can be estimated by

$$\alpha = \left[\frac{\mathbf{A}}{\pi}\right]^{1/2} \qquad \qquad 3.3$$

Where A is the nominal contact area evaluated using standard measurements for material hardness. It is widely accepted [48], [49] that the true contact area is determined by the deformation of a-spots. Under this assumption, the area of mechanical contact can be determined from

$$\mathbf{F} = \mathbf{A}_{\mathbf{c}} \times \mathbf{H}$$
 3.4

Where F is the applied load and H represents the material hardness. Equation (3.4) states that the true contact area is independent of the nominal area and only depends on the load and the hardness of the material [47].

From $R_{cont} = \rho / 2\alpha$, $\alpha = (A_c / \pi)^{1/2}$ and $F = A_c \times H$ the contact resistance can be obtained from

$$R_{cont} = \sqrt{\frac{\rho^2 \pi H}{4F}} \qquad 3.5$$

Equation (3.9) expresses the contact resistance as a function of force and material hardness. As expected, the contact resistance is inversely proportional to the applied

pressure. Although a low contact resistance is desired, the pressure has to remain below the critical point of plasticity region where the deformation of the material is irreversible.

3.3.1.2 Contact Capacitance Ccont

The actual contact area at the contact interface is considerably lower than the apparent contact area [50]. The multi-spot nature of contact surface creates regions of parallel capacitances as shown in Fig. 3.9. Two different types of capacitors are formed between the contacts interface. In regions filled with air voids, micro air voids capacitors C_{air} are created. The actual contact points which are separated by thin insulating layers form a set of parallel micro-contact capacitors C_{mc} . Thus, the total effective capacitance is

$$\mathbf{C}_{\rm eff} = \sum \mathbf{C}_{\rm air} + \sum \mathbf{C}_{\rm mc} \qquad 3.6$$

As the actual contact area is much smaller than the apparent area, the capacitance due to the micro-contacts can be neglected. Hence, the effective contact capacitance can be approximated by the sum of the parallel elements of non-contacting regions filled with air voids [51]. For the proposed MEMS structure, the surface area of a contact pad is much larger than the separation between DUT pins and contact springs; therefore, the electric field fringing effect can be neglected. With this assumption, the contact capacitance due to the air voids can be approximated by the standard parallel plate capacitor model using an average gap between the two surfaces.



Fig. 3.9: Contact interface of air voids and micro-contacts capacitance.

$$C_{cont} = \frac{\varepsilon_0 \varepsilon_r A}{g} \qquad 3.7$$

Where \mathcal{E} is the permittivity of free space 8.85×10^{-12} F/m, \mathcal{E} is the relative permittivity of the dielectric material and g is the average gap at the interface. Due to the short path between the contacts where they are connected, the contact inductance has no significant effect and can be ignored from the contact model.

3.3.2 Contact Spring's Conductive Path Circuit Model

3.3.2.1 AC resistance

One of the critical factors that affect the signal integrity is the AC resistance. At high-frequencies, current flows near the surface reducing the effective cross section of the conductor. The current density reduces exponentially from the surface towards the center. This phenomenon, called skin effect, increases the resistance of wires at higher frequencies [52-53].



Fig. 3.10: cross section of one contact spring path.

The skin depth δ is given by

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} = \sqrt{\frac{\rho}{\pi f\mu}} \qquad 3.8$$

Where the resistivity of conductor is ρ , *f* represents frequency, and μ is the absolute magnetic permeability. As the frequency of interaction increases, the effective area of the cross section used by the current becomes smaller increasing the effective resistance of the conductor. For the proposed model, with a length of *l* and for the square cross section shown in Fig. 3.10, the AC resistance R_{AC} is equal to

$$R_{AC} = \frac{\rho l}{A}$$
 3.9

The cross section A is given by

$$A = a^{2} - (a - 2\delta) \times (a - 2\delta) = 4a\delta - 4\delta^{2} \qquad 3.10$$

$$R_{AC} = \frac{\rho l}{4\delta(a-\delta)} \frac{\rho l}{A}$$
 3.11

Where *a* is the width, *l* is the length, ρ is the resistivity of conductor, *A* is the effective cross section area, and δ is the skin depth. For the contact spring module with two identical parallel paths, the total AC resistance is equal to $R_{AC}/2$.

3.3.2.2 Self and Mutual Inductance Lself, Lm

Partial inductance represents the component of inductance that results only from the part of the current loop that is explicitly modeled. To calculate the partial inductances of rectangular cross-sectional wires, closed form equations presented in [54-56] are used. The equations for self and mutual inductances of a rectangular wire with $l \gg w + t$ are given in (3.12) and (3.13) respectively.

$$L_{self} = \frac{\mu_0 l}{2\pi} \left[ln \left(\frac{2l}{w+t} \right) + \frac{0.2335(w+t)}{l} + \frac{1}{2} \right]$$
 3.12

$$L_{\rm m} = \frac{\mu_0 l}{2\pi} \left[\ln \left(\frac{l}{d} + \sqrt{1 + \frac{l^2}{d^2}} \right) - \sqrt{1 + \frac{d^2}{l^2}} + \frac{d}{l} \right]$$
 3.13

Where d is the distance between wires, w is the width, t is the thickness, and l is the length. The self-inductance is not affected by the presence of a neighboring contact springs. The total partial inductance of each conductive path segment is

$$L_{\text{total}} = L_{\text{self}} + \sum_{1}^{i} L_{\text{mi}}$$
 3.14

where *L_{mi}* is the mutual inductance of the ith neighboring contact spring.

3.3.2.3 Mutual Capacitance C_m

Mutual coupling exists between any two adjacent conductors. The coupling is a function of area, length and the separation between them, as well as dielectric barrier thickness and permittivity. The mutual capacitance C_m per unit length for two identical cylindrical conductors [57], [58] is given by

$$Cm = \frac{\pi \varepsilon_0 \varepsilon_r}{\cosh^{-1} \frac{d}{2a}} = \frac{\pi \varepsilon_0 \varepsilon_r}{\ln\left(\frac{d}{2a} + \sqrt{\frac{d^2}{4a^2}} - 1\right)}$$
3.15

Where εo is the permittivity of free space 8.854X10-12, εr is the relative permittivity of dielectric material, d is the distance between the two conductors, and a is the radius of the conductor.

The total mutual capacitance of a single contact spring in a 3x3 array configuration is shown if Fig. 3.11, where C(m/cross) and C(m/diag) are the mutual capacitance of the neighboring contact springs. If the distance *d* between two rectangular conductors is

equal or larger than the width W as shown in Fig. 3.12, then the mutual capacitance Cm can be approximated as two cylindrical wires with similar cross-sectional area with center to center distance of (d+W) and Cm can be obtained from [59, 60]



Fig. 3.11: Total mutual capacitance of a 3x3 array configuration where *Cm/cross* and *Cm/diag* are the mutual capacitance of the neighboring contact springs.



Fig. 3.12: Two adjacent rectangular conductors.

3.4 Summary

In this chapter a new test interface module based on MEMS technology is presented. The proposed module lowers the physical separation between ATE and the device under test due to its micro-scale dimensions, as a result the undesired effect of long traces of wires on signal integrity are significantly attenuated.

The operating principle of the building blocks of the MEMS based TIM has been discussed, the dimensions of each block have been presented in this chapter.

A circuit model for the proposed MEMS TIM has also been developed to predict its behavior at high frequencies.

Chapter 4

Analysis of Simulation Results

In this chapter, design verifications using electromechanical simulations are presented to evaluate the behavior of the proposed MEMS test interface module. In addition, the RLC parameters of the proposed structure have been extracted to validate the circuit model derived in chapter two. A three dimensional prototype has also been constructed to verify the results and the system behaviour at high frequencies.

4.1 Three Dimensional Model

Layout masks for the proposed module were created to generate a 3D model using IntelliSuite CAD tools. The model was then exported to Thermo-Electro-Mechanical (TEM) analysis module.

The structure was constructed on a Czochralski [n-type, 2.54 Ohm-cm, <100> 500 μ m Silicon substrate. The substrate is patterned and etched using PR-KTI-820 photo resist to create:

- Removable and fixed sockets
- Physical cantilever spring layout

- Conductive metal layer of the MEMS spring
- Alignment keys

The Cantilevered bridge-type contact spring has a square geometry of $100 \times 100 \ \mu m$ area, with a contact pad dimensions of $50 \times 50 \ \mu m$ and $10 \mu m$ height. The metal layer is 2 μm thick.

4.2 Mechanical Reliability

Mechanical reliability of MEMS Microsystems is critical as failure can be catastrophic. The period of time over which a component or a system can function according to the nominal specifications is the measure of reliability. In order to investigate the reliability of the proposed module the following terms have to be defined:

- Yield Strength
- Ultimate Yield Strength

4.2.1 Yield strength

Yield strength or yield point of a material is defined as the stress at which a material starts to deform in an irreversible manner. A typical yield behavior is shown is Fig. 4.1. Prior to the yield point (σ y), materials deform elastically and return back to their original form when the applied stress is removed. Material response is linear within the elasticity region. This linear portion can be used to determine Young's modulus of elasticity (E) which is a measure of stiffness of elastic materials. Beyond the yield point, the deformation is permanent and non-reversible. For a reliable elastic process, the stress must be within the linear region of the material stress/strain curves.

4.2.2 Ultimate yield strength

Ultimate Yield Strength (UTS) is the maximum stress that a material can withstand before breaking [61]. The UTS (σ u) is an indication of material hardness. A high tensile modulus means that the material is more rigid.



Fig. 4.1: Typical yield behavior.

4.3 Mechanical performance analysis.

The knowledge of yield point is vital when designing a micro-electromechanical structure since it represents an upper limit to the load where the operation remains within the elasticity linear region. In designing the removable MEMS socket, Copper Beryllium (Be Cu) was selected to implement the contact springs due to

- ➢ High yield strength
- Anti-oxidation
- ➢ Non-magnetic qualities

It is one of the hardest and strongest copper alloy with a yield strength of 585-675 MPa and an ultimate strength of 690-795 MPa [62], [63]. Electro-mechanical analysis was performed to determine the maximum pressure "contact force" that can be applied during the test stage while avoiding any structural deformation.

Simulation results using Intellsuite CAD tools show a linear relationship between the deflection and the applied pressure as shown in Fig. 4.2. The graph also indicates a low pressure "contact force" to initiate the deflection of the MEMS spring-type probe. This is highly desired as a low contact force is necessary to ensure operation in the elasticity

linear region. In addition, lower contact force implies minimized scrub marks at I/O pins of the device under test. The stress distribution of the proposed structure was also analyzed using Intellsuite's Finite Element Analysis (FEA) tool. The maximum stress of the module under various deflection points are shown in Fig. 4.3. It holds a linear relationship which is an indication of a safe operation below the yield point. The deflection points extracted from Fig. 4.2 are shown to underline the stress values at these points.



Fig. 4.2: Contact spring's deflection versus pressure load.



Fig. 4.3: Maximum Von-Mises stress versus applied pressure.

In order to establish an electrical connection with an I/O pin of the unit under test, the tip of MEMS probe has to deflect 2 μ m to achieve a good connectivity and to eliminate any damage caused by the probe tip. This deflection, compared to the probe pad geometry (50x50 μ m) is sufficient to achieve a robust connectivity. The maximum stress at this pressure is 200 MPa as shown in Fig. 4.2 and Fig. 4.3, which is clearly below the yield strength of the material.

Fig. 4.4 shows a 3D full electromechanical stress analysis for the MEMS probe deflected by 2 μ m. The top surface is nearly stress-free. This maximizes the contact area between the DUT I/O pins and the MEMS probes and, as a result, reduces the contact resistance.

As expected, the maximum stress occurs at the supporting edges of the structure at 200 MPa which is one third of the yield strength (590-675 MPa). This will ensure damage free and reversible deformation since the deflection remains well below the yield point in the elasticity region. The shape of the structure greatly affects the stress distribution; square shapes or sharp edges will lead to higher local stresses and possible structural cracks. The stress in the edges can be reduced by using curved edges.

It is known that thermal expansion can cause significant stress if the design cannot tolerate any expansion or contraction of the structure. In the proposed design, the configuration of the spring arms can tolerate the stress caused by temperature variations.



Fig. 4.4: Stress analysis of the MEMS spring-probe under applied pressure of 2 MPa.

Fig. 4.5 shows stress analysis due to temperature change from -20° to 50° . The stress exhibits a linear relationship and the structure remains within the limits of linear elasticity region.

Since the MEMS probe has moving parts, fatigue can be a life limiting factor where structural damage occurs after a material is subjected to a cyclic loading and unloading. Fatigue is defined as the number of stress cycles sustained before structural breakdown. Fatigue is commonly characterized by S-N curve, also known as Wohler curve [62]. This is a diagram of the magnitude of a cyclic stress (S) against the logarithmic scale of cycles to failure (N). This curve is generated by applying a sinusoidal stress by a tester and measuring the number of cycles to failure.

For copper beryllium (Be-Cu), simulation results indicate that the maximum stress is at 200 MPa as shown in Fig. 29. The S-N curve "cycles to failure" is above 10^6 cycles at this value [63], [64]. This has been seen in many RF MEMS switches which work more or less based on the same principle. Moreover, current high end probes use Be-Cu at the contact tips, where a typical probe life of 500,000 contacts on gold pads has been reported [65].



Fig. 4.5: Stress analysis versus change in temperature.

4.4 Electrical Performance Analysis

To validate the model, the extracted characteristic parameters were used to determine the bandwidth of the transmission lines. The electrical performance of the proposed structure was analyzed using Ansoft's 3D full-wave electromagnetic field software HFSS and Q3DExtractor. This model, which is a lumped model, can be used to predict the behavior of the implemented MEMS structure up to 50 GHz due to its micro scale dimensions Table I presents the extracted lumped parameters for the MEMS probe at 50 GHz. The lumped element model is valid for $Lc \ll \lambda$, where Lc denotes the length and λ represents the wavelength.

Fig. 4.6 shows the derived and simulated results for the AC resistance as a function of frequency. It can be observed that the derived model eq. (3.15) can predict the AC resistance up to 100 GHz with a good degree of accuracy. The contact resistance of the proposed model determined from (3.9) for 2 μ m deflection at 1 MPa is 11.3 m Ω .

Mutual capacitance with neighbouring contact springs is shown in Fig. 4.7. Both extracted and mathematical values are within an acceptable range and are inversely proportional to the distance. The amount of mutual capacitance between a contact spring and the nearest neighbors is the dominant term to characterize the overall mutual capacitance as shown in Fig. 4.8. This is due to the fact that the diagonal neighbors are partly shielded by the cross conductors. As discussed in chapter three, the contact capacitance for an average gap ranging from 0.1 μ m to 0.5 μ m, varies from 340 pF/m to 70 pF/m.

Table 4.1Extracted Parameters Using Q3dextractor at 50 GHz at 100 um Pitch.

MEMS Contact Spring 100x100 μm-500 μm long	
Mutual Capacitance	4.3 fF
Partial Inductance Self + mutual	0.59 nH
Contact capacitance	170 fF-35 fF for a gap 0.1-0.5 um
RAC	423 mΩ
Contact resistance	11.3 mΩ



Fig. 4.6: AC resistance of the MEMS contact spring versus frequency.



Fig. 4.7: Extracted mutual capacitance of two adjacent contact springs.


Fig. 4.8: Scatter chart of capacitance contribution by neighboring contacts indicating the contribution of adjacent, diagonal and non-adjacent contact in blue, red and green colors respectively.

Q3DExtractor calculates partial inductance which represents the inductance that results only from the part of the current loop that is explicitly modeled. The mutual inductive effect becomes negligible as the separation distance increases as shown in Fig. 4.9. The extracted and mathematical values are in a good agreement. The self-inductance determined from (3.16) is 440 pH.



Fig. 4.9: Mutual inductance of contact springs as a function of distance.

For two coupled parallel contact springs, the total partial inductance is given by [66]

$$Ltotal = Lself + Lm$$
 4.1

Fig. 4.10 shows the partial inductance as a function of distance. As expected, the partial inductance decreases as the mutual inductance decreases with distance.

The RLC parameters of the proposed contact spring presented in Table 4.1 are very small due to the micro-scale dimension. This will allow a test channel to operate at much higher frequency compared to conventional test channels.

To demonstrate the advantages of the proposed MEMS TIM over traditional structures, a typical strip-line and coax cable were designed using Agilent ADS software tool. A strip-line of 8-cm long with cross section of 1.12x0.05 mm and a 10-cm coax cable with 1mm inner core diameter and 3.35 mm outer diameter were implemented. The scattered parameters of the implemented transmission lines and the MEMS contact spring were determined through simulation. Both the strip-line and the coax cable at 10 GHz exhibit a moderate insertion loss as shown in Table 4.2 while the MEMS structure presents a negligible insertion loss of -0.002 dB.



Fig. 4.10: Total inductance of a contact spring versus distance

3-D full wave simulations using Ansoft's HFSS simulation tool were also carried out to determine the S-parameters of the MEMS structure. In this analysis, 3-D distribution of the electric and magnetic fields are used to determine the insertion loss of the structure. The 3-D current density propagation on the surface of the MEMS contact spring is shown in Fig. 4.11 and the insertion loss up to 300 GHz is presented in Fig. 4.12. It can be seen that the MEMS contact spring can operate up to 200 GHz with less than -0.3 dB insertion loss.

	Insertion Loss (S ₂₁) at 10 GHz	Return Loss (S ₁₁) at 10 GHz
MEMS Contact Spring 100x100 μm 500 μm long	-0.002 dB	-56.2 dB
Strip-Line 1.12x0.05 mm 8cm long	-0.169 dB	-46.4 dB
Coax Cable 1.0x3.35 mm 10cm long	-0.371 dB	-45.1 dB

 Table 4.2

 Insertion loss and return loss of the transmission lines at 10 GHz.



Fig. 4.11: Ansoft HFSS 3D simulation, Current surface density.



Fig. 4.12: Ansoft HFSS 3D simulation insertion loss.

The extracted parameters in Table 4.1 were used to build a circuit model for the MEMS structure to perform transient and AC analysis using Agilent's Advanced Design System (ADS) tools. A sinusoidal waveform of one volt peak-to-peak was applied to the stripline, coax cable, and the MEMS structure as input. Fig. 4.13 shows the transient response at 50 GHz for the three extracted models. The applied input signal propagates through the contact spring without much attenuation while it is attenuated by the strip-line and the coax cable.

S-parameter analysis was also carried out using ADS tools to determine the insertion loss and the return loss over a frequency range spanning from DC to 300 GHz. Fig. 4.14 shows the insertion and the return loss of the three transmission lines. It can be seen that the MEMS structure can operate up to 50 GHz without a significant insertion loss while the insertion loss becomes much higher for the coax cable and the strip line. This is not an unexpected result since the physical dimensions of the MEMS spring are much lower than its conventional counterparts. Such a small structure can only present minute RLGC values allowing operation at high frequencies without a considerable signal loss.



Fig. 4.13: Transient response at 50 GHz. (a) 10 cm Coax cable, (b) 8 cm strip-line (c) MEMS contact spring.



Fig. 4.14: (a) Insertion and (b) return loss for MEMS contact spring, 8-cm strip-line, and 10 cm coax cable, and 10 cm Coax cable.

4.5 Summary

A MEMS contact spring was designed and simulated to evaluate its performance parameter. Electro-mechanical simulations were also performed to determine the behavior of the proposed MEMS test interface module.

Simulation results indicate that the extracted RLC parameters using Ansoft's 3D fullwave electromagnetic field software HFSS and Q3DExtractor are in good agreement with the circuit model derived in chapter three. It was also verified through simulation that the designed MEMS test interface can operate up to 200 GHz without significant signal integrity degradation.

The scattered parameters of the MEMS contact spring exhibit negligible insertion loss as compared to standard strip-line and coax cable at 10 GHz.

The stress distribution of the proposed structure was also determined using Intellsuite's finite element analysis tool. Using S-N curves, the life cycle was estimated to be over 10^6 cycles before breakdown. The device operates in the linear elasticity region well below the yield point.

Chapter 5

Fabrication Process

To validate the simulation results, two variants of the device prototype have been fabricated using customized fabrication process and SOIMUMPS process. Silicon-on-insulator (SOI) wafer is used as the starting substrate:

- Silicon thickness: $10 \pm 1 \mu m$.
- > Oxide thickness: $2 \mu m$.
- Handle wafer (substrate) thickness: 500 μm.

The prototype of the removable MEMS socket with two contact springs of $100x100 \ \mu m$ and a contact pad of $40x40 \ \mu m$ is shown in Fig. 5.1.

It was necessary to modify the proposed structure based on the limitation of available fabrication processes. The tip of the contact pad was not integrated into the prototype as electro-plating method was not available. In addition, it was difficult to deposit 10 μ m of metal by E-beam and likewise it was difficult to lift off 10 μ m of metal from the rest of the wafer. We simply flattened the structure between the top and bottom of the removable sockets as shown in Fig. 5.1. Necessary measures were taken into consideration to minimize the effects of modifications on the performance parameters. The following steps have been taken to simplify the test and fabrication of the structure:



Fig. 5.1: Prototype of the proposed MEMS probe.

- \blacktriangleright Distance between the two springs remained constant at 500 µm as per the proposed model.
- Deflection was accessible through the back-penetrated through holes; the spring geometry, thickness, and dimensions were not altered.
- Two ground and one signal contact pads have been added at 75 μm pitch to test the device with G-S-G or GS high frequency probes [65].
- ➤ A thin oxide layer has been deposited to isolate the prototype from the wafer.

5.1 Fabrication process:

- 1. **Back penetration**: The substrate is patterned and etched from the "bottom" side to the oxide layer. This allows for through-hole structures around the area of the contact springs as shown in Fig. 5.1, and opens the space for deflection.
- 2. **Physical structure**: The MEMS contact spring prototype was patterned and etched from the top side down to the oxide layer.
- Oxide removal: To open through holes around the physical structure for deflection.
- 4. **Metallization**: To establish electrical conductivity between the two contactsprings and to provide common ground for the RF probes.

The following three layers have been deposited to establish the electrical conductivity:

- > Chromium (Cr) for adhesion.
- > Copper (Cu) as the conducting metal.
- ➢ Gold (Au) thin layer for anti-oxidation.

5.2 Back Penetration

A polished SOI wafer with oxide (SiO_2) back protection layer was used as a starting substrate as shown in Fig. 5.2.

➤ Wet Chemical Etching: The oxide layer is removed using BOE (Buffered Oxide Etchant) as shown in Fig. 5.3. BOE consists of a mixture of Fluoric Acid (HF) and Ammonium Fluoride (NH₄F). The etch rate is 90 nm/min.



Fig. 5.2: Substrate with oxide SiO₂ protection.



Fig. 5.3: Oxide SiO₂ removal.

- Reactive Ion Etching (RIE): To remove any resist residuals from the exposed substrate areas on the wafer using oxygen (O₂) plasma at 10 sccm (standard cubic centimeters per minute). This step, known as Descuming, improves metal adhesion to the substrate.
- Chromium Deposition: To protect the top polished silicon surface with a thin metal layer of Cr (100 nm) as indicated in Fig. 5.4.



Fig. 5.4: Deposition of Chromium (Cr) thin metal layer (100 nm).

- > Wafer was cut into small pieces $(3x3 \text{ cm}^2)$ using an ADT 7100 dicing saw.
- Photolithography: Through-holes patterns were transferred to photo-resist material as shown in Fig. 5.5. To etch through-holes patterns, a lift-off step was required. In this step, metal layer was deposited after lithography. The metal on top of the patterned area was removed during the resist lift-off process; creating through-holes openings and leaving the metal which was deposited directly onto the substrate as a protection layer during the etching process. The lift-off process was conducted through the following steps:
 - 1. HMDS layer (hexamethyldisiloxane) for adhesion to the substrate
 - LOR5A: Lift-off resist used in combination with conventional positive resists. By optimizing the initial bake time and temperature, an undercut was created for the lift-off process.
 - Photo resists (S1813): Positive photoresist to transfer the mask patterns by ultraviolet light. Optimized for use with the MICROPOSIT MF-319 (Metal-lon-Free) developer family. Exposure (8.1 seconds at 4.9 mw/cm² measured for I-line 365 nm).



Fig. 5.5: Lithography (HMDS, LOR A5, and photo resist).

Developing: MF-319 was used to develop the positive photo resist for one minute to remove all exposed resists as shown in Fig. 5.6. It was extended for an additional minute for LOR5A resist. Samples were cleaned with DI water (Deionized water).



Fig. 5.6: Photo resist pattern after developing.

Chromium (Cr) deposition: A thin metal layer was deposited over the resist stack. The Cr layer was used to protect silicon surface from etching during the DRIE process. Cr thickness is 100 nm at a deposition rate 1-2 A^o/s, as indicated in Fig. 5.7.



Fig. 5.7: Deposition of Chromium (Cr) for silicon surface protection.



Fig. 5.8: Chromium (Cr) Lift-off.

- Lift off: Using remover PG, LOR5A was removed in ultrasonic bath, leaving open areas for etching through-holes by DRIE process as shown in Fig. 5.8.
- Piranha cleaning: Piranha is a mixture of sulfuric acid (H₂SO₄) and hydrogen peroxide (H₂O₂) with a ratio of 1:3. It is used to clean organic residues. Because the mixture is a strong oxidizing agent, it removes most organic residues. Piranha cleaning process was carried out for ten minutes.
- DRIE (Deep Reactive Ion Etching): Through holes were etched using DRIE BOSCH Process as shown in Fig. 5.9. BOSCH process, also known as pulsed etching, alternate between two modes: passivation layer using Perfluorocyclobutane (C4F8) and isotropic plasma etch using sulfur-hexafluoride (SF6).
- > Oxide removal: Oxide layer was removed using HF (hydrofluoric) solution at an etch rate of 2 μm/min as shown in Fig. 5.10. Finally, samples were cleaned by Piranha process for 10 minutes.



Fig. 5.9: Through holes DRIE etching up to the oxide layer.



Fig. 5.10: Oxide removal.

5.3 Physical Structure (Top Wafer Fabrication)

Chromium removal: Prior to the implementation of the physical structure, the thin metal layer (Cr) was removed from the top wafer surface. 200 nm SiO_2 layer was then deposited as an insulator layer to electrically isolate the wafer from the physical structure.

- Back side alignment: Infra-red alignment was used to align through holes with contact-spring physical structure.
- Lithography: The physical structure and ground contacts pattern was transferred to the photo-resist material as shown in Fig 5.11. In this step, LORA5 was made thicker to ensure proper lift-off process for the three metal layers. This was achieved by using lower spin speed at 1500 rpm for 30 seconds. The following material were used:
 - 1. HMDS
 - 2. LOR5A (Thick)
 - 3. Photoresist (S1813)

Developing time was extended to make sure that LORA5 was fully developed. RIE O_2 plasma process (Descuming) was followed to remove possible resists traces before metallisation.

- Metal deposition: Layout of the conducting metal was patterned from the top wafer surface; three metal layers were deposited using E-Beam evaporization. Low deposition rate at 1 A⁰ / second was conducted to enhance the surface roughness. The three metal layers, as indicated in Fig. 5.12, with their thickness are:
 - 1. 100 nm Chromium (Cr) layer.
 - 2. 1200 nm Copper (Cu) layer.
 - 3. 25 nm gold (Au) layer



Fig. 5.11: Lithography (HMDS, LORA5, and photo resist) for implementation of the main structure.



Fig. 5.12: E-Beam deposition of the three metal layers (Cr, Cu, and Au).



Fig 5.13: Metal pattern for the proposed prototype.

Metal lift-off: Lift-off process using PG remover was carried out in ultrasonic bath for 60 minutes. An IPA (isopropyl alcohol) rinse was necessary prior to deionized water rinse to avoid potential residues. Two-bath systems were used to reduce the possibility of re-deposition of the removed resist. In this step the geometry of the prototype metal trace was completed as shown in Fig. 5.13.

Finally, the geometry of the MEMS spring was created and etched through the following steps.

- Lithography: (HMDS + photo resist, LORA5 is not necessary since there is no lift-off process). The pattern is shown in Fig 5.14.
- ➤ Developing
- SiO₂ oxide-etch: To etch the protective oxide layer underneath the spring structure for the DRIE process. BOE was used as the etching solvent.
- DRIE: To create the contact spring geometry around the contact spring geometry as shown in Fig. 5.14. The etch depth was considered to be more than 10 µm to reach the back through-holes for complete release of the structure.
- Piranha cleaning and RIE process.



Fig. 5.14: Contact spring's top view.

5.4 Other Prototype Configurations

In addition to the prototype discussed in the previous section, various dimensions and other structures were also fabricated. For example, a module was fabricated where the deflection is controlled by the thickness of the oxide layer. These devices have the same structure without the back penetration for the through holes.

Scanning Electron Microscope (SEM) images of the fabricated prototypes are presented below. Fig. 5.15 shows the cross section of the through holes from the backside penetration. The side walls roughness (scalloping) is minimized and straight. Fig. 5.16 shows the top view for through holes of a contact spring.



Fig. 5.15: Cross section of the through holes.



Fig. 5.16: SEM top view of the fabricated device.

Fig. 5.17 shows the top view of a complete signal path connected to the RF probes; the image has been taken by Microtech summit 9101 probe station microscope.

Fig. 5.18 shows the prototype using the etched oxide layer for deflection. In this configuration the maximum deflection is $2 \mu m$.



Fig. 5.17: Top view of the prototype connected to RF probes.



Fig. 5.18: SEM image for a controlled deflection by oxide layer.

5.5 Summary

The fabrication process for the proposed prototype has been discussed in this chapter

A prototype was fabricated using customized fabrication process. A Silicon-On-Insulator (SOI) wafer was used as the starting substrate with 2 μ m oxide layer and 10 μ m silicon thickness.

To provide a space for deflection, through-holes were created from the back side. These holes were etched all the way to the oxide layer; the oxide was then removed to free the structure.

Metallization was carried by E-beam evaporation. Three metal layers were used to create the conducting layer. Copper was chosen as a conducting layer, with a thin gold layer for anti-oxidation. The wafer was isolated by a thin oxide layer (200 nm) deposited at the top surface.

Scanning Electron Microscope (SEM) images of the fabricated prototypes were also presented.

Chapter 6

Experimental Results and applications

A prototype of a MEMS probe was fabricated using 500 µm Silicon-on-Insulator (SOI) wafer. To ensure the testability of the structure, minor modifications were required. Necessary measures were taken into consideration to ensure that these modifications do not affect the device performance.

In this chapter, the measurements results will be presented. The measured performance parameters of the implemented probes have been compared with the probes currently used in the industry. In addition, the proposed probing scheme has been modified for two other applications:

- High-Density Wafer Level Test Probe Card
- Direct Probing for Through Silicon Vias (TSVs)

Prototypes for these applications have been fabricated with standard MEMS processes SOIMUMPS and UWMUMPS.

6.1 Test Interface Module Measurement Results

Scattering parameters were measured using Anritsu ME7808B Vector Network Analyser (VNA) and a Microtech GS-probe with 40 GHz bandwidth. The experimental measurements were conducted over a frequency range of 1MHz to 40GHz on Microtech summit 9101 probe station.

The measured insertion loss (S21) and return loss (S11) have been shown in Fig. 6.1 and Fig. 6.2. The results indicate an insertion loss of 0.5 dB at 40 GHz and a return loss of - 18dB at 40 GHz. These results are in a relatively good agreement with the values predicted by simulations. However, due to the bandwidth limitation of the employed VNA probe, the measurement for frequencies higher than 40 GHz could not be performed.

The differences between the simulation and measurement results are mainly due to the un-modeled contacts between the MEMS structure and the GS-probes. If these factors are taken into consideration, the difference between the measured and simulated results reduces to less than 0.2 dB over the entire measured frequency range.



Fig. 6.1: Measured insertion loss.



Fig. 6.2: Measured return loss.

The micro-probes were also placed under mechanical force exerted by the tip of Dektak stepper [67] at a deflection of 2-3 μ m to test their performance. The mechanical force was applied over a period of 24 hours. Good elastic characteristics were observed and they were neither deformed nor damaged.

Moreover, the contact springs were placed under cyclic loading using the tips of the RF GS probes with Microtech summit 9101 probe station. The controlled computer resolution of the workstation was 0.1 μ m/step. The fabricated micro-probes were placed under 2 μ m continuous deflection. After the test, the micro-probes maintained their elastic properties.

The thickness of the contact spring as mentioned before was chosen to be 10 μ m. The thickness does not affect the test procedure; however it can be adjusted to meet tight pitch requirements. The alignment for the micro-probes is critical and without an accurate alignment the test results can be affected significantly. This requirement can potentially increase the cost of testing. However, the proposed MEMS based probes do not require a

complex and costly alignment and they can use current probe stations. The positioning resolution of available probe stations is good enough for this purpose [68].

To evaluate the maximum DC power that can be delivered by each contact probe, static DC tests have also been performed using Agilent 34401A Digital Multi-meter. The current was increased to determine the DC current where the metal gets melted or cracked. The probes can handle maximum DC current of 500 mA. The testing procedure for the maximum current is shown in Fig. 6.3.



Fig. 6.3: DC current measurement, (a) Normal, (b) Cracked due to high current.

Minimum **Insertion Loss Return Loss** Typical Contact Pad Size @ 40 GHz @ 40 GHz Lifetime Resistance 20 mOhm **Cascade Microtech** 17 dB 25x35 0.9 dB >500,000 Based on **Infinity Probes** @ 40 GHz **Copper Beryllium Cascade Microtech** 18 dB 50 mOhm AirCoplanar 50x50 1.25 dB >500,000 (a) 40 GHz Based on Al Probes 50 mOhm **Cascade Microtech** 18 dB 80x80 0.8 dB >1,000,000 |Z| Probes GSG (a) 40 GHz **Based on Al Cascade Microtech** 15 dB 50 mOhm 70x70 0.8 dB >1,000,000 **Unity Probes** @ 20 GHz **Based on Al** ~20 dB > 500,000 <20 mOhm **MEMS** Probe < 40 x 40<0.5 dB @ 40 GHz **Copper Beryllium**

Table 6.1Performance comparison with existing RF probes.

Table 6.1 shows the performance comparison with the existing high-density RF probes [65]. The MEMS probe can operate at higher frequencies without a significant loss. Furthermore, it supports a smaller pitch which is highly desired to support the fine pitch requirement of next generation of ICs.

6.2 Applications

6.2.1 High-Density Wafer Level Test Probe Card

Current wafer-level test technology cannot support high-density and fast test channels. Multi-channel die probing increases the test speed and lowers the overall cost of testing. A new high-density wafer probe based on MEMS technology is implemented. High-speed MEMS micro test-channels are designed to establish connectivity between the die-under-test and the tester at the wafer level. Measurement results indicate that the proposed architecture can be used to access die pads and conduct manufacturing tests up to 40 GHz without much loss or distortion. The proposed MEMS based scheme can be used to probe fine pitch pads and interconnects of 3D ICs.

6.2.2 Direct Probing for Through Silicon Vias (TSVs)

Testing the integrity of interconnects realized by Through Silicon Vias (TSVs) in 3D IC is considered a challenging task. TSV's are excessively small and fragile for current probe technology. In this section, a new spring-type probe using Micro-Electromechanical Systems (MEMS) technology is presented. The implemented MEMS probe supports the required pitch for TSV direct probing and minimizes the undesired scrub marks on TSV surface. Simulation results indicate that the implemented MEMS probe can operate up to 50 GHz without significant test signal degradation.

6.3 High-Density Wafer Level Test Probe Card

6.3.1 Introduction

Developing manufacturing tests for new generation of ICs requires reliable and highspeed probes to access dies at the wafer level. During wafer-level IC testing, probe cards are utilized as the primary interface to establish the electrical connectivity between the device-under-test (DUT) and the Automatic Test Equipment (ATE). Test requirements are becoming more stringent, complex and costly [1, 2]. These requirements include an increasing number of test channels, tighter probe pitches, faster clock speeds, and higher measurement accuracy and resolution [3, 4]. It is essential to improve the probe card technology to meet these requirements. Manufacturing tests can play a critical rule in reducing the cost of fabrication of ICs.

An effective method to reduce the cost of testing is to increase the number of devicesunder-test through parallel testing. The pitch and accuracy of conventional probe cards are limited and they cannot readily be utilized for fine pitch IC pads. The effect of crosstalk and parasitic inductance adds additional limitations to the application of conventional needle probe cards [69]. Probe card needles have become smaller, fragile, and more likely to break. Moreover, they exert excessive vertical force on contact pad surfaces causing scrub marks and structural deformation. Current probe cards are expensive and as a result, the cost per touchdown is relatively high [69].

Various test methods have been proposed in the literature [70-75] to overcome the limitation of conventional wafer probes. In [70], a flexible polyimide membrane card which is implemented above a silicon substrate has been proposed. The main drawbacks of this solution are the deflection and force non-uniformity across the membrane leading to unreliable electrical connection among the tips. It also needs an extra gas pressure system, which increases the complexity of the ATE system. In [71, 72], thermal actuation of a bimorph has been proposed to establish the connectivity with the die I/O pads. The microprobes can only support a probing force of 45–60 μ N, which is too small to break the natural oxide on the surface of the pads. In [73] a new method using micro-spring probe card using multi-layer electroplating has been presented. This method was widely

used in the 2-D arrayed layouts by IBM for liquid crystal display LCD-driver ICs [74, 75]. However, it requires several electroplating steps that cannot be easily implemented.

A new MEMS based high-density wafer probe card using high speed spring-type micro test channels has been designed [76] in this work. These test channels are used to establish the connectivity between the die-under-test and the tester at the wafer level. In this method, multiple test points can be observed or controlled simultaneously. Furthermore, the time-to-market for MEMS probe cards is much shorter as compared to the conventional probe cards [77]. MEMS probe cards has the potential to support an increasing number of test channels and even provide access to all dies on a wafer in one-touch.

6.3.2 MEMS Probe Architecture and Simulation Results.

Fig. 6.4 shows the prototype of the implemented MEMS probe card. The connectivity between the die under test and the tester resources are established through high-speed micro test channels. The physical dimensions of the test probes are approximately 75 μ m length and 10 μ m thickness with 100 μ m pitch. The test channels have a maximum of 2 μ m room for deflection. The micro-test channels were metalized with gold for high conductivity and high anti-oxidation properties.

Electro-Mechanical analysis was performed using Intesuitte CAD tools to determine the dynamic range of the material elasticity region, and the required pressure for full deflection. The analysis in Fig. 6.5 shows a linear relationship between deflection and the applied pressure. The graph indicates that the pressure must not exceed 0.75 MPa for 2 μ m deflection to avoid physical damages to the probe and I/O contact pads.



Fig. 6.4: Prototype of the fabricated MEMS probe card. (a) Scanning electron microscope (SEM) image of the fabricated probe card, (b) Cross section of a contact spring probe indicating the thickness and the contact gap.



Fig. 6.5: Contact spring's deflection versus pressure load.

3-D full electromechanical analysis using Finite Element Method (FEM) was carried out to analyse the stress distribution across the structure at full deflection as shown in Fig. 6.6. Maximum stress of 170 MPa occurs at the supporting edges of the structure which is well below the material yield point. This ensures damage free and reversible operation where the steady state position is restored [78]. The contact pad surface is nearly stress-free which increases the contact area and reduce the contact resistance during touchdown.

At a stress of 170 MPa, S-N curves [62-63] indicate that the range of failure is above 500,000 cycles [64].

Table 6.2 presents the extracted lumped parameters of the MEMS-probe obtained at 50 GHz using Ansoft's Q3Dextractor CAD tools. The physical size of the probe is so small that the extracted parameters can be considered lumped components for test speeds up to 50 GHz. The contact resistance and contact capacitance were calculated using equations (3.9) and (3.11).



Fig. 6.6: Stress analysis of the implemented MEMS spring-probe under applied pressure of 0.75 MPa.

MEMS contact probe100µm pitch					
Mutual Capacitance	4.31 fF				
Mutual Inductance	0.14 nH				
R _{AC}	423 mΩ				
Contact resistance	11.3 mΩ				
Contact Capacitance	< 40 fF				

Table 6.2Extracted lumped parameters at 50 GHz.

6.3.3 Experimental Results and Discussion

A prototype of MEMS based probe card was fabricated on 400 μ m Silicon on Insulator wafer (SOI) as shown in Fig. 6.7 using UWMEMS process. UWMEMS process has been explained in detail in appendix B.

Scattering parameters were measured using Anritsu ME7808B Vector Network Analyser (VNA) over a frequency range of 1 MHz to 40 GHz. Fig. 6.8 shows the measured insertion loss (S21) of -1 dB at 38.6 GHz and Fig. 6.9 shows the return loss (S11) of -12 dB at 39.6 GHz. The probes can handle maximum of 500mA DC current.



Fig. 6.7: Photo of the tested MEMS contact probes.



Fig. 6.8: Measured insertion loss.



Fig. 6.9: Measured insertion loss.

The proposed MEMS based probe can also be designed as a test socket at the die level to fit fine pitch I/O pads. Table 6.3 shows the performance comparison with the existing high-density test sockets [79, 80]. The mutual capacitance and inductance for the proposed module shows higher parasitic values, this is due to the fact that these parameters have been extracted at lower pitch values which, in general, increases the mutual inductive and capacitive effects.

The implemented prototype has been designed to verify and validate the concept of utilizing MEMS technology to probe high-speed fine pitch I/O pads. The designed probecard can be modified to support tighter pitch I/O pads since it is implemented using the same fabrication process developed for ICs. Moreover, it can be modified to provide a place for interface circuits to facilitate accurate measurements during critical tests.

	Pitch um	Insertion Loss S21@ 1dB	Return Loss S11@10dB	Capacitance	Inductance	Contact Resistance
ArdentConcepts RC10-12	1000	18.1 GHz	15.7 GHz	0.463 pF	1.25 nH	NA
Johnstech PAD ROL100A	>400	40.0 GHz	14.5 GHz @ 20 dB	Mutual 0.050 pF	Mutual 0.15 nH	25 mOhm
Cascade Microtech G40	400- 800	22.7 GHz	12.4 GHz	0.129 pF	0.81 nH	<25 mOhm
Cascade Microtech G80	1000	20 GHz @ 0.6 dB	15.0 GHz	0.22 pF	1.0 nH	<25 mOhm
Verticon [™] 100 BGA	500- 1200	33.7 GHz	25.1 GHz	Mutual 0.012 pF	Mutual 0.068 nH	<50 mOhm
MEMS Probe Card	50- 100	38.6 GHz	39.58 GHz @ -12 dB	Mutual 0.0043 pF 100 um pitch	Mutual 0.140 nH 100 um pitch	<20 mOhm

 Table 6.3

 Performance comparison to existing High-Density test sockets.

6.4 Direct probing for Through Silicon Vias (TSVs)

6.4.1 Introduction

3D IC technology has the potential to significantly improve the performance of integrated systems. It enables single-chip integration of electro-mechanical structures with analog and digital signal processing functions to produce acoustic, inertial and RF systems on a single chip. The success of 3D ICs will not be fully materialized without significant progress in overcoming the challenges of developing test solutions for their mass production.

3D IC technologies allows vertical integration of multiple stacked dies into a single chip by using Through-Silicon Vias (TSVs) that utilizes short, vertical connections that passes through a silicon wafer to establish an electrical connection as shown in Fig. 6.10. This new system integration supports higher frequency of operation and lower power consumption which can lead to the creation of new generations of system-on-chips [81-85].



Fig. 6.10: 3D IC simple architecture.

Although most of the defects can be properly characterized by conventional fault models, 3D-ICs are susceptible to new class of manufacturing intra-die defects that may require new fault models. Testing TSV interconnects and the induced intra-die defects are considered by many experts a major obstacle in successful integration of 3D ICs [86], [87].

A comprehensive test for 3D-ICs includes post-bond and pre-bond tests. Pre-bond tests are performed to identify Known Good Dies (KGD). At this stage faulty die are identified and removed from the fabrication line. After adding each new die to the 3D stacked die assembly, post-bond tests are performed to ensure a fault-free bonding process.

Various built-in self-test (BIST) methods have been proposed in the literature to address the challenges of test development for 3D ICs [88], [89]. Implementation of BIST for a large number of TSVs requires a considerable die area. Current probe technology using cantilever or vertical probes require a minimum pitch of 35 μ m. Moreover, they require large contact pads added to TSVs to ensure the connectivity [90-91]. In [92], Noia and Chakrabarty have presented a DFT method for pre-bond testing; in which multiple TSVs are contacted. In this method a defective cluster of TSVs can be located however a faulty TSV cannot be clearly identified.

6.4.2 Through Silicon Via (TSV) Defects

TSV constitutes a new structure which does not exist in conventional 2D ICs [93], [99]. It is essential to investigate the type and the behaviour of TSV defects to model them correctly. These defects can occur during (a) the bonding process of copper Cu-Cu or Tin-Copper (Cu-Sn), (b) the thinning process, and (c) the fabrication of TSVs [100-104].

In the bonding process, misalignment can cause *open or short faults*. For example, in Tin-Copper TSV bonding, due to temperature and pressure effect, Tin (Sn) may spread over stacked dies creating short circuits. During the thinning process, the TSV tips need to be exposed at the back-side which can lead to new intra-die defects. Research results show that the thinning process contributes to *I-V* characteristics degradation changing device functionality [99]. In addition, the thinned dies are more vulnerable to the effects of mechanical stress caused by vertical stacked dies.

During the fabrication process, non-conformal dielectric deposition can lead to a lower breakdown voltage. Non-uniform TSV insulation caused by particles induced by impurities or dust in the fabrication process can cause defects. Insulator defect can create a bridge between the substrate and the TSV. Such a defect can be modeled by a *resistive short*. The resistive path created between TSV and substrate can add delay to the applied signals leading to slower transitions and lower voltage level [100]. A complete TSV structural breakdown leads to an *open-circuit failure*. The critical failure mechanism for TSVs during fabrication is random open defects caused by micro-voids [101] due to filling and plating mechanism. These micro-voids vary in size and shape and change TSV electrical resistance; the location is random and can lead to catastrophic faults [102]. The mechanisms associated with the TSV defects are different however; the main TSV defects caused by micro-voids reduce the speed of signal transition across the TSVs causing delay faults.

TSV tips are too small for direct access though current wafer probes. Therefore, dedicated contact probe pads located close to the TSV are added to the stacked dies to match the probe size [103], [104]. The minimum pitch of current probe pads is in the ranges of 35µm for the cantilever type probing and 100µm for vertical probes with a minimum pad size of 25µm [105], [106]. Probe pads create several problems; they occupy significant area within the die. The addition of probe pads can also create different layout implications thus their locations must be selected carefully. These implications become more severe when the number of dies increases. Ideally, the probe pads location should be placed over the TSV pad. This will minimize the area overhead and the contact resistance. Conventional on-chip probes are too stiff for TSV probing; they create scrub marks which considerably affect the contact surface. The scrub marks have a negative effect on the bonding process [107], [108].

Non electrical contacts using wireless transmitters and receivers have also been offered as an alternative solution to the problem of TSV probing [109]. However this method requires complex circuits and designs. Nevertheless, power delivery must still be made by physical contact.
6.4.3 MEMS Contact Probe for TSVs

The architecture of the proposed MEMS probe is shown in Fig. 6.11. A MEMS probe provides a temporary electrical connection with the TSV's surface during the test phase. In this work, each probe is designed to have a square geometry of $25x25 \ \mu m$ with a cylindrical contact tip of 5 μm diameter and 5 μm height.

A typical TSV has a diameter of 5 μ m and 50 μ m height. The minimum pitch between TSVs is about 10 μ m [110]. The implemented MEMS probe requires minimum pitch of 25 μ m between adjacent TSVs. However, this is not an intrinsic limitation and if required cantilever MEMS probes can be designed to handle smaller pitches. The MEMS probe is supported by two beams to sustain a balanced pressure around the contact probe tip during the contact phase. It is designed to allow maximum of 5 μ m deflection during touchdowns in the test phase.



Fig. 6.11: Layout of the MEMS probe tip in steady state.



Fig. 6.12: Cross section of the MEMS probe and a TSV (a) before applying pressure and (b) under pressure providing a temporary connection.

Fig. 6.12 shows the cross section of the MEMS contact probe and a TSV pad in the steady state during the test phase. The MEMS contact probe experiences elastic deformation due to the applied contact force in the test phase. It should be noted that in this design, the mechanical force is the only mechanism to retrieve the moving plate back to its equilibrium position. The MEMS probe is designed using copper alloy "(copper beryllium (Be Cu) which has been discussed thoroughly in chapter 4.

The proposed MEMS probes can be used as a test-access-mechanism for 3D IC to increase the observability and controllability at the test phase. These probes can provide direct access to the internal nodes of 3D ICs reducing the amount of required test data and increasing the fault coverage. They can be utilized to detect the same defects that are currently covered by conventional wafer probes. Moreover, they can be used to detect high speed transient and delay faults due to their relatively high bandwidth. TSV defects are currently modeled by stuck-at and delay faults. Thus the algorithms developed to cover these faults in ICs can be used to generate test data for TSVs.

A circuit model for the MEMS probe has been developed to predict its electrical behavior at high frequencies. As shown in Fig. 6.13, it includes two distinct sections:

- 1. TSV contact interface formed between the MEMS probe tip and the TSV contact surface.
- 2. The conductive path of the MEMS probe.

6.4.4 Simulation Results

Electro-mechanical analysis was performed to determine the maximum pressure "contact force" that can be applied during the test stage where the probe remains in the elasticity region. The analysis shows a linear relationship between the deflection and the applied pressure as shown in Fig. 6.14. The graph also indicates a low pressure "contact force" to initiate the deflection of the MEMS spring-type probe. This is one of the design objectives as a low contact force is necessary to minimize the contact resistance between the MEMS probe and the TSV contact. In addition, lower contact force implies minimized scrub marks at the TSV surface.



Fig. 6.13: MEMS probe circuit model at the TSV interface.



Fig. 6.14: Contact spring's deflection versus pressure load.

The MEMS probe tip has to deflect 1 μ m. This is to minimize the scrub marks and any damage caused by the probe tip at the TSV surface. From Fig. 6.14, it is concluded that the required pressure is 2 MPa. This deflection, compared to the probe geometry is sufficient to achieve a robust connectivity. The maximum stress at this pressure is 200 MPa which is clearly below the yield strength of the material. As a result, the MEMS probe operates in the elasticity region and restores its equilibrium position once the applied pressure is removed. Fig. 73 shows a 3D full stress analysis for the MEMS probe at a pressure of 2 MPa.

Electromechanical 3D analysis results as shown in Fig. 6.15 indicate that the proposed MEMS probe operates at one third of the Yield Strength (585-675 MPa). This will ensure reliable, reversible deformation as the deflection during the test stage remains well below the yield point. The life cycle of the probe calculated based on the measurement results indicate the probe's life cycle exceeds 500,000 contacts [62-63].



Fig. 6.15: Stress analysis of the MEMS spring-probe under 2 MPa pressure.

Table 6.4Extracted parameters using Q3dextractor at 50 GHz

	$R_{AC} m\Omega$	Inductance	Capacitance
Spring-Probe 5x5 μm	85.5 mΩ	5.6 pH	1.99 fF

The electrical performance of the proposed spring-probe model was analyzed using the parasitic parameters extracted through Ansoft's Q3Dextractor. Table 6.4 presents the extracted lumped parameters for the MEMS probe at 50GHz.

6.4.5 Experimental Results

A prototype was fabricated using 400 μ m p-type Silicon on Insulator (SOI) wafer using SOIMUMPs process. The SOIMUMPs process is a simple 4 mask level SOI patterning and etching process derived from work performed at MEMSCAP (formerly Cronos Integrated Microsystems and the MCNC MEMS Technology Applications Center). To ensure the testability of the structure, minor modifications were required. The photograph of the prototype is shown in Fig. 6.16.

The scattering parameters of the fabricated prototype were measured using Cascade semiautomatic Summit 12761B Probe Station with a controlled resolution of 0.1 um/motor step. The experimental measurements were conducted using GGB's 40 A-GS Cascade Microtech RF probes and GGB's CS-2-150 calibration substrate. The results indicate an insertion loss (S21) of 0.5 dB at 40 GHz and a return loss (S11) of -10 dB at 30 GHz as shown in Fig. 6.17 and Fig. 6.18, respectively. S-parameters above 40 GHz could not be measured due to the bandwidth limitation of the RF probes. Measured insertion and return loss are in good agreement with the simulation results. The microprobes were also placed under mechanical force exerted by Dektak stepper. Elastic properties were maintained without any structural deformation.



Fig. 6.16: (a) Scanning electron microscope (SEM) image of the fabricated prototype probe, (b) cross section indicating the deflection gap.



Fig. 6.17: Measured insertion loss.



Fig. 6.18: Measured return loss.

6.5 Summary

In this chapter, the experimental results have been presented. The measured insertion loss (S21) and return loss (S11) up to 40 GHz are in agreement with the simulation results. The TIM maintained its elastic properties without any deformation.

In addition, the proposed MEMS based TIM module was modified as a solution for testing interconnects realized by Through Silicon Vias (TSVs) in 3D IC. The MEMS based test access mechanism for ICs at the wafer level has been proposed. It supports high-speed, fine pitch contacts which increases the test speed and lowers the overall cost of testing.

Experimental measurements were conducted using Anritsu ME7808B Vector Network Analyser (VNA) and a Micrtech Microtech GS-probe with 40 GHz bandwidth. The experimental measurements were conducted over a frequency range of 1 MHz to 40 GHz on Cascade Microtech summit 9101 probe station. The measured insertion and return loss indicate that the fabricated probes can operate at high frequency range without significant test signal degradation.

Chapter 7

Conclusions and Future Works

7.1 Conclusions

7.1.1 HIGH SPEED TEST INTERFACE MODULE (TIM)

In this dissertation, a test interface module based on MEMS technology has been proposed to reduce the physical separation between the tester and device-under-test to a few hundred of micro- meters. High-speed micro test-channels are designed to establish connectivity between the device under test and the tester at the die level.

The proposed MEMS module provides a solution to problem of undesired transmission line effects that limits the bandwidth of ATE test channels. As a result, these effects are significantly attenuated allowing the test channels to operate at high frequency range without considerable signal integrity degradation.

Extensive simulations were carried out to verify the validity of the proposed architecture. Industry standard CAD tools from different vendors were used to cross-check the results. These results were also compared with the results of 3-D full wave analysis using Ansoft's HFSS and Q3Dextrator tools. Simulated s-parameters indicate that the proposed MEMS based probe can outperform the performance of traditional structures by a significant margin. This is not an unexpected result since the physical dimensions of the proposed MEMS probe are much lower than its conventional counterparts. Such a small structure can only present minute RLGC values allowing operation at higher frequencies. In fact the proposed MEMS probe can be considered a lumped component up to 60 GHz due to its microscale dimensions.

A prototype of the proposed module core has been designed and fabricated using customized process silicon on insulator (SOI) wafer. The testing has been carried out using Anritsu ME7808B Vector Network Analyser (VNA) and a Micrtech GS-probe with 40 GHz bandwidth. The measurement results using the prototype indicate that the proposed scheme can support test speeds up to 50 GHz while maintaining a high level of signal integrity.

In brief the proposed module:

- ✤ Reduces the effect of parasitic capacitances and inductances.
- Increases high speed test channels capabilities to operate beyond 50 GHz without considerable signal integrity degradation.
- ✤ Can be designed to support all types of I/O pins.
- Can provide a place for interface circuits to facilitate accurate measurements during critical tests.
- ✤ Reduces the cost of fabrication by allowing fault detection at the wafer level.

7.1.2 DIRECT PROBING FOR THROUGH SILICON VIAS (TSVS).

A MEMS probe has been designed for testing Through-Silicon Vias (TSVs) of three dimensional ICs. The proposed MEMS probe provides direct access to TSVs while reducing stress on TSV pads and minimizing the scrub marks. Measurement results indicate that the implemented MEMS probe can operate at the gigahertz frequency range without significant test signal degradation.

Electromechanical 3D analysis indicates that the proposed MEMS probe operates at one third of the yield strength. This will ensure reliable, reversible deformation during the test stage. It is also an indicator that the proposed module life cycle exceeds 500,000 contacts.

A prototype of the proposed probe has been designed and fabricated using SOIMUMPs four layer mask process my MEMSCAP Inc. Experimental measurements results indicate an insertion loss of 0.5 dB at 40 GHz and a return loss of -10 dB at 30 GHz. Good elastic performance was observed under mechanical stress, the MEMS probe was neither deformed nor damaged.

7.1.3 HIGH-DENSITY WAFER LEVEL TEST PROBE CARD

The dissertation also presents a new test access mechanism for ICs at the wafer level. High-density wafer probe based on MEMS technology has been proposed. MEMS based micro test-channels have been designed to establish high-speed connectivity between the die-under-test and the tester at the wafer level. The MEMS based test scheme can be utilized to probe fine pitch pads.

Electromechanical simulations show that the proposed scheme exerts a minute contact force during the probe touch down. The small contact force reduces the scrub marks and structural damage at the test stage.

A prototype of the proposed probe has been designed and fabricated using UWMEMS seven layer mask process. Measurement results indicate that the proposed probe card can be used to conduct manufacturing tests up to 40 GHz without much loss or distortion. Mechanical reliability was also confirmed by applying continuous load where the model preserve its elasticity and reversible deformation after the pressure load has been removed.

It is adaptable to variable die sized, and has the capability to be scalable to fit many types of I/O pins. It can support small pitch requirement for the next generation ICs.

7.2 Suggestions for Future Works

The focus of this research work was to design and implement new MEMS probes for high frequency testing to provide high speed test micro-channels.

- 1. The proposed module can be optimized in terms of mechanical reliability by
 - > Exploring various shapes to support beams of the contact spring.
 - Investigating the optimal thickness of the module for better mechanical performance.
 - Improving the electrical performance by implementing different types of substrates with lower dielectric permittivity.
- Refine the proposed design to provide contactless MEMS based probe for testing 3D ICs at the wafer and die level. The current alignment resolution for probe station can be utilized to conduct wireless testing. It is feasible to place the probe within 1-2 µm distances from either I/O pins or the TSV's, as the current probe stations can support 0.1 um resolution.
- **3**. Enhance the design of test sockets for ball grid array (BGA). The spring type probes can be configured to match the resolution of the BGA's.

Appendix A

Intellifab Process flow chart

INTELLIFAB PROCESS FLOW CHART						
		Properties	Procedure			
1	Type: Definition	Material: Si Process: Czochralski Process ID:100 Process Option:				
2	Type: Deposition	Material:PR-KTI-820 Process: Spin Process ID:Spin1 Process Option non-conf.				
3	Type: Definition	Material:UV Process: Contact Process ID: Suss Process Option:	mask: no:80111 Side: Both			
4	Type: Etch	Material:PR-KTI-820 Process: Wet Process ID: Solvent Process Option: Partial Etching				
5	Type: Etch	Material: Si Process: Dry Process ID:SF6_O2 Process Option: Partial Etching				
6	Type: Etch	Material: Si Process: Dry Process ID:SF6_O2 Process Option: Partial Etching				
7	Type: Etch	Material:PR-KTI-820 Process: Wet Process ID: Solvent Process Option: Partial Etching				
8	Type: Deposition	Material: Au Process: Bulk Process ID: Standard Process Option non-conf.	T-film (nm) :100 Sidebottom			

9	Type: Deposition	Material:PR-KTI-820 Process: Spin Process ID:Spin1 Process Option non-conf.	
10	Type: Definition	Material:UV Process: Contact Process ID: Suss Process Option:	mask_no:608 Side: Both
11	Type: Etch	Material:PR-KTI-820 Process: Wet Process ID: Solvent Process Option: Partial Etching	
12	Type: Deposition	Process: Bulk Process ID: Standard Process Option:	T-film (nm):12000 Side: Both
13	Type: Deposition	Material:PR-KTI-820 Process: Spin Process ID:Spin1 Process Option non-conf.	
14	Type: Definition	Material:UV Process: Contact Process ID: Suss	mask_no:609 Side: Both
15	Type: Etch	Material:PR-KTI-820 Process: Wet Process ID: Solvent Process Option: Partial Etching	
16	Type: Etch	Process: Dry Process ID:SF6_O2 Process Option: Partial Etching	
17	Type: Etch	Material:PR-KTI-820 Process: Wet Process ID: Solvent Process Option: Partial Etching	
18	Type: Deposition	Material:PR-KTI-820 Process: Spin Process ID:Spin1 Process Option non-conf.	
19	Type: Definition	Material:UV Process: Contact Process ID: Suss	mask_no:610 Side: Both
20	Type: Etch	Material:PR-KTI-820 Process: Wet Process ID: Solvent Process Option: Partial Etching	
21	Type: Etch	Material: Si Process: Dry Process ID:SF6_O2 Process Option: Etch Through	

22	Type: Etch	Material:PR-KTI-820 Process: Wet Process ID: Solvent Process Option: Partial Etching	
23	Type: Etch	Material: Au Process: Wet Process ID: Iodide Etch Process Option: Etch Through	Etch Type: Etch Through Time-Etch (min):2 T_Etch (nm): 990000 Side: Both
24	Type: Deposition	Material:PR-KTI-820 Process: Spin Process ID:Spin1 Process Option non-conf.	
25	Type: Definition	Material:UV Process: Contact Process ID: Suss Process Option:	mask_no: 608 Side: Both
26	Type: Etch	Material:PR-KTI-820 Process: Wet Process ID: Solvent Process Option: Etch Through	
27	Type: Etch	Material: Si Process: Dry Process ID:SF6_O2 Process Option: Partial Etching	
28	Type: Etch	Process: Dry Process ID:SF6_O2 Process Option: Partial Etching	
29	Type: Deposition Process: Evaporate Process ID:E-Beam Process Option: conform	Recipe: 29# Time-dep (min):10 T-film (nm):2000 Side: Both	
30	Type: Deposition	Material:PR-KTI-820 Process: Spin Process ID:Spin1 Process Option: non-conf.	
31	Type: Definition	Material:UV Process: Contact Process ID: Suss Process Option:	mask_no(#):610 Side: Both
32	Type: Etch	Material:PR-KTI-820 Process: Wet Process ID: Solvent Process Option: Partial Etching	
33	Type: Etch	Material: Au Process: Wet Process ID: Iodide Etch Process Option: Etch Through	Etch Type: Etch Through Time-Etch (min) T_Etch(nm):990000 Side: Both

34	Type: Etch	Material:PR-KTI-820 Process: Wet Process ID: Solvent Process Option: Sacrifice	
35	Type: Deposition	Material:PR-KTI-820 Process: Spin Process ID:Spin1 Process Option non-conf.	
36	Type: Definition	Material:UV Process: Contact Process ID: Suss Process Option:	mask_no:11116 Side: Both
37	Type: Etch	Material:PR-KTI-820 Process: Wet Process ID: Solvent Process Option: Partial Etching	
38	Type: Etch	Process: Dry Process ID:SF6_O2 Process Option: Partial Etching	
39	Type: Etch	Material:PR-KTI-820 Process: Wet Process ID: Solvent Process Option: Sacrifice	

Appendix B

SOIMUMPs Design Process ^{1, 2}

A general process description for micromachining of Silicon-on-Insulator (SOIMUMPs) structures is presented (1, 2).

The MUMPs (Multi-User MEMS Processes) is a cost effective industrial process for proof-of concept MEMS fabrication. It is available for universities, government and industry sectors. It is a general process designed to support several designs on a single silicon wafer.

Three standard processes are offered by MEMSCAP as part of the MUMPs® program:

- PolyMUMPs: A three-layer polysilicon surface micromachining process.
- MetalMUMPs: Electroplated nickel process.
- SOIMUMP: Silicon-on insulator micromachining process.

The SOIMUMPS process uses Silicon-On-Insulator (SOI) wafer as the starting substrate. There are two types for the SOI wafer:

- Silicon thickness:
 - a) $25 \pm 1 \,\mu m$.
 - b) 10 ± 1 mm.
- Oxide thickness:
 - a) 1 μ m for the 10 μ m silicon.
 - b) $2 \mu m$ for the 25 μm thickness.
- > Handle wafer (Substrate) thickness: 400 ± 5 mm.

2. CMC Microsystems SOIMUMPs Design Handbook, Rev. 8.0 [112].

^{1.} MEMSCAP Inc. [111].

The following notations and colors are adapted by MEMSCAP for their process flow [111-112].

Silicon	Substrate	Bottom Oxide	Shadow Mask
Oxide	Metal	PSG (dopant)	Frontside Protection Material

SOIMUMPs process consists of 4 simple mask layers SOI patterning and etching process. It was originally derived from work process performed at MEMSCAP. The starting substrate is Silicon On Insulator wafer polished at both sides. The top surface of the SOI wafer is doped with phosphosilicate glass (PSG) layer annealed with Argon for 1 hour. The deposited PSG layer is removed using wet chemical etching as shown in Fig. A1.

The Pad Metal is the first layer deposited (Mask Level: PADMETAL). It consists of 20 nm of chrome and 500 nm of gold. The stack metal layer is patterned through a lift-off process. Features can be transferred with a 3 um resolution to the Device layer. During the Deep Reactive Ion Etch (Deep RIE) process, the metal layer must be covered, thus it is limited to relatively large areas in the actuator. Surface roughness has the tendency to be higher as this metal is exposed to relatively high temperatures during the DRIE process; therefore, the SOIMUMPS is not suitable for low-loss optical mirror applications as shown in Fig. A2.

The second mask Level (Mask Level: SOI) is patterned through lithography, and then etched using Deep RIE. This process is implemented using Inductively Coupled Plasma (ICP) technology. Etching continues until the oxide layer is reached as shown in Fig. A3. Next, a protection material is deposited to the top surface of the Silicon layer to prepare the wafer for the back penetration. This layer is to protect the wafer surface from ant scratches or damage during the DRIE process where the wafer is placed on to the wafer holder.

The back side of the SOI wafer is lithographically patterned (Third mask level TYRENCH). The mask pattern is then etched using the DRIE process to establish the

through holes features. The back etching is carried all the way to the buried oxide layer as shown in Fig. A4.

After reaching the oxide layer from the back side, the buried oxide is etched through a wet oxide etch process. The oxide regions to be etched are defined by the TRENCH mask. The protection material on the top wafer surface is removed in a dry etch process. This wills releases the mechanical structures in the Silicon layer located over the back penetrated through-holes defined by the TRENCH mask as shown in Fig. A5. To minimize stiction, a vapor HF process is used to remove the remaining exposed oxide layer from the top side of the SOI wafer. This step is necessary to allow electrical contact to the Substrate. Also it is required to provide an undercut in the oxide layer that will prevent any metal shorts between the Silicon layer and the Substrate layer.

A shadow masking technique is used to deposit and pattern the blanket metal layer, consisting of 50nm Cr+ 600 nm Au. The shadow mask is arranged from a separate double side polished silicon wafer. The shadow mask is then patterned with the BLANKETMETAL mask, the through holes for the BLANKETMETAL mask is etched by DRIE process. Metal is evaporated using an E-Beam tool. Metal is deposited on the top surface of the Silicon layer only in the through-holes regions of the shadow mask (Fig. A6). After evaporation, the shadow mask is removed, leaving a patterned Metal layer on the SOI wafer (Fig A7). The wafers are then diced using a laser, sorted and complete.





Fig. A1: A phosphosilicate glass layer (PSG) is deposited, and the wafers are annealed at $1050 \,^{0}$ C for 3 hour in Argon to drive the Phosphorous dopant into the top surface of the Silicon layer. The PSG layer is subsequently removed using wet chemical etching [112].



Fig. A2: The wafers are coated with UV-sensitive photo-resist and lithographically patterned by exposing the photo-resist to UV light through the first level mask (SOI), and then developing it. The photo-resist in exposed areas is removed, leaving behind a patterned photo-resist mask for etching. Deep reactive ion etching (DRIE) is used etch the Silicon down to the Oxide layer. After etching, the photo-resist is chemically stripped [112].



Fig. A3: Protection material is applied to the top surface of the patterned Silicon layer. The bottom side of the wafers are coated with photo-resist and the second level (TRENCH) is lithographically patterned. Reactive ion etching (RIE) is used to remove the Bottom Side Oxide layer. A DRIE silicon etch is subsequently used to etch completely through the Substrate layer, stopping on the Oxide layer. After the etch is completed, the photo-resist is removed. A wet oxide etch process is then used to remove the Oxide layer in the regions defined by the TRENCH mask [112].

Release" – Protection Layer and Oxide layer removal



Fig. A4: Protection material is then stripped using a dry etch process. The remaining "exposed" Oxide layer is removed from the top surface using a vapor HF process. This allows for an electrical contact to the Substrate layer, and provides an undercut of the Oxide layer [112].

Metal Shadow Mask Fabrication Mask Level: BLANKET METAL



Fig. A5: A separate silicon wafer is used to fabricate a shadow mask for the Metal pattern. Standoffs are pre-fabricated into the shadow mask so that the shadow mask does not come into contact with patterned features in the Silicon layer of the SOI wafer. The shadow mask wafers are then coated with photo-resist and the third level (METAL) is lithographically patterned. DRIE silicon etching is used to etch completely through the shadow mask wafer, producing through holes for the Metal to be evaporated. After the etch is completed, the photo-resist is removed [112].

Shadow Mask Bonding and Mirror Metal Deposition



Fig. A6: The shadow mask is aligned and temporarily bonded to the SOI wafer. The Mirror Metal layer, consisting of 50 nm Cr + 600 nm Au, is deposited through the shadow mask [112].

Shadow Mask Removal



Fig. A7: The shadow mask is removed, leaving a patterned Metal layer on the SOI wafer [112].

Material Layer	Thickness (µm)	Lithography Level Name	Lithography Level Purpose	Comments
Pad Metal	0.52	PADMETAL	Provide metal for electrical interconnects	20 nm Cr 500 nm Au
Silicon	10 or 25	SOI	Define structures in Silicon layer of SOI wafer	
Oxide	1 or 2			
Substrate	400	TRENCH	Define through-hole structures in Substrate layer of SOI wafer	
Blanket Metal	0.65	BLANKETMETAL	Pattern through holes in shadow mask. The shadow mask is then bonded to the SOI wafer so that a patterned Metal layer is achieved when the Metal is deposited.	50 nm Cr + 600 nm Au

Table B1Layer names, thicknesses and lithography levels [112].

Table B1 summarize the thickness, lithography level names and material for the SOIMUMPs process [112].

Layout Requirements:

The design area for SOIMUMPs is 9 mm x 9 mm. Due to the incorporation of an exclusion zone required for the Metal shadow mask bonding process, the actual size of the chips that are shipped to the user is 1.115 cm x 1.115 cm. (The 9mm x 9mm user design area is centered in the chip). Users are advised to place any critical elements of their designs at least 0.25 mm away from the edge of the 9 mm x 9 mm usable area.



Usable chip area

Appendix C UWMEMS Design Process¹

The UW-MEMS Process is a multi-user MEMS fabrication process optimized for industries, universities and government organizations. It is offered at the University of Waterloo, Waterloo, Ontario, Canada. The process is a surface micromachining process gold-based originated from work derived by the University of Waterloo over the past 6 years. In general, it has been optimized for RF applications. However, the process can be applicable to wide range of MEMS devices.

The UW-MEMS process consists of seven mask processes. This process has been developed and optimized at the University of Waterloo, Center for Integrated RF Engineering (CIRFE). The starting substrate is 0.025 inch thick Aluminum which is polished on both sides. The relative permittivity of the substrate is 9.8 with loss tangent of 0.0001 at 1 MHz. E-beam-write chrome masks are used in UW-MEMS process.

^{1.} Center for Integrated RF Engineering (CIRFE) at the University of Waterloo, Waterloo, Ontario, Canada [113].

Table C1Materials, thicknesses and mask levels [113].

Table C1 outlines the materials, thicknesses and mask levels for each layer in the UWMEMS fabrication process [113].

MASK#1Chromium

The process begins with standard cleaning steps (RCA) to remove oxide layers, organic and ionic contaminants. The first layer of Chromium (Cr) is then patterned and deposited using the lift-off technique.



Mask #1 patterning [113].

MASK#2 Dielectric1

Silicon Oxide $(0.5 \ \mu m)$ is deposited over the Cr layer by Plasma-Enhanced Chemical Vapor Deposition (PECVD) process. Next, the oxide is patterned by RIE (Reactive Ion Etching) process. In this step, the patterning photo-resist is also removed.



Mask #2 patterning [113].

MASK #3 Gold 1

A bilayer metal consists of 400 Å chromium and 100 nm gold is deposited by evaporation as a seed layer. The Cr is deposited as an adhesion layer for the gold metal. 1 μ m gold is electroplated inside a mold formed in the third lithographic step. Both the mold and the seed layer are removed.



Mask #3 patterning [113].

MASK #4 Dielectric 2

Silicon oxide dielectric layer is deposited over the first gold metal for beam elevation. 300 Å of chromium (Cr) film is sputtered as an adhesion layer for the silicon oxide to the gold followed by 0.7 μ m oxide using PEVCD process.



Mask #4 patterning [113].

MASK #5 Anchor

To clear an opening for the anchor, spin coated polyimide is deposited as a sacrificial layer. Initially, the coating is $2.5 \mu m$ thick. The polyimide is patterned and then etched by RIE process to establish the hole for the anchor deposition.



Mask #5 patterning [113].

MASKS #6 DIMPLE

Dimples are created by photo-resist mask using RIE etching process. The depth of the dimples is 1 μ m.



Masks #6 patterning [113].

MASK #7 GOLD 2

The second gold layer which is used as the structural device layer consists of a sputtered seed layer and an electroplated fold layers. The total thickness of both layers is $1.25 \mu m$. The definition (geometry) of this layer is done by moulding method.



Masks 7 patterning [113].

Release Process

Before the final release, the wafers are diced into individual dies. The sacrificial lay is then removed using oxygen plasma dry-etch process. The process is complete and samples are packaged at this step.



Released Device [113].

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Education

PhD in Electrical and Computer Engineering 2008-2012 University of Windsor, Ontario, Canada Advisor: Dr. Majid Ahamdi, Co-Advisor: Dr. Rashid Rashidzadeh Dissertation topic: High Speed Test Interface Module Using MEMS Technology 1991-1993 M.Sc. in Electrical and Computer Engineering Iowa State University, Ames, Iowa, USA Advisor: Dr. Vikram Dalal Dissertation topic: Stability Studies on Hydrogenated Amorphous Silicon Films **Using Reactive Plasma Beam Epitaxy B.Sc.** in Electrical and Computer Engineering 1987-1991 Iowa State University, Ames, Iowa, USA **Concentration: Electronics B.Sc.** in **Physics** 1983-1987

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Honors and Awards

MNT Technology Award, Canadian Microelectronics Corporation	2012
Fredrick Atkins Graduate Award, University of Windsor	2008-2012
Ian and Terrya Graduate Award, University of Windsor	2012
A. R. & E. G. Ferris Graduate Award, University of Windsor	2012
Vice President Research Award. University Of Windsor	2011
MNT Award, Canadian Microelectronics Corporation	2012
Graduate Student Scholarship, University of Windsor	2008-2012
Top Innovations at IEEE International Test Conference	Nov. 2010
Special recognition at Canadian Microelectronics Corporation	2010
Graduate Student Scholarship, Iowa State University	1989-1993
King Hussein Award. University of Jordan, Valedictorian	1987