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Characterization of a CMUT Array

by

Tugrul Zure

A Thesis
Submitted to the Faculty of Graduate Studies
through Electrical and Computer Engineering
in Partial Fulfillment of the Requirements for
the Degree of Master of Science at the
University of Windsor

Windsor, Ontario, Canada

2011

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Characterization of a CMUT Array

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DECLARATION OF ORIGINALITY

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ABSTRACT

Ultrasound transducers are used in a broad range of applications covering from underwater communications to medical imaging and treatment. The ultrasonic transducer determines the key specifications such as resolution, sensitivity and signal to noise ratio. The capacitive micromachined ultrasonic transducer (CMUT) has emerged as an alternative to standard piezoelectric transducers due to advanced microelectronics fabrication technology and methods. Comparing to piezoelectric transducers, the CMUT is superior to it's competitor with higher acoustic bandwidth, higher sensitivity and greater coupling with the acoustic medium. Design, fabrication, and characterization of a capacitive micromachined ultrasonic transducer (CMUT) array have been presented along this thesis. The array is designed to operate in the frequency range of 113-167 kHz. The CMUT array is fabricated using an SOI based fabrication technology and includes 6x6 CMUTs. Necessary test setups and readout circuitry is designed in order to carry out the characterization process. Static analysis results are verified with Wyko™ optical profilometer, Agilent™ LCR meter and SEM analysis. Dynamic characterizations are done with Polytec™ MSA-4 laser Doppler vibrometer. An efficient and low noise capacitive readout circuit is designed using transimpedance amplifier scheme with 75 kΩ gain and fabricated on a PCB. The developed analytical models, FEA and experimental results are in very good agreement to exhibit accuracy of the design methodology.

DEDICATION

I would like to dedicate this thesis to my parents, Bulent and Muhlise Zure, and whoever benefits from this publication.

ACKNOWLEDGEMENTS

This thesis would not have been possible without the guidance and support of my thesis advisor, Dr. Sazzadur Chowdhury. I have learned from his great discipline and professional style through the research work, and those qualities will remain with me through my career.

I would like to thank my committe members, Dr. Elena Maeva and Dr. Roberto Muscedere for their valuable reviews and comments on the manuscript.

I would also like to thank the technical and administration staff members of Electrical and Computer Engineering at University of Windsor. I appreciate great help of Ms. Andria Ballo, Ms. Shelby Marchand and Mr. Frank Cicchello.

I am greatly thankful to my friends and colleagues, Fatih G. Sen, Ayca Yurtseven, Sundeep Lal, Ismail Hamieh, Jonathan Hernandez, Ali Attaran and Ashim Raj Das for making my life easier.

I would like to express my graditute for Dr. Eihab Abdel-Rahman and Ph.D. candidate Mahmoud Khater from University of Waterloo for their valueable support in characterization process and allowing me to their lab equipments. I would also like to thank Dr. Ahmet T. Alpas and Ph.D. candidate Fatih G. Sen from University of Windsor for allowing me to use their lab.

Finally, this thesis is dedicated to my parents and brother, who supported me through the period of research, and helped me to overcome difficulties.

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LIST OF ABBREVIATIONS

MEMS – Microelectromechanical Systems

CMUT – Capacitice Micromachined Ultrasonic Transducer

LCR – Inductance, Capacitance and Resistance

SOI – Silicon on Insulator

MSOI – Multilayered Silicon on Insulator

FEA – Finite Element Analysis

PCB – Printed Circuit Board

DC – Direct Current

AC – Alternating Current

RCA – Radio Corporation of America

DRIE – Deep Reactive Ion Etching

BOE – Buffered Oxide Etch

SNR – Signal to Noise Ratio

BW – Bandwidth

LDV – Laser Doppler Vibrometer

BNC – Bayonet Neill-Concelman

BOX – Buried Oxide Layer

HF – Hydrogen Fluoride

HMDS – Hexamethyldisilazane

UV – Ultraviolet

TFA – Trifluoroacetic Acid

CPD – Critical Point Drying

RMS – Root Mean Square

Spice – Simulation Program with Integrated Circuit Emphasis

BCB - Benzocyclobutene

NOMENCLATURE

C = capacitance

C_0 = parallel plate capacitance

C_{ff} = fringing field factor

C_F = feedback capacitor

C_{Deform} = deformed parallel plate capacitance

C_{in} = input capacitance

C_S = sensor capacitance

C_C = cable capacitance

C_{AMP} = operational amplifier total parasitic input capacitance

C_a = air gap compliance

C_m = diaphragm mechanical compliance

R_r = radiative resistance

R_g = air gap loss

R_h = movable plate vent loss

M_r = air mass

M_m = diaphragm mechanical mass

p_0 = air density

c = sound velocity

ω = angular frequency

ω_i = angular resonant frequency with respect to the resonant mode i

w_0 = diaphragm center deflection

T = tensile force per unit length

Q = quality factor

Q_i = quality factor with respect to the resonant modde

σ = residual stress

ε_r = relative dielectric constant

ε_0 = permittivity of the free space

ε_{rm} = dielectric constant of the top membrane

ε_{ri} = dielectric constant of the top electrode

D = flexural rigidity

D_{eff} = effective flexural rigidity

P = incident acoustical pressure

P_{Ext} = external mechanical pressure

V = volt

V_o = output voltage

V_b = bias voltage

E = Young's modulus

$\tilde{E}$ = effective Young's modulus

v = Poisson's ratio

d = average airgap distance

d_c = conductor thickness

d_0 = airgap

d_{eff} = effective airgap

d_m = membrane thickness

d_i = top electrode thickness

d_{0-OCI} = thickness of the dielectric medium

w_{0-OCI} = on chip interconnect width

h_{0-OCI} = on chip interconnect thickness

a = half side length

n = hole density in the diaphragm

α_{sf} = surface fraction occupied by holes

α = mass damping factor (Rayleigh damping coefficient)

u = air viscosity coefficient

Z_t = equivalent impedance

S_t = total sensitivity

f_{res} = resonant frequency

f_z = frequency of the zero in the system

f_p = frequency of the pole in the system

f_{-3dB} = cut-off frequency

f_H = higher f_{-3dB} frequency

f_L = lower f_{-3dB} frequency

f_{AOL} = frequency at the intersection of the noise gain and the open loop bandwidth

f_u = gain bandwidth product

k = stiffness parameter

m = mass

g = airgap distance

x = displacement

$\dot{x}$ = first derivative of displacement

$\ddot{x}$ = second derivative of displacement

b = damping factor

β = stiffness damping factor

ξ_i = damping factor with respect to the resonant mode i

R_F = feedback resistor

i_{in} = input current

Z_{CMUT} = impedance of CMUT

Z_{in} = input impedance

Z_F = feedback network impedance

F = feedback factor

B = operational amplifier input noise density at 1 Hz

K = Boltzmann's constant

T = temperature in Kelvin

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Chapter 1

INTRODUCTION

1.1 Goals

The objective of this project is to design, fabricate and characterize a CMUT (Capacitive Micromachined Ultrasound) array for air-coupled applications such as blind spot monitoring for cars. The CMUTs have become a strong alternative to piezoelectric transducers in medical imaging and immersion applications, however research has been mainly focused on immersion applications, and few research efforts are made for air-coupled CMUTs and their characterization. CMUT's enabled wide bandwidth imaging of tissues and vessels and with better resolution [1]. Intravascular ultrasound imaging i another techniques enabled by the CMUT technology which occupies very small area while providing excellent transducer characteristics. Moreover extensive research has been done for non-destructive valuation [2], microphones [3] and smart microfluidic channels [4]. As explained above, much of the research has been focused on immersion applications. This thesis investigates air-coupled CMUT applications such as park assist and blind spot monitoring.

The specific goals of this thesis is 1) design and fabricate a CMUT 2) design and realize a transimpedance amplifier based read out circuit, and 3) develop necessary test benches and equipment to carry out the characterization processes in order to obtain the experimental data, and compare the experimental data with the theoretical simulation results from analytical model using Matlab™ and Intellisuite™ finite element analysis simulation results. Characterization process is divided in two sections, which are static and dynamic characterization. Laser Doppler vibrometer is used to obtain the AC

characteristics of the CMUT membrane. For static characterization, experimental data is obtained from optical profilometer, scanning electron microscope and capacitance meter.

For static characterization purposes, the deflection profile of the CMUT membrane is characterized using analytical load deflection model, FEA (Finite Element Analysis) and optical profilometer. Laser vibrometer is used for dynamic characterization in order to obtain steady state response and transient response of the diaphragm. For air-coupled transmission tests, designed readout circuit based on transimpedance amplifier is used to operate the CMUT in receive mode.

This work is believed to provide useful guidance on characterization of CMUTs, therefore bridging the gap between the theory and practice.

1.2 CMUT Operating Principle

A typical CMUT geometry is built with a square, circular, or hexagonal diaphragm separated from a fixed backplate by a small airgap. Typical cross section of a square diaphragm CMUT is shown in Figure 1.1.

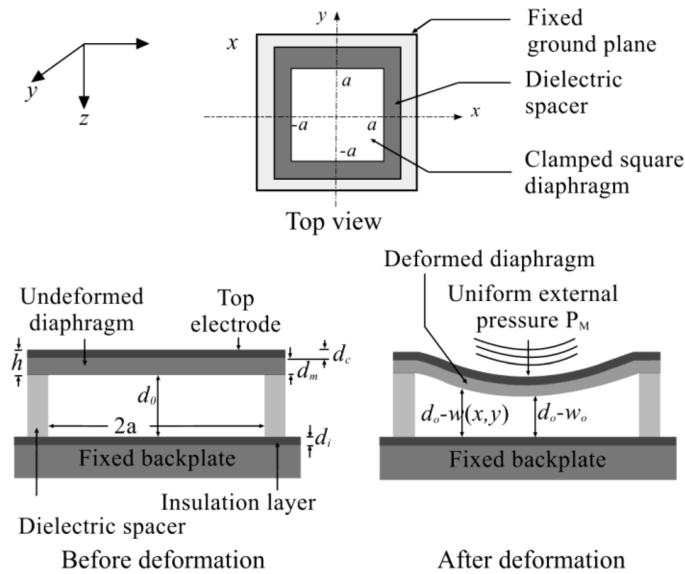


Figure 1.1. CMUT cross section [38].

The CMUTs have reciprocal properties; that is it can operate both as a receiver of ultrasound and also as a transmitter or an emitter. In the receive mode, the incident ultrasound wave causes a deformation of the diaphragm to affect a change in the capacitance between the diaphragm and the backplate. A suitable microelectronic circuit is used to convert this capacitance change to a useful voltage signal [1], [5], [6] . In the transmit mode, an AC signal of suitable amplitude causes the diaphragm to vibrate to create an ultrasonic vibration in the surrounding medium.

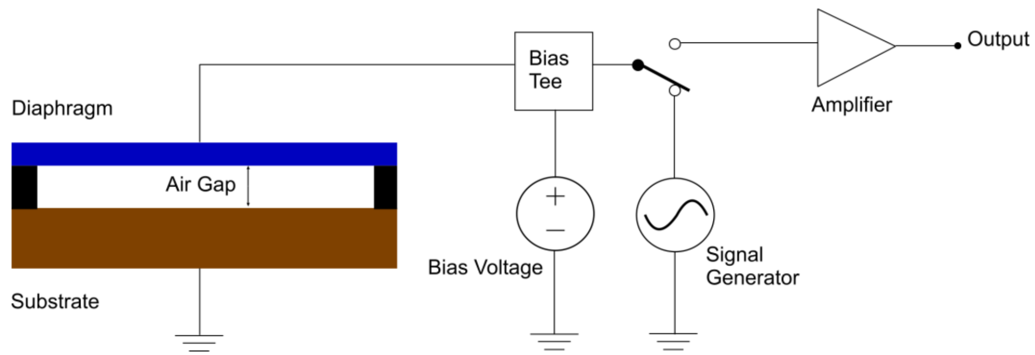


Figure 1.2. CMUT modes of operation.

A control signal operates a switch to enable mode switching from transmit to receive and vice versa as seen in Figure 1.2. Typically, the diaphragm is created using a microfabricated thin film conductor such as aluminum or polysilicon or a composite of a non conducting thin film structural material such as silicon nitride with a thin coating of a conducting material such as aluminum or gold on the top is used. Additionally, to avoid electrical breakdown after collapse due to the pull-in phenomenon, a thin insulation layer, either under the diaphragm conducting material or on the top of the backplate is used. Finally, a passivation layer on the top of the diaphragm is used to protect the CMUT from environmental elements.

As the CMUT's sensing characteristics depend on the change of capacitance between the deformed diaphragm and the backplate, accurate calculation of the capacitance between the deformed diaphragm and the flat backplate is crucial and the calculation must take account of: 1) the deformed shape of the diaphragm, 2) contribution of the fringing field capacitance associated with charge concentration at the diaphragm edges, and 3) dielectric contribution of the thin insulation layer used to protect the device against any electrical breakdown.

1.3 Background

Acoustical sensors have been used for a long time since World War I for underwater imaging and further improvements in piezoelectric materials have been done during World War II [1]. Increased computing power have enabled more complicated algorithms to be run with larger amounts of data from transducers, however the quality of transducers and read out circuit (SNR, bandwidth, etc.) determines the final results of ultrasound systems, therefore making front-end electronics and transducers as the most critical components of ultrasound imaging systems [1] . Recent advances in microfabrication technology made small air gaps to be made, therefore creating very large electric field strengths required for capacitive electrostatic transducers to work effectively, and compete with piezoelectric transducers. CMUTs also offer advantages of larger bandwidth, large arrays with individual electrical connections and integration with microelectronics [7]. As the CMUT's improved over the time, the characterization techniques and understanding of the working principles have advanced as well.

Characterization provides the validity of the theory, design methodology and fabrication of the device. It is also useful for making improvements in theoretical equations by data fitting. For static response of CMUT, it is common to use non-contact optical profilometers, which scan the surface of the CMUT under a microscope using optical interferometry method. Another reported static characterization method is called Dynamic Holographic Microscopy [8] , using the principle of holography.

For dynamic response of CMUTs, laser Doppler vibrometer (LDV) is becoming the most common choice, because it causes no loading effect on the membrane, exploiting Doppler Effect of the laser beam. Limiting conditions for LDV is the surface

roughness, and a good reflection back to the laser sensor is required [9]. Moreover, their very high cost decreases accessibility of the device.

There are many approaches to design of a readout circuit for CMUTs, including charge amplifier [10], transimpedance amplifier [11] and standard voltage amplifier. Charge amplifier has an advantage of high sensitivity by using charge transfer method, but when the transducer has relatively high DC current leakage, this solution becomes troublesome. Transimpedance amplifier has large bandwidth, good sensitivity and flexibility for many capacitive sensors. Last alternative, voltage amplifiers are not used commonly due to small input impedance of the amplifier and high output impedance of the capacitive sensors.

1.4 Scientific Approach

According to [1], [12] and [13], it has been shown that the static deflection due to electrostatic force and acoustic force can be modelled accurately compared to FEA results. This thesis provides methods and experimental data for validation of the previously developed mathematical models by MEMS Lab. Thesis also extends the static characterization into the dynamic characterization area, in order to accurately predict diaphragm's transient response. Non-contact surface profilometer is used in this thesis, and they are often used in material engineering and their resolution is under 1nm vertically [14], which is far exceeding the resolution needed for this work. Scanning electron microscope (SEM) plays an important role of the static characterization, since every detail about the fabricated CMUT have to be known in order to achieve good accuracy in static and dynamic characterization of the device.

Laser Doppler vibrometer (LDV) is the most accurate method available to characterization researchers for dynamic analysis [15]. LDV extracts the time varying displacement and velocity of the surface due to electrostatic change as a function of time. Steady state response of the diaphragm due to frequency of excitation voltage and transient response due to impulse excitation voltage are obtained with LDV technique.

1.5 Literature Search

In recent years, significant progress has been done in modelling and characterization of the CMUTs in air and immersion applications. The first air coupled CMUT was presented by Stanford researchers M.I. Haller and B.T. Khuri-Yakub [16]. Group fabricated two devices based on work of Mason [17], the transducers were fabricated using standard micromachining techniques. They have used an optical interferometer was used to measure the peak displacement of the 1.8 MHz electrostatic transducer at 230 Å/V.

In [18], 275 x 5600 μm one dimensional CMUT array was characterized successfully, showing good agreement with theory. Device operated at 3 MHz in immersion, with a DC bias of 35V, outputting 5 kPa/V.

FEA simulations are an important part of CMUT design to understand the transducer characteristics and optimize the transducer response [1]. Authors of [19] showed that the device performance can be optimized by depositing the electrode where it works the most effective by FEA simulations. Authors showed that bandwidth of the metalized devices are twice of the fully metalized CMUT devices. B. Bayram et al [19] used FEA to model a circular membrane CMUT. They concluded that the collapse voltages of half-metallized and full-metallized structures are almost equal for typical

metal plate thickness. Authors of [20] state that the equivalent circuit model of the CMUT lacks important features such as coupling to the substrate and the ability to predict cross-talk between elements of an array of transducers. They have proposed the evidence of crosstalk between CMUTs and took precautions including change of its thickness and etched trenches or polymer walls between array elements.

Stanford researchers I. Wygant, M. Kupnik et al. has fabricated CMUTs with vacuum- sealed cavities for transmitting directional sound with parametric arrays for air coupled applications which have resonance frequencies of 46 kHz and 54 kHz, respectively. [21]. Characterization of the CMUTs showed center frequencies of 46 kHz and 55 kHz and 3 dB bandwidths of 1.9 kHz and 5.3 kHz for the 40 μm and 60 μm thick membrane devices, respectively. Although they have achieved a range of 3 m, the devices operate with excessive DC bias and AC excitation voltages that cannot be found outside the laboratories.

M. Torndahl et. al has compared two similar piezoelectric and CMUT transducers using light diffraction tomography method [22]. They have found out superior bandwidth characteristics of CMUTs comparing to piezoelectric transducers.

M. Buigas, F. Espinosa et al. characterized their fabricated CMUT for immersion applications in [23]. CMUTs impulse response is obtained through a send-and-receive experiment to be compared with the theoretical results. They have used data fitting to achieve a good agreement between theoretical and experimental results. A readily available calibrated hydrophone is used in characterization tests in order to measure output pressure.

J. Kiihamaki et al proposed a new concept for SOI MEMS devices, called plug up [24]. They reported a novel process sequence for fabricating micromechanical devices on silicon-on-insulator (SOI) wafers. Authors concluded the advantages of the techniques as improved immunity to stiction and elimination of conductor metal endurance problems during sacrificial etching in hydrofluoric acid. Authors validated their theory with a fabricated CMUT device successfully.

Authors of [25] proposed an SOI based CMUTs and characterized it with an impedance analyzer. Their CMUTs consist of 2700 circular active cells of 65 mm diameter, with 2 mm thick silicon membranes suspended over a 0.5 mm air gap.

S.T. Hansen et al [26] reported air coupled CMUTs with dynamic range larger than 100dB, for non-destructive testing purposes. Experiment was done using two identical transducers facing each other, with a 3 mm thick aluminum plate in the middle of two transducers. The same transducer was used in [27] for ranging, proximity measurement and robotic sensing.

Nicolas Sénégond, Dominique Certon et al. characterized a CMUT with a rarely used method called Digital Holography Microscopy [8]. They provided characterization results for static deflection and roughness tests. Author state that this method provides one of the best tools for statistical evaluation of CMUT.

Andrew Logan et al. fabricated an immersion application CMUT fabricated with wafer bonding process and characterized it by using atomic force microscope for surface characterization and a commercial hydrophone for dynamic characterization [28].

1.6 Thesis Organization

Chapter 1 starts with the introduction, and summarizes the available literature on CMUT characterization and state-of-art in characterization process. This chapter builds the necessary background for the rest of the thesis.

Chapter 2 presents the method to design CMUTs analytically with Matlab™ and using Intellisuite™ FEA tool.

Chapter 3 presents the method of designing a capacitive readout circuit using based on transimpedance amplifier topology including noise calculations. Important topics like noise figure and printed circuit board are included in this chapter.

Chapter 4 includes the fabrication details and processes that is chosen to fabricate the CMUT. Specifications of the SOI wafer used are given in this chapter. Validation of the fabrication follows the explanation of the fabrication steps.

Chapter 5 of this thesis shows the results of static characterization part of the project. Essential parameters like capacitance, residual stress, stiffness constant, center deflection and pull-in voltage are measured and compared with the theoretical results.

Chapter 6 presents the dynamic characterization results. Simulated and measured parameters are resonant frequency, transient response, steady state response, fractional bandwidth, and specific bandwidth response of CMUT.

Chapter 7 deals with the characterization of readout circuitry which is necessary for the receive operation of the CMUT. Design of a transimpedance amplifier is presented in this chapter. Also, simulation of receive mode and pitch catch mode is presented

Finally chapter 8 draws up the conclusions and future directions.

Chapter 2

CMUT DESIGN

This chapter described the design methodology adopted to design the capacitive micromachined ultrasound transducers (CMUT) and a transimpedance amplifier based readout circuit. Mathematical models used for designing CMUTs are presented in detail for square membranes. Analytical results are then verified with Intellisuite™ FEA. Readout circuit is an essential part of CMUT system. It translates the capacitive change of the CMUT to the electrical signal.

2.1 Design Methodology

The final application determines the key parameters of a CMUT such as operating frequency and operating voltage. For air coupled blind spot applications, the operating frequency should be kept as low as possible, without getting interfered by the natural ultrasound noise signals [29]. Capacitance change and deflection of the diaphragm at the operating point are also significant factors to determine the device geometry, operating voltage, and sensitivity. In the design process, initially an analog equivalent circuit model using lumped circuit elements is used to determine approximate behaviour of the CMUT considering geometry, materials, fabrication process, etc. The developed geometry is then analyzed using 3-D electromechanical FEA and modified to optimize the device performance in the target design space. The optimized geometry is then fabricated and characterized to verify the design parameters.

2.2 Center Deflection of CMUT Diaphragm

The diaphragm center deflection determines the maximum change in capacitance for any bias voltage and electrical or ultrasonic load. For this analysis, the diaphragm is

considered to be homogenous and isotropic with perfect edge conditions. It is also assumed that the clamped edges hold the diaphragm rigidly against any out-of-plane rotation or displacement at the edges but allow displacement parallel to the diaphragm plane. At the edges, out-of-plane displacement is zero and the tangent plane to the displacement surface along the edge coincides with the initial position of the middle plane of the diaphragm. The boundary conditions imposed by the clamped edges can be expressed mathematically as [30-34]:

$$\left.\begin{array}{l} w(x=\pm a, \forall y)=0 \\ w(y=\pm a, \forall x)=0 \\ \dfrac{dw}{dx}(x=\pm a, \forall y)=0 \\ \dfrac{dw}{dy}(y=\pm a, \forall x)=0 \end{array}\right\} \tag{2.1}$$

During the receive mode operation, the diaphragm experiences two pressure loads: an electrostatic pressure between the backplate and the diaphragm due to the bias voltage and the external mechanical pressure due to the incident acoustical waves. Following the variational method, the combined load deflection model of a clamped single material square diaphragm subject to large deflection due to both electrical and mechanical pressures can be expressed as [35]:

$$\begin{aligned} &\left[C_{\mathrm{s}} f_{\mathrm{s}}(\nu)\frac{\tilde{E}h}{a^4}\right]w_0^3 + \left[\begin{array}{l} C_{\mathrm{r}}\dfrac{\sigma_0 h}{a^2} + C_{\mathrm{b}}\dfrac{12D}{a^4} \\ -\dfrac{\varepsilon_0 V^2}{2a}\left(\dfrac{4a}{d_{eff}^3} + 0.394\dfrac{a^{0.25}}{d_{eff}^{2.25}}\right) \end{array}\right] w_0 \\ &\qquad - \left[P_{\mathrm{Ext}} + \frac{\varepsilon_0 V^2}{2a}\left(\frac{2a}{d_{eff}^2} + 0.315\frac{a^{0..25}}{d_{eff}^{1.25}}\right)\right] = 0 \end{aligned} \tag{2.2}$$

where w_0 is the diaphragm center deflection, σ_0 is the residual stress, ε_0 is the permittivity of free space, V is the bias voltage, D is the flexural rigidity, P_{Ext} is the external mechanical pressure, and ν is the Poisson ratio of the diaphragm material. In (2.2), the term within the first square bracket represents diaphragm stiffness due to nonlinear spring hardening, the first term within the second square bracket represents the stiffness due to the residual stress; the second term within the second square bracket represents the stiffness due to bending, and the third term within the second square bracket represents the spring softening due to the nonlinearity of the electrostatic force. Moreover, in (2.2) the electrostatic pressure due to the fringing field capacitance is neglected as its contribution is negligible compared to the total pressure load. The constants C_r, C_b, and C_s are determined by adjusting the analytical solution with the numerical results for a specific design space and following [36] their values for typical thin diaphragms are:

$$\left.\begin{aligned} C_r &= 3.45, \\ C_b &= 4.06, \text{and} \\ \mathrm{C_s} &= 1.994. \end{aligned}\right\} \tag{2.3}$$

The Poisson ratio dependent function $f_s(\nu)$ in (2.2) is given by [36]:

$$f_s(\nu) = \frac{1 - 0.271\nu}{1 - \nu} \tag{2.4}$$

Equation (2.2) can be modified to determine the load-deflection characteristics of a multilayered diaphragm as shown in Figure 2.1 by replacing the flexural rigidity D with the effective flexural rigidity D_{eff} and the airgap d_0 with the effective airgap d_{eff}.

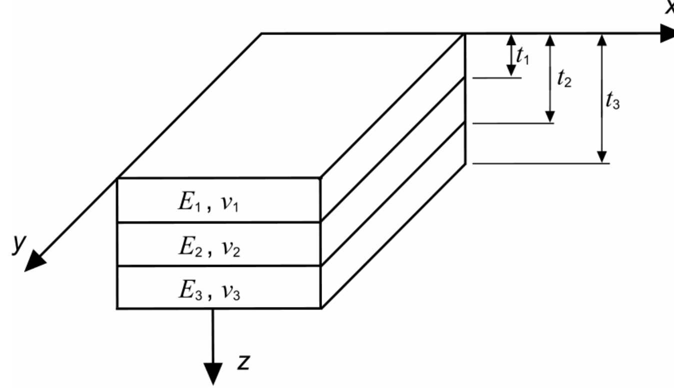


Figure 2.1. A section of a multilayer laminated plate [38].

Following Figure 2.1, the effective flexural rigidity D_{eff} is expressed as:

$$D_{eff} = \frac{AC - B^2}{A} \tag{2.5}$$

where the constants *A, B* and *C* are expressed as:

$$A = \sum_k Q_k (t_k - t_{k-1}), \tag{2.6}$$

$$B = \sum_k Q_k (\frac{t^2{}_k - t^2{}_{k-1}}{2}), \tag{2.7}$$

$$C = \sum_k Q_k (\frac{t^3{}_k - t^3{}_{k-1}}{3}), \tag{2.8}$$

and

$$Q_k = \frac{E_k}{1 - v^2{}_k} \tag{2.9}$$

where E_k and v_k are the Young's modulus and the Poisson's ratio of the kth layer respectively. In (2.2), the effective Young's modulus $\tilde{E}$ is the plate modulus and is expressed as:

$$\tilde{E} = \frac{E}{1-\nu^2} \quad (2.10)$$

where E is the Young's modulus of the diaphragm material. As the thickness of the top conducting layer is much lower compared to the thickness of the structural diaphragm material, considering only the Young's modulus, Poisson ratio, and the residual stress of the main structural layer to determine the nonlinear stiffness associated with the spring hardening and the stiffness due to the residual stress in (2.2) would not introduce any significant error.

The effective airgap d_{eff} is defined as:

$$d_{eff} = \frac{d_m}{\varepsilon_{rm}} + \frac{d_i}{\varepsilon_{ri}} + d_o \quad (2.11)$$

where, d_m is the membrane thickness, d_i is top electrode thickness, ε_{rm} is dielectric constant of the membrane, ε_{ri} is dielectric constant of the top electrode and d_o is air gap distance between diaphragm and backplate.

The real root of the 3rd order polynomial (2.2) represents the center deflection of the diaphragm subject to both electrostatic and external pressure. Two other roots are imaginary and have no practical significance.

As the diaphragm lies in the *x-y* plane, the parallel plate capacitance between the deformed diaphragm and the backplate can be calculated following [37]:

$$C_{\text{Deform}} = \varepsilon_0 \iint_A \frac{dxdy}{d_{eff} - w(x, y)} \quad (2.12)$$

In (2.12) $w(x,y)$ represents the deflection surface of the deformed diaphragm also known as the deflection shape function.

2.2.1 Deflection Shape Function

Following [38], the deflection profile of a multilayered diaphragm as used in typical CMUTs can be determined from:

$$w = w_0 \left(1 - \frac{x^2}{a^2}\right)^2 \left(1 - \frac{y^2}{a^2}\right)^2 \sum_{n=0,1,2}^{N} c_n \left(\frac{x^2 + y^2}{a^2}\right)^n \tag{2.13}$$

where w_0 is the diaphragm center deflection determined using (2.2) and the coefficients c_n are adjustable parameters to be determined from FEA simulation results for any particular design space. For typical CMUT design space (diaphragm thickness range of 0.5-3 μm and sidelength range of 200-1000 μm), investigation shows that three terms ($N = 2$) in (2.13) are necessary for large deflection cases while only two terms ($N = 1$) are necessary for small deflection cases to achieve a high degree of accuracy. For the specified design space, the parameters c_0, c_1, and c_2 are determined as:

$$\left.\begin{aligned} c_0 &= 1 \\ c_1 &= \frac{0.0011}{\sqrt{h}} \\ c_2 &= \frac{0.0005}{\sqrt{h}} \end{aligned}\right\} \tag{2.14}$$

by comparing the results from (2.13) with 3-D FEA using IntelliSuite™.

2.3 Capacitance

Commonly used parallel plate capacitance model in (2.12) does not take account of the fringing field effects that is associated with the electric flux lines originating from

diaphragm sides and charge concentration at the diaphragm edges. Though an accurate value of the fringing field capacitance can only be obtained by solving Poisson's equation using a 3-D field solver, a highly accurate value of the fringing field capacitance can be calculated by modifying a VLSI on-chip interconnect capacitance model presented in [35].

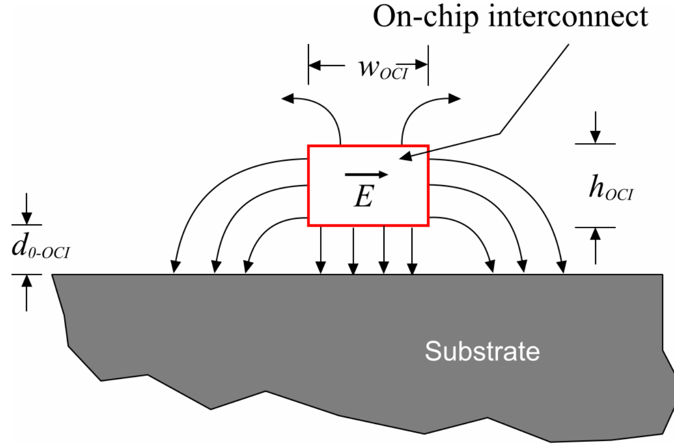


Figure 2.2. Cross- sectional view of a VLSI on-chip interconnect separated from a fixed ground plane by a dielectric medium [38].

Following [35], the per unit length capacitance of a VLSI on-chip interconnect of width w_{OCI} and thickness h_{OCI}, separated from the substrate by a dielectric medium of thickness d_{0-OCI} and relative dielectric constant ε_r, as shown in Figure 2.2 can be expressed as:

$$C_{OCI} = \varepsilon_0 \varepsilon_r \left[\left(\frac{w_{OCI}}{d_{0-OCI}} \right) + 0.77 + 1.06 \left(\frac{w_{OCI}}{d_{0-OCI}} \right)^{0.25} + 1.06 \left(\frac{h_{OCI}}{d_{0-OCI}} \right)^{0.5} \right] \tag{2.15}$$

It has been determined that the maximum deviation of (2.15) from the most accurate numerical method presented in [35] is only 2% when

$w_{OCI} / d_{0-OCI} \geq 1,\ 0.1 \leq \mathrm{h}_{\mathrm{OCI}}/d_{0-OCI} \leq 4$ and 6% as long as $w_{OCI} / d_{0-OCI} \geq 0.3,\ h_{OCI}/d_{0-OCI} \leq 10$ holds. An approximate value of the fringing field capacitance for a CMUT fabricated with a square diaphragm of sidelength $2a$ as shown in Figure 1.1 can be calculated by modifying (2.15) as:

$$C = \frac{4\varepsilon a^2}{d_{eff}} + 1.44\varepsilon a + 2.12\varepsilon a\left(\frac{2a}{d_{eff}}\right)^{0.25} + 2.12\varepsilon a\left(\frac{d_c}{d_{eff}}\right)^{0.5} \qquad (2.16)$$

The first term in (2.16) represents the parallel plate capacitance associated with the CMUT as shown in Figure 1.1. The second and third term together represent the fringing field capacitance due to the diaphragm sidelength $2a$ while the fourth term represents the fringing field capacitance due to the conductor thickness d_c. By rearranging (2.16), a functional form of total capacitance associated with a CMUT can be derived as:

$$C = C_0 (1 + C_{\mathrm{ff}}) \qquad (2.17)$$

where C_0 is the parallel plate capacitance expressed as

$$C_0 = \frac{\varepsilon_0 4a^2}{d_{eff}} \qquad (2.18)$$

and C_{ff} is the fringing field factor expressed as:

$$C_{\mathrm{ff}} = \frac{0.385}{a}\left[d_{eff}\right] + 1.06\left[\frac{1}{2a}\left\{d_{eff}\right\}\right]^{0.75} + \frac{0.53}{a}\left[d_c\left\{d_{eff}\right\}\right]^{0.5} \qquad (2.19)$$

The third term in (2.19) represents the fringing field capacitance due to the conductor thickness d_c and can be neglected as the flux lines originating from the conductor sides along the thickness will terminate beyond the coupling area of the device and will not contribute to the total capacitance.

After deformation, the total capacitance is also contributed by two factors: the parallel plate capacitance C_{Deform} between the deformed diaphragm and the backplate which can be calculated using (2.12), and the fringing field factor C_{ff}. Thus the total capacitance after deformation can be expressed as:

$$C = C_{\text{Deform}}(1 + C_{\text{ff}}) \tag{2.20}$$

As the diaphragm edges are rigidly fixed and don't undergo any deformation and as the fringing field capacitance is contributed mainly by the charges concentrated at the edges, the fringing field factor C_{ff} can be assumed to remain unchanged despite diaphragm deformation and **(2.19)** can be used to calculate C_{ff} as before.

2.4 CMUT Lumped Element Model

Lumped element modeling is used to reduce the complexity of CMUT modeling to a manageable level for rapid and efficient simulation. This includes modeling of all major sensor performance criteria such as, resonant frequency, damping effects, radiation resistance, sensitivity due to bias voltage, etc.

Sensitivity of the CMUT depends on size, thickness, stress of the diaphragm, airgap distance and the bias voltage. These parameters can be calculated following the analog electrical model of CMUT presented in [39]. The acoustic force is modeled as equivalent voltage source as seen in Figure 2.3. R_r represents radiative resistance and M_r

represents air mass. M_m is diaphragm mechanical mass and its compliance is C_m. the air gap and movable plate vent losses are represented by resistances R_g and R_h, and the air gap compliance is C_a.

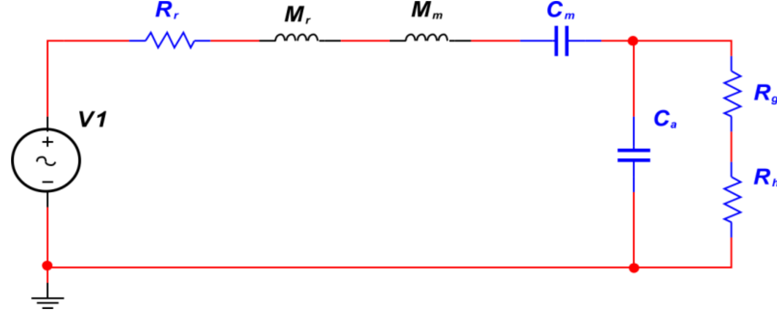


Figure 2.3. Equivalent circuit model of CMUT.

The acoustic impedance of the air in contact with the vibrating diaphragm is represented by radiative resistance R_r and air mass M_r.

$$R_r = \frac{\rho_0 a^4 \omega^4}{2\pi c} \tag{2.21}$$

$$M_r = \frac{8\rho_0 a^3}{3\pi\sqrt{\pi}} \tag{2.22}$$

where ρ_0 is the air density, c is the sound velocity, and ω is the angular vibration frequency. The diaphragm compliance is equal to the average diaphragm deflection divided by the applied force. It is estimated from the energy method:

$$C_m = \frac{32a^2}{\pi^6\left(2\pi^2 D_{eff} + a^2 T\right)} \tag{2.23}$$

where D_{eff} is the effective flexural rigidity and T is tensile force per unit length which is calculated as:

$$T = t_d \sigma \tag{2.24}$$

where σ is the residual stress of the diaphragm.

The equivalent mass element M_m is derived from kinetic energy of the square diaphragm under the uniform loading.

$$M_m = \frac{\pi^4 \rho \left(2\pi^2 D_{eff} + a^2 T\right)}{64T} \tag{2.25}$$

where ρ is mass per unit area of the diaphragm.

The viscosity loss in the air gap R_g and its compliance C_a are:

$$R_g = \frac{12ua^2}{nd^3\pi}\left(\frac{\alpha_{sf}}{2} - \frac{\alpha_{sf}^2}{8} - \frac{\ln(\alpha_{sf})}{4} - \frac{3}{8}\right) \tag{2.26}$$

$$C_a = \frac{d}{\rho_0 c^2 \alpha_{sf}^2 a^2} \tag{2.27}$$

where n is the hole density in the diaphragm and α_{sf} is the surface fraction occupied by the holes, u is the air viscosity coefficient, and d is the average air gap distance. Also viscosity loss of the diaphragm plate holes can be approximated as:

$$R_h \approx \frac{8uha^2}{\pi n r^4} \tag{2.28}$$

Equivalent impedance Z_t of the CMUT is expressed as:

$$Z_t = R_r + j\omega\left(M_r + M_m\right) + \frac{1}{j\omega C} + \frac{R_g + R_h}{1 + j\omega(R_g + R_h)C_a} \tag{2.29}$$

The total sensitivity S_t of the CMUT is defined as the output voltage V_o per unit of incident acoustical pressure P and can be expressed as [39]:

$$S_t = \frac{V_0}{P} = \frac{V_b a^2}{j\omega d Z_t} \tag{2.30}$$

where V_b is the bias voltage. Also, resonant frequency is estimated with [39]:

$$f_{res} = \sqrt{\frac{1}{\rho}\left(\frac{D_{eff}\pi^2}{a^4} + \frac{T}{2a^2}\right)} \tag{2.31}$$

2.5 Stiffness and Residual Stress

Stiffness and residual stress are key parameters for both static and dynamic analysis of the CMUT displacement. Stiffness is calculated from the relationship between the mass and resonant frequency. After measuring the resonant frequency, then the stiffness parameter is extracted then from the known relationship between mass and resonant frequency which is;

$$w_0 = \sqrt{\frac{k}{m}} \tag{2.32}$$

From the extracted stiffness, residual stress of the diaphragm is calculated using the equation from [40]:

$$k = C_r \frac{t_d \sigma}{a^2} + C_b \frac{12 D_{eff}}{a^4} \tag{2.33}$$

2.6 Pull-in Voltage

If the bias voltage exceeds certain limits, the electrostatic attraction force between the diaphragm and the backplate overcomes the elastic restoring force associated with the diaphragm and the diaphragm collapses on the backplate resulting in a device failure [37]. This voltage is known as the pull-in voltage. Determining the pull-in voltage is critical in the design process in order to determine the optimum DC operating point of the CMUT as increasing the DC bias voltage increases the sensitivity of the device. The pull-in voltage for a square diaphragm CMUT as shown in Figure 1.1 can be calculated following:

$$V_{pi} = \sqrt{\frac{\left(\frac{C_r \sigma h}{a^2} + \frac{C_b 12 D_{eff}}{a^4}\right) + \left(\frac{C_s f_s(v) \tilde{E} h}{a^4}\right)\frac{d_{eff}^3}{9}}{3\varepsilon_0\left(\frac{0.665}{d_{eff}^2} + \frac{0.2231 a^{-0.75}}{d_{eff}^{1.25}}\right)}} \tag{2.34}$$

2.7 Simulink Model for Dynamic Analysis

For Dynamic simulation, first order parallel plate capacitor model [41] and FEA methods are used. First order model is computationally efficient and reaches very good accuracy which is a derivation of the parallel plate actuator model represented in [37]. The model is built on Matlab/Simulink using building blocks as in Figure 2.4 and Figure. Fundamental equation of motion for an electrostatic parallel plate actuator can be modeled as:

$$m\ddot{x} + b\dot{x} + kx = -\frac{\varepsilon_0 A V_{dc} V_{ac}(t)}{g^2} \tag{2.35}$$

where A is area, ε_0 is permittivity of air, g is the air gap distance, m is mass, b is damping factor and k is the stiffness parameter.

Since (2.35) expresses position as a function of time, continuous iteration is necessary to solve the equation to determine the diaphragm position as a function of time. In (2.35) the stiffness parameter k is determined from material properties and geometric specifications of the diaphragm and the mass m can be calculated from the known volume and density of the diaphragm material. The damping factor b can be calculated following [37]:

$$b = \frac{mw_0}{Q} \tag{2.36}$$

where Q is the quality factor. As the mass m and the angular resonant frequency w_0 is known, then damping factor b can easily be calculated. A Simulink model as shown in Figure 2.4 then can be built to solve (2.35) to determine the dynamic response of the system.

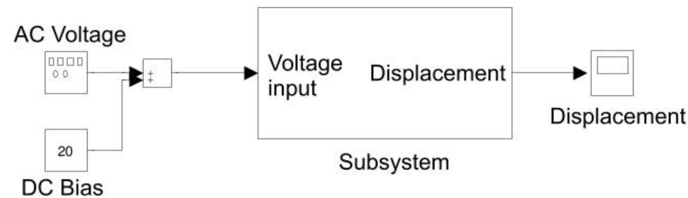


Figure 2.4. Simulink model of CMUT.

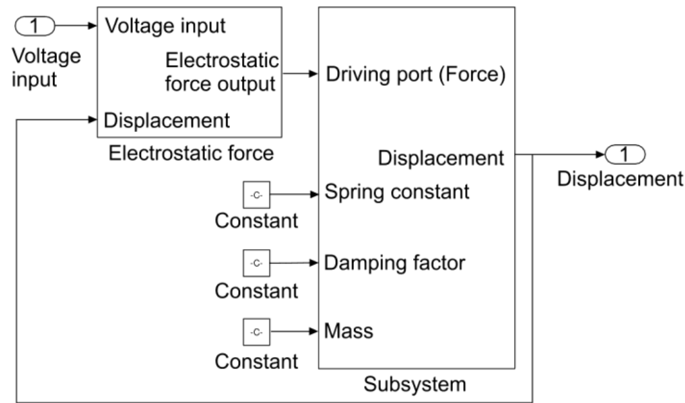


Figure 2.5. Simulink model of CMUT.

2.8 FEA Model for Dynamic Analysis

Intellisuite™ FEA package is used for dynamic analysis of the CMUT. In order to run a successful dynamic analysis, Rayleigh damping coefficients α (mass damping factor) and β (stiffness damping factor) are determined from [42]:

$$\xi_i = \frac{\alpha}{2\omega_i} + \frac{\beta\omega_i}{2} \tag{2.37}$$

The associated quality factor is expressed as:

$$\xi_i = \frac{1}{2Q_i} \tag{2.38}$$

Once a set of Q_i are determined (Table 2.4) from a frequency analysis with resonant modes (Table 2.2), respective damping factors ξ_i can be determined from (2.38). The values of ξ_i along with ω_i are then inserted in (2.37) and solved simultaneously to obtain α and β. Then, these values are inserted into the damping settings of the simulation as in Figure 2.6. As the system is nonlinear, a direct integration

method with squeezed film damping has been chosen to carry out the transient analysis using FEA with IntelliSuite™.

2.9 Final Design Specifications

Following the mathematical models and design methodology presented above, a CMUT has been designed and analytically analyzed. Final design specifications of the CMUT are summarized in Table 2.1.

Table 2.1. Final CMUT Design Specifications

Parameter	Value	Unit
Operating Frequency Range	113-167	kHz
Operating Voltage	20	V_{DC}
Resonant Frequency	614	kHz
Pull-in voltage	110	V_{DC}
Airgap	1	µm
Diaphragm thickness	2	µm
Diaphragm Sidelength	225	µm
Number of CMUTs in an Array	6x6	-
Array Sidelength	1.8	mm
Vent Hole Dimension	15x15	µm
Number of Vent Holes	5x5	-

For FEA simulation of the transient response, a large displacement option with 10 iterations and an increment number of 70 has been used as shown in Figure 2.7. For steady state analysis, first six mode Rayleigh damping coefficients are calculated and fed into the simulation to reach the best accuracy. Respective ξ_i values are presented in Table 2.3.

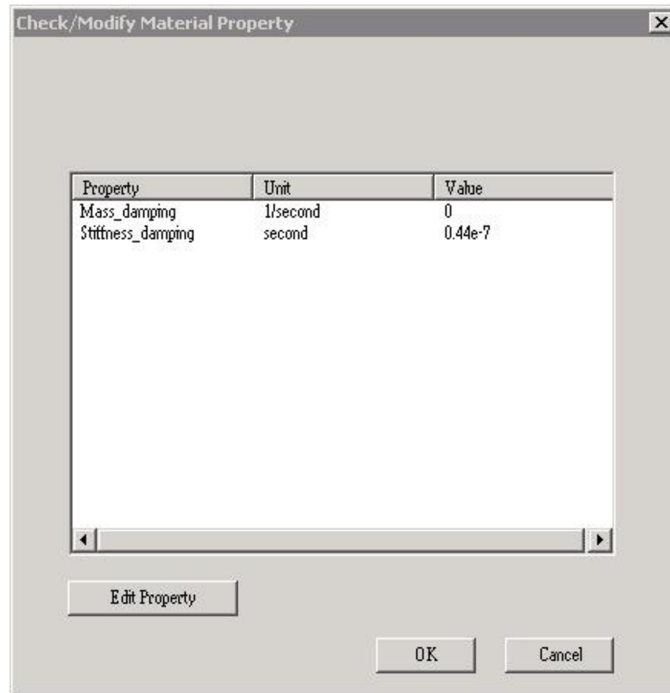


Figure 2.6. Material damping properties entry window.

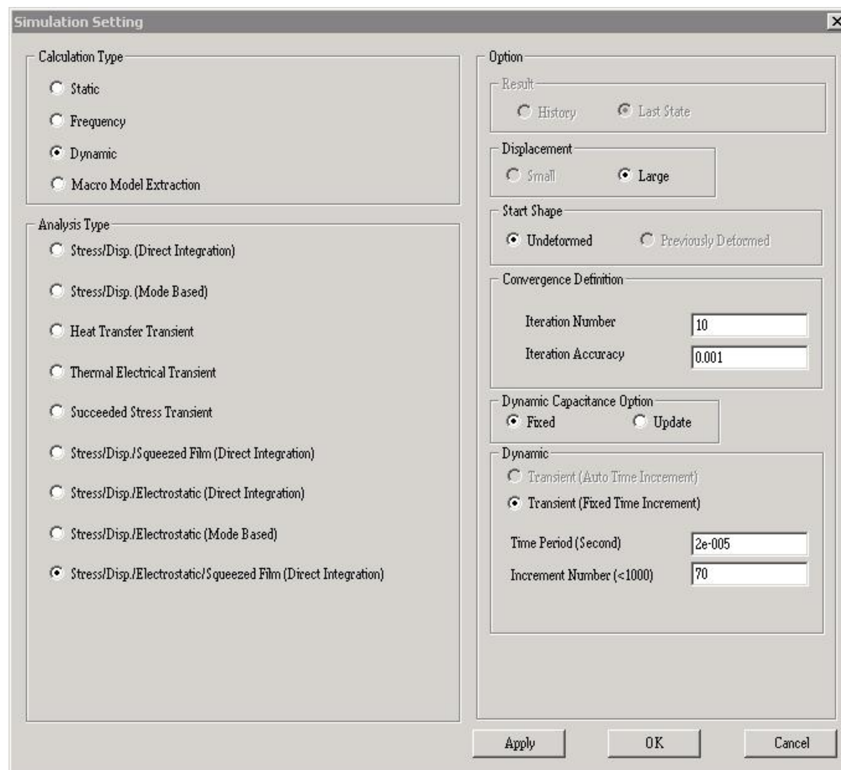


Figure 2.7. Dynamic analysis with FEA.

Table 2.2, Table 2.3, Table 2.4 represents mode frequency, mode damping ratio and mode quality factor values respectively.

Table 2.2. Frequency with Respect to Mode Number

Mode Number	Frequency (MHz)
1	0.614
2	1.3
3	1.35
4	2.048
5	2.49
6	2.5

Table 2.3. Damping Ratio with Respect to Mode Number

Mode Number	Damping Ratio (ξ_i)
1	0.086
2	0.1865
3	0.1865
4	0.282
5	0.344
6	0.345

Table 2.4. Quality Factor With Respect To Mode Number

Mode Number	Quality Factor (Q_i)
1	5.81
2	2.68
3	2.68
4	1.77
5	1.45
6	1.44

Chapter 3

READOUT CIRCUIT

This chapter presents the design and implementation of a readout circuit developed for use with the CMUT to generate a voltage signal in response to an ultrasound excitation which is an essential part of the CMUT system. Readout circuit translates the capacitive change of the CMUT due to an ultrasound excitation to a useful electrical signal. The basic theory of transimpedance amplifier is, when a CMUT's capacitance changes due to external ultrasound pressure, this change is capacitance will require charges to flow from DC bias supply. Due to transimpedance amplifier's feedback mechanism, this flowing current is forced to pass through a feedback resistor R_F, connected between the input and output ports of an operational amplifier (Figure 3.1), causing an output voltage from the transimpedance amplifier.

3.1 Design of a Transimpedance Amplifier

Basic operating principle of a transimpedance amplifier as shown in Figure 3.1 is that the current generated by the CMUT due to a change in capacitance flows through the RC network which is parallel to an operational amplifier to generate an equivalent voltage signal [43]. The ideal operational amplifier will not draw any current in the negative input, which translates into very high input impedance for the operational amplifier. The negative feedback mechanism of the high gain operational amplifier forces current to flow only through the feedback resistor and the capacitor. So the I to V (current to voltage) gain is simply defined as:

$$\text{I - V Gain} = \frac{V_o}{I_{in}} = \frac{-Z_f}{1+\left(\frac{1+Z_f / Z_{CMUT}}{A(s)}\right)} \tag{3.1}$$

where

$$Z_f = \frac{1}{sC_f} \parallel R_f \tag{3.2}$$

and V_o, I_{in}, Z_{CMUT} and *A(s)* are the output voltage, input current, complex impedance of the CMUT and the open loop gain of the operational amplifier respectively.

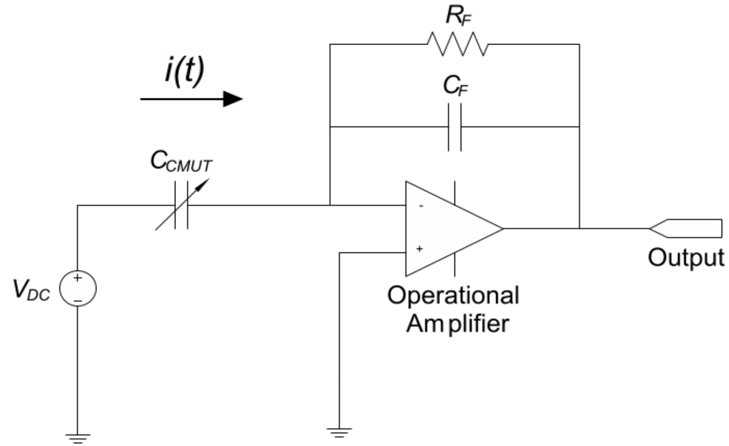


Figure 3.1. Transimpedance amplifier scheme.

Since transimpedance amplifier is a feedback amplifier structure, feedback factor *F* should be calculated, which is basically how much of the output is fed back to the input of the amplifier:

$$F = \frac{V_{in}}{V_{out}} = \frac{Z_{in}}{Z_{in} + Z_f} = \frac{\frac{1}{sC_{CMUT}}}{\frac{1}{sC_{CMUT}} + \frac{R_F}{1 + sC_F R_F}} \tag{3.3}$$

From knowledge of the feedback factor, the noise gain of the amplifier can be calculated following:

$$\text{Noise Gain} = \frac{1}{F} = 1 + \frac{Z_f}{Z_{in}} \tag{3.4}$$

It is necessary to design the transimpedance amplifier in such a way that the I-V gain doesn't have a peak caused by a zero introduced due to the capacitance of the CMUT. In order to overcome this zero, a feedback capacitor C_F is introduced in parallel to R_F simply because of stability issues. If the capacitance of the CMUT is large enough, and the amplifier is not compensated with a feedback capacitor, the overall system becomes prone to serious ringing and oscillation problems. The gain vs. frequency and phase vs. frequency plots of typical transimpedance amplifiers are shown in Figure 3.2 and Figure 3.3 respectively. The Matlab codes for the figures are presented in Appendix A. From the figures, it can be concluded that to design a stable transimpedance amplifier, noise gain curve should be flattened before it crosses the open loop gain line of the operational amplifier.

The CMUT capacitance introduces a zero to the system which is:

$$f_Z = \frac{1}{2\pi R_F C_{CMUT}} \tag{3.5}$$

The noise gain increases until it hits the open loop gain of the operational amplifier. If there is no pole-zero cancellation applied, the amplifier will oscillate. In order to prevent that, a feedback capacitor C_F is introduced to the system which will create a pole at f_p, which is:

$$f_p = \frac{1}{2\pi R_F C_F} \quad (3.6)$$

However, besides cancelling the zero, this pole also introduces a phase margin of 45º at f_P , stabilizing the circuit and prevent peaking in the I-V Gain graph. It is to be noted that 45º is a theoretical estimation and the actual phase margin (PM) does vary for different implementation. A comparison between Matlab simulated design parameters and Spice parameters are presented in Table 3.1.

Table 3.1. Matlab and Spice Comparison Table

	Opamp BW (MHz)	R_f (kΩ)	C_f (pF)	C_s (pF)	f_{-3db} (kHz)	Phase Margin (°)
Spice	14 MHz	75	4.7	65	675	55
Matlab	14 MHz	75	4.7	65	63 6% Deviation	58 5.1% Deviation

Where

- GBW is the Gain Bandwidth product of the operational amplifier
- R_f is the feedback resistor on the feedback loop of the operational amplifier.
- C_f is the feedback capacitor on the feedback loop of the operational amplifier, which is used for stability of the transimpedance amplifier topology.
- C_s is the CMUT capacitance.
- f_{-3db} is the cutoff frequency of the transimpedance amplifier.
- Phase margin is the phase difference between input and output signals in a feedback amplifier.

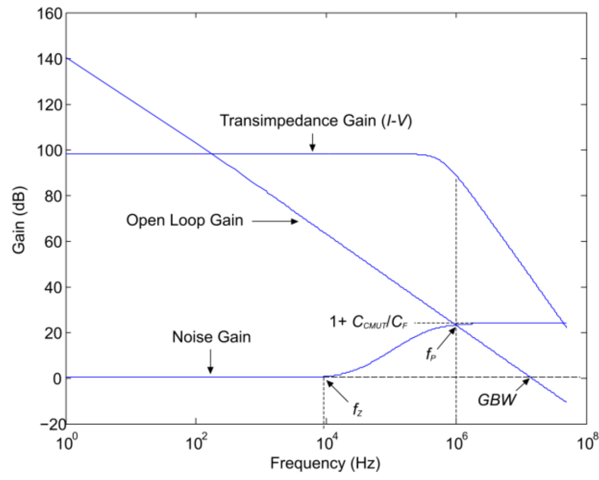


Figure 3.2. Design graph of the transimpedance amplifier.

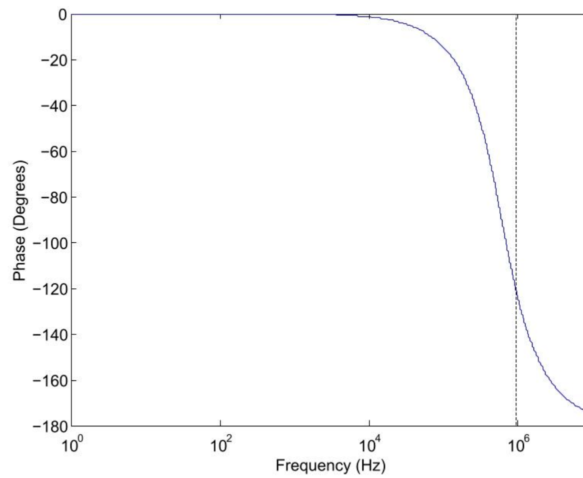


Figure 3.3. Phase graph of the circuit.

3.2 Noise

Noise of the transimpedance amplifier can be derived from the circuit in Figure 3.4. In Figure 3.5, noise regions of the system are clearly indicated. The first noise region f_1 is a result of the zero introduced by the input sensor capacitance, and is represented as:

$$f_1 = \frac{1}{2\pi(R_S \parallel R_F)(C_{in})} \quad \textbf{(3.7)}$$

where $C_{in} = C_S + C_C + C_{AMP}$, C_C is cable capacitance and C_{AMP} is amplifier input capacitance.

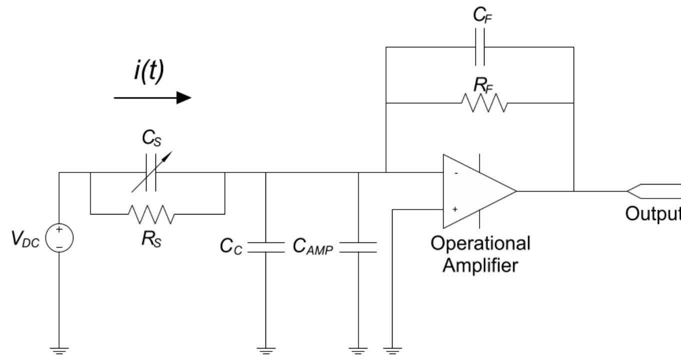


Figure 3.4. Transimpedance amplifier.

Second noise region f_2 is a pole introduced by inserting the feedback capacitor, in order to stabilize the transimpedance amplifier, and is expressed as:

$$f_2 = \frac{1}{2\pi(R_S \parallel R_F)(C_F)} \quad (3.8)$$

Operational amplifiers open loop gain frequency, f_{AOL} is estimated as:

$$f_{AOL} = \sqrt{\frac{f_u}{2\pi R_F C_{in}}} \quad (3.9)$$

F_{AOL} represents the intersection of the noise gain and open loop bandwidth where f_u is the gain bandwidth product which indicates the bandwidth of the operational amplifier. After defining the noise regions, RMS noise of the first region e_1 is calculated as:

$$e_1 = \left(1 + \frac{R_F}{R_S}\right) * B * \sqrt{\ln\left(\frac{f_b}{f_a}\right)} \tag{3.10}$$

where B is operational amplifiers input noise density at 1 Hz and f_a=1 Hz

Second and other noise regions are calculated as multiplying the area under the closed loop gain and amplifier noise density curves. Second region's RMS noise e_2 is calculated following:

$$e_2 = \left(1 + \frac{R_F}{R_S}\right) * e_n * \sqrt{f_1 - f_b} \tag{3.11}$$

where f_b is $1/f$ noise corner frequency. Third, fourth and fifth noise region noise values are calculated as:

$$e_3 = \left(1 + \frac{R_F}{R_S}\right) * e_n * \left(\frac{1}{f_1}\right)\sqrt{\frac{f_2^{\,3}}{3} - \frac{f_1^{\,3}}{3}} \tag{3.12}$$

$$e_4 = \left(1 + \frac{C_{in}}{C_F}\right) * e_n * \sqrt{f_{AOL} - f_2} \tag{3.13}$$

$$e_5 = \left(1 + \frac{C_{in}}{C_F}\right) * e_n * \sqrt{\frac{\pi}{2}\left(f_u - f_{AOL}\right)} \tag{3.14}$$

The feedback resistor R_F contributes to total noise of the amplifier, which is calculated as:

$$e_R = \sqrt{4KTR_F BW} \tag{3.15}$$

Finally the total RMS noise of the transimpedance amplifier is represented following:

$$V_{OUT(NOISE_RMS)} = \sqrt{e_1^{\ 2} + e_2^{\ 2} + e_3^{\ 2} + e_4^{\ 2} + e_5^{\ 2} + e_R^{\ 2}} \qquad (3.16)$$

RMS noise calculation is carried out using the values represented in Table 3.2.

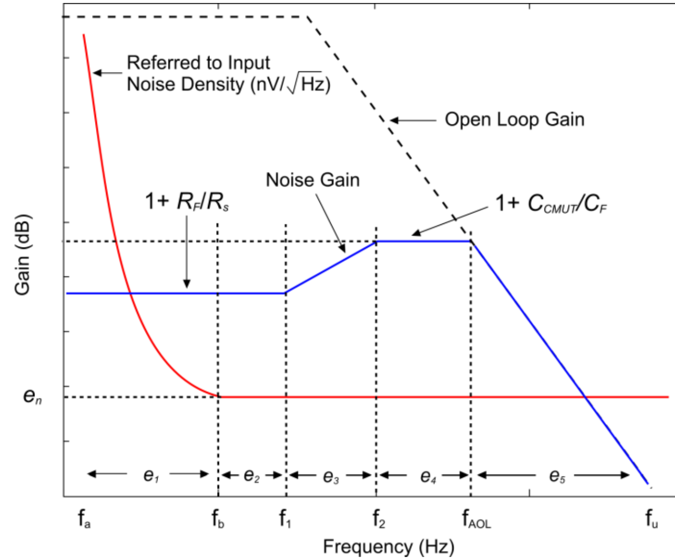


Figure 3.5. Noise calculation graph of transimpedance amplifier.

Table 3.2. Transimpedance Circuit Component Values

Component	Value	Unit
Operational amplifier bandwidth (LT1122)	14	MHz
Feedback resistor R_F	75	kΩ
Feedback capacitor C_F	4.7	pF
Cable capacitance C_c	2	pF
Operational amplifier input capacitance C_{AMP}	4	pF

3.3 Printed Circuit Board

Printed circuit board (PCB) is necessary in order to create a robust amplifier circuit. The PCB is fabricated in Electrical and Computer Engineering Department Technician's office, with TTECH PCB Prototyping Machine. The design files are

generated in EAGLE PCB Design software, then translated into universal Gerber files and fed into the PCB Prototyping machine. Fabricated PCB is presented in Figure 3.6.

Figure 3.6. Fabricated PCB.

In the design of the PCB, ground plane is used in order to reduce noise. The CMUT is connected to the circuit with a BNC cable, in order to increase flexibility of the overall system. The layout of the PCB can be seen in Figure 3.7. Amplifier circuit requires +5V, -5V and V_{bias} voltages.

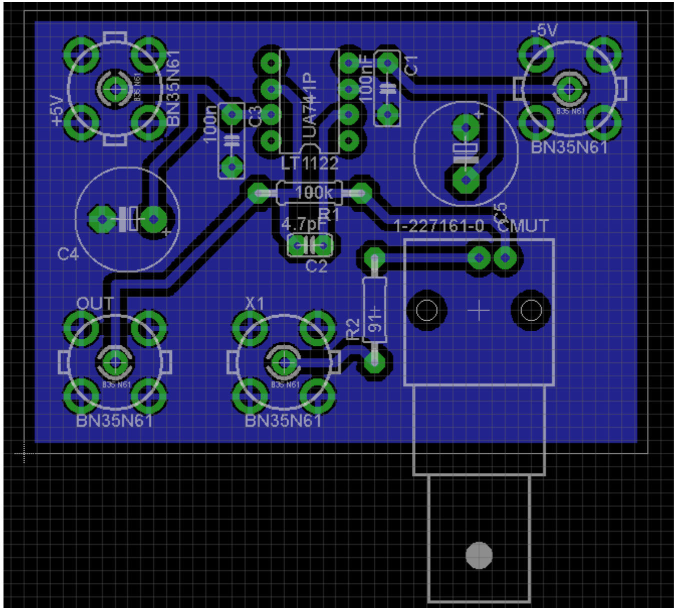


Figure 3.7. **PCB design file.**

Chapter 4

FABRICATION

This chapter presents a step by step description of the process sequence followed to fabricate the CMUTs on silicon on insulator (SOI) wafers using a single mask. Scanning electron microscopy (SEM) has later been used for geometrical verification of the fabrication process. The details of each fabrication step is provided with operating conditions, used materials, process type and a conceptual cross sectional view has been provided.

4.1 SOI Wafers

CMUTs are typically fabricated using the surface micromachining technique or using a SOI wafer. In the surface micromachining technique, a CMUT is fabricated with a silicon nitride or polysilicon structural diaphragm coated with a thin layer of conducting material such as gold or aluminum on the top. The air cavity is realized by sacrificial etching of a low temperature deposited silicon dioxide layer on the top of a passivated silicon wafer. On the other hand, the SOI wafers come with a buried oxide layer (BOX) sandwiched between a single crystal device layer and a handle layer as shown in Figure 4.1.

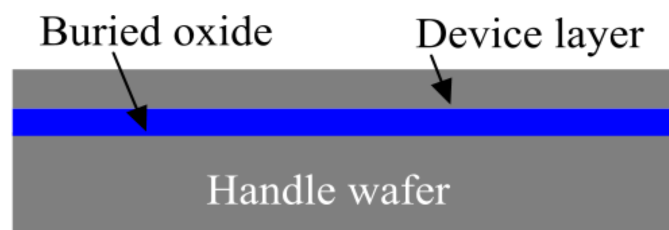


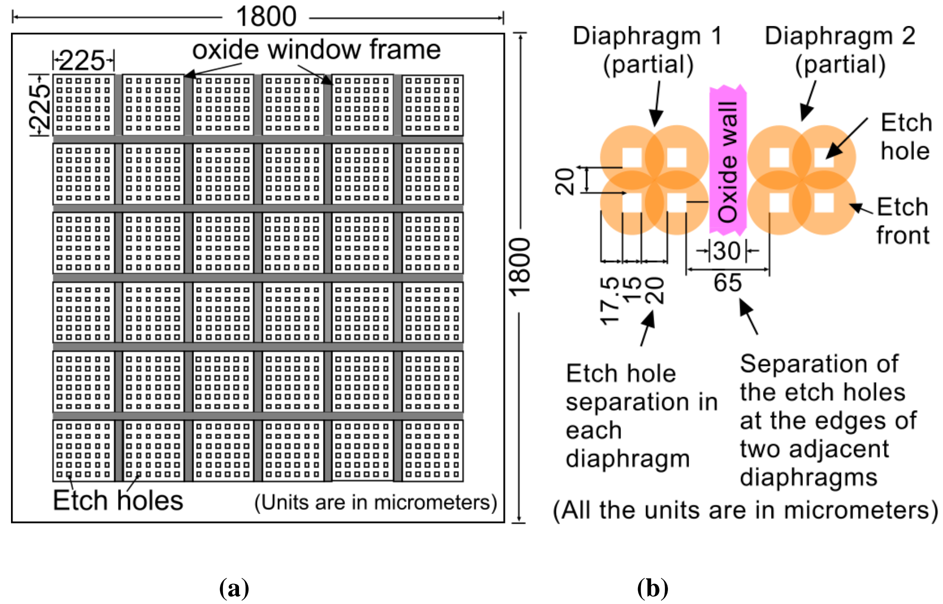
Figure 4.1. Cross section of a SOI wafer.

Small holes are created in the device layer to facilitate entry of the silicon oxide etchant such as buffered oxide etch (BOE) to dissolve the oxide layer to create the cavity. The overall process is simpler than the surface micromachining technique. Additionally, the SOI wafers offer superior electrical and mechanical qualities such as: 1) higher switching speeds [44], 2) higher quality factor, 3) lower residual stress, and 4) better thickness uniformity when compared to other diaphragm material like Si_3N_4 and Polysilicon. Based on these considerations, an SOI based fabrication process has been selected to fabricate the CMUTs.

4.2 Mask Preparation

Only a single mask is necessary to fabricate the CMUTs on an SOI wafer. CMUTs are designed to be fabricated as a 6 x 6 planar array separated by a thin strip of silicon dioxide as shown in Figure 4.2a. Each of the CMUTs in the planar array has a sidelength of 225 μm, a diaphragm thickness of 2 μm, and an airgap of 1 μm as listed in table 2.1. The width of the SiO_2 window frame has decided to be 30 μm. A 150 μm wide strip is left in the planar array for gold wire bonding, dicing and handling purposes. Etch holes of 15 x 15 μm^2 with a spacing of 20 μm edge to edge has been incorporated in each of the CMUT diaphragms to release the sacrificial oxide layer underneath the diaphragms. These etch holes not only provide the route for etching of the buried oxide (SiO_2), but also help reducing the air damping during diaphragm deflection. The dimensions and spacing of the etch holes are determined from the etch rate of buffered oxide etch (BOE) and considering the isotropic etch characteristic of BOE. Figure 4.2b shows the details of the etch hole dimensions and their separation distances. The separation distances are calculated such that two circular BOE etch-fronts intersect in the

middle of the diagonal distance between two etch holes to ensure that the buried oxide layer is removed and the diaphragm is released properly at the farthest distance. Material properties and geometrical specifications of the SOI wafer used to fabricate the CMUTs are listed in Table 4.1.



(a) **(b)**

Figure 4.2. 6 x 6 planar array configuration.

Table 4.1. SOI Wafer Specifications

Parameter	Specification(s)
Diameter	150±0.2 mm
Crystal Orientation	<100>
Overall Thickness	352±5 µm
Front side finished	Polished
Back Side Finished	Nanogrind @2000mesh
Device Layer	
Thickness	2±0.5 µm
Type/Dopant	n/Sb
Resistivity	<0.2 Ohm-cm
Handle wafer	
Thickness	350±5 µm
Type/Dopant	n/Phos
Resistivity	<5 Ohm-cm
Buried Oxide	
Thermal Oxide	1±5% µm

4.3 Fabrication Steps

Step 1: RCA Clean

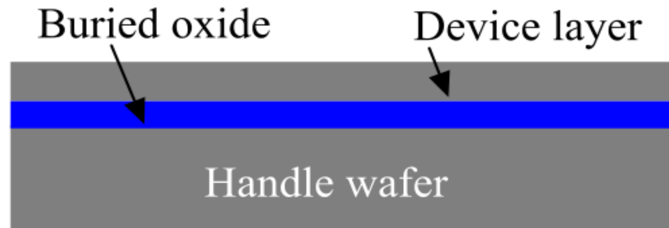


Figure 4.3. RCA clean.

Before the SOI wafers are subject to any microfabrication process, an RCA cleaning is necessary to clean all organic contaminants, oxide layers and heavy metal contamination that may build up on the wafer surface. In the RCA cleaning, the first step is removal of all organic coatings in a strong oxidant, such as a 7:3 mixture of concentrated sulphuric acid and hydrogen peroxide ("pirhana"). Then organic residues are removed in a 5:1:1 mixture of water, hydrogen peroxide, and ammonium hydroxide. As this step can grow a thin oxide on silicon, it is necessary to insert a dilute HF etch to remove this oxide when cleaning a bare silicon wafer. The HF dip is omitted when cleaning wafers that have intentional oxide on them. Finally, ionic contaminants are removed with a 6:1:1 mixture of water, hydrochloric acid, and hydrogen peroxide [37]. The RCA cleaned wafer cross section is shown in Figure 4.3.

Step 2: Metal Deposition (Chromium and Gold)

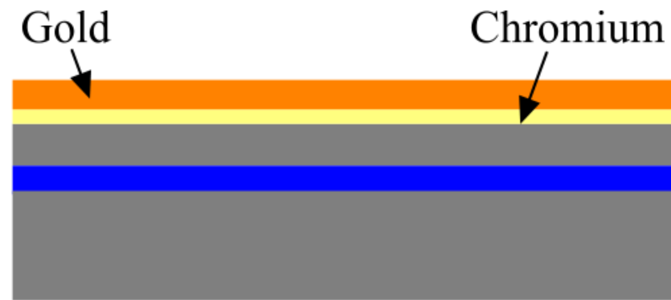


Figure 4.4. Metal deposition.

The second step includes deposition of Gold (Au) layer, which is the top electrode of the CMUT. Since gold cannot be deposited on Silicon, a 25 nm layer of Chromium is deposited as an adhesion layer. After that, 200 nm thick gold layer is deposited using electron-beam evaporation technique (Figure 4.4). The Chromium seed layer was deposited at 20% power to obtain a deposition rate of 3.0 Å/sec and Gold conductive layer was deposited at 30% power which gives a rate of 9.2 Å /sec. In order to avoid oxidation of Chromium, two deposition processes were done in one duty cycle.

Step 3: Photolitography

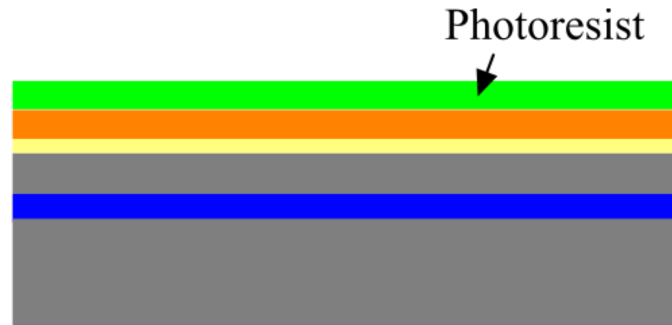


Figure 4.5. Photolitography.

After deposition of the electrode layer, pattern of etch holes must be developed. These etch holes provides a router for etching the buried oxide layer (SiO_2) as well as reducing the air damping during diaphragm deflection. For photolithography process, a 0.5 μm thick Shipley 1805 photoresist has been spin deposited using a thin HMDS layer as the primer (Figure 4.5). After soft baking of the photoresist layer, the wafer was exposed to UV light to carry out the photolithography and the final pattern was developed as seen in Figure 4.6.

Figure 4.6. Final pattern after photolitography.

Step 4: Metal (Gold and Chromium) and Silicon Etch

Figure 4.7. Metal and silicon etch.

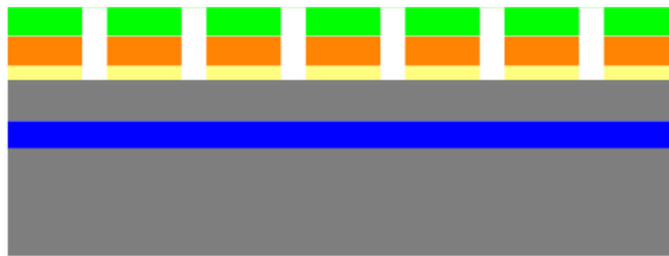


Figure 4.8. Chromium etching.

After patterning the device with photoresist, gold and chromium layers are etched in order to expose the silicon layer for further etching of the diaphragm. Gold layer was etched using Transene™ TFA solution (8% I, 21% KI, 71% H2O, etch rate 28 Å /sec) for 140 seconds (Figure 4.7). After etching the gold layer, RCA cleaning procedure is carried out. Then for etching of the Chromium layer, Transene™ 1020 is used for 12 seconds (10-20% Cericmonium Nitrate, 5-6% HNO3, etch rate 40 Å /sec) at 40 ^{0}C (Figure 4.8). The silicon layer is then DRIE (Deep reactive ion etch) etched in the next step, which is seen in Figure 4.9.

Figure 4.9. Silicon DRIE etch.

Step 5: Dicing and Photoresist Removal

After etching of silicon and devices are ready for release, it is important to get the individual dies separated. Dicing process is carried out before the photoresist removal, in order to protect the CMUT's diaphragm from heat, pressure and any failures due to dicing saw. After the dicing process, photoresist was stripped.

Step 6: Release and Critical CO_2 Drying

In order to release the diaphragm, Transene™ Improved BOE (4-8% HF + NH4F, etch rate~800A/min) has been used to sacrificially etch the oxide layer which is followed by critical point drying in a typical CPD dryer (Figure 4.10). Critical point drying is carried out to avoid stiction of the devices.

Figure 4.10. SiO_2 etch.

4.4 SEM Validation of Fabricated CMUT Geometry

After drying, the dies were inspected in SEM to check for proper diaphragm release. Figure 4.11 shows SEM image of one of the sensor diaphragms. Figure 4.12 shows the SEM image of one of the DRIE etched holes before oxide release and Figure 4.13 shows diaphragm after release.

Figure **4.14** shows the SEM measurement across the diagonal distance between two etch holes. From

Figure **4.14**, it is clear that the diagonal distance between two etch hole corners of 29.07 μm matches very closely with the mask value of 28.28 μm and the oxide layer has been completely etched in that region. The designed 17.5 μm lateral distance of an etch hole from the CMUT edge (Figure 4.2b) also matches very closely with SEM measured value of 18.03 μm as shown in Figure 4.15.

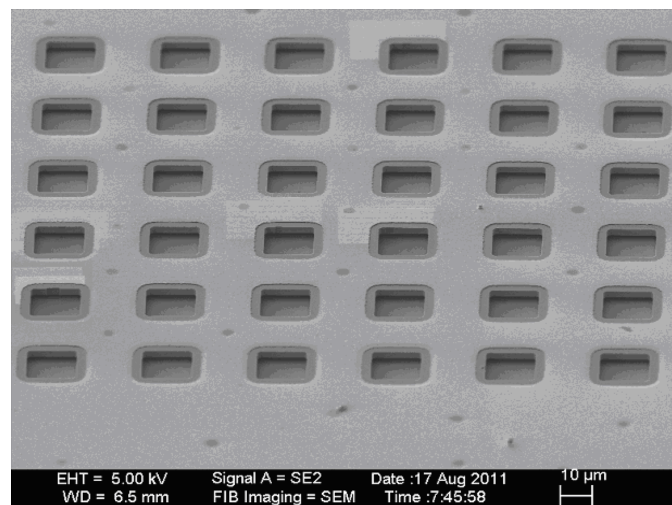


Figure 4.11. SEM image of a fabricated CMUT.

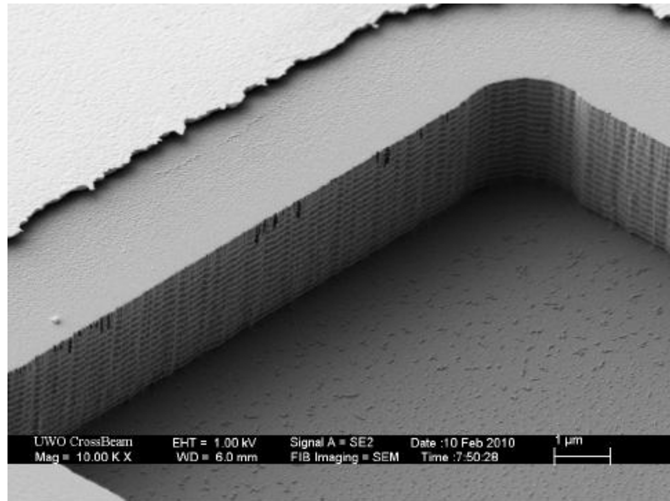


Figure 4.12. SEM image of an etch hole after DRIE of silicon.

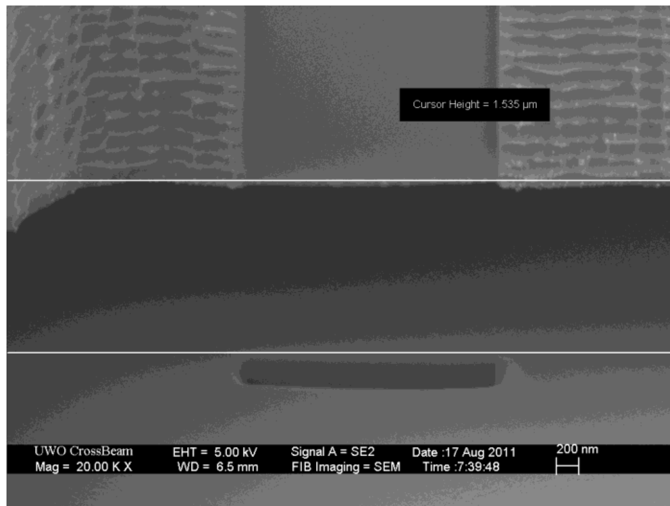


Figure 4.13. SEM image of a CMUT diaphragm after release.

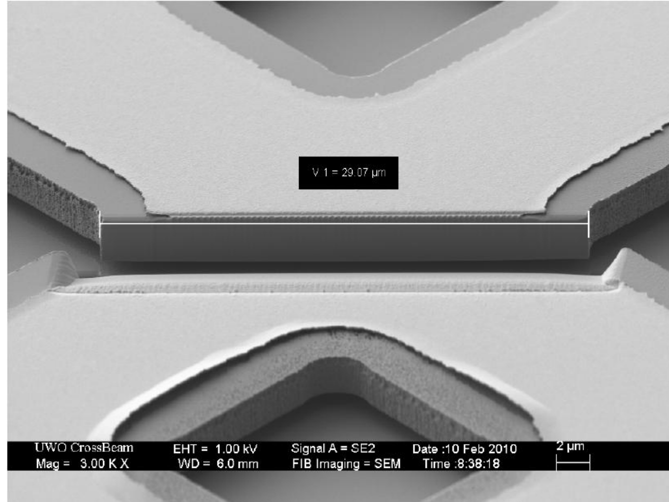


Figure 4.14. **SEM image after BOE showing the release of the SiO2 layer in the diagonal region between two etch holes.**

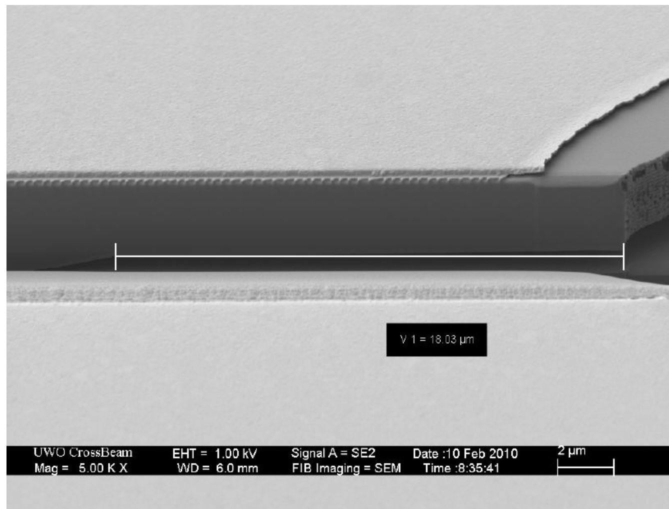


Figure 4.15. **SEM image of lateral etch distance at CMUT edge.**

These results conclude that the accuracy of the fabrication process is very good.

Chapter 5

STATIC CHARACTERIZATION

This chapter presents the detailed methodology of static characterization of the fabricated CMUTs. The methodology involves experimental measurement of key static device parameters and comparing them with analytical and FEA results to verify the design process. The key measured parameters are: diaphragm and airgap thicknesses, diaphragm static deflection, diaphragm stiffness, pull-in voltage, and static capacitance of the CMUT. Scanning electron microscope, Polytec laser Doppler vibrometer, LCR meter, and optical profilometer are used for measurements. Very good agreement has been found between the measured, calculated, and simulated values.

5.1 SEM and Optical Profilometer Analysis

As the microfabrication process is associated with some level of uncertainty in the thickness of the deposited layer and as the vendor supplied SOI wafers come with a certain percent variation in the thickness of the device layer and the oxide layer as listed in Table 4.1, it is necessary to measure the actual thickness of the diaphragm and the airgap for use in the simulation models to validate the design process. Any deviation in these values will cause discrepancy between simulation and experimental results. In order to achieve the most accurate results, SEM analysis is done at the University of Western Ontario Nanofabrication facility and the optical profilometer analysis is done at the Tribology lab at the University of Windsor.

An inspection of the results from the Wyko optical profilometer, it has been observed that the samples have an upwards warping in the center of about 500 nm a

shown in Figure 5.2. To verify this, another measurement of the same sample has been carried out using a scanning electron microscope. For the SEM analysis employing focused ion beam technology, two CMUTs are cut along a mid-point to mid-point cross-section in order to measure the dielectric layer thickness (before oxide etch), air gap distance (after oxide etch), and the diaphragm thickness.

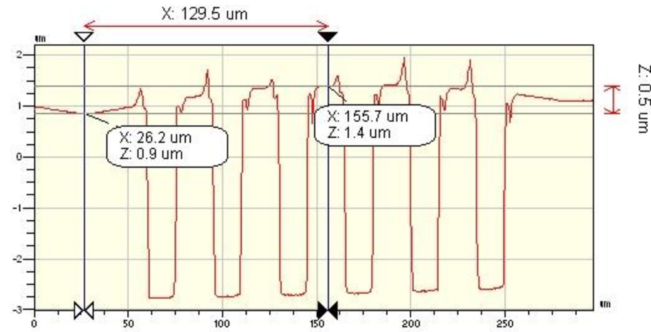


Figure 5.1. Wyko measurement of warping on CMUT diaphragm.

Figure 5.1 shows the SEM image of the CMUT before oxide release. The measurement shows that the thickness of the oxide layer is 997.6 nm and the thickness of the SOI device layer is 2.506 µm. Though the oxide layer thickness matches the designed airgap thickness, the actual diaphragm thickness is about 25% higher than the designed thickness of the diaphragm. However, this deviation matches with the vendor specification of 2±0.5 µm. Consequently, the whole analytical and FEA modeling was then carried out using the measured thickness of the diaphragm.

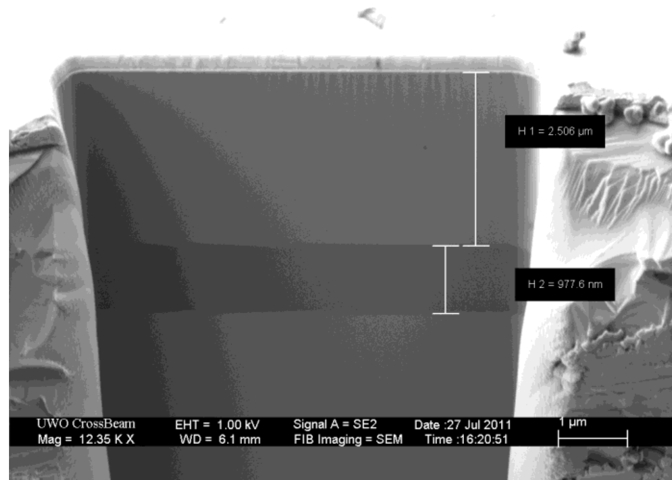


Figure 5.2. Dielectric and diaphragm layer thickness measurement with SEM.

Figure 5.3 shows the SEM measurement results of the CMUT after oxide etch. From the figure it is clear that the CMUT diaphragm indeed has an upward warping in the center of 535 nm. This warping can be attributed to the combined residual stress having its root in the mismatch of the coefficient of thermal expansion of silicon and gold after the underneath oxide was removed. A Comparison of the Wyko and the SEM results is provided in Table 5.1.

Table 5.1. Comparative Table Of Warping Measurement

Parameter	Wyko	SEM	Deviation from SEM (%Δ)
Air gap warping (nm)	500	512	2.3

In conclusion, Both SEM and Wyko measurements enabled to determine important device dimensions with nm precision. Wyko optical profilometer is found to be very accurate within 1.2% compared to SEM measurements. Optical profilometer is found to be easy to use, and results are obtained much faster than SEM. But exact

diaphragm thickness and dielectric layer thickness cannot be determined with this device. The measured dimensions are then used in subsequent comparisons.

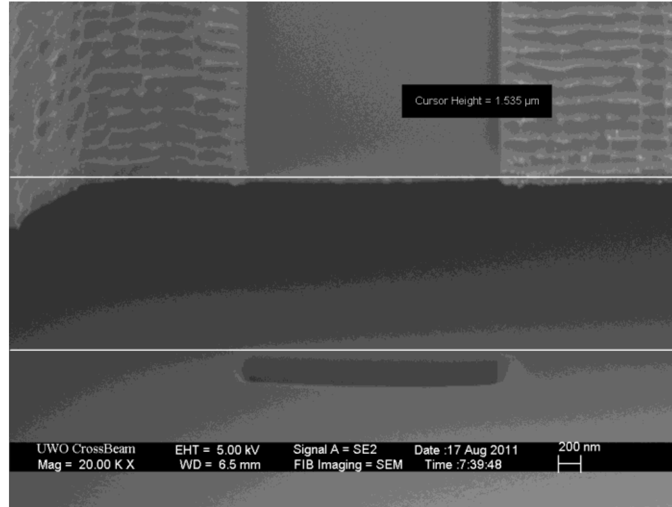


Figure 5.3. SEM air gap measurement from center of the diaphragm.

5.2 Capacitance

As the CMUT is basically a variable capacitor, static capacitance measurement (zero external pressure and zero bias voltage) is an important part of static characterization. Capacitance is calculated using equation (2.16) with a total tier area of 1.8 mm x 1.8 mm as shown in Figure 4.1a while excluding the coupling area associated with the 15 µm x 15 µm etch holes. The theoretical and experimental results are summarized in Table 5.2 without considering the warping effect and in table 5.3 with the warping effect.

Table 5.2. Comparison Of Theoretical And Experimental Capacitance

Calculated Capacitance (pF)	Experimental Capacitance (pF)	Percent Deviation (%Δ)
60.1	58.2	3

Following [45], the 535 nm warping of the diaphragm in the center can be averaged over the entire plate area to enable a parallel plate style capacitance calculation model. Following the prescribed method, the warping distance w_0 has been averaged by $w_0/3$ to evenly distribute the effect of warping over the entire diaphragm area and this average distance ($w_0/3$) has been added to the original airgap thickness to take account of the warping. As the effective airgap increases slightly, the warping effect reduces the capacitance slightly. Table 5.3 provides the comparison of measured capacitance with capacitance calculated considering the warping effect.

Table 5.3. Comparison Of Theoretical And Experimental Capacitance With Warping

Calculated Capacitance (pF)	Experimental Capacitance (pF)	Percent Deviation (%Δ)
58.6	58.2	0.7

5.3 Capacitance Change with Bias Voltage

The electrostatic attraction force between the diaphragm and the backplate will cause the diaphragm to deform. This will decrease the airgap and the capacitance between the diaphragm and the backplate will change.. An Agilent E4980A LCR meter is used to measure this change of capacitance as the bias voltage is increased or decreased. During the measurement, the DC bias voltage is swept from 0V to 20V (up sweep) and again from 0V to -20V (down sweep) using a 1V step size. The corresponding capacitance values are recorded using the LCR meter. Figure 5.4 shows the experimental capacitance values for both up and down sweep measurements as a function of bias voltage. For comparison purpose, the capacitance values are plotted as a function of the absolute values for the bias voltage.

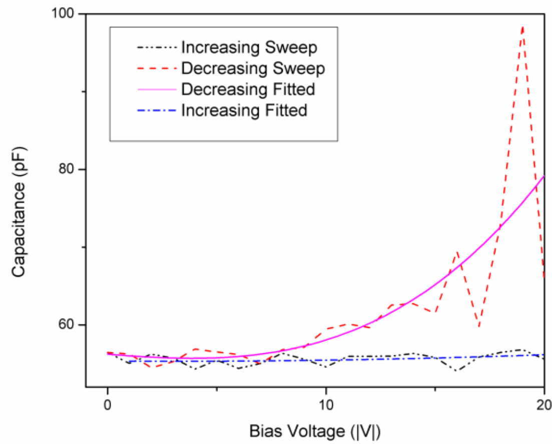


Figure 5.4. **Bias voltage vs capacitance.**

One important characteristic of the measurement results to be noticed in Figure 5.4 is that the capacitance change as a function of bias voltage (for both up sweep and down sweep operation) does not increase monotonously. Instead it fluctuates while maintaining an overall upward trend. Another interesting fact to be noticed in the graphs is that a higher slope of the data fitted curve for the down sweep operation. Figure 5.5 shows a comparison of FEA and analytical capacitance change results with the data fitted experimental capacitance values.

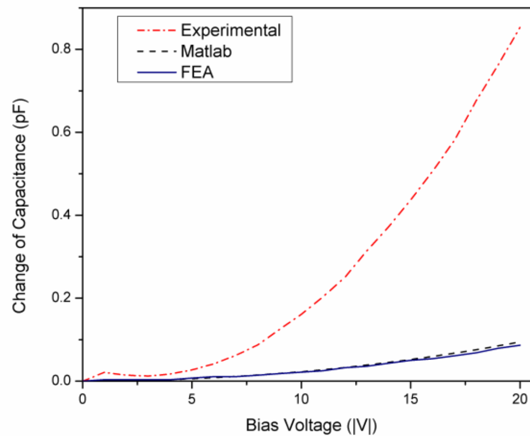


Figure 5.5. Capacitance change vs bias voltage.

From Figure 5.5, it is evident that analytical and FEA capacitance change values are in very good agreement; however, the measured capacitance change values are 4 to 10 times higher than the theoretical or FEA values.

Since similar data were obtained with multiple test runs, it can be concluded that some dielectric charging phenomena occurs in the CMUT as the bias voltage is increased or decreased to effect a fluctuation in the capacitance values. The actual physics of this dielectric charging is still under investigation and sufficient mathematical models are yet to be developed to capture the complex physical phenomenon that takes place when a dielectric material like silicon dioxide is exposed to a strong electric field. The breakdown voltage of silicon dioxide is 10^7 V/cm. At 1 V DC bias across the CMUT airgap of 1 μm results in an electric field of 10^4V/cm which is well below the breakdown voltage of silicon dioxide. At 20 V, the electric field is 20 x 10^5 V/cm. Thus, it can be concluded that no electrical breakdown has occurred even at 20 V_{DC} . Obvious question is what causes this higher capacitance change at higher bias voltage.

It is to be noted that although silicon dioxide exhibit excellent insulating properties, their lattice is formed by either covalent or ionic bonds, which affect significantly the dielectric polarization or charging. Temperature can also provide enough energy to the trapped charges to get released and for the dipoles to overcome potential barriers and randomize their orientation. In [46] it has been concluded that space charge polarization in silicon dioxide due to the presence of free charges or injected charges as well as the dipolar polarization constitutes the major charging mechanisms. The presence of nanoclusters or nanocrystals is expected to give rise to a random distribution of dipolar polarization and in the same time it is expected to give rise to interfacial polarization [46]. According to [47] as the electrostatic field gets stronger as the DC bias voltage increases causing a decrease in the airgap, excessive charges get trapped into the dielectric layer associated with the silicon dangling bonds. Also according to [46] low temperature deposition which is usually used in MEMS devices, leads to formation of silicon clusters, therefore causing leakage and charge trap interfaces.

For a fixed bias voltage and no mobile charges and charge traps, electrostatic force is assumed to be constant in time [48]. However, in the test scenario, DC voltage is swept and LCR meter uses a small AC signal in order to complete the measurements. Also leakage currents are detected in the CMUT device, which comes from the SiO_2 walls and between the electrodes. From the cross section of the CMUT in Figure 5.6, it can be seen that there exists a possible charge injection path from the top gold conductor to the bottom silicon backplate through the top silicon diaphragm and the oxide layer. In addition, a charge injection path may also be created from the top diaphragm to the

bottom electrode through the airgap to absorbed moisture particles because of the relative humidity [48].

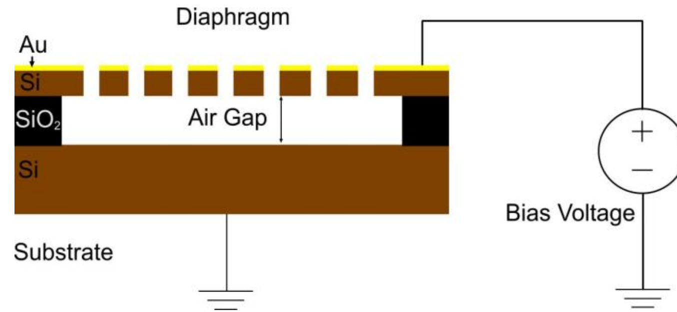


Figure 5.6. CMUT cross section.

Paschen defined breakdown voltage of parallel plates in air as a function of pressure and gap distance; however, it is not valid for air gaps less than 4 μm [49]. Corrected Paschen curve for narrow gaps in MEMS devices is presented in [49], and breakdown voltage in air for a 1 μm plate is about 60V. Comparing with high DC operating voltages of CMUT's, leakage through air is inevitable, and this effect contributes to leakage current and charge trapping. Since leakage currents cause i^2R heating, this effect also increases dielectric charging as mentioned above.

Due to combined effects of the different phenomena for dielectric charging, the net charge that contributes to the capacitance change will be different from the theoretical values. Consequently, the measured capacitance is ought to be different from the theoretical values. Additionally the amount of trapped charge or dipoles in a silicon dioxide film depends on the specific deposition technique. Without sufficient

mathematical models it is very difficult to analytically quantify the amount of dielectric charging and consequently the change in capacitance as a function of bias voltage.

5.4 Stiffness and Residual Stress of the Diaphragm

Following **(2.32)**, the diaphragm stiffness can be extracted from a measurement of the resonant frequency. The mass m of the diaphragm has been calculated from the known volume and density of silicon (2330 kg/m^3) as 3.68×10^{-10} kg. The resonant frequency of the CMUT has been measured using a Polytec™ laser Doppler vibrometer available in the University of Waterloo. The experimental set up and a picture of the test scenario is shown in Figure 5.7 and Figure 5.8. Using the relation **(2.32)**, the extracted stiffness parameter has been extracted as 5400 N/m. Using this value of k in **(2.33)**, the measured value of residual stress of the diaphragm has been extracted as 55 MPa.

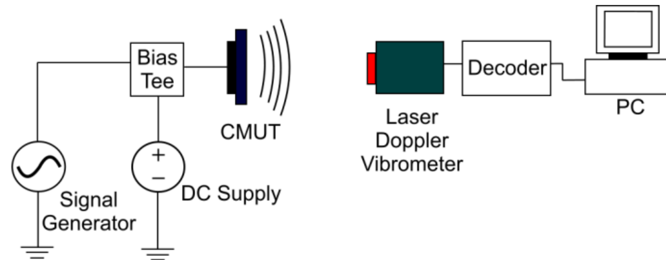


Figure 5.7. Measurement setup of Polytec laser Doppler vibrometer.

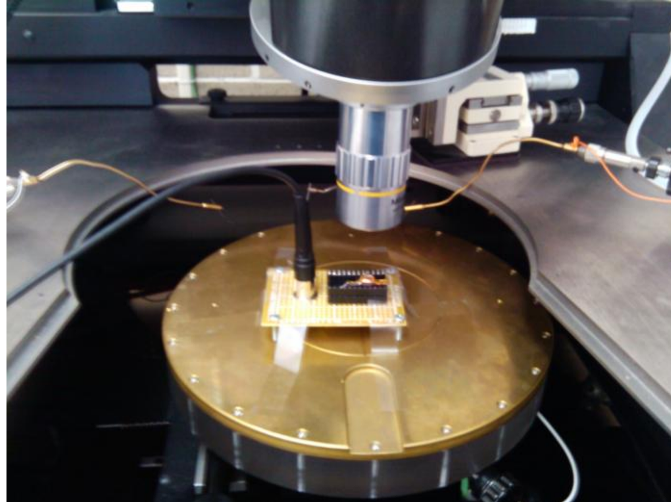


Figure 5.8. Picture of the CMUT planar array in experiment.

A comparison between analytical Matlab calculation, FEA and measurement of stiffness parameter is provided in Table 5.4. Very good agreement between theory and experiment is achieved.

Table 5.4. Comparison of Stiffness Constant

Parameter	Matlab	FEA	Measurement
Stiffness (N/m)	5447	5339	5410
Deviation from Measurement (%Δ)	1.2	1.3	

5.5 Bias Voltage vs. Center Deflection

Center deflection is measured using Wyko™ optical profilometer, under different bias voltage conditions. Then this measured data is compared with analytical model developed in MEMS lab [12], and FEA data.

In Figure 5.9, center deflection versus bias voltage is presented. Table 5.5 represents the deviation of the Matlab and FEA results from the measurement results. Very good agreement between theory and experiment is achieved.

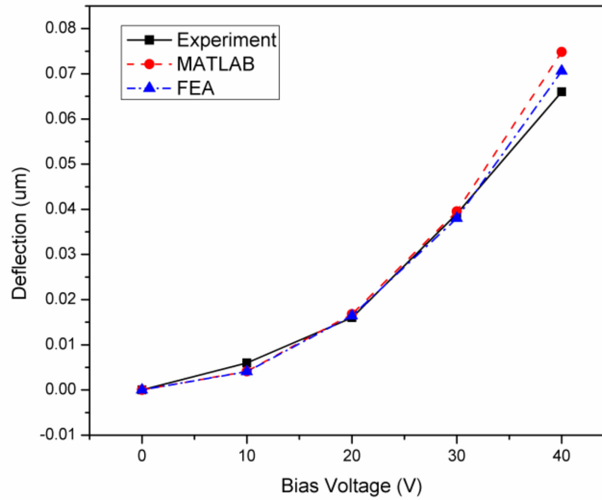


Figure 5.9. Maximum deflection vs bias voltage.

Table 5.5. Center Deflection Deviation From Measurement

	Deflection (µm)	Maximum Deviation from Measurement (%Δ)
Measurement	0.066	-
FEA	0.07	6
MATLAB	0.0748	10.2

5.6 Pull-in Voltage

The analytical pull-in voltage has been calculated using relation (2.34), and the experimental pull-in voltage has been determined using the Polytec laser Doppler vibrometer. The experimental set up for pull-in voltage measurement is shown in Figure 5.7. The experimental pull-in voltage has been measured by observing the diaphragm response to decay until the device fails while increasing DC bias voltage. After pull-in, the CMUT is failed as shown in Figure 5.12. The pull-in voltage has also been determined by 3-D electromechanical FEA using Intellisuite. The 3-D FEA result characterizing the pull-in phenomenon is shown in Figure 5.10. It is to be noted that the

etch holes are not included in the analytical and the FEA simplification and minimize simulation time. Table 5.6 presents a comparison of the experimental pull-in voltage with the analytical and FEA simulation results.

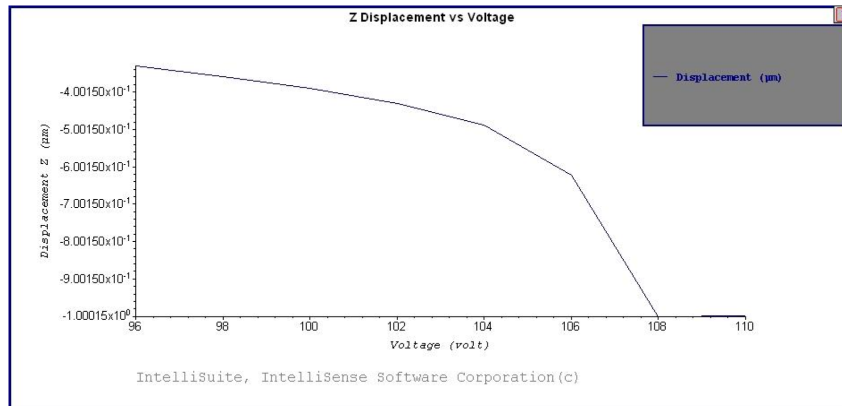


Figure 5.10. FEA displacement vs voltage graph.

Table 5.6. Pull-In Voltage Comparison Table

	Pull-in Voltage (V)	Deviation from FEA (%Δ)	Deviation from MATLAB (%Δ)
FEA	106	-	-
Matlab	111.2	4.5	-
Sample 1	118	10.1	5.7
Sample 2	110	3.6	1.1

In Figure 5.11 and Figure 5.12, diaphragm after the pull-in is presented. After focused ion beam etching, a cross section view shows that the CMUT becomes unusable due to the short circuit condition after the pull-in.

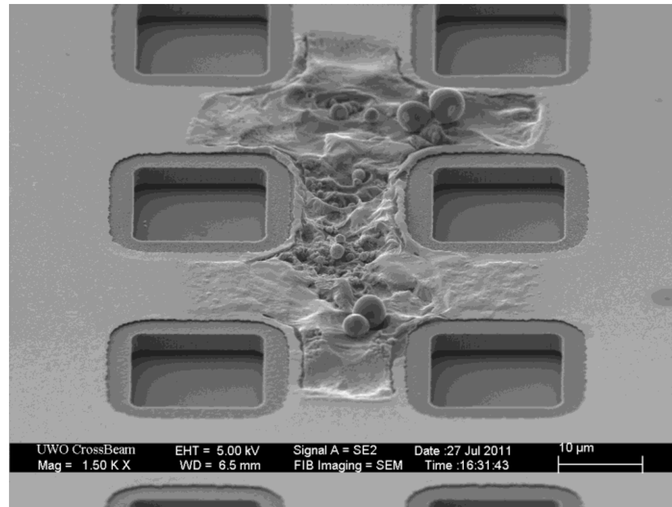


Figure 5.11. Middle of the diaphragm where pull-in occurred.

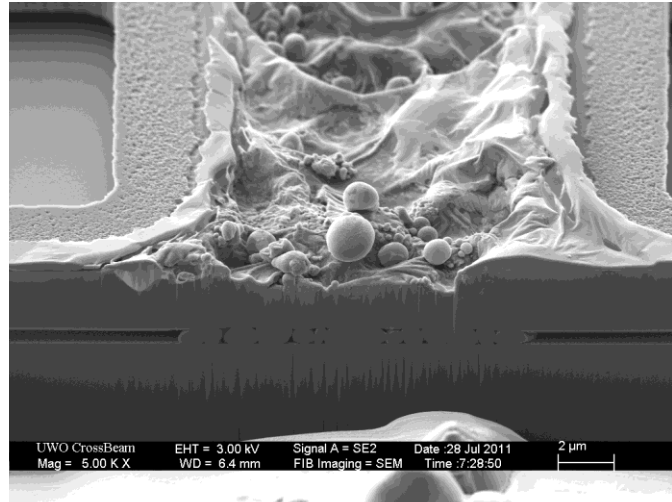


Figure 5.12. Pulled-in device cross section.

Chapter 6

DYNAMIC CHARACTERIZATION

This chapter presents the detailed methodology of dynamic characterization of the fabricated CMUTs. The methodology involves experimental measurement of the transient and steady state response of the CMUT, electrostatic spring softening, bandwidth response and comparing them with analytical (Simulink™) and FEA results to verify the design process. Polytec laser Doppler vibrometer has been used for measurements. Very good agreement has been found between the measured, calculated, and simulated values.

6.1 Resonant Frequency as a Function of Bias Voltage

The resonant frequency of the SOI based CMUT is measured with a Polytec™ laser Doppler vibrometer (MSA 4). The experimental set up is similar for the static measurement. The resonant frequency has been measured for three different bias voltages: 10 V, 20 V and 30 V, respectively and a 20 V_{AC} peak to peak signal. The frequency of the AC signal has been swept from 100 kHz to 860 kHz. Figure 6.1 shows the displacement vs. frequency measurement result from the laser Doppler vibrometer. Figure 6.1 also shows the electrostatic spring softening effect due to the bias voltage as the resonant frequency goes down with an increasing bias voltage. The measured results for 20 V DC excitation with 20 V peak-to-peak AC sweep are compared with the analytical values calculated using Matlab™ and 3D electromechanical FEA using Intellisuite™. Table 6.1 shows the comparison along with percent deviations.

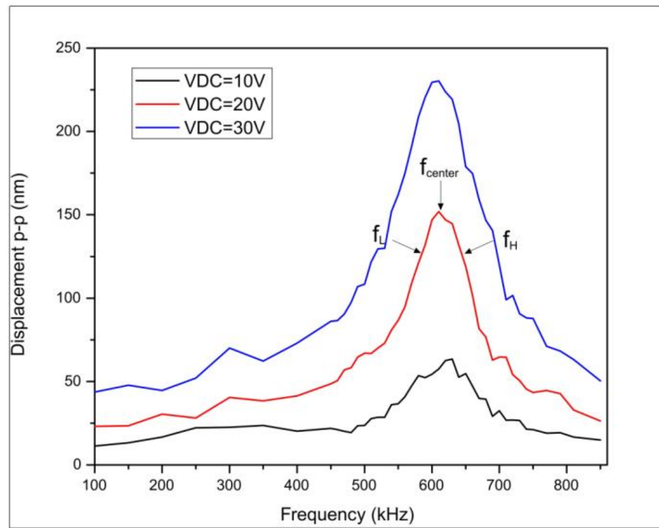


Figure 6.1. Displacement vs. frequency graph with different bias voltages.

Table 6.1. Resonant Frequency Comparison at 20V_{DC}

	Resonant Frequency (kHz) with 20 V_{DC} and 20 V_{AC}	Deviation from Measurement (%Δ)
FEA	614	0.02
MATLAB	614	0.02
Measured	615	-

The resonant frequency is plotted as a function of bias voltage in Figure 6.2. Comparative table for resonant frequency vs. bias voltage is provided in Table 6.2.

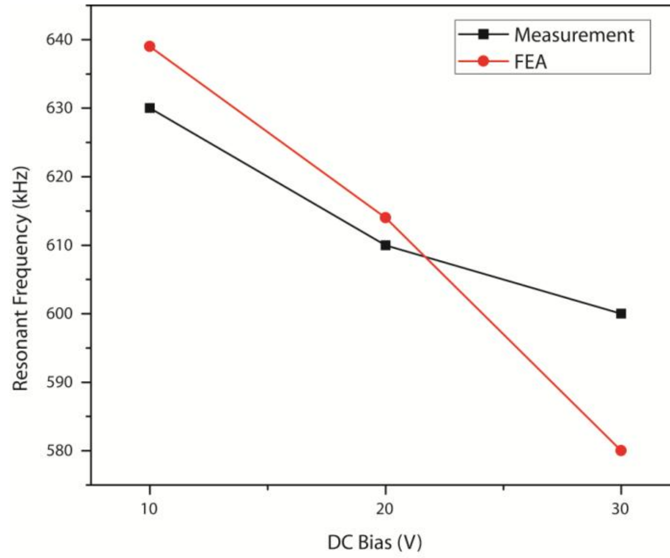


Figure 6.2. Resonant frequency vs. DC bias voltage graph.

Table 6.2. DC Bias Vs Resonant Frequency Comparison Table

DC Bias (V)	FEA (kHz)	Measurement (kHz)	Deviation (%Δ)
10	639	630	1.4
20	614	615	0.02
30	580	600	3.3

Quality factor of the CMUT is extracted from displacement vs. frequency graph in Figure 6.1, and defined as:

$$Q = \frac{f_H - f_L}{f_{center}} \tag{6.1}$$

where f_H is the higher f_{-3db} frequency, f_L is the lower f_{-3db} frequency, and f_{center} is the resonant frequency. Following (6.1) quality factor is found to be 5.87.

6.2 Transient Analysis of CMUT

Transient analysis of the diaphragm is done with Polytec laser Doppler vibrometer, and compared with Simulink and FEA dynamic simulation results with calculated and extracted parameters. For the transient analysis, the CMUT is biased with 20 V_{DC} and the AC excitation voltage is 20 V_{AC} while a Bias Tee superimposes the AC and DC signal as presented in Figure 5.7. An Agilent signal generator is used to generate 20 $V_{p\text{-}p}$ AC signal from 100 kHz to 860 kHz. Laser vibrometer is connected to a decoder and a PC in order to record the dataset.

The Time vs. displacement graph obtained from the measurement is presented in Figure 6.3, and a comparative table is provided in Table 6.3.

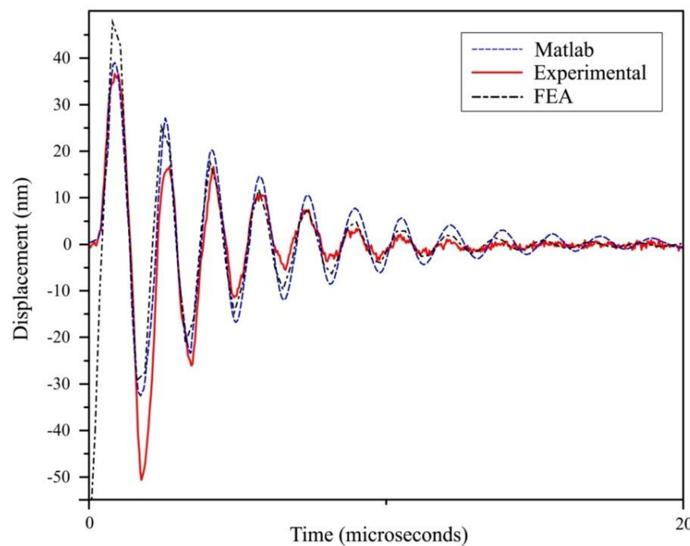


Figure 6.3. Displacement vs. time results with V_{DC}=20V and V_{AC}=20$V_{p\text{-}p}$.

Table 6.3. **Transient Analysis Deviation from Measurement with V_{DC}=20V and V_{AC}=20V_{p-p}**

	Maximum Peak to Peak Deflection (nm)	Maximum Deviation from Measurement (%Δ)
Measurement	87.12	-
FEA	78.9	9.4
MATLAB	76.9	11.7

6.3 Steady-state Analysis of CMUT

Steady-state analysis of CMUT diaphragm is done with a Polytec laser Doppler vibrometer. An Agilent signal generator is used to generate 20 V_{p-p} AC signal from 100 kHz to 860 kHz. DC bias voltage is swept from 10 V_{DC} to 30 V_{DC}. Mode based FEA analysis is done with Intellisuite to simulate the steady state response using the same excitation values for the DC and AC excitation. Figure 6.4 presents a comparative plot of the steady-state response obtained from Matlab/Simulink, Intellisuite FEA and experimental method. Table 6.4 provides maximum deviation of simulation and calculated data from the experimental values.

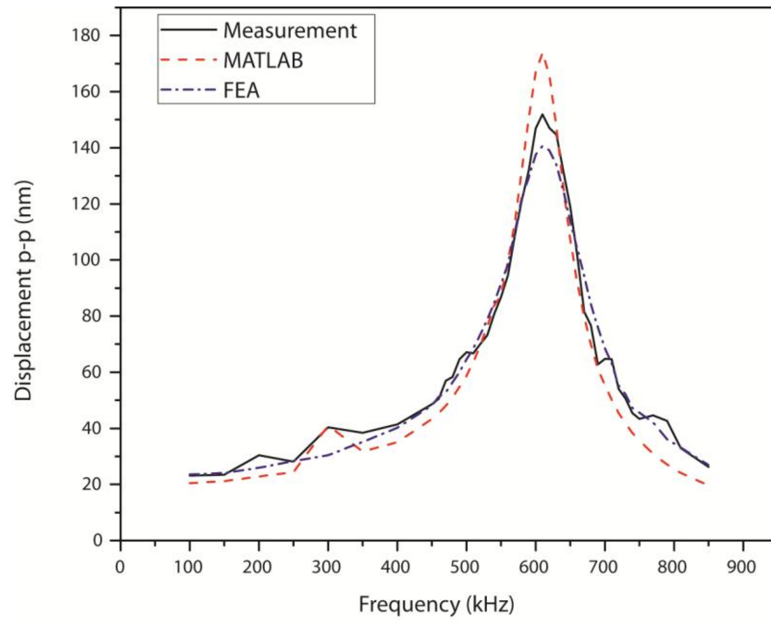


Figure 6.4. Displacement vs. frequency results with V_{DC}=20V and V_{AC}=20$V_{p\text{-}p}$.

Table 6.4. Steady State Analysis Deviation from Measurement

	Maximum Peak to Peak Deflection (nm)	Maximum Deviation from Measurement (%Δ)
Measurement	151.9	
FEA	143.8	5.3
MATLAB	168.6	11

FEA has approximated the peak to peak displacement of diaphragm much better than Simulink first order model, because it simulates the displacement with taking account of first six vibrational modes from Table 2.3, which are calculated with help of FEA frequency analysis.

6.4 Fractional Bandwidth

Fractional bandwidth F_{BW} is a figure of merit that shows how wideband the CMUT is. Fractional bandwidth is calculated from the displacement vs. frequency plot shown in Figure 6.1 and Figure 6.4 following:

$$F_{BW} = \frac{BW_{-6dB}}{f_{Center}} \times 100\% \qquad (6.2)$$

The experimental and theoretical bandwidth values are summarized in Table 6.5.

Table 6.5. Fractional Bandwidth Deviation from Measurement

	Experimental - V_{DC}=20 V	Theoretical - V_{DC}=20 V	FEA - V_{DC}=20 V
Fractional BW (%)	27	20	30.7
Deviation from Experimental (%Δ)	-	7	3.7

6.5 Bandwidth Response of CMUT

An important aspect of an ultrasound transducer is the bandwidth flatness in a desired frequency range. CMUT is tested with a variety of DC voltages in 113-167 kHz frequency band to see the bandwidth flatness.

The CMUT is excited with constant 20 $V_{AC\ p\text{-}p}$, with 113 kHz and 160 kHz respectively. DC bias voltages are swept from 10 V_{DC} to 60 V_{DC} and the results are presented in Figure 6.5. The CMUT shows exactly the same peak to peak displacement in 10 and 40 V_{DC} in 113-167 kHz frequency band. For the rest of the bias voltages the maximum deviation from 113 kHz to 160 kHz is in order of 5 nm peak to peak which is negligible. The CMUT is concluded to have a flat bandwidth response in 113-167 kHz band.

3D scan feature of the Polytec laser Doppler vibrometer is used to see the diaphragm movement as 3D animation. Fabricated CMUT is found to vibrate dominantly in first mode which is seen in Figure 6.6.

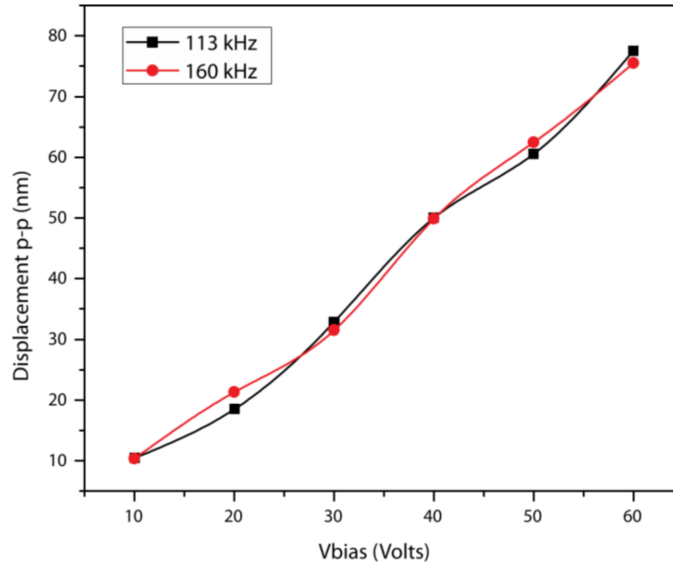


Figure 6.5. **Displacement vs bias voltage.**

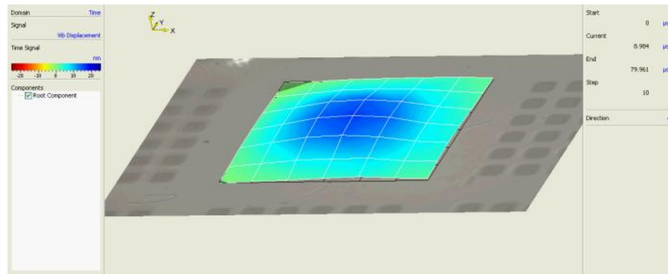


Figure 6.6. **3D scan result of CMUT with V_{DC}=30V and V_{AC}=20V_{p-p} at 113 kHz.**

Chapter 7

READOUT CIRCUIT CHARACTERIZATION

This chapter presents the characterization results of the transimpedance amplifier based readout circuit used along with the CMUT. Very good agreement has been found between theory and practice.

7.1 Noise

Measured and calculated RMS noise values are compared in Table 7.1. Deviation of the total output noise from theoretical is due to the inevitable noise sources from the environment, such as fluorescent lamps, computer power supplies, grid noise and 60 Hz noise. Since the fabricated PCB is not enclosed with shielding, all these noise sources are affecting the circuit noise level.

Table 7.1. Experimental And Theoretical Noise Comparison

	Calculated (mV_{rms})	Experimental (mV_{rms})	Deviation (%Δ)
RMS Noise	1.09	1.3	16

7.2 Simulation of Receive Mode

Microacoustics™ BAT-3 Ultrasound Transmitter is used as a transmitter. First, output pressure curve of the transmitter is extracted in NVH Lab at University of Windsor, and the result is represented in Figure 7.1.

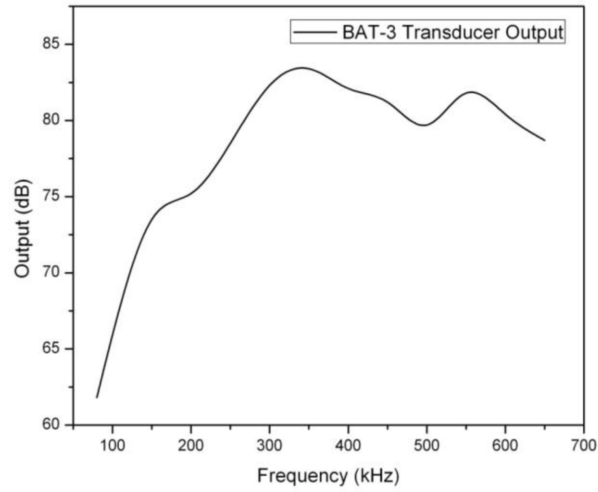


Figure 7.1. Output pressure of BAT-3 transducer with $50V_{p-p}$ excitation at 30 mm distance.

For receive mode characterization purpose, the testbench in Figure 7.2 is used. Receive mode is simulated using Mason's model represented in [39]. From the model, output of the CMUT is estimated as a result of incoming sound pressure.

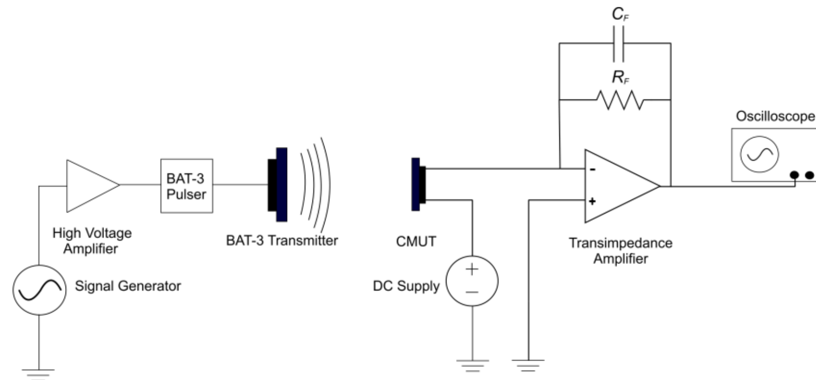


Figure 7.2. Testbench for CMUT receive mode.

Figure 7.3 represents the Spice simulation result of current from the lumped element circuit. This result can be fed into the transimpedance amplifier simulation as a current source.

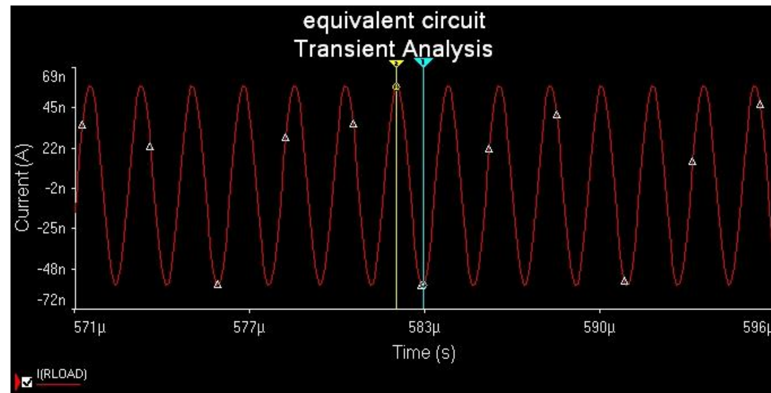


Figure 7.3. Simulated current output of the CMUT.

Transimpedance amplifier is modeled in Spice and is represented in Figure 7.4, where C_1 is the total CMUT tier capacitance, and C_2 is the parasitic capacitance seen from the input of the amplifier.

Transmitter is excited with 50 V_{p-p} AC voltage which results in 0.24 Pa in 20 mm distance. 5 Cycle sinusoidal pulse is sent in order to recognize the ultrasound wave from the electromagnetic feedthrough noise. The received signals are shown in Figure 7.5 and Figure 7.6. Note that after 5 cycles, it takes 2 cycles to damp the oscillation of the diaphragm. CMUT is biased with 30 V_{DC}. A comparative table of the experimental and theoretical results with 550 kHz 0.24 Pa sound pressure is in Table 7.2.

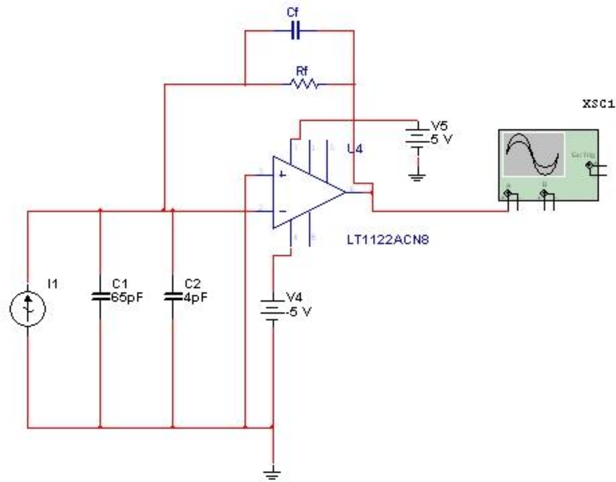


Figure 7.4. Simulation of transimpedance amplifier.

Table 7.2. Amplifier Output Deviation from Theory

	Amplitude (mV_{p-p})	Deviation (%Δ)
Theoretical	9.25	
Experimental	8.78	5.1

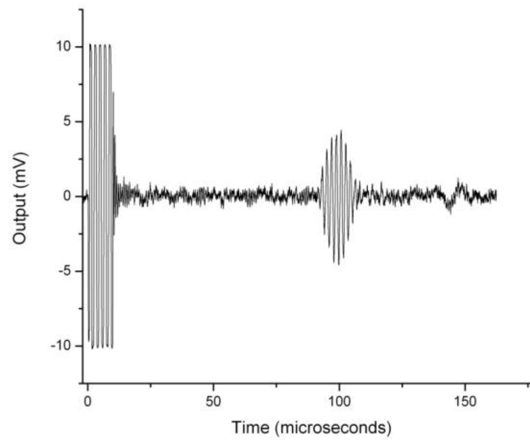


Figure 7.5. Incoming received signal.

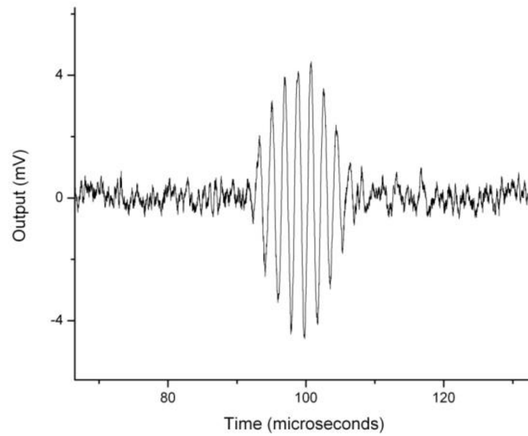


Figure 7.6. Incoming received signal, zoomed version.

7.3 Simulation of Pitch-Catch Mode

In Pitch-catch mode, two identical CMUTs are used as both receiver and transmitter, and the testbench is in Figure 7.7.

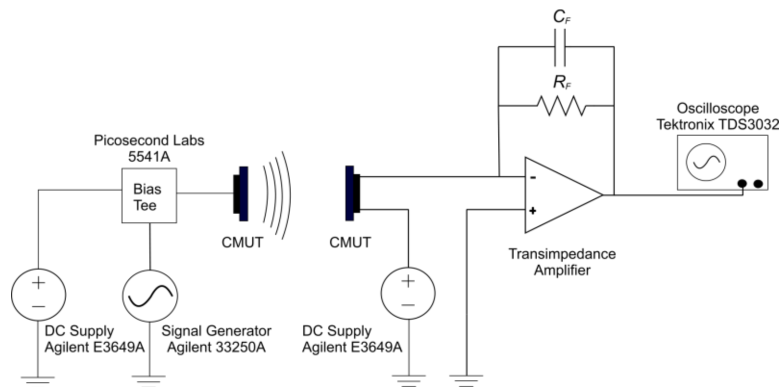


Figure 7.7. Pitch-catch mode testbench.

Both CMUT's are biased with 50 V_{DC} and transmitting CMUT was excited with 40 V_{AC} at 550 kHz. Transmitting CMUT failed after the test because of overheating due to high leakage currents at this high bias and excitation voltages required due to low output pressure of the CMUTs. Table 7.3 represents the deviation between experimental

and theoretical results. Incoming ultrasound wave from the readout circuit is in Figure 7.8.

Table 7.3. Amplifier Output Deviation From Theory

	Amplitude (mV_{p-p})	Deviation (%Δ)
Theoretical	2.1	-
Experimental	1.96	6.6

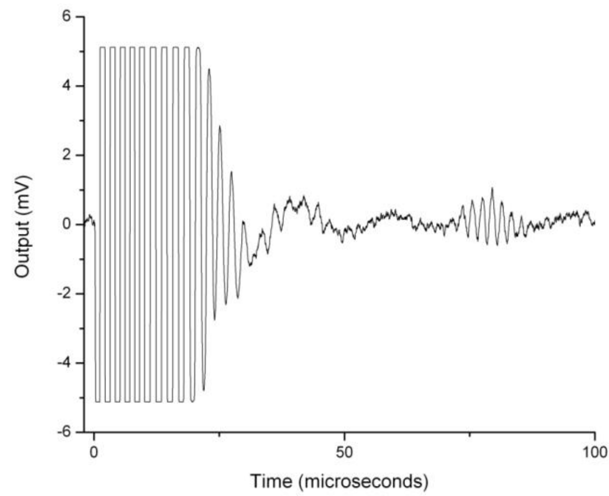


Figure 7.8. Pitch-catch mode incoming received signal.

Chapter 8

CONCLUSIONS AND DISCUSSIONS

8.1 Conclusions

An SOI based CMUT is successfully fabricated, simulated and experimentally characterized with detailed static and dynamic characterization methods explained throughout the thesis. Necessary testbenches were developed and realized for both static and dynamic characterization. Theoretical simulations are successfully carried out with analytical modeling using Simulink/Matlab™ and Intellisuite™ FEA software packages. Dynamic characterization is done by comparing theoretical data with experimental data obtained from Polytec™ laser Doppler vibrometer. Static characterization is done by using Wyko™ optical profilometer, SEM (Scanning electron microscope), and LCR meter. Finally readout circuit is designed, fabricated, and tested successfully in order to operate the CMUT in receive mode.

Very good agreement has been found in all parts of characterization, except for the dynamic capacitance change readings. After investigation, it is concluded that this apparent discrepancy in the capacitance change as a function of bias voltage values is due to the dielectric charging and trapped charges in the silicon dioxide layer and charge conduction through the air in the cavity as suggested in [46] and [50]. Sufficient mathematical models to capture these effects of dielectric charging, and charge conduction through the air in the cavity are unavailable in literature [46]. Consequently, it was not possible to include these effects in the simulation.

Overall, the characterization process gave insight into the proper methodology of design, fabrication, and testing of CMUTs.

8.2 Discussion

Major discrepancy has been found in dynamic capacitance change as a function of bias voltage due to dielectric charging, conduction through the moisture trapped in the air cavity, ionic contamination of the insulating layer (trapped charges, mobile charges in SiO_2 and interface charges).

As the whole test array consists of 6x6 CMUTs, 44% of the total array area includes SiO_2 as diaphragm support. To overcome this, the total area of insulating layer must be minimized.

As the typical SOI wafers have a single oxide layer that is etched away to create the air cavity, if the deflection of the diaphragm due to combined load of electrostatic force and ultrasound pressure reaches the pull-in limit, the diaphragm will collapse on the back plate to cause a short circuit and destroy the device. Consequently, appropriate measure must be taken to ensure that the diaphragm deflection as a combined effect of electrostatic force and the ultrasound pressure is well below the pull-in limit of the device. Thus, typical SOI wafer based construction, though it is simple and low cost, bears a risk of device failure.

Recently, SOI wafers are available with multiple dielectric layers where one of the layer could be made of SiO_2 and the other could be made of Si_3N_4 . Using such an SOI wafer will mitigate the risk of device failure. Following the same SOI etching technique, Si_3N_4 will be left after etching of the SiO_2, which will act as an insulating barrier between the diaphragm and the backplate to prevent any device failure due to diaphragm collapse. However, both SiO_2 and Si_3N_4 layers are mingled with trapped charges, ionic contamination and interface charges in addition to dielectric charging when exposed to a high electric field. In typical MOS (metal oxide semiconductor) geometry, the thickness

of the field oxide is very small, typically in the range of a few nm. Thus the effect of the impurity charges is small; however, for MEMS devices where the thickness of the oxide layer is 1-4 μm's the capacitance contributed by the impurity charges is significant. Further investigation is necessary to develop thicker oxide films with lower contamination or other insulating materials needs to be used as the dielectric spacer between the diaphragm and bottom electrode.

8.3 Future Directions

For future designs of CMUT, two possible fabrication techniques are suggested.

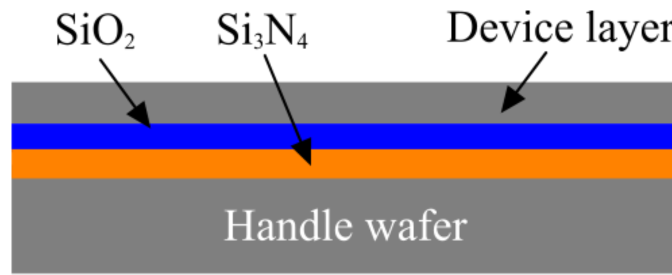


Figure 8.1. Cross section of a multilayered SOI wafer.

Some companies now offer Multilayered SOI wafers, which is a great option to provide a Si_3N_4 insulating layer on the backplate after the SiO_2 etch. A cross section of a multilayered SOI wafer is presented in Figure 8.1. After etching of the Si and SiO_2 layers, the Si_3N_4 will remain as an insulator shown in Figure 8.2.

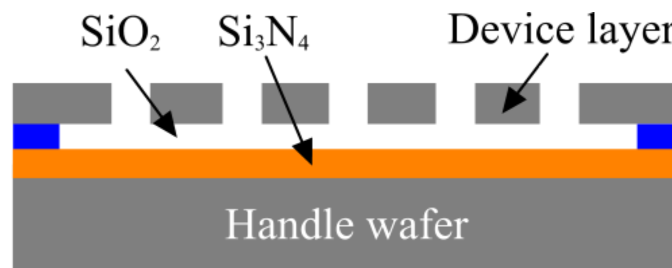


Figure 8.2. Cross section of a multilayered SOI wafer after etching Si and SiO_2 layers.

An alternative to multilayered SOI is to use a polymer called benzocyclobutene (BCB) as the insulator layer. BCB has many figures of merit [51] such as low dielectric constant, a low electrical current loss factor at high frequencies, low moisture absorption, low cure temperature, high degree of planarization, low level of ionic contaminants, high optical clarity, good thermal stability, excellent chemical resistance, and good compatibility with various metallization systems. Lower ionic contamination prevents leakage currents and charge traps, which is an important factor in MEMS devices.

APPENDICES

APPENDIX A

Transimpedance Amplifier Matlab Code

```
%% The following code calculates the transimpedance gain and phase of a transimpedance amplifier
clc;
clear;
clear all;
%% Transimpedance Amplifier Design by Tugrul Zure
%% Frequency and GBW
f= 1:100:50e6; %frequency range to be simulated
w=2*pi.*f;
s=1i.*w;
GBW=14e6; %Gain BW product of opamp
%% Parameters
flp=6.5; %Lower pole of opamp
Cs=65e-12; %Sensor capacitance
Ccm=1e-12; %Opamps common mode capacitance
Cdiff=1e-12; %Opamp differential mode capacitance
Cp=Ccm+Cdiff; %Opamp input capacitance
Cc=2e-12; %cable capacitance
Cin=Cs+Cp+Cc; %Total input capacitance to opamp
Rf=75e3; %Feedback resistor
```

```
Cf=4.7e-12; %Feedback capacitor

%% Plot A(open loop gain)

A=(GBW*flp)./(s+flp);

figure(1);

semilogx(f,db(A));

hold on;

%% Transimpedance gain of the amplifier

w0=sqrt(((GBW+1)*flp)/(Rf*(Cin+Cf)));

q=w0/(flp*(1+GBW*(Cf/(Cin+Cf)))+(1/(Rf*(Cin+Cf))));

Gainadv=Rf.*(GBW./(GBW+1)).*(w0.^2./(s.^2+s.*w0/q+w0.^2));

Gainadvdb=db(Gainadv);

semilogx(f,Gainadvdb);

xlabel('Frequency (Hz)')

ylabel('Gain (dB)')

%% Noise gain calculation

X1=s.*Cf*Rf+1;

X2=s.*Rf*(Cin+Cf)+1;

F=(X1)./(X2);

noisegainx=abs(F);

noisegain=1./noisegainx;

semilogx(f,db(noisegain));

%% Estimated bandwidth of the transimpedance amplifier

pole=1/(2*pi*Rf*(Cin+Cf));
```

```
F0=sqrt(pole*GBW)

temp=max(Gainadvdb);

temp=temp-3.0;

temp1=find(abs(Gainadvdb-temp)<.01);

f3db=mean(temp1*100)

%% Plotting the phase of the transimpedance amplifier

phase=angle(Gainadv)*180/pi;

figure(2);

%semilogx(f, angle(Gainadv)*180/pi);

semilogx(f, phase);

xlim([1 50e6]);

xlabel('Frequency (Hz)')

ylabel('Phase (Degrees)')
```

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