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Design methodology for electron-trap memory cells

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Design Methodology for Electron-Trap Memory Cells

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ABSTRACT

It is widely known that the decreasing feature size facilitated vast improvement in semiconductor-based design. But this improvement will eventually come to an end. The MOS transistor itself cannot overcome its limits dictated by its operating principle. In order to ensure further feature size reduction, the field of single-electronics has been developed. Single Electron Tunneling (SET) technology offers the ability to control the transport and position of a single or a small number of electrons.

In this thesis we investigate the implementation of arithmetic operations in SET technology. In particular we focus on design methodologies for SET based Electron-Trap which is a basic memory cell that has been recently fabricated.

Given a circuit topology and the corresponding targeted behaviour, the proposed methodology assists the circuit designer in deriving the circuit parameters in an analytical way. The methodology is based on the mathematical description of the tunnel junctions in the circuit. Moreover the method allows for the analysis of reliability issues.

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CHAPTER I
INTRODUCTION

Because of the ongoing increase in complexity of software, there is an urgent need for more powerful computers. The enormous success of semiconductor microelectronics during the past three decades was based on scaling down of silicon field effect transistors (MOSFETs) and the resulting increase of density of logic and memory chips. Moore's law (which states that the number of components per chip doubles every 18 months) has remained valid since it first became known in 1965. However, prospects to continue the Moore Law beyond the 10 nm are much more uncertain. It is generally expected that current technology eventually cannot be pushed beyond some limit. This limit is expected to arise in mainly two areas: power consumption and scalability. In order to keep variations of the transistor threshold voltage below an acceptable limit (~50 mV), gate length of a 5-nm MOSFET should be controlled better than ~ 0.25-nm, which shows high sensitivity to parameter fluctuations, and hence to the fabrication process as a whole, may lead to increasing of chip fabrication facilities cost, very high even now. As a result, the Si-MOSFET-based Moore Law may stop at gate length ~ 10 nm, long before fundamental physical limits have been reached. These prospects

give a strong motivation for the search for alternative devices that could replace MOSFETs beyond the 10-nm.

In order to ensure further feature size reduction, the field of single-electronics has come of age. SET technology allows controlled transport of single electrons among quantum islands. If values or bits are represented by single or few electrons this technology has in principal the potential of performing computation with lower power consumption than CMOS technology. When semiconductor structures are scaled down to the nanometer region and beyond, quantum mechanics effects increase and finally determine the behaviour. While for CMOS this causes faults to occur, and therefore is a limit to the scalability, for SET this means scalability even on atomic scale set, because SET is based on quantum mechanics effects [1].

Because of the SET technology potential several proposals have been made to implement computational structures using SET technology. The main type of implementation represents bits by single electrons, thus it utilizes the SET device capability to control the transport of single electrons. In these implementations SET devices are used to transport electrons to and from quantum islands (sometimes called quantum dots). Using this approach the power consumption is very low. For an overview of these implementations the reader is referred to [2].

These attempts of scientists to build circuits using SET technology have mainly taken place in the last decade, although the principles of SET have been known for many decades. Since SET technology is different from MOS technology, existing design methodologies are not applicable. Additionally, CAD

tools are not available and only a small number of simulators exist. Thus the design of SET circuits is generally speaking not automated. Therefore the first objective of this research is to propose a design methodology for deriving the circuit parameters of SET based Electron-Trap memory cell. A SET Electron-Trap is a small circuit consisting of a few (typically between one and four) tunnel junctions and some other circuit elements (like capacitors, voltage sources, etc.), which performs an elementary operation. Nano-scale devices are more sensitive to a variety of random noises which are the random charges appearing on nodes of SET devices during the fabrication process. These charges generate a biased voltage contributing to the total voltage across the SET device. The function of the device could be destroyed. Thus reliability turns out to be one of the biggest concerns in designing SET devices. Our second objective is the reliability analysis of SET Electron-Traps.

This thesis is organized as follows. Chapter 2 provides a background on the SET phenomenon and introduces the previous works, including the theoretical background of SET technology, several proposed SET memory cells, and some challenges. In Chapter 3 the first objective of this research is met by proposing a design methodology for SET based Electron-Trap memory cells. Chapter 4 concerns the second objective. We analyze the reliability of SET circuits by introducing Random Background Charge on the single island. Chapter 5 concludes this thesis with future works being discussed.

CHAPTER II

SINGEL-ELECTRON TUNNELING BACKGROUND

In this chapter some background information on SET technology is provided. In the first section the basic theory of single electron tunneling is presented. Since this thesis is about the utilization of basic SET devices for computation, and not about the physics of SET devices only the theory needed for understanding the SET tunnel junction behaviour is presented. Section 2.2 discusses the reliability issue of SET, we concern Random Background Charge which is the biggest challenge in designing SET devices. In Section 2.3 an overview of the proposed SET memory cells is given. The simulator-SIMON is introduced in Section 2.4.

2.1 Theoretical Background of SET

2.1.1 Single Electron Tunneling

In the classic physics theory electrons are viewed of as particles and the theory does not allow electrons to cross a barrier like a piece of insulator. In 1923 L. de Broglie [3] suggested that particles may also behave like waves. Three years later this hypothesis was formally described by Schrodinger, which became the basis for the quantum mechanics theory of today. Using the Schrodinger wave equation there is a probability that an electron tunnels through a barrier and enters a classically forbidden region.

This tunneling phenomenon is the basic principle of SET technology. It is used to create the basic circuit element of SET technology, the tunnel junction. The symbol for the tunnel junction is depicted in Figure 2.1. The junction is created by separating two conductors with a thin insulator and therefore it behaves like a capacitor. Given that the insulator is thin enough quantum tunneling may occur. The tunneling of an electron through the junction is called a tunnel event.

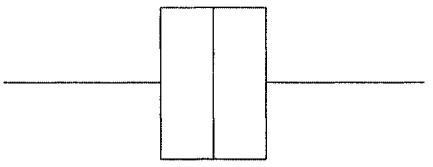

Fig 2.1: Symbol of tunnel junction

2.1.2 Single Electron Box

The electron box (see Figure 2.2) is one of the most simple SET circuits. On one side the island is connected to a voltage source through a tunnel junction, On the other side it is connected to the ground through a capacitor, which is formed by the thick piece of insulator.

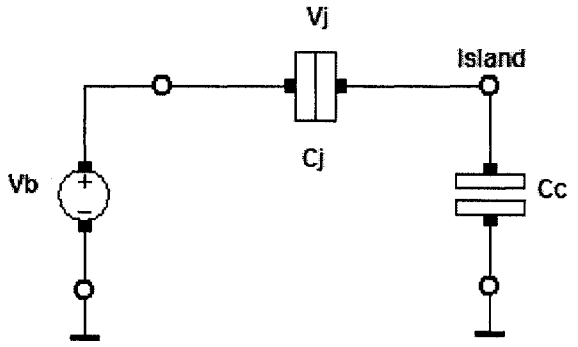

Fig 2.2: Single Electron Box

The basic working principle of Single Electron Box is that one needs Coulomb energy E_c to charge an island with an electron:

$$E_c = \frac{e^2}{2C_\Sigma} >> kT \qquad (2.1)$$

Where k is Boltzmann's constant, T is absolute temperature, C_Σ is the total capacitance of the island which is charged, e is the elementary charge. If the Coulomb energy is not available a tunnel event cannot happen. This phenomenon is known as Coulomb blockade. The voltage source can provide the energy needed for an electron to tunnel. If the bias voltage exceeds a certain value an electron

tunnels from the island. Further increase of the bias voltage eventually leads to a second electron to tunnel. This way, the number of electrons present on the island can be controlled by the bias voltage (see Fig 2.3).

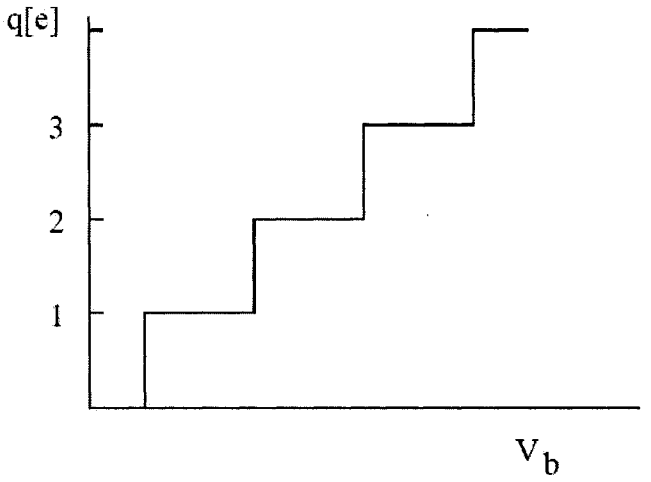

Fig 2.3: Transfer function of Single Electron Box

When building circuits with tunnel junctions, one needs to predict the tunneling of electrons. This could be done by calculating all free energy in the circuit. But even for modest sized circuits this method results in very complex computation. Therefore generally the method of critical voltage is employed [4, 5]. This method predicts that an electron only tunnels if the voltage across the tunnel junction (V_j) is greater than some critical voltage (V_c). For the Single Electron Box displayed in Fig 2.2:

$$V_c = \frac{e}{2(C_j + C_c)} \tag{2.2}$$

$$V_j = \frac{C_c V_b}{C_j + C_c} + \frac{e}{C_j + C_c} \tag{2.3}$$

2.2 Reliability issue of SET

SET devices show high sensitivity to parameter fluctuations. During fabrication process, it is unavoidable that certain amount of charges (Random Background Charge) appears on islands of SET devices. It may be caused by several reasons: charged impurities in the surrounding material, charged tarps on surface and grain boundaries, charges on nearby conductors, etc. These background charges will be mobile and move and change over time. With today's techniques, one is not able to control them. These random charges are so devastating, because they can fully suppress the Coulomb Blockade.

One observes the Coulomb blockade in the I-V characteristic (see Fig 2.4) [6]. The size of the blockade is

$$V_c = \frac{e}{2C_\Sigma} - \frac{2Q_0}{C_\Sigma}, \text{for } Q_0 = [0,0.5]\,e \qquad (2.4)$$

Where $e = 1.6 \times 10^{-19}\,C$, C_Σ denotes the capacitance of the island. It shows that the Coulomb Blockade is largest for zero background charge, but if we consider a background charge, the Coulomb Blockade, depending on the amount of background charge, decreases and vanishes completely for $Q_0 = 0.5$. As one can imagine, the Random Background Charge problem is crucial. It will decide the usability of SET devices.

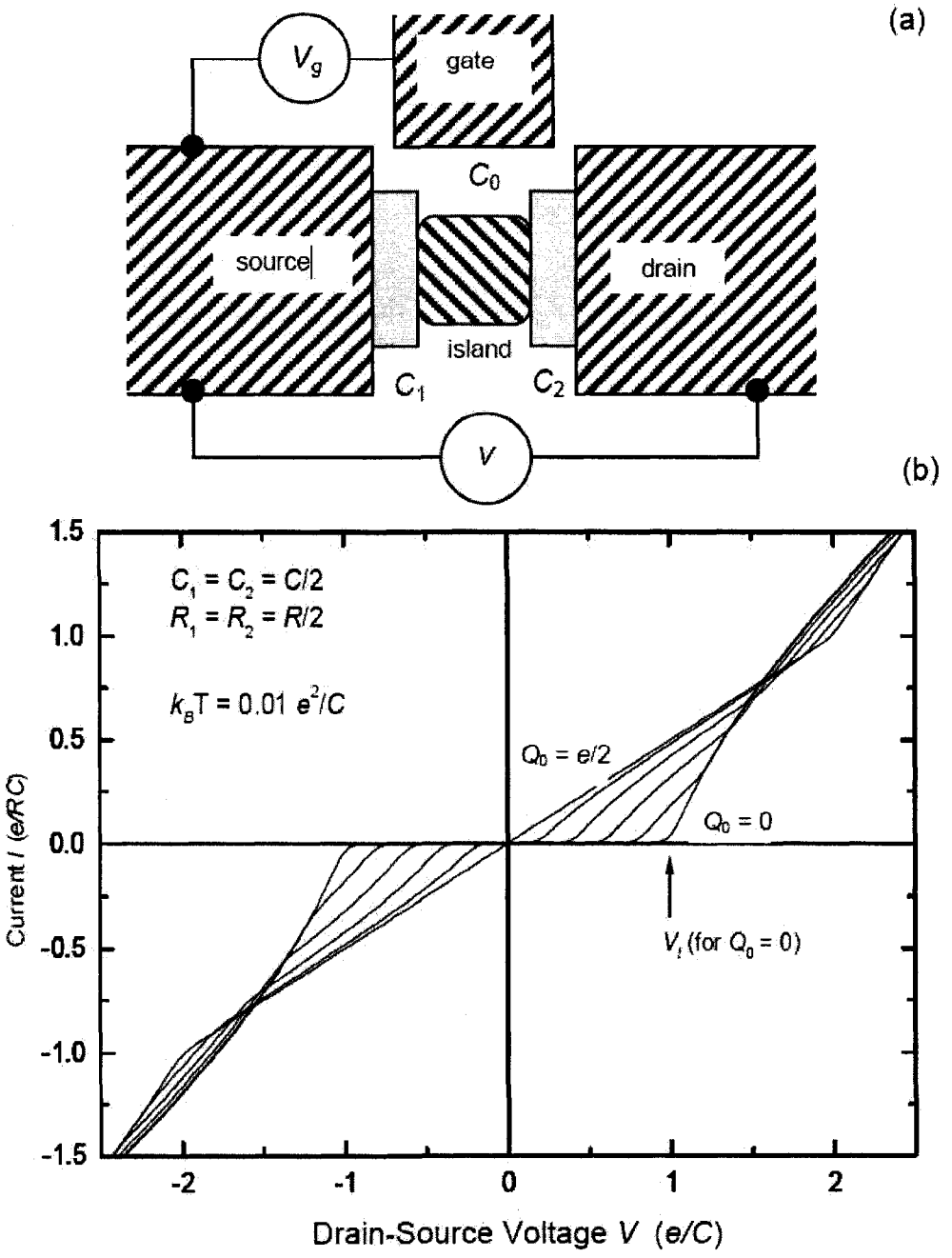

Fig 2.4: I-V characteristic with different background charge Q_0

Now there are some promising solutions such as using current oscillations to determine the presence of absence of charge on a floating gate [7] and using multi-island structure [8,9]. But they are not perfect. So, one of our purposes to design SET devices is to make the circuit more tolerant to background charge. The detailed reliability analysis and simulation are given in Chapter IV.

2.3 Some basic memory cells

Memory is one of the most promising SET applications. What are the criteria for a good single electron memory cell? Such a SET memory should work at room temperature with a reasonable bit error rate. It should have low power consumption and not sensitive to background charge which is a random offset charge induced by stray capacitances and impurities located near the circuit nodes [10]. Several different single-electron memory cells are analyzed and compared on the basis of the above criteria in [11].

2.3.1 SET Flip-Flop

One design possibility is to mimic conventional memory design with SET devices, such as a static SET memory cell or Flip-Flop. The design was proposed by A. Korotkov etal [13]. R-S Flip-Flop is one of the most basic memory elements, the behaviour and structure of which are shown in Table 2.1 and Fig 2.5, respectively.

Table 2.1: The behaviour of Flip-Flop

R	S	Q	QN	Function
0	0	last Q	last QN	Hold current output values Q and QN.
0	1	1	0	Set output Q to 1 (and QN to 0).
1	0	0	1	Reset output Q to 0 (and QN to 1).
1	1	?	?	Unspecified / Forbidden input combination.

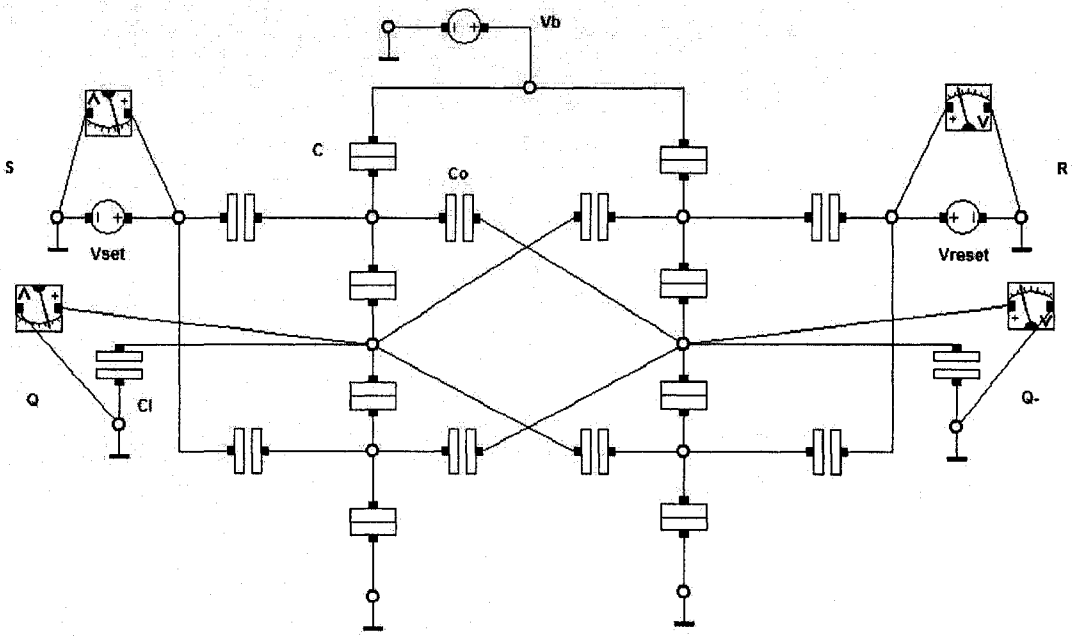

Fig 2.5: SET R-S Flip-Flop

The first two bars represent the inputs $\bar{S}$ and $\bar{R}$, and the bottom two bars represent the outputs Q and $\bar{Q}$. Initially, the inputs are $\bar{S} = 1$ and $\bar{R} = 0$, while the

outputs $Q = 0$ and $\bar{Q} = 1$. These output values are memorized when the input $\bar{R}$ becomes one. When the input $\bar{S}$ becomes zero, the outputs are set to $Q = 1$ and $\bar{Q} = 0$. Next, $\bar{S}$ and $\bar{R}$ are both set to zero, as a result of which the outputs Q and $\bar{Q}$ are both one. Therefore, we conclude that the circuit correctly implements the behaviour as traditional Boolean gate-based R-S Filp-Flop.

2.3.2 Electron-Trap Memory

Nakazato and Ahmed [15, 16] proposed the idea of a dynamic memory cell pushed to its extreme. A small number of electrons, or even just a single electron, is stored on a single island. Their presence on the island corresponds to logical '1' and their absence to '0' [17, 18] (see Fig 2.6). The line of tunnel junctions introduces an energy barrier for electrons entering or leaving the island. Thus, stored electrons reside in a local energy minimum. To write in this cell a voltage pulse V_g is applied, which eliminates the energy barrier. A positive pulse forces electrons to tunnel through junctions onto island. A negative voltage pulse forces electrons to tunnel off of the island to ground. The state of the island is sensed at V_{out}. The more tunnel junctions are used the less likely it is that electrons escape from the storage node to ground.

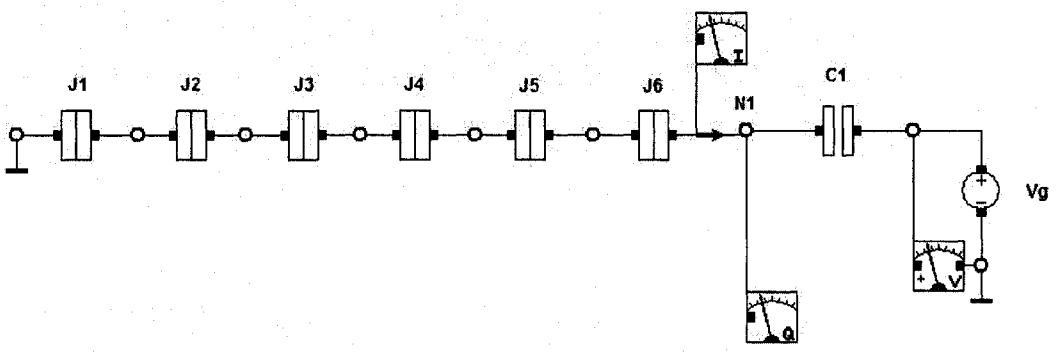

Fig 2.6: SET Electron-Trap Memory with six tunnel junctions

2.3.3 SET Ring Memory

A different idea which is a generalization of the bistable quantum cell for cellular automata by Lent et al. [14] is shown in Fig 2.6. On the circuit level it is also similar to the electron trap memory, because it is a trap connected to a ring, a so called ring memory cell. However the operation is different. An even number (n=6 in our case) of tunnel junctions is connected to a ring, and n/2 electrons are inserted into the ring. Due to their Coulomb interaction, they will repel each other and thus can form two stable configurations (see Fig 2.7). Applying positive or negative voltage pulses on V_{in} will switch the state of the ring to either one of the stable configurations. The capacitors should be small compared to the capacitances of the tunnel junctions, so that the electrons have a large influence on their neighbors and keep their distance.

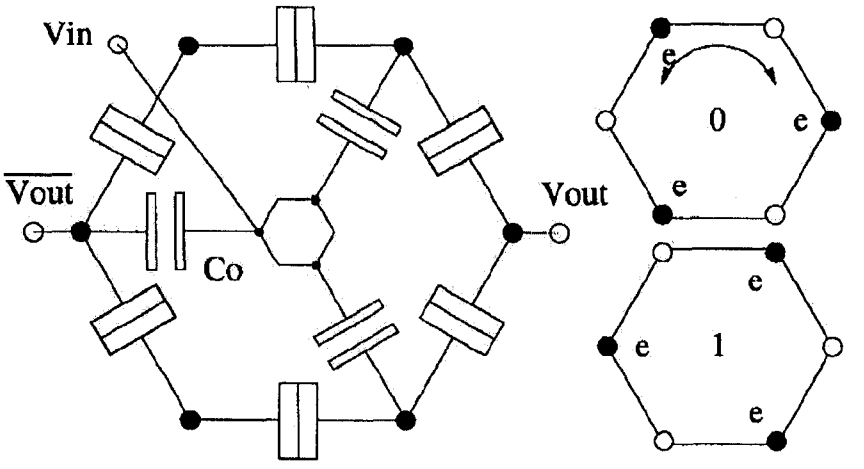

Fig 2.7: SET Ring Memory Cell

2.4 Simulator-SIMON

SIMON is a single-electron tunnel device and circuit simulator [12]. It allows transient and stationary simulation of arbitrary circuit consisting of tunnel junctions, capacitors, and voltage sources of three kinds: constant, piecewise linearly time dependent, dan voltage controlled. A graphic user interface allows the quick and easy design of circuits with single-electron tunnel devices. Parameters can be changed interactively, and simulation results can be looked at in graphical form. Also, all simulation parameters such as simulation mode, event number, and temperature, are modifiable. Fig 2.8 shows the interface of SIMON. All the simulation results issued in the following two Chapters are achieved by SIMON.

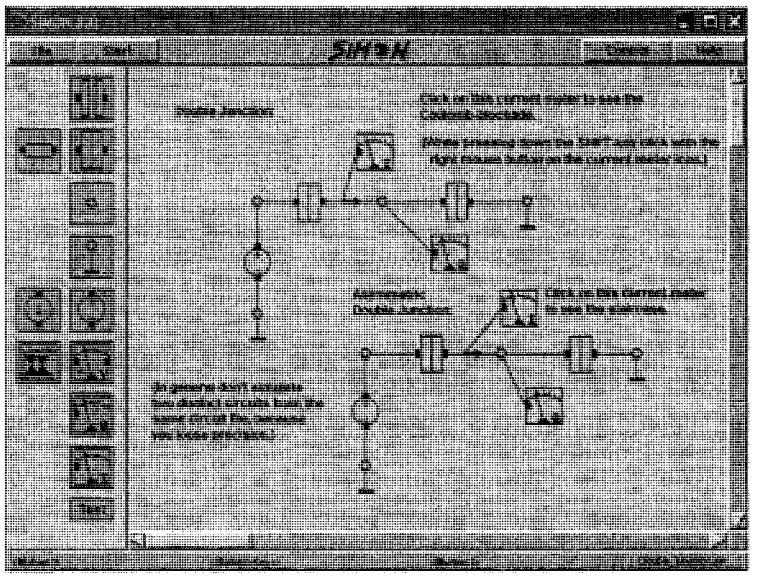

Fig 2.8: Interface of SIMON

CHAPTER III

DESIGN METHODOLOGY

Although the principles of electron tunneling have been known for many decades, it has only been in the last decade that a few circuits using SET technology have been designed. Since SET technology is different from MOS technology, existing design methodologies are not applicable. Therefore, designing circuits with SET components has not been done very often. Computer design tools are not available and only a small number of simulators exist. The design of SET memory cells is generally not automated. This chapter provides a methodology for finding the circuit parameters of SET based Electron-Trap memory cell. The design methodology presented in this section focuses on implementations where values are represented by single or few electrons.

This chapter is organized as follows. In Section 3.1 a brief overview of steps of the methodology is given. In Section 3.2 these steps are explained in more detail based on a SET memory cell model. The design is verified and Simulation results are showed in Section 3.3. An improved structure of Electron-Trap is showed in Section 3.4. Section 3.5 discusses the voltage range and the number of tunnel junctions which are important for memory cell design.

3.1 Overview of the methodology

The aim of the methodology is to calculate the circuit parameters given a circuit topology, the corresponding targeted behaviour and some known parameters. It consists of the following steps:

A. Derive the basic equations.

B. Derive the voltage value applied to the circuit.

C. Write logical value "1" in the cell.

D. Hold the electron at N1.

E. Write logical value "0" in the cell.

In the next sections the steps of the methodology are explained in more detail using an example circuit. Since the SET Electron-Trap memory cell, presented in Section 2.3.2, is an important memory cell for the research described in this thesis, it is used throughout this chapter to explain the methodology.

3.2 SET Electron-Trap memory cell model for the methodology

Fig 3.1 shows the circuit diagram of the SET Electron-Trap memory cell that will be used throughout this work. The electron trap circuit consists of N tunnel junctions and N islands, One capacitor C_g is bounded by N1. The resistance of each junction is $10^5\Omega$ and we assume each junction and capacitor have same capacitance $C_n = C = 10^{-18}F$. An electron or a small number of electrons is stored on the island N1. Their presence on N1 corresponds to logical '1' and their absence to logical '0'. The line of tunnel junctions introduces an energy barrier for electrons entering or leaving N1. To write in this cell, a voltage pulse is applied at V_g, which eliminates the energy barrier. A positive voltage pulse V_g forces electrons to tunnel from ground, through junction J_n and eventually to island N1. A negative voltage pulse V_g forces electrons to tunnel off of N1 to ground.

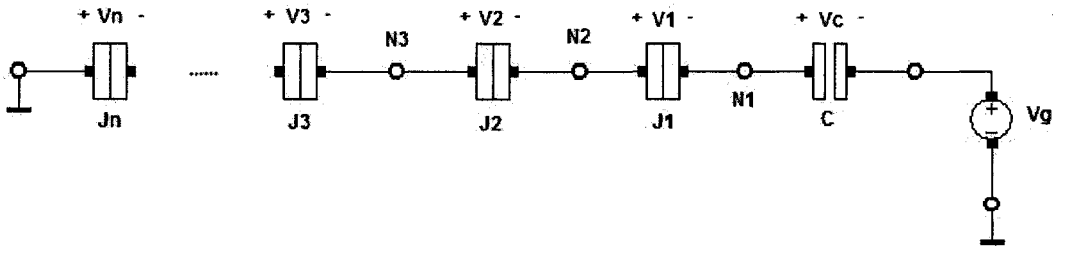

Fig 3.1: Circuit diagram of an Electron-Trap memory cell

A. Derive the basic equations.

The first step of the methodology is to derive the characteristic equations for all junctions of the circuit. The behavior of a SET circuit is mainly determined by the behavior of the tunnel junctions. Thus the behavior can be characterized by a set of equations describing the voltages across the junctions. For each junction one equation can be derived. In the following part, we will use these equations to show the detailed operation of the Electron-Trap memory cell and do parameter selection based on some known parameters.

The characteristic equations can be derived by performing the following steps:

- Derive the basic equations describing the charges on the capacitors, tunnel junctions and the circuit nodes.
- For each junction, find a voltage relation to start the derivation. A good voltage relation should at least contain some important input voltage, the voltage across the junction of which the characteristic equation is being derived, and as many other voltages across junctions as possible.
- Specify what parameters are know, what are unknown.

To derive the basic equations describing the charges on the tunnel junctions, they can be treated as capacitors, and therefore the charges can be described as the product of the capacitance of the junction times the voltage across it. Assuming

$q_1, q_2, \ldots q_n$ are the initial charges in the islands $N_1, N_2, \ldots N_n$ respectively, for the SET Electron-Trap memory cell the following basic equations were found:

$$q_1 = C\ V_c - C_1 V_1 \tag{3.1}$$

$$q_2 = C_1 V_1 - C_2 V_2 \tag{3.2}$$

$$q_3 = C_2 V_2 - C_3 V_3 \tag{3.3}$$

$$\cdots$$

$$q_n = C_{n-1} V_{n-1} - C_n V_n \tag{3.4}$$

The SET Electron-Trap memory cell contains N tunnel junctions, so N characteristic equations should be derived and we need a voltage relation to start with. For this topology there is a voltage relation which meets the conditions of a good starting point for all the derivations:

$$-V_g = V_1 + V_2 + V_3 + V_c + \cdots V_n \tag{3.5}$$

$$V_{cri} = \frac{e}{2(C_e + C_j)} \quad (j=1, 2, 3) \tag{3.6}$$

$$V_g \geq (n+1)V_{cri} \tag{3.7}$$

Where V_n , V_c are the voltages across each tunnel junction and capacitor C, respectively. V_g is the voltage applied to the circuit. Equation (3.6) calculates the critical voltage of a junction, we assume a tunnel junction with a capacitance of C_j . The remainder of the circuit, as viewed from the tunnel junction's perspective, has an equivalent capacitance of C_e [10].

B. Derive the voltage value applied to the circuit.

Initially, the voltage V_g is zero and there are no electrons at the island N1. After some time it becomes positive and reaches a certain value, which makes the voltage across the tunnel junction J_n larger than its threshold voltage, tunnel event happens. The value of V_g can be determined by equation (3.5) and (3.6).

C. Write logical value "1" in the cell.

To write logical value "1" in the cell, V_g becomes positive and reaches a certain value. One electron tunnels from ground to the nearest island.

D. Hold the electron at N1.

After some time, the value of V_g becomes zero and remains for a short time. As a memory cell, the electron should remains in N1, because the voltage across J_1 is less than its critical voltage. It means that the electron can not surmount the potential barrier imposed by junctions J_1 - J_n .

E. Write logical value "0" in the cell.

To write the logical value "0" in the cell, which currently keeps the logical value "1", V_g becomes negative and reaches a certain value. At this time the electron is transported from N1 to ground. The process is the same as step C.

3.3 Design Verification

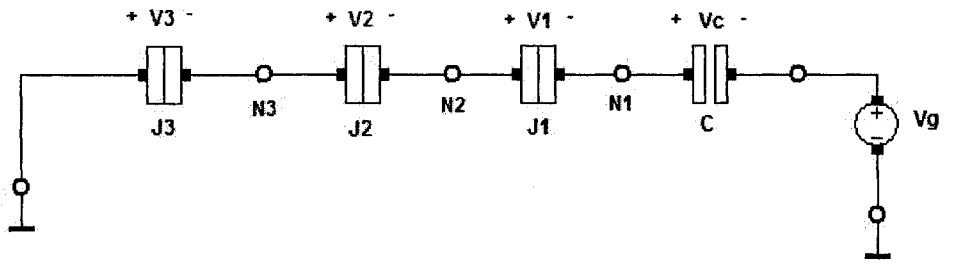

Fig 3.2: Circuit diagram of an Electron-Trap with 3 tunnel junctions

To verify the above methodology, we use the Electron-Trap with three tunnel junctions which is shown in Fig 3.2. According to the methodology above, the basic equations can be written as:

$$q_1 = C\ V_c - C_1 V_1 \tag{3.8}$$

$$q_2 = C_1 V_1 - C_2 V_2 \tag{3.9}$$

$$q_3 = C_2 V_2 - C_3 V_3 \tag{3.10}$$

$$-V_g = V_1 + V_2 + V_3 + V_c \tag{3.11}$$

$$V_{cri} = \frac{e}{2(C_e + C_j)} \quad (j=1, 2, 3) \tag{3.12}$$

$$V_g \geq 4V_{cri} \tag{3.13}$$

We assume each junction and capacitor have same capacitance $C_1 = C_2 = C_3 = C = 10^{-18}\,F$, Using (3.8)~(3.13), q_1, q_2 and q_3 all being zero, the minimum value of V_g to make the tunnel event happen is $V_g = 0.24V$. We

choose $V_g = 0.25V$ to ensure that one electron tunnels. The threshold voltage for one tunnel junction is $V_{cri} = 0.06V$.

To write logical value "1" in the cell, V_g becomes positive and reaches the value of 0.25V. One electron tunnels from ground to N3. Table 3.1 shows the values of voltage across each tunnel junction when the electron stays in N3, N2, N1, respectively.

Table 3.1: The process of voltage changes with 3 tunnel junction3 Electron-Trap

V_g (V)	V_1 (V)	V_2 (V)	V_3 (V)	Electron position	Tunnel?
0.25	0.0625	0.0625	0.0625	None	YES
0.25	0.1025	0.1025	-0.0575	N3	YES
0.25	0.1425	-0.0175	-0.0175	N2	YES
0.25	0.0225	0.0225	0.0225	N1	NO

After some time, V_g decreases to zero. In Table 3.2, since the voltage across J_1 is less than its threshold voltage, that the electron remains in N1.

Table 3.2: The voltage across junctions when V_g =0 for 3 tunnel junctions

Electron-Trap

V_g	V_1	V_2	V_3	Electron position	Keep on tunneling?
0V	-0.04V $< V_{cri}$	-0.04V	-0.04V	N1	No

To write the logical value "0" in the cell, which currently keeps the logical value "1", V_g becomes negative and reaches the value of -0.09V. At this time the electron is transported from N1 back to ground.

Fig 3.3 shows the simulation results.

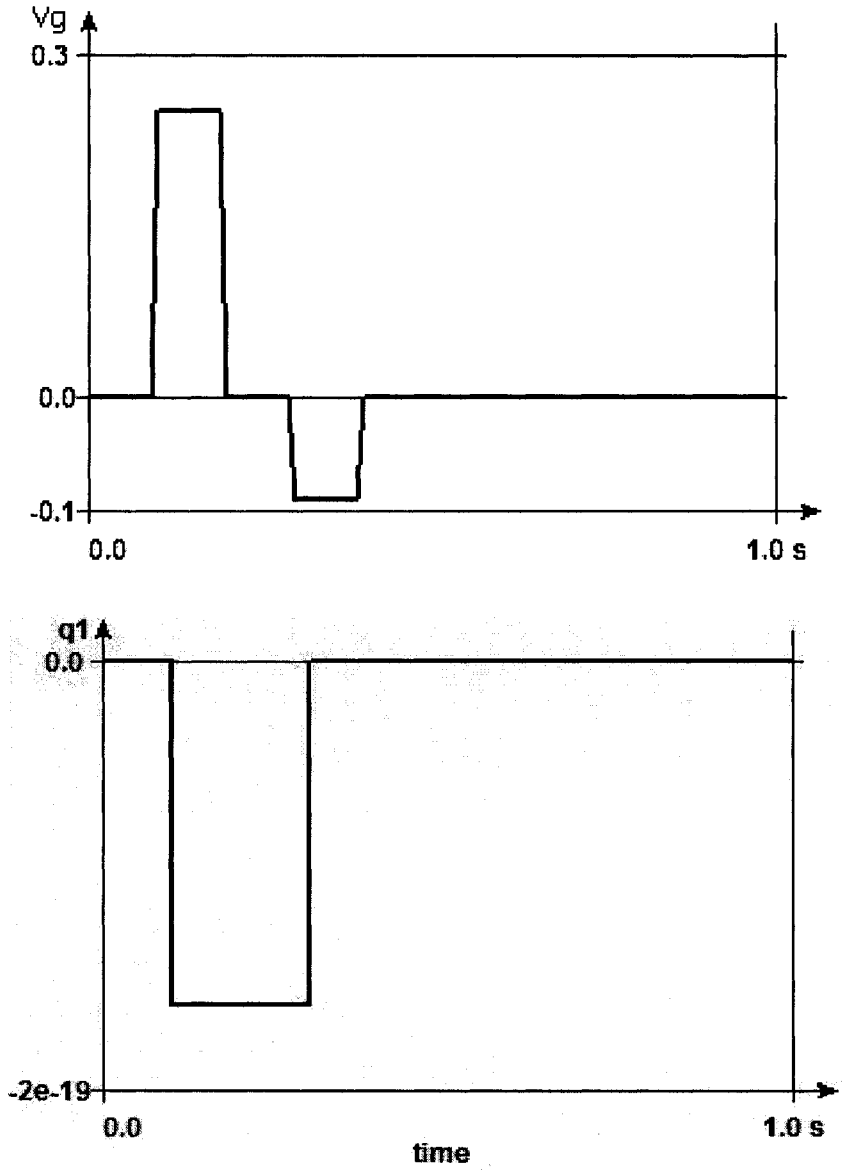

Fig 3.3: The time variation of the voltage V_g and the charge at N1

3.4 Improved structure of Electron-Trap

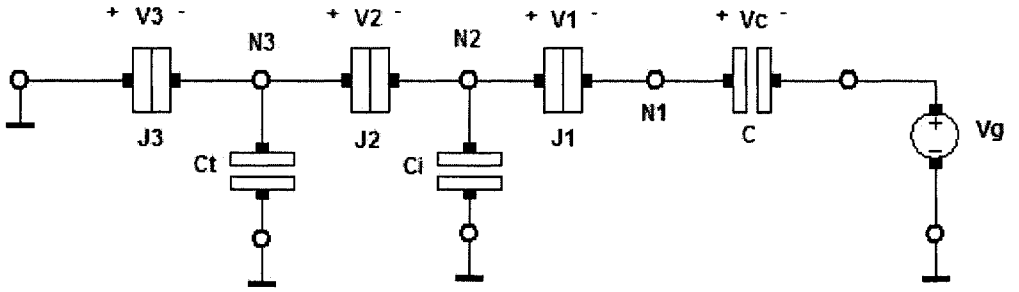

Fig 3.4 Electron-Trap with capacitances to ground

Fig 3.4 shows a SET Electron-Trap memory cell which is slightly different from the one shown in Fig 3.2. It has capacitances connected to ground. The basic equations can be derived using the methodology shown in previous sections.

$$q_1 = C\ V_c - C_1 V_1 \tag{3.14}$$

$$q_2 = C_1 V_1 - C_2 V_2 + C_i V_i \tag{3.15}$$

$$q_3 = C_2 V_2 - C_3 V_3 + C_t V_t \tag{3.16}$$

$$-V_g = V_1 + V_2 + V_3 + V_c \tag{3.17}$$

$$V_t = V_3 \tag{3.18}$$

$$V_i = V_2 + V_3 \tag{3.19}$$

$$V_{cri} = \frac{e}{2(C_e + C_j)} \quad (j=1, 2, 3) \tag{3.20}$$

$$V_g \geq 4V_{cri} \tag{3.21}$$

Where each tunnel junction has same capacitance $C_1 = C_2 = C_3 = 10^{-18}\,\mathrm{F}$, the value of capacitor is $C = 2\times10^{-18}\,\mathrm{F}$. By using equations (3.14)~(3.21), the minimum

value of V_g to make a tunnel event happen is $V_g = 0.09V$, the electron goes back to ground when V_g becomes negative and reaches the value of -0.07V. Observation from the Fig 3.5, it is obvious that the minimum value of V_g to drive the circuit reduces to 0.09V, compared with 0.24V for the structure shown in Fig 3.2.

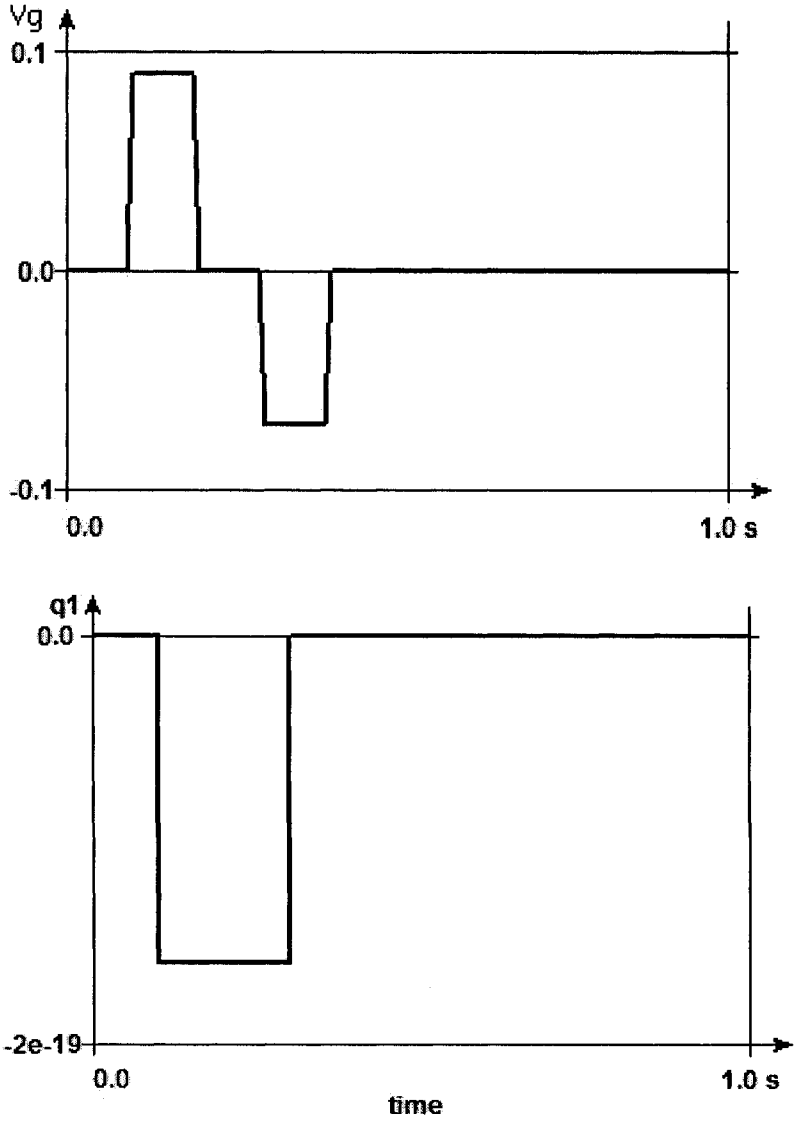

Fig 3.5 Simulation results of Electron-Trap with capacitances to ground

3.5 Some discussions

3.5.1 Discussion about voltage range

The above methodology of determining the parameters of the circuit for required behavior of memory cell applies to any number of junctions and initial charges in the island. A question to ask is: Is there a maximum value of V_g ? We take 3-tunnel Electron-Trap again for example (shown In Fig 3.2). When the voltage V_g increases from 0.25V to 0.4V, it is found that a second electron starts to tunnel from ground to N1. However, this additional electron goes back to ground as the voltage decreases to 0V. This is to say that the transport of the second electron is unnecessary. Therefore, the proper voltage range of V_g for this case is from 0.24V to 0.39V. Simulation results are given in Fig 3.6. Table 3.3 shows the approximate voltage range of V_g for Electron-Traps with different number of tunnel junctions.

Table 3.3: The voltage range of V_g for Electron-Traps with different number of tunnel junctions

Number of Tunnel junctions	Two	Three	Four	Five
Voltage range(V)	0.17-0.33	0.25-0.39	0.33-0.48	0.41-0.56

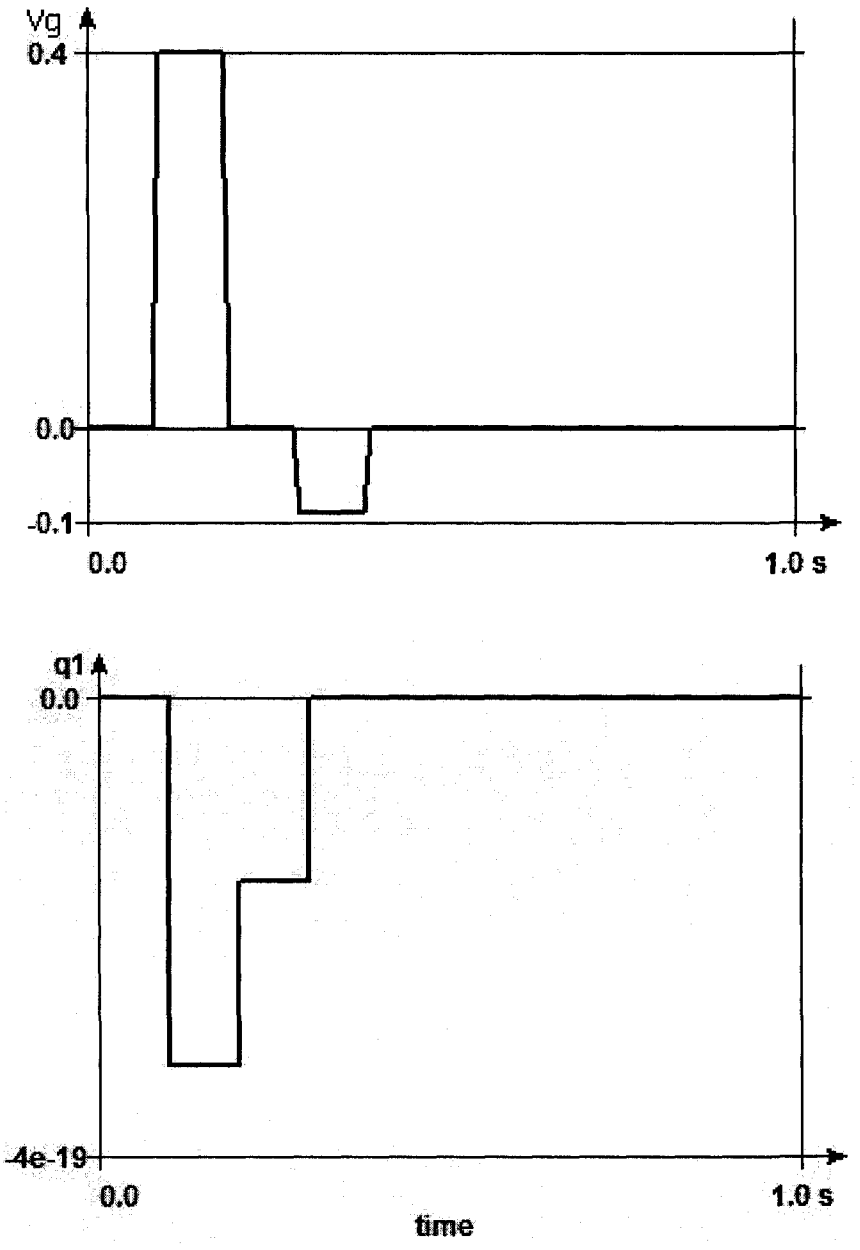

Fig 3.6: Simulation results in the case of $V_g = 0.4$

3.5.2 Discussion about the number of tunnel junctions

In this chapter, we use the Electron-Trap with 3 tunnel junctions as the example. As the number of tunnel junctions increases, the Electron-Trap memory cell shows better reliability in terms of its insensitivity to the Random Background Charge. However, if the number of tunnel junctions in the cell reduces to one, the electron at island N1 can not be held when V_g goes back to zero from a positive value. This means that at least two junctions are needed for the Electron-Trap to work as a memory cell.

In this chapter we introduced a design methodology that allows us to derive circuit parameters in an analytical way, assuming the topology and targeted behaviour are known. In the following chapter we utilize this method for the reliability analysis of SET Electron-Trap memory cells.

CHAPTER Ⅳ
RELIABILITY ANAYSIS

Background charge is one of the most serious problems with single-electronics, which could be caused by stray capacitances and impurities located near the circuit nodes. These background charges may be mobile and change over time, and are less likely to control with today's technology. Thus, the memory cell should be designed to tolerate certain amount of background charges for its reliable operation.

Section 4.1 presents reliability analysis of SET Electron-Trap memory cell, while the improved structure of Electron-Trap is discussed in Section 4.2.

4.1 Experiment on Electron-Trap

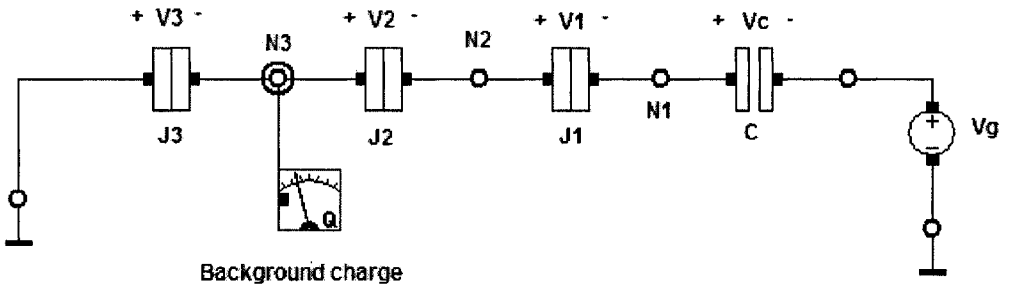

Fig 4.1: Three tunnel junctions Electron-Trap with background charge on island N3

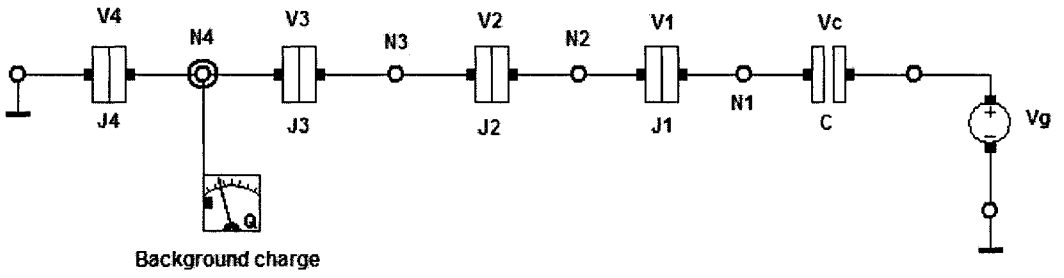

Fig 4.2: Four tunnel junctions Electron-Trap with background charge on island N4

When introducing background charge to the Electron-Trap memory cell with the structure of Fig 4.1 and Fig 4.2, it has been observed that they are not sensitive to positive background charge on any of the single islands. Therefore, we conducted the experiments on the reliability of the Electron-Trap by introducing negative background charges into the islands.

According to the above methodology, with the same parameters we use in section 3.3, the basic equations for 3 tunnel junctions Electron-Trap with background charge on island N3 (Fig 4.1) can be written as follows:

$$0 = C\ V_c - C_1 V_1 \tag{4.1}$$

$$0 = C_1 V_1 - C_2 V_2 \tag{4.2}$$

$$q_3 = C_2 V_2 - C_3 V_3 \tag{4.3}$$

$$-V_g = 0.25 = V_1 + V_2 + V_3 + V_c \tag{4.4}$$

$$V_{cri} = \frac{e}{2(C_e + C_j)} \quad (j=1, 2, 3) \tag{4.5}$$

The results show that the maximum background charge that the circuit can tolerate is -0.5e, where e is the elementary charge. Moreover, the voltage range is narrowed down to 0.25V-0.32V. It is clear that the existing of background charge limits the function of the circuit.

This situation can be improved by introducing more tunnel junctions to the circuit. For example, our experiments show that the Electron-Trap with 4 tunnel junctions (Fig 4.2) can tolerate the background charge up to -5.1e. In general, the more tunnel junctions are present in the Electron-Trap memory structure, the more reliable operation one can expect.

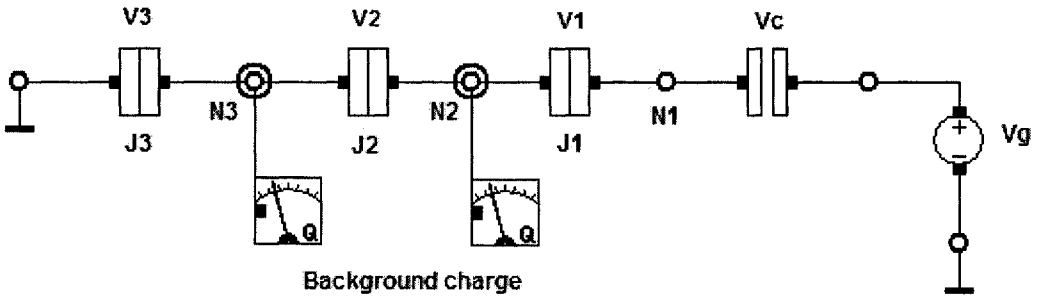

Fig 4.3: Three tunnel junction Electron-Trap with background charge on two islands

A question to ask is: What happens when background charge exists in more than just one island? We take 3-tunnel Electron-Trap (Fig 4.3) again for example. Both the islands N3 and N2 get background charge, in compliance with previous research, the maximum background charge that island N2 can tolerate is -0.2e, we can calculate that the range of background charge on island N3 is from -0.1e to 0.3e. We conclude that background charges could be anywhere of the circuit and affect each other.

4.2 Experiment on the improved structure of Electron-Trap

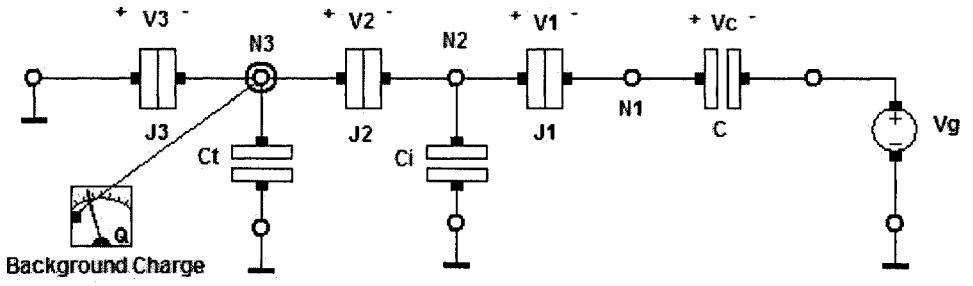

Fig 4.4: Improved 3 tunnel junctions Electron-Trap with background charge on island N3

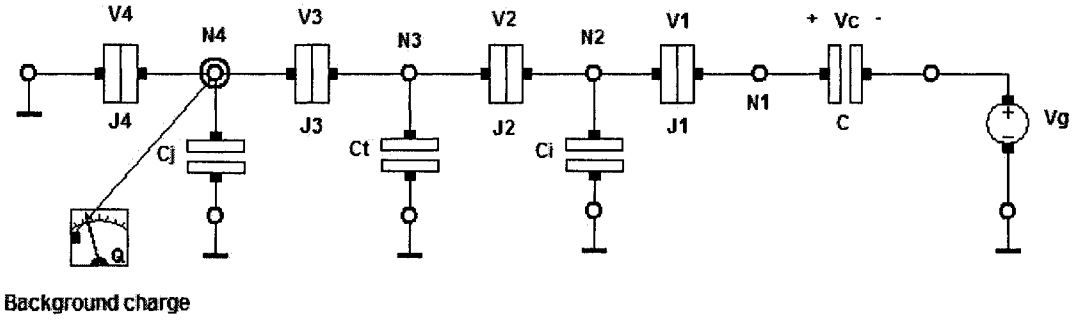

Fig 4.5: Improved 4 tunnel junctions Electron-Trap with background charge on island N4

We do the similar procedure and obtain that the maximum background charge that can be tolerated by improved 3 tunnel junctions Electron-Trap (Fig 4.4) is -1.2e, as while -6.1e for the structure of 4 tunnel junctions (Fig 4.5). Compared

with the structures of Fig 4.1 and Fig 4.2, the improved Electron-Trap shows better reliability.

CHAPTER V
CONCLUSIONS AND FUTURE WORK

5.1 Conclusion

In this thesis, we considered the design methodology for Single Electron Tunneling (SET) technology and reliability issues. Our overall investigation and achievements can be summarized as follows.

We investigated the design process of SET based Electron-Trap memory cell in which logic values are represented by single or few electrons. A design methodology was proposed that, given a circuit topology and the corresponding targeted behaviour, allows for the derivation of the circuit parameters in an analytical way. The methodology is based on the mathematical description of the tunnel junctions in the circuit, called the characteristic equations. It has been shown that the parameter selection is the key to the correct logic operation.

Moreover, we analyze the reliability of SET Electron-Trap memory cell by introducing Random Background Charge on the islands. Two structures of Electron-Trap were simulated and compared, we conclude that more reliable

behavior can be achieved by using more tunnel junctions in series in this particular cell structure.

The proposed methodology and reliability analysis are verified by means of simulation using SIMON, and all the calculation are verified by MATLAB.

5.2 Future Work

5.2.1 Investigation on different memory cells

Several different single-electron memory cells have been proposed, including SET Flip-Flop, Electron-Trap memory, SET Ring Memory, etc.

In this thesis, we used a rather simple and basic, though generally accepted, model of the SET phenomenon. The detailed design methodology and simulation results of Electron-Trap memory cell are presented. For the purpose of this research this model was sufficient, but as SET technology matures a more detailed model will be necessary. We suggest that these models are worked out in detail.

5.2.2 Reliability issue

The research on reliability issues of SET circuits involves two aspects, reliability analysis and reliability improvement.

The above reliability analysis assumes that Random Background Charge exists on just one or two islands. However, during fabrication process, background charges could appear on every island at the same time.

Reliability improvement, on the other hand, is to use various architectures or new encoding techniques to increase reliability.

These two aspects will be investigated in our future research work.

APPENDIX

Matlab Program for SET memory cells

In this thesis, all the calculations are verified by MATLAB. The following program shows the procedure for the proposed methodology in MATLAB.

Program for 4 tunnel junctions Electron-Trap memory cell:

```
clear
c=10^-18;
q=1.6*10^-19;
vcri=0.062;
vg=v;
[v1,v2,v3,v4,v5]=solve
('v1-v2=0*q/c',
'v2-v3=0*q/c',
'v3-v4=0*q/c',
'v4-v5=0*q/c',
```

'v1+v2+v3+v4+v5=vg');

v1=subs(v1)

v2=subs(v2)

v3=subs(v3)

v4=subs(v4)

v5=subs(v5)

If v5>vcri

Fprintf('electron tunnels from ground to island N4')

Else

Fprintf('no electron tunnels')

end

%given the input voltage $V_g = 0.33$, we obtain:

v1 =0.0660, v2 =0.0660, v3 =0.0660, v4 =0.0660, v5 =0.0660, one electron tunnels to N4.

[v1,v2,v3,v4,v5]=solve

('v1-v2=0*q/c',

'v2-v3=0*q/c',

'v3-v4=0*q/c',

'v4-v5=1*q/c',

'v1+v2+v3+v4+v5=vg');

If v4>vcri

Fprintf('electron tunnels from island N4 to island N3')

```
Else
   Fprintf('no electron tunnels')
end
%we get:
v1 =0.0980, v2 =0.0980, v3 =0.0980, v4 =0.0980, v5 =-0.0620, one electron
tunnels to N3.

[v1,v2,v3,v4,v5]=solve
('v1-v2=0*q/c',
'v2-v3=0*q/c',
'v3-v4=1*q/c',
'v4-v5=0*q/c',
'v1+v2+v3+v4+v5=vg');
If v3>vcri
   Fprintf('electron tunnels from island N3 to island N2')
Else
   Fprintf('no electron tunnels')
end
%we get:
v1 =0.1300, v2 =0.1300, v3 =0.1300, v4 =-0.0300, v5 =-0.0300, one electron
tunnels to N2.

 [v1,v2,v3,v4,v5]=solve
```

```
('v1-v2=1*q/c',
'v2-v3=0*q/c',
'v3-v4=0*q/c',
'v4-v5=0*q/c',
'v1+v2+v3+v4+v5=vg');
If v2>vcri
    Fprintf('electron tunnels from island N2 to island N1')
Else
    Fprintf('no electron tunnels')
end
%we get:
v1 =0.1940, v2 =0.0340, v3 =0.0340, v4 =0.0340, v5 =0.0340, one electron tunnels
to N1.

[v1,v2,v3,v4,v5]=solve
('v1-v2=1*q/c',
'v2-v3=0*q/c',
'v3-v4=0*q/c',
'v4-v5=0*q/c',
'v1+v2+v3+v4+v5=vg');
If v2>vcri
    Fprintf('electron tunnels from N1 to island N2')
Else
```

Fprintf('no electron tunnels')

end

% given the input voltage $V_g = 0$, we obtain:

v1 =0.1280, v2 =-0.0320, v3 =-0.0320, v4 =-0.0320, v5 =-0.0320, no electron tunnels.

```
[v1,v2,v3,v4,v5]=solve
('v1-v2=1*q/c',
'v2-v3=0*q/c',
'v3-v4=0*q/c',
'v4-v5=0*q/c',
'v1+v2+v3+v4+v5=vg');
If v2>vcri
   Fprintf('electron tunnels from island N1 to island N2')
Else
   Fprintf('no electron tunnels')
end
```

% given the input voltage $V_g = -0.17$, we obtain:

v1 =0.0940, v2 =-0.0660, v3 =-0.0660, v4 =-0.0660, v5 =-0.0660, the electron goes back to N2.

Program for 3 tunnel junctions Electron-Trap memory cell:

```
clear
c=1*10^-18;
q=1.6*10^-19;
vcri=0.06;
vg=v;
 [v1,v2,v3,v4]=solve
('v1-v2=0*q/c',
'v2-v3=0*q/c',
'v3-v4=0*q/c',
'v1+v2+v3+v4=vg');
v1=subs(v1)
v2=subs(v2)
v3=subs(v3)
v4=subs(v4)
end
```

%given the input voltage $V_g = 0.24$, tunnel event happens.

Program for 5 tunnel junctions Electron-Trap memory cell:

```
clear
c=10^-18;
q=1.6*10^-19;
vcri=0.067;
```

```
vg=v;
 [v1,v2,v3,v4,v5,v6]=solve
('v1-v2=1*q/c',
'v2-v3=0*q/c',
'v3-v4=0*q/c',
'v4-v5=0*q/c',
'v5-v6=-1.4*q/c',
'v1+v2+v3+v4+v5+v6=vg');
v1=subs(v1)
v2=subs(v2)
v3=subs(v3)
v4=subs(v4)
v5=subs(v5)
v6=subs(v6)
end
```

%given the input voltage $V_g = 0.41$, tunnel event happens.

Program for 3 tunnel junctions Electron-Trap memory cell with capacitances to ground:

```
clear
c=1*10^-18;
q=1.6*10^-19;
```

```
vcri=0.06;
vg=v;
 [v1,v2,v3,v4]=solve
('v1-v2=0*q/c',
'v2-v3+vi=0*q/c',
'v3-v4+vt=0*q/c',
'v1+v2+v3+v4=vg'
'vt=vg-v4'
'vi=vg-v4-v3');
v1=subs(v1)
v2=subs(v2)
v3=subs(v3)
v4=subs(v4)
vi=subs(vi)
vt=subs(vt)
end
```

Program for 4 tunnel junctions Electron-Trap memory cell with capacitances to ground:

```
clear
c=1*10^-18;
q=1.6*10^-19;
```

```
vcri=0.06;
vg=v;
 [v1,v2,v3,v4]=solve
('v1-v2=0*q/c',
'v2-v3+vj=0*q/c',
'v3-v4+vi=0*q/c',
'v4-v5+vt=0*q/c',
'v1+v2+v3+v4+v5=vg'
'vt=vg-v4'
'vi=vg-v4-v3'
'vj=vg-v4-v3');
v1=subs(v1)
v2=subs(v2)
v3=subs(v3)
v4=subs(v4)
v5=subs(v5)
vi=subs(vi)
vt=subs(vt)
vj=subs(vj)
end
```

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VITA AUCTORIS

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