TÍTULO

SUBSTITUTION OF ELECTROLYTIC CAPACITORS COMMONLY USED IN SOLAR INVERTERS BY FILM CAPACITORS SPECIFICALLY DESIGNED FOR THE APPLICATION

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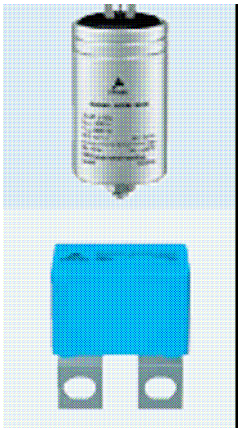

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Introduction

Capacitors are profusely used in photovoltaic systems as protecting elements for people and the equipment, also as filters and, more specifically, in the solar inverter in the so-called DC-Link position. The operation of the solar generators is certainly singular both in the environmental operating conditions but also in the electrical conditions that their subsystems must withstand during operation. On the one hand, they are usually subjected to strong variations and possible over-voltages. On the other hand, the high quality and reliability levels increasingly demanded by designers and final users of the equipments should be added to these special requirements.

Solar inverters are special equipments that must fulfil several functions in the solar generator, including of course DC-AC conversion, but also assuring output power quality, various protection mechanisms and system check. Additional requirements for these components, which are increasingly asked by final customers and developers are high efficiency and high reliability. These requirements have driven the inverter development towards more simple topologies and structures, lowering the number of components, and becoming strongly modular . But also a detailed study of the quality of the components used for the design implementation is required. This project will focus in a very particular component of the solar inverter: The DC-link capacitor.

Manufacturers usually decide to over-dimension their components. In many solar inverters, electrolytic capacitors are used due to their relatively higher density of capacitance, compared to other technologies (specially film capacitors). This directly increases the overall costs of the inverter. Film capacitors, on the contrary, offer high benefits in terms of operational stability and reliability, as well as very long lifetimes. All these features make the film technology extremely suitable for the new requirements implied by solar inverters and other equipments related to the use renewable energy sources.

The exact knowledge of the specific requirements of the photovoltaic systems, would definitely help to define and design an specific product adapted to solar applications, with optimal performance form the electrical and economical point of view.

The aim of this project is therefore to define clearly the conditions and operating demands of main capacitive components in the solar inverter. Once the main requirements of these products are collected and evaluated, a film capacitor of optimal performance will be specially designed. On the one hand, it will be necessary an extensive review of the different technical solutions used by manufacturers of solar inverters. On the other hand, the design rules used for film capacitors will also be reviewed and bring face to face with the different technical solutions used in the inverters. A most important part of this project will deal with the characterisation of the final product. In this respect, it will very important to establish the reliability parameters of the design and the estimated lifetime under the main operating conditions.

State of the art

2.1 The Solar Inverter

Photovoltaic systems are usually modular devices located close to electricity users. They commonly are used to feed a local need, but when connected to the grid, can revert the excess of energy to the utility network. Solar inverters are specifically required for this latter sake. There are several inverter technologies for this purpose (central inverters, string inverters, module integrated inverters…) They usually experience a wide range of input voltage variations due to the fluctuations of the photovoltaic generator. Simulation results show that the maximum output current of the inverter decreases by a constant factor with a decrease in the solar insulation. This constant factor is approximately given by $(V_s/V_{ms})^2$, where V_s is the generator voltage and V_{ms} is the maximum voltage of the solar generator [7].

Figure 1 shows a typical scheme of a general photovoltaic system. More practical designs will not require a battery, when the generator is directly connected to the grid. Some stand-alone PV systems (like the so called solar-home-system), will have an inverter either, for no further connection to the utility net is done. But note that stand-alone systems may also required of an inverter (like modular AC-coupled systems or small AC local grids).

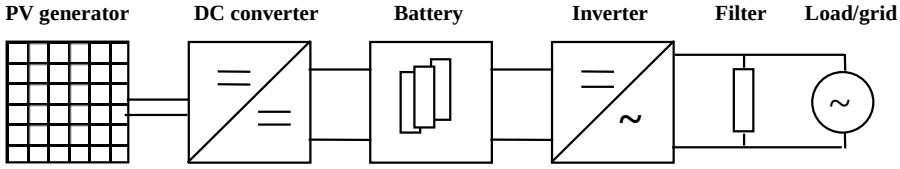


Figure 1. Block diagram of a general PV system

The solar inverter is a main component of photovoltaic (PV) systems, specially of those directly connected to the grid. It is in charge of converting the continuous electric signal originated at the modules into an alternating current with quality enough for injecting into the utility grid [31]. It is important to remark this last part since the efficiency of the inverter is mainly determined by the precision of the algorithm used for the conversion of the continuous (DC) into alternating current (AC). The utility manager and the suppliers have strong quality requirements for the injection of electricity into the grid. The fulfilment of these conditions is typically guaranteed by the solar inverter.

From all functions performed by the inverter, there are two of them that can be identified as key functions. Firstly, the inverter must perform a commutation step, followed by filtering of the signal. In the commutation step, the continuos signal is transformed in a square signal. This can be done thanks to power semiconductors, working in two distinct modes: shut and saturation. The filtering stage, in which a sinusoidal wave is reached, can be performed using power filters, which are basically LC circuits. In this constructions, the film technology are perfectly suitable for the capacitive part.

There are a number of operations of the solar inverters in the PV systems that differentiate them from a typical or standard inverter used in any other applications:

- Having a very high efficiency is even more crucial than other typical applications for inverters.

- Power conversion from variable DC voltage to variable AC voltage must be done as per the requirements of the local utility grid. The variable DC voltage can be higher or lower than the AC output voltage.
- Output power quality must be assured with low total harmonic distortion (THD), voltage and frequency deviation.
- The inverter usually includes the protection strategies of the PV generator and electrical power systems from abnormal voltage, current, frequency and temperature conditions, with additional functions such as anti-islanding protection (alternating part) and electrical isolation (continuous part), if necessary.
- The solar inverter typically implements monitoring function on the overall photovoltaic parameters of the system. In particular, tracking the maximum power point of the generator (MPPT) is usually included, for assuring an optimal efficiency of the modules.

This latter point is extremely important for photovoltaic applications, since direct connection to the array of modules imposes stricter power de-coupling restrictions to the single stage inverters than the connection through a maximum power point tracking (MPPT) control module, which is usually implemented by a DC-DC converter. The common challenge is, in any case, to extract the maximum energy from the sources under the variable conditions of the generator. In order to run the inverter at the maximum power, the circuit has to be able to adjust the input voltage according to the current irradiance conditions. This maximum power point is usually at the 70% of the power corresponding to the open voltage in the IV curve. Nevertheless the input voltage has to be adjusted dynamically, for example, with a boost circuit. A boost circuit is a DC converter whose output is at a higher voltage level than the input. The booster therefore adjusts the input voltage to the maximum power point, and the second stage of the inverter converts this DC signal into a sinusoidal grid-compatible voltage, and injects it into the utility.

Power de-coupling between the generator and the source is essential especially for a directly photovoltaic-fed single phase inverter system, since the power generated is constant at the maximum power point, whereas an ideal single phase AC load or grid demands a pulsating $2 \cdot f_{grid}$ instantaneous power. Most topologies use a large (< 1 mF) electrolytic capacitor placed at the input terminal of the inverter for power de-coupling. This is known to be one of the main limitation regarding volume and service life in photovoltaic systems. In more sophisticated designs [34], a DC power smoothing circuit is used, which reduces the voltage ripple at the DC-link bus. This allows to downsize the input capacitor to a dozen of micro farads, therefore being then possible to use film capacitors, with the consequent improvement in performance and reliability of the device.

Consequently with all these previous reasoning, a typical photovoltaic inverter has to satisfy a number of design characteristics [7]:

1. The PV system should not exceed 100V, otherwise specific insulation and protection strategies should be defined.
2. The current harmonic distortion (THD) fed to the grid by the solar inverter should not exceed the limit permitted by local utilities and/or authorities.
3. Care should be taken to control the radio interference generated due to the high frequency switching of the power devices in the inverter.
4. The solar plant should be disconnected from the grid at times of too low insulation.

5. The inverter should be equipped with a maximum power point tracker (MPPT) to be able to get the maximum power possible from the photovoltaic generator at any time.
6. During a power failure, an isolator should disconnect the inverter from the grid and connect it to an emergency load .

Inverters for grid connected and stand-alone systems have different requirements regarding the power flow direction, load characteristics and also grounding [31]. Normally, power flow in a grid connected system goes in the direction pointed from the power source to the grid; a unidirectional inverter can therefore be used. For stand alone systems with reactive loads, the inverters have to be tolerant of load-fed reactive current and transients by providing effective paths to the reactive energy. Controlled bi-directional inverters can also be useful in the case of grind interconnections with a local load.

2.1.1 Pulse Width Modulation

Modern solar inverters take advantage of pulse width modulation (PWM) techniques for converting the DC signal into a AC signal compatible to the utility grid. Although conceptually simple, PWM inverter systems are complex equipments (see Figure 2), comprising several sub-circuits [28]:

- An output voltage setting circuit for generating a pattern of output voltage value corresponding to a speed command value,
- An oscillator for generating a pulse train having a frequency proportional to the speed command value,
- A frequency division circuit for dividing the frequency of the pulse train produced by the oscillator to produce interrupt pulses,
- A pulse interval measuring circuit for measuring a pulse interval between predetermined ones of the interrupt pulses supplied from the frequency division circuit,
- An arithmetic unit responding to the input of the interrupt pulses from the frequency division circuit to produce a timing signal corresponding to the timing at which said interrupt pulse is inputted and update data associated with current operating phase relative to a fundamental wave, to thereby produce pulse width data corresponding to the result of multiplication of a value associated with the output voltage value supplied from the output voltage setting circuit,
- A value associated with the pulse interval supplied from the pulse interval measuring circuit
- A value associated with the operating phase relative to said fundamental wave,
- A pulse width conversion circuit supplied with the pulse width data from the arithmetic unit for producing a width pulse train conforming to the pulse width data at every timing signal supplied from the arithmetic unit,
- A waveform processing circuit supplied with the width pulse train from the pulse width conversion circuit and the timing signal from the arithmetic unit to produce sequentially phase output pulse trains.

The PWM of a signal or power source itself, involves the modulation of the input signal to either convey information over a communications channel or control the amount of power sent to the load or grid. The simplest way to generate a PWM signal is the intersective method, which requires only a sawtooth or a triangle waveform (easily generated using a simple oscillator) and a reference signal. In grid connected systems, this reference signal is the grid AC itself.

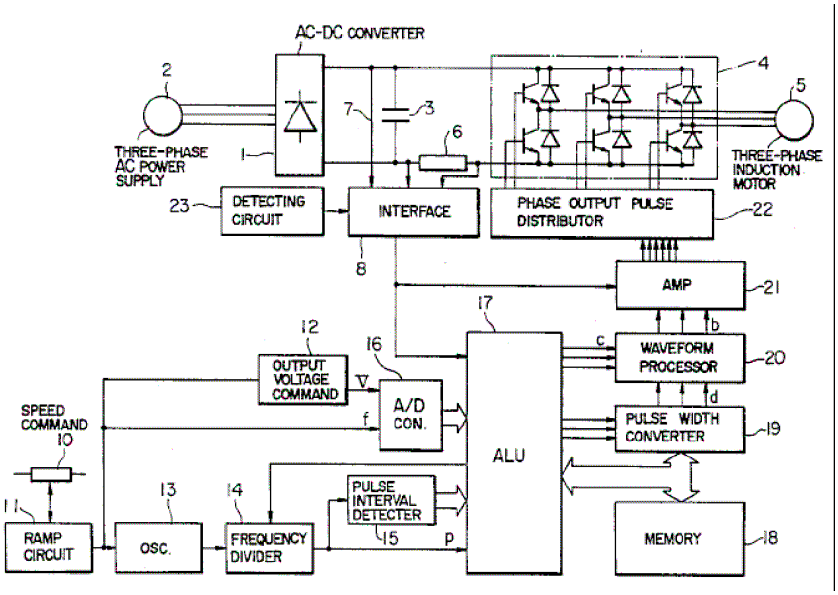


Figure 2. Block diagram showning a general arrangemets of a PWM DC-AC inverter system according to [28]

High frequency PWM power control systems are easily realisable with semiconductor switches. The discrete on/off states of the modulation are used to control the state of the switches which correspondingly control the voltage across or current through the load. The major advantage of this system is the switches are either off and not conducting any current, or on and have (ideally) no voltage drop across them. The product of the current and the voltage at any given time defines the power dissipated by the switch, thus (ideally) no power is dissipated for this system. Realistically, semiconductor switches such as MOSFETs or BJTs are non-ideal switches, but high efficiency controllers can still be built.

The main drawback of wide input range PWM-inverters is the high amplitude of the current al the lowest required input voltage, which leads to an expensive and large design. Also the switching ripple in the output waveform due to the limited switching frequency of the inverter calls for a complex filter. Another big problem is the output rectifier operating as the high DC-link voltage, which leads to high losses. For high performance converters, three possible solutions are given [18]:

1. A very high switching frequency in the initial stage, synchronised operation. In this case, the filter can be simplified. The main inconvenience is then the rising switching losses, which depend on the frequency.
2. A high order input and output filter, so that the switching frequency can be reduced. This leads to big volume and weight.
3. A multiphase PWM structure. In this case, the effective resulting switching frequency is the switching frequency of the partial power stages times the count of the output stages. The result is an inverter with reduced current stress in the input capacitor and a reduced filter in the output stage. In addition, due to the divided output current, the design is much easier to handle.

Recently advanced modulation techniques such as space vector modulation (SVM) have been introduced for inverter control. SVM enable better utilisation of the DC-link voltage than sine PWM [15], and losses are also reduced. For example, with minimum loss SVM techniques (MLSVM) each inverter leg is not switched during a third of the fundamental period. As a result, switching losses are significantly reduced. SVM is actually

based on the fact that output voltage space-vector can be expressed as a weighted average combination of the two adjacent active space vectors and the zero state vectors (2 states in which the DC-link is disconnected from the load) [17]. Different arrangements of the state sequences gives two common SVM techniques: symmetric SVM and minimum loss SVM. MLSVM uses only one zero state within each switching period. As a result, one of the switches is always on within a sector (the sixth of a period) resulting in a significant reduction of the losses. The level of switching losses reduction depends on the load displacement power factor (cos φ). Maximum reduction is reached if non-switched leg carries the highest phase current of the three ones. As cos φ gets lower, the highest current area is displaced with regards to the desirable sector area. However, at the same switching frequency symmetric SVM shows less output current harmonic distortion in the whole modulation index range than MLSVM.

In the particular case of stand-alone solar inverters, another significant advantage is the improvement in case of partial load. One possible solution is to reduce dynamically the number of switching output stages depending on the load. The result is a significant increase in the inverter efficiency in case of weak loads, compared to the conventional PWM inverter topologies. The new topology can be derived form the standard version, only two additional switches are necessary. A definite advantage of the modified version is the split rectifier, which leads to loss reduction of the switching diodes in the DC-link path [18].

New trends in inverter designs points to modular structures, for reducing costs and increasing reliability, two main point of concern of developers for inverters. Small transformer-less AC modules can be use to decompose a multilevel inverter system accommodating a wide range of input voltage variations and a large power capability. Incorporation of adaptive and intelligent control techniques allow the treatment of a wide range of input fluctuations for extracting the maximum power from the PV generator. Soft-transition and zero current transition techniques have been developed to minimise and eliminate both switching losses and stresses, thus improving converter efficiency. Currently proposed soft-switched converters are based in buck inverters. Their main drawback is however the higher cost (due to the additional power components) and increased control circuit complexity. They have a promising future, though.

2.1.2 Protection strategies

Grounding is necessary when considering maintenance, safety, lightning, electromagnetic coupling diminishment and electromagnetic pulses protection [31]. In most cases, an isolation barrier between the solar cells and the power grid is required which is mostly realised by a DC-DC converter. A major problem is the nominal capacitance of the input capacitor, which is connected in parallel to the solar generator. This can lead to a system where most of the energy can be stored in the DC-link capacitor operating at a higher voltage range which leads to significantly smaller (and therefore cheaper) capacitors. In those cases, film technology is usually the best option. The constant power flow can be achieved by a controlled voltage ripple in the DC-link. Besides, the use of a multiphase concept, leads also to a further reduction of the input DC-current ripple . Each output stages switches at 80 kHz with a phase delay of 45° to the previous one. The maximum peak current can be significantly reduced, therefore reducing the costs of the final product and, allowing film technology, increasing the lifetime of the inverter.

2.1.3 Evolution of solar inverters.

The classical design for solar inverters is based on centralised inverters that interfaced a large number of PV modules to the grid. The PV modules are usually divided into series connections called *strings*. Each string generates sufficient voltage for avoiding further amplification. These series connections is then connected in parallel, through string diodes in order to reach high power levels (see Figure 3). This centralised inverter includes some severe limitations, such as high-voltage DC cables between the PV modules and the inverter, power losses due to a centralised MPPT, mismatch losses between the PV modules, losses in the string diodes, and a non-flexible design where the benefits of mass production could not be reached. In the first designs, the grid-connected stage was usually line commutated by means of thyristors, involving many current harmonics and poor power quality. The large amount of harmonics was the occasion of new inverter topologies and system layouts, in order to cope with the emerging standards which also covered power quality.

Present technology consists of string inverters and AC modules [19], whose sketches are also included in Figure 3. The string inverter, is a reduced version of the centralised inverter, where a single string of PV modules is connected to the inverter. The input voltage may be high enough to avoid voltage amplification. For European systems, this requires roughly 16 PV modules in series. The total open-circuit voltage for 16 PV modules may reach as much as 720 V. The normal operation voltage is, however, as low as 450 - 510 V. The possibility of using fewer PV modules in series also exists, if a DC–DC converter or line-frequency transformer is used for voltage amplification. There are no losses associated with string diodes and separate MPPTs can be applied to each string. This increases the overall efficiency compared to the centralised inverter, and reduces the price, due to mass production.

Future designs for inverters in solar applications seem to point out to multi-string inverters, where several strings are interfaced with their own DC–DC converter to a common DC–AC inverter. This is beneficial, compared with the centralised system, since every string can be controlled individually. Thus, the operator may start his/her own PV power plant with a few modules. Further enlargements are easily achieved since a new string with DC–DC converter can be plugged into the existing platform. A flexible design with high efficiency is hereby achieved.

The AC module is the integration of the inverter and PV module into one electrical device: It removes the mismatch losses between PV modules since there is only one PV module, as well as supports optimal adjustment between the PV module and the inverter and, hence, the individual MPPT. It includes the possibility of an easy enlarging of the system, due to the modular structure. The opportunity to become a “plug and- play” device, which can be used by persons without any knowledge of electrical installations, is also an inherent feature. on the other hand, the necessary high voltage-amplification may reduce the overall efficiency and increase the price per watt, because of more complex circuit topologies.

Finally, still to fully develop is the AC cell inverter concept, in which one large PV cell is connected to a DC–AC inverter. The main challenge for the designers is to develop an inverter that can amplify from a very low voltage, (~1.0 V) and 100Wper square meter, up to an appropriate level for the grid, and at the same time reach a high efficiency. For the same reason, entirely new converter concepts are required.

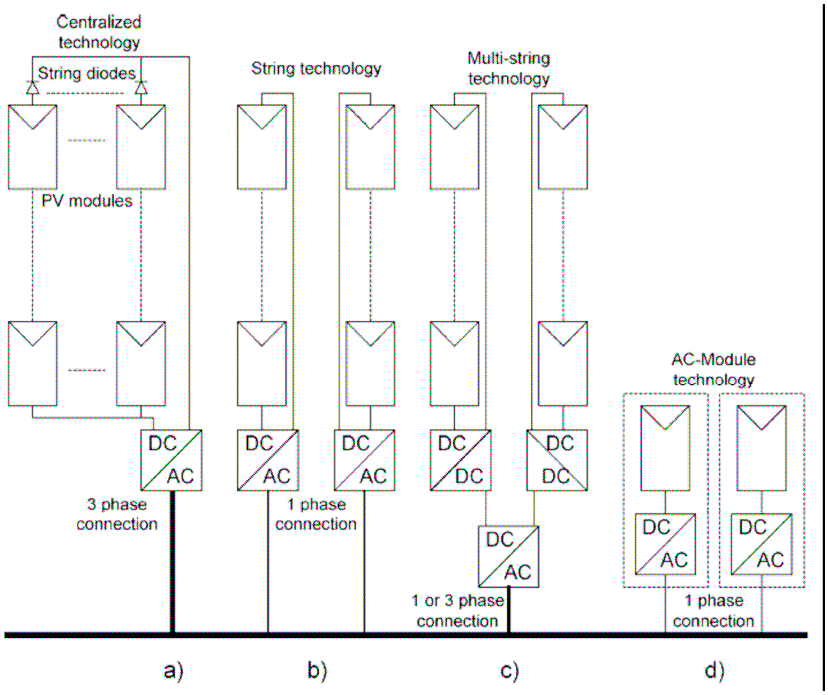


Figure 3. Historical evolution of PV generator designs, going from the classical centralised technology to the most modern AC-modules. Figure taken from [19].

2.1.2 Classification of Solar Inverters.

There are several ways of classifying the different topologies and technologies of inverters currently available in the market. We will go over the main differences, but a very complete review on this topic can be found on [6].

Based on the electrical isolation between input and output, inverters cane be classified as isolated inverters or non-isolated inverters. This electrical isolation is usually achieved using transformers, but a choice can be made using line-frequency transformers, or high frequency transformers. Depending on this, the DC-link voltage may vary in a wide range. According to the input DC voltage, in comparison to the output AC voltage, inverters can be buck inverters, boost inverters, or buck-boost inverters. Figure 4 shows the traditional (single phase) buck inverter with a line frequency transformer. This design results in overall low cost and high efficiency, together with robust performance and high reliability. These are the reasons why this topology is often used if performance requirements are high. The main drawback of such design is the high volume and weight. And this is the main reason why high-frequency transformers or transformer-less design are increasingly replacing more traditional designs like the one in Figure 4. The main inconvenient for transformerless topologies are their limitations in power capacity, their compromised output quality, and limited operation range imposed to DC sources. It is observed in such inverters certain lack of control in the output current. Increasing the power will lead to excessive peak current stresses on the power switches.

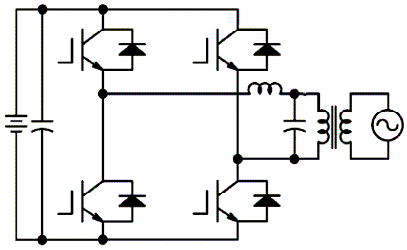


Figure 4. Traditional design of buck inverter with an electrolytic DC-link capacitor.

Single stage buck-boost inverters use DC inductors for energy storage or fly-back transformers for both energy storage and electrical isolation as required for safety reasons. A distinctive feature of these topologies is the elimination of low frequency transformers, presenting therefore a more compact design with a good performance-cost ratio compared to more conventional buck inverters with line-frequency transformers

Another classification of inverters distinguishes between single-stage and multiple-stage inverters. A single inverter is usually defined as an inverter with only one stage of power conversion for both stepping-up the low DC voltage and modulating the sinusoidal load current or voltage. Based on the number of power switches, single-phase inverters can be classified as four-switch topologies or six-switch topologies. For each of these two possibilities, several topologies can be found in the literature and in the industry [6]. In general, additional switches compared to four-switch topologies facilitate the grounding of both the grid and PV modules. Multiple-stage inverters are often used in applications where high power, high performance and wide output voltage range are required.

A multiple-stage inverter is defined as an inverter with more than one stage of power conversion, in which mostly one or more stages accomplish voltage step-up or step-down or electrical isolation, and the last step performs DC-AC conversion. Multiple stage inverters are listed as:

1. DC-DC-AC topologies
2. DC-AC-DC-AC topologies
3. DC-AC-AC topologies

In these inverters, boost and isolation are carried out in the first DC stage while inversion is conducted in the second. Each stage can be controlled individually or synchronously. For the buck or boost operation, either a DC-DC converter or a DC-AC-DC converter can be used. For the choice of the DC-link, the system can be configured with a DC-link followed by a pulse width modulation inverter or a pseudo DC-link followed by a line frequency operated inverter.

2.1.2.1 DC-DC-AC topologies

The simplest two stage boost inverter can be built by adding a DC-DC converter at the input of a buck inverter. In this structure, and elevated DC voltage with tolerable ripple is obtained in the first stage, and- in the second- a high frequency pulse width modulator is used for obtaining the AC signal. The large intermediate DC-link capacitor can be saved if the topology is slightly changed, introducing a rectified sine wave at the DC-link [9].

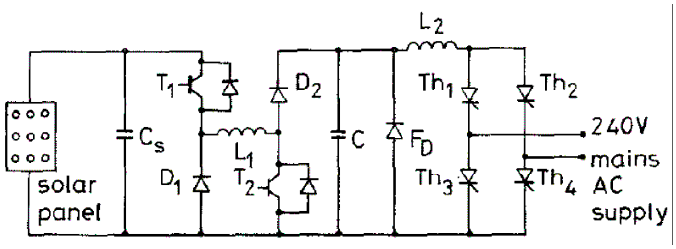


Figure 5. Novel configuration for grid connected solar photovoltaic inverter [7].

A slightly more complicated design is shown in Figure 5 [7]. This is a buck-boost inverter designed for PV grid connected applications, and with a DC input voltage of no more than 100V due to safety reasons.

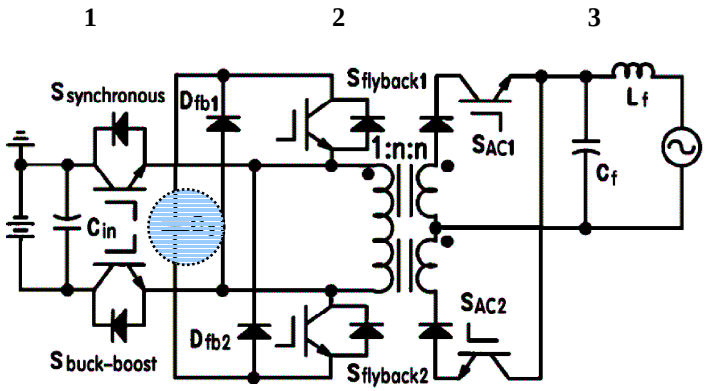


Figure 6. Innovative topology of solar inverter with a small intermediate DC-link film capacitor (C_S).

A further step is introduced in the isolated fly-back buck-boost inverter by Shimizu et al. [10] (see Figure 6). The constant input power, required by the maximum power point tracking (MPPT) control is processed in the first part of the switching cycle by the buck-boost converter and energy is stored in the intermediate capacitor (1). The energy stored in the magnetising inductance is, in the third stage, transferred to the secondary side of the transformer and injected into the single-phase grid by the AC switches through an LC filter (3). Thus, the intermediate capacitor is used as an energy buffer, where the voltage across it is composed of a DC component and an AC component alternating twice the frequency of the load (i.e. 100/120 Hz). The benefit of this topology is that a small intermediate film capacitor (C_S, in the shadowed region) can be used instead of a large electrolytic, with the consequent improvement in the service life of the inverter.

Innovative designs use parallel filter capacitors (2x22 μF, 500V) for intermediate energy storage [11]. The DC bias of this capacitors is controlled in such a way that the current or power drawn from the PV modules is almost constant, i.e. without low frequency ripple. Hence, the energy can be stored in high voltage film capacitors when the instantaneous power generated is higher than the power injected in the grid, and taken out of the same capacitors when the power from the PV is lower than required power by the load.

2.1.2.2 DC-AC-DC-AC topologies

This topology can be subdivided in terms of the kind of DC-link used. In both cases, they normally consist of a high frequency DC-AC-DC converter for getting a controlled DC voltage from a variable input, and of a high frequency or line-frequency inverter for the required AC output.

1. DC-link between two stages

This is the most traditional topology, using high step-up transformer, a rectifier and a DC filter are also included. Both stages operate at high frequency, resulting in high losses and high cost.

2. Pseudo- DC-link between two stages.

This is a multi-stage inverter with a pulse width modulation DC pulse train, consisting of multiple pulses whose widths distribute in a sinusoidal or semi-sinusoidal way repeating in half of an AC output period. It is remarkable that as compared to previous topology, the filter components are eliminated, but an output low-pass filter is still needed to ensure an

acceptable total harmonic distortion of AC output. Such configuration is found, for example in old 10 kW inverters commercially developed by the General Electric Company [8]

2.1.2.3 DC-AC-AC topologies

For standalone or autonomous systems, a bi-directional power flow is required in the inverter control. In this case, provisions must be provided for the power to flow from the output side to the input side.

2.1.3 The DC-link position

Figure 4 and Figure 5 show simplified diagrams of two phase solar inverters. According to those diagrams, only one capacitor is needed in the purely inverter stage. Strictly speaking, even this capacitor is redundant because it is connected in parallel with the solar generator. The main concern of this project is to establish why and what type of capacitor can be best used at this position. To answer this, it is obviously necessary to gain perfect knowledge of the inverter switching mechanisms and circuit parasitic components.

The synthesis of a smooth sinusoidal current for the connection to the general network needs to have high rate of switching in different combinations of the inverter switches so that the output current can track the desired sinusoidal current to reduce the ripple content. This ripple is a function of the DC voltage, circuit inductance, and the switching period. The switching frequency in today's insulated-gate-bipolar-transistor (IGBT) based inverter is in between 10 kHz and 20 kHz. The ripple current of the two or three phase leg sum together, being able of seriously damaging the generator and any other element added to the circuit (i.e. batteries). The bus capacitor is therefore needed for absorbing the ripple due to the switching.

Most usual solutions of inverters take advantage of the space vector modulation scheme (SVM), with which one phase keeps un-switched over one sixth of the line cycle (in six switch topologies), while the other phases are switching at a pre-calculated duty cycle pattern to ensure a sinusoidal current output.

At the end, we will find that the DC bus capacitor is in fact a most important passive component in a solar inverter [37]. In particular, it is the element restricting and defining the overall lifetime of the final product. The most traditional designs use an electrolytic capacitor, but several new developments already point out to the advantages of using film technology for this position [9, 12, 11, 34, 35, 36, 37,38]. With this more sophisticated option, significant results are obtained concerning:

1. The ripple current due to the inverter switching
2. Voltage fluctuation due to the generator
3. Possible voltage transient due to leakage inductance and fast device switching

If electrolytic capacitors are to be used, then special designs should be considered taking into account:

4. Introduction of diodes in order to avoid current inversion, that may eventually destroy the capacitor.

If film technology is considered, on the contrary, this costly requirements are not needed, and only special attention should be paid to the existence of over voltage during operation due to self-healing. As it is explained in Section 3.5, this is the ability to clear

faults, such as pores or impurities in the film, under the influence of a voltage. Although it produces instantaneous increases of current, that must be taken into account when designing the circuits. This characteristic of the film capacitors is indeed a positive feature, for it leads to much more robust and stable products, as will be explained in the mentioned section.

The capacitance needed to deal with the first three matters of concern may not be high, but the pulse handling capability and frequency response of the capacitor are the major concerns. For the self-healing, if the generator is directly connected to the capacitor, the capacitance value is not an issue. The overall design should focus on the current handling capability in a wide temperature environment.

Traditionally, the size of the DC-link capacitor has been chosen in an arbitrary basis. The design philosophy with high capacitance electrolytic capacitors is typically inherited from the design of industrial drives, where the capacitance is calculated to smoothening the 6^{th} harmonic ripple caused by the utility line. The size of the capacitor can be calculated in terms of the power supplied by the solar generator [19] as

$$C = \frac{P_{PV}}{2\,\omega_{grid}\,U_c\,\hat{u}_c}, \qquad (2.1)$$

where P_{PV} is the nominal power if the PV modules, U_c is the mean voltage across the capacitor, and $\hat{u}_c$ is the voltage amplitude of the ripple current. This equation is based on the fact that the current from the PV modules is pure DC, and that the current from the grid connected inverter follows $sin\ 2(\omega_{grid}\,t)$ waveform, assuming that U_C is constant. Note that all these assumption are only approximately fulfilled in a real system.

According to simulations [12], the need for smoothing the 6^{th} harmonic is no longer necessary if a battery is used in between the generator and the inverter, and the capacitor selection criterion should now be focused on the current handling capability but not the voltage ripple.

Besides ripple current handling capability, there are several important features that need to be required to the DC-link capacitor:

- Operating temperature range from –55°C to 105°C
- Dielectric strength
- E.S.R.: 0.003 W tested at 10kHz, 25°C
- E.S.L. (typical): 21 nH
- Peak current (maximum): 9818 A

In fact, integration imposes strong compactness requirements on the DC-link capacitor. In transformerless topologies, it is the DC-link capacitor that account for a major fraction of the volume, weight and also cost of an inverter. Both capacitor rating and inverter losses depend heavily on ambient temperature, thus both loss reduction and thermal management are of special importance.

Temperature is in fact a matter of concern if film capacitors are to be used. Besides the greater capacitance/volume ratio, electrolytic capacitors ambient temperature can go up to 105°C [26], while a traditional film capacitor designs will withstand 85°C. Film capacitors will work up to 105°C only with a certain de-rating, which as we will be showing later, can be reduced thanks to optimised production process. Moreover, service life is reduced almost by

half every 10-15°C increase. Typical running temperature of a drive is 65°C [12] , but this may increase in some designs typical to 85°C. Although some designers have considered the control of operating temperature by a cooling system, the optimal film capacitor solution should be able of working at reasonable voltages at 100°C without considerably reducing the overall service life of the inverter.

Thus, at this point, we can identify two main drawbacks for film technology, which need to be tackled in the sake of doing the technology more competitive against other possible solutions. These are namely:

- Density of capacitance,
- Temperature performance.

On the other hand, it is well known the limited life expectancy of electrolytic capacitors, due to the tendency of the electrolyte to dry out after 10,000 hours usage. Substituting the bulky electrolytic capacitor by a film capacitor improves as mentioned above will overcome this shortage.

2.1.4 Capacitors in the inverter.

In addition to the DC-link, there are some other capacitors that are traditionally used in an inverter to deal with parasitic components and switching problems. Take the parasitic inductance as an example. Physical size constraint makes it nearly impossible to eliminate parasitic inductance in a high power inverter.

A DC snubber capacitor is usually added across the top and bottom DC rails on each phase leg to suppress the voltage spike locally. The requirements for this capacitor are high peak current capability and extremely low inductance (i.e. ranging from 10's to 100's nH). The leakage inductance and its interconnect inductance of the snubber capacitor should be at least one order of magnitude less than the lumped parasitic inductance, otherwise it will defeat the purpose of voltage spike suppression. When electrolytic capacitors are used as DC-link, the use of a snubber capacitor is unavoidable because the parasitic inductance of the electrolytic is quite significant. However, with the use of a low-inductance film capacitor and an appropriate PCB layout, it is also possible to eliminate the snubber capacitor [12].

Capacitors are also used as protection and filters at the input and output of the inverter. X2 and Y2 are typical protection functions that film capacitors usually carry out in industrial drives and inverters [29].

According to the UL 1741 [31], standard for inverters for use with distributed energy resources, all capacitors in the inverter should comply with standard UL 810 [32]. In general, power capacitors should comply with the IEC standard 1071 for power capacitors [33]. Filtering positions should also comply with more specific standards [29].

Film capacitors

A capacitor is an electrical passive component whose basic function is energy storage. This is achieved thought the confinement of certain amount of charge at a given voltage. Film capacitors are capacitors where the dielectric is a base plastic film, and the electrode is either a thin metal film on the top of the base film, or a thin metal coating deposited on the base film.

There are several ways of characterising a film capacitor, depending on the base film used, the design rules followed or the technology applied in its production. Figure 7 gives an overview of different film arrangements and dielectric, that will be described in later sections. The basic distinction between metallized films (MKT, MKP, MKN) and metal foil plus plastic film (MFT, MFP) is clearly depicted in following diagram. Figure 8 is also clarifying in this respect.

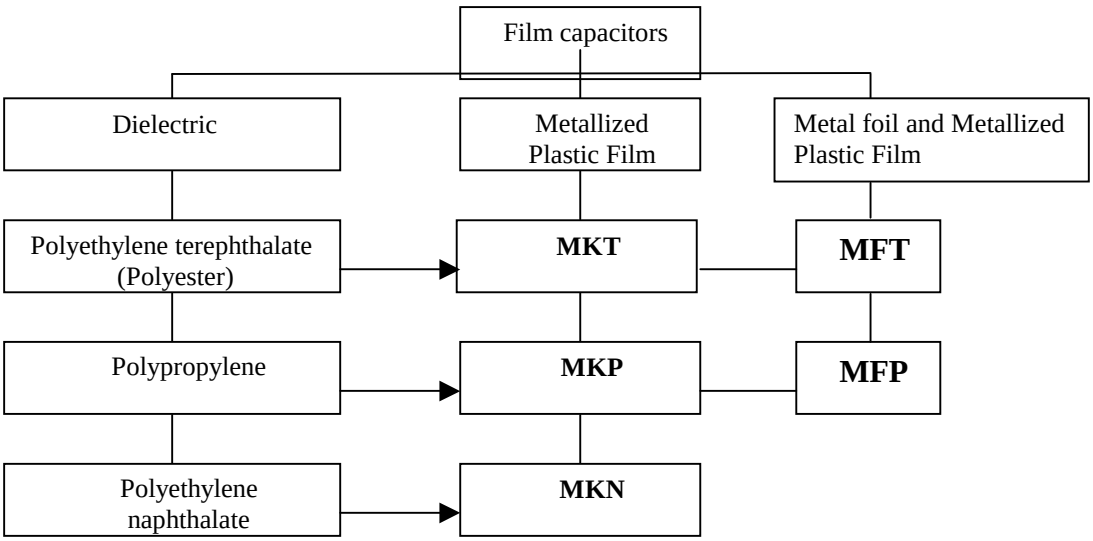


Figure 7 Classification of film capacitors according to DIN 41 379

Many of the information shown in this chapter are extracted from EPCOS Film Capacitors databook [4], where detailed information about this other technologies and products can be found.

3.1 Classification of film capacitors:

3.1.1 In terms of the base dielectric used.

The characteristics and application possibilities of film capacitors are effected so strongly by the dielectric used that the capacitors are grouped and designated according to the type of dielectric. Short identification codes for the type of construction, describing the dielectric and the basic technology applied, are defined in the standard DIN 41 379. This is actually the code used in Figure 7. The last character in the short code indicates the type of dielectric:

$T \rightarrow$ Polyethylene terephthalate (PET)
$P \rightarrow$ Polypropylene (PP)
$N \rightarrow$ Polyethylene naphthalate (PEN)

Due to Historical reasons, an "*MK*" (for Metallised plastic) is prefixed to the short identification code of capacitors with metallized films, while "*MF*" (for Metal foil) is prefixed for the design that uses a metal foil in between base dielectric plastic films.

The following table summarises the most relevant technical data of the base film typically used for the production of film capacitors:

TABLE 1: Characteristics of plastic film dielectrics (generalised typical values).

	PP	PET	PEN
Dielectric constant (ε_r)	2.2	3.2	3.0
C drift with time ($i_z=\Delta C/C$)	3%	3%	2%
C Temperature coefficient α_c [10^{-6}/K]	-250	+600	+200
C humidity coefficient β_c (50%...95%) [10^{-6}/%r.h]	40…100	500…700	700…900
Dissipation factor (1kHz)	0.0005	0.0050	0.0040
Time constant [s]	100.000	25.000	25.000
Dielectric absorption [%]	0.05	0.2	1.2

3.1.2 Classification in terms of the film arrangements

In order to provide a better understanding of the differences in the internal structure of the capacitors, Figure 8 shows some typical film and foil arrangements.

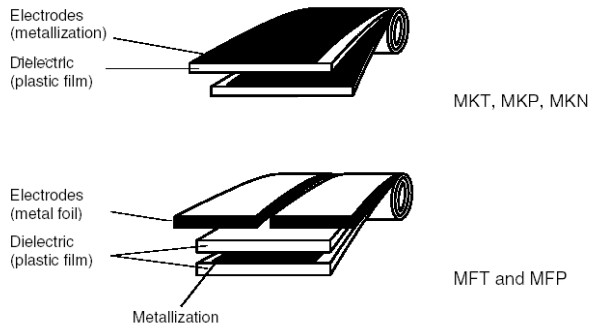


Figure 8 Examples of typical film and foil arrangements

The relation between various foil and film arrangements and the capacitor types is more clearly shown in Figure 9. Again the distinction between metallized film and metal foil construction is done:

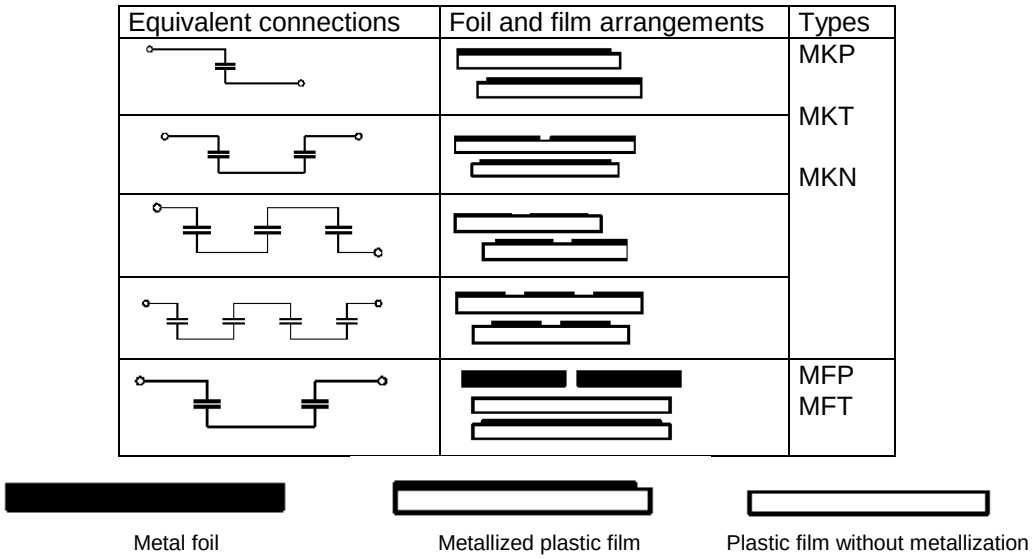
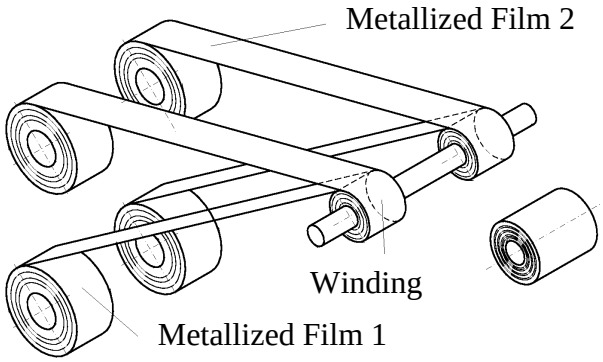


Figure 9 Schematic foil and film arrangements of various capacitor types

3.1.3 Classification in terms of construction

Power film capacitors are produced using the so called **wound** technology. In this production process, the capacitors are made by individually rolling the metallized films or the film/foils into cylindrical rolls and then covering them with an insulating sleeve or coating.



An alternative production process for film capacitors is the so called **stacked** technology [4]. This is done by winding big wheels of metallized film that is latter cut in smaller capacitors. At the end, one obtains a series of hundreds capacitors in parallel, which make this technology extremely appropriate for pulse applications, but inappropriate for power applications.

3.2 Electrical characterisation.

3.2.1 Equivalent circuit diagram

Any real capacitor can be modelled according to the following schematic ideal circuit:

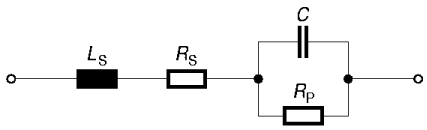


Figure 10. Real capacitor model.

Where the different elements represent:

C	Capacitance
R_S	Series resistance, due to contacts (leads, sprayed metal and film metallization)
R_p	Parallel resistance due to insulation resistance
L_S	Series inductance

Note that C, R_S and L_S are magnitudes which vary in the domain of frequency (AC) while R_p is a magnitude defined in DC (insulation resistance). In the next sections, all these magnitudes will be studied next in detail.

3.2.2 Capacitance

3.2.2.1 Rated capacitance / measuring conditions

Capacitance is a measure of the amount of electric charge stored for a given electric potential. The capacitance can also be understood as the amount of electrically charged carriers that a capacitor can store per unit of voltage.

The **rated capacitance C_R** of a capacitor is the value for which it is designed, and which is indicated upon it. Capacitance is measured under standard conditions in accordance with IEC 60068-1. In case of doubt, stricter reference conditions are defined in sub-clause 5.2 of the same specification.

Measuring conditions	Standard conditions	Reference conditions
Temperature	15°C...35 °C	(23 ± 1) °C
Relative humidity	45% ... 75%	(50 ± 2) %
Ambient atmos. Pressure	86 kPa...106 kPa	86 kPa...106 kPa
Frequency	1 kHz	1 kHz
Voltage	0,03 x V_R (max. 5 V)	0,03 x V_R (max. 5 V)

Any real capacitor has a certain **capacitance tolerance,** which is the permissible relative deviation of the real capacitance from the rated value. The measuring conditions are the same as for the rated capacitance. In normal operation, the capacitance drift of the capacitor during its lifetime should be within its tolerance. In this respect, as we will see in next sections, there are several factors affecting the actual value of the capacitance measured on any real capacitor.

3.2.2.2 Variation of capacitance with temperature

The capacitance will undergo a **reversible change** within a range of temperatures between the upper and lower category temperatures. The gradient of the capacitance versus temperature curve is given by the **temperature coefficient α_c** of the capacitance, which is usually defined as the average capacitance change, in relation to the capacitance measured at (20 ± 2)°C, occurring within the temperature range T_1...T_2. It is expressed in units of 10^{-6}/K.

$$\alpha_C = \frac{C_2 - C_1}{C_3 \cdot (T_2 - T_1)}, \quad (3.1)$$

being:

- C_1 Capacitance measured at temperature T_1
- C_2 Capacitance measured at temperature T_2
- C_3 Reference capacitance measured at (20 ± 2)°C

The temperature coefficient is essentially determined by the properties of the dielectric, the capacitor construction and the manufacturing parameters. Polypropylene capacitors have negative temperature coefficients, polyester capacitors have positive temperature coefficients (see Table 1).

Usually, the reversible changes of capacitance with temperature are expressed as ΔC/C. Figure 11 shows typical temperature characteristics of different capacitor types.

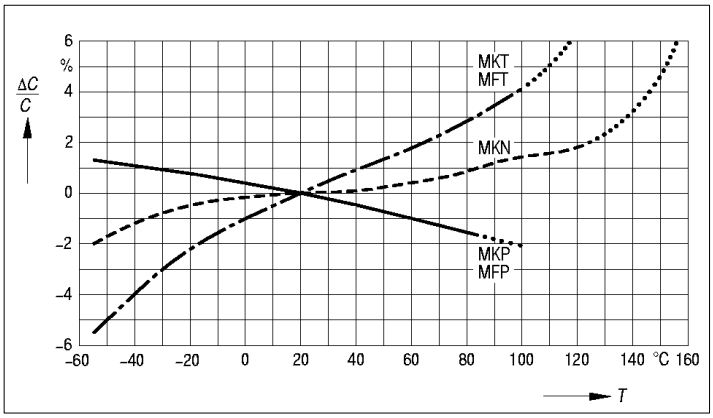


Figure 11. Relative capacitance change ΔC/C versus temperature T (typical values)

If a capacitor is subjected to a temperature cycle from the reference temperature to T_{min}, then up to T_{max} and back to the reference temperature, a small **irreversible change** may be observed between the initial and the final capacitance (cf. Figure 12). This aging is designated as the **temperature cyclic capacitance drift**, and is expressed as a percentage of the reference capacitance. For film capacitors it is usually very small.

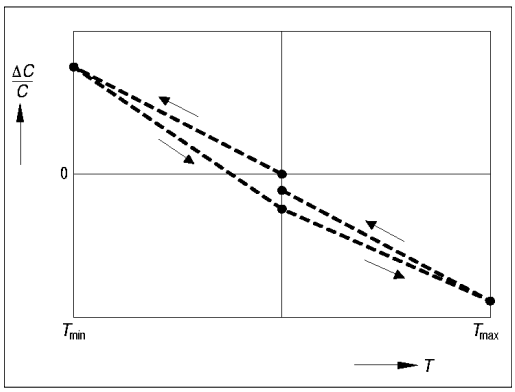


Figure 12. Capacitance change versus temperature (schematic curve)

Generally, when making the measurements of the cyclic capacitance drift, it must be taken into consideration that every temperature change is accompanied by a relative humidity change, which will affect the measurement (as described in section 3.2.2.3). The changes caused by the humidity variations remain within the scatter limits specified for α_c if measurements are carried out under standard conditions and the temperature cycles are not too long.

3.2.2.3 Variation of capacitance with humidity

The capacitance of a plastic film capacitor will undergo a **reversible change** of value in relation to any change in the ambient humidity. Depending on the type of capacitor design, both the dielectric and the effective air gap between the films will react to changes in the ambient humidity, which will thus affect the measured capacitance.

The **humidity coefficient** β_c is defined as the relative capacitance change determined for a 1% change in the humidity (at a constant temperature).

$$\beta_C = \frac{2 \cdot (C_2 - C_1)}{(F_2 - F_1) \cdot (C_2 + C_1)}, \qquad (3.2)$$

where C_1 is the capacitance value at relative humidity F_1, and C_2 is the capacitance value at relative humidity F_2.

The values of β_c provided in Table 1 are valid for a relative humidity range of 50%...95%. At relative humidity below 30%, the humidity coefficient is relatively low. Wide variations are to be expected at relative humidity above 85%.

Figure 13 shows typical capacitance/humidity characteristics of the different capacitor styles.

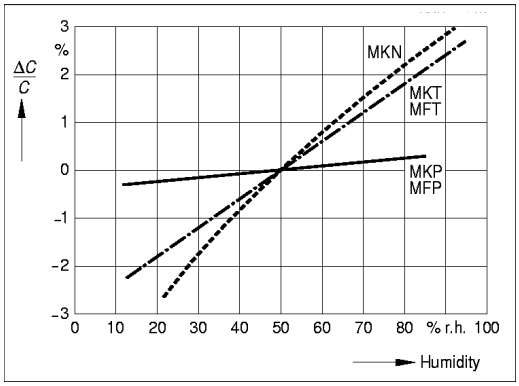


Figure 13. Relative capacitance change ΔC/C versus relative humidity (typical values)

An additional effect of humidity on the capacitor will be discussed later, when the so-called **corona effect** will be described. In this case, there must be a conjunction of AC voltage with humidity, leading under certain extreme conditions to an anomalous capacitance lost due to loose of metallization (active area).

3.2.2.4 Variation of capacitance with frequency

For polypropylene based capacitors, the capacitance remains virtually unaffected by the frequency up to 1MHz. For PET and, specially, for PEN capacitors, the effect of frequency is more noticeable:

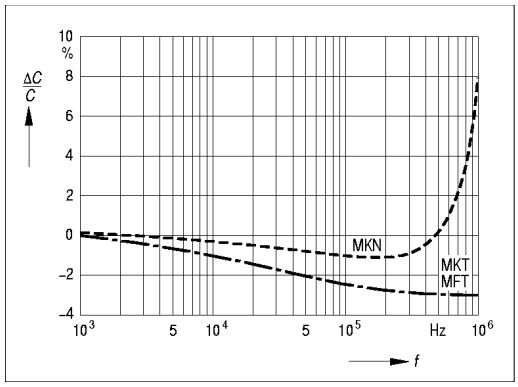


Figure 14. Relative capacitance change ΔC/C versus frequency (typical example)

Additionally, in the vicinity of the natural resonance frequency of the capacitors, the self-inductance leads to an additional decrease of the impedance. This has the same effect as an increase in the capacitance (refer to section 3.2.6).

3.2.2.5 Variation of capacitance with time

In addition to the changes described, the capacitance of a film capacitor is also subjected to irreversible changes known as drift, $i_z = |\Delta C/C|$. The values stated for the capacitance drift in

Table 1 are maximum values and refer to a two-year period and a temperature up to 40ºC. Here the reversible effects of temperature changes (β_c) and changes in relative humidity (α_c) are not taken into consideration

The drift is stabilised over the time and thus provides the long-term stability of capacitance; however, it may exceed the specified values if the capacitor is subjected to frequent, large temperature changes in the vicinity of the upper category temperature and relative humidity limits.

3.2.3 ESR / Dissipation factor

Under an AC voltage signal of specified frequency, the equivalent circuit diagram in Figure 10 can be simplified to a series connection of the capacitance *C*, an **equivalent series resistance** (*ESR*) and the series inductance L_S:

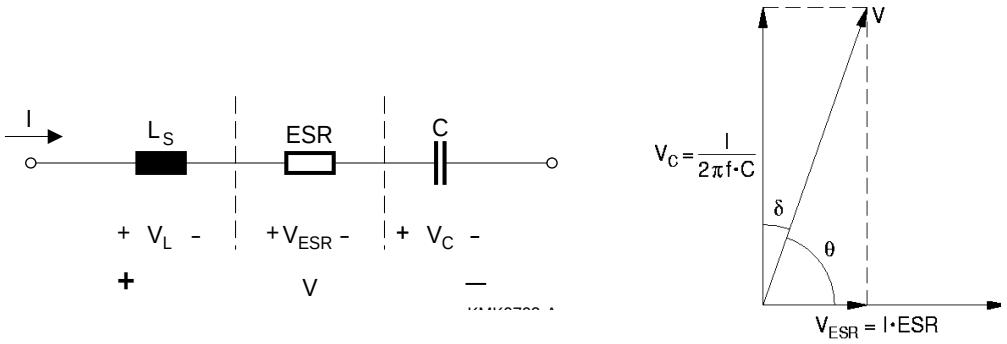


Figure 15. Simplified capacitor model for AC. Complex voltage calculation.

For frequencies well below the natural resonance frequency (L_S, V_L<<), due to the ESR the phase shift between voltage and current is slightly less than 90 degrees. The difference between the phase angle and 90º is the defect angle δ, which is measured through the **dissipation factor tanδ**. This latter number is defined as the ratio of the equivalent series resistance ESR to the capacitive reactance [$X_c=1/(2\pi f\, C)$]. And therefore,

$$tan\delta = ESR\ 2\pi f\ C. \qquad (3.3)$$

It can be easily deduced that the dissipation factor is also the ratio of effective power (i.e. power dissipation) to reactive power. The power dissipation can be expressed as a function of the voltage V_{ESR} across the equivalent series resistance *ESR*, or the current I through it:

$$P = \frac{V_{ESR}^2}{\mathrm{ESR}} = E\mathrm{SR} \times \mathrm{I}^2, \qquad (3.4)$$

given

$$V_{ESR}^2 = \frac{\mathrm{ESR}^2}{\mathrm{ESR}^2 + \left(\frac{1}{2\pi \mathrm{fC}}\right)^2} \times \mathrm{V}^2 \qquad (3.5)$$

And since for film capacitors $tan\delta = 2\pi f \cdot C \cdot ESR << 0.1$

$$V_{ESR}^2 = \mathrm{ESR}^2 \cdot (2\pi\, \mathrm{f\ C})^2 \cdot \mathrm{V}^2 \quad (3.6)$$

the power can be expressed as

$$P = 2\pi \text{ f C} \cdot \tan\delta \cdot \text{V}^2 \qquad (3.7)$$

As it will be seen later in section 3.3.3, both *ESR* and *tan*δ are important because they dictate the **power dissipation** of the capacitor and thus its **self-heating**, i.e. how much will they increase their temperature above the environment when subjected to AC operation voltage.

3.2.3.1 Dependence with of the dissipation factor with the capacitance value.

The generic standards and the sectional standards specify the same measuring conditions for measuring the dissipation factor tanδ as for measuring the capacitance. 1kHz is the standard frequency. For PP and PET film capacitors with $C_R \leq 1\mu F$, additional measuring frequencies of 10kHz or 100kHz are used for determining the dissipation factor.

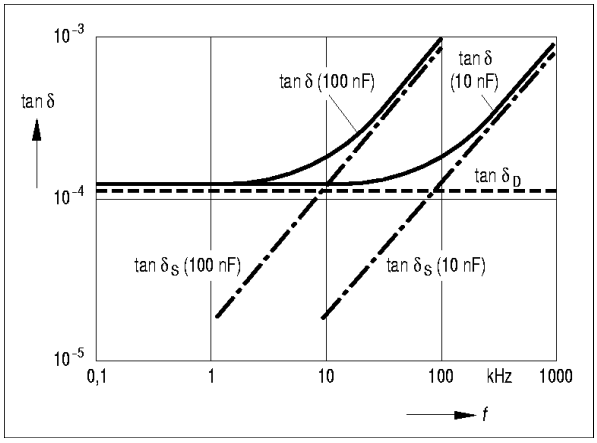


Figure 16. Dissipation factor versus measuring frequency (schematic representation using two polypropylene capacitors of different capacitance as examples).

Figure 16 depicts the behaviour of *tan* δ for two capacitors with very different capacitance values, illustrating the dependence of the asymptotic behaviour is both cases (series contribution, *tan* δ_S).

3.2.3.2 Variation of dissipation factor with frequency

For frequencies well below the natural resonance frequency, if the inductance L_S in Figure 10 is neglected, the dissipation factor tanδ is a combination of a parallel component $\tan\delta_P$, a series component $\tan\delta_S$ and a dielectric component $\tan\delta_D$:

$$\tan\delta = \tan\delta_P + \tan\delta_S + \tan\delta_D$$

$$\tan\delta_P = \frac{1}{R_P \cdot 2\pi f \cdot C} \qquad (3.8)$$

$$\tan\delta_S = R_S \cdot 2\pi f \cdot C$$

$$\tan\delta_D = \textit{characteristic of the dielectric}$$

The **parallel component** $tan\delta_P$ depends on the insulation resistance (parallel resistor R_P in Figure 10). Due to the extremely high values of insulation resistance, this component is negligible in the entire frequency range and contributes virtually nothing to the overall dissipation factor even at very low frequencies ($f << 1\ kHz$).

The **dielectric component** $tan\delta_D$ measures the losses associated to the dielectric (i.e. the energy wasted to polarise and re-polarize the dielectric in two opposite directions for the successive half-cycles of the AC voltage). It determines self-heating at low frequencies:

- for polypropylene capacitors, $tan\delta_D$ remains approximately constant with frequency and will typically result in a value of approximately 10^{-4}.
- for polyester capacitors, $tan\delta_D$ is considerably greater and increases with frequency. Therefore, these capacitors display a noticeably higher overall dissipation factor at lower frequencies (cf. Figure 15).

The series component $tan\delta_S$ is determined by the series resistance (R_S in Figure 10), which represents the sum of the contact resistances and the resistances of leads, metal layers and electrode foils. This component increases rapidly with frequency until it becomes the dominating component in the $tan\delta$ curve for high frequencies.

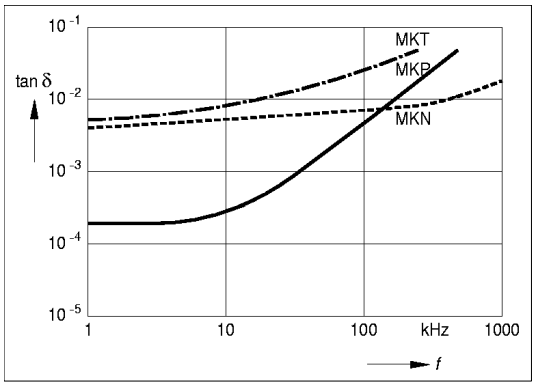


Figure 17. Frequency dependence of the dissipation factor, e.g. for C_R = 0.10 µF (typical behaviour)

3.2.3.3. Variation of ESR with frequency

From the definition of *tanδ,* given in Eq. (3.3), *ESR* can be expressed as:

$$ESR = \frac{\tan\delta}{2\pi \mathrm{fC}} \qquad (3.9)$$

Thus *ESR* comprises all the resistive, as the ones already described for the dissipation factor. Figure 18 gives a general frequency response for a film capacitor:

- For very low frequencies, leakage is prevalent (range not represented).
- At low frequencies, *ESR* is dominated by the dielectric losses, behaving roughly as f^{-1}.
- For medium and high frequencies, losses in the conductors are dominant and *ESR* becomes relatively constant.
- For very high frequencies (>1MHz) *ESR* increases by $f^{1/2}$ due to skin effect.

ESR variations with temperature follow those of dissipation factor, which will be discussed in next subsection.

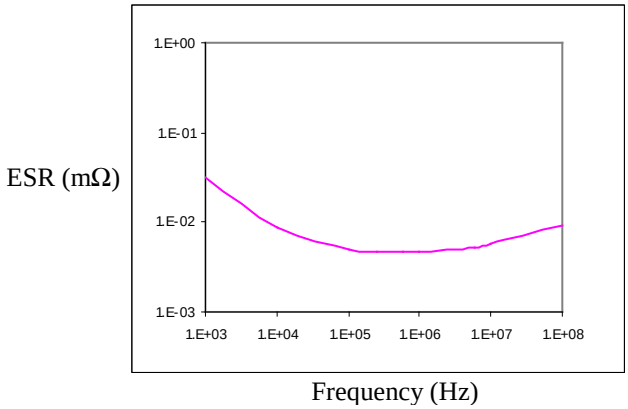


Figure 17. ESR versus Frequency for a MKT capacitor.

3.2.3.4. Variation of dissipation factor with temperature, humidity and voltage

The dissipation factor of capacitors with polypropylene dielectrics is largely unaffected by the temperature, whereas polyester capacitors show a characteristic dissipation factor minimum at approximately 80 °C (at 1kHz), see Figure 19.

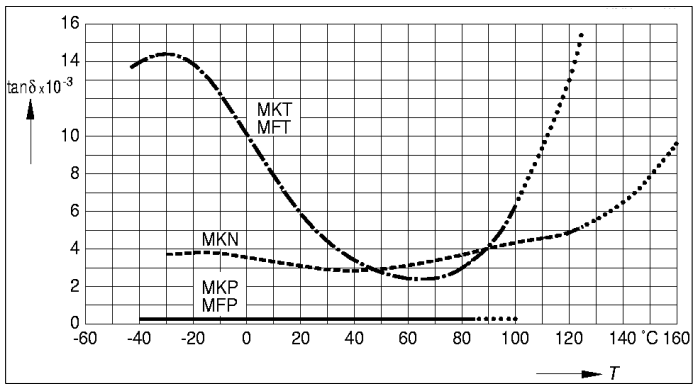


Figure 18. Dissipation factor tanδ versus temperature T for f = 1 kHz (typical values)

The dissipation factor values may increase as well under humid conditions, but this is only a secondary effect. It is virtually impossible to detect any variation of the dissipation factor with voltage.

3.2.4 Insulation resistance

3.2.4.1 Definition

The insulation resistance R_{is} of a capacitor is a measure of its resistance in DC. Under a stationary DC voltage, a leakage current flows through the dielectric and over the capacitor surfaces. R_{is} is measured by determining the ratio of the applied DC voltage to the resulting leakage current flowing through the capacitor, once the initial charging current has ceased (typically, after a period of 1 min ± 5 s). According to Figure 10, it is related to the R_P, parallel resistance of the capacitor.

The measuring voltage depends on the rated voltage and is specified in section 4.5.2. of IEC 60384-1:

Rated voltage V_R of capacitor	Measuring voltage
$10\ V \leq V_R < 100\ V$	(10 ± 1) V
$100\ V \leq V_R < 500\ V$	(100 ± 15) V
$500\ V \leq V_R$	(500 ± 50) V

For capacitors with capacitance ratings > 0,33 µF the insulation is often given in terms of a **time constant**.

$$\tau = R_{is}\ x\ C_R \qquad (3.10)$$

(Conversion for this formula: 1 MΩ x 1 µF =1 s).

3.2.4.2 Factors affecting the insulation resistance

The specified measuring temperature is 20ºC. At different temperatures, a correction shall be made to the measured value to obtain the equivalent value for 20°C, by multiplying the measurement result by the appropriate correction factor.

Measuring temperature in °C	Correction factors (average values) according to the sectional specification		
	MKT, MFT	MKN	MKP, MFP
15	0,79	0,79	0,75
20	1,00	1,00	1,00
[23]	1,15	1,15	1,25
27	1,38	1,38	1,50
30	1,59	1,59	1,75
35	2,00	2,00	2,00

In case of doubt a reference measurement at 20 °C and (50 ± 2) % relative humidity is decisive. As can be deduced from this correction factor table, the insulation resistance is strongly affected by temperature. In figure 20 the typical behaviour for different base materials is shown.

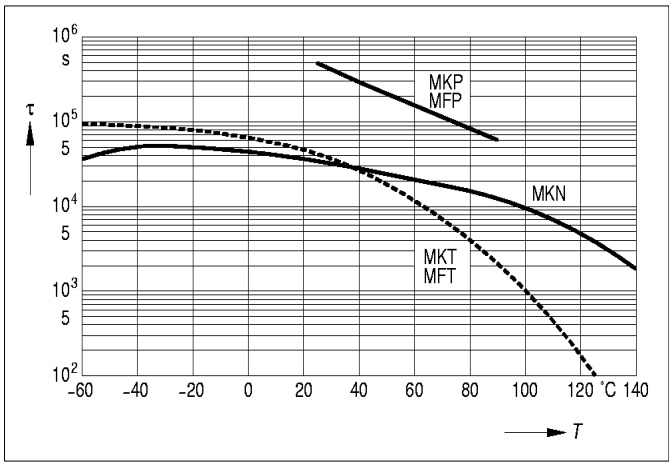


Figure 19. Insulation as self-discharge time constant τ (= R_{is} x C_R) in s (= MΩ x µF) versus temperature T (typical values)

The insulation resistance is also affected significantly by humidity (as humidity increases, the insulation resistance decreases).

3.2.5 Self-inductance

The self-inductance or series inductance L_S of a film capacitor is due to the magnetic field created by the current in the film metallization and the connections. It is thus determined by the winding structure, the geometric design and the length and the thickness of the contact paths. As far as possible, all modern film capacitors are constructed with low-inductance bifilar electrode current paths or extended-foil contacts, and thus feature a very low inductance. A general rule for deducing the self-inductance states that the maximum value is 1 nH per mm of lead length and capacitor length.

3.2.6 Impedance. Resonance frequency

The impedance Z represents the component's opposition to current flow and is both resistive and reactive in nature. It is thus of particular importance in AC and ripple current filtering. From the capacitor model in Figure 10, *Z* is defined as the magnitude of the vectorial sum of *ESR* and the total reactance (inductive reactance minus capacitive reactance):

$$Z = \sqrt{\mathrm{ESR}^2 + (2\pi \mathrm{f}\ \mathrm{L_S} - \frac{1}{2\pi \mathrm{f}\ \mathrm{C}})^2} \qquad (3.11)$$

Z is strongly frequency dependent: At low frequencies, the capacitive reactance $X_c=1/2\pi f C$ prevails, whereas at very high frequencies the inductive reactance $X_L=2\pi f L_S$ is dominant. When the capacitive reactance equals the inductive reactance, a natural resonance occurs. At this point the reactance cancel each other and the impedance equals the *ESR*. The natural resonance frequency is therefore given by

$$f_{RES} = \frac{1}{2\pi\sqrt{\mathrm{CL_S}}} \qquad (3.12)$$

The frequency range of the natural resonance (also termed self-resonance) as a function of the capacitance can be read off the following diagram.

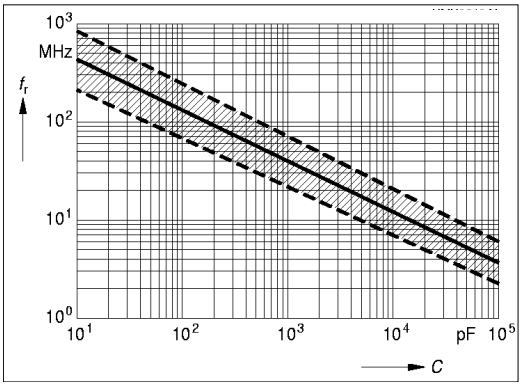
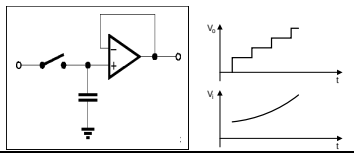
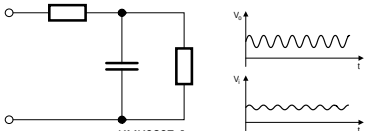
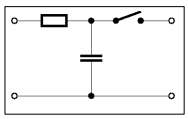
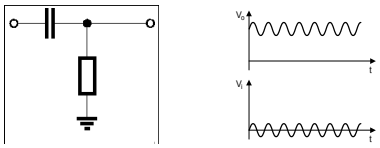
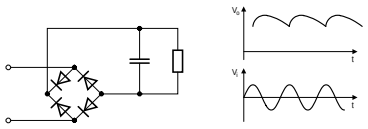
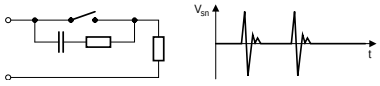
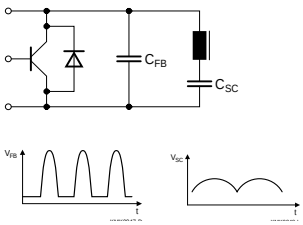
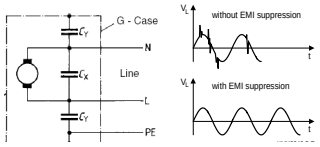


Figure 20. Resonant frequency versus capacitance (typical values)

3.3. OPERATION

3.3.1 Typical applications of film capacitors:

The following table shows the main current applications of film capacitors, together with the typical design configuration in each case, and the requirements of the application in terms of the electrical properties just described.

APPLICATION		REQUIREM.	
SAMPLE AND HOLD The capacitor stores a voltage until a sample is taken.		High R_{IS} Low dielectric absorption	DC
DC-LINK – BYPASS – DECOUPLING The capacitor acts as a low-pass filter, preventing the transmission of AC voltages.		High R_{IS} Low L_S	DC
TIMING / ENERGY STORAGE / IGNITION The capacitor stores a charge until a specific amount of time (time delay) has elapsed. The capacitor stores a charge and then releases it in a short energetic pulse.		Good pulse characteristics	DC
BLOCKING / COUPLING The capacitor acts as a high-pass filter: • Preventing from DC voltages (blocking). • Transferring only the AC load (coupling).		High R_{IS} Low L_S	AC
SMOOTHING The capacitor keeps the working voltage level, supressing fast transient changes.		Low tanδ Good AC characteristics	AC
SNUBBERING A capacitor/resistor connection absorbs arcs to avoid damages on relays/switches.		Low tanδ Good pulse characteristics	AC
FLY-BACK AND S-CORRECTION (horizontal deflection circuits in TV sets) When the deflection coil current flows into the fly-back capacitor (C_{FB}), the electron beam is rapidly shifted from the right to the left side of the screen The S-correction capacitor (C_{SC}) imposes an 'S' shape to the current ramp in the deflection coil, correcting the path difference between the centre and the edge of a flat screen tube.		Low tanδ Good pulse characteristics Low tanδ Good pulse characteristics	AC
EMI SUPRESSION A capacitor/resistor network at the input of a device supresses external noise pulses that could damage the device components.		Low flammability	AC

3.3.2 Operation under DC Voltage

The most classical operation of a capacitor is the accumulation of energy under a continuous DC voltage. In this situation, there are two points of concern related to the electrical requirements of the application (rated voltage, loss factors…) and the influence of the environmental working conditions on the performance of the component.

3.3.2.1 Rated voltage

The **rated voltage V_R** is the DC voltage for which the capacitor is designed. It is defined as the maximum DC voltage which may be applied continuously to the terminals of a capacitor at any temperature between the lower category temperature T_{min} and the rated temperature T_R (see 3.3.2.2). **V_R** is dependent upon the dielectric material, the film thickness and the operating temperature.

3.3.2.2 Maximum DC voltage vs. temperature

The **category temperature range** of a capacitor gives the range of ambient temperatures at which the capacitor can operate continuously. It is defined by the upper and lower category temperatures (T_{min} and T_{max}).

In this range, there exists a **rated temperature T_R** which is defined as the maximum ambient temperature at which the capacitor can operate continuously under the rated voltage V_R. It is directly dependent on the dielectric material:

Dielectric	T_R
PET, PP	85ºC
PEN	125ºC

The **category voltage V_C** is the maximum voltage that can be applied continuously to a capacitor at a given temperature. It is defined as follows: Between the lower category temperature T_{min} and the rated temperature T_R, the maximum continuous voltage is the rated voltage V_R., i.e. V_C=V_R.

Between the rated temperature T_R and the upper category temperature T_{max}, a de-rating factor needs to be applied. V_C is expressed in a fraction of the rated voltage, as shown in Fig. 22:

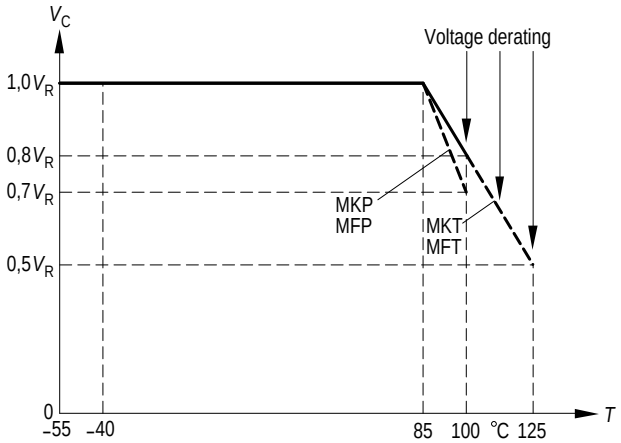


Figure 21. Maximum permissible continuous voltage in relation to ambient temperature.

3.3.3 Operation under AC Voltage

A more complex operating mode of the capacitor is found when subjected to alternating voltage. Far beyond the performance of electrolytic capacitors, film technology enables the possibility of operating on alternating signals in a wide range of frequencies, as it will be shown in the following.

3.3.3.1 Rated AC voltage

Similarly to the definition of DC rated voltage, the **rated AC voltage V_R** is defined as the maximum root mean square (*RMS*) voltage at specified frequency (typically 50Hz) which may be applied continuously to the terminals of a capacitor at any temperature between the lower category temperature T_{min} and the rated temperature T_R.

3.3.3.2 Maximum AC voltage vs. frequency

The ability of a capacitor to withstand a continuous (sine-wave) alternating voltage load V_{RMS} or alternating current I_{RMS} is a function of frequency and is limited by different factors (see Figure 23). In the whole frequency range, three regions can be identified in terms of the limiting factor for the V_{rms} voltage level admissible to the capacitor. These regions have been clearly depicted in Figure 23, and will be explained in more detail in the following paragraphs.

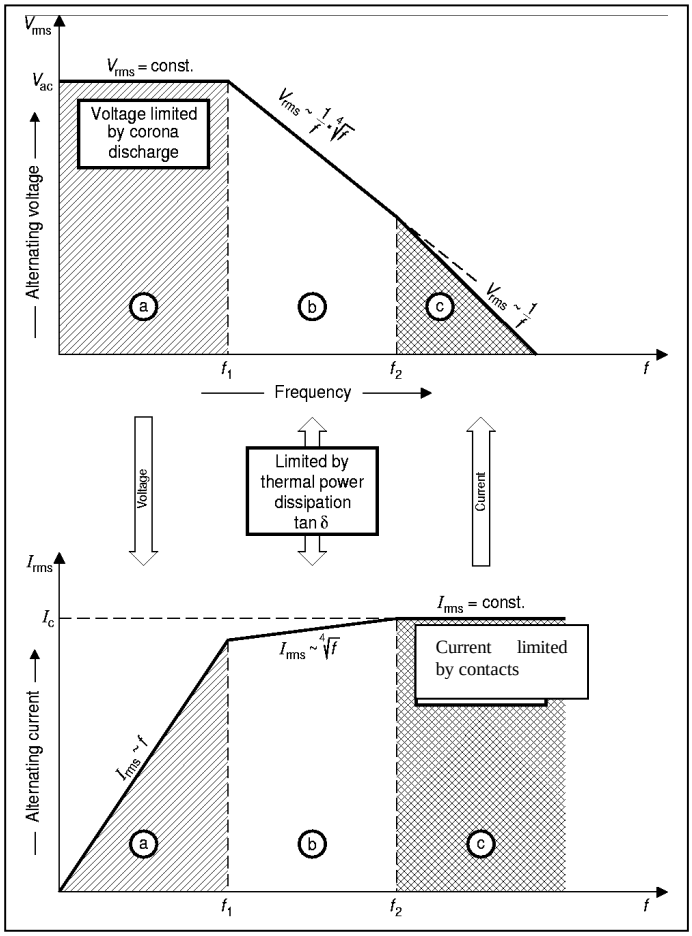


Figure 22. Alternating voltage and alternating current load limits

Region (a): Limit at which corona discharges start to occur, V_{CD}:

Below a certain frequency limit, f_1, the applied AC voltage V_{RMS} should not exceed the threshold voltage V_{CD} at which corona discharges would start to occur by ionisation of small air pockets present in the capacitor (please refer to Section 3.6). This effect may degrade the film metallization and occasionally, endanger its dielectric strength. For sinus waveforms, the following relation must be taken into consideration:

$$V_{RMS} \le V_{CD} \; or \; I_{RMS} \le V_{CD} \cdot 2\pi f \cdot C \qquad (3.13)$$

For non-sinus wave form,

$$V_{PEAK-TO-PEAK} \le 2 \cdot \sqrt{2} \cdot V_{CD} \qquad (3.14)$$

Region (b): Limit due to thermal power dissipation:

Above a certain frequency limit, f_1, the permissible alternating voltage load must be reduced with increasing frequency, in order to keep the power P_E generated in the capacitor body below the power P_A which can be dissipated by the surface of the capacitor. Both powers are defined as:

$$P_A = \alpha \cdot A \cdot \Delta T \qquad (3.15)$$

$$P_E = V_{RMS}^2 \cdot 2\pi f \cdot C \cdot \tan\delta \qquad (3.16)$$

where:

α = Heat Transfer Coefficient.

ΔT = Self-heating or steady-state over-temperature attained at the hottest part of the capacitor surface in relation to the surrounding atmosphere (the so-called hot spot).

A = Surface area of the capacitor

It is important to remark that, in order to prevent permanent damage to the capacitor, the self-heating ΔT (at the rated temperature) must not exceed a certain value, always depending on the dielectric material:

Dielectric	Max. ΔT
PET, PEN	15ºC
PP	10ºC

Since $P_E \le P_A$, the conditions for the maximum permissible alternating voltages and alternating currents in this region can be deduced as:

$$V_{rms} \le \sqrt{\frac{\alpha A \Delta T}{2\pi f C \tan\partial}} \; or \; I_{rms} \le \sqrt{\frac{2\pi f C \alpha A \Delta T}{\tan\partial}} \qquad (3.17)$$

And therefore the frequency dependence can be approximated by:

$$V_{rms,\max} \prec \frac{1}{f}\sqrt[4]{f} \; or \; I_{rms,\max} \prec \sqrt[4]{f} \;\; , \qquad (3.18)$$

where the relationship between voltage and current has been taken into account.

The heat transfer coefficient α and the dissipation factor $\tan\delta$ depend strongly on technology, construction, material and geometry of each capacitor; $\tan\delta$ also depends on frequency and temperature. This makes difficult the use of these equations to work out, for example, the maximum allowed V_{RMS} or the self-heating (ΔT) for any known operating conditions. Hence the limit lines for the maximum V_{RMS} at ambient temperature must be obtained empirically.

Sometimes it is required to estimate the self-heating *ΔT'*, for a given V'_{RMS} (i.e. *75 V*) and frequency (i.e. *20 kHz*) in terms of a certain observation performed under very particular conditions of self-heating at a this reference voltage. Attending to last equations, the following relationships shall be applied:

$$\Delta T_{V',f} = \left(V'_{RMS} / V_{RMS,MAX} \right)^2 \cdot \Delta T_{V,f} \quad \textit{for PET or PEN dielectric} \qquad (3.19)$$

$$\Delta T_{V',f} = \left(V'_{RMS} / V_{RMS,MAX} \right)^2 \cdot \Delta T_{V,f} \quad \textit{for PP dielectric} \qquad (3.20)$$

It is important to remark that the former calculations correspond to pure sinusoidal waveforms. Usually, practical applications will not involve loads with perfect sine-wave functions. In some applications, however, it is possible to estimate the loads accurately enough by approximating them to sine waves, as in the following cases:

WAVE-FORM	ELECTRICAL PARAMETERS
FLY-BACK Voltage Current t/T = 0.15 to 0.25	$N = \frac{t_2}{t_1}$ $V_{RMS} = 1.07 \cdot \frac{V_{pp}}{\sqrt{2 \cdot N}}$ $f = \frac{1}{2 \cdot t_1}$
S-CORRECTION Voltage Current	$V_{rmsc} = \frac{V_{pp}}{2\sqrt{2}}$ $I_{rmsc} = \frac{I_{pp}}{2\sqrt{2}}$ $f = \frac{1}{T}$
TRAPEZOIDAL Voltage	$V_{rmsc} = V_{pp} \sqrt{\frac{3T-4t}{12T}}$ $f = \frac{1}{T}$

In more general cases, the power dissipation must can be always calculated by Fourier decomposition of the wave-form into its harmonics:

$$P_E = \sum V_{rms\,i}^2 \, 2\pi f_i \, C \tan\delta(f_i) \qquad (3.21)$$

And thus a theoretical over-temperature *ΔT* can be calculated equating P_E=P_A. If we are to assist in such cases, please send us scaled oscillograms.

Region (c): Limit due to maximum current handling capability

Above another certain frequency limit f_2, the permissible AC voltage load is limited by the maximum current I_C that can pass through the connection sprayed metal-film metallization without causing overheating due to associated resistive losses:

$$V_{rms} \leq \frac{I_C}{2\pi f\, C} \; or \; I_{rms} \leq I_C \qquad (3.22)$$

In practice, however, this region is only evident for small capacitance with short contact lengths. It is not relevant for power application, in which we are more interested.

3.3.3.3 Maximum AC voltage vs. temperature

For low frequencies (region "a" of Figure 23) a de-rating of the RMS voltage versus the working temperature has to be applied, following the rules defined in 3.3.2.2. For higher frequencies (regions "b" and "c") the use under temperatures higher than room temperature must take into account the following factors:

- The operating temperature of the capacitor is always the sum of the ambient temperature and the self-heating:

$$T_{op} = T_{amb} + \Delta T \qquad (3.23)$$

It is essential to remark that, in any case, **T_{op} should not exceed the upper category temperature.**

- tanδ presents natural variations with temperature, as described in 3.2.3. This is specially critical for ambient temperatures above the rated temperature: in these cases tanδ (T_{op},f) has to be used in the power calculations.

In any case, for design and validation purposes, any theoretical approach must be validated by measn of an empirical temperature check on the capacitor. The test fixture should be as shown in Figure 24: a dummy capacitor similar to the capacitor under test shall be used to measure the ambient temperature (the points for measuring temperature are marked with an "X").

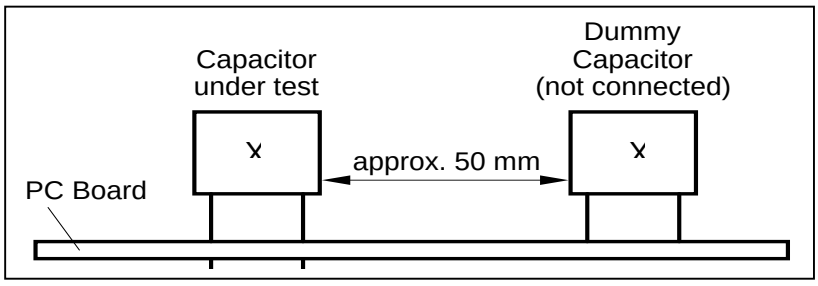


Figure 23. Test fixture to measure the self-heating under working conditions.

3.3.3.4 Pulse withstanding capability

The pulse handling capability of a capacitor is determined, in particular, by the internal structure of the capacitor element. (construction variants have already been shown). Voltage pulses due to rapid voltage changes will lead to strong peak currents in the capacitor. These currents will generate heat in the contact regions between the sprayed-on metal terminations and the metal layers. Thus we will find a limit to the pulse we can apply to a particular capacitor when the heat dissipated is high enough to damage these regions. The parameters

that define the pulse handling capability of a capacitor are the maximum *dV/dt* and k_0 it can withstand.

Voltage pulse slope dV/dt

If we only take into account the peak current I_P associated to a voltage pulse, we may define the maximum voltage pulse slope *dV/dt* of the pulse as

$$\frac{dV}{dt} = \frac{I_P}{C} \qquad (3.24)$$

Pulse characteristic k_0

The heat energy Q generated by the pulse in the capacitor can be calculated by the equation:

$$Q = \int_0^\tau I^2 \cdot R_i \cdot dt = \int_0^\tau \left(\frac{dV}{dt}\right)^2 \cdot \frac{R_i}{C^2} \cdot dt \qquad (3.25)$$

where τ is the pulse-width and R_i is the resistance of the contacts. To relate the heat energy and the pulse slope, a characteristic factor k_0 depending on the waveform can be defined:

$$k_0 = 2\int_0^\tau \left(\frac{dV}{dt}\right)^2 \cdot dt \ . \qquad (3.26)$$

Given the small dependence of the resistance and the capacitance with time, it is possible, in first approximation, to take advantage of this definition to express:

$$Q \approx \frac{k_0}{2}\frac{R}{C^2}. \qquad (3.27)$$

k_0 values are valid under the assumption of a complete dissipation of the heat between consecutive pulses, which is the case for duty cycles higher than *100μs*. For lower duty cycles (i.e. for frequencies higher than *10kHz*), the dissipation of heat from pulse to pulse is not complete and a dangerous overheating which might destroy the capacitor builds up. These cases should be studied under the conditions of section 3.2.

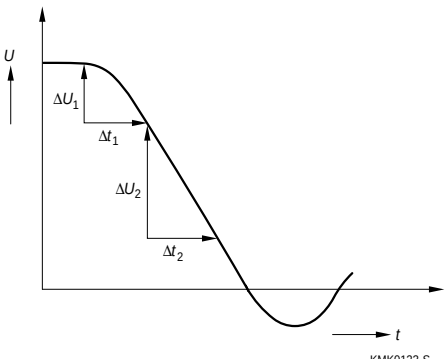
Modern digital oscilloscopes allow direct calculation of k_0 from a wave-form (integration time ranges not higher than *10μs* should be used). However, there are two cases in which k_0 can be calculated analytically:

- **Ramp discharge:** when the capacitor is discharged from a particular voltage to zero in a single ramp (Figure 25), the voltage pulse slope can be approximated by

$$\frac{dV}{dt} \approx \frac{V_{pp}}{\tau} \qquad (3.28)$$

V_{pp} Peak-to-peak voltage
τ Voltage decay time

On the other hand, the k_0 can be calculated by a piece wise linear decomposition, comprising *ΔV - Δt* segments:



$$k_0 \approx 2\left(\Delta V_1 \cdot \frac{\Delta V_1}{\Delta t_1} + \Delta V_2 \frac{\Delta V_2}{\Delta t_2} + \ldots\right)$$

Figure 24. Piece-wise linear approximation of a voltage pulse

A simpler approximation (which is exact for trapezoidal or saw-tooth pulses) can be obtained by:

$$k_0 = 2 \cdot \frac{V_{PP}^2}{\tau} \qquad (3.29)$$

and thus

$$\frac{dV}{dt} = \frac{V_{PP}}{\tau} = \frac{k_0}{2V_{PP}} \qquad (3.30)$$

- **Passive discharge**: for discharging in passive (*RLC*) and short-circuit configurations, there is no simple approximation for *dV/dt*, which has to be obtained from I_P. k_0 is exactly determined by:

$$\frac{dV}{dt} = \frac{I_P}{C} \qquad (3.31)$$

$$k_0 = \frac{V_{CH}^2}{R \cdot C} \qquad (3.32)$$

V_{ch} Charging voltage
R Ohmic resistance of discharge circuit

3.3.4 Climatic stress

We will finally discuss about the climatic category of our product, which is a relevant parameter identified for any capacitor, as specified in *IEC 60068-1*, Appendix A.

3.3.4.1 Effect of temperature

The **reversible effects** of temperature on capacitance, loss factor and insulation resistance have been treated in the respective sections. At this point, we should only remark that an excessive exposition to temperatures higher than T_{max} will cause a thermal ageing of the film following Arrhenius´ law, which will produce **irreversible effects** on the electrical characteristics. Additional changes in the capacitor dimensions will follow as a consequence of film shrinkage.

3.3.4.2 Effect of humidity

The absorption of moisture increases the number of permanent dipoles inside the capacitor, producing **reversible effects** on capacitance, loss factor and insulation resistance which have been treated in the respective sections These occur for relative humidity less than 93%, applied for a limited time, and can be reversed by a drying process. The equilibrium data provided for the reversible changes are independent of the construction and finish of the film

capacitor: there will only be differences in the rate of moisture absorption/de-sorption, which will depend on:

- Capacitor finish: humidity penetrates faster into unprotected components (as well as it diffuses out faster).
- Ambient temperature and humidity.

Typical values of the time constants for absorption/de-sorption vary between 1/2 a day (e.g. for unprotected capacitors) and several weeks (e.g. for capacitors with plastic cases).

More dangerous are the **irreversible effects** that long contact of the film capacitor with humidity will produce. Direct contact with liquid water (specially for unprotected components) or excess exposure to high ambient humidity or dew will eventually remove the film metallization and thus destroy the capacitance. More details about this failure mode will be giving in Section 3.6, when the so called corona effect is explained.

Simulations of the effect of humidity are done through the humidity test defined in the climatic category. Accelerated testing can be performed under more severe conditions, if the relative severity is taken into account. The severity S of any humidity test can be defined as the product of two factors:

$$S = \rho : D \qquad (3.32)$$

where

ρ = Density of water in the ambient, which is a function of both the relative humidity and the temperature. This data can be extracted from standard psychometric charts. For example, for T=40ºC H=93%, we obtain ρ=47 gr/m^3.

D = Diffusion coefficient of water into the parts. At the end, this is a function of temperature through the Arrhenius' law:

$$D = \exp\left\{-\frac{E_A}{RT}\right\} \qquad (3.33)$$

where:

E_A = Activation energy for diffusion = 10 Kcal/mol
R = Universal molar constant for gases = 1,987 cal/mol K
T = Temperature in Kelvins = T (in ºC) + 273

The test severity S helps to compare the conditions of humidity tests. As an example, in the following table, the data for some common test conditions are compared and referred to the standard conditions (*40ºC/93%, S'=1*):

Temp (ºC)	**Hum. (%)**	**ρ (gr/m^3)**	**S**	**S'**
40	93	47,0	4,89E-06	1,0
65	95	151	5,14E-05	10,5
85	85	294	2,31E-04	47,3

As it will be explained in Appendix I, severity factors and accelerated testing are also extremely important for determining reliability performance of the capacitors.

3.3.5 Self healing capability

The most important reliability feature of film capacitors is their self-healing capability: the ability to clear faults (such as pores or impurities in the film) under the influence of a voltage and become a much more robust structure. The metal coatings, which are vacuum-deposited directly onto the plastic film, have a thickness of only 20...50 nm. If the dielectric breakdown field strength is exceeded locally at a weak point, a dielectric breakdown occurs. In the breakdown channel, the high temperatures reached (up to 6.000K) transform the dielectric into a highly compressed plasma which forces its way out. The thin metal coating in the vicinity of the channel is totally evaporated by interaction with the plasma, retreating from the breakdown channel. The rapid expansion of the plasma causes it to cool after a few microseconds, thus quenching the discharge before a greater loss of voltage takes place. The resulting insulated region around the former weak point will cause the capacitor to regain its full operation ability. At low voltages, anodic oxidation of the metal coatings leads to an electrochemical self-healing process.

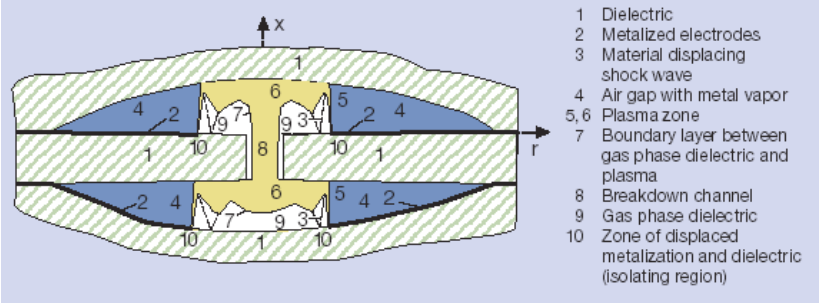


Figure 25. Schematic of the self-healing area during electrical breakdown

3.3.6 Typical failure mode: Corona discharges

The air inside the micro-gaps which are normally present in and around the capacitor (for example, inside and in-between the films, near the corners, etc.) may get ionised, leading to a destructive process called corona effect.

This occurs when the intensity of the electric field in the capacitor exceeds the dielectric rigidity of the air. In these conditions, small corona discharges take place, producing two undesirable effects:

- Removal of the film metallization edges, and thus drop of capacitance.
- Occasionally, structural damages caused by the bombardment of the film with ions and electrons might occur as well. This produces a reduction of the breakdown voltage level of the dielectric, and eventually might give rise to a short circuit or fire.

The voltage at which this phenomenon starts is called corona starting voltage V_{CD}. Its value is determined, above all, by the internal construction of the capacitors (which determines the field strength at the edges); it also depends, to a lesser extent, on the thickness of the dielectric. This voltage limit can be raised, in particular, by using internal series connection designs. However, if the capacitor is used below V_{CD}, no corona effect will be observed and the corresponding degradation can be neglected.

Although the corona corrosion has some points of coincidences with the self-healing mechanism, there are important differences among them that, as stressed in following table:

	Self-healing	**Corona corrosion**
In time…	Isolated phenomenon	Continuos mechanism
Voltage	Mainly DC	Mainly AC
Outcome	Improved design	Destructive loss of electrode area
Measure	Momentary increase of current intensity	Permanent capacitance loss

Specific design of a film capacitor for the DC-link position in a solar inverter

The interest in film capacitors has revived recently as a result of their successful introduction in new industrial applications such as power converters for new renewable energies (solar, wind,..), heavy duty drives for motors and in general for critical applications (like hybrid automotive systems, energy distribution…).

A relevant function of film capacitors in these applications is the DC-link position, where it is subjected to a main DC voltage accompanied by a high frequency ripple signal. The response to this high frequency signal and the existing peak voltage in the application determines the suitability of the capacitor.

4.1. *Basic requirements for capacitors in the DC-Link position*

Typical industrial applications where DC-Link capacitors play an important roll are un-interruptible Power Supplies (UPS), switch-mode power supplies (SMPS), and more generally inverters (see Figure 28). As we have been already discussing, particularly interesting is the development experienced by the solar inverter sectors in the most recent years. The need of more reliable, modular and also economic products, have forced designers around the world to be much more demanding in terms of reliability, stability and also compactness [6, 7, 8, 9, 10, 11, 12].

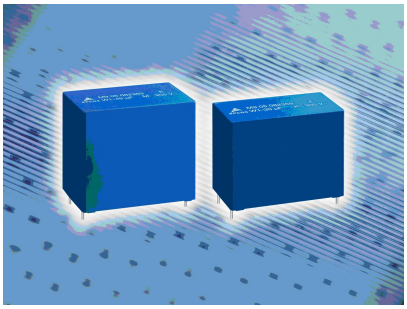


Figure 26. New DC-Link High Density series. The four pin configuration improves the mechanical stability and current capability of the design.

There are two basic functions that DC-Link capacitors can perform in a circuit. On the one hand, i.e. in induction hobs, they can be intended for stabilising the voltage after a rectifier providing enough current to the load (see Figure 29). On the other, i.e. in solar inverters, they are set in parallel to the source (either the solar generator directly or the intermediate batteries) prior to the buck inverter module (see Figure 30). In both cases, the capacitor is subjected to a high frequency ripple voltage, which is superimposed to a main DC voltage.

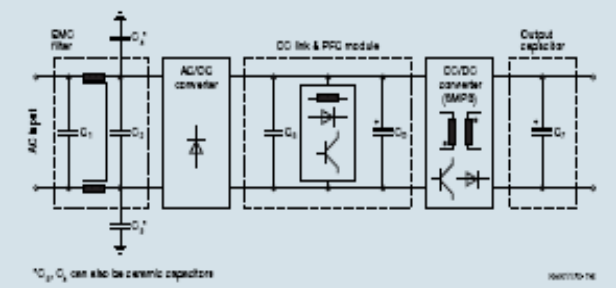


Figure 27. SMPS modules are typical industrial applications where DC-Link capacitors play an important role

Figure 4 shows a simplified diagram of a two phase solar inverter. According to this diagram, only one capacitor is needed. Strictly speaking, even this capacitor is redundant because it is connected in parallel with the solar generator. The question is then why and what type of capacitor can be best used at this position. To answer this question, gaining perfect knowledge of the inverter switching mechanisms and circuit parasitic components is obviously necessary.

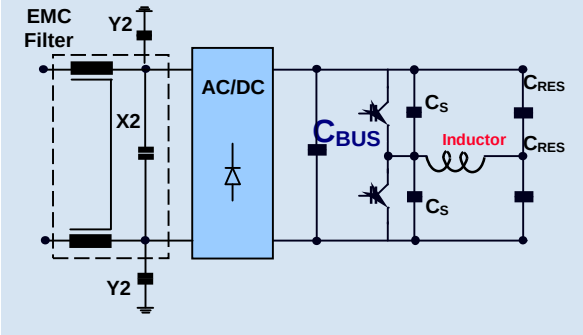


Figure 28. Basic scheme of an induction hob circuit.

The synthesis of a smooth sinusoidal current for the connection to the general or local AC network requires high switching rates in different combinations of the inverter switches so that the output current can track the desired sinusoidal current. The ripple is a function of the DC voltage, circuit inductance, and the switching period. The switching frequency in today's insulated-gate-bipolar-transistor (IGBT) based inverter is in between 10 kHz and 20 kHz. The ripple current of the two or three phase leg sum together, being able of seriously damaging the generator and any other element added to the circuit (i.e. batteries). The bus capacitor is therefore needed for absorbing the ripple due to the switching.

The DC bus capacitor is in fact the most important passive component in a solar inverter. In particular, it is the element restricting and defining the overall lifetime of the final product. Most traditional designs use a large (~1 mF) electrolytic capacitor placed at the input terminal of the inverter for power decoupling. This is known to be one of the main limitations regarding volume and service life in photovoltaic systems.

As reliability and stability are increasingly becoming the most important requirements for those capacitors, and film capacitor technology becomes the preferred solution. Therefore, designers are working on optimising their circuit in order to reduce the weight of the capacitance value, which was the limiting factor to use film capacitors [1].

Accordingly to this, more sophisticated designs, use a DC power smoothing circuit which reduces the voltage ripple at the DC-link bus. This allows downsizing the input

capacitor to a dozen of micro farads, being then possible to use film capacitors, with the consequent improvement in performance and reliability of the device. In fact, several new developments already point out to the advantages of using film technology for this position [9, 11, 12]. With this more sophisticated option, significant improvements are obtained concerning:

- Size reduction
- Cost reduction
- Reliability.

In any case, the DC-Link capacitor in solar inverters needs to cope with following problems:

1. The ripple current due to the inverter switching
2. Voltage fluctuation coming from to the generator
3. Voltage transient due to leakage inductance and fast device switching

To these general requirements, we should add an specific feature if film technology is considered:

4. Over voltage due to self-healing.

On the contrary, if electrolytic capacitors are going to be used, then special designs should be considered taking into account:

5. Introduction of diodes for avoiding current inversion, which may destroy the electrolytic capacitor.
6. The relatively high ESR of electrolytic components, which under certain operation conditions can double that of a typical film capacitor.

The capacitance needed to deal with the first three matters of concern may not be high, but the pulse handling capability and frequency response of the capacitor are the major concerns. For the self-healing, if the generator is directly connected to the capacitor, the capacitance value is not an issue. The overall design should clearly focus then on the current handling capability in a wide range of ambient temperatures.

Traditionally, the size of the DC-Link capacitor has been chosen in an arbitrary basis. The design philosophy with high capacitance electrolytic capacitors is typically inherited from the design of industrial drives, where the capacitance value is calculated to smooth the 6th harmonic ripple caused by the utility line [12]. According to simulations, the need for smoothing the 6th harmonic is no longer necessary if a battery is used in between the generator and the inverter, and the capacitor selection criterion should now be focused on the current handling capability but not the voltage ripple [12].

Additional features that are asked for to the DC-Link capacitor include:

- Thermal stability. Operating temperature range from –55°C to 105°C.
- High dielectric strength.
- Low E.S.R. ~5 mΩ tested at 10kHz, 70°C
- Low E.S.L.

In the following pages, a new series of film capacitors will be introduced with a capacitance density that can be considered competitive against electrolytic capacitors, especially if the gain in reliability, stability and price are also taken into account. As what the

rest of the requirements concern, it is extensively known that film technology offers a better performance in terms of low equivalent series inductance and resistance.

4.2. *Additional capacitive positions in the inverter.*

In addition to the DC-link position, there are some other capacitors that are traditionally used in an inverter for dealing with parasitic components and switching problems. Take the parasitic inductance as an example. Physical size constraint makes it nearly impossible to eliminate parasitic inductance in a high power inverter. For this reason, a DC snubber capacitor is usually added across the top and bottom DC rails on each phase leg to suppress the voltage spike locally. The requirements for this capacitor are high peak current capability and extremely low inductance (i.e. ranging from 10's to 100's nH). The leakage inductance and its interconnect inductance of the snubber capacitor should be at least one order of magnitude less than the lumped parasitic inductance, otherwise it will defeat the purpose of voltage spike suppression.

When electrolytic capacitors are used as DC-link, the use of a snubber capacitor is unavoidable because the parasitic inductance of the electrolytic is quite significant. However, with the use of a low-inductance film capacitor and an appropriate PCB layout, it is also possible to eliminate the snubber capacitor [12].

Capacitors are also used as protection and filters at the input and output of the inverter. X and Y positions are typical protection functions that film capacitors usually carry out in industrial drives and inverters.

In some occasions, these X/Y capacitors cannot offer all the capacitance that the application requires. In these cases, DC-Link capacitors are also then used as complement to the X/Y filters, which are reinforced with an additional capacitive charge. In these applications, the capacitor is also subjected to a continuous DC voltage and a high frequency ripple current.

4.3. *Optimised design*

For most applications, size is a synonym for cost efficiency and customer satisfaction. For that sake, we have concentrated our efforts into the miniaturisation of the very successful EPCOS High Power DC-link series, already used in the solar market [5]. In Section 2.1.3, we have identified "Density of Capacitance" and "Temperature performance" of current film technology. This is at the end related to the dielectric strength of the base film at high temperature

As a consequence of the collaboration and the feed back received from several benchmarking producers and designers, we proposed in this project an innovative design of High Density capacitance products, that we will prove to be perfectly suitable for DC-Link applications.

In this sense, **polypropylene** becomes the best choice with respect to the dielectric material, due to its low dielectric loss factor and, what is even more important for the application, its stable performance for a wide range of temperatures. As we have shown in Section 3, its main features have a reduced dependency with the frequency, which is also important for this application [2]. The thickness of the dielectric film finally determines rated voltage of the capacitor and thus it is a parameter that has been analysed deeply to optimise the relation among the capacitor sizes, its electrical performance and the product costs.

In this respect, a careful study of the base film capabilities and performances, allowed us to enhance the dielectric strength of the dielectric, which finally leads to a much more competitive final product in terms of energy per unit of volume. Following table shows proposal for our new design, result of our initial investigations on the base film:

Thickness of base film (μm)	Rated voltage @ 70 °C (V)	V/μm @ 70 °C	Rated voltage @ 85 °C (V)	V/μm @ 70 °C
3	450	150	450	150
4	800	200		
5	1100	220		
6	1300	220		

The most important advantages of these new capacitors could be summarised as follows:

- Low ESR values [3]. It helps the capacitor to minimise the power generated by working under high frequency AC voltages. ESR will lie between 3mΩ and 10mΩ (at 10KHz).

- High reliability due *Self-healing* properties [4]. Self-healing is a specific characteristic of metalized film capacitors and can be defined as the capacitor ability to clear faults (such as pores or impurities in the film) when subjected to high voltage. This process causes the capacitor to regain its full operation ability and, therefore, enhances the product reliability during its life-time.

- Safety. Drift of the electrical parameters and eventually open circuit are the standard failure modes for film capacitor, while for other technologies (i.e. electrolytic) a failure or malfunction might lead the capacitor to a short circuit putting into risk the integrity of the whole equipment. Besides, film capacitor can withstand changes of polarity, not needing protection diodes or any especial design rule.

- Stability during operation. For film capacitors, capacitance change remains within ±5% in a wide range of temperatures going from -50ºC to 105ºC, four times lower than the values expected for electrolytic capacitors (see Figure 30), whose temperature operating window is even narrower.

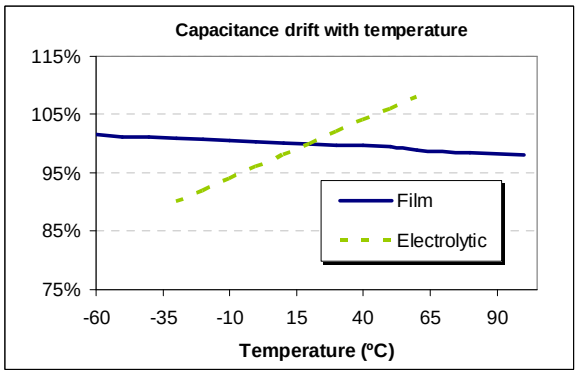


Figure 29. Comparison of capacitance drifts of Electrolytic and Film technologies [4]

- High I_{rms} handling capability. Maximum I_{rms} could be up to 20A (at 20KHz).

From the electrical point of view, the key factor for many purposes is the behaviour of the DC-link capacitor at high currents and frequencies. Every real capacitor has some resistive parts which produce a self-heating of the overall structure when subjected to sufficiently high currents.

For the optimisation of the design, we have carried out a careful study on the self-heating of the capacitor due to the dissipation losses. A theoretical model has been developed that takes into account the contribution of the different elements of the capacitor. Figure 31 shows the results of applying this model to the new High Density series. The contribution of each of the electrodes (metalized films) is shown, and also the total dissipated power in the capacitor. The theoretical prediction confirms the empirical observation that the most critical area concerning self-heating is the areas of contact between the sprayed electrodes (at both ends of the windings) and the metalized film. The less resistive area, on the contrary, is the centre of the capacitor. Local hot-spots should therefore be expected in the vicinity of the sprayed electrode areas. For this reason the improvement and optimisation of the contact area has been a priority at the design stage of the new High Density series.

Note that the calculation of the hot-spot temperature T_h is important, because it determines the life expectancy of the capacitor. Hot-spot temperature is dependent on capacitor power losses P and ambient temperature T_a as follows,

$$T_h = T_a + P \cdot R_{th}, \qquad (4.1)$$

R_{th} being the relative thermal resistance between capacitor hot-spot and the environment [15]. This is a parameter that depends on environmental temperature and air speed, whose values are typically in the range 3-4 ºC/W. Capacitor losses are mainly due to the equivalent series resistance (ESR), so:

$$P = I_{cap}^2 \cdot R_{ESR}, \qquad (4.2)$$

where I_{cap} is the root mean square current through the capacitor.

The quadratic dependence predicted by equation (4.2) is confirmed by experimental results, as shown in Figure 32. The self-heating temperature values measured in the capacitor agree very well to a second order polynomial (depicted with the dashed line in the figure).

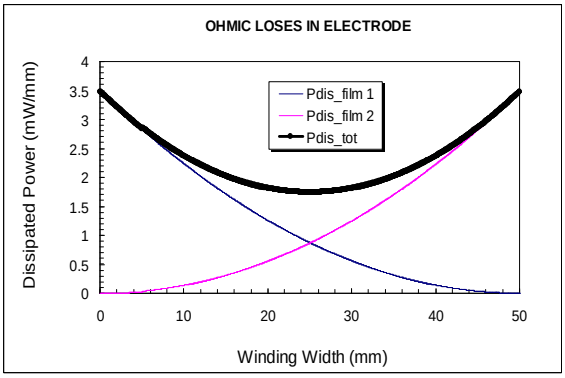


Figure 30. Simulation result of the dissipated power (P) due to ohmic losses in the film capacitor and contribution from each of the electrodes.

The typical behaviour of the ESR for our capacitors as a function the frequency (See Figure 39) shows a slightly increase around 50 kHz. Above that, the value of ESR remains also approximately constant for frequencies as high as 300 kHz. As already stated, this result applies for a wide range of ambient temperatures going from -40º C to 105 ºC.

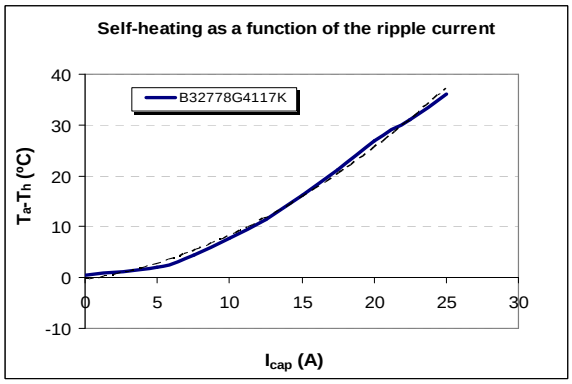


Figure 31. Dependence of the increment of temperature due to dissipation losses in the B32778G4117K (450 V_R, 110 μF) capacitor. Dashed line depicts a second order polynomial.

In [12] a rule of the thumb relation between maximum DC-Link capacitor current and input DC current is used. There might be more specific criteria used for estimating I_{cap}, [16], but in any case and according to the reasoning just exposed, it is safe enough to meet the requirements as follows:

$$I_{cap} < I_{cap,\max}. \qquad (4.3)$$

Note that the exact calculation of I_{cap} will not be in general an easy task, since it will always contain some harmonic components of various frequencies, due to pulse width modulation (PWM) of the inverter.

In order to improve the performance under high frequency ripple currents, and in accordance with prior analysis, the new design has been specially optimised in the contact area, which has been shown to be the most critical area in terms of self-heating,.

In this sense, additional measures cover the generalisation of the 4-pin configuration for higher lead spacing (Figure 27), improving ESR and I_{rms} ratings further. Apart from this, 4-pin configuration also gives a higher mechanical stability for those capacitors, which could be needed in certain situations where mechanical vibrations play a major role.

Given the existing dichotomy between current handling capability and optimised volume, we remark that with the new design, we are able to offer two complementary solutions to the currently existing offer in the market (see Figure 33). On the one hand, the existing High Power series, which gives high maximum admissible current ratings. On the one hand, the proposed High Density series, although slightly lowering the maximum admissible current of existing design, offers much more compact designs and reaches capacitance values above 100 μF. In any case, it is remarkable the convergence of both current ratings for higher capacitance values.

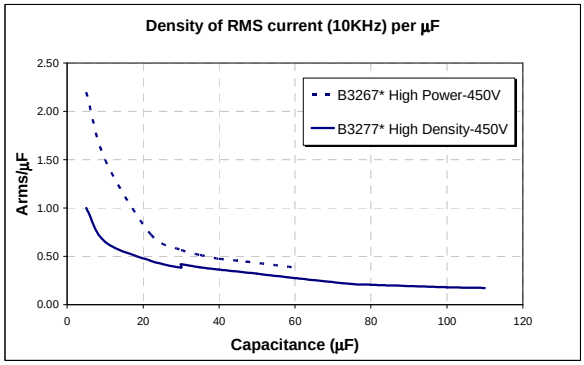


Figure 32. Comparative of maximum admissible I_{rms} current for existing EPCOS High Power and the new High Density DC-link design

4.4. *Validation tests and reliability*

In order to evaluate the performance of these capacitors, several tests have been designed according to the general requirements of the application. Three set of tests have been carried out at different characteristic temperatures for the applications: 70ºC, 85ºC, and finally 105ºC which is the maximum operating temperature for these capacitors.

For the sake of ensuring the capacitor reliability within the product life time, long endurance tests have been carried out under the following conditions:

Test Environmental Conditions	Voltage (rel. to rated)	Duration (h)	Conversion factor acc. IEC 61709	Simulated life* (h)
40ºC/93%rh	V_R	1500	6.09	9135
70ºC	$1.25V_R$	2000	74.36	148720
85ºC	$1.25\ V_R$	2000	171.6	343200
105ºC	$1.25V_{op}$	2000	278.85	557700

In the conditions just described and according to the conversion factors given by standard IEC 61709 [13], tests performed allow us to simulate service life of the capacitor performance for more than 50 years under standard operation conditions (0.5·Vr and 40ºC).

As a result of the tests performed, the following dependence of admissible continuous operating voltage on temperature was found.

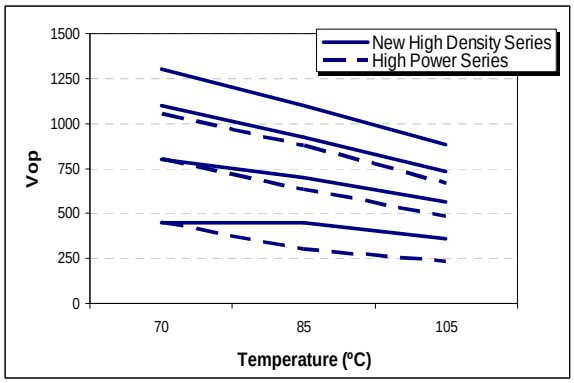


Figure 33. Continuous operation voltages for the high power and the High Density series

According to the data extracted from the analysis of the long endurance tests, the failure rate at standard conditions for this new High Density series has been calculated to be below 50 fit, .i.e. 50 failures per 10^9 component hours with a confidence level higher than 90%. In our particular case, this figure implies at least 100,000 hours lifetime at rated voltage.

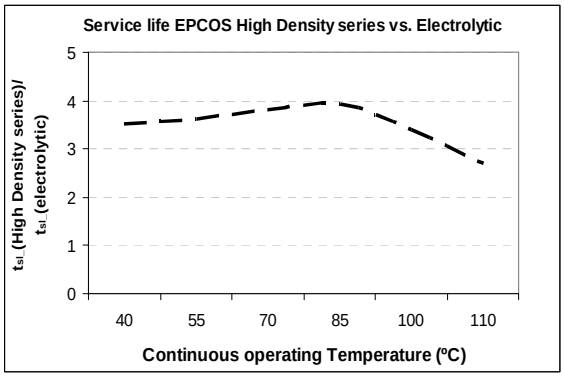


Figure 34. Comparison of the service life (t_{sl}) of our new High Density series with a typical electrolytic capacitor for power applications [14]

Another point of interest refers to the stability of the structure, which is reflected in a consistent good level of service life in a wide window of continuous operating temperatures (see Figure 35). As a reference, we should mention that the expected service life of any of these products will always be between 3 and 4 times that of a electrolytic capacitor, for room temperatures and up to 105ºC.

It is well known the limited life expectancy of electrolytic capacitors, due to the tendency of the electrolyte to dry out after 10,000 hours usage. For each 10ºC working temperature increase, their typical working life is divided by two. This is due to the fact that at lower temperatures, the diffusion of the gaseous parts of the electrolyte through the end seal is reduced and thus the drying of the capacitor is delayed [16].

According to our previous results, it is obvious that substituting the bulky electrolytic capacitor by a DC-link film capacitor is the best option for assuring long life lasting inverters.

4.5. *Product ratings*

The new proposed DC-link High Density design, offers a high reliable solution for new converter technologies covering a wide spectrum of capacitance values and rated voltages that perfectly enhances the already existing series.

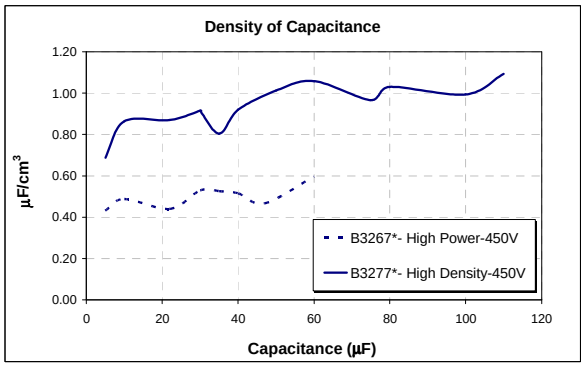


Figure 35. Maximum capacitance range reached with the new design rules of the new high Density series.

The new design rules applied to the High Density series improve existing film designs in different ways: On the one hand, we have been able to reach rated voltages up to 1300V. On the other hand, the de-rating factors applied for temperatures above 70ºC have been considerably improved; especially in the voltages most extensively demanded by the market.

Special mention is deserved to the improvements in the efficiency of the design in terms of the capacitance per unit volume. Figure 36 shows that in most case, we have been able to double current levels of capacitance density, and also extend the range of capacitance above the 100µF.

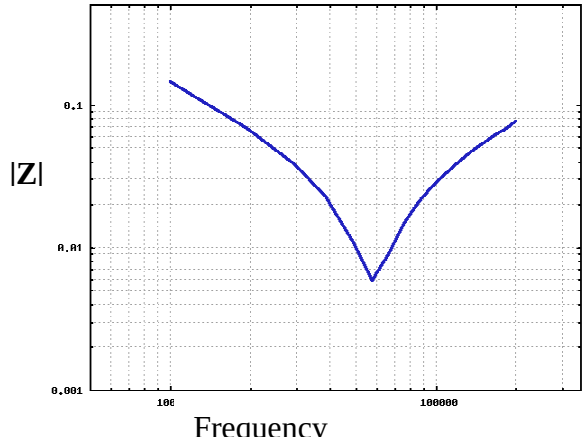


Figure 36. Impedance versus frequency for the 110 µF, 450 V_R capacitor

Impedance, ESR, and ESL values and maximum admissible I_{rms} are also defined for those capacitors, giving to converter designers the basic information to select the right product according to their needs. Figure 37 shows the impedance behaviour with frequency for the representative 110 µF capacitor.

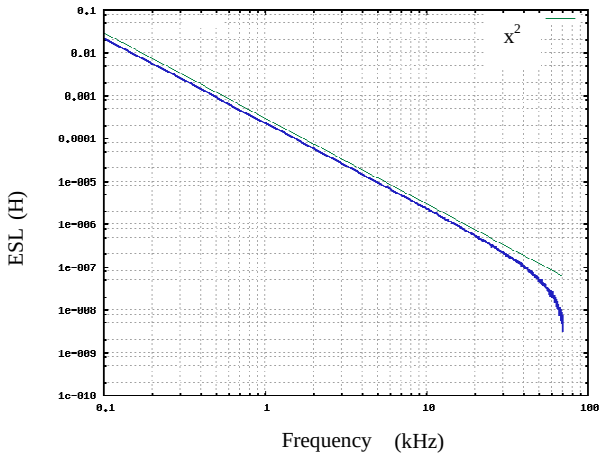


Figure 37. Measurement of the ESL for the 110 µF capacitor. For comparison, an x^{-2} potential law has also been plotted (thin line).

Figure 38 and 39 show typical behaviours of the ESL and ESR (respectively). Referring to this latter, it is noticeable the potential behaviour of the values in a wide region of frequencies. The ESR is on the contrary approximately constant; slightly increasing from very low values measured at frequencies below 100 kHz.

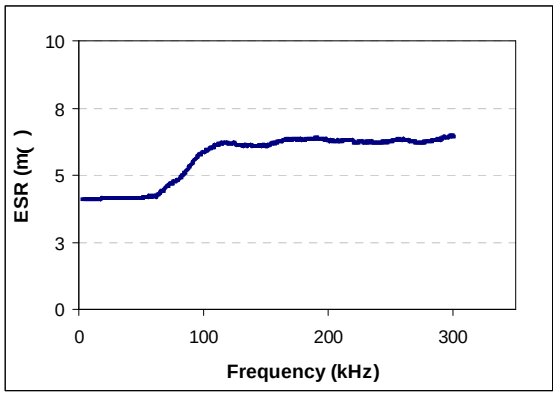


Figure 38. Typical ESR measurement for the 110 μF capacitor.

Additional technical data for those capacitors is listed in the following table:

Working temperature:	-40ºC…+105ºC
dV/dt:	up to 100 V/μs
Tan δ (at 20ºC and 1KHz):	$< 1 \cdot 10^{-3}$
Riso (25ºC, 65%r.h.):	>30 000 s
DC Test voltage between terminations:	1.5 x V_R for 10 s
Test voltage terminal to case:	2110 Vac, 50 Hz for 10 s

Financial Analysis. Impact of the new design in the final cost of the solar inverter.

Photovoltaic industry is expected to steadily grow in the next years based in two strong pillars, namely strong growth of the demand and cost reduction. Several industry associations around the world have forecasted several scenarios or roadmaps for the evolution of the industry [21, 20, 22, 23, 24, 25]. In the US alone, the following key points are predicted:

- Total installed capacity will increase from 340MW to 9,600MW by 2015.
- The average installed cost in 2015 will be 2.62€ per watt (2.07€ for manufacturing and 0.55€ for construction and installation.
- Direct employment will increase from 20,000 now to 62,000 by 2015.

In Europe, the European Commission has set a target of 22% contribution of renewable energy sources to electricity for 2010. Countries like Holland are going further and forecast 25% of PV contribution to the national electricity production [24]by 2050. New PV technologies for and applications are planned for solar cells, modules … [22] for achieving this and successive targets, the costs for on-grid systems are expected to fall from current 6 €/Wp (for 5 kWp systems) to 3.6 €/kWp [22]. This particularly implies a price erosion of 5% per year in all components (modules, inverters and installation).

Japan is nowadays the global leader in both PV production and installed capacity, an ambitious future for PV technology is also expected. It is expected that by 2030 PV power generation could supply 50% of residential electricity consumption (that would approximately mean 10% of total electricity consumption) [20]. In this year, PV power generation will be fully competitive with other energy resources by achieving an approximate cost of 0.05 €/kWh (current cost is 0.33 €/kWh).

In summary, total installed capacity world-wide is expected to multiply by a factor of 1000 in 30 years [22]. Current applications of PV electricity generation is divided into four categories:

- Grid-connected systems 71% market share in 2002 [22]
- Off-grid industrial applications 15% “
- Rural electrification in developing countries 7% “
- Consumer applications 7% “

Currently the market is dominated by grid connected systems, with Japan and Germany having the highest share. A small but high value and promising application is the building integrated PB (BIPV), special PV modules used for facades, roofs or shadowing elements.

The off-grid industrial market is probably the most competitive application of PV electricity generation, compared with other techniques of generation. Rural electrification has a strong added value in terms of providing essential services to isolated areas, or developing countries.
Finally, the consumer market is a constantly growing sustainable market. It implies a wide variety of applications from substitution of batteries in small devices to the electrification of recreational vehicles…

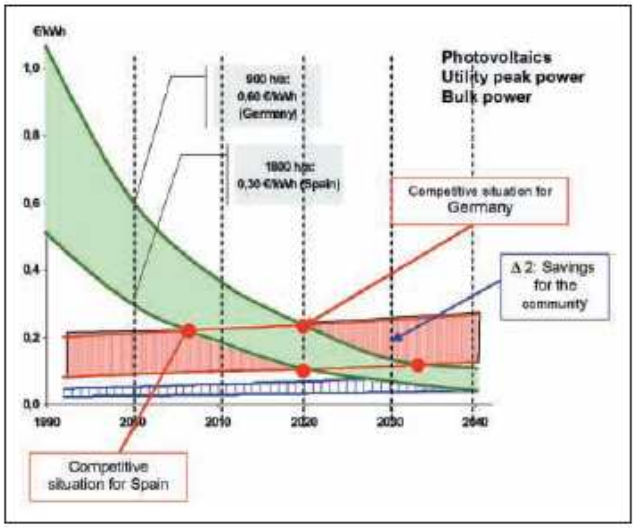


Figure 39. Cost development of PV generated electricity vs. conventional price of electricity (source RWE Schott solar [22])

Figure 42 shows an estimation of the cost development of the electricity versus the price for electricity produced in Europe by conventional means. The two major references for the market are shown (Spain and Germany). In the case of Spain, it is expected to reach a competitive situation by the end of the 2010, while the situation in Germany will lead to a competitive situation a decade later. Of course, this behaviour of the market is strongly dependent on the subsidies and the policies for encouraging the use of renewable energy sources.

An additional point of concern with increasing importance is the durability of the PV system [20,22]. Service life of the PV generator will be higher than 30 years, which will demand even longer durability to the components. Two electronic devices are predominant in PV systems: The charge controller in the stand-alone systems with batteries and the inverter for converting DC current to AC. Charge controllers are responsible for the long life of the batteries. Since the battery is an expensive part of the equipment, high quality change controllers are needed for stand alone applications.

The inverter has to fulfil even higher expectations. It is mainly used in grid connected generators, and three properties are essential: high conversion efficiency, extremely long life, and meeting the safety requirements of the utility. The quality of the inverter must fit to the highest industrial standard, while the price of the device should be reasonable.

Expected service life for the inverter must be extended to 35 years and beyond [22]. In what refers to cost reduction, strong efficiencies should result from large production quantities. In this respect, standardisation of components and systems is important for mass production. This scenario is clearly depicted in Figure 43.

Finally, a matter of concern that will have direct influence on the economical feasibility of the photovoltaic project is the efficiency of the system [30]. Assuming a 4000 Euro installation cost per kW and a nominal power of 3 kW, we get 120 EURO per 1% gained efficiency [27]. Although IGBT and PWM strategies are key factors for the efficient performance of the inverter, the capacitor selected has also its importance.

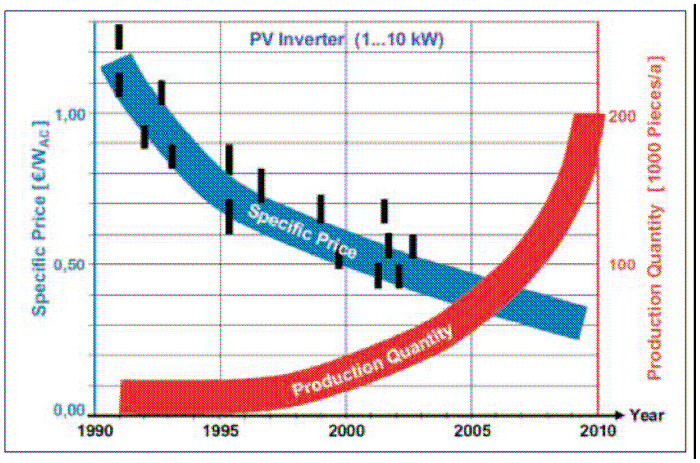


Figure 40. Development and prognoses of specific cost and production quantity for different range of PV inverters [22].

The solar inverter

Reliability and cost efficiency are therefore two key points for PV systems, directly pointing to the inverter. In the following sections we will analyse the effect of the proposed film capacitor design in the performance of the inverter, but also the impact on the cost of the final product.

5.1.1 Cost structure

The most expensive part of a solar generator is the module, which can be up to 75% of the total cost. The inverter roughly represents 10% of the overall cost. The impact of the capacitor in the inverter is actually difficult for estimate, for different factors may affect mainly due to the type of inverter, the topology or strategy used, as well as the capacitance finally selected for the DC-link bank.

In general terms, it is well known that electrolytic capacitors need to be overestimated, for the capacitance drift during service life is not negligible, as it is in film technology. Besides, if electrolytic technology is selected, the inverter should include several extra diodes in order to avoid destruction of the capacitor due to possible current inversions. In case of film technology this would be also unnecessary, for film capacitors perfectly withstand current inversion.

5.1.2 Reliability

Since already discussed, service life is a key parameter for the inverter, that has a direct effect on the economical performance of the photovoltaic system. The estimated service life for film capacitors, as calculated in section 4.4, is at least one order of magnitude longer than the typical values found for electrolytic technology [26]. Besides, the effects of voltage and temperature on the service life are much stronger in electrolytic technology than for film capacitors (see Appendix I).

We can estimate the effect of the higher reliability of film technology in the following way. Given a solar project whose service life is 30 years. A solar inverter with a DC-link bank based in electrolytic technology would typically be able to offer a service life at operating conditions in the range of 5 years. In the cost analysis for the project, there should be included a system maintenance and replacement for the inverter. This would increase the overall cost

of the project, at least, in 20%, supposing that 2 replacements of the electrolytic inverter are required during the lifetime of the project (remember that the inverter is roughly 10% of the total cost of the project). Film capacitors, on the contrary, using the proposed design in this work, would offer reliability levels in the required range, therefore multiplying the expected life of the electrolytic by 6. No extra cost increase on the project are required, for replacement is unnecessary and maintenance is strongly reduced.

Conclusions

1. Thermal stability, efficiency and reliability are key requirements for modern industrial designs that are now perfectly accomplished by the film capacitor technology proposed in this project.

2. In solar inverters, the DC bus selection should be based in the current handling capability. The conventional design using multiple bulky electrolytic capacitors can thus be completely replaced with a single high-current film capacitor.

3. In fact, high current film capacitors satisfy not only the ripple current requirements, but also the life expectancy needed in a solar inverter.

4. The DC-link capacitor design proposed in this project is much more compact than already existing versions in film technology, reaching competitive levels of capacitance per unit of volume even when compared to some electrolytic designs.

5. New developments in film technology allow to offer very competitive products in terms of density of capacitance, in the most relevant voltage range 450-900V for medium power inverters. A wide range of capacitance values can be offered going up to 110 μF in a reduced volume of 35x50x57.5mm^3

6. By enhancing the dielectric strength of the film, rated voltages have also been optimised, reaching up to 1300 V.

7. De-rating due to high temperatures (environment temperature above 85ºC) have also been reduced thanks to the innovative design. Validation tests have shown a correct performance up to a service life of 100,000 hours at normal operating conditions.

8. The new DC-link film capacitors exhibit low inductance, and thus the voltage overshooting during device switching can be substantially reduced.

9. With a low inductance power bus bar design along with the use of low inductance DC link High Density film capacitors, it is possible to eliminate the DC snubber capacitor for additional size and cost reduction.

Appendix I. Basic concepts of product reliability

I.1 Reliability

The European Power Supply Manufacturers association defines reliability in their "Guide to Understanding Reliability Prediction" as the probability that a piece of equipment operating under specified conditions shall perform satisfactorily for a given period of time. Two significant parameters are usually given concerning the reliability of our different products: **Failure rate and service life**. Both figures are always given referred to certain environmental and electrical conditions. While the failure rate is usually given in the conditions indicated in the standard IEC 1709 [13], more realistic conditions are often used for the service life. In any case, in the following sections it will be shown how to estimate the failure rate and service life of our products for operating conditions different to the standard reference temperature and voltages.

I.2 Failure rate (long-term intrinsic failure rate)

The failure rate or **intrinsic failure rate** (λ) of any product is the **statistical number of units** failing per unit of time in the **intrinsic failure period** (see figure below). The failure rate changes throughout the life of the product. In the meaningful period, however, empirical evidence has shown that the failure rate can be assumed constant in time (λ).

The failure rate is expressed in units of fit (fit = failure in time), where 1 fit = $1 \cdot 10^{-9}$/h (1 failure per 10^9 component hours)

I.3 The Bathtub curve

The evolution of the failure rate in time during the lifetime of our products follows the typical *bathtub* curve. Figure 44 shows the characteristic shape of this curve, highlighting the three main regions that can be distinguished in a typical lifetime of any product. The first region, starting when customer use commences, is characterised by a relatively high but rapidly decreasing failure rate. This is related to what is called **infant mortality**. The time scale here ranges from hours to weeks. After this transient, the failure rate levels off, remaining roughly constant for the majority of the useful life of the product. This long period is usually called **Intrinsic Failure Period,** and the failure rate is then called **Intrinsic Failure Rate**. Finally, if units from the population remain in use long enough, failure rate begins to increase significantly again as materials wear out and degradation failures occur. This is the **wear out failure period**.

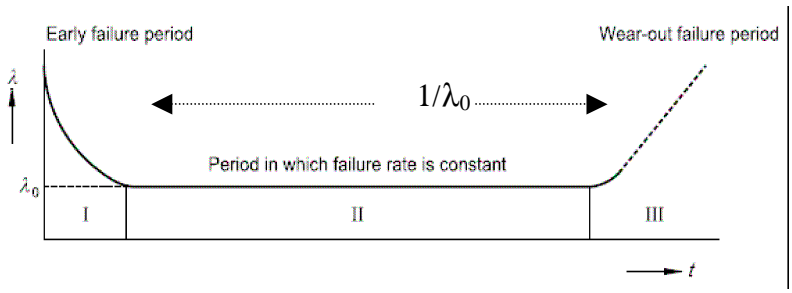


Figure 41. Typical failure rate curve of a product.

It is important to remark that time scales in this figure are arbitrary. In particular, the wear out (III) and early failure period (I) have been represented as much longer than they are in reality,

when compared with the intrinsic failure period (II). In a real case, this latter period covers several decades, and therefore it is clearly much longer than the infant mortality period (which, as it was mentioned, can last a couple of months at maximum). Additionally, EPCOS capacitors are specially treated during production in order to eliminate early failures, and the early failure period is further reduced. The wear out failure period, however, is not as relevant as the other two, for at the end of the intrinsic failure period, most of the samples will have failed. Due to these two considerations, it can be understood why the intrinsic failure period can be interpreted for our products as **the service life of the product**:

$$\text{Service Life} \equiv t_{SL} \approx \text{Intrinsic Failure Period}$$

Failure rates stated in this data book refer to this constant failure rate phase (service period), and, as will be discussed next, they apply to the reference load and reference conditions. The failure rate for each component type is stated in the respective data sheet together with the corresponding reference load and failure criteria. Normally, no failure rate is stated for EMI suppression capacitors because of their direct connection to the mains, where electrical conditions are not stable, and there is a potential for over-voltage to occur.

I.4 Failure rate and mean operating time to failure (MTTF)

Several conclusions can be extracted from the assumption that during the service period, the failure rate, $\lambda(t)$, is actually constant:

$$\lambda(t) \approx \lambda_0 = const. \qquad \text{(A.1)}$$

In particular, it can be demonstrated that the distribution of failures is exactly exponential in this approximation, being the cumulative distribution function:

$$F(t) = 1 - e^{-\lambda_0 t}. \qquad \text{(A.2)}$$

This function gives the probability that a product fails by a specified time *t*. It is often interpreted as the population fraction failing by time *t*.

The *reliability function*, R(t), also called the survival function, is often interpreted as the population fraction surviving time *t*. R(t), being the probability of success, is therefore the complement of F(t):

$$R(t) = 1 - F(t). \qquad \text{(A.3)}$$

Finally, another extremely significant definition is the mean time to failure (MTTF), which in general is the expected life of a non-repairable product. It can be defined in terms of the reliability function:

$$MTTF = \int_0^\infty R(t)dt = \int_0^\infty e^{-\lambda_0 t} dt = \frac{1}{\lambda_0}. \qquad \text{(A.4)}$$

In any case, the MTTF is a measure of the centre of a life distribution. In the exponential approximation, the MTTF is the same as the median of the distribution (most probable case).

At this point, it is essential to understand any figure of MTTF or λ (and any other magnitude derived from them) as statistical averages. A **constant failure rate** actually means that failure occurs **randomly** with a mean frequency given by the inverse of λ. It is also very common

(but completely erroneous) to assume that the MTTF indicates a minimum time between failures, which is absolutely not the case. On the contrary, failures will occur randomly, the distribution being:

$$F(t) = 1 - e^{-\lambda_0 t} = 1 - e^{-\frac{t}{MTTF}}. \qquad \text{(A.5)}$$

It is however true that, for a given period of time [0,t] the bigger the MTTF, the smaller the probability of finding a failure. Suppose we are testing, in the proper climatic and electrical conditions (given by [13]), a high enough number of units of our product (whose λ_0= 2 FIT, i.e. MTTF=$5 \cdot 10^8$ hours). The previous equation is then telling us that after $5 \cdot 10^8$ hours, 63% (~1-1/*e*) of the pieces will have failed. Please observe that even in the ideal case (a very big sample) some of the pieces will have failed before this time ($5 \cdot 10^8$ hours). Attending to the exponential distribution, for example, 1% of the pieces will have failed after ~$5 \cdot 10^6$ hours, i.e. 100 times earlier than the MTTF. We stress, once again, that this is a statistical value that may present some deviations in different realizations.

I.5 Reference conditions and failure rate calculation

As already said, standard failure rate figures are always calculated referred to certain climatic, mechanical and electrical reference conditions. The exact conditions are indicated in the IEC 1709 norm for the different passive components. In case of film capacitors:

- Among others, the relevant **climatic conditions** (as per IEC 721-3-3, class 3k3), read:

Temperature limits	Rate of change of temperature	Condensation
+5-+40 °C	0.5 °C/min	No

Attention is driven in the mentioned standard to the fact **that combinations of the environmental parameters given may increase the effect on a particular component**. As we will be discussing later on this document, this especially applies to the presence of high relative humidity in addition to biological conditions or to conditions of chemically active substances.

- The **electrical stress** should be 50% of the rated voltage at 40°C ($V / V_R = 0.5$).

- The **mechanical stress** is also specified in IEC 721-3-3 with class 3M3

For a correct understanding of failure rate figures, it is essential to take into account that any failure rate estimation is related to these general conditions and applies to the constant failure rate period (as explicitly mentioned in the IEC 1709 standard). Components may however not always operate under these standard conditions. In which case, failure rates different to those given for the reference will be expected.

In the case of film capacitors, the two most relevant parameters affecting the failure rate are temperature and voltage. In the IEC 1709 standard, models for stress factors are consequently applied in order to convert the failure rates under reference conditions to values applying for operating conditions. The conversion should be carried out according to:

$$\lambda = \lambda_{ref} \times \pi_V \times \pi_T, \qquad \text{(A.6)}$$

Where the correction factors are those indicated in following table:

T (ºC)	π_T	T (ºC)	π_T	V/V_R	π_V
≤40	1	110	77	10%	0.26
50	1.8	120	206	25%	0.42
55	2.3	125	346	50%	1.00
60	3.1			60%	1.42
70	5.2			70%	2.04
80	9			80%	2.93
85	12			90%	4.22
90	16			100%	6.09
100	33			110%	9.00
105	50			120%	13.00

I.6 Service life t_{SL}

In the context of the exponential approximation and, following our earlier reasoning, the service life of our product is directly related to the duration of the intrinsic failure period (II, of the bathtub curve), which is also proportional to the inverse of the constant failure rate λ_0. Given the statistical nature of this figure, any estimation for a certain product will be inherently linked to a certain confidence level. We therefore calculate the service life after:

$$t_{SL} = \frac{p}{\lambda_0}, \qquad \text{(A.7)}$$

where *p* is a factor related to the confidence level of the estimation:

confidence level (%)	*p*
37	0.716
63	0.333
75	0.207
90	0.076
95	0.037
98	0.015

It is important to remark that using the proposed formula, the environmental and operating conditions for which t_{SL} applies are exactly those of λ_0. For a detailed example of good use of the formula and the correction factors, see next section.

I.7 Practical example.

Suppose we have a product that will be used at the rated voltage and a stable temperature of 85ºC. For estimating the failure rate of this product, an accelerated endurance test has been performed at the reference conditions (40ºC & $V=0.5V_R$). Further details of the test are:

- Number of component tested (N): 20.000
- Duration of the test (T). 50.000 hours
- Number of failures at the end of the test (n) 1

A good estimator for the failure rate can then be calculated in terms of the total testing time, which results of multiplying the duration of the test by the number of samples tested (TTT = N·T),

$$\hat{\lambda}_{ref} = \frac{n}{TTT} = \frac{n}{N \times T} = \frac{1}{20.000 \times 50.000h} = 1{\cdot}10^{-9}\ h^{-1}, \qquad \text{(A.8)}$$

Accordingly, we conclude that the failure rate of this product operating at reference conditions is λ_0=1 fit:

$$\lambda_{ref} = 1{\cdot}10^{-9} h^{-1},\ at\ (40^{o}C\ \&\ V = 0.5V_R). \qquad \text{(A.9)}$$

The standard factors shown in previous section can be used for calculating the failure rate at the operating conditions:

$$\lambda_0^{op} = \lambda_{ref} \times \pi_T^{85^{\circ}C} \times \pi_V^{V_R} = 1{\cdot}10^{-9} \times 12 \times 6.09\, h^{-1} = 73.10{\cdot}10^{-9} h^{-1} \approx 73\ fit. \qquad \text{(A.10)}$$

And the corresponding service life under the same operating conditions can be then calculated with a *98% confidence level* after:

$$t_{SL}^{op} = \frac{p^{98\%}}{\lambda_0^{op}} = \frac{0.015}{73.1{\cdot}10^{-9}} h \approx 200.000h. \qquad \text{(A.11)}$$

Now, note that if we wanted to restrict our estimation to a lower confidence level, i.e. 90%, the result would then have been:

$$t_{SL}^{op}\Big|_{90\%} = \frac{p^{90\%}}{\lambda_0^{op}} = \frac{0.076}{73.1{\cdot}10^{-9}} h \approx 1.000.000h. \qquad \text{(A.12)}$$

Both figures are compatible, and should be interpreted as follows. For a big enough sample of products that are being tested under the given operating conditions, 98% of the pieces will be fully operative after 200.000 working hours, but after 1.000.000 working hours, only 90% of them will remain.

Appendix II. Glossary.

AC Module

The smallest complete unit that includes solar cells, optics, inverters and other components, excluding tracking devices, intend to generate ac power from sun light.

Ambient temperature

The temperature of the air surrounding the component.

Capacitance tolerance

Permissible relative deviation of the capacitance from the rated value, expressed in per cent.

Category voltage (V_C)

The maximum voltage (expressed in a fraction of the rated voltage) which may be continuously applied to a capacitor at any working temperature inside a range of category temperatures.

Category temperature range

The range of ambient temperatures at which the capacitor can operate continuously. The limit temperatures (**upper** and **lower** category temperatures) are defined in the climatic category.

Climatic category

Numerical code which specifies the limits of the Category temperature range and the duration of a specified humidity test.

Converter

A device that accepts AC or DC power input and converts it to another form of AC or DC power.

Dissipation factor (tanδ.)

Ratio between the effective power (power dissipation) to the reactive power for a sine-wave load of specified frequency, expressed in per cent. Also referred to as Loss factor.

Equivalent series resistance (ESR)

Ohmic part of the equivalent series circuit of the capacitor. It represents the losses associated to the capacitor, due to metallic contacts, polarisation, leakage currents, etc. It is expressed in miliohms (mΩ).

Insulation resistance (RIS)

Ratio between an applied DC voltage and the resulting leakage current, after a specified time. It is expressed in megaohms (MΩ).

$$i_P[A] = C[\mu F] \cdot \frac{dV}{dt}\left[\frac{V}{\mu s}\right]$$

Operating temperature

The temperature of the component under steady operation, which is the addition of the ambient temperature plus the self-heating due to the operation.

Pulse characteristic (k_0)

Characteristic factor of a pulse wave-form, providing its energy content. The maximum allowable k0 defines the capability of a capacitor to withstand pulses involving several current peaks.

$$k_0 = 2\int_0^{\tau}\left(\frac{dV}{dt}\right)^2 \cdot dt\left[\frac{V^2}{\mu s}\right]$$

Pulse-width modulation (PWM)

This is a powerful technique for controlling analog circuits with a microprocessor's digital outputs. Through the use of high-resolution counters, the duty cycle of a square wave is modulated to encode a specific analog signal level. The PWM signal is still digital because, at any given instant of time, the full DC supply is either fully ON or fully OFF. The voltage or current source is supplied to the analog load by means of a repeating series of ON and OFF pulses. The ON-time is the time during which the DC supply is applied to the load, and the OFF-time is the period during which that supply is switched off. Given a sufficient bandwidth, any analog value can be encoded with PWM. Based on the rate of switching, the overall current is able to taper similar to the constant voltage type regulation.

Rated capacitance (C_R)

Capacitance measured at 1 kHz, under standard ambient conditions. This value is normally marked on the product.

Rated temperature

Maximum ambient temperature or hottest contact point at which the rated voltage can be applied continuously. For higher temperatures (up to the upper category temperature) a de-rating of voltage needs to be applied.

Rated voltage (V_R)

The maximum voltage which may be continuously applied to a capacitor at any ambient temperature below the rated temperature.

Rate of voltage rise (dV/dt)

The maximum allowable dV/dt defines the capability of a capacitor to withstand high current peaks due to fast voltage changes. The peak current is the product of the capacitance and the dV/dt.

Self-healing

The process by which the electrical properties of a metallized capacitor, after a local breakdown, are rapidly and essentially restored to the values before the breakdown.

Stand-alone inverter

A PV system intended to supply a local load and does not provide power back to the electric utility.

Time constant (τ)

Time in seconds during which the voltage between the wires of a charged capacitor decreases to 37% due to self-discharging. It is the product of the nominal capacitance and the insulation resistance:

$$\tau\ [s] = R_{is}\ [M\Omega] \times C_R\ [\mu F]$$

Total Harmonic Distortion (THD)

The ratio of the root mean square (rms) of the harmonic content fo the root mean square value of the fundamental quantity, expressed as a percentage.

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