OULUN YLIOPISTO
UNIVERSITY of OULU

DEGREE PROGRAMME IN ELECTRICAL ENGINEERING

MASTER'S THESIS

LTCC PACKAGING FOR LAB-ON-A-CHIP APPLICATION

Author	Joni Kilpijärvi
Supervisor	Anita Lloyd Spetz
Second Examiner	Niina Halonen
(Technical advisor	Maciej Sobocinski)

May 2015

Kilpijärvi J. (2015), LTCC -pakkaus Lab-on-a-chip -sovellukseen. Oulun yliopisto, sähkö- ja tietotekniikan osasto, Mikroelektroniikan ja materiaalifysiikan laboratoriot. Diplomityö, 40 s.

TIIVISTELMÄ

Tässä työssä suunniteltiin, valmistettiin ja testattiin uusi pakkaustekniikka ”Lab-on-a-chip” (LOC) -sovellukseen. Pakkaus tehtiin pii-mikrosirulle, jolla voidaan mitata solujen kiinnittymistä sirun pintaan solujen elinkelpoisuuden indikaattorina. Luotettavuustestaukset tehtiin daisy-chain -resistanssimittauksilla solunkasvatusolosuhteissa. Lisäksi työssä selvitettiin LTCC- ja ”Lab-on-a-chip” -teknologioiden perusteet teoreettiselta pohjalta.

Mikrosirun pakkauksessa käytettiin joustavaa LTCC-teknologiaa. Sähköisiin kontakteihin ja niiden suojauksiin käytettiin sekä johtavia että eristäviä epoksi-liimoja.

LOC-sovelluksiin on tärkeää kehittää uusia pakkausmenetelmiä jotta näiden laitteiden kaikki ominaisuudet saadaan toimimaan luotettavasti. Pakkaus testattiin samoissa olosuhteissa missä sitä tullaan käyttämään ja pakkaus kesti kaikki nämä haasteet. Lisäksi esitetty valmistusprosessi on sellainen, että sitä voidaan käyttää myös muihin ”Lab-on-a-chip” -sovelluksiin.

Avainsanat: LOC, pakkaustekniikka, solumittaus

Kilpijärvi J. (2015), LTCC packaging for Lab-on-a-chip application. University of Oulu, Department of Electrical and Information Engineering, Microelectronics and materials physics laboratories. Master's Thesis, 40 p.

ABSTRACT

This work presents design, manufacturing and testing of new packaging method for Lab-on-a-chip (LOC) application. Packaging was made for silicon microchip which can measure cell adhesion on chips surface as indication of cell viability. Reliability testing was done with daisy-chain resistance measurement in real conditions. Moreover basic theory of LTCC and Lab-on-a-chip technology is presented.

Resilient LTCC technology was used for packaging material and conductive/insulating epoxies were applied for electrical contacts and barriers against the environment.

It is fundamentally important to develop new packaging methods for LOC applications, so all the properties can be utilized reliably. Packaging was tested under the cell growth conditions and the package showed to withstand all these challenges. Moreover the presented packaging method is possible to use also in other Lab-on-a-chip applications.

Key words: LOC, packaging, cell measurement

TABLE OF CONTENTS

ACKNOWLEDGEMENTS

This work was undertaken at the Microelectronics and Materials Physics Laboratories of the University of Oulu and was part of projects funded by the Tekes.

I would like to thank my first supervisor FiDiPRO professor Anita Loyd Spez and second supervisor Dr. Sc. Niina Halonen for opportunity to do this work. I also would like to thank Maciej Sobocinski from his introduction to the LTCC technology. I appreciate deeply you all for reviewing and guiding me through this work. Thanks to Antti Hassinen for making the cell culture tests. Moreover I would like to thank Center of Microscopy and Nanotechnology, especially Pekka Moilanen, for precious technical guidance to get this work done. Also I would like to thank my fellow students, especially Kari and Jarkko, from all studying years and also work colleagues of the laboratory for enjoyable conversations and sharing their scientific knowledge.

The most beloved thanks go to my family and to my girlfriend Suvi for encouraging me to get this work done.

Oulu, May 12. 2015

Joni Kilpijärvi

LIST OF ABBREVIATIONS AND SYMBOLS

ABBREVIATION	Explanation
f	frequency
c	light velocity
λ_g	wave length
ε_r	dielectric constant
μ_0	permeability of vacuum
ρ	conductor resistance
LOC	Lab-on-a-chip
LTCC	Low Temperature Co-fired Ceramics
CMOS	Complementary metal-oxide-semiconductor
PCB	Printed circuit board
FR-4	Glass-reinforced epoxy laminate sheets, printed circuit boards
CAD	Computer aided design
CCD	Charge-Coupled Device
IC	Integrated circuit
MEMS	Microelectromechanical systems
DNA	Deoxyribonucleic acid
MOSFET	Metal-oxide-semiconductor field-effect transistor
MAGFET	Magnetic field-effect transistor
DEP	Dielectrophoresis
FACS	Fluorescence activated cell sorter
PALS	Phase analysis light scattering
DAQ	High speed data acquisition
ACA	Anisotropic conductive adhesive

ICA	Isotropic conductive adhesive
BGA	Ball grid array
PDMS	Polydimethylsiloxane

1. INTRODUCTION

Low temperature co-fired ceramic (LTCC) is very versatile technology due to material characteristics and constantly developing manufacturing processes. It has developed from a simple substrate material technology to a complex microelectronic system which involves packaging, buried passive components, heat sinks, sensors, actuators, micro channels and energy harvesters. This evolution started in the 1980s when DuPont and Hughes made radar chip for jet plane. [1]

Lab-on-a-chip is a technology which incorporates one or more laboratory functions in to a single microchip. Idea of this is that everything is small and integrated around the microchip. Advantages of this are: low fluid, reagent and sample consumption, faster analysis times, better control and accuracy, mobility/disposability, low fabrication costs and easy usability. However, lab-on-a-chip needs still more developing for killer applications. Challenges involving miniaturization makes fabrication and fluid handling more difficult because physical phenomena become more complex. [2]

The goal of this work is to combine these two technologies and design and manufacture robust package for CMOS based lab-on-a-chip 'Cell Clinic' with the LTCC technology. The Cell Clinic is based on a capacitance sensor chip. Traditional packaging methods are inadequate, because CMOS needs dry environment and biology needs wet environment. Joining these two worlds together is the problem solved in this work. This package needs to withstand hostile environment and still enable the chip to make measurements on cells. LTCC ceramic material is well suited for this challenge because of the material characteristics and flexibility of LTCC processing technology.

1.1. Low temperature co-fired ceramics technology

Low temperature co-fired ceramic (LTCC) material which normally consists of composite substrate made of ceramic particles and glass (green sheets). Low temperature means that maximum process temperature is between 850 - 1000 °C. Conductors are made from paste containing high electric conductivity metals and which are typically screen printed on green sheets and then sintered in one step (in the other words co-fired). Other methods can also be used like sputtering and photolithography. These green sheets can be stacked and made to form multilayer structures. This technology allows integration of embedded components like resistors, capacitors and coils seamlessly into the substrate. Moreover mounting active and passive components, such as, microchips and heat sinks, on surface of the LTCC is possible. Because of these LTCC specific features high packaging density is possible. [3]

Ceramic materials have low transmission loss at high frequencies. Transmission loss at high frequencies ($1/Q$) is identified with dielectric loss ($1/Q_d$) and conductor loss ($1/Q_c$) which depends on surface resistance R_s. Conductor loss dominates attenuation on low frequencies (<1 GHz) and dielectric loss at high frequencies (>1 GHz). Equations 1 and 2 are used to calculate these characteristics. [1]

$$\frac{1}{Q_d} = \frac{20 * \pi * \log e}{\lambda_g} \tan\delta = 2{,}73 * \frac{f}{c}\sqrt{\varepsilon_r} * \tan\delta \left(\frac{db}{m}\right) \quad (1)$$

Where λ_g is wave length, f is frequency, c is light velocity, ε_r is dielectric constant and $\tan\delta$ is dielectric loss tangent;

$$Rs = \frac{1}{d * \sigma} = \sqrt{\frac{\pi * f * \mu_0}{\sigma}} = \sqrt{\pi * f * \mu_0 * \rho} \quad (2)$$

Where f is frequency, μ_0 is permeability of vacuum and ρ is conductor resistance

High frequency properties of LTCC material are superior compared to polymer based printed circuit board (PCB). At 2 GHz alumina/borosilicate LTCC material has dielectric constant ranging from 5 to 8 and most common PCB material FR-4 (epoxy + EGlass 60 wt.%) 4.3 and dielectric loss tangent for LTCC is 0.005- 0.0016 and for PCB 0.015, respectively. With this concept advanced high frequency applications can be made on LTCC including communication devices such as Bluetooth, wireless LAN, in-car radar and GPS. [3]

LTCC has also another perk; excellent mechanical and electrical characteristics in harsh environment such as high humidity, chemicals, high temperature and vibration. For example thermal expansion coefficient for LTCC 3-4 ppm/°C versus FR-4 16-18 ppm/°C, if this coefficient is large thermal stress may lower especially silicon chip electrical connection reliability significantly [3]. Moreover LTCC enables rapid prototyping since layouts are made with computer aided design (CAD) and only few process steps are needed. Furthermore this shortens the time to get ready products in the open market. Additionally sensors, actuators and microsystems with lab-on-chips can be implemented on LTCC substrate enabling a broad spectrum of applications. [1]

Typical manufacturing process for making multilayer ceramic substrates is shown in figure 1. First raw material powder and binder is chosen for the application. Then ceramic, glass and organic binder are mixed to make slurry compound. The slurry is poured in container and forced to go between “doctor blade” and moving tape. Then after drying, solid sheets, called green sheets, are blanked to specific sized blocks. At this stage green sheets are soft and flexible like paper. Next vias are formed by laser cutting or mechanically punching followed by via filling with conductive paste. Moreover, conductors and other functional materials, such as, resistors and dielectrics, are screen printed to the substrate. Then multiple green sheets are arranged in layers and they are laminated to form a stack. Last stage is firing (also called sintering) and final inspection. [3] It is also possible to machine the LTCC material also after sintering with laser or diamond tools and make post process printing. [4]

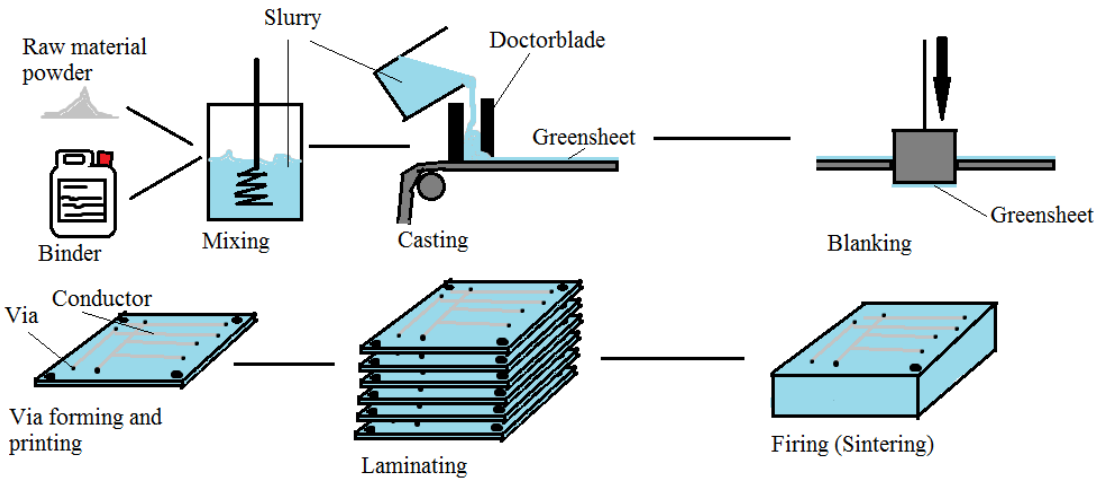


Figure 1. Typical manufacturing process for multilayer ceramic substrates.

Raw material powder is made from great variety of pretreated materials. This powder consists of inorganic ceramic and glass powder. The organic materials added to the powders, such as binders, plasticizers, dispersing agents and solvents, have significant impact on the ability to shape the material. The compounds are formed into slurry by mixing them in ball mill or similar device. [3]

In casting stage the green sheets are formed from slurry. Most important part of the casting device is the casting head where slurry is dispensed on to the moving carrier film through gap formed by doctor blade. This gap height determines thickness of the green sheets. Green sheets need to be dried before further processing. This is normally done by infrared heaters or hot air. After drying the mechanical strength of the green sheets need to be sufficient to withstand handling in the subsequent processes.

The green sheets are blanked to desired size and vias for conductors and other uses, e.g., heat sinks, are made by punching, drilling or laser cutting. These methods can be used also for making cavities and micro-channels [5]. Then using printing technique called screen printing (also called gap printing) materials, such as, conductors, resistors, and dielectric patterns, are printed on the green sheet. In this method conductive, resistor or dielectric paste is squeegeed through screen on to the substrate. This process is shown on figure 2. Screen is made from steel wire mesh and polymer emulsion with precise gaps patterned on it. As mentioned before green sheets are flexible like paper before laminating and sintering, furthermore green sheets are also porous. Porosity is desirable because paste solvent can penetrate the surface of the green sheet resulting in good adhesion after firing. [3]

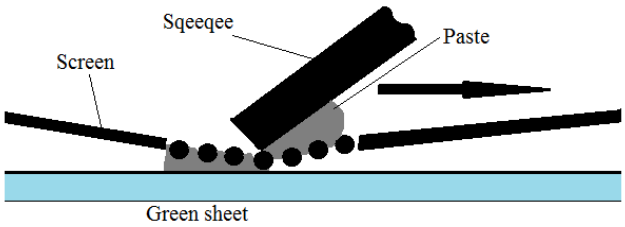


Figure 2. Screen printing process

Processed green sheets are then laminated to form a multilayer module by aligning the sheets to each other. Aligning is done with help of CCD cameras, aligning marks and x-y- θ stage. After aligning the stack of green sheets is laminated with heat and

pressure. Heat is applied because it activates binders (organic resins) which increase the adherence between layers. [3]

When using conductors with low resistance, such as copper (Cu), gold (Au) or silver (Ag), the sintering temperatures need to be below melting point of these materials which are 1083, 1063 and 960 °C, respectively. Ceramics (typically alumina (Al_2O_3)) have high melting points so glass is inserted as binder to the LTCC composite. Glass acts like a glue which keeps ceramic particles together after sintering. Figure 3 shows ceramic composite before and after sintering. Glass particles melt into liquid form and as the particles cool down they bind ceramic particles together. Precise control of sintering process is the key to manufacture LTCC substrates with desired properties and high quality. [3]

LTCC Ceramic material shrinks and densifies during sintering due to diffusion of particles and the reduction of pores. This phenomenon needs to be taken into account as shrinkage rate can be defined and compensated during the design. LTCC ceramic manufacturers provide the shrinkage information on the datasheets of the tapes. [3] There is also zero shrinkage LTCC tapes, like Heraeus HeraLock® Tape HL2000 which is used also in this work.

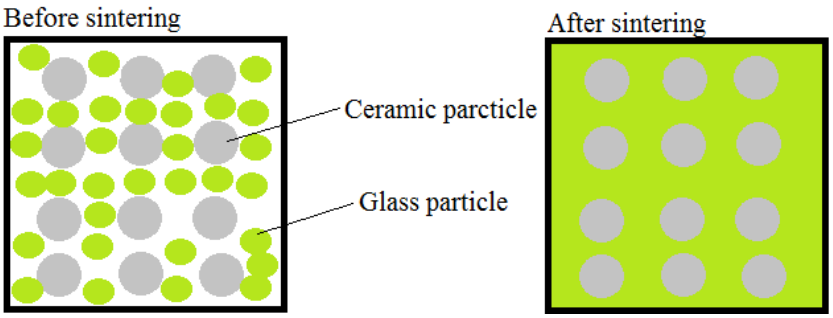


Figure 3. LTCC material before and after sintering.

It is possible to mount active components such as silicon chips on LTCC substrate. Common conductor pastes (Ag, Cu, Ni, Au, Pd and their alloys) used in LTCC top layer have excellent solder wettability. Solder wettability in principle means how strong the adhesion is between solder and substrate, although conductors with poor wettability can be plated with thin layers to improve adhesion. Two typical bonding methods for bonding are flip chip bonding and wire bonding, which are shown in figure 4. [3]

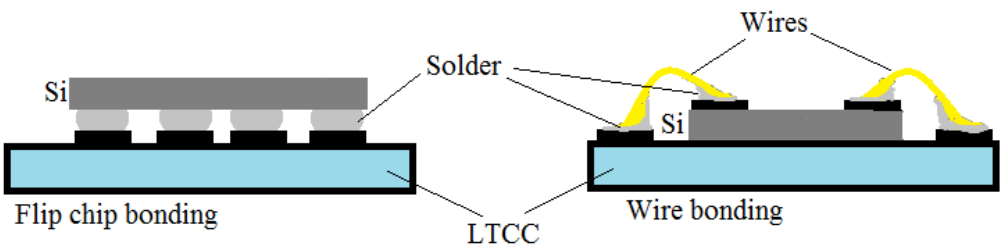


Figure 4. Typical chip bonding methods, flip chip and wire bonding.

1.2. Examples of LTCC biological applications

K. A. Peterson presented, at 2005, a paper where application called Cell Lyser was demonstrated. This device has LTCC substrate with channel surrounded by heating elements. The device can heat to 180°C killing unwanted spores from the sample and leave proteins intact. Fluidic channels are made so that fluidic ports can be glued on input and output. [6]

The LTCC technology was used to manufacture Micro Ceramic Cell Analyzer, this compact, simple and inexpensive device was presented on paper made by Malecha et al. 2007. Device consists of optoelectronic components integrated on LTCC. Components included light source (UV led), photodetector, light guide and chamber for biological material. It measured fluorescence of the biological sample on the LTCC substrate. Device showed response to various concentrations of E. coli and S. cerevisiae cells, and number of cells can determined. [7]

1.3. Lab-on-a-chip

Lab-on-a-chip (LOC) is a device that integrates one or several laboratory functions on a single microchip. Size of the microchip is on the scale of few square millimeters to centimeters. This small size means also faster measurements, on the order of seconds rather than minutes like with conventional measurement systems [8]. LOC may possess many applications such as chemical analysis, environmental monitoring, and medical diagnostics. [2] However, this chapter presents only medical diagnostics focusing cell analysis. Figure 5 presents the number of articles, conference papers and reviews in www.scopus.com (31.3.2015), with search word "Lab-on-a-chip".

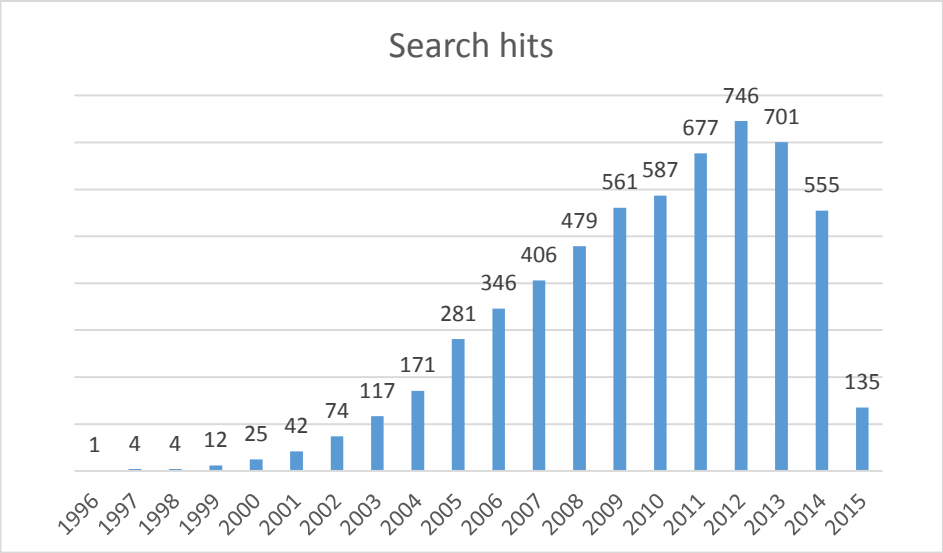


Figure 5. Search hits on www.scopus.com.

Key aspects of lab-on-a-chip are miniaturization and integration. These subjects are strongly connected to integrated circuit (IC) technology including complementary metal oxide semiconductor (CMOS) technology. CMOS is matured technology and it is relatively easy to implement to the LOC structures. Also new technologies such as microelectromechanical systems (MEMS) has been used. [2] MEMS may be

implemented also with other substrate materials, such as ceramics, plastics, quartz and glass, instead of commonly used silicon. [8]

Lab-on-a-chip is usually a very complicated device. LOC devices have extremely small cavities and flow systems (in µL and even pL scale) [8]. Therefore these devices can utilize small fluid volumes. LOC possess three major function categories: actuators, sensors, and readout circuits. Actuating means moving the sample, usually in liquid form (e.g., cell medium), inside LOC with mechanical (e.g. syringe) or electrical forces (e.g., electric field or magnetic field). Sensors measure electrical, optical, magnetic or thermal properties of the sample. Readout circuit handles signals (e.g., amplifiers and filters) and provides interface to outside world (e.g., computers). [2]

1.3.1. Electrical and physical behavior of cells

Lab-on-a-chip can be used to measure cells since these act like particles which have electrical and magnetic properties. A cell is the building block of life and the smallest unit of an organism that is classified as living. All the cells are formed from preexisting cells by division. Cells absorb and emit energy and these processes are called metabolism and biochemistry. There are unicellular (single-celled) and multicellular (more than one cell e.g., humans) organisms. The cells can be subdivided into two categories; simple prokaryotes and more complex eukaryotes. Both cell types have cell membranes (which are different for animals and plants cells), but unlike prokaryotes, eukaryotes have distinct membrane-bound organelles and nuclei with organized chromosomes which contain genetic material known as DNA. Eukaryotes are also 10 times bigger and 1000 times greater in volume compared to simple prokaryotes. Most of the interior of the cells is salty liquid called cytoplasm. [2]

Two kind of basic models are used to characterize cells. Single-layer model, shown in figure 6, can be used to prokaryotes because of their relatively simple structure. Membrane is characterized by effective capacitance and conductance. Cells interior (cytoplasm) is simplified as homogenous with permittivity and ohmic conductivity. Double-layer model, presented on figure 6, is used for eukaryotic cells. This model mimics also nucleus which is located inside the membrane. Four distinct regions with different electrical regions are modeled. Cell membrane, cell interior (cytoplasm), nuclear membrane with selectively bilayer of lipid protein molecules, and nucleoplasm. The cell wall simulates a homogeneous spherical concentric shell of finite thickness with bulk permittivity and ohmic conductivity. The membrane is set to have effective capacitance and conductance. Cytoplasm is the same like in single-layer model as mentioned earlier. Nucleoplasm is similar to the cytoplasm, simplified to be homogenous model with permittivity and ohmic conductivity. Figure 6 shows single-layer and double-layer models. Also more complex models (e.g. Hodgkin-Huxley model) have been created for the cells which produce electrical signals (electrogenic cells) including brain cells, neurons and heart cells. [2]

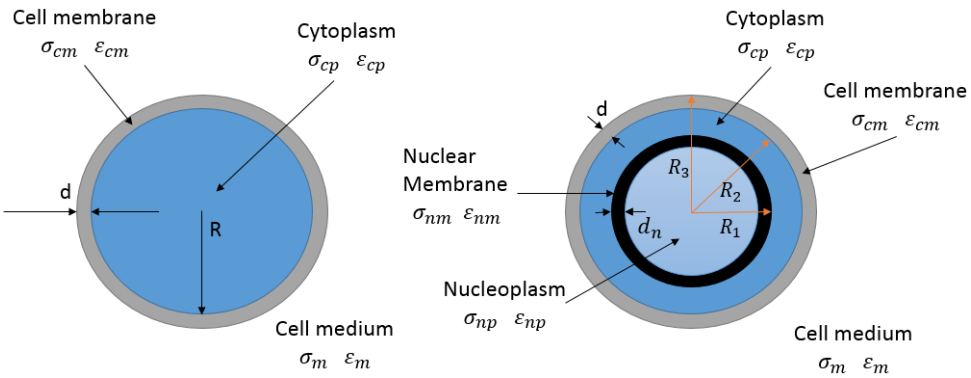


Figure 6. Single-layer and double-layer model of the cells.

1.3.2. Sensing techniques

Cell sensing techniques of LOCs are basically the same as in bulky equipment. Examples are optical, fluorescent labeling, impedance sensing, capacitive cytometry and magnetic field sensing techniques. It is preferable to have a measurement system, which can be entirely miniaturized.

Optical technique uses photo detectors and laser beam to characterize cells. In principle these systems measure optical absorbance of liquid containing cells. Cells are manipulated by nonuniform electric field. Force on cells is called DEP (dielectrophoresis) force. This way it's possible to characterize positive, neutral and negative cells. One realization of optical technique is dual beam optical spectrometer shown in the schematic figure 7. Dual beam arrangement increases tolerance to fluctuating light and signal-to-noise ratio is improved. [2]

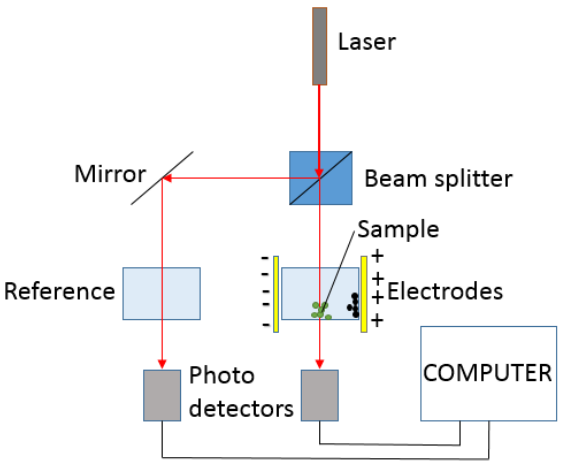


Figure 7. Dual beam optical spectrometer with cell manipulation capabilities (DEP).

Fluorescent labeling technique involves marking the cells with fluorescent dye and then detecting them with optical techniques. The fluorescence-activated cell sorter FACS device is used for this technique. This machine can identify the cells size from wavelength of the scattered radiation they emit. After identification the cells can be sorted to separate containers with DEP forces. [2] A schematic picture of the FACS measurement system is shown in figure 8. Partly miniaturized device, µFACS, is demonstrated in a paper by Fu, A. Y. et al [9].

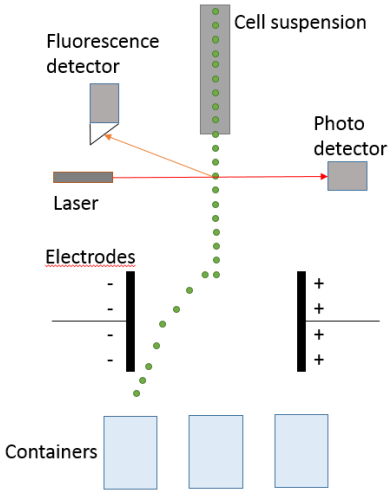


Figure 8. Fluorescence-activated cell sorter (FACS).

Impedance sensing technique may be realized by micromachining and utilizes the impedance change ΔR between electrodes when a cell goes through a microchannel. There are more than one electrode pair so that reference electrodes are inherently switched. This way also the speed of the cell in the microchannel can be measured. In these systems it is important that the microchannel between the electrodes is as small as possible because sensitivity is then increased. Moreover, energy consumption becomes minimal. The output signal is realized by differential variation of the impedance Z_{ac}-Z_{bc}. Similar capacitive cytometry technique, also based on micromachining technology, measures change in total capacitance, ΔC_T, across electrodes using AC voltage and different frequencies. The current change between the electrodes is differentially measured and then analyzed to determine the dielectric properties. Dielectric properties reveal information about membrane resistance, membrane capacitance and cytoplasmic conductivity [10]. With this method it is possible to quantify DNA content because DNA is a highly charged molecule. Figure 9 presents the idea of impedance and capacitive cytometry technique.

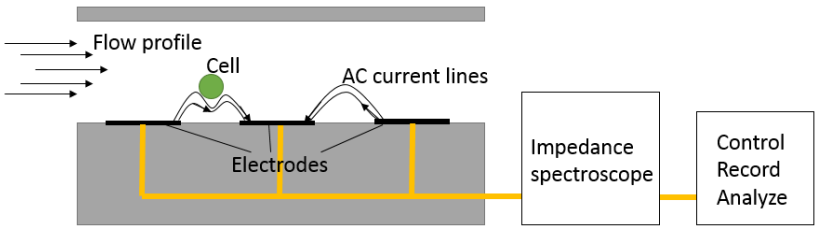


Figure 9. Schematic side view of the microchannel with impedance/capacitive cytometry sensing capabilities.

The magnetic field sensing technique uses magnetic field and a metal-oxide-semiconductor field-effect transistor (MOSFET) to measure changes in the field when cell passes through. Magnetic field-effect transistor (MAGFET) is a MOSFET with two drains and it is implemented for this technique. [2] Table 1 presents comparison between different sensing techniques.

Technique	Tasks	Miniaturization	Cell damage	Advantages	Disadvantages
Optical	Selective separation depending on charge of the cell (positive, negative, neutral)	No	No	Ability to characterize cells with DEP based on positive, negative or neutral charge.	Bulky and expensive.
FACS (fluorescent activated cell sorter)	Selective separation, and size measurement	Hybrid possibility(e.g. µFACS)	Cell modifying by fluorescent labeling	Impressively fast and efficient sorting	Expensive, mechanically complex and bulky. Complex to operate. Needs cell modification
Impedance sensing, capacitance cytometry (CellClinic presented on this paper uses this tecnique)	Counting, population study, trapping, size, velocity, information inside the cell	Yes	No	Reference comes naturally, many different tasks	No actuating capability, needs microfluidic techniques to move cells in the device
Magnetic field sensing	Control and manipulating of cells, detection	Yes	Paramagnetic micro-bead labeling	Quite simple	Temperature dependent large offset

Table 1. Comparison of different cell detection techniques.

1.3.3. Examples of LOC devices

Chiem and Harrison (1998) presented microchannels and electrodes made on glass substrate (7.6 x 7.6 cm) to mix, react, separate and analyze serums. They used microlithographic patterning technique and HF/HNO_3 acids to etch microchannels and cavities. Liquid was moved by electroosmotic pumping, in other words by electric fields. Instrumentation was done by two power supplies/relays (30kV) and laser-induced fluorescence. Emission was measured by microscope objective and optical bandpass filter. Also photomultiplier tube was used. The device integrates entire groups of laboratory steps used in clinical analysis. Performance is comparable with conventional instrumentation, expect analysis times, which was shorter. This device was designed for rapid reporting of critical analyses in emergency situations. [11]

Müller et al., (1999), introduced a 3-D microelectrode system for handling and caging single cells and particles. This device consists of two layers of electrode structures separated by a 40um thick polymer spacer. The device can focus, trap and separate eukaryotic cells or latex particles with diameter of 10-30um using negative dielectrophoresis (nDEP). It operates by changing AC fields between electrodes. Two fabrication methods are presented, laser ablation and photolithography

This system can successfully handle and trap single cells/particles and allow population of one to several hundred single particles to be controlled and addressed individually. This is also a contact free method. Also using electrorotation characterization (particle rotation as a function of field frequency shows one peak for homogeneous particles) of cells dielectrically is possible. Instrumentation like fluorescence correlation spectroscopy, optoelectronic data recording and PALS can be used. [12]

Manaresi et al. published the paper 'A CMOS Chip for Individual Cell Manipulation and Detection' (2003), which presents a 8 x 8 mm^2 device. The chip can perform parallel experiments on individual cells, detect and isolate rare cells from very small sample volume, possibly selectively deliver controlled amounts of compounds to target cells and has the possibility to investigate in real time the dynamics of cell response to chemicals and to cell-cell interactions. Structure is made of two-poly three-metal 0,35 µm CMOS technology, and it consist of 102 400 actuation electrodes arranged on an array of 320 x 320, 20 µm x 20 µm microsites. Every microsite has addressing logic, embedded memory and an optical sensor. The software controlled device can handle up to 10 000 individual cells. This is a noninvasive method and uses DEP force (nDEP and pDEP) to manipulate cells. Also DEP cages are used, which can trap cells and then they can be moved. [13]

Liu et al. (2004) published the paper "Cell-Lab on a chip", which describes a MEMS-on-CMOS device to encage, culture and monitor cells. This system was developed to perform long-term measurements on arrays of single electrically active cells. Also a MEMS process was developed to manufacture closeable micro-vials for cells. [14]

Mina et al. approach "spectrophotometric analysis of biological fluids" presented in a paper published 2005. The device included: microfluidic system; optical filtering system based on Fabry-Perot optical resonator using a stack of CMOS compatible thin-film layers; and CMOS detection/readout (photodiode array) system. Output of this device is a signal proportional to the intensity of the light transmitted through the biological fluids. The Fabry-Perot resonator allows the use of white light illumination, so no need of complex light sources. The lab-on-a-chip presented here is inexpensive

because of utilizing well established CMOS/SU-8 manufacturing processes. Also, it makes this LOC device disposable. Performance was successfully demonstrated measuring uric acid and total protein in human urine. Highly selective filtering system makes this device broadly applicable to other types of clinical diagnostics. [15]

Yun et al. (2005) demonstrated a microfluidic device for a fast and parallel single-cell based assay. The system captures single-cells or beads passively and specific reagents or drugs can be injected to the target cell. The device consists of surface-modified silicon channels capped with a grooved polydimethylsiloxane (PDMS) cover layer, and an electrochemical measurement system.

Cells/beads are trapped in a microfluidic channel passively using hook-shape and a narrow drain channel where fluid can flow until the cell is immobilized. This is achieved using a hydrophilic region. The drug injection channel has hydrophobic region, which allows also air/bubbles to leak out, while overflow of drug is drained through a separate drain channel.

Tests were successful with polystyrene beads and CHO DG44 cells. Also simulated drug (ink) was injected into the target cell without air introduction. [16]

Group Blazej et al. (2006) developed a bioprocessor for integrated nanolitre-scale Sanger DNA sequencing. The Sanger method has ability to generate long and accurate sequence reads compared to other methods. The device consists from three Sanger sequencing steps, thermal cycling, sample purification and capillary electrophoresis. PDMS wafer-scale construction was used to combine 250-nl reactors, affinity-capture purification chambers, high-performance capillary electrophoresis channels, and pneumatic valves and pumps onto a single microfabricated device. To achieve all steps the device is multilayer with hybrid glass-PDMS assembly.

The device was constructed from three patterned (100mm diameter) glass wafers and a PDMS (254um thick) membrane. Patterns were photolithographically transferred to the glass wafers and etched to a depth of 30um. Holes were drilled for electric, pneumatic, fluidic and interlayer access. Glass and PDMS wafers were bonded in a vacuum furnace, forming all-class enclosed surfaces. Also a 10mm diameter surface heater is mounted underneath the thermal cycling reactor.

Thermal cycling (voltage) and microvalve actuation (pressure) are controlled by computer software (LABVIEW). [17]

Research made by Chin et al. (2011) presents a lab-on-a-chip device which can run diagnostic tests of infectious diseases in the developing world. They managed to integrate all steps of ELISA in an easy-to-use point-of-care (POC) system. (ELISA is the clinical standard for detecting most protein-based biomarkers.) POC means that it is as easy to use as a mobile phone and does not need user interpretation of the signal. The chip had performance equal to reference bench top assays in the diagnostics of HIV using only 1uL of unprocessed whole blood. The presented device is also made low cost and available for mass production.

Another paper presents three new microfluidic innovations. First, development of high-throughput manufacturing of microfluidic cassettes at low cost. This is achieved by manufacturing the device from transparent polystyrene and cyclic olefin polymer from single mold. The ELISA technique needs 14 separate reagents to get enough strong signal trough enzyme-mediated signal amplification. Second, they used bubble actuated reagent delivery system, therefor no need of moving parts, electricity or external instrumentation in the micro channels. Bubbles are moved by a syringe integrated in the device. Finally, they needed signal amplification and detection using minimal instrumentation. They used reduction of silver ions onto gold nanoparticles

in an “immunosandwitch”. This allows signal to be amplified on a solid substrate under continuous flow of fluid. Optical density of the silver film can be measured by LED and photo detectors.

They made tests with real specimens from 70 known HIV status patients. And only one test was false. Also duplex test with HIV and syphilis were successful. So this device works like its “big brothers” expect that it uses a hand held instrument that is no more expensive or complicated to use than a cell phone. [18]

1.3.4. CMOS on LOC packaging

A main challenge for packaging CMOS chip (millimeter scale) on an LOC device is harsh environment, e.g., when the active area of the chip needs to be exposed to liquid (cell growth medium, e.g., electrolyte solution). In addition living cells often require incubator where temperature, humidity and other conditions are controlled. So even non active areas are exposed to difficult conditions.

Different kind of packages are presented in literature to overcome this problem. These approaches are presented in figure 10. To make CMOS chips handheld they are e.g., attached to a wafer. Different materials such as silicon wafer, standard chip package, a printed circuit board or a flexible substrate can be used.

Moreover, the active area of the chip needs to be passivated to prevent cell medium to destroy the CMOS circuitry and yet allow measurement signals to pass through. Finally, it needs to be biocompatible, micromachinable and allow integration of microfluidics. Materials like oxide (SiO_2), nitride (Si_3N_4) or polymers are exploited.

When CMOS chips are made in low volume they become expensive (5-metal, 2-poly CMOS 60-300$ per mm^2). In conclusion, smaller chips are cheaper, but handling of the smaller chips become more difficult. Moreover this requires packaging to be a high yield process meaning less process steps, more yield. Balance between yield and package life-time also need to be carefully considered. [19]

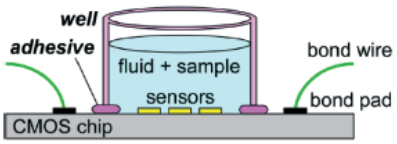
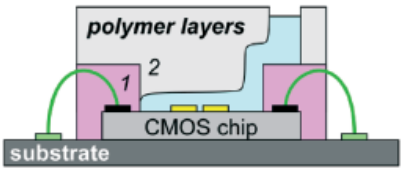
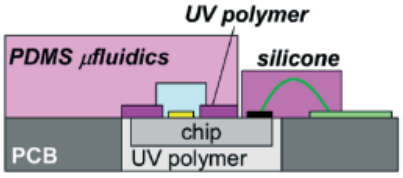
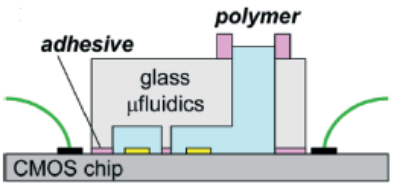
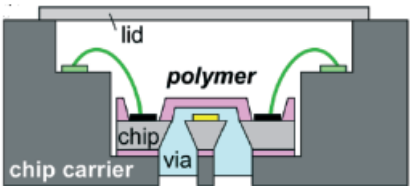
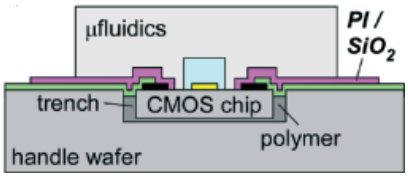
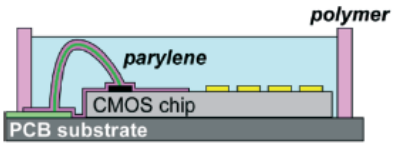
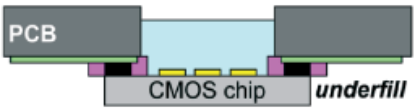
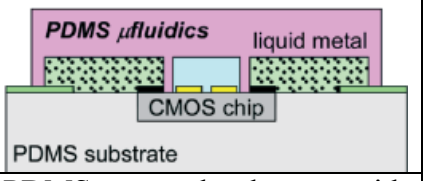
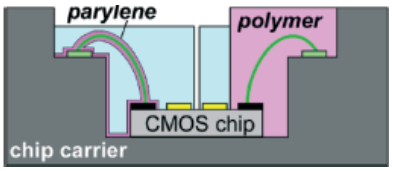
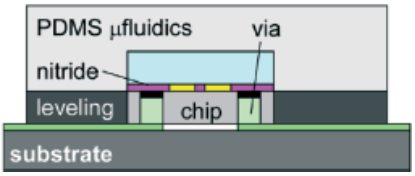
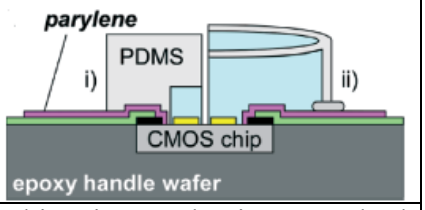
		
A large die with well glued on top.	First layer capsules wires and second layer forms microchannels. Second layer made with sacrificial ink or polymer thread	A "chip in hole" structure on PCB. UV curable polymer seals chips active area and PDMS cap with microchannel. Also bottom half is UV polymer.
		
A large chip with glass bonded on top. Microfluidic channel etched in the glass.	Chip in a cavity with separated microchannel. Upper half for wires and lid. Bottom side via for microchannel.	Another "chip in hole" structure with handle wafer. CMOS chip is molded to polymer and PI/SiO2 works as a passivation layer.
		
Chip wire bonded to PCB substrate. Passivation done with parylene inside a well.	A flip-chip packaged die with PCB forming well.	PDMS top and substrate with liquid metal electrodes.
		
Chip in a cavity made in chip carriers. And two options for passivation layer.	Conceptual LOC structure. Wire connections are buried to leveling layer.	This is packaging method described in [19].

Figure 10. Different approaches to packaging CMOS on LOC. The critical fluid barriers are colored pink and protection for electrical connections green. [19]

2. LOC PACKAGE DESIGN AND MANUFACTURING

The aim of this work is to design and manufacture a package for fully differential capacitance sensor chip (cell clinic) for monitoring cell adhesion and viability. Figure 11 shows the working principle. The cell clinic is used for evaluation of toxic effect of nanoparticles and also other applications are possible.

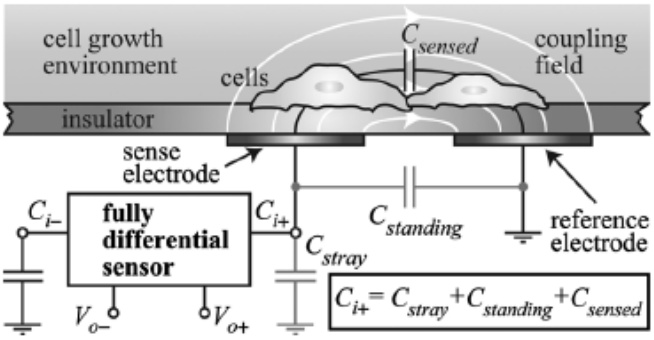


Figure 11. Fully differential capacitance chip, also associated capacitances are shown [20]. [2009] IEEE. Reprinted, with permission, from [Prakash, S.B. ; Abshire, Pamela, Fully Differential Rail-to Rail CMOS Capacitance Sensor With Floating-Gate Trimming for Mismatch Compensation, Circuits and Systems I: Regular Papers, 13 February 2009

The chip (Cell Clinic) is manufactured by using commercial 0.35 µm CMOS process at MOSIS IC foundry. The chip had 40 bond pad configuration without bumping on bond pads. Bumping is used normally with flip chip packaging. The area of the chip was 3x3mm^2 and pad size 80 µm x 80 µm. The package was connected to PC through printed circuit board (PCB) and high speed data acquisition (DAQ) USB card. On the PCB there were two 1.5 V AA batteries as a low-noise power supply and two shunt capacitors to compensate for fluctuating power consumption of the supply. The PC used MATLAB code to collect data and to program the chip. Sampling rates were 10 to 40 kHz. [20]

Figure 10 presents the layout of the chip. Each column has finger electrodes for capacitance sensing, dummy electrodes, and shielded current bus and sensor evaluation module. Amplifiers are inside these modules. The differential sensor was reported to have maximum sensitivity of 200 mV/fF, a resolution of 15 aF, and an output dynamic range of 65dB. [20]

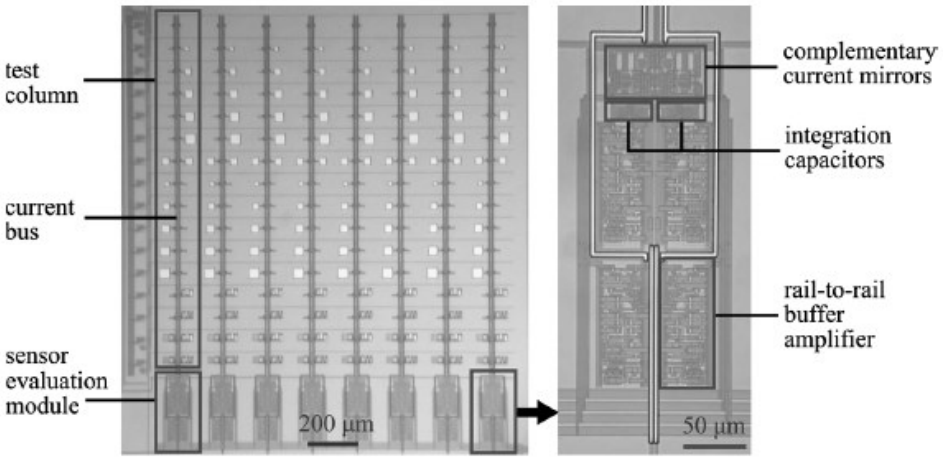


Figure 10. Layout of the chip, from [20]. [2009] IEEE. Reprinted, with permission, from [Prakash, S.B. ; Abshire, Pamela, Fully Differential Rail-to Rail CMOS Capacitance Sensor With Floating-Gate Trimming for Mismatch Compensation, Circuits and Systems I: Regular Papers, 13 February 2009]

The goal of this work is to combine these two technologies (LTCC and LOC) and design and manufacture a robust package for CMOS based lab-on-a-chip 'cell clinic' with the LTCC technology. Traditional packaging methods are inadequate, because CMOS needs dry environment and biology needs wet environment. In this work one solution to the problem of joining wet and dry world is introduced. This package needs to withstand hostile environment and still enable the chip to make measurements on cells. LTCC ceramic material is well suited to this challenge because of the material characteristics and flexibility of LTCC processing technology. Electrical connections are done with conductive silver epoxy. Two types of conductive epoxy have been tested; anisotropic and isotropic.

2.1. Choosing materials

2.1.1. LTCC Tape and Conductor material

LTCC tape material should be selected so that all requirements of the application will be fulfilled. Many companies manufacture these tapes and often these materials come as readily purpose built paste systems (conductor, resistor and dielectric pastes).

In this system Heraeus HeraLock® Tape HL2000 was chosen. System requirements for LTCC package are possibility to print fine line conductors, hydrostatic stability and near zero x-y shrinkage. The fracture strength is < 200 MPa which is very good. Surface roughness is 0.7µm, and this is equivalent to grain size. Roughness is an important property because it affects adhesion of the materials. Moreover this tape does not shrink in x-y directions so designing is easier. Draw backs of this tape are different thermal coefficient of expansion compared to chip material (Si 2.6ppm/°C vs. HL2000 6.1ppm/°C) and z shrinkage is significant. Tape properties are shown in table 2. [21]

Table 2. Properties of LTCC tape. [21]

Tape	Heraeus HeraLock® Tape HL2000
Dielectric Constant @ 2.5 GHz	7.3 ±0.3
Thermal Coefficient of Expansion	6.1 ppm/°C
x-y shrinkage	0.20%±0.04
z shrinkage	32%
Fired layer thickness	225µm
Fracture Strength	>200 MPa
Surface Roughness	0.7 µm

Heraeus Co-Firing Silver Conductor TC0307 paste recommended by the manufacturer was chosen as conductor material. It has low resistivity (≤0.003Ω sheet resistance) and good fine line printing characteristics (≥ 100µm). [22]

2.1.2. Anisotropic conductive adhesive (ACA)

Anisotropic conductive adhesive (ACA) (anisotropic means that conductive particle loading is low and therefore only certain "direction" is conductive) chosen due its suitability for closely spaced (pitch 160µm) contacts and for the need of good hydrolytic stability due the cell growth medium. Moreover the glue needs to be screen printable and chip adhesion also needs to be sufficient. Anisotropic glue consists of conducting silver particles and adhesive polymer resins. These adhesives have conductive particle loading of 5-20%.

Creative Materials Anisotropic 115-29 Conductive epoxy adhesive was chosen for this work. It seems to fulfill all demands of this application. Properties of this glue are shown in table 3. [23]

Table 3. Properties of anisotropic conductive adhesive. [23]

Name	Creative Materials 115-29
Volume resistivity x-y axis	$1x10^{12}$ Ω-cm
Volume resistivity z axis	0.0001 Ω-cm
Temperature range	-55 to +200 °C
Hydrolytic Stability	Excellent
T-Shear Strength (Psi)	1000

2.1.3. Isotropic conductive adhesive (ICA)

Isotropic conductive adhesive (ICA) (isotropic means that conductive particle loading is high and therefore material conducts electricity in all directions) was chosen so that it handles closely spaced (pitch 160 µm and pad size 80 µm x 80 µm) contact pads. Moreover the glue needs to be suitable for "stamping" process. Epoxy Technology EPO-TEK H20E-PFC electrically conductive two component silver epoxy was chosen for this work. This epoxy is designed for flip chip interconnects, the glue consists of conductive silver particles and adhesive polymer resins. It should have all

characteristics to fulfill all demands of this application. Properties of this glue are shown in table 4. [24]

Table 4. Properties of isotropic conductive adhesive. [24]

Name	EPO-TEK H20E-PFC
Volume resistivity	≤ 0.0004 Ω-cm
Viscosity (100 RPM / 23°C)	3000 – 4000 cPs
Temperature range	-55 to +225 °C (max 325 °C)
Particle size	≤ 20 µm
Die Shear	≥ 5 Kg, 1700 psi

2.1.4. Underfill

Epotek 302-3M is a two component capillary action epoxy that was chosen for flip chip underfill application with isotropic conductive adhesive. This adhesive was also used to glue container for cell medium on substrate and cover all electrical connections. This material has low curing temperature and excellent water (can resist 85°C /85% moisture soak), chemical and solvent resistant properties. This adhesive is also bio-compatible. [25]

Table 5. Properties of underfill epoxy. [25]

Name	EPO-TEK 302-3M
Volume resistivity	≥ $1x10^{13}$ Ω-cm
Viscosity (100 RPM / 23°C)	800 – 1600 cPs
Temperature range	-55 to +175 °C (max 250 °C)
Die Shear	≥ 10 Kg, 3400 psi
Medical	USP Class VI bio-compatible
Hydrolytic Stability	Excellent

2.2. Design and manufacturing

Designing of this package started from problems in packaging complementary metal oxide semiconductor (CMOS) chip, ‘the cell clinic’, in an epoxy handle wafer. This packaging concept was presented in paper made in Maryland University. Design of the packaging is shown in figure 11. [19] This is a relatively easy way of packaging tiny chips and it can handle all demands in connection with the Lab-on-a-chip concept. Main problems with this method were bubble formation before curing epoxy and conductor/passivation layer adhesion on the epoxy.

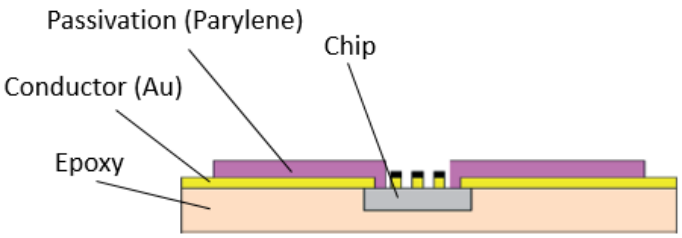


Figure 11. Cross-sectional view of the epoxy package. [19]

Design of alternative package started with sketch shown in figure 12. LTCC is used as substrate and conductors are screen printed on it. Then opening is made with laser for CMOS chip (the sensor chip of the Cell Clinic) so that cells and cell medium can be placed on the active area of the cell clinic (sensor array). The chip is flip chip bonded to LTCC with conductive adhesive (anisotropic and isotropic conductive adhesive are tested). The anisotropic glue has two purposes; provide adhesion and work as conductor between chip pads and printed conductors. Isotropic adhesive needs also underfill to form sufficient adhesion. 40 pin ATA connector is used to provide output to the computer.

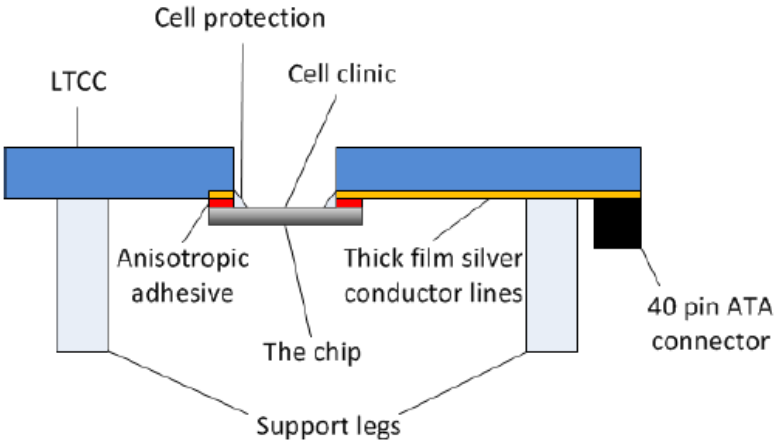


Figure 12. Schematic image of the planned LTCC packaging of the chip.

2.2.1. LTCC design 1

First step was to investigate printing of the conductors on the LTCC green sheets. For this printing screen was made with CAD tool. Conductor layout was designed with AutoCAD 2014 and then it was printed on transparent foil as film mask. Figure 14 shows the layout of the mask. Then in the clean room the screen (interwoven wire mesh with photosensitive emulsion) was exposed to UV-light trough a mask. Next the screen was developed (soaked in water) to make openings in the screen mesh and the screen was ready for printing. With automated screen printing machine conductors were thereafter printed on LTCC green sheets. Then standard LTCC process recommended by manufacturer's datasheet was used [21]. Laminating was done with vertical hydraulic press (T = 75°C, t = 10min, P = 130bar) and three layers of LTCC tape were used. Sintering profile is shown in figure 13. Thickness of the module after sintering was 300 µm. Printed conductors were inspected and five discontinuities were

found. Figure 15 shows photograph of processed prototype LTCC with printed conductors. Notice that opening for chip is not yet made.

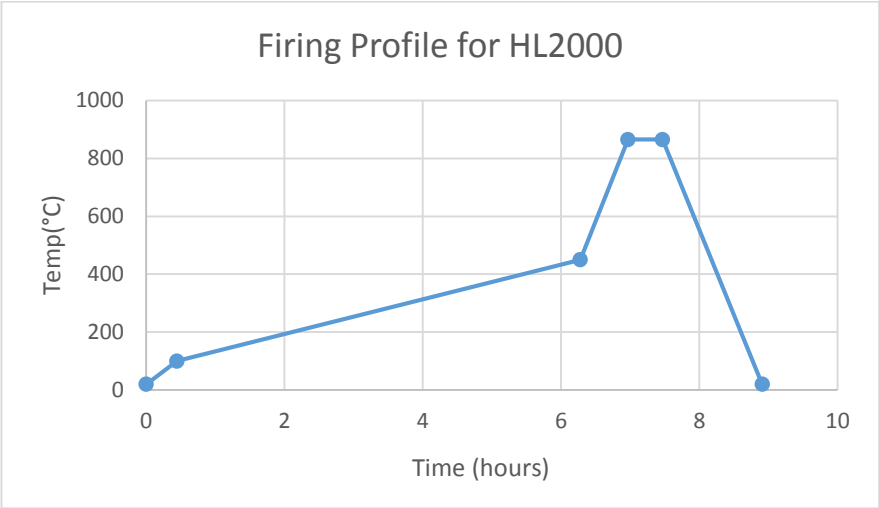


Figure 13. Sintering profile.

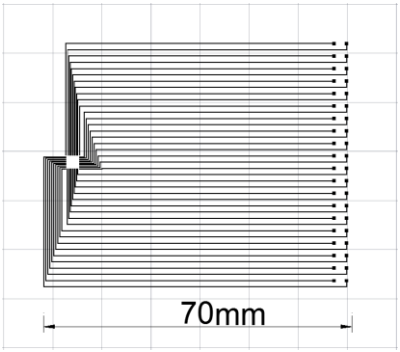


Figure 14. AutoCAD drawn mask layout.

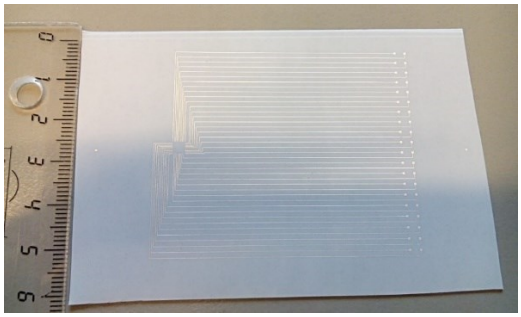


Figure 15. First sintered LTCC prototype with printed conductors

2.2.2. Anisotropically conductive adhesive testing

Anisotropic adhesive Creative Materials 115-29 (ACA) was tested for dummy chip bonding on LTCC substrate. First conductivity of the ACA was confirmed and different forces for curing was investigated. A testing jig and brass test samples were built and then glue was screen printed on copper plated printed circuit board (PCB). ACA was cured in oven as manufacturer recommended (30 – 40 min, 150 °C with pressure applied). Twelve samples were tested with different weights to apply different pressures. Figure 16 shows principle of bonding process and figure 17 photographs of the test setup. All samples were conductive.

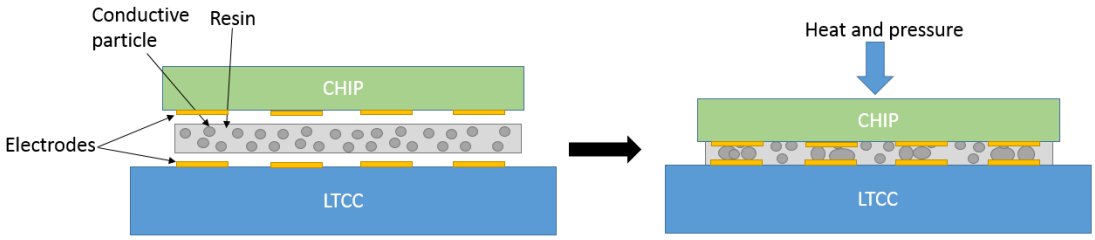


Figure 16. Principle of anisotropic conducting adhesive bonding process

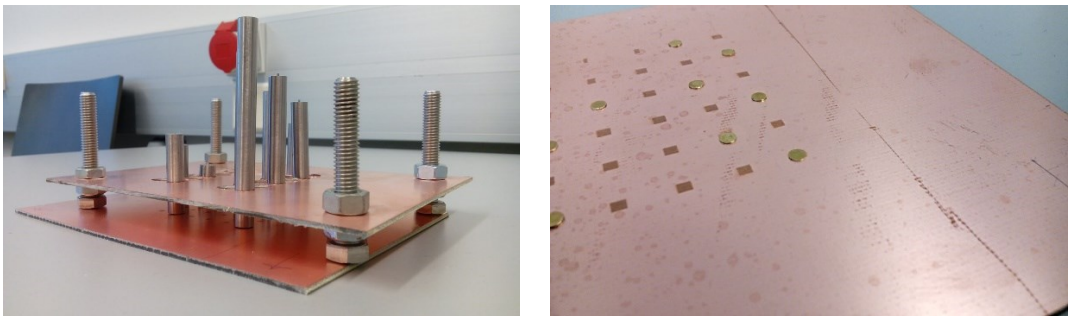


Figure 17. Anisotropic glue test setup, to the left and glued samples on PCB on right hand side.

Next the anisotropic glue was tested with dummy chips made by photolithography. These chips had the same pad size and orientation as the sensor chips for the Cell Clinic, but the total chip size was larger. These chips were flip chip bonded to LTCC substrate, shown in figure 18, with anisotropic glue. The glue was screen printed on LTCC and then flip chip bonding machine (Finetech Electronics Fineplacer Pico 145) was used to align and apply heat and pressure. Flip chip bonding machine had a maximum of 5 min process time, so after that, the samples were placed in the oven to get them fully cured. 2 Nm of force (equals to about 200g weight) and a temperature of ~160°C was applied in the bonding machine for 5 minutes and in the oven 10 minutes at 155°C (total 15min).

Two of these samples were prepared, followed by conductivity testing, and as result, none of the samples were conductive. The reason for this is probably incomplete cure of ACA, when ACA is not fully cured it exhibits insulating property, but the conductivity increases dramatically after sufficient cure.

Again two samples were prepared like earlier but the force of 3 Nm was used with the temperature of ~165°C of the flip chip bonder. Temperature of 170°C, 30min, was applied after that in oven. Also, one sample had weight placed on chip (59.25g) in oven to apply continuous force. Still none of the samples were conductive. Again we presume that ACA was not cured sufficiently. Samples were examined with X-ray and ultrasound, but information with these techniques were not adequate. Figure 18 shows sample with bonded dummy chip and 19 shows the ultrasound image of the sample, implying the that glue is not spread evenly, notice the air trapped under the chip made error in image (bright areas).

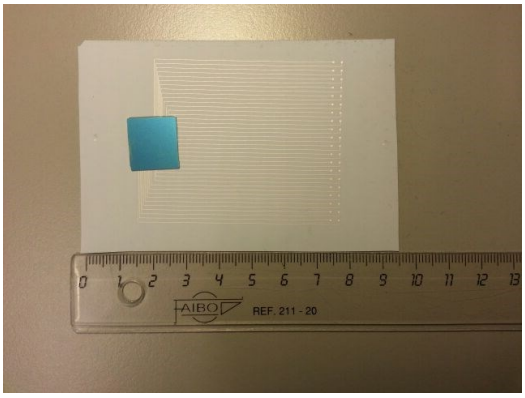


Figure 18. Glued sample

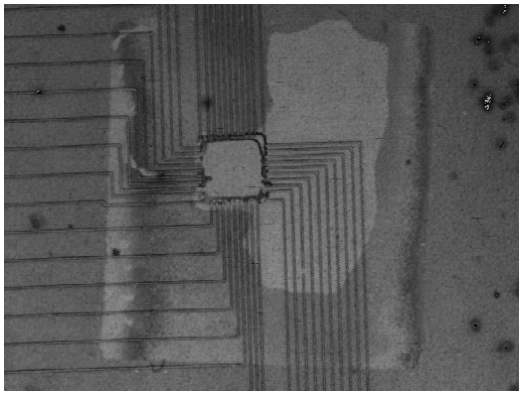


Figure 19. Ultrasound image of the glued sample

2.2.3. LTCC design 2

For the next prototype a smaller masks was made for printing conductors on LTCC to minimize the material consumption and to optimize the manufacturing process. Two prints were made on 88x88 mm laser cut green sheets, also aligning holes for more precise laminating were made. Tape aligning before laminating was made mechanically with four aligning holes. Figure 20 shows the mechanical aligning plate and figure 21 shows principle of mechanical aligning. Again three layers of tape was used. Green sheets were glued together with ethanol after aligning to avoid movement of the tapes during further handling.

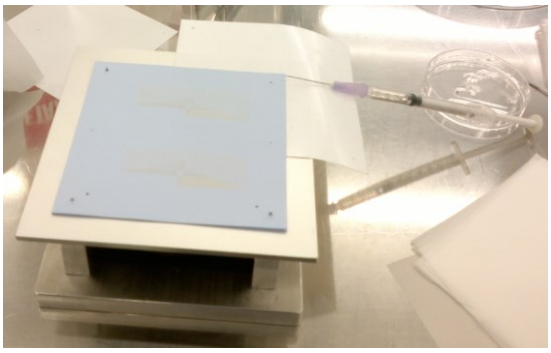


Figure 20. Aligning of the green sheets before laminating, ethanol was injected with syringe to glue green sheets together.

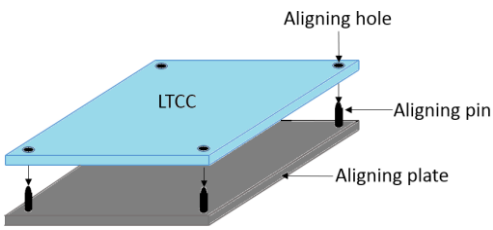


Figure 21. Principle of mechanical aligning.

Laminating was done in isostatic laminating system (PIC PACIFIC TINETICS CORPORATION MODEL 1L-4008), this device applies pressure in water providing stable laminating conditions compared to hydraulic vertical press. Temperature was 70 °C, pressure 1400 psi and process time 10 minutes. Samples were put on vacuum packs before laminating to keep them dry. After lamination the samples were sintered as described earlier.

Next we used laser to cut samples apart and then cut hole for the chip. Improved dummy chips (450nm aluminum deposited on silicon wafer, daisy chain pattern) were manufactured on 4” silicon wafer and scribed by laser. These dummies had the same

size (3x3mm) as the real Cell Clinic chip. Figure 22 and 23 shows ready LTCC prototype and dummy chip.

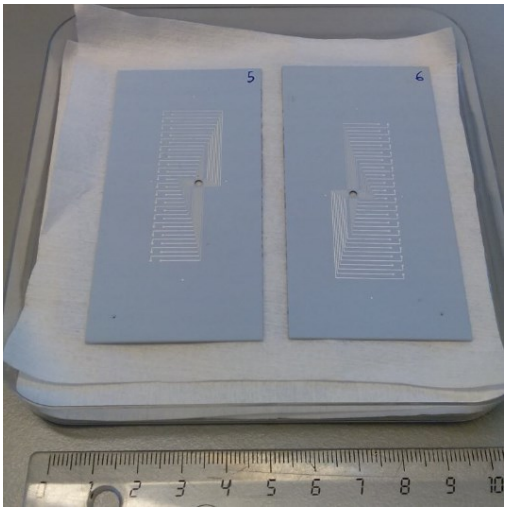


Figure 22. Two LTCC prototypes, laser was used to cut these.

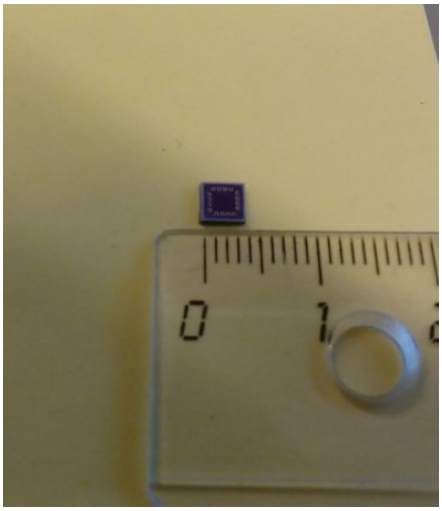


Figure 23. Dummy chip with aluminum daisy chain pattern.

More samples were manufactured with different process parameters and it was noticed that anisotropic glue was not suitable for this application. The number of conductive particles trapped between the bond pad and the silver conductor was not sufficient.

The anisotropic conductive silver epoxy, Creative Materials 115-29, was determined to be unsuitable for this application. This epoxy had too few and big conductive silver particles which resulted in bad electrical connections with small connection pads. Figure 33 and 34 shows particle distribution after the bonding process and after the chip is ripped off. Anisotropic glue would be beneficial because it can be screen printed on the sample with relatively imprecise alignment and underfill is not needed. Tests could preferably be performed with different loading of conductive particles and with bonding pad bumping/modification, but this is out of scope of this work because materials are hard to obtain.

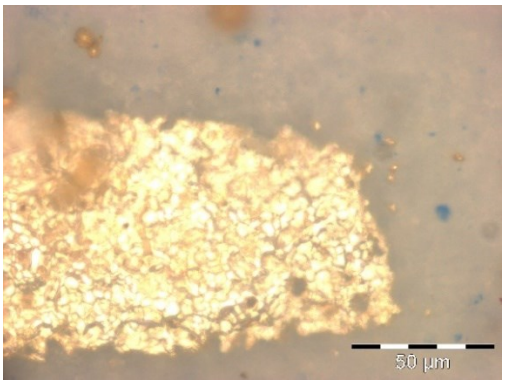


Figure 33. Conductor on LTCC without any conductive particles

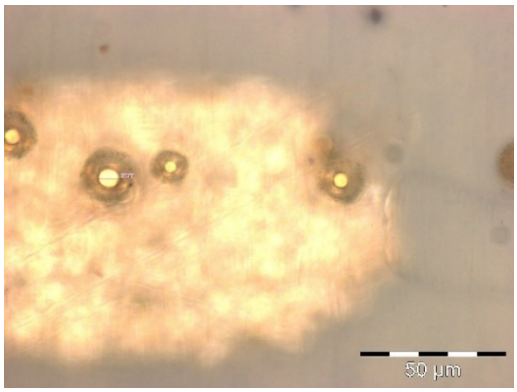


Figure 34. Conductor with some conductive particles, the probability to have particles on all pads is near zero.

2.2.4. Electrical connections using ICA

Anisotropic glue was changed to isotropic adhesive EPO-TEK H20E-PFC (ICA). The process is the same but applying glue precisely onto bond pads is crucial to get good electrical connection. Otherwise electrical shortcuts or open circuit between pads are common. Silver epoxy was applied to the substrate by stamping technique. To get better adhesion and cover conductive epoxy from environment (moisture etc.,) underfill is needed. Figure 24 shows conductive epoxy process and the underfilling step.

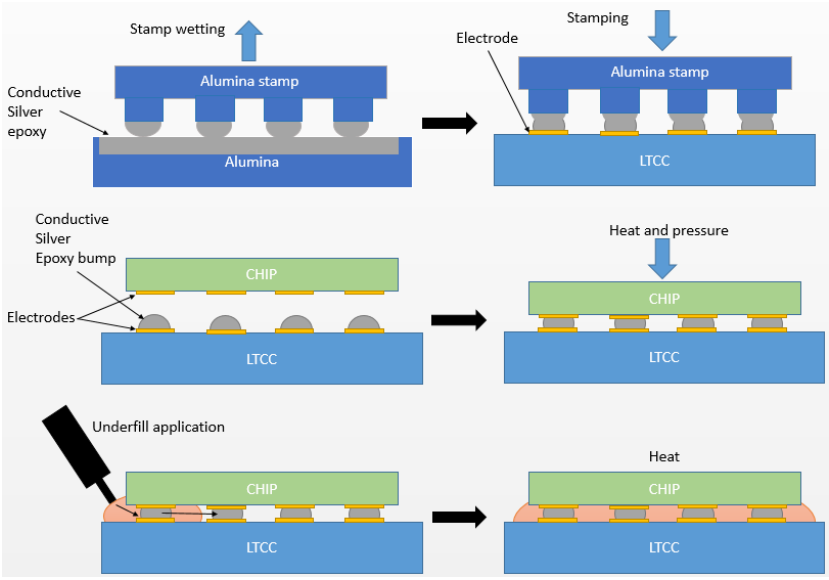


Figure 24. Flip chip process: stamping with conductive epoxy and underfill application.

Stamp was manufactured from alumina (Al_3O_2) by laser patterning to form the desired structure. Different types of stamps were manufactured and tested.

To get even layer of adhesive on stamp silver epoxy was spread on an alumina plate with a cavity to make uniform layer of epoxy. Then this epoxy was picked up with the alumina stamp, and aligning was made with Finetech flip chip bonder, see figure 24. ICA was stamped on LTCC substrate and then FC bonder was used to align and bond the dummy chip. Also curing (175°C for 5 minutes) was done in the same process step.

The underfill (EPO-TEK 302-3M) was applied with needle tip and capillary action made the underfill to fill the space between chip and LTCC. The active area on the chip stayed clear because of the capillary phenomenon. The underfill was cured on a hot plate.

The best stamp had 80x120µm contours aligned to hit connection pads. Figure 25 shows photograph taken with microscope of the used stamp. Problem here was the size of the ICA bump, if it is too big shortcuts will appear and if the bump is too small epoxy won't cure properly. Also the adhesion needs to be strong enough to withstand further handling. Good ICA bump diameter was 100 µm. Moreover FC bonding machine needs to be aligned correctly. Figure 26 shows failed stamping process and also good stamping print, microscope pictures has been taken after curing the ICA and removal of the chip.

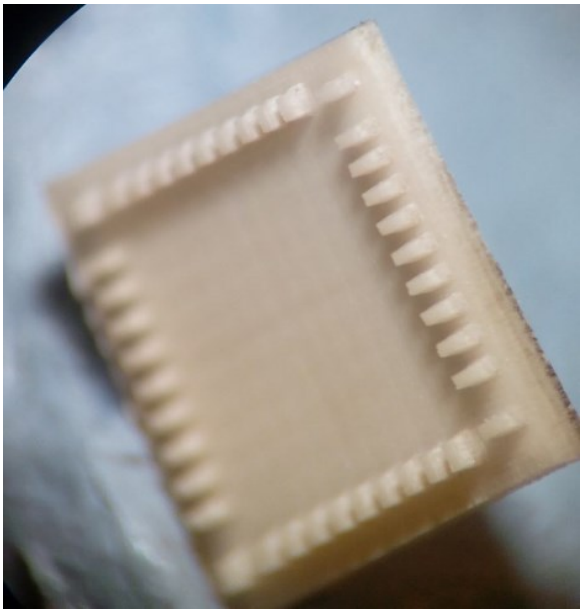


Figure 25. 3 x 3 mm alumina stamp with 80 x 120 x 50 µm contours.

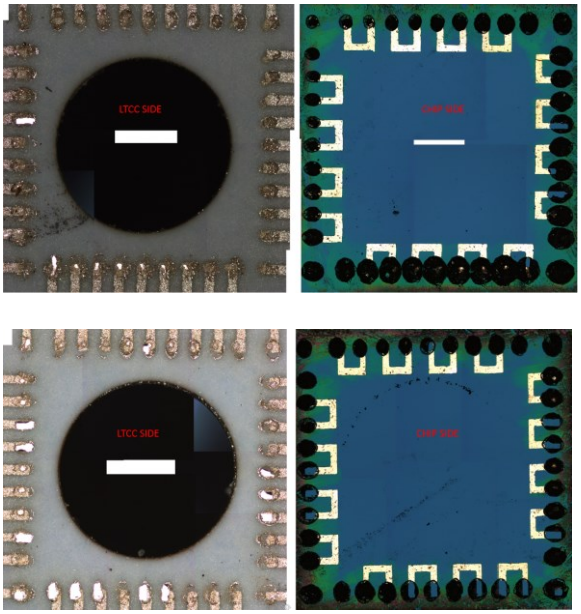


Figure 26. **Top**: ICA bumps too small at top corner and too big at lower part (electrical shorts), due to alignment error.
Down: Good stamping print.

2.2.5. Gold patterned dummy chips

More samples with dummy chips were made but silver epoxy did not work sufficiently with aluminum pads of the dummy chips because aluminum oxidizes readily. This causes unreliable contact resistances and also weakens physical adhesion between the chip and printed silver conductors. For this reason dummies with gold conductors were manufactured by photolithography process and contact resistance descended to one tenth (10Ω → 1Ω). Figure 26 shows scribed wafer and diced dummy chips.

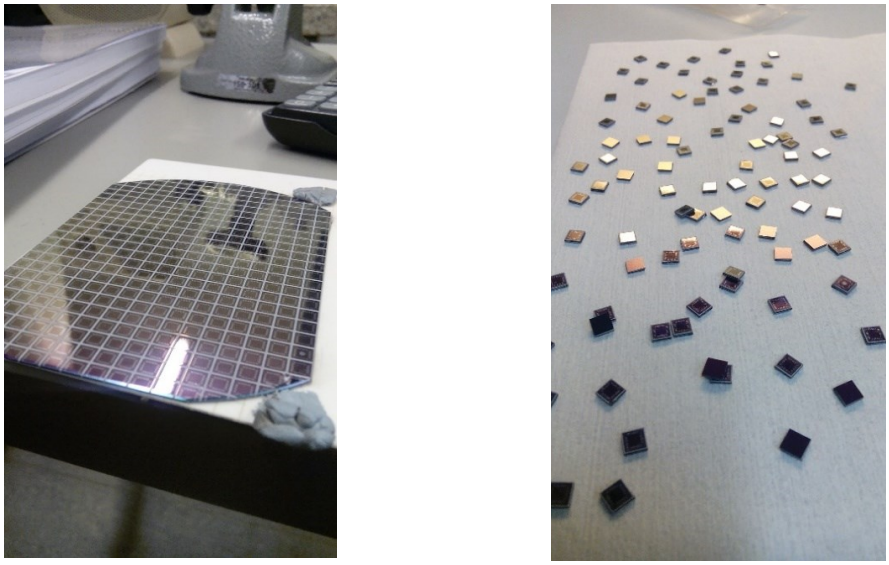


Figure 26. **Left**: Laser scribed wafer and **right**: separated dummy chips with gold pattern.

2.2.6. LTCC design 3.

After successful flip chip bonding of the gold patterned dummy chip the connector pins were glued on LTCC with instant glue and then silver conductive paint (Elctrolube) was used to make electrical connections. Then silver paint was sealed with epoxy. But this was not a good solution because the brittle LTCC substrate cracked when female connector was pressed down. The solution to this problem was replacing the connector pins with zero insertion force connector (ZIF).

ZIF connector had different pin pattern so new LTCC layout was designed with AutoCAD. This also enables to make four devices instead of two devices on one 88x88mm substrate. Thickness was increased from three layers to four and top layer was used to cover conductive lines, thickness is 300µm and 400µm respectively.

Conductive silver epoxy was used, instead of silver paint, to make electrical connections to pins and everything was sealed with underfill. Figure 27 shows the top side and the bottom side of the device.

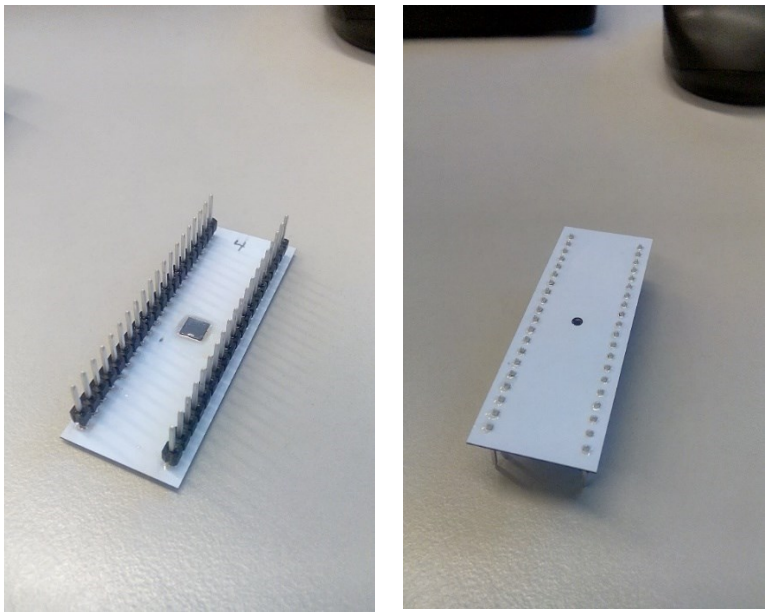


Figure 27. **Left**: bottom side of the device **Right**: top side of the device. Package size is 55 x 20 x 11 mm.

Last stage was to glue cell well with underfill epoxy on top of the device to hold the cell growth medium. The cell well was made of capped tube by cutting it down. Figure 28 shows ready package with cell well and ZIF connector. Figure 29 presents microscope pictures of the cross section of the sample cut from the far end of the hole, note that all electrical connections are buried in underfill. This sample had some alignment tuning errors with FC bonder and some misalignment can be seen. This was fixed on later samples.

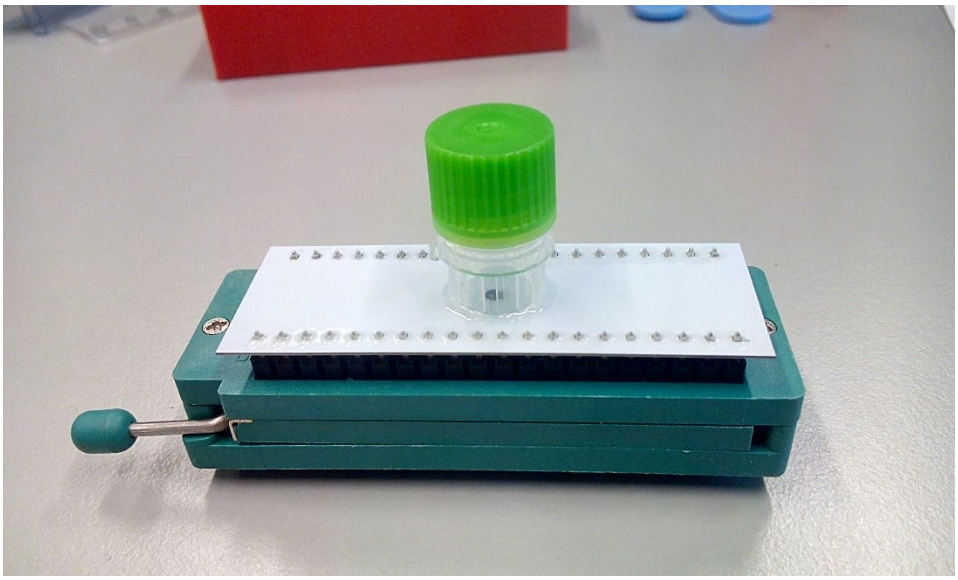


Figure 28. Device attached to ZIF connector with cell well glued on top.

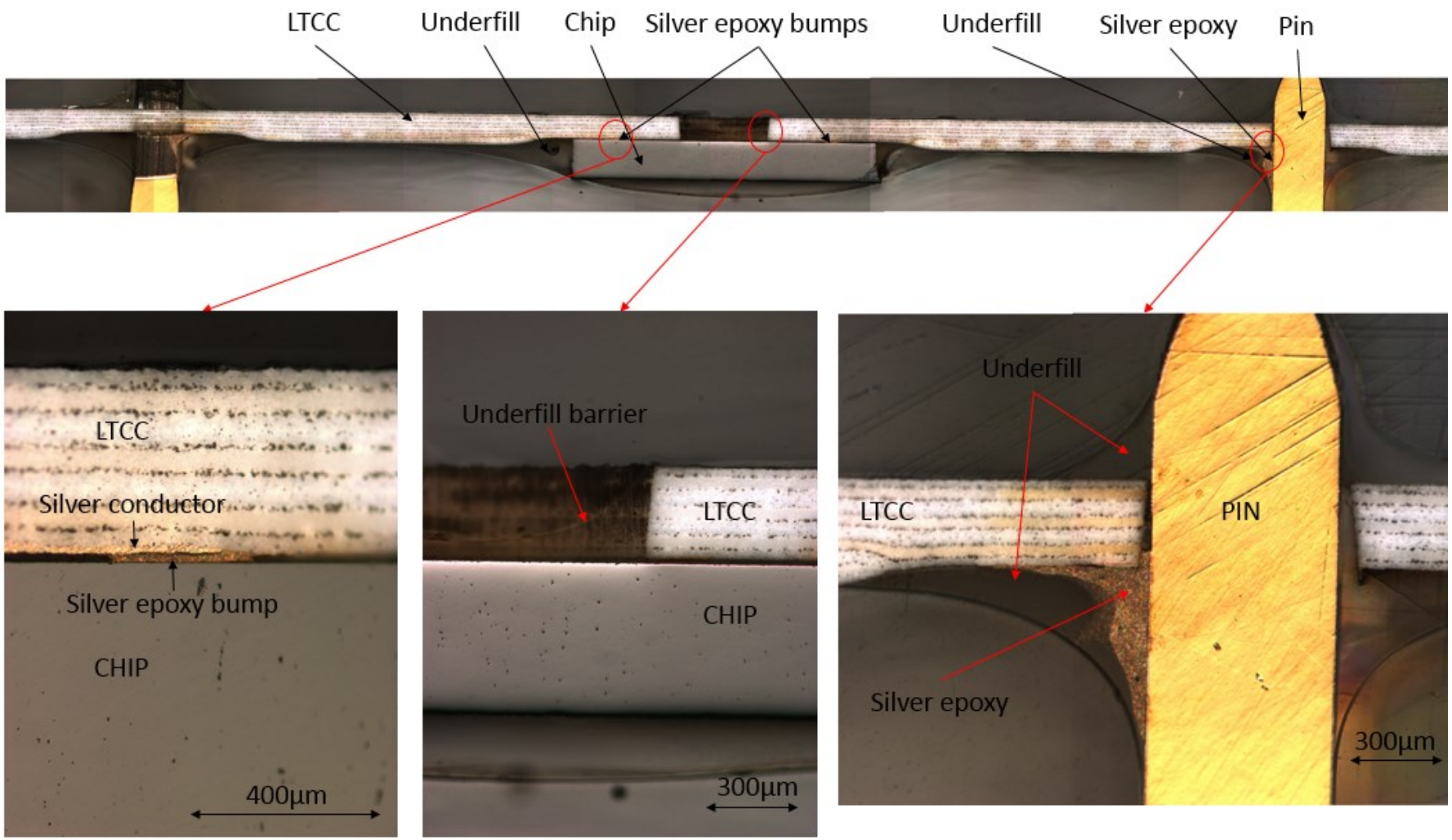


Figure 29. Side view of the package taken with microscope, gap between the chip and LTCC is 20 µm (alignment error can be seen as the right side of the chip has bigger gap).

3. TESTING

3.1. Resistance measurement

Testing the performance and the reliability of the package was done by measuring DC resistance over dummy chip under different conditions. DC resistance measurement was used because it tells when the package fails and therefore the device is not working properly anymore. Also, it is relatively simple measurement. The testing conditions were the same as the Cell Clinc would encounter. Also testing between process steps were performed. Figure 30 shows the dummy chip pattern, this pattern is referred to as daisy chain. The resistance through these loops can be measured.

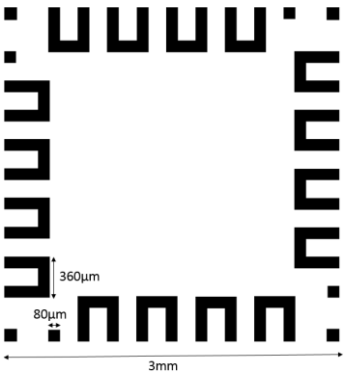


Figure 30. Dummy chip layout “daisy chain”.

First measurement was done with after curing the conductive silver adhesive to ensure that electrical connection through all loops is established, then after applying and curing the underfill, and finally, after the connector has been attached to the device.

A testing PCB, for fast measurement of the resistance, was manufactured. This way the overall resistance through all loops can be measured simultaneously, this is also referred to as the two point method. Otherwise every loop needs to be measured one by one. If resistance changes over 20% in the test, it is considered as packaging failure.

A holder for PCB was also manufactured with the 3D printer from ABS plastic. Figure 31 shows the device connected to PCB with ABS holder.

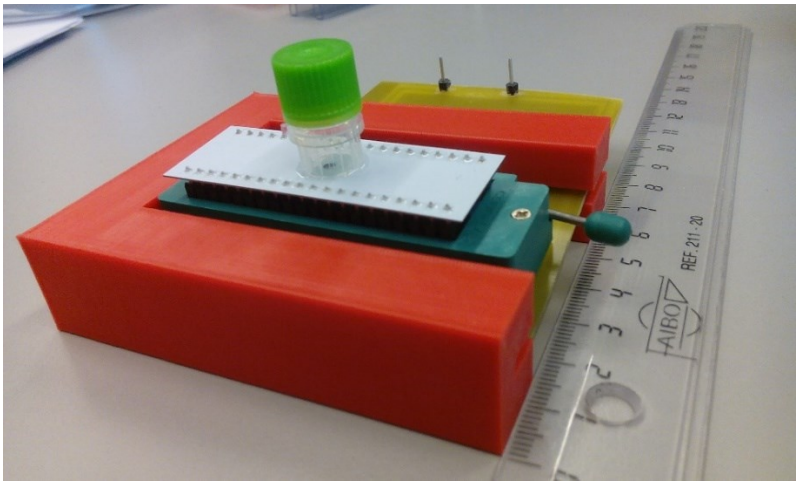


Figure 31. Package ready for testing, two testing pins to the side of the device.

3.2. Testing conditions

Cell Clinic measurement conditions were used, incubator at 37 °C, 85 % humidity and 5 % CO_2. Cell growth medium was injected into the cell well and cells were grown on the chip. Then resistance was measured with multi-meter (Amprobe 5XP-A) for several days. If the package would have failed the resistance should have risen considerably.

In preliminary testing one package was first immersed in tap water for one day and after that one week in cell growth medium at 20°C during which the overall resistance stayed constant. Also biocompatibility of the used materials was confirmed before testing. BEAS2B cells were successfully grown on the surface of the package. Figure 32 shows that cells adhered and grew on chip as expected.

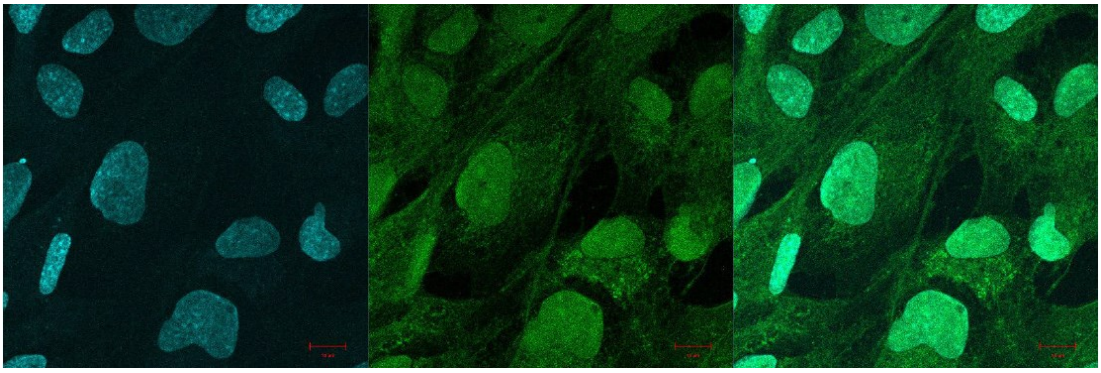


Figure 32. BEAS2B cells on packaged dummy chip, size of the cells are 10 – 30 µm.

4. RESULTS

Two samples were tested in cell growing conditions (incubator with 37 °C, 85 % humidity and 5 % CO_2) and both had similar design. Two-point DC resistance measurement was used and the package was considered to fail if resistance changes over 20%.

Both samples survived from typical cell growing conditions, resistance measurements are presented on figures 35 and 36. There was some resistance change when the samples were placed in the incubator. This happens because the temperature increases from room temperature 21°C to 37°C. The electrical resistance increases when temperature rises, and also when cell medium is added, and furthermore when cells are added. This increase in resistance happens because the package is taken out of the incubator during the cell adding procedure. Moreover multi-meter (Amprobe 5XP-A) is not precise when measuring low resistances. The maximum resistance change is 1.8 Ω and the overall change is 7.2%, which is below 20% that was considered package failure.

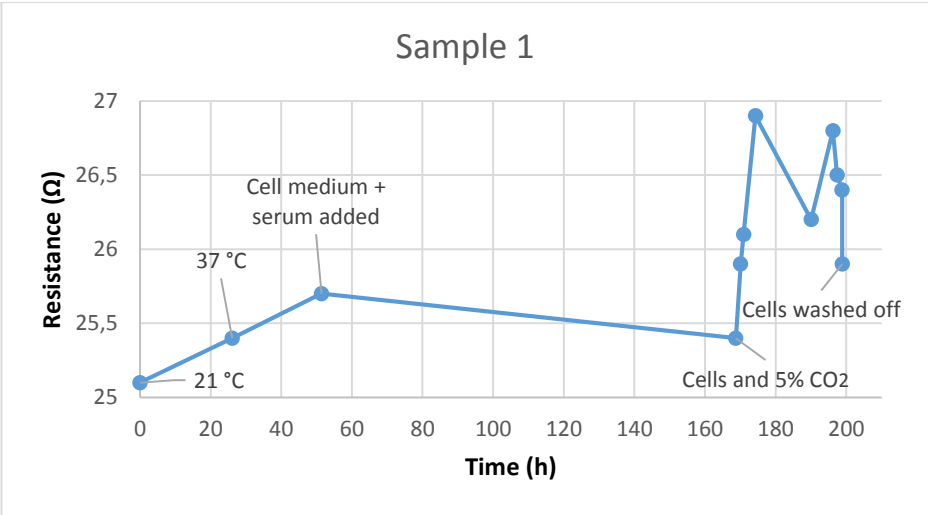


Figure 35. Sample 1 DC resistance measurement.

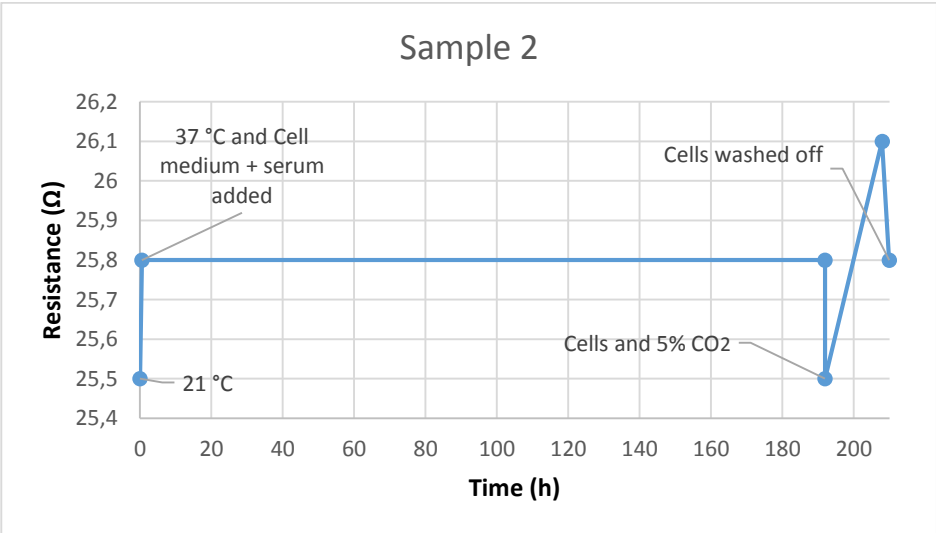


Figure 36. Sample 2 DC resistance measurement, notice less data points.

5. CONCLUSION

In this work packaging method for lab-on-a-chip was presented, manufactured and the functionality was demonstrated. Developing new packaging methods for LOC applications are crucial in order for these devices to work properly and reach their full potential. In this work LTCC substrate was used with conductive/noncoductive epoxies for insulating and electrical contacts. Using epoxies also makes it possible to utilize other substrate materials such as plastic and glass, and furthermore, everything can be cured at a maximum temperature of 90°C. Moreover, a stamping process allows depositing ICA in cavities which is impossible with the screen printing process. Also biocompability of the used packaging was confirmed.

Limitation of this package is that it has many process steps, all thought they are quite simple. Furthermore, the stamping method requires careful calibration of the equipment for success. Also, the stamped fine pitch ICA dots are really small and mechanically fragile before applying the underfill epoxy.

Advantages include package robustness against harsh conditions when growing cells and that this packaging method can be easily modified for other lab on a chip applications.

Further work involves packaging of the real Cell Clinic sensor chip using the presented method and performing measurements with living cells. Moreover, migration of metals in the conducting leads will be studied, since this might cause short circuits between conductors when the chip is under load (influenced by electric fields). BGA module version of the package will also be investigated. Also microfluidic channels will be built from LTCC or PDMS (PDMS is under testing, figure 37 presents the design) on top of the device and maybe an integrated micro incubator around the device. Then Cell Clinic would be a really handheld device, which can be used in the field, for example for harmful mold spore detection in households. Also, other harmful toxins can be detected using different types of cells, since some cells are more sensitive to toxins. Figure 38 shows an artistic view of the Cell Clinic in a mini incubator.

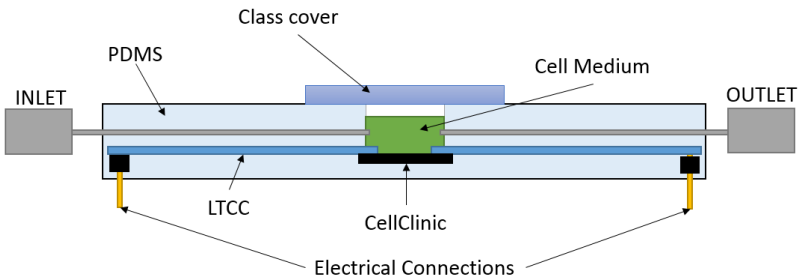


Figure 37. Package inside PDMS with integrated fluidic channels.

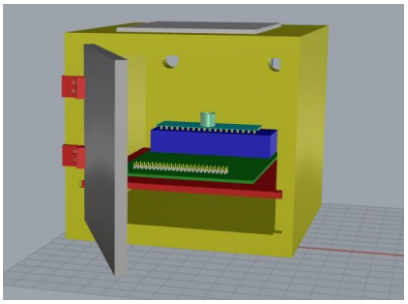


Figure 38. Cell Clinic in mini incubator made by the 3D printer, size of incubator is 12 x 12 x 11 cm.

6. REFRENCES

[1] Multilayer low-temperature co-fired ceramic systems incorporating a thick film printing process, M. Soboncinski, J. Putaala and H. Jantunen, 2012

[2] Lab-on-a-chip: Techniques, Circuits, and Biomedical applications (2010) In artecg House Integrated Microsystems Series. Norwood, Mass: Artech House. Ghallab, Yehya H. Badawy, Wael

[3] Multilayered Low Temperature Cofired Ceramics (LTCC) technology, Yoshiko Imanaka, 2005

[4] Overview of low temperature co-fired ceramics tape technology for meso-system technology (MsST) Authors of Document Gongora-Rubio, M.R., Espinoza-Vallejos, P., Sola-Laguna, L., Santiago-Avilés, J.J. Source of the Document Sensors and Actuators, A: Physical 2001

[5] Vortex configuration flow cell based on low-temperature cofired ceramics as a compact chemiluminescence microsystem. Ibanez Garcia, Analytical chemistry N yr: 2008 vol: 80 iss: 14 pg: 5320 -5324

[6] Novel Microsystem Applications with New Techniques in Low-Temperature Co-Fired Ceramics K. A. Peterson,* K. D. Patel, C. K. Ho, S. B. Rohde, C. D. Nordquist, C. A. Walker, B. D. Wroblewski, and M. Okandan

[7] Micro Ceramic Cell Analyzer (MCCA) - Preliminary results, Karol Malecha, Mateusz Czok , Anna Hetnar , Anna Pawlik , Helena Sztajer , Leszek J. Golonka (2011)]

[8] Microfluidics Meets MEMS. (2003) Proceedings of the IEEE vol. 91, no.6 June. Elisabeth Verpoorte and nico F. De Rooij 23 pages.

[9] Fu, A. Y., et al., “A Microfabricated Fluorescence-Activated Cell Sorter,” Journal of Nature Biotechnology, Vol. 17, 1999, pp. 1109–1111.

[10] Microfluidic impedance cytometer for characterization of subcellular morphology of single cells (2013), IEE, Haandbak, N. ; Burgel, S.C. ; Rudolf, F. ; Heer, F. ; Hierlemann, A.

[11] Microchip systems for immunoassay: An integrated immunoreactor with electrophoretic separation for serum theophylline determination (1998) Chiem, N.H., Harrison, D.J. Clinical Chemistry Volume 44, Issue 3, 1998, Pages 591-598

[12] A 3-D microelectrode system for handling and caging single cells and particles (1999). Müller, T., Gradl, G., Howitz, S., Shirley, S., Schnelle, Th., Fuhr, G. Biosensors and Bioelectronics, Volume 14, Issue 3, 15 March 1999, Pages 247-256

[13] A CMOS Chip for Individual Cell Manipulation and Detection (2003) Manaresi, N., Romani. A., Medoro, G., Altomare, L., Leonardi, A., Tartagni, M., Guerrieri, R. ,IEEE Journal of Solid-State Circuits Volume 38, Issue 12, December 2003, Pages 2297-2305

[14] Cell-lab on a chip: A CMOS-based microsystem for culturing and monitoring cells (2004) (Conference Paper) Liu, Y., Smela, E., Nelson, N.M., Abshire, P. Annual International Conference of the IEEE Engineering in Medicine and Biology - Proceedings Volume 26 IV, 2004, Pages 2534-2537

[15] A lab-on-a-chip for spectrophotometric analysis of biological fluids, (Article, 2005) Minas, G. , Wolffenbuttel, R.F. , Correia, J.H. Lab on a Chip - Miniaturisation for Chemistry and Biology Volume 5, Issue 11, November 2005, Pages 1303-1309

[16] Micro/nanofluidic device for single-cell-based assay, (2005) Yun, K.-S. , Yoon,E. Biomedical Microdevices, Volume 7, Issue 1, March 2005, Pages 35-40

[17] Microfabricated bioprocessor for integrated nanoliter-scale Sanger DNA sequencing (Article,2006)Blazej, R.G., Kumaresan, P., Mathies, R.A. Proceedings of the National Academy of Sciences of the United States of America Volume 103, Issue 19, 9 May 2006, Pages 7240-7245

[18] Chin, C. D. et al. Microfluidics-based diagnostics of infectious diseases in the developing world. Nature Med. 17, 1015–1019 (2011).

[19] Packaging commercial CMOS chips for lab on a chip integration, Timir, Pamela and Elisabeth (2014)

[20] Fully Differential Rail-to Rail CMOS Capacitance Sensor With Floating-Gate Trimming for Mismatch Compensation, Somashekar Bangalore Prakash, Pamela Abshire (2009)

[21] Heraeus HeraLock® Tape HL2000

[22] Heraeus Co-Firing Silver Conductor TC0307

[23] Creative Materials Anisotropic 115-29 Conductive epoxy adhesive

[24] Epoxy Technology EPO-TEK H20E-PFC

[25] Epotek 302-3M