Final Project Report

Project Title: University Crystalline Silicon Photovoltaics Research and Development

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Contacts: Ajeet Rohatgi
Phone: 404-894-9886
Fax: 404-894-5934
Email: ajeet.rohatgi@ece.gatech.edu

Serelia Woods
Phone: 404 894 5945
Fax: 404.894.7002
Email: serelia.woods@osp.gatech.edu

DOE Project Team:

DOE Field Contracting Officer - Beth Dwyer
DOE Field Project Officer - Glenn Doyle
Project Engineer - Pat Saito

Project Objective: The overall goal of the program is to advance the current state of crystalline silicon solar cell technology to make photovoltaics more competitive with conventional energy sources. This program emphasizes fundamental and applied research that results in low-cost, high-efficiency cells on commercial silicon substrates with strong involvement of the PV industry, and support a very strong photovoltaics education program in the US based on classroom education and hands-on training in the laboratory.

Background: The major technical issue addressed by this project is reduction of the PV module manufacturing cost through the development of high-efficiency cells on low-cost c-Si wafers. Currently, about 95% of PV modules use c-Si cells and have a cost of $3-4/W. According to projections in the MYPP, the module price should reach $1.25/W by 2020 resulting in an installed PV system cost of $3.30/W in order to achieve an LCOE of 9¢/kWh. Our calculations show that an LCOE of 8.3¢/kWh can be achieved if the direct manufacturing cost can be reduced to as low as 66 ¢/W by reducing the cell thickness from 250 μm to 100 μm, the polysilicon feedstock cost from $50/kg to $25/kg, increasing cell efficiency from 14.5% to 20%, and increasing the production capacity of the line to ≥500 MW.

We have performed extensive device modeling to show that 20%-efficient cells on 100 μm thick wafers can be achieved by improving the current screen-printed contact technology to achieve high fill factors (≥0.78) on ~100 Ω/sq emitters while reducing the finger line width to lower the shading loss to ≤6%. We also need to improve defect gettering and passivation to achieve a bulk minority carrier lifetime ≥100 μs in low-cost materials. The next major advancement involves the development of rear contacts that can reduce the back surface recombination velocity (BSRV) to 100 cm/s and increase the back surface reflectance (BSR) to 95%. This development will allow a reduction of

cell thickness to 100 μm without any loss in cell efficiency. Finally, surface texturing can drive the efficiency to 20%.

Status:

Task 1: Development of Low-cost and High-performance Screen-printed Metallization for Silicon Solar Cells

Screen-printed contacts to high sheet resistance emitters

Significant progress has been achieved in this task by improving the performance of screen-printed contacts. One of the most difficult and challenging tasks in achieving high-efficiency screen-printed cells is to form high quality contacts to high sheet resistance emitters. The junction depth of high sheet resistance emitters is usually shallow, <0.3 μm and therefore, front silver paste and firing should not etch more than 0.1 μm of the silicon surface to protect the junction. However, majority of the commercial front silver pastes available today cannot form good ohmic contacts to high sheet resistance emitters without shunting the p-n junction or producing high ideality factor. Most commercial pastes contain about 3-5% (by weight) glass frit. The Heraeus paste SOL9807A, used as a reference in this study, also contained ~ 3-5% glass frit. Although this paste gave good fill factor on 45-Ω/sq emitters it was inferior when used on 65-Ω/sq emitters. The cell analysis showed the low fill factor in the cells fabricated with paste SOL9807A on high sheet resistance emitters were dominated by high series resistance. This was attributed to the high total glass content in the paste which could lead to a thick glass layer. Therefore we reduced the total glass content in the paste by varying only the PbO component, since PbO is the key ingredient in the glass frit. Three new silver pastes, A-C, were formulated with varying amount of PbO in the range of 20-50% by weight. Cells fabricated with pastes A to C, respectively, produced average fill factor of 0.770, 0.769, and 0.767, at the peak firing temperature. Average efficiency of 17.2% was achieved with paste A, which had the highest amount of glass frit. We measured contact resistance values of 10.5-mΩ-cm2, 14.1-mΩ-cm2 and 14.2-mΩ-cm2, respectively, for paste A, B and C. The contact resistance value was about three times higher than the theoretical value for achieving fill factors ≥0.790. The remarkable feature for all these pastes is the narrow finger widths. The grid width ranged from 106-113-mm for

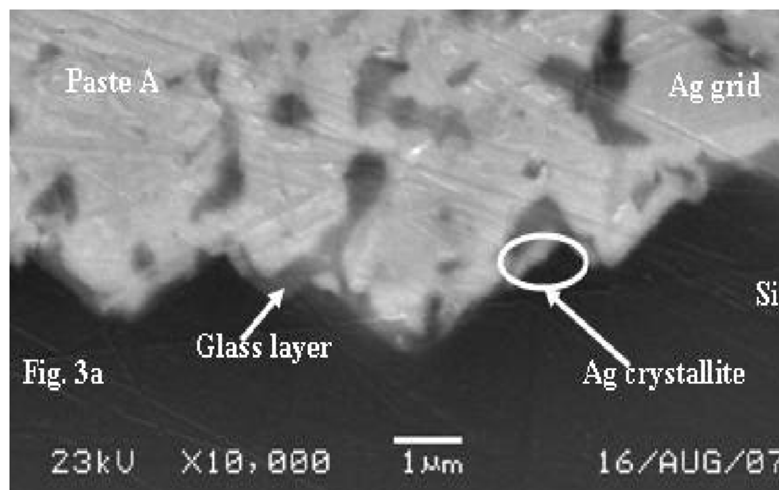


Fig. 1: SEM cross-section of the Ag grid for paste A fired at a peak temperature of 775°C showing the presence of thin glass layer and small Ag crvstallites at the contact interface.

the three pastes after the contact co-firing. However, the finger height was only 12-μm, possibly due to poor printing. The SEM micrograph in Fig. 1 shows the contact interface for paste A with thin glass layer and small Ag crystallites. From this micrograph and top-view micrographs, we conclude that the Ag crystallite density and distribution should be sufficient to give low contact resistance. However, since we do not know the size and penetration depth of the Ag crystallites and the peak phosphorus concentration at the points of contact, we could not estimate the theoretical contact resistance for comparison.

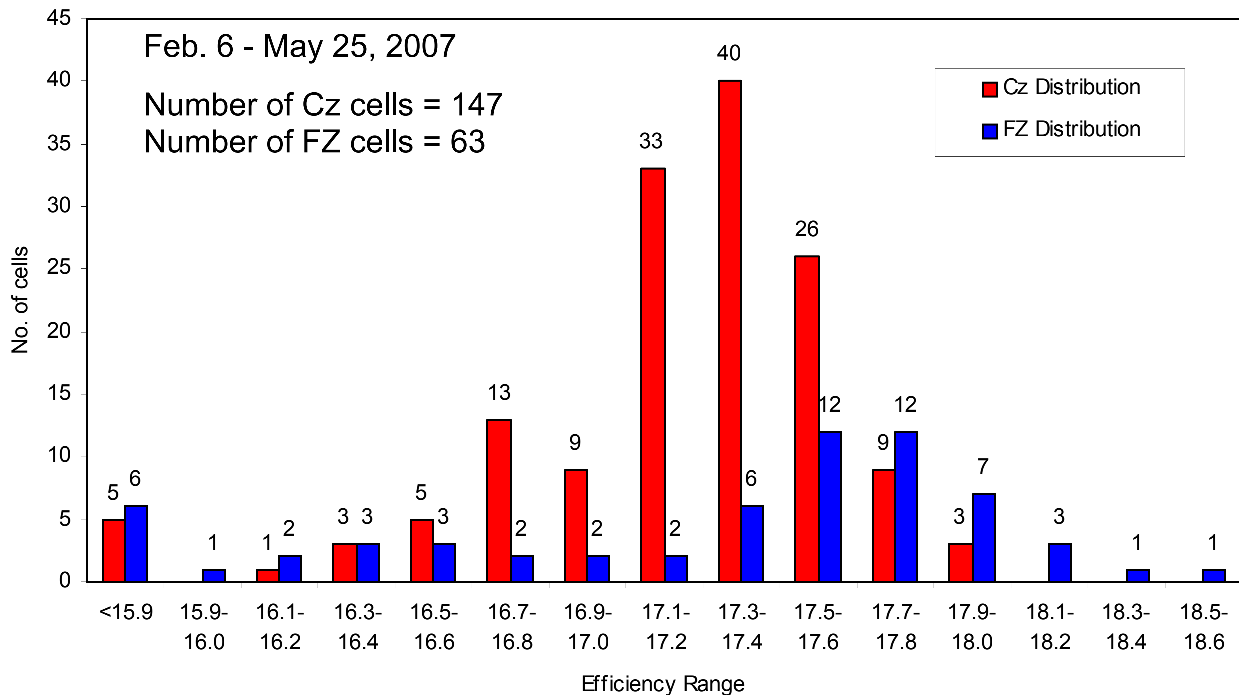


Fig. 2: Efficiency distribution of 149 cm^2 commercial–ready monocrystalline solar cells produced at Georgia Tech.

Through this work, Georgia Tech has achieved commercial-ready 17.8%-efficient B-doped Cz Si cells by developing and optimizing a process to make high-quality screen-printed contacts to high-sheet-resistance emitters. Fig. 2 shows the solar cell efficiency distribution for these cells made on B-doped Cz and FZ Si.

Large area EFG (100-cm^2) ribbon silicon solar cells with screen-printed contacts

Screen-printing is a simple, rapid, and cost-effective technique for forming contacts for solar cells. The method of forming the emitter controls the bulk minority carrier lifetime of the cell, the ease of forming the screen-printed contacts and the quality of the p-n junction after contact co-firing. Emitter formation typically involves phosphorus spray or spin-on followed by drive-in in the IR belt furnace or diffusion from a liquid source ($POCl_3$) in a conventional tube furnace. $POCl_3$ emitters with high sheet resistance and screen-printed contacts have produced cells with efficiencies >16% on 4-cm^2 EFG

ribbon silicon [1]. The major feature of these cells was the processed minority carrier lifetime of 100 µs, because of SiNx induced hydrogen passivation of bulk defects. In another study, we achieved efficiency of 15.5% 4-cm^2 screen-printed EFG ribbon silicon solar cell [2] by using low sheet resistance emitter (~45-Ω/sq) formed by $POCl_3$ and a processed minority carrier lifetime of 80 µs. However, efficiencies of only 15.1% and 14.1% were obtained, respectively, for 4-cm^2 screen-printed EFG Si cells with emitters formed by IR belt diffusion. In this study we investigate large area (100-cm^2) EFG ribbon silicon solar cells with screen-printed contacts using emitters formed by $POCl_3$ and IR belt diffusion. To eliminate the use of forming gas after the co-firing, we investigated a front silver paste (CL80-8729 from Heraeus Inc.) that could produce high fill factor, low ideality factor, low junction leakage current and acceptable fill factor.

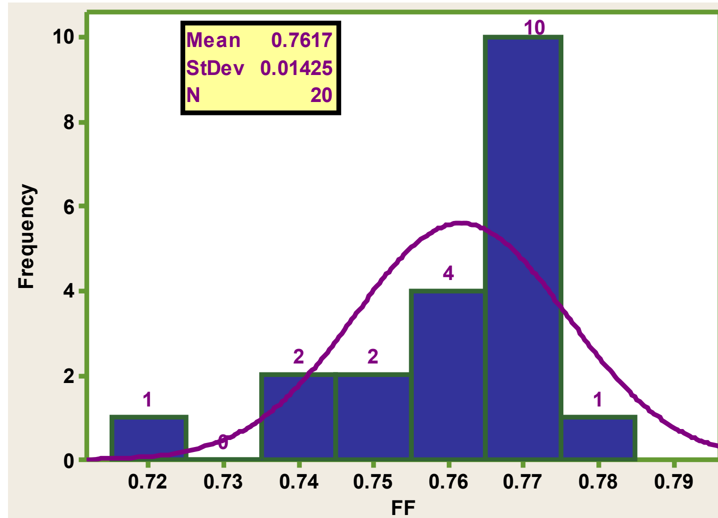


Fig. 3: Fill factor distribution for 20 EFG ribbon silicon cells using CL80-8729 front silver paste from Heraeus Inc and emitters by SCHOTT Solar Inc.

To optimize the metal co-firing for EFG Si cells, we weighed each wafer after all the metal contacts were screen-printed. We used the middle of the range group of wafers to optimize the peak firing temperature. We then used this optimized value to co-fire twenty wafers of various weights between 5.9 – 8.9 g. Fig. 3 shows a mean fill factor of 0.762 and a standard deviation of only 0.014 for twenty EFG Si solar cells. The fill factor varied from 0.72 to 0.78 because of the varying weight. Variation in the silicon nitride thickness might also have contributed to the fill factor variation. Note: the mean value of the short circuit current density was 30.6 mA/cm^2 and maximum of 31.5-mA/cm^2.

Task 2: Gettering and Passivation of Defects in Low-Cost c-Si Materials

Carrier lifetime enhancement during solar cell processing

We have found that hydrogen passivation of defects during cell processing is very effective is low-cost silicon materials such as cast mc-Si and ribbon Si. In order to assess the effectiveness of SiN_x-induced defect hydrogenation on average lifetime enhancement, the carrier lifetime studies have been performed using the quasi-steady-state photoconductance (QSSPC) technique. In this study we obtained ribbon silicon wafers grown from low-cost Si feedstocks by our industry partners. The results of this lifetime study are shown in Fig. 4. The average carrier lifetime was measured by sampling several locations of each wafer at an injection level of 1.0×10^{15} cm^{-3} on as-grown, P diffused, and fully processed wafers. The results show that gettering passivation incorporated into our solar cell process were able to increase the carrier lifetime in standard ribbon wafers from 2 μs to 98 μs, which is very close the target in M2.1 (100 μs). The gettering and passivation treatments also improved the lifetime in wafers from low-cost feedstock sources A and D, but the lifetime in these wafers is still less than 100 μs. We are also developing a model I that incorporates factors such as the area fraction of defective regions and the recombination strength of the defective regions to assess their impact on mc-Si cell performance and meet M2.2. We have developed a model that transforms the inhomogeneous mc-Si cell with a distributed diffusion length to an equivalent homogeneous cell with an effective uniform diffusion length. This model uses an area-weighted average or effective uniform value of L_{eff} (L_{eu}) that is used to obtain the effective uniform bulk diffusion length (L_{bu}) or carrier lifetime (τ_{eu}). τ_{eu} represents the lifetime of a hypothetical homogeneous cell that will produce a Voc and efficiency equivalent to the inhomogeneous mc-Si cell. Thus, this model transforms the inhomogeneity into an effective homogeneous lifetime value, which is easy to relate to and understand.

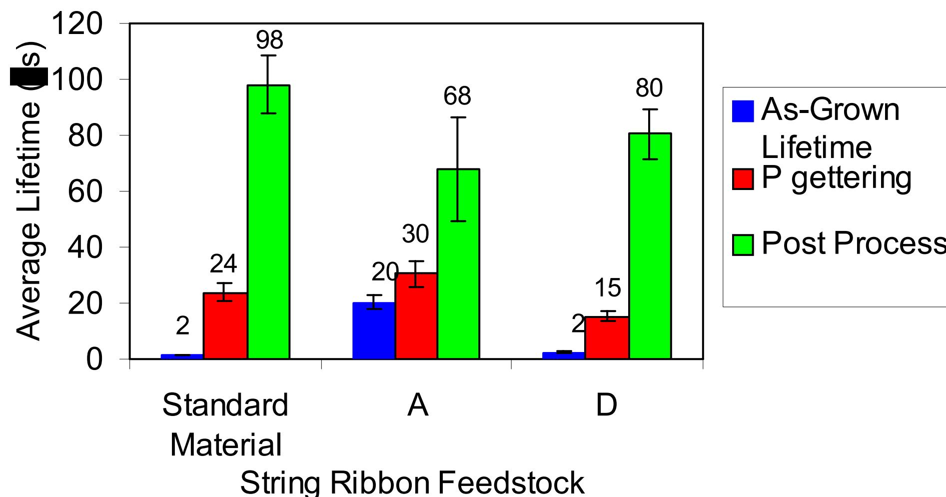


Fig. 4. Effect of defect gettering and passivation on the lifetime in ribbon wafers from standard and low-cost Si feedstocks

Hydrogen diffusion in silicon from PECVD silicon nitride film at high temperature

Hydrogen (H) diffusion in the silicon (Si) from the amorphous silicon nitride (SiNx) antireflection coating is critical for the defect passivation of low cost materials used in photovoltaics. The H concentration in Si is very low and usually below the detection limit [3,4,5], therefore, the positive effects of H released from hydrogenated SiNx (SiNx:H) film during a high-temperature annealing (hydrogenation) have been observed and reported mostly via indirect measurements of solar cells [6,7]. We report on the secondary ion mass spectrometry (SIMS) measurements of deuterium (D), which was released from the SiNx:D film, and “penetrated” through a defect-free c-Si wafer, during rapid thermal annealing. This study helps to quantify the amount of D that is injected into the Si during firing of the screen-printed contacts. From these measurements, the average flux of H through crystalline silicon is estimated. SiNx:D was deposited on the front-side float zone (FZ) wafers using deuterated silane (SiD4) and deuterated ammonia (ND3) as precursors in a low frequency PECVD reactor. RF sputtering was used to deposit defective α-Si films on the rear side of the wafer in argon environment. This sputtered layer was found to be a highly defective, which is ideal for trapping high concentrations of D.

Fig. 5 shows the D concentration profiles in the sputtered Si layer on the rear side of the FZ samples. The peak D concentration in the sputtered Si film for 1, 5, 60, and 300 sec anneal was found to be 3.84×10^{18}, 4.43×10^{18}, 5.23×10^{18}, and 7.87×10^{18} cm^{-3}, respectively. Fig. 5 also shows the D content in the sputtered Si layer for a sample which had no SiNx on the front and was co-annealed with the 300 sec sample. No D was detected in this sample, which establishes that the source of D detected in sputtered Si is the SiNx:D film on the front-side and D gets there via diffusion through the c-Si wafer. The concentration of the trapped D increases in the sputtered Si layer, as the anneal time increases, but the increase is limited by the supply of D from the SiNx:D film. The D concentration inside the sputtered Si layer shows a typical diffusion profile with a tail away from the c-Si/ sputtered Si interface, decreasing towards the free surface. This indicates the diffusion of D through the c-Si and into the sputtered Si, rather than diffusion from the ambient.

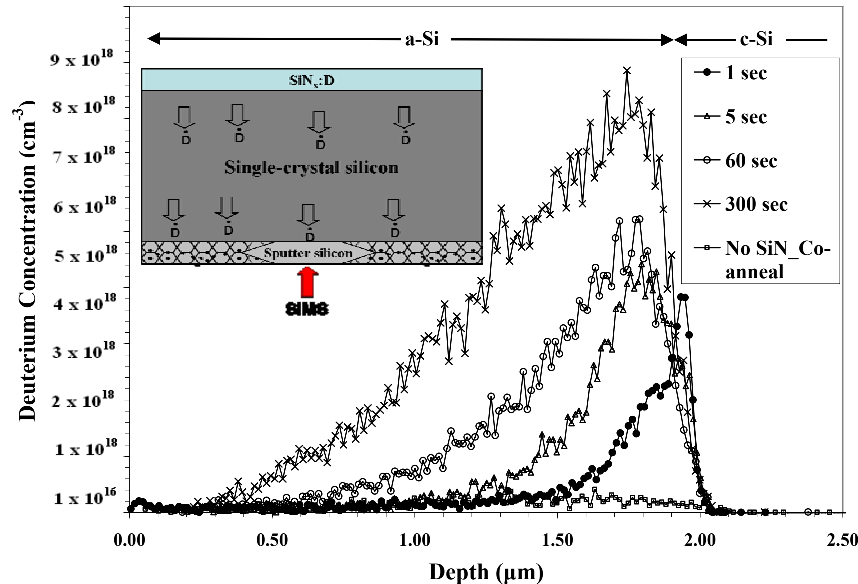


Fig. 5: Penetrated D concentrations in the sputtered Si layers on the rear-side of the wafers, released from the front SiN_x:D film, for a 215 μm thick p-type FZ wafer with a resistivity of 0.35 Ω.cm. These samples were annealed for 1, 5, 60 and 300 seconds at 750°C in an RTP chamber. Also shown is the D concentration for a sample with no SiNx:D film, but co-annealed with the 300 sec sample.

The average "areal density" of D in the sputtered Si layers was calculated from the integrated area under the concentration curves in Fig. 5. The areal density increases, but its slope decreases with the increase in anneal time. This suggests a rapid decrease in the rate of released D from the SiNx:D film. From the areal density of the trapped D, the average flux (areal density divided by anneal time, in $cm^{-2}.s^{-1}$) of D diffusing through the Si has been estimated. The average fluxes for the shorter anneal times are substantially higher than the ones for the longer anneal times. A higher flux of H, during a shorter time anneal, enhances defect passivation. For longer anneal times the flux of H decreases, which in turn decreases the ratio between the hydrogenated and the de-hydrogenated defects, resulting in inferior defect passivation, even though the total amount of released H from SiNx:H increases. It is important to recognize that at 750 °C, trapped H dissociates from the defect and hurts defect passivation, when the H flux decreases with time. If the total amount of D captured in the sputtered Si was trapped uniformly inside the 215 μm thick FZ Si, the concentration would be at least 4.7×10^{15} cm^{-3} for the 1 sec anneal and at least 2.7×10^{16} cm^{-3} for the 300 sec anneal, which can also be viewed as the defect passivating capacity for these anneal times.

To further study the effect of thickness and c-Si substrate, we also measured the penetrated D through a Czochralski (Cz) Si wafer of thickness 575 μm, which has oxygen in the bulk and could trap some D2. The peak concentrations for the 1 sec and 60 sec anneals were found to be 7×10^{17} and 5.6×10^{18} cm^{-3} respectively. This result shows that it only takes 1 sec at 750 °C for the D to penetrate through the entire 575 μm

thick wafer. This is consistent with the high Van Wieringen and Warmolz (VWW) diffusivity of H measured in single crystal Si[16]. Thus, even in the presence of defects like oxygen in Cz Si and more than twofold increase in thickness, a considerable amount of D was detected on the rear-side after the 1 sec anneal. This study demonstrates that D released from the PECVD SiNx:D film on top of Si, penetrates through the entire Si wafer. The c-Si wafers are highly transparent to D diffusion, therefore, a significant amount of the released D is captured by the sputtered Si layer on the rear-side of the sample.

Retention of H at the defects to achieve higher lifetime and cell efficiency on low-cost defective mc-Si

In this study, we investigated the retention of H at the defects which is very important to achieve higher lifetime and efficiency on low-cost defective mc-Si. As grown string ribbon wafers, which are very sensitive to hydrogenation, were gettered with $POCl_3$ for a time and temperature typically used to form the n^+ emitter during the solar cell

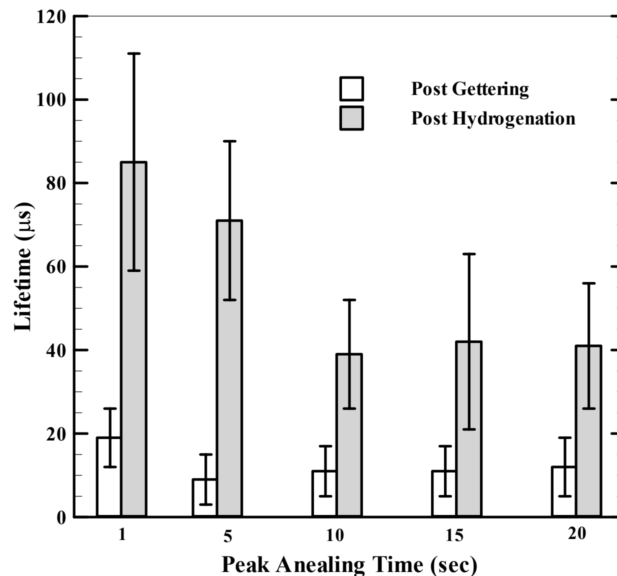


Fig. 6: Average lifetime of string ribbon wafers after gettering and hydrogenation for different peak annealing times. Error bars show the standard deviation.

fabrication. After etching off the emitter, post gettering lifetime was measured and then 80 nm thick low-frequency SiN_x:H films were deposited on these samples for hydrogenation study. After measuring the post gettering lifetime, samples were divided into two groups of lifetime greater and less than 15 μs. For every annealing condition, one sample from each group was chosen and annealed to see the effect of hydrogenation on the low and the high lifetime group. Lifetime was measured at four different locations on a wafer; hence the reported lifetime is an average of eight measurements on two different wafers. A faster cool-down would yield a higher lifetime due to the fast quenching of H at the defects. To study the effect of annealing time only,

the cool-down rate was kept constant to ensure that the change in lifetime observed is due to the change in annealing time only. Fig. 6 shows the QSSPC lifetime, with surfaces passivated by iodine methanol solution, after the gettering and hydrogenation steps. Highest lifetime is obtained for the shortest anneal time of 1 sec. Lifetime decreases as annealing time increases and saturates after just 10 sec of annealing. Due to the heating of the RTP chamber for longer anneal times; the cool-down rate is reduced. To ensure a fair comparison the cool-down rates of shorter annealing times were matched with the cool-down rate for the 300 sec anneal. The H flux values were also determined from SIMS profiles of D in Si, for different annealing times. For a similar cool-down profile, the lifetime values follow the same trend as that of the flux of H in the Si, showing the importance of rapid annealing to improve the quality of low-cost Si through hydrogenation from SiN_x. Hence a high flux of H for short annealing time is crucial for enhanced hydrogenation of defects in the Si bulk.

Task 3: Low-cost Formation of Rear Contacts with a Low Back Surface Recombination Velocity and a High Back Surface Reflectance

Promising dielectric materials that reduce the back surface recombination velocity in c-Si cells

We have explored several promising dielectric materials to reduce the back surface recombination velocity in c-Si cells. This research leading to the achievement of Milestone 3.1, which calls for an evaluation of the surface passivation characteristics of

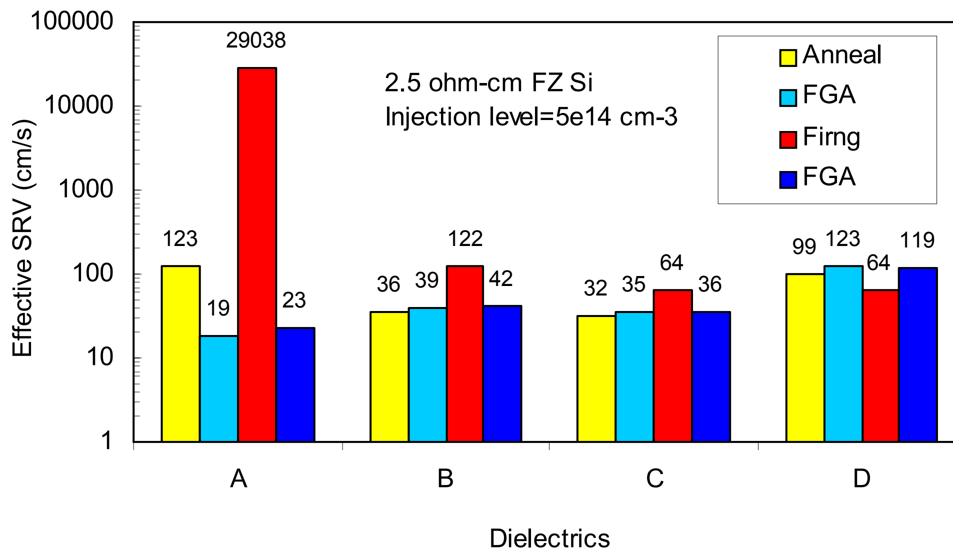


Fig. 7. Surface recombination velocity for different spin-on dielectrics measured at different process steps. The surface recombination velocity is calculated from the measured effective lifetime on 2.5 ohm-cm FZ Si at injection level of 5×10^{14} cm^{-3}.

various dielectrics and their stacks. To this point, the lowest back surface recombination velocity has been achieved using a dielectric film applied by a spin-on technique followed a brief anneal. The surface recombination velocity for several of these dielectrics on c-Si wafers is shown in Figure 7. Figure 7 shows that dielectrics B, C, and D result in very low surface recombination velocities on single crystal Si. We re also developing a process to open windows in the dielectric and form a local back surface field and rear contact in order to implement dielectric surface passivation and meet Milestone 3.2. Currently, the process for opening windows in the dielectric involves screen-printing of an etching paste, low temperature annealing for one minute, and removal of etching residue by water rinsing. We have found that this process can result in a good local BSF without significantly deteriorating the passivation quality of the dielectric.

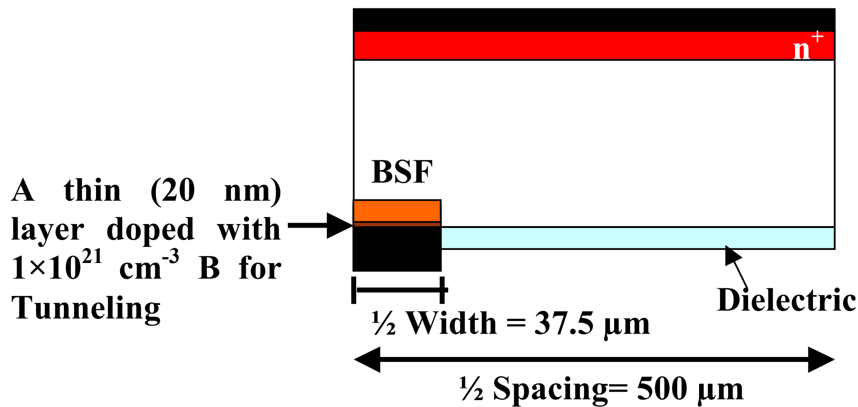


Fig. 8: 2D simulation domain used to investigate the impact of the fixed charge density in the back dielectric on the cell performance.

With the trend toward thinner Si substrates for crystalline Si solar cells, development of a back surface passivation scheme that can provide better quality surface passivation and internal reflection becomes very important. Additionally, the conventional process of forming full area Al-back surface field (BSF) induces high stress onto the Si substrate resulting in undesirable wafer warping. The most promising way to obtain high quality surface passivation and internal reflection is to use dielectric passivation.

Simulations were performed using a multi-dimensional semiconductor simulation program DESSIS™ to study the impact of the fixed charge density in the back surface passivating dielectric on the solar cell performance. The unit device structure used in the simulations is shown in Fig. 8. It consists of a back contact formed through a dielectric with a 75 µm line width and a 1000 µm spacing. A thin (20 nm) heavily B-doped (1×10^{21} cm^{-3}) p+ Si layer is introduced underneath the contact to allow simulation of an ohmic back contact via a tunneling mechanism. A shunt path between the dielectric-induced inversion layer and the back contact is intentionally introduced in

Table 1: Fixed parameters used in the simulation.

Parameters	Values
Emitter sheet resistance	80 Ω/sq
Cell thickness	200 μm
Resistivity	2.0 Ω-cm
Front surface recombination velocity	60,000 cm/s
Back surface recombinatoin velocity (BSRV) at dielectric	S_{n0} =1000 cm/s S_{p0} = 15 cm/s With midgap trap $(E_t=(E_c+E_v)/2)$
Effetive BSRV at the contact (BSRV including BSF effect)	<300 cm/s
Optical generation	Textured 8.5% shading with SiN_x (750 Å n=2) R_{front} (internal)=0.92 R_{back} (internal)=0.85
Contact resistance	0 ohm-cm^2
Contact formation	Line contact (2D), 75 μm width, 1000 μm spacing

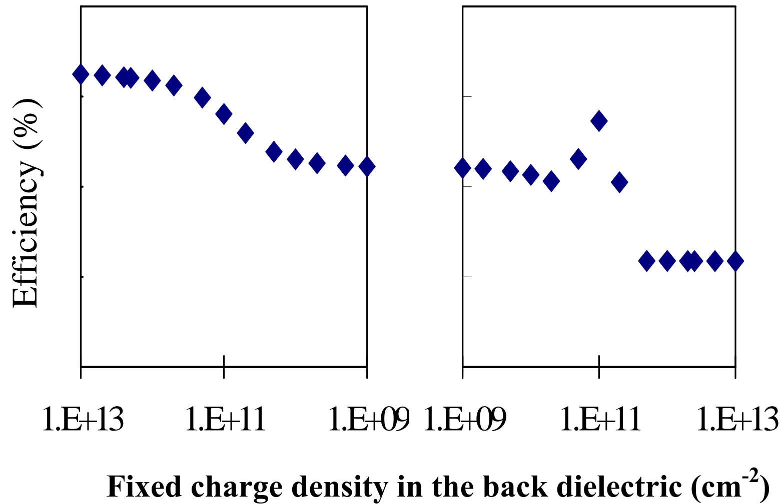


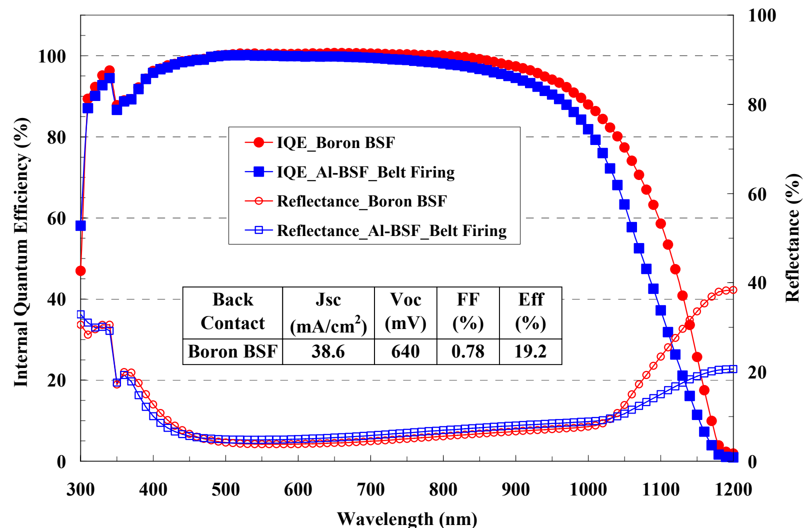
Fig. 9: Simulated efficiency of dielectric back-passivated p-type Si solar cells as a function of the fixed charge density in the back dielectric in the presence of back contact shunting.

this model by the use of a low work function (4.1 eV) metal back contact. Because of its low work function, the contact itself induces an inversion layer in between the metal and the B-doped p+ layer forming a direct path for electrons to flow from the dielectric-induced inversion layer to the contact. It should be recognized that this structure is solely used as a tool to allow the simulation of a shunt path in the device, and is not intended to represent the actual mechanism responsible for the parasitic shunting in real devices. Another point worth mentioning is that this condition represents the worst case of the parasitic shunting, where electrons in the dielectric induced inversion layer can flow readily to the contact with negligible resistance.

The fixed material and device parameters used in the simulations are summarized in Table 1. The values for the fundamental recombination velocity of electron (Sn0) and hole (Sp0) at Si/dielectric interface were taken from [8], where they were used to simulate the recombination activity at the Si/SiO2 interface. The simulated solar cell efficiency as a function of the fixed charge density in the back dielectric is shown in Fig. 9. The simulations reveal that, for a 2 Ω-cm p-type substrate, the positive charge density should be kept below $1x10^{11}$ cm^{-2} to avoid a low performance caused by parasitic shunting of the inversion layer. Model calculations also show that obtaining negatively charged dielectric is even more desirable, because the passivation is achieved via an accumulation of majority carriers rather than an inversion. This forms one of the required properties of a dielectric to be used as a back surface passivation layer of p-type Si solar cells.

Development of a boron back surface field formed using boric acid

A high quality back contact with low back surface recombination velocity (BSRV) and high back surface reflectance (BSR) is one of the key requirements for achieving high efficiency crystalline silicon solar cells. This requirement is even more critical for achieving high efficiency on thinner substrates, which is the current strategy adopted by PV industry for reducing the cost of crystalline silicon solar cells. A boron BSF is one of the promising techniques for achieving high quality back contact. It has three advantages over the screen-printed Al-BSF as: 1) it can be formed without inducing high stress in the substrate, 2) it can be used in conjunction with a dielectric passivation to further enhance the



Back Contact	Jsc (mA/cm^2)	Voc (mV)	FF (%)	Eff (%)
Boron BSF	38.6	640	0.78	19.2

Fig. 10: IQE and reflectance as a function of wavelength for solar cells with the B-BSF and Al-BSF.

passivation and optical properties, and 3) it can provide higher p+ doping concentration because of its higher solid solubility limit in Si allowing better passivation to be achieved. In this study, a novel process for boron diffusion is presented where boric acid diluted in deionized water is used as a boron source.

A heavily doped boron emitter was formed by spin coating the boric acid onto Si wafers followed by annealing in the diffusion furnace or an RTP chamber. Various sheet resistances and doping profiles were obtained by adjusting the diffusion temperature, time and concentration of the boric acid solution. J_{oe} values of ~100 fA/cm^2 were obtained on a ~100 Ω/sq boron emitter with SiO_2-based dielectric passivation. The effective bulk lifetime of completed cells was measured to be > 500 μs in 1.3 Ω-cm p-type FZ wafers. A solar cell efficiency of 19.2 % was achieved on FZ Si with a B-BSF due to the enhanced back contact performance. The benefits of B-BSF in the IQE and back reflectance are clearly shown by the enhanced long wavelength response of IQE and reflectance shown in Fig. 10. The reflectance values at above 1030 nm wavelength indicate that BSR of B-BSF contact is higher than that of the Al-BSF contact. The blue response is also seems to be high due to the oxide passivation of the emitter during the annealing of rear dielectric. However, the V_{oc} (~640 mV) of the completed cells is significantly lower than the implied V_{oc} (660-665 mV) measured before the metal contact formation process. We are currently investigating the interaction between the dielectric and the metal contact as well as the cause of high diode ideality factor in order to improve the cell efficiency.

Light Trapping in crystalline silicon solar cells with rear local contacts

Dielectric passivation of the rear side of Si solar cells has recently gained attention for use in production of high-efficiency cells. Compared to the standard screen-printed AL-BSF passivation scheme, suitable dielectrics can provide a lower BSRV and a higher Voc and are easily applicable to thin (~100um) cells since they do not create any wafer bowing [9]. In order to maintain the passivating effect of a rear dielectric after contact formation, the metal fraction covering the rear must be kept as low as possible. This requires point contacts formed either through opening windows or punching through the dielectric. In laboratory devices, evaporated silver or aluminum are commonly used to connect these point contacts since they are highly conductive and can serve as a back surface reflector (BSR). However, evaporated metals are not a viable method for low-cost solar cell production. Additionally, they are highly specular reflectors, resulting in inefficient light trapping. Light-trapping is especially critical in thin cells since as wafer thickness drops, an increasing fraction of the incident light reaches the rear of the cell without being absorbed. Therefore, an ideal rear reflector must be a Lambertian scatterer in addition to being highly reflective and conductive. Random scattering results in light-trapping (via total internal reflections) which can offset the impact of having a thinner substrate. In this quarter we investigated two new light-scattering BSR materials, which can connect rear point contacts formed through a dielectric.

For an ideal Lambertian BSR, the total escape reflectance (which is the total reflectance less the reflectance of the front surface, i.e. only the light reflected by the rear) and diffuse reflectance curves are expected to be nearly identical.

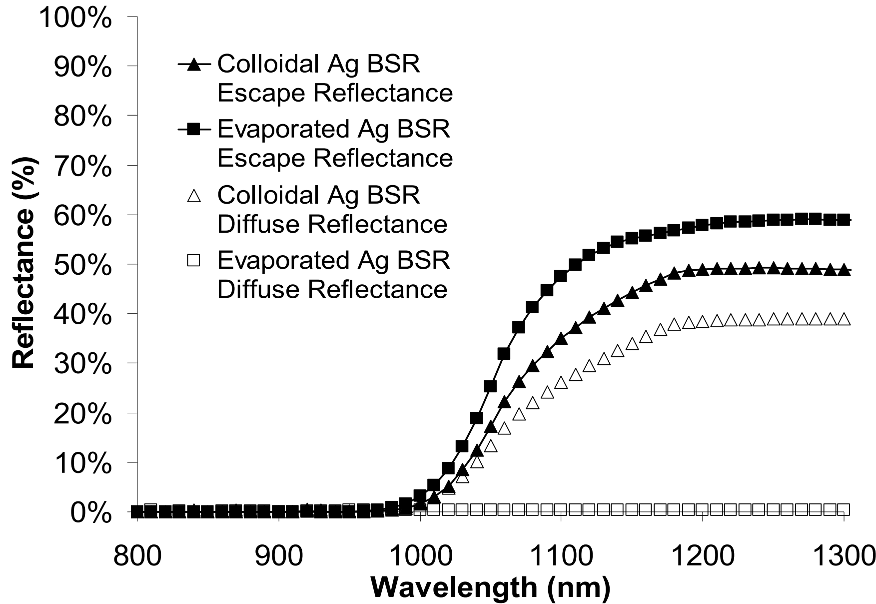


Fig. 11. Total escape reflectance and diffuse reflectance curved for Evaporated Ag and Colloidal Ag BSRs

A Lambertian reflector should show also low escape reflectance due to light-trapping since scattered light suffers multiple total internal reflections within a sample. Fig. 11 shows total and diffuse reflectance curves for evaporated Ag and Colloidal Ag. Wavelengths above 800 nm were chosen for these measurements since on 200 um substrates, rear reflectors will largely reflect only those wavelengths that are not strongly absorbed by silicon. The evaporated Ag BSR shows a very high total escape reflectance (closed squares) that is almost 100% specular (as observed by the near-zero diffuse reflectance). In contrast, the Ag colloid BSR exhibits a much lower total escape reflectance (closed triangles). In addition, the diffuse reflectance curve for the Ag colloid BSR (open triangles) shows that a majority of the light reaching the Ag colloid BSR is scattered. This indicates that the silver colloid BSR is highly (but not perfectly) scattering and that at least part of the lower escape reflectance using a Ag colloid BSR is a result of better light trapping. Using the quantitative method outlined by Ristow et al., the reflectance and the Lambertian character of the BSRs were calculated at 1300 nm [10-13]. These are tabulated in Table 2 where β is a percentage of light scattered by the BSR – the higher the percentage, the more Lambertian/randomly scattering is the reflector. R_B is the internal back reflectance of the BSR.

Table 2. Comparison of the Lambertian/scattering character (β) and internal reflectance at 1300 nm.

BSR	R_B (%)	β (%)	J_{SC} – Sunrays (mA/cm^2)
Al-BSF	60.0	99	42.2
Evaporated Al	91.6	11.5	41.6
Evaporated Ag	92.9	9	41.5
SP Ag	98.7	67.5	42.4
Colloidal Ag	97.3	81.6	42.4

The data in Table 1 confirms that while the evaporated reflectors are highly reflective, they are almost perfectly specular which results in poor light-trapping. However, both the colloidal Ag and the SP Ag BSRs scatter most of the light reaching them, with the colloidal Ag BSR being much closer to the Lambertian ideal (β=100%) than the SP Ag BSR. However, the colloidal Ag has a lower R_B compared to SP Ag. From this reflectance data alone, it is unclear which of the two scattering BSRs will result in a higher short-circuit current. Therefore, ray tracing simulations using the Sunrays program were performed. The simulated J_{SC} for both scattering BSRs are identical, which indicates that the respective strengths of the two scattering BSRs (R_B for the SP Ag and β for the colloidal Ag) balance each other out. The simulation results also indicate that the scattering BSRs provide a significant current boost (+0.8-0.9 mA/cm^2) over the evaporated BSRs and a modest boost (+0.2 mA/cm^2) over an Al-BSF BSR. The simulation model assumed a 300 um thick substrate with a textured front surface with an 800 Å oxide-SiN AR stack. Solar cells were fabricated with either a local or full-area Al-BSF, and the and the colloidal Ag BSR.

Table 3. I-V data for solar cells (4 cm^2) with the Al-BSF and dielectric passivation with a BSR.

Cell	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Eff (%)
Colloidal Ag BSR	639	38.9	75.1	18.7
Al-BSF	639	37.9	75.3	18.2

The new scattering BSR shows an advantage over the full-area Al-BSF cell and results in a cell efficiency of 18.7%.

Task 4: Surface Texturing and Light Trapping

Texturing cast mc-Si wafers

The milestones in this task target an efficiency enhancement due to surface texturing of 0.7% for single crystal cells (M4.1), and 0.3% for mc-Si cells (M4.2) through a reduction of the surface reflectance. We have successfully developed and implemented a process to produce random texturing (pyramid size 3-5 μm) for single crystal solar cells. This surface texturing has led to a 1.9% efficiency enhancement on float zone silicon cells which is greater than the expected enhancement exceeds the target efficiency enhancement of 0.7% in M4.1. Analysis of these cells showed that the decrease surface reflectance associated with texturing is responsible for a ~1% efficiency enhancement. An additional efficiency enhancement of 0.8% to 0.9% is attributed to an improved fill factor in single crystal Si cells with surface texturing. We have also developed a surface texturing process for mc-Si wafers that leads to a 0.7% efficiency enhancement. This enhancement is due to improved short circuit current and fill factor. However, the weighted reflectance for this texturing process on mc-Si wafers, shown in Fig. 12, is not less than 13% after deposition of a SiN AR-coating.

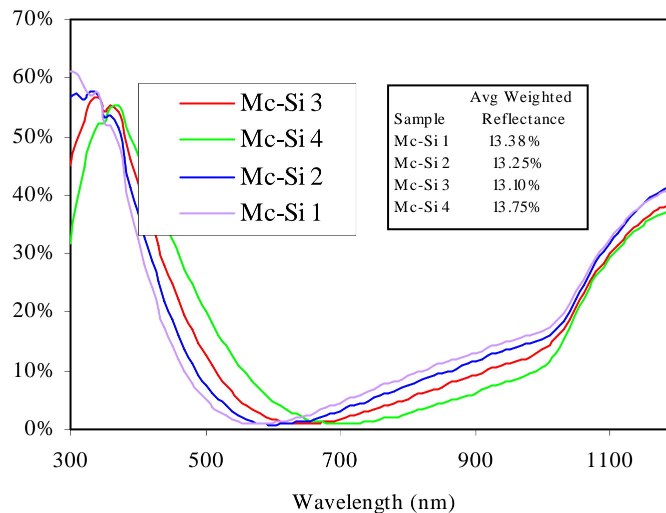


Fig. 12. Preliminary results of the reflectance of textured mc-Si wafers after deposition of a SiN AR-coating.

Texturing ribbon Si wafers

String Ribbon Si is an inexpensive material for the fabrication of solar cells and shows promise as a cost-effective alternative to single crystal silicon. To date, 4 cm^2 cells with a peak efficiency of 16.8% have been reported earlier on cells with screen-printed contacts. These high efficiency cells used SiNx as the single layer antireflection coating (SLAR) with no surface texturing. The effect of texturing on String Ribbon Si and its potential for high efficiency low-cost was investigated in this study. Reflectance

measurements were made at each stage of cell processing. As can be seen in Fig. 13, the texturing of String Ribbon wafers reduces their weighted reflectance to 9.4% after deposition of the SiN ARC. While this decrease in reflectance is less than that typically observed in single crystalline materials (also shown in Fig. 5), this represents a substantial potential increase in the current density (1-1.5 mA/cm^2) and cell efficiency (0.5% absolute) of String Ribbon cells. The J_{sc} obtained in the textured cells was higher than those obtained on the untextured cells by an average of 1 mA/cm^2 and current densities of over 35.5 mA/cm^2 are the highest reported on String Ribbon Si solar cells with screen printed contacts. In the case of the screen-printed textured wafers, the best efficiency was 16.8%, which is equal to the best on the untextured String Ribbon Si reported earlier. It is proposed that with an improved lifetime and optimized contact firing, the V_{oc} can be improved and the efficiencies can reach values higher than those on untextured String Ribbon.

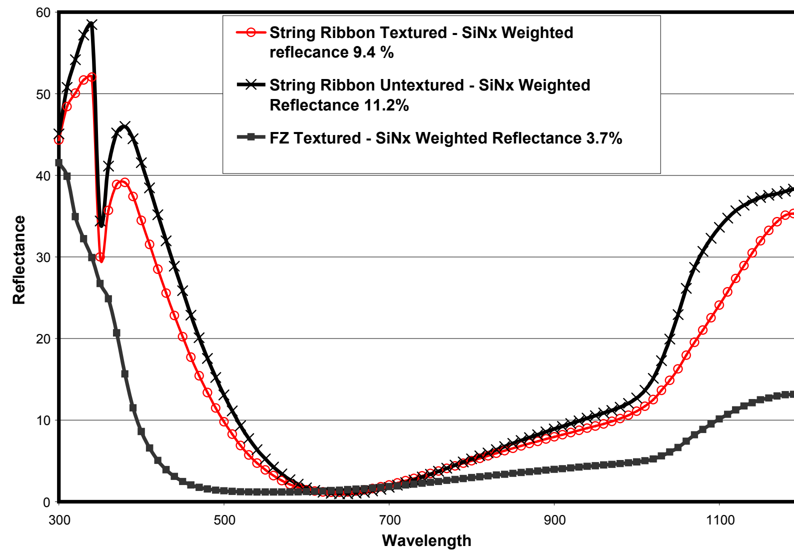


Fig. 13: Comparison of reflectance between untextured String Ribbon, textured String Ribbon and textured FZ

Task 5: Improvement of front surface passivation and contacts in high-efficiency commercial ready c-Si solar cells

Plasma enhanced chemical vapor deposition (PECVD) deposited silicon nitride (SiNx) films are widely used to provide a surface passivation and an anti-reflection (AR) coating on the phosphorus-doped emitter. SiNx films provide good surface passivation on the emitter due to its highly positive fixed charge density which induces an inversion or accumulation layer in Si under the SiNx. Recently, PECVD-deposited SiCx films have been studied for the surface passivation of crystalline silicon (c-Si) as low surface recombination velocity (SRV) lower than 30 cm/sec has been reported at the SiCx/c-Si interface [14,15]. SiCx films also have a high refractive index (greater than 2.3), suggesting that SiCx may be an improvement over PECVD deposited SiNx. SiNx and SiCx films typically require dangerous pyrophoric silane (SiH_4) gas as a silicon source, which is a significant inhibiting factor in the cost reduction economies-of-scale strategies employed by silicon PV plants. A novel silane-free process and apparatus for a solid source has been developed at SiXtron Advanced Materials to eliminate the storage and handling of dangerous pyrophoric silane gas in a manufacturing line. The solid source can be connected to the existing silane gas line to replace it. In this study, we

investigated the optical and electrical properties of dielectric films deposited with the solid source for the surface passivation of c-Si solar cells.

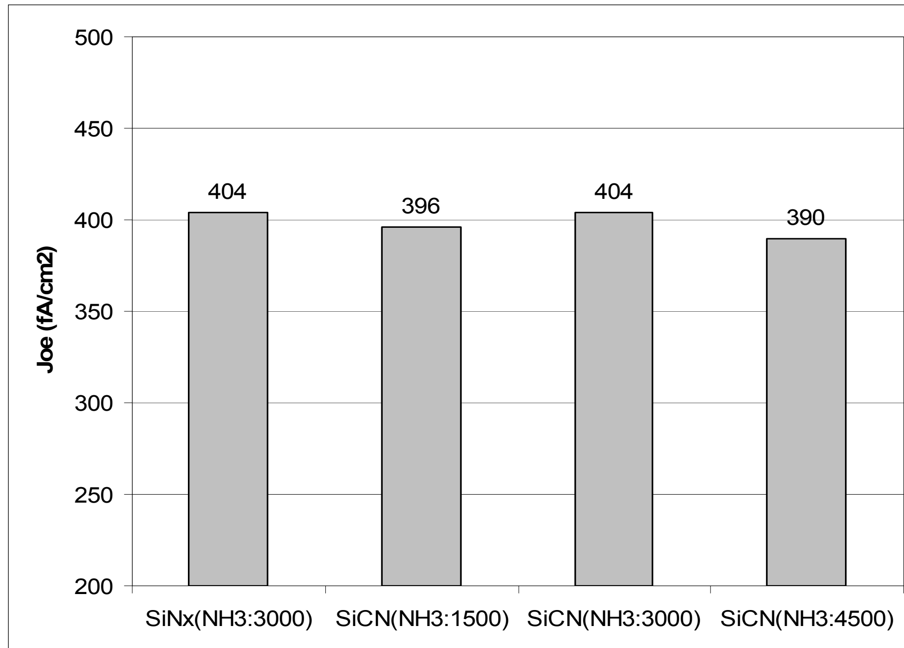


Fig 14. J_{oe} values of 45 ohm/sq emitters as a function of NH_3 gas flow rate. The samples were annealed in an RTP chamber at 850 ^oC for 5 sec.

J_{oe} values were measured on 45 ohm/sq textured emitters in order to study electrical properties of SiC_xN_y films coated with different NH_3 gas flow rates and compare with those of SiN_x films as shown in Fig. 14. All the samples were fired in an RTP chamber at 850 ^oC for 5 sec before J_{oe} measurement. It is found that there was no much difference in J_{oe} values between SiN_x and SiC_xN_y films regardless of NH_3 gas flow rate in the range of 1500-4000 sccm. These comparable properties of SiH_4-free process to those of the SiH_4 process mean that the SiC_xN_y can provide an excellent cell performance when the film is utilized for the front surface passivation of Si solar cells. Fig. 15 shows the surface charge densities, Q_{FB} in the dielectric films after annealing in an RTP chamber at 850 ^oC for 5 sec. The surface charge density plays a critical role to the surface passivation as well as a device performance [16,17]. The surface charge density in the SiC_xN_y film was measured to be in the range of 1.58-1.77x10^{12}/cm^2 which is slightly lower than that of SiN_x film (1.89x10^{12}/cm^2). It seems to be that the comparable J_{oe} values of SiC_xN_x films to that of the SiN_x film in Fig. 14 are caused by highly positive surface charge density and relatively high hydrogen concentration.

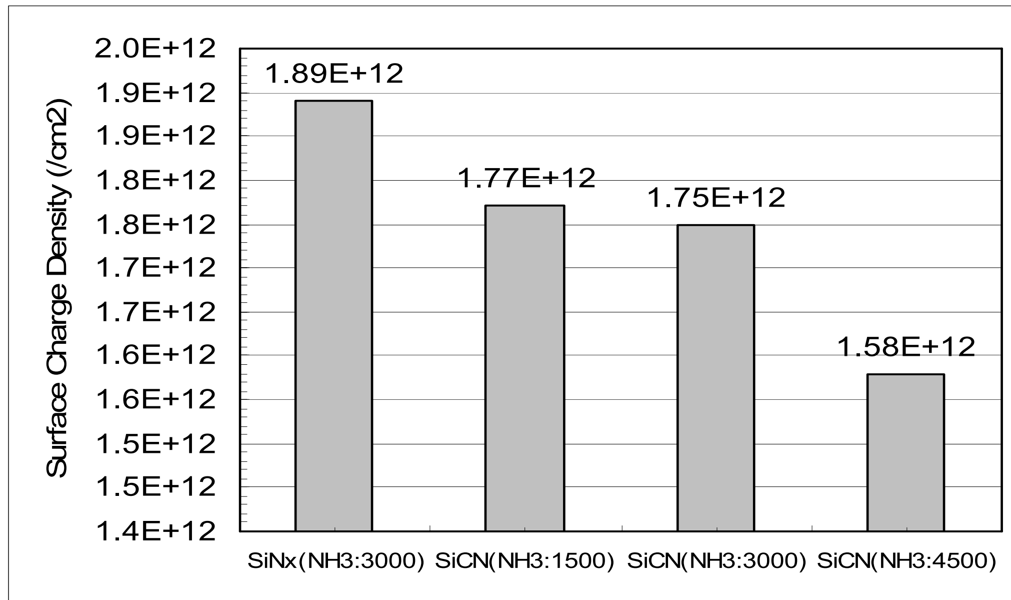


Fig 15. Surface charge densities of SiN_x and SiC_xN_y films as a function of NH_3 gas flow rate after annealing in an RTP chamber at 850 ^oC for 5 sec.

SiC_xN_y films coated with the new solid source were applied to the solar cell fabrication to compare their performance with that of a conventional PECVD SiN_x film. Table 4 shows the current-voltage characteristics for the solar cells with AR layers deposited using SiH_4 and new solid source. It is impressive that a cell efficiency above 16.8% was achieved on the solar cells with SiC_xN_y AR coatings deposited using the new solid source. Both Si sources provided comparable J_{sc} and V_{oc} values while slight difference FF was observed. The comparable J_{sc} and V_{oc} can be attributed to high-quality optical and electrical properties of the SiC_xN_y films. It is interesting that SiC_xN_y AR coatings shows higher FF than SiN_x film does, which seems to be related to the different etching behavior of the glass frit in the Ag paste for different dielectric films. The contact formation process will be further investigated to understand the difference in FF.

Table 4. Performance of 149 cm^2 solar cells with ARC layers deposited using SiH_4 and new solid source as a Si source. The emitters were industrial type phosphorus diffused emitters with ~ 60 ohm/sq sheet resistance.

ARC	NH_3 (sccm)	Eff (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)
SiN_x	3000	16.82	619.7	35.90	75.6
SiC_xN_y	1500	16.84	616.9	35.51	76.9
SiC_xN_y	3000	16.89	616.7	35.71	76.7

Fig. 16 shows the internal quantum efficiency (IQE) and reflectance values measured on the two types of cells. From blue and long wave length responses, SiC_xN_y films deposited from the new solid source developed at SiXtron provides a high surface passivation quality without hurting bulk lifetime.

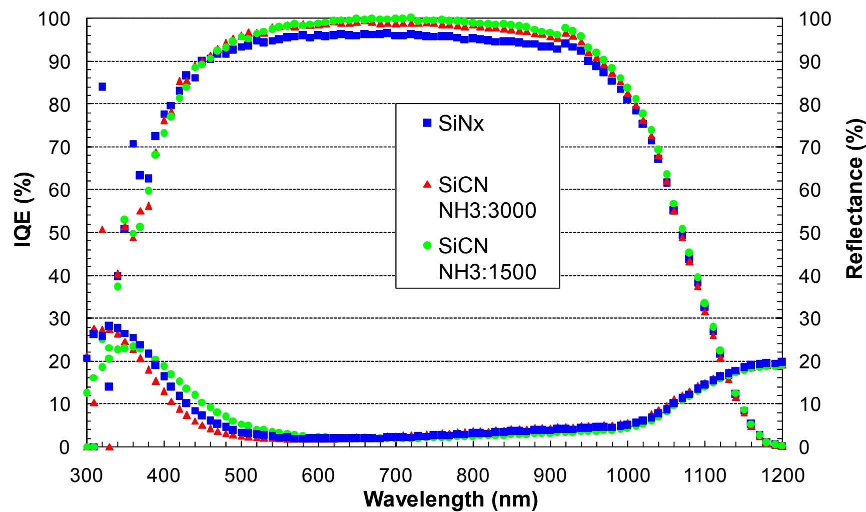


Fig 16. IQE responses of the solar cells with the SiN_x AR layer coated using SiH_4 source and SiC_xN_y AR layer coated using the solid source.

Task 6: Investigation of novel rear surface passivation and contact schemes

Application of spin-on dielectrics to c-Si solar cels

The development of low-cost Local Back Surface Field (LBSF) technology is critical for commercially viable high efficiency thin solar cells. Structures that have demonstrated better performance than a full area BSF [18] usually involve multiple high temperature steps or expensive and low throughput processes. Charge control in the rear dielectric for surface passivation is also an important factor in achieving high performance and cost-effective LBSF solar cells [19]. Recent work at Georgia Tech has demonstrated the use of spin-on dielectrics for tailoring the charge for effective rear passivation of solar cells [20]. An appropriate spin-on SiO_2 / PECVD SiN_x stack was found to be effective in reducing or controlling the inversion of the rear surface, which is important for reduced parasitic shunting in the LBSF structures. The use of spin-on phosphorous for limited source diffusion has also been demonstrated at Georgia Tech [21]. Spin-on limited source diffusion provided high quality emitters, while providing flexibility with profile engineering. This study demonstrates a spin-on solution based process for the

simultaneous formation of emitter and rear dielectric passivation resulting in ~19 % efficient screen-printed solar cells with Al-LBSF structure.

In this study, 4 cm^2 were fabricated on 300 μm thick 1.3 ohm.cm p-type wafers. Solid source wafers for limited source diffusion were prepared in-house which enables the in-situ front and rear oxidation due to negligible glass formation. Spin-on dielectric was applied on the rear surface prior to phosphorous diffusion. After the single step phosphorous diffusion and front and rear passivation, nitride coating was deposited on the front and rear. After opening the vias on the rear by screen printing of an etching paste, Al was screen printed on the rear and Ag grid on the front followed by cofiring. The nine 4 cm^2 cells were isolated with a dicing saw and subjected to a forming gas anneal (FGA) at 400°C before cell testing.

Table 3 shows the I-V data of these Al LBSF cells with spin-on dielectric passivation. The highest efficiency achieved on these cells was 18.9 % on wafers with a sheet resistance of 55 Ω/□ with an average efficiency of 18.7 %. The distribution of cell efficiencies on all wafers was found to be quite uniform as indicated by the average values of the I-V parameters. The V_{oc} and J_{sc} values for these cells were found to be higher than those obtained on reference cells with a similar emitter and a full area BSF. This demonstrates superior passivation, good local BSF and a good back reflector. Further analyses and modeling will be shown to quantitatively support the observed improvements in V_{oc} and J_{sc} in these cells along with the merit of using this process for thinner cells.

Table 3: Results of I-V testing with the best and average results for three different sheet resistances.

	Sheet ρ (Ω/□)	Voc (V)	Jsc (mA/cm^2)	FF (%)	Eff (%)
Average	**40**	**0.640**	**37.7**	**75.5**	**18.2**
Best		**0.641**	**38.2**	**75.4**	**18.5**
Average	**48**	**0.644**	**38.3**	**72.4**	**17.9**
Best		**0.644**	**38.5**	**74.0**	**18.4**
Average	**55**	**0.647**	**38.5**	**74.9**	**18.7**
Best		**0.648**	**38.6**	**75.6**	**18.9**

Notice that while J_{sc} and V_{oc} were high, the fill factors (FF) were low for these cells. With further optimization of the emitter and contact formation process, FF of >0.77 are expected which should further increase the efficiency of these cells. Passivated emitters diffused for these cells had a J_{oe} of 155 fA/cm^2 for a sheet resistance of 55 Ω/□. Further optimization of the diffusion profile for high sheet resistance emitters is expected to reduce the J_{oe} to ~120 fA/cm^2. The implementation of high sheet resistance emitters, which is being attempted, is expected to give even higher V_{oc} and J_{sc} resulting in screen printed cell efficiencies of around 19.5 %.

A simple boron diffusion process for high Voc in c-Si solar cells

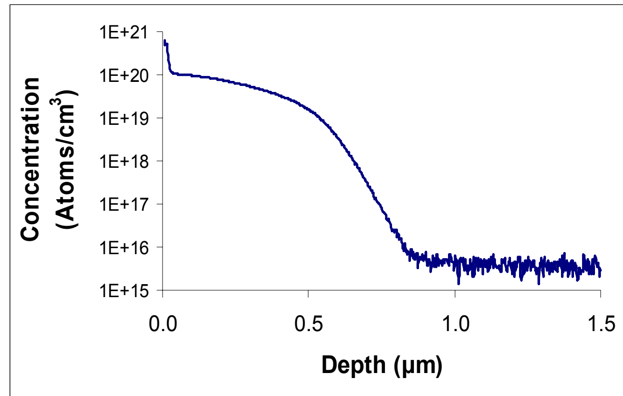


Fig. 17 Boron doping profile after < 30min diffusion at 1000C using a Boric Acid solution as the dopant source.

We have established a simple process scheme for achieving high open-circuit voltages (640 mV and higher) on p-type FZ silicon solar cells with a shallow (~0.8 µm), continuous B-BSF and screen-printed contacts. These cells are processed without any photolithography or evaporation steps. Analysis of the fabrication process and the finished cell are used to quantify the impact of the short boron diffusion process and the impact of the local contacts on the rear. Screen-printed n-p-p^+ solar cells with an active area of 4 cm^2 were fabricated on 0.6 and 1.3 Ω-cm float zone (FZ) Si. A short (< 30 minutes) boron diffusion was performed using a dilute boric acid solution as the dopant source. Phosphorous diffusion was performed using phosphoric acid as the dopant source to obtain n^+ emitters of 75-100 Ω/□. After removal of the boron and phosphorous glasses, the front and rear surfaces were passivated in a single step with a thermal oxide on the front and a spin-on dielectric on the rear. After deposition of a PECVD SiN_X layer on the front, Ag and Ag/Al pastes were screen-printed on to the front (grid pattern) and rear (point contact pattern) of all wafers. The size of the square rear point contacts was varied in order to study their impact on B-BSF passivation quality. All the cells were then co-fired using the same firing recipe. A conductive, light-scattering

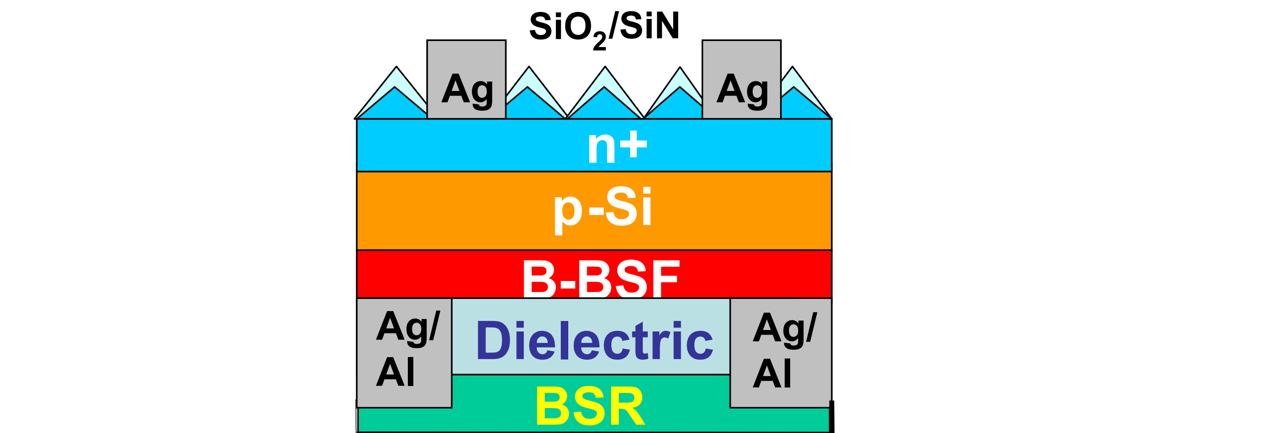


Fig. 18 Cell Structure with B-BSF and local rear contacts.

film was used to electrically connect the rear local contacts after firing [22]. To characterize the J_{0e} of the Boron BSF, 500 Ω-cm n-type float zone wafers were diffused on both sides and passivated with a thermal oxide annealed in N_2.

Figure 17 shows the doping profile of the B-BSF resulting from the short diffusion process. The ~0.8 µm deep B-BSF has a sheet resistance of 40-45 Ω/□. On a 500 Ω-cm n-type Fz Si wafer diffused with Boron on both sides, a J_0 value of 117 fA/cm^2 was measured which sets a V_{OC} limit of ~680mV. After phosphorous diffusion and surface passivation, implied V_{OC}s of 670 mV+ were measured using the QSS-PC method for devices with 100 Ω/□ emitters. The small drop in achievable V_{OC} indicates that there is little degradation of the rear passivation during the emitter diffusion and surface passivation steps. Additionally, after removing the metal contacts and etching off the doped layers on a finished solar cell (Fig. 18), an effective lifetime of 450 µs was measured using Iodine/Methanol passivation. This indicates that degradation of bulk lifetime was avoided. However, since the B-BSF is shallow, it is sensitive to surface conditions and increased recombination at the rear after screen-printing and firing of contacts provides a pathway for V_{OC} loss. The presence of this loss mechanism is seen in LBIC maps where the effect of the rear metal points is observed as points of degraded passivation. The impact of this V_{OC} loss mechanism can be controlled by reducing the size of the rear local contacts. Fig. 19 shows that a reduction in the size of the rear contacts from 120 µm to 100 µm resulted in an average V_{OC} gain of 4 mV (for the cell structure in Fig. 18). On cells with a planar front surface, a larger V_{OC} gain of 16mV was observed and the loss in V_{OC} after metallization (i.e. the difference between Implied V_{OC} and cell V_{OC}) was limited to just 11 mV.

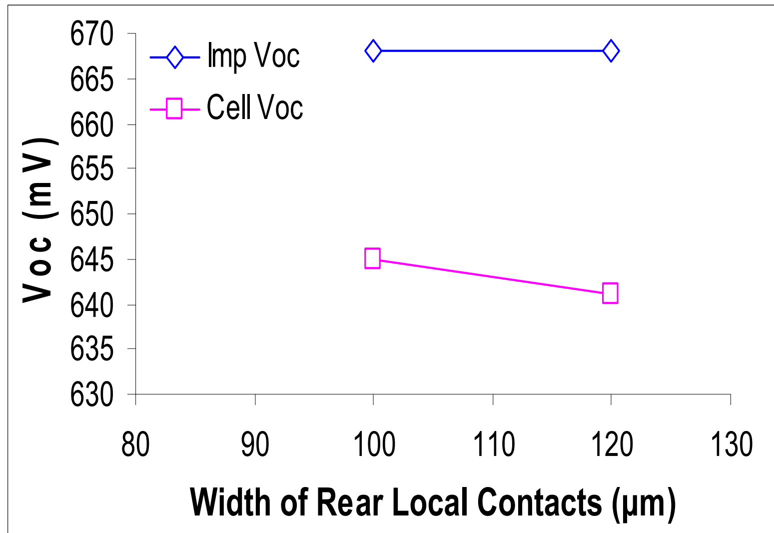


Fig. 19 Variation in open-circuit voltage with width of rear local contact for cells with a textured front surface.

With 100 µm wide screen-printed rear local contacts and an emitter sheet resistance of 75 Ω/□, a maximum cell efficiency of approximately 19% (Table 5) was achieved with a high V_{OC} of 646 mV on 1.3 Ω-cm p-type FZ material (cell structure in Fig. 18). V_{OC} of 650 mV was achieved for the same device structure on 0.6 Ω-cm p-type FZ material. The high ideality factor (~1.4) and low FF (~76%) exhibited by these cells can be improved by optimization of the front contact formation process. In addition, further V_{OC} gains are expected from a reduction of the rear contact width to 80 µm. These modifications can raise the efficiency of this screen-printed, passivated B-BSF cell structure to the 19-20% range.

Table 5: Lighted I-V data on 4 cm^2 1.3 Ω-cm cells.

Efficiency (%)	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	n-factor	R_S (Ω-cm^2)	R_{Shunt} (Ω-cm^2)
18.9	642	38.8	76	1.4	0.5	10670

Task 7: Development of high-efficiency cells on thin c-Si wafers

Development of high-efficiency thin silicon solar cells with screen-printed contacts

The current silicon feedstock crisis has accelerated the need for using thinner substrates. In addition, solar cells using thin mc-Si wafers are expected to be less sensitive to material inhomogenieties because of the higher diffusion length to thickness ratio. There are several challenges with the use of thin wafers including: a) reduced yield, b) bowing of the wafers due to contact firing of a full area Al-BSF, and c) reduced mechanical stability due to surface texturing. Some of these challenges can be overcome by appropriate cell designs and processing so that the advantages of reducing thickness can be harnessed. This study focuses on the impact of thin wafers on the cell performance using the current screen-printed industrial process. In this study, performance of 4 cm^2 screen-printed solar cells made on mono and mc-Si wafers in the range of 115-280 μm were analyzed and compared. The contact firing cycle for each thickness was adjusted so that all the wafers experienced the same peak contact firing temperature. This was necessary to ensure comparison of the impact of thickness reduction alone. We obtained efficiencies of 15.7% and 16.5% on 115 μm thick HEM and FZ wafers, respectively. The 4 cm^2 screen-printed cells were un-textured, single layer SiNx antireflection (AR) coated with full area aluminum back surface field (Al-BSF). Identical processing on 280 μm thick wafers gave screen-printed un-textured cell efficiencies of 16.8% (HEM) and 17.4% (FZ). The ~1% difference in the efficiency of thick and thin cells was analyzed by detailed cell characterization and PC1D modeling. Bulk lifetime was found to be in excess of 200 μs for all the cells, which made the thin cells more sensitive to back surface recombination velocity (BSRV) and less dependent on lifetime. It was found that the high BSRV (~400 cm/s) and low back surface reflectance (BSR) (~65%) associated with the full area Al-BSF were the major reasons for the lower performance of thin cells. BSRV of ≤100 cm/s and BSR of ≥ 95% could virtually eliminate the gap between 280 μm and 115 μm thick cells. Cost modeling was also performed to show that reducing the thickness of the wafers to 115 μm reduces the module manufacturing cost in spite of lower cell efficiency.

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Spending Summary – 10/01/06 to 6/31/08

Object Class Categories Per SF 424a	Approved Budget	Project Expenditures
a. Personnel	$787,385.00	$875,678.78
b. Fringe Benefits	$165,477.00	$173,962.36
c. Travel	$10,354.00	$42,332.55
d. Equipment	$225,000.0	$225,000.00
e. Supplies	$261,392	$319,034.13
f. Contractual	$0	$0.00
g. Construction	$0	$0.00
h. Tuition	$58,323.00	$58,024.78
i. Total Direct Charges (sum of a to h)	$1,507,931.00	$1,469,031.60
j. Indirect Charges	$617,379.00	$668,341.16
k. Totals (sum of i and j)	$2,125,310.00	$2,137,372.76
DOE Share	$1,662,515.00	$1,653,054.60
Cost Share	$462,795.00	$484.318.16
Calculated Cost Share Percentage	22%	22.7%