Wire Position Monitoring with FPGA based Electronics

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Abstract

This fall the first Tesla-style cryomodule cooldown test is being performed at Fermilab. Instrumentation department is preparing the electronics to handle the data from a set of wire position monitors (WPMs). For simulation purposes a prototype pipe with a WMP has been developed and built. The system is based on the measurement of signals induced in pickups by 320 MHz signal carried by a wire through the WPM. The wire is stretched along the pipe with a tensioning load of 9.07 kg. The WPM consists of four 50 Ω striplines spaced 90° apart. FPGA based digitizer scans the WPM and transmits the data to a PC via VME interface. The data acquisition is based on the PC running LabView.

In order to increase the accuracy and convenience of the measurements some modifications were required. The first is implementation of an average and decimation filter algorithm in the integrator operation in the FPGA. The second is the development of alternative tool for WPM measurements in the PC. The paper describes how these modifications were performed and test results of a new design.

Introduction

The last cryomodule generation has a single chain of seven WPMs (placed in critical positions: at each end, at the three posts and between the posts) to monitor a cold mass displacement during cooldown. The system was developed in Italy in collaboration with DESY [1-4]. Similar developments have taken place at Fermilab in the frame of cryomodules construction for SCRF research. This fall preliminary cryomodule cooldown test is being performed. In order to prepare an appropriate electronic system for the test a prototype pipe with a WMP has been developed and built, figure 1. The system is based on the measurement of signals induced in pickups by 320 MHz signal carried by a wire through the WPM. The 0.5 mm diameter Cu wire is stretched along the pipe with a tensioning load of 9.07 kg and has a length of 1.1 m. The WPM consists of four 50 Ω striplines spaced 90° apart. An FPGA based digitizer collects the WPM data and transmits it to the

VME controller. The VME front-end processes the raw data to calculate positions and perform FFT. It is also provides the raw data to LabView running on a PC upon request.

In order to increase the accuracy and convenience of the measurements some modifications were required. The first is connected with realization of average and decimation filter algorithm in the integrator operation in the FPGA. The second is connected with development of alternative tool for WPM measurements in the PC. We will discuss how these modifications were performed and test results of a new design.



Figure 1: The prototype pipe with a WPM.

Modification of the FPGA Design

The integrator consists of an accumulator, a fifo and a state machine, which performs the general operation of the integrator. The operation principle of the integrator was the following. The accumulator read the input flux of data. When it gathered the required number of samples, it was being stopped and was transmitting the result to the fifo. Then it was making reset, was being switched on again and was repeating the procedure. The general number of such cycles was defined by the number of averaging. The thing was that we were loosing several samples during the time slots when accumulator didn't work. The design also exhibited glitches which were believed to be due to the asynchronous nature of the accumulator reset. A new design was implemented which does not reset the accumulator.



Figure 2: A block diagram of the integrator

The operation principle of the new algorithm is the following, figure 2. Instead of shutting down and being switched on again during every cycle the accumulator works in continuous mode. We introduce several new variables, which are called registerValue, LastValue and NewValue. In the beginning the LastValue is equal to zero. Every time when the accumulator gathers the required number of samples, it puts the sum to registerValue. Then NewValue is equal to registerValue minus LastValue. Then we save NewValue, i.e. the sum in the past cycle, in RAM. And finally, LastValue is equal to registerValue. Doing in this way we take all samples into account.

The appropriate VHDL code has been modified and loaded into the board. The testing showed the system works correctly.

Development of the LabView design

Another problem occurred in the VME controller. Its primary function is to gather the raw data



Figure 3: A block diagram of the VME controller.

from the FPGA for storing and then to perform FFT and position calculations, figure 3. For ease of testing and diagnostics, it was necessary to develop an alternative tool to gather the raw data and perform FFT and position calculations just inside the PC. To this end, Labview code was developed to provide system diagnostics and cross-check the front-end data.

The operation principle of the LabView design is the following. The program takes the raw data from the old and performs FFT. Beside this, it performs demodulation according to the following formulas:

$$D_x = \frac{V_R - V_L}{V_R + V_L},\tag{1}$$

$$D_y = \frac{V_U - V_D}{V_U + V_D},\tag{2}$$

where $V_{\rm R}$, $V_{\rm L}$, $V_{\rm U}$, $V_{\rm D}$ are the signals form right, left, up and down electrode correspondingly. Then, the position characteristic is mapped by a 2D polynomial:

$$x[mm] = 6.61995D_{x} + 0.0246297y^{2}D_{x} + 0.000227912y^{4}D_{x} - 0.00000327286y^{6}D_{x} + 3.29058D_{x}^{3} + 0.0831568y^{2}D_{x}^{3} + 0.00262332y^{4}D_{x}^{3} + 0.0000272008y^{6}D_{x}^{3} - (3) 4.28734D_{x}^{5} - 0.150491y^{2}D_{x}^{5} + 0.00557827y^{4}D_{x}^{5} - 0.0000507939y^{6}D_{x}^{5} + 5.5398D_{x}^{7} + 0.143012y^{2}D_{x}^{7} - 0.00272022y^{4}D_{x}^{7} + 0.0000257823y^{6}D_{x}^{7}$$

The expression for y is the same, with substitute $y \rightarrow x$ and vice versa. The first column is a 1D 7th order polynomial fit, assuming no vertical displacement of the wire (y = 0 mm). To completely correct for non-linearities, the program takes the 2D polynomial, and applies a little routine: 1. sets y = 0 mm

2. computes x using (1)

3. computes *y* (same polynomial) using (2) and *x* in mm from step 2.

- 4. computes x using (1) and y in mm from step 3.
- 5. iterates steps 3 and 4 until a small error (≤ 10 um) is reached.

The results of the calculations are delivered on the screen as well as raw measurements.

New operation mode has been added. In FFT (1) mode the system performs FFT of the first four channels. In FFT (2) mode it performs FFT of the second four channels. It allows to analyze raw data from the test signal source and the WPM separately. In FFT (3) mode it performs FFT of the demodulated signals D_x and D_y as intermediate calculations. And finally, in FFT (position) mode it performs FFT of the actual position of the wire in vertical and horizontal planes. It allows to see wire oscillation harmonics and measure wire displacement in the most accurate way. Additionally the program calculates mean value and standard deviation of the position in each plane. The results of the program operation are in complete accordance with the front-end measurements.

Testing and operation of WPM

The first testing consisted of a long term (up to 72 hours) WPM measurements. The wire was kept in equilibrium and no signal was given to the tests channels. The first four (0-3) channels were connected to the WPM, the other four (4-7) were connected to the test signal source. Correspondingly, the program calculated two (*x*, *y*) test positions and two actual wire positions. Then the channels were changed: the first four channels (0-3) were connected to the test signal source, the others (4-7) were connected to the WPM. In each case all the boards showed stable level of signals, figure 4. The results of standard deviation calculations (σ_x , σ_y) are presented in table 1. The ratio of voltage levels between test and WPM channels N = 4 due to different amplification. Correspondingly, the ratio of standard deviations is $\sqrt{N} = 2$. The resolution of the system is ~ 1 um.



Figure 4: Example of position measurements (board #4, 08/25/09-08/26/09). Signals (0) and (1) are actual wire position, (2) and (3) are test position.

board	test signal (0-3, 4-7)				wire position (0-3, 4-7)			
#	$\sigma_{ m x}$, um	$\sigma_{ m y}$, um	$\sigma_{ m x}$, um	$\sigma_{ m y}$, um	$\sigma_{ m x}$, um	$\sigma_{ m y}$, um	$\sigma_{ m x}$, um	$\sigma_{ m y}$, um
1	0,45	0,57	0,66	0,50	0,29	0,24	0,27	0,31
2	4,93	2,50	2,27	2,34	0,98	1,21	2,01	8,13
3	1,43	1,61	4,32	3,06	1,26	0,98	0,58	0,67
4	1,17	1,31	1,23	2,70	1,02	0,44	4,17	7,97

Table 1: Standard deviations of the wire position and test signal for all the boards.

In some cases there were significantly large standard deviations of the WMP signals, figure 5. At the same time the test source channels didn't change. The actual reason these for this is unknown at the moment. Though, we believe it to be connected with a power supply issue for the amplifiers.



Figure 5: Example of position measurements (board #2, 08/24/09-08/25/09). Signals (0) and (1) are test position, (2) and (3) are actual wire position. It is clearly seen the dip in wire position measurements.

The second testing was the respond to a periodic mechanical excitation of the system. The wire proper oscillations are calculated from the vibration string equation:

$$f_n = \frac{n}{2l} \sqrt{\frac{F}{\rho A}},\tag{4}$$

where l = 1.1 m - length of the wire, F = 9.07 kg - tension load, $\rho = 8.41 \frac{\text{g}}{\text{cm}^3}$ - density of Cu, $A = \frac{\pi d^2}{4}$ - cross section of the wire, d = 0.05 cm - diameter of the wire and n - number of harmonic.Submitting all the values to (4) we receive:

(5)



$$f_n = n \cdot 104.5 \, \text{Hz}$$





Figure 7: Example of FFT measurements (log scale, board #2, 09/03/09). The red and green channels are connected to the WPM. It is clearly seen the first wire harmonic around 104.5 Hz and the second around 209 Hz (red and green). No signal observed in test channels (yellow and blue).

We strike the table with experimental equipment several times and measured the changes in wire position. The channels connected to WPM showed increasing of amplitude of wire oscillations, figure 6. At the same time, FFT measurements were performed, figure 7. The latter were scaled in decibels (dB), where 0 dB corresponds to wire deviation of 1 um, 20 dB corresponds to 10 um, -20 dB corresponds to 100 nm and so on. In equilibrium the noise of FFT level is below -20 dB, so it actually defines the resolution of the system, which is ~ 100 nm. The first and the second wire proper oscillation harmonics are clearly seen on the screen around 104.5 Hz and 209 Hz correspondingly. The first peak corresponds to wire deviation of about 10 um, which is clearly seen on position measurements. The peaks position is in complete accordance with theory. Besides, many additional harmonics present due to mechanical vibrations of the different parts of the armature.

Conclusions

Average and decimation filter algorithm in FPGA has been successfully implemented. It allows to take all samples into account and provides a glitch free implementation of the integrator operation.

LabView design for WPM measurements has been developed. It provides another powerful tool for WPM operation and diagnostics and presents a good cross check for the front-end measurements.

Concurrent testing of all the boards is performing shortly. Preliminary testing of the whole system will be the final step before the real cool down diagnostics is being performed.

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