Development of a Fluxless Flip Chip Bonding Process for Optical Military Electronics

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Abstract

As military electronics tend to become lighter, smaller, thinner, and lower cost, the use of flip chip technology is becoming more common place to meet system requirements, yet survive environments. This paper explores the development of an optical flip chip application and details the selection/qualification of the substrate. The selected assembly consists of a procured 1x12 Vertical Cavity Surface Emitting Laser (VCSEL) die, having 80um diameter eutectic AuSn solder bumps at 250um pitch and flip chip bonded to a .006" thick 99.6% alumina substrate with .006" diameter thru holes and metallized with 500Å WTi, under minimum 2.0-3.0µm (80-120µ") thin film deposited Au. An 8 run, 3 factor, 2 level Full Factorial Design of Experiments (DOE) was completed on procured detector arrays and procured ceramic substrates using the Suss Microtec FC150. The optimum settings for the peak temperature, peak time and final die z-height were selected using the ANOVA results and interaction plots. Additional studies were completed to qualify in-house produced substrates. An epoxy glob-top encapsulant was selected to dissipate stress on the flip chip solder joints and to enhance thermal shock performance.

Keywords: Flip Chip, DOE, Optical

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Background:

The design used by the Telemetry Group at the National Nuclear Security Administration's (NNSA) Kansas City Plant was historically based on a chip on board wire bonded design. In order to meet customer and the ever increasing size reduction system requirements, the use of flip chip interconnection was investigated. The function of the Miniature Mechanical Transfer Assembly (MMTOA) (Patent Pending, SN11/690,495, filed 3/16/07) VCSEL array die/substrate flip chip fiber optic assembly is to transmit focused light from the die into a MT (mechanical transfer) fiber connector (see Figures 1 and 2).

Figure 1

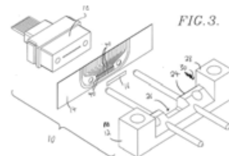

Figure 2

The MMTOA allows for a passive alignment of the fiber vs an active alignment system. This allows for the MMTOA to become a plug and play device. The VCSEL array is powered from a next assembly printed circuit board. A similar die/substrate flip chip assembly is also used in the Next Level Assembly and functions as a detector for transmitted light in a sensor application.

The completed assembly consists of a procured 1x12 VCSEL die having 0.124" x 0.0177" x 0.004" dimensions, 60um diameter eutectic AuSn solder bumps at 250um pitch flip chip bonded to a 0.620" x 0.147" x 0.006" 99.6% alumina substrate with .006" diameter thru holes and metallized with 500Å WTi, under minimum 2.0-3.0µm (80-120µ") thin film deposited Au. A corresponding assembly uses a detector die with the same physical attributes. This substrate studied did not include the currently used polyimide solder mask. Following fluxless flip chip attach, a bead of procured one part epoxy glop-top encapsulant is dispensed along the perimeter of the die and cured using a two step cure process. The function of the highly thixotropic epoxy glop-top encapsulant is to enhance the mechanical integrality the flip chip attach and to improve the survivability in environments yet leaving the functions of the vcsel and detector unaffected by the absence of outgassing or flow out of the encapsulant. The MMTOA assembly is designed to withstand vibration and thermal environments in the range of -65C to +80C.

The top and side view of the flip chipped assembly before and after dispensing/cure of the encapsulant and are shown Figures 3 and 4:

Figure 3

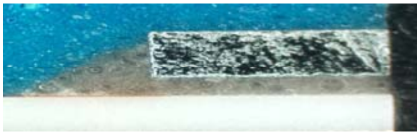

Figure 4

Prior to performing this study, the development effort used a .006" thick polyimide substrate with ½ oz. Cu traces under 118 uinches of electroless Ni and 4 uinches of immersion Au and the procured die discussed above**.** Early prototype field testing resulted in an electrical open circuit that was analyzed to be an intermittently connected flip chip solder bump(s). SEM analysis of the sheared die directly following flip chip bonding provided the insight to identify the root cause for these failures. See the 60X optical microscope view of the substrate and 500X SEM photo of the individual polyimide solder finger in Figures 5 and 6:

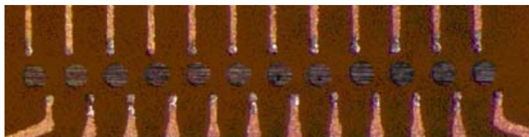

Figure 5

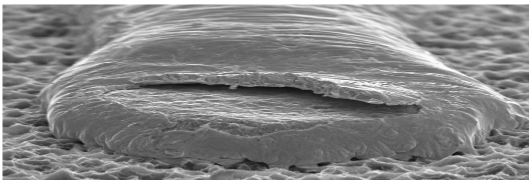

Figure 6

All polyimide substrates flip chip bonded at the optimum settings identified in the preceding study displayed the same failure mode at die shear. The failure always occurs within the solder at or near the substrate NiAu plating/AuSn solder interface with the die shear strength being approximately half of that measured as compared to the die shear strength on ceramic substrates (171g – 755g for the polyimide printed circuit vs 1256g – 1377g for the ceramic thin film metallized). One should note that a solder dam was absent from the design due to the registration capabilities of standard printed circuit board fabrication resulting in an inconsistent solder bump cross sectional area. One should also note that the Ni and Au plating thicknesses on the polyimide substrate had previously been optimized to enhance solderabilty. Hence, the basis to purse a different substrate/metal stack design.

Experimental Design:

Following screening experiments used to select main factors and test levels an 8 run, 3 factor, 2 level Full Factorial DOE was completed on procured ULM detector arrays and procured ceramic substrates using the Suss Microtec FC150. The input factors and levels consisted of the following:

	Low	**High**
Peak Temperature (substrate)	320C	330C
Time at Peak Temperature	15 sec	25 sec
Final Die z-Height (initial contact height = zero)	-5um	zero

The constants for the DOE were the 60 second ramp time to the peak temperature, a static force of 50g, the die was lowered -10 um from the initial contact die height for 5 seconds during the peak time, and raised to the final die height and the flip chip bonding was performed in forming gas atmosphere (97%N2/3% H2). The process map of the fluxless flip chip attach is shown in Figure 7.

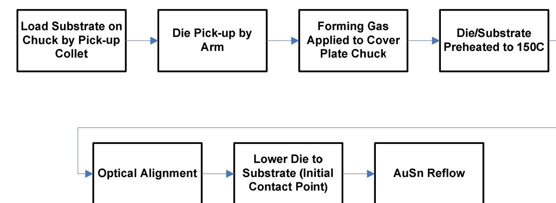

Figure 7

The response factor for the DOE was the average die shear of based on a sample size of four (due to cost constraints). Failure analysis was performed following die shear using an optical microscope and SEM with EDX to determine the interfacial failure mode(s).

The DOE run combinations following randomization can be broken down as shown in Table 1.

Table 1

Run Order	Peak Temp	Time at Peak	Final Die z-Height	Average Die Shear
1	320	25	0	1156
2	320	25	-5	1083
3	320	15	0	1046
4	335	25	0	1178
5	335	15	0	1377
6	335	15	-5	1164
7	320	15	-5	1138
8	335	25	-5	1146

The analysis of variance (ANOVA), calculated by Minitab v14, can be summarized as shown in Table 2.

Table 2

Factorial Fit: Average Die Shear versus Peak Temp, Final Die Height

Estimated Effects and Coefficients for Average Die Shear (coded units)

Term	Effect	Coef	SE Coef	T	P
Constant		1161.00	29.33	39.59	0.000
Peak Temp	110.50	55.25	29.33	1.88	0.133
Final Die Height	56.50	28.25	29.33	0.96	0.390
Peak Temp*Final Die Height	66.00	33.00	29.33	1.13	0.323

S = 82.9533 R-Sq = 58.94% R-Sq(adj) = 28.15%

Analysis of Variance for Average Die Shear (coded units)

Source	DF	Seq SS	Adj SS	Adj MS	F	P
Main Effects	2	30805	30805	15403	2.24	0.223
2-Way Interactions	1	8712	8712	8712	1.27	0.323
Residual Error	4	27525	27525	6881		
Pure Error	4	27525	27525	6881		
Total	7	67042				

Estimated Coefficients for Average Die Shear using data in uncoded units

Term	Coef
Constant	-2664.33
Peak Temp	11.7667
Final Die Height	-565.100
Peak Temp*Final Die Height	1.76000

The low Rsquared (adjusted) value seen in the ANOVA confirms that the die shear is robust to changes in the process inputs within the process window studied.

The main effect and interaction plots for the DOE are shown in Figures 8 and 9.

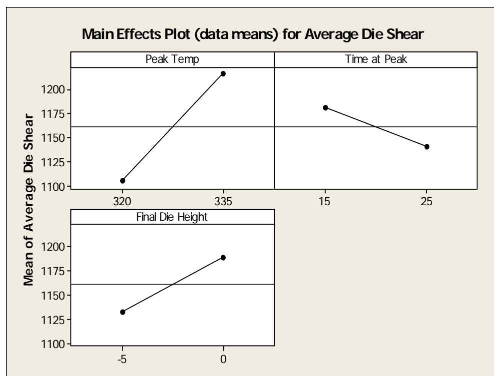

Figure 8

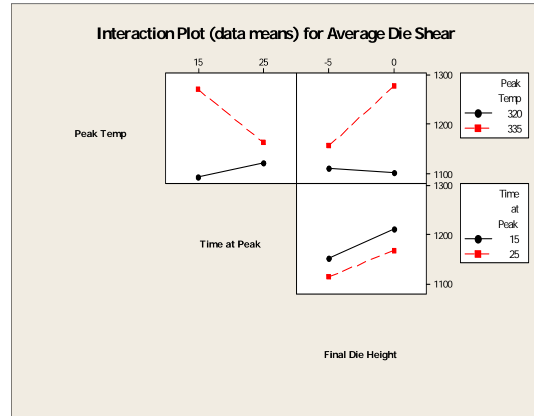

Figure 9

Based on the ANOVA, the factor "peak temperature" was identified as significant in terms of die shear strength. While examining the interaction plots, the interactions "peak temp x time at peak" and "peak temp x final die height" are of interest and support the optimum settings identified later in the report.

Based on the SEM photos and EDX area scans, the failure modes seen on all samples were either (1) mix of substrate thin film TiWAu metallization lifts and separation at the GaAs/Ti die interface or (2) 100% separation at the GaAs/Ti die interface. Since most of the sheared samples exhibited the (2) failure mode, the experiment was mainly a measure of how well the Ti was bonded to the GaAs die.

Optical and SEM photos of the sheared assembly at 60x and 500x magnification are shown in Figures 10 and 11.

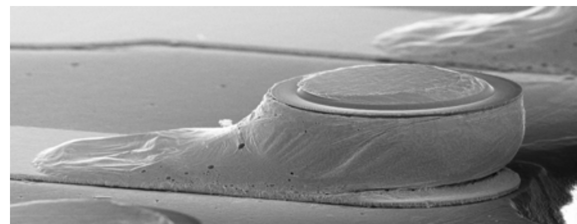

Figure 10

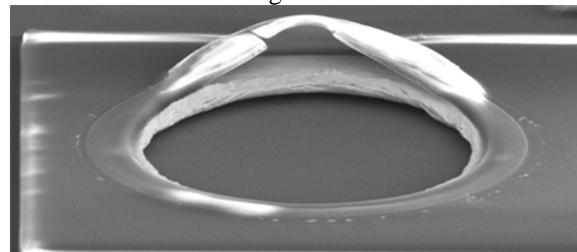

Figure 11

A follow-up DOE experiment, at the optimum settings, was performed to better characterize the effect of the final die z-height and investigate if this factor displayed a response output having curvature [1]. An additional run included flip chip bonding at 325/335C peak temperature for 15 seconds with the final die z-height at + 5um from the initial contact point. The greatest die shear strength was seen at a final die z-height of zero as given in Figure 12.

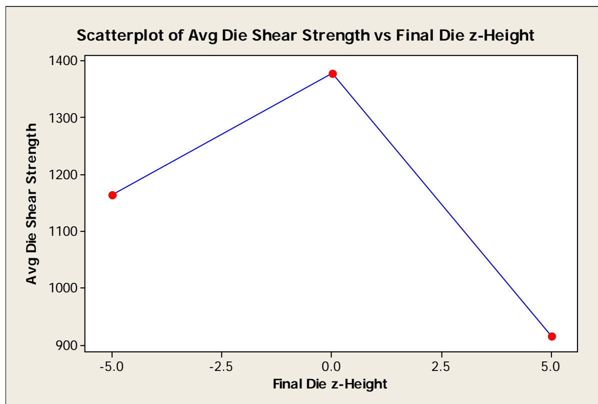

Figure 12

The optimum settings for the DOE performed on the procured ceramic substrates and detector die were identified as 325C die/335C substrate peak temperature, 15 seconds at peak temperature, and final die z-height of zero. An average of 1377 gm or 57gram/solder bump die shear and a standard deviation of 92g was achieved at the these settings. A graphic representation of the optimum process settings detailing the part time/temperature and die z-height profile over time is shown in Figure 13.

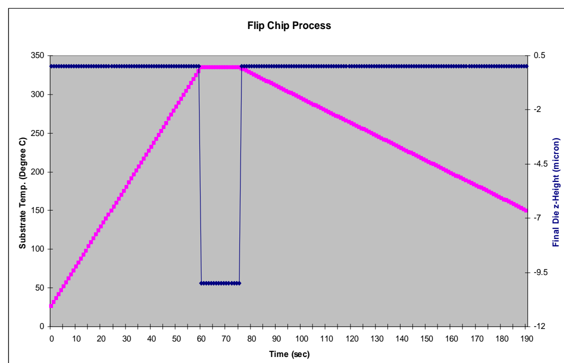

Figure 13

Conclusions:

The DOE factor level settings selected confirm the wide process window. Comparing the die shear strength/variance and the interfacial die shear failure mode on the ceramic substrate vs polyimide, the ceramic substrate was chosen as the preferred substrate choice for the application. The die shear strength variation and the interfacial die shear failure mode seen on the .006" polyimide printed circuit boards were determined to be unacceptable for production and the failure mode seen on the polyimide die shear samples was borne out during field testing. In addition, the polyimide circuit boards were found to flex during handling resulting in die/substrate bonding damage as seen in the lower die shear strengths further supporting the selection of ceramic substrate for the application [2].

Additional Process Development Summary for the Internal Substrate Qualification:

The internal produced alumina substrate that uses production qualified processes differs from the procured substrate in terms of the metallization stack. The internal substrate is fabricated using 2000ÅTi/3000ÅPd, under minimum 3.0-5.0µm electroplated Au. Initial bonding trails at the optimum settings determined above did not result in 100% wetting to the plated Au and electrical opens were seen during the initial electrical continuity testing. Die shear results ranged from 72g to 342g in these samples with the failure mode was mainly located within the solder at or near the substrate Au plating/AuSn solder interface. A significant difference was seen in terms of solder wetting when comparing the thin film deposited Au on the procured substrates versus Au plated deposition on the internal produced substrate. See the 60x magnification photos (Figure 14) following die shear below that illustrate the poor AuSn wetting to the substrate metallization.

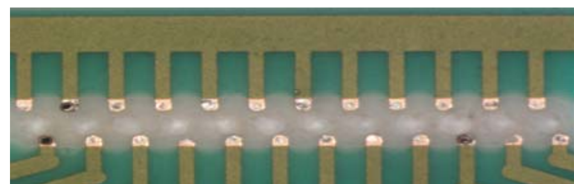

Figure 14

Based on prior experience with eutectic die attach processes, a 10um scrub was added during the 15 second peak temperature. The solder wetting was improved significantly but 5% – 10% of the substrate solder fingers exhibited less than 100% wetting (see the photo above). It was then thought that the solderability could be enhanced by lowering the die 15 more microns (from -10um to -25 microns). See the 60x magnification optical in Figure 15.

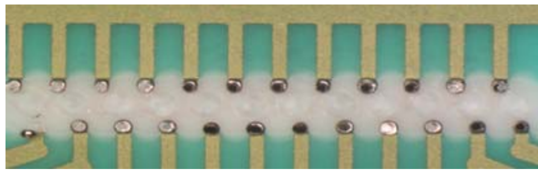

Figure 15

The solderabilty was found to be acceptable only when the die was lowered -25um from the initial contact point, 10 um scrub for 10 seconds and that the scrubbing occurred while the die was being lowered in the z-direction to -25um from the initial contact point. The corresponding die shear average and standard deviation using this new process was 913g and 108g respectively and the failure mode was shifted to the GaAs/Ti die interface. In summary, the combination of the scrubbing the die and lowering the die further from the initial contact point was required to duplicate the solderability results seen on the procured thin film metallized Au substrate.

The cross sections showing the flip chip bonded die to the internally produced substrate are shown in Figures 16 and 17.

Figure 16

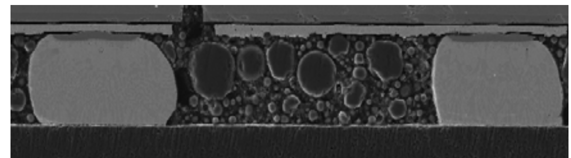

Figure 17

References

[1] John H. Lau, Flip Chip Technologies, McGraw-Hill Companies, Chapter 3, p. 133, 1996

[2] Ken Gilleo, Area Array Packaging Handbook, McGraw-Hill Companies, Chapter 7, p. 7.30, 2002