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Epitaxial Thin Film Silicon Solar Cells Fabricated by Hot Wire Chemical Vapor Deposition Below 750ºC

Preprint

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ABSTRACT

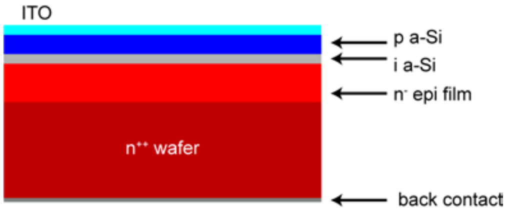
We report the fabrication of film c-Si solar cells on Si wafer templates by hot wire chemical vapor deposition. These devices, grown at glass-compatible temperatures below 750° C, demonstrate open-circuit voltages greater than 500 mV and efficiencies above 5%. Analysis of the device characteristics and quantum efficiency provides important information about the epitaxial c-Si absorber material quality as a function of growth temperature.

INTRODUCTION

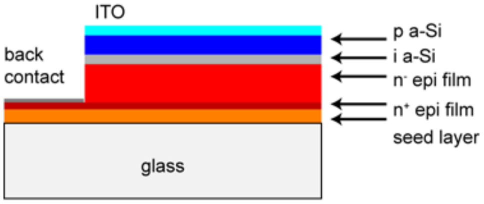
Film crystal silicon solar cells produce energy at much lower costs than Si wafer-based photovoltaics due to reduced material and energy consumption. We are working to grow silicon films epitaxially on crystalline seed layers affixed to inexpensive foreign substrates [1-3]. Through the integration of light trapping schemes, cells with 2-10 μm absorber layers could realistically display efficiencies above 15%. Such efficiencies will require growth of high quality absorber layers on substrates that are constrained to low temperatures compared with those used in conventional c-Si epitaxy. Thus, the development of a scalable, low-T high-quality epitaxial silicon growth technique is critical. Here we report on the realization of single crystalline thin film Si solar cells with efficiencies over 5%, grown on Si wafer templates by hot wire chemical vapor deposition (HWCVD) at glass compatible temperatures ≤ 750°C. Our results yield a consistent picture of the relationship between the absorber material quality and device performance and suggest means of improvement.

EXPERIMENTAL

Hot wire chemical vapor deposition is a scalable approach to low temperature Si epitaxy that has been shown to produce c-Si layers with controlled dopant concentrations and majority carrier mobilities that are nearly equal to those of bulk crystalline material [4]. The simple reactor design and high deposition rates (almost 300 nm/min has been demonstrated), make HWCVD an economical route to film c-Si production. In order to demonstrate the feasibility of growing high quality c-Si films at display-glass compatible temperatures (620 - 750°C), our initial efforts have focused on assessing the performance of devices fabricated on heavily-doped (100) single crystal wafer templates. Cells consisting of a 2 μm epitaxial n-type (10^{16} cm^{-3} P) base layer were fabricated on an electronically dead (10^{19} cm^{-3} As) n^{++} wafer and finished with a hydrogenated amorphous Si heterojunction, as displayed in Fig. 1. The area of each device was 0.05 cm^2, so no metal front grid was used. The substrate temperatures, T_{sub}, for the growth of the epitaxial layer ranged from 650°C to 750°C, and no post-deposition hydrogenation or annealing treatments were applied to these devices. There is no intentional texturing or other light-trapping structure.



Device on Wafer Template



Device on Seed-on-Glass

Fig. 1. Device structures for n^- epitaxial thin film c-Si cells fabricated on heavily-doped Si wafer and seed-on-glass substrates.

RESULTS AND DISCUSSION

Representative current-voltage (J-V) characteristics for two cells, one grown at 655°C and one at 710°C, are displayed in Fig. 2. Both the open circuit voltage (V_{OC}) and short circuit current (J_{SC}) exhibit enhancement with an increase in T_{sub}, indicating an improvement in the absorber crystalline quality. In fact, these results (V_{OC} = 0.51 V, efficiency = 5.11%), demonstrate that the quality of

HWCVD films is competitive with other epitaxial technologies [5].

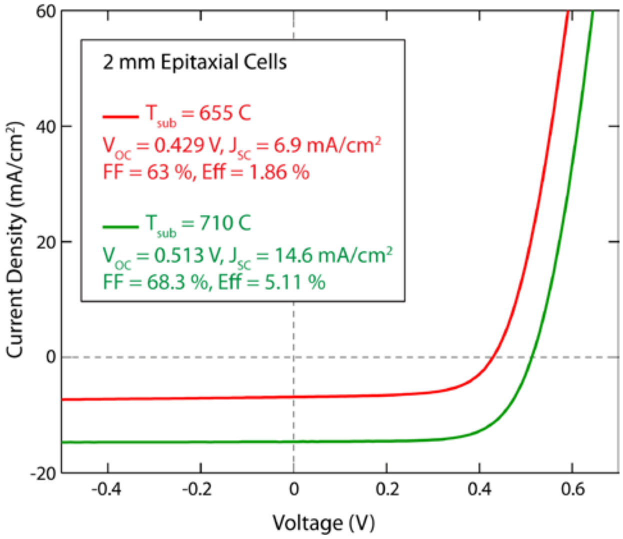


Fig. 2. Current-voltage characteristics for devices grown on Si wafer substrates at 710° C (green) and 655° C (red).

Internal quantum efficiency (IQE) measurements, displayed in Fig. 3 for the same cells, provide additional insight into the absorber quality. The cell grown at 710° C demonstrates up to 70% conversion of photons in the 500-800 nm range. Furthermore, the relatively high IQE in the 600-1000 nm range compared to that expected from a 2 μm cell of ideal material quality (no light trapping) suggests that most of the carriers generated at the back of the absorber are collected. We note here that in this device configuration it is possible to collect up to a 1 mA/cm^2 of current from the heavily-doped wafer substrate, however some degree of unintentional light trapping from a rough back interface is conceivable as well. Analysis [6] of the inverse IQE vs absorption depth (1/α) yields an effective diffusion length, L_{eff}, of roughly 7 μm, which is more than three times the absorber thickness. In comparison, the device grown at 655° C exhibits lower IQE at all wavelengths, and the calculated L_{eff} =1.5 μm is less than the absorber thickness.

The performance of these cells is consistent with the material quality ascertained by other means. Average lifetime values of approximately 10 ns were determined by microwave photoconductive decay in identically grown 40 μm films. The measured device J-V parameters are also reproduced in PC1D simulations using nanosecond minority carrier lifetimes in the absorber layer. Considering the significant number of extended defects observed in these films by optical microscopy, post-growth rapid thermal annealing and hydrogenation steps are expected to substantially enhance the device performance. Enlargement of the cell area and the addition of a front metal grid should also improve the fill factor.

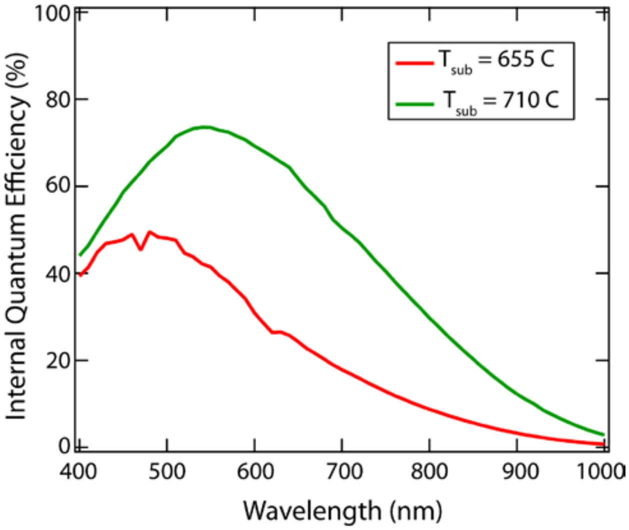


Fig. 3. Internal quantum efficiency spectra for devices grown on Si wafer substrates at 710° C (green) and 655° C (red).

While we have made significant progress in the fabrication of low-temperature epitaxial materials on single crystalline substrates, the transfer of an optimized HWCVD epitaxial growth routine to the deposition of c-Si on a seed layer is the true test of this technology. We have fabricated our first device on a layer-transferred Si-on-glass substrate, the structure of which is also shown in Fig. 1. In this configuration, the back contact was made by etching down to an n$^+$ epi layer (10^{18} cm^{-3} P) after all of the layers were deposited. The total absorber thickness including the n$^+$ and n$^-$ epitaxial c-Si layers was approximately 5 μm. Current-voltage characteristics for this cell are displayed in Fig. 4. The low V_{OC} = 0.22 V indicates that the absorber material quality did not approach that grown on Si wafers and is most likely limited by the lower temperature required to accommodate the glass substrate as well as the rough surface of the Si template. Overall, the device demonstrated an efficiency of 0.42 %. We anticipate significant improvement, however, with optimization of the cell structure and growth conditions.

CONCLUSIONS

In summary, thin film c-Si solar cells grown by HWCVD show promise as an inexpensive alternative to wafer-based PV. Model devices fabricated on Si wafer templates at glass-compatible growth temperatures demonstrate open circuit voltages above 0.5V and efficiencies greater than 5%. Initial devices were also demonstrated on seed-on-glass substrates. Post-deposition treatments are expected to lead to significant improvement in cell performance, as the epitaxial absorber material quality is constrained by the glass-compatible deposition temperatures.

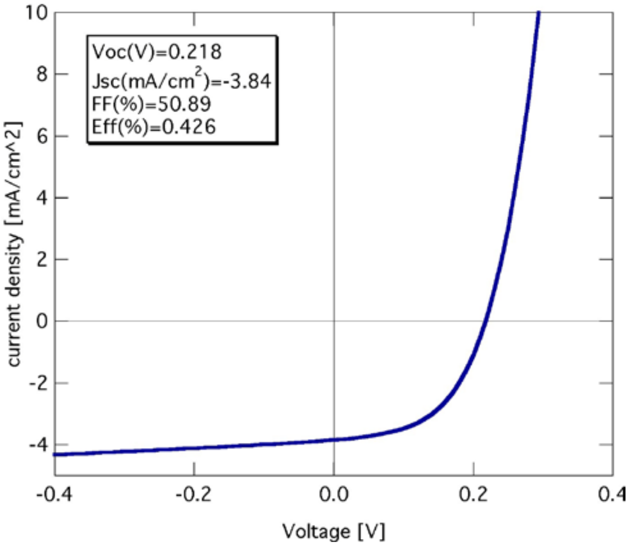


Fig. 4. Current-voltage characteristics for a 0.05 cm^2 device grown on a seed-on-glass substrate (see Fig. 1 for cell structure).

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We report the fabrication of film c-Si solar cells on Si wafer templates by hot wire chemical vapor deposition. These devices, grown at glass-compatible temperatures < 750°C, demonstrate open-circuit voltages > 500 mV and efficiencies upward of 5%. Analysis of the device characteristics and quantum efficiency provides important information about the epitaxial c-Si absorber material quality as a function of growth temperature.

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