Design and Fabrication of a Radiation-Hard 500-MHz Digitizer Using Deep Submicron Technology

K.K. Gan[*], M.O. Johnson, R.D. Kass, J. Moore
Department of Physics, The Ohio State University

S. Smith
Stanford Linear Accelerator Center

Project Summary

The proposed International Linear Collider (ILC) will use tens of thousands of beam position monitors (BPMs) for precise beam alignment. The signal from each BPM is digitized and processed for feedback control. We proposed the development of an 11-bit (effective) digitizer with 500 MHz bandwidth and 2 G samples/s. The digitizer was somewhat beyond the state-of-the-art. Moreover we planned to design the digitizer chip using the deep-submicron technology with custom transistors that had proven to be very radiation hard (up to at least 60 Mrad). The design mitigated the need for costly shielding and long cables while providing ready access to the electronics for testing and maintenance. In FY06 as we prepared to submit a chip with test circuits and a partial ADC circuit we found that IBM had changed the availability of our chosen IC fabrication process (IBM 6HP SiGe BiCMOS), making it unaffordable for us, at roughly 3 times the previous price. This prompted us to change our design to the IBM 5HPE process with 0.35 μm feature size. We requested funding for FY07 to continue the design work and submit the first prototype chip. Unfortunately, the funding was not continued and we will summarize below the work accomplished so far.

Design of the Digitizer

We proposed a 12-bit pipelined digitizer as shown in Fig. 1. In this scheme the input is crudely digitized in the first stage (3-bit cell). The digitized value is then subtracted from the sampled input value, amplified by eight and presented to the second stage. This identical process is repeated for each of the four stages. A one-bit comparator follows the last stage so the final result can be rounded to 12 bits.

The 12-bit digitizer is somewhat beyond the state-of-the-art. However, there is one characteristic of the BPM that may ease the design requirements. The input from each bunch to this system is a sequence of doublets. The digitizer is designed for a bunch spacing of 1.4 ns. The bunch spacing is expected to be somewhat larger for the dumping rings of the ILC and this will improve the feasibility of the project. Only one parameter is needed to completely specify a doublet. Thus the requirements could be met with a digitizer sampling at the bunch frequency (1/1.4ns or 714 MHz). By interleaving three digitizers, we can have a chip with 2 G samples/s to provide more redundancy.

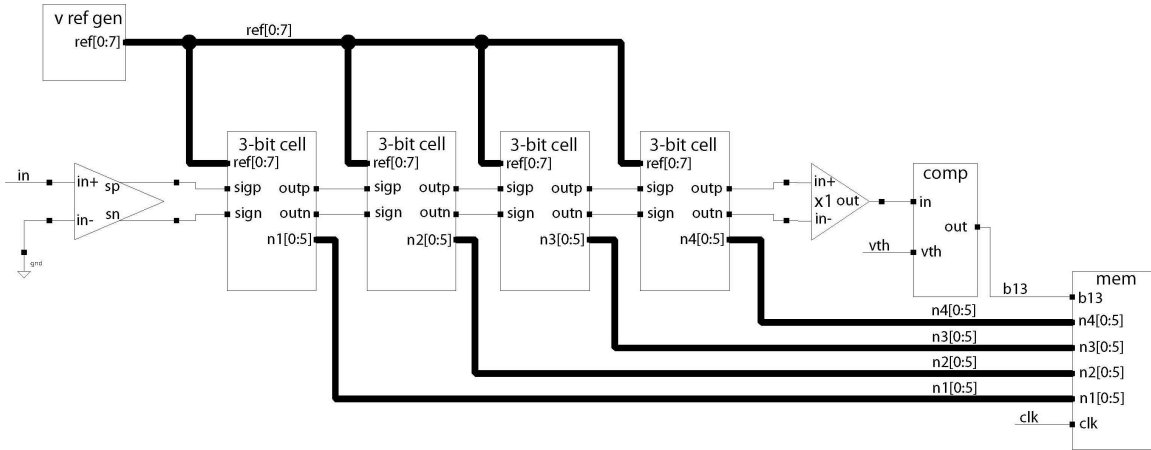[*] Contact: K.K. Gan, 614-292-4124, gan@mps.ohio-state.edu

Figure 1. Schematic of a 12-bit pipelined digitizer.

In FY06 as we prepared to submit a chip with test circuits and a partial ADC circuit we found that IBM had changed the availability of our chosen IC fabrication process (IBM 6HP SiGe BiCMOS), making it unaffordable for us, at roughly 3 times the previous price. This prompted us to change our design to the IBM 5HPE process, with 0.35 μm features rather than the 0.25 μm of the 6HP.

Unfortunately, changing processes was not a trivial matter. Our design used enclosed layout transistors with guard rings for radiation hardness, which were not a standard IBM part. On our last chip design project we were able to use component libraries and Cadence rules files developed at LBNL, CERN, and Rutherford, but these libraries were not available for the BiCMOS process we had chosen for this ADC. We implemented parameterized cells (PCELLs) for the transistors (radiation-hard circular gate MOSFET's) and re-written the Cadence rules files to enable them to be laid out and extracted. We also had to change the sizes of all transistors in all circuits to suit the larger feature size of the new process and did some redesign to accommodate the larger feature sizes.

A major difficulty we encountered in the redesign was that the amplifier used in the sample-and-hold circuit designed in the 6HP process was not fast enough in the 5HPE process. We spent significant effort designing a faster amplifier in the new process.

We completed a layout in the 5HPE process for a chip containing all the elements for a 3-bit block of the ADC shown in Fig. 2. The required bias generators to run the chip were also designed. A picture of the chip is shown in Fig. 3. Many internal points were brought out to pads so we could test the circuits individually. For example, the output of the sample-and-hold was brought out as were the seven comparator outputs. In simulations from the schematic and from extracted layouts, the comparators and the decoder circuit were all fast enough to run at the desired clock frequency (714 MHz = 1/1.4 ns), but more refinement of the amplifier was still needed.
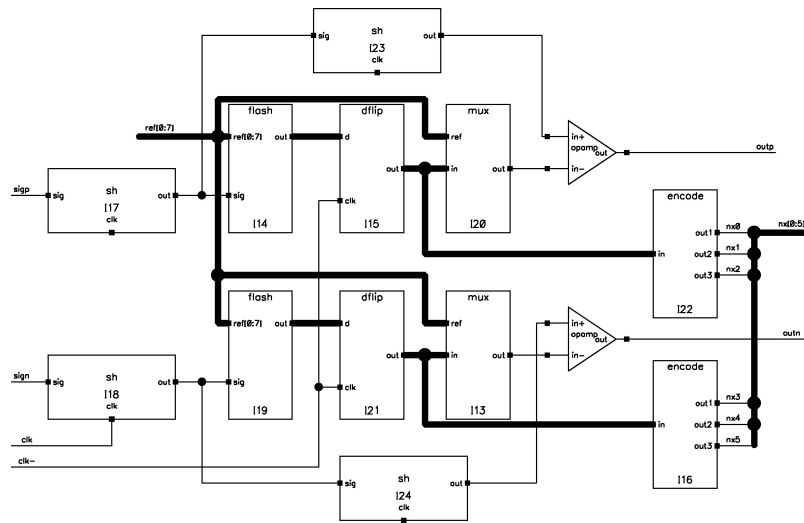
Figure 2. Schematic of a 3-bit cell.

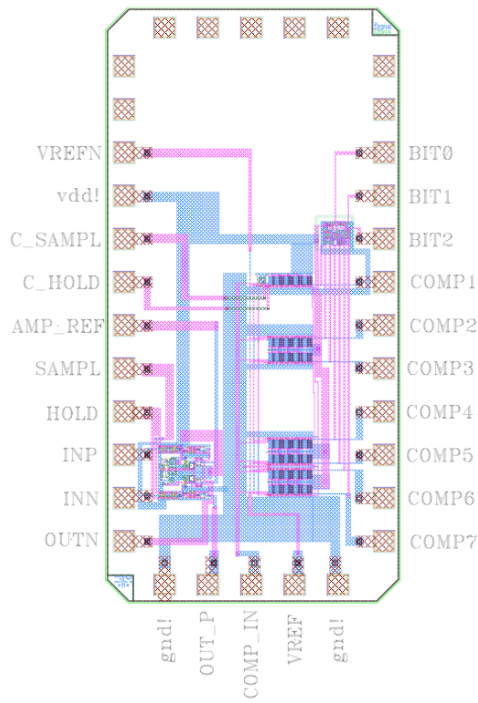Our plan was to submit the chip for fabrication in 2007 but the project was not funded and hence no chip was submitted.

Figure 3. Picture of a 3-bit cell.