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# Development of Standardized Power Electronic Components, Sub-systems and Systems for Increased Modularity and Scalability

S. Chakraborty, C. Pink, J. Price and B. Kroposki
*National Renewable Energy Laboratory*

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*Coal Creek Design*

***Technical Report***
**NREL/TP-581-42482**
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Prepared under Task No. DPE6.1000

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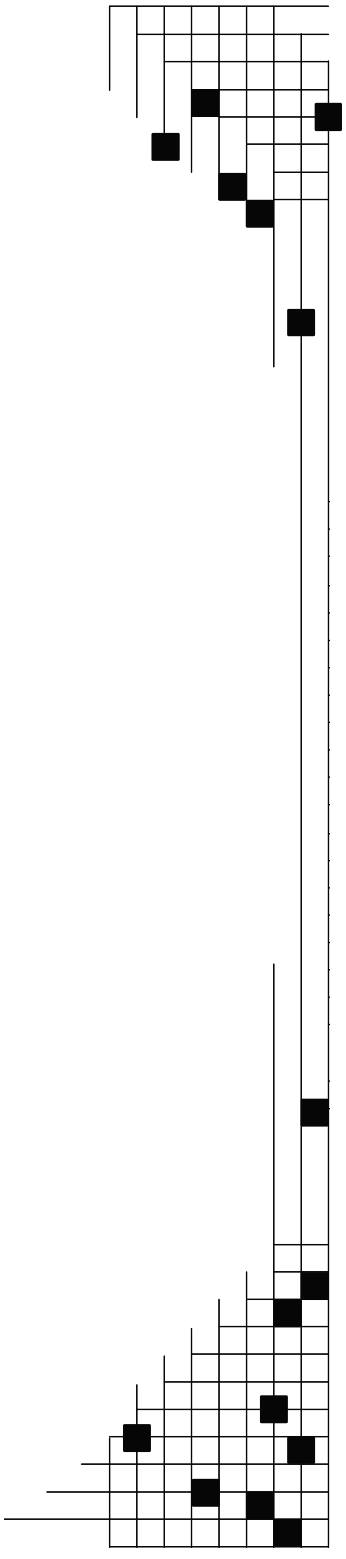

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## Acronyms

| | |
|---|---|
| AC | alternating current |
| A/D | analog to digital |
| APEI | advanced power electronics interface |
| CAN | controller area network |
| CPU | central processing unit |
| CT | current transformer |
| DC | direct current |
| DSP | digital signal processing |
| HMI | human machine interface |
| IC | internal combustion |
| IEEE | Institute of Electrical and Electronics Engineers |
| IGBT | insulated-gate bipolar transistor |
| IPEM | Integrated Power Electronics Module |
| JTAG | Joint Test Action Group |
| NREL | National Renewable Energy Laboratory |
| PEBB | power electronics building block |
| PI | proportional integral |
| PSCAD | Power Systems Computer Aided Design |
| PV | photovoltaic |
| PWM | pulse-width modulation |
| RAM | random access memory |
| RMS | root mean square |
| SKAI | Semikron Advanced Integration |
| SRAM | static random access memory |
| THD | total harmonic distortion |
| VAR | volt-amperes reactive |

# 1 Introduction

Power electronics devices hold substantial promise for making distributed energy applications more efficient and cost effective. There is a need to develop advanced power electronics interfaces for the distributed applications with increased functionality (such as improved power quality, voltage/volt-amperes reactive (VAR) support), compatibility (such as reduced distributed energy fault contributions), and flexibility (such as operation with various distributed energy sources) while reducing overall interconnection costs. This project is motivated towards developing and testing inverters that will allow distributed energy systems to provide ancillary services such as voltage and VAR regulation, and increased grid reliability by seamlessly transitioning between grid-tied and stand-alone operation modes.

The objectives of this work are to identify system integration and optimization issues and technologies and to provide solutions through research, analysis, and testing of power electronic interfaces for distributed energy applications that are cost-competitive and have substantially faster response times than conventional technologies. In addition, the testing of power electronics interfaces will develop a technical basis for performance assessment for distributed energy systems, subsystems, and components that will finally create a foundation for standardized measurements and test procedures. The ultimate goal for this research is to advance the potential benefits of distributed energy to provide ancillary services, enhance power system reliability, and allow customer choice. Proper integration of distributed energy power electronic interfaces will: (1) improve the overall system dependability while providing varying reliability levels to meet individual customer needs; (2) reduce price volatility through better management of peak demand; (3) enhance the resiliency of the system against energy supply disruptions; and (4) reduce vulnerabilities by enabling safe "islanding" of critical infrastructure for faster restoration of service.

In an effort to promote advanced functionality of power electronic interfaces for utility connected distributed and renewable energy systems, the National Renewable Energy Laboratory (NREL) is building a generic inverter platform based on insulated-gate bipolar transistors (IGBT) as the power electronic switching devices. The platform's use will depend on its specific application, but generally it will be used to evaluate the performance of new controls and protection algorithms as related to utility connected inverter. To ensure flexibility, the inverter is built around a digital signal processor (DSP) control system that can be reprogrammed to suit a variety of objectives, which may include implementation of more optimized controls and experimentation with advanced utility connected power delivery and protection functions.

A simulation model is being developed in parallel with the construction of the inverter platform. The model provides a test and development platform for control methodologies of the various functions that the inverter will be designed to perform. The basic circuit operations and the more advanced design objectives will be worked out in the model before they are implemented in the actual hardware. This approach provides many benefits including the reduced risk of equipment damage. Furthermore, once the model is validated to reflect actual hardware operations, it can be used to design, test, and implement other functions relative to the inverter platform.

In Section 2, the design of the inverter model is described and interesting results on the operation of the inverter are presented. The circuit model for the inverter was developed in PSCAD [1]. The PSCAD modeling environment is well-suited for the evaluation of power system level transient dynamics, but because of its limited capability to model power electronic circuits, it is not ideally suited for this type of modeling. Nevertheless, it was chosen because it is a very useful tool available for utility system connected power electronics studies. In the future, MATLAB/Simulink models will be able to link with PSCAD to supplement the capabilities of the existing model. The circuit model is used initially to aid in developing the control strategy and circuit operations of the inverter platform. Later, more advanced control schemes and algorithms will be developed and validated prior to implementation on the hardware platform.

In Section 3, the hardware design of the inverter platform is described. The power circuit of the inverter platform consists of a Semikron integrated power electronics module (IPEM) along with sensors, auxiliary power supplies, and relays. At this initial phase of development, a California Instruments alternating current (AC) electronic load is used for testing. A Sorensen direct current (DC) power supply is used as the input of the inverter, but in the future this DC supply can be replaced by the distributed energy sources with associated converters. In addition to the power circuit, inverter control is designed with the Spectrum Digital eZdsp$^{TM}$ F2812 evaluation module. This module contains the TMS320F2812 DSP by Texas Instruments. There are three significant parts in the control design. Along with the DSP board, interface between both the control board and the hardware setup and the control board and the higher level central processing unit (CPU) based controller are part of control design. And the final component of control design is the development of software codes both for the local DSP controller and for the higher level CPU based controller. The initial results showing the voltage and current control of the inverter platform are also given in this section.

In Section 4, the concept of modularity is discussed in order to understand the potential of scalable, flexible designs. Present power electronics topologies are discussed that can be used with different DE sources with little or no modifications. In addition to that, the future requirements for standardization of the power flow and signal distribution network, which in turn allows for open architecture distributed controller approach, are also discussed in this section. Modularity, flexibility, and standardization will, in the future, lead to application software that is independent of the hardware specifications of power stage. This will lead to products from different vendors that can communicate and work with each other as long they support the standardized interfaces between control levels.

# 2 Inverter Model

An inverter is a power electronic-based device that converts DC power to AC power. Feeding AC loads from DC sources is an integral part of distributed energy systems. A circuit schematic for the inverter is shown below in Figure 2-1.

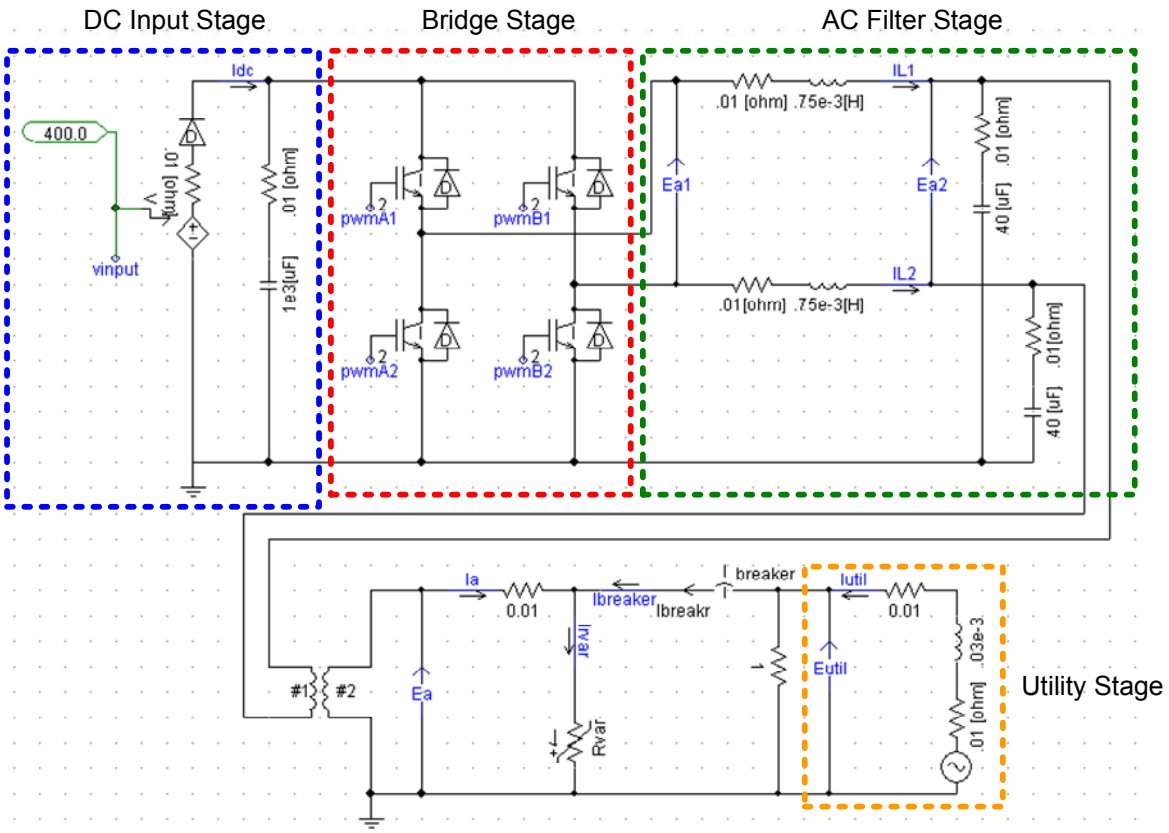


**Figure 2-1 Inverter Circuit Schematic (in PSCAD)**

## 2.1 Power Circuit Components

The inverter circuit converts a DC input (as would commonly be from a distributed energy source after proper conditioning) into a grid-suitable AC output. The DC input voltage is nominally 400 V ± 5%. Conversion is done by a power electronics bridge circuit that operates to produce a pulse-width modulation (PWM) AC output, which for this model will be nominally 120 V AC. To allow a seamless transition between utility connected mode and stand-alone mode, the inverter must transition its operations from current control to voltage control. The power circuit can be divided into four essential parts: (1) DC input stage; (2) bridge stage; (3) AC filter stage; and (4) utility stage. A number of small resistances (of 0.01 ohm) are included throughout the model to make the model more realistic and to facilitate convergence of the model in PSCAD simulation environment.

### *2.1.1 DC Input Stage*

The inverter is designed to accommodate a DC input from a 400 V DC source. In the model, the input consists of a controlled DC voltage source. The design also incorporates an input filter capacitor of 1mF to reduce input voltage disturbances. To prevent modeling verses actual device inconsistencies due to the nature of ideal electrical sources, a diode is also placed in the DC input path. As the model's usefulness matures, the DC input will be replaced with sources more representative of the intended DG source (photovoltaic array for example), and will not operate at a fixed voltage, but over a voltage range.

### *2.1.2 Bridge Stage*

The bridge stage is made up of four IGBTs that are controlled using a unipolar switching scheme as described in [2]. In a unipolar switching scheme, each leg of the bridge is controlled as a separate pair. The two switches in each pair are controlled in a complimentary fashion. In other words, when the top switch in a leg is closed, the bottom is open, and vice versa for the next switching interval. The control for each leg of the bridge is accomplished by comparing a control signal (onA) with a triangular waveform (sig1). This results in the following logic signals being applied to the gates of the IGBTs (using leg A as an example):

onA < sig1 : A1 on and A2 off
onA > sig1 : A1 off and A2 on

The control signal (onB) for the B leg is the negative of onA, but is compared to the same triangular waveform (sig1). This is shown below in Figure 2-2 with the frequency of triangular waveform significantly reduced for illustrative purposes.

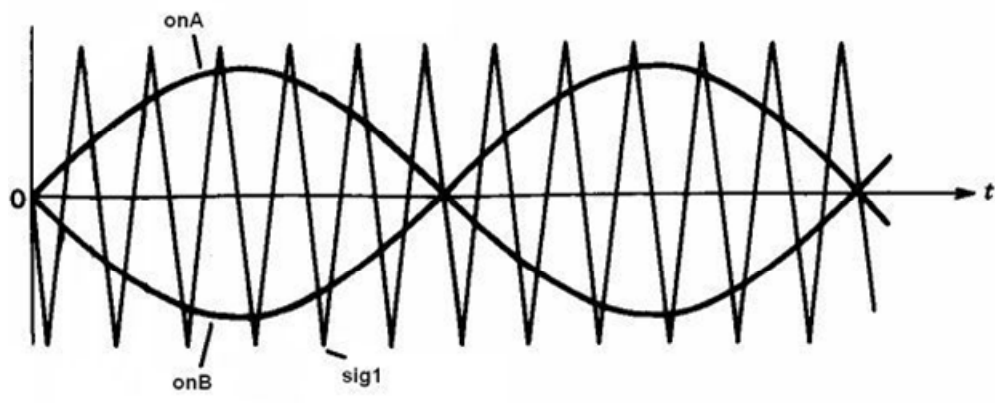


**Figure 2-2 Relationship between A and B Leg Control Signals and Triangular Carrier Waveform**

This results in the following gate signals being applied to the leg B IGBTs:

onB (or –onA) < sig1 : B1 on and B2 off
onB (or –onA) > sig1 : B1 off and B2 on

Figure 2-3 illustrates the results of this switching scheme for leg A. The bottom graph shows the comparison of the control signal with the triangular waveform and the other two graphs show the control logic being applied to the IGBT gates. The IGBT switches are closed when their logic inputs are high. When onA is less than sig1, A1 is commanded on (top graph) and A2 is off (middle graph). The opposite also holds true, as shown.

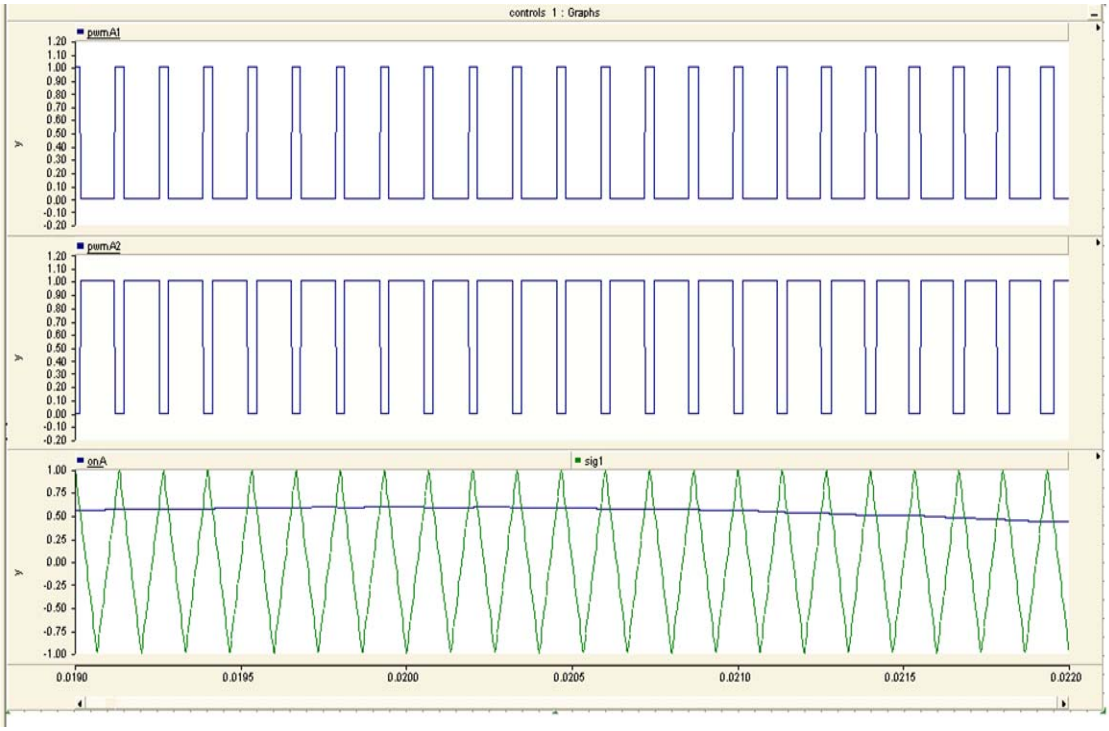


**Figure 2-3 PWM Switching Scheme for Leg A of Inverter**

Combining the effects of switching the A and B legs in this manner results in four output voltage states:

A1, B2 on : output = DC input
A2, B1 on : output = -DC input
A1, B1 on : output = 0
A2, B2 on : output = 0

Notice that when either both the top or both the bottom switches are on at the same time, the output is zero and current flows through the forward biased diodes. Controlling the IGBTs in this manner generates an output with an average that follows the control signal onA. Moreover, as long as the frequency of the control signal is much smaller than that of the triangular waveform, the output can effectively be a scaled mirror of the control signal. Thus, a controlled inverter output can be achieved by precisely controlling the signal onA.

The onA signal is either generated using a sine function (with variable magnitude, phase, or frequency components) or by a comparator output depending on whether the inverter is in current or voltage control mode. Details on these modes and how they affect onA are discussed in the next subsection. The result of this switching scheme is illustrated in Figure 2-4 which shows the PWM positive and negative pulses in green and red, respectively, along with their average values traced in blue showing it to be a sinusoidal signal.

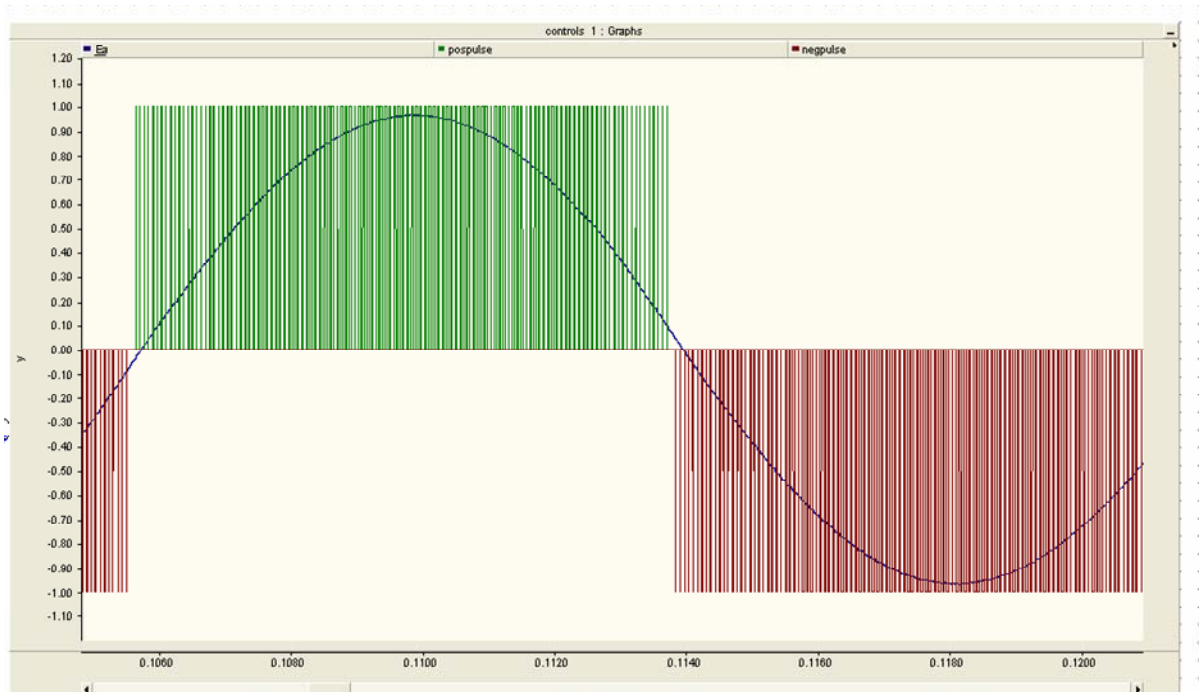


**Figure 2-4 Combined PWM Switching for Inverter**

Another thing to note is that the actual hardware used for the IGBT bridge stage can be configured to operate as either a single phase inverter or a three phase inverter, as they actually consist of six IGBTs. During single-phase inverter operations, two of the six switches are disabled. For single-phase modeling, these IGBTs add computational overhead without any benefit, and are, therefore, omitted.

### *2.1.3 AC Filter Stage*

The bridge output goes into the filter stage, which contains the energy storage elements necessary for circuit operation. The series-connected, 75mH inductors and parallel, 40uF capacitors are sized in order to achieve desired voltage and current ripple characteristics. The output is a single phase, 60 Hz, 120 V AC waveform.

PSCAD has certain source referencing (grounding) requirements for voltage and current sources that need a ground on the negative side of the input DC voltage. This arrangement does not accommodate utility grounding, therefore improper current paths are created. To prevent this from affecting the modeling performance, an ideal 1:1 turns ratio transformer is placed on the output. Actual system hardware implementation will not include this transformer.

### *2.1.4 Utility Stage*

The utility stage consists of a 120 V AC source and a circuit breaker. The breaker is controlled with timed breaker logic to facilitate opening and closing during a simulation run. The utility source is a constant magnitude, frequency, and phase AC source with some nominal series impedance. The state of the breaker is represented by the variable Breaker_52a, which varies between logic level 0 or 1, depending on whether the breaker is open (0) or closed (1).

## 2.2 Inverter Control Methodology

### *2.2.1 General Description*

A representative control block diagram for the inverter model is shown below in Figure 2-5. Actual control connections at the schematic level are more complex and not connected exactly as shown; nevertheless, their effects are accurately depicted in the block diagram.

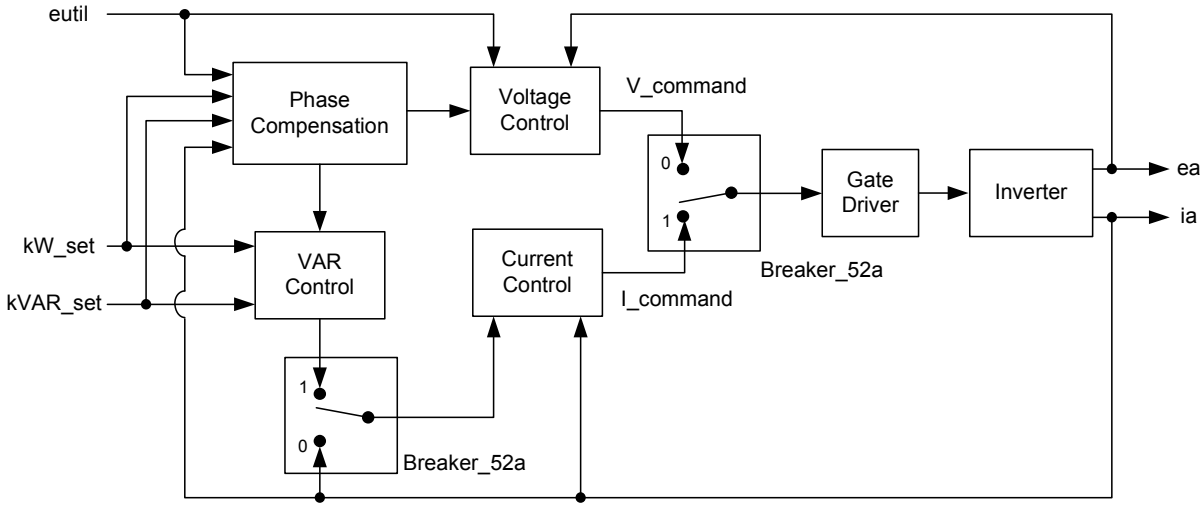


**Figure 2-5 Simplified Block Diagram of Inverter Control**

The inverter control system can be broken down into six basic parts with regard to its controls and operations. Starting with the reference signals for utility voltage (eutil), real power (kW_set), and reactive power (kVAR_set), these signals pass through control sub-systems for phase compensation, VAR control, voltage control, and current control. The output of these systems is fed into the gate driver block, which then provides the logic commands to the inverter IGBTs in the inverter block. The inverter block represents the model circuit and is described in the previous subsection.

In Figure 2-5, it can be observed that there are two active control loops, one for current control and the other for voltage control. Both control loops receive a compensation signal for phase adjustments from the phase compensation block. The inverter runs in the voltage control mode when it is not connected to the utility (i.e. in the islanded operation). When the inverter is connected to the utility, the system operates in the current control mode. There are two selection blocks, named Breaker_52a, that connect the appropriate control signals to the gate drivers based on the state of the utility connection. Breaker_52a follows the status of the utility breaker. When the utility breaker is closed, Breaker_52a is in state 1, and when it is open, it is in state 0.

When the Breaker_52a is open (state 0), the voltage control loop is providing the control signal to the gate driver block and the current control block's reference signal is inverter current (ia). Thus, the current control block is generating a current command signal that follows the actual inverter current. Even though it isn't being used in this mode, this feature

ensures a smooth transition between voltage control mode and current control mode depending on utility breaker state.

When the breaker closes, the controller changes to current control mode. In this mode, the VAR control block generates the desired current command based on set points for real power (kW_set) and reactive power (kVAR_set) along with the phase compensation signal. As the Breaker_52a is in state 1, the current command signal is fed to the gate driver controller and voltage command is ignored. Nevertheless, the voltage command signal is still generated to match utility voltage, so in the event of utility disconnection, the inverter transitions back to voltage control mode.

The phase compensation block provides control inputs to both the current and voltage control loops. The voltage control loop receives a signal that compensates for the phase difference between inverter voltage and utility voltage. Current control signals are adjusted by the phase compensator to ensure the desired reactive power is generated from the inverter.

### *2.2.2 Gate Driver*

The primary function of the gate driver is to convert an incoming control signal into an array of signals for turning on or off the IGBTs. It is made up of a triangular wave generator, a comparator network, and a time interpolation function. The PSCAD model screenshot of this circuit is shown below in Figure 2-6.

Each IGBT has its own dedicated interpolated firing circuit block with inputs to establish the logical conditions for turning each switch on or off. The carrier triangular waveform is also part of this circuit. The control signals, along with the triangular waveform, are supplied to the firing blocks, which make the decision to open or close the IGBT switches.

The outputs of the firing blocks contain a two element array of data. The first element is the logical state of the IGBT (0 or 1) and the second element is a time interpolation signal. Time interpolation is necessary when a crossing of two or more control signals must be detected, as is the case in a comparator circuit. Due to the fixed time step nature of PSCAD, any crossing of signals will most likely occur between time steps. By providing a time interpolated signal to the IGBT gates, more accurate model performance is achieved.

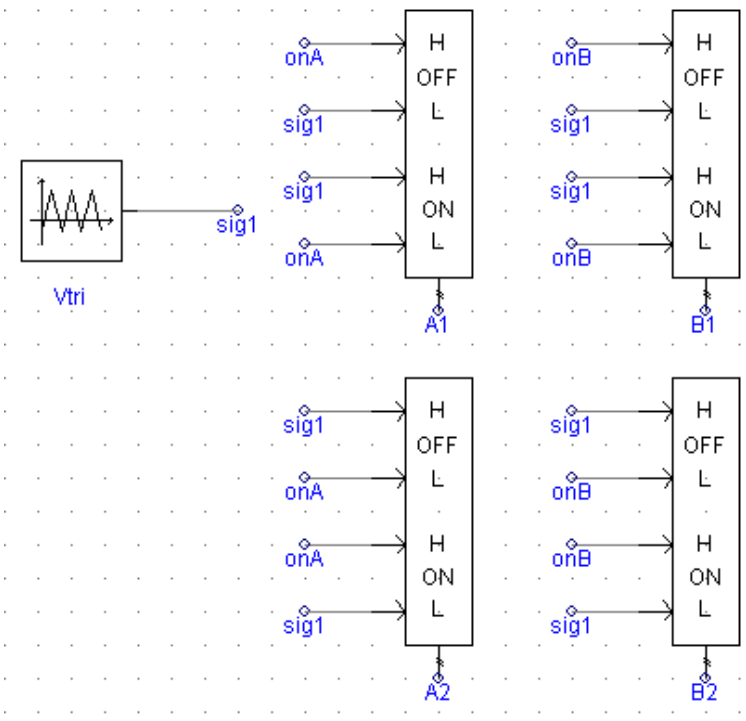


**Figure 2-6 Gate Driver with Interpolated Firing Pulses**

### *2.2.3 Voltage Control*

The voltage control system consists of a negative feedback loop containing a proportional integral (PI) compensator. As shown in Figure 2-7, a root mean square (RMS) voltage signal of the inverter output (E_arms) is normalized and subtracted from a reference. In this case the reference value is unity, as it is assumed that utility voltage is constant. The error signal is passed into the PI compensator that generates the amplitude of the control waveform, which is then used to generate the voltage control signal V_command. The phase of the V_command signal is generated by the phase compensation block. In voltage control mode (i.e. islanded operation), this V_command signal is fed to the gate driver block where it is compared with a triangular waveform to determine the duty cycle. As V_command increases, the average duty cycle of the gate driver circuit also increases raising the average output voltage of the inverter.

The initial gains of the compensator are determined using the Ziegler-Nichols Oscillation Method as described in [3]. Further tuning is achieved by performing multiple simulations of several scenarios. Best performance is observed when the following gain values are used, where G(s) is the PI compensator transfer function:

$$G(s) = \frac{K_P s + K_I}{s}, \; K_P = 0.5, \; K_I = 0.1 \qquad (1)$$

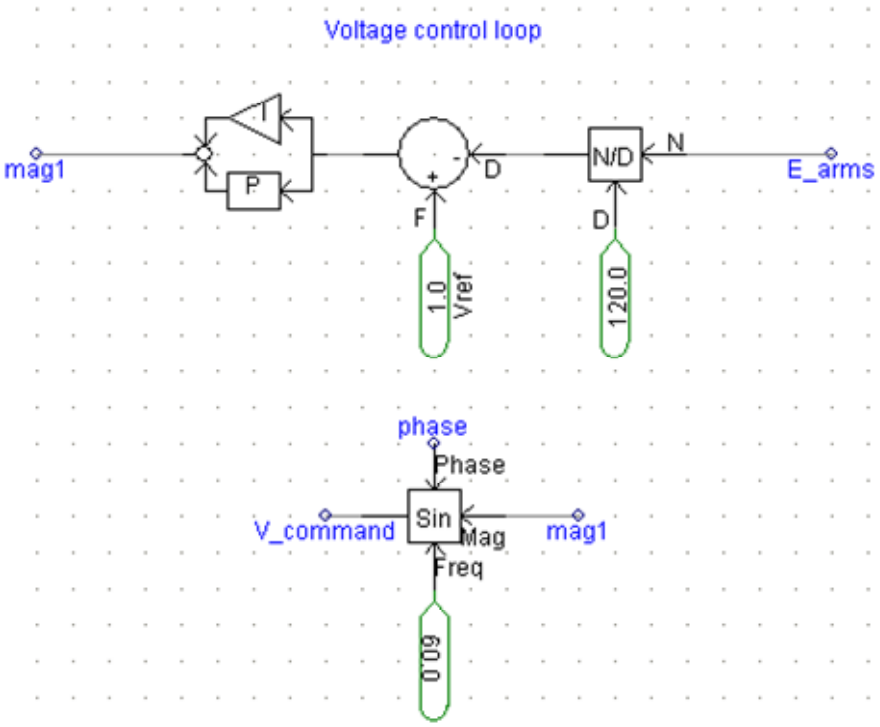


**Figure 2-7 Voltage Control Loop for the Inverter**

The performance of the voltage controller is evaluated against expected system transients. The most pronounced of these includes step input DC voltage changes. The response to these transients is displayed in Figure 2-8 and Figure 2-9. On both figures, the top graph is of the input DC voltage and the bottom graph is of the response of the inverter output RMS voltage. It is observed that the inverter responds correctly to the transients and re-establishes 120 V AC nominal voltage in about 10 cycles.

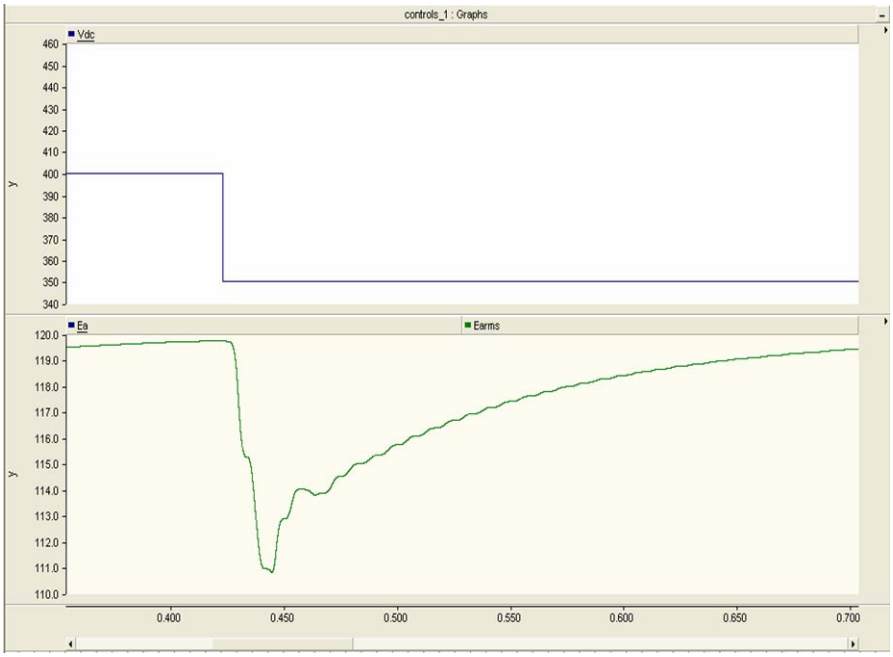


**Figure 2-8 Voltage Controller Response to a Step Decrease in Input Voltage**

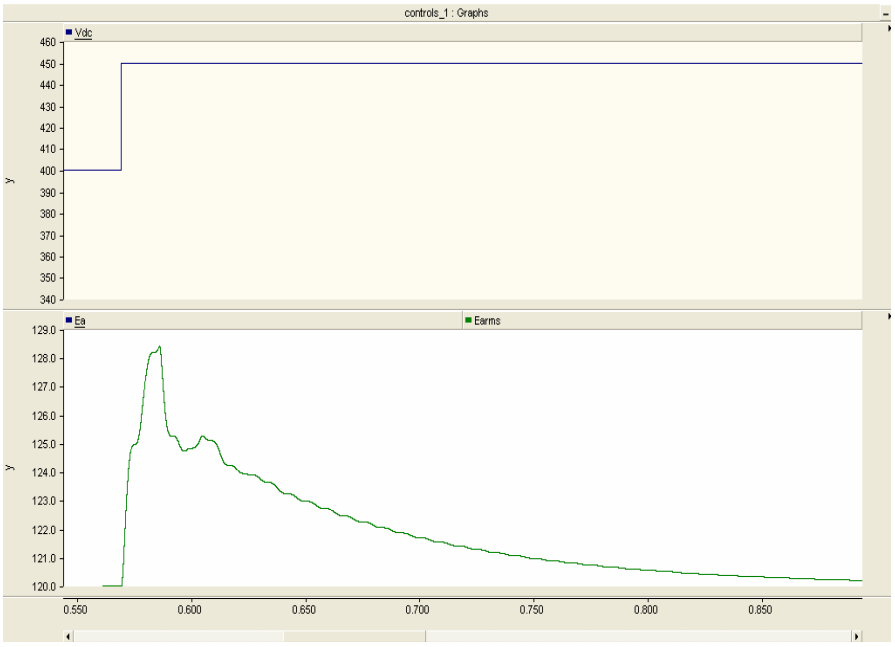


**Figure 2-9 Voltage Controller Response to a Step Increase in Input Voltage**

### *2.2.4 Current Control*

The current control loop is functional when the inverter is utility connected. The current controller can be subdivided into three parts: (1) transition circuit, (2) comparator circuit, and (3) stability saw tooth compensator circuit. Figure 2-10 shows the model schematic of the current control block.

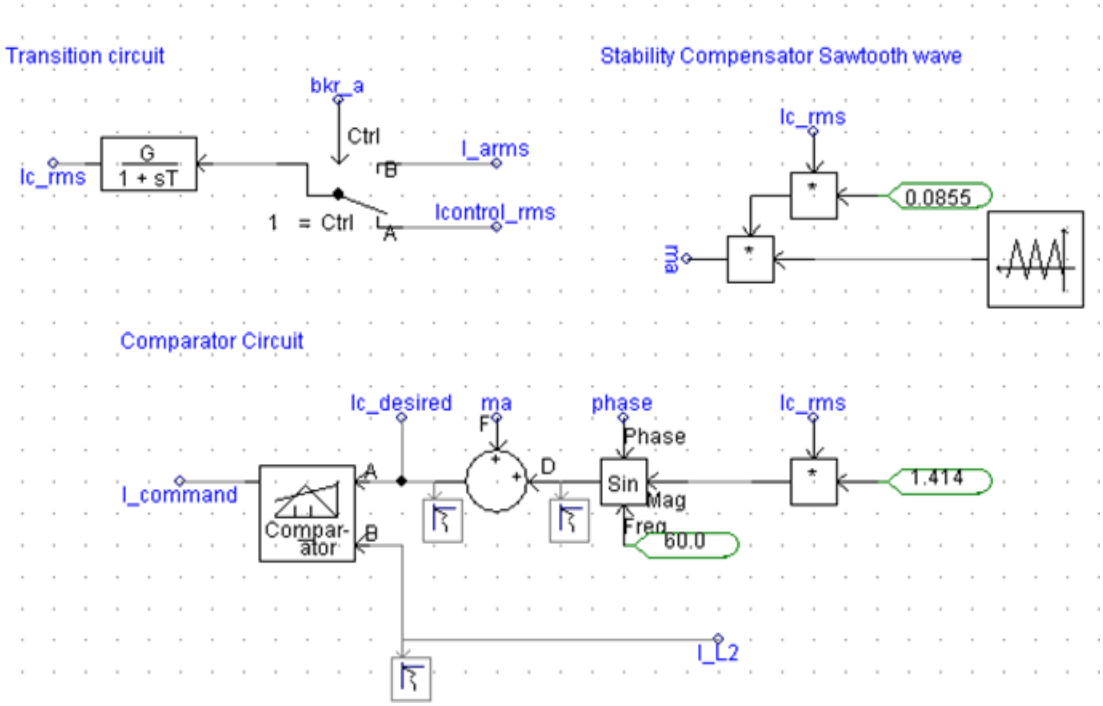


**Figure 2-10 Current Control Loop for the Inverter**

The VAR control block generates the desired current command (Icontrol_rms) for the current control block based off the KW_set and KVAR_set references, which is then fed to the transition circuit. This transition circuits is made up of a Breaker_52a switch and a unity gain with a real pole. Its output is the desired RMS current that feeds into the comparator circuit. Both actual measured inverter current (I_arms) and desired current (Icontrol_rms) settings are supplied to Breaker_52a. When the inverter is in voltage control mode, Breaker_52a is in state 0, and the desired RMS current is set to I_arms. When the inverter transitions to utility connected mode, Icontrol_rms becomes the controlling variable. However, to ensure a smooth transition, the unity gain real pole dampens this step change causing the inverter output current to slowly ramp to its new value. The time constant for the real pole is determined through trial and error and is 64ms.

Figure 2-11 displays the operation of the transition circuit. The top curve (green) in the graph represents the desired current based on the settings for real and reactive power. The other two curves in the graph represent the measured inverter current (red) and the desired current signal (blue). Prior to the transient, the inverter is in voltage control mode and current is being controlled to the actual inverter output current. Once the breaker is closed, the inverter transitions into current control mode and the output current slowly ramps up to the desired current.

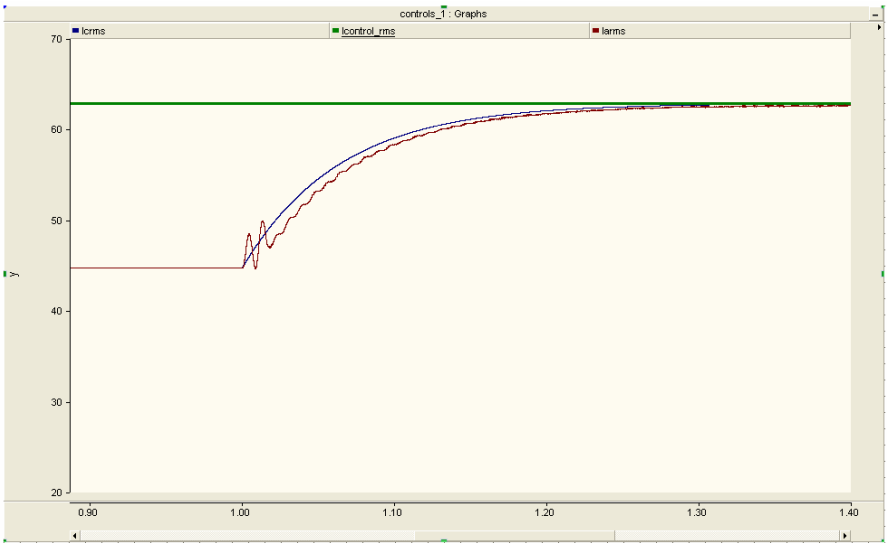


**Figure 2-11 Inverter Currents during Transition from Voltage to Current Control Mode**

The comparator circuit receives four inputs. The two primary inputs are the measured current across one of the inductors (IL2) and Icontrol_rms. A phase adjusted sine wave is generated based on the magnitude of Icontrol_rms and the phase input. This sine wave is compared to IL2 and the controlling output I_command is generated. To ensure stability for high-duty cycle conditions, a stabilizing saw tooth wave is added to the phase adjusted sine wave. The saw tooth wave parameters are developed following the guidance described in [4] and are scaled based on operating conditions.

The user inputs to the current control block are the desired real and reactive power settings. These settings are used to determine the magnitude and, via the phase compensation network, phase adjustments to the control current signal. The current control block is tested by making step changes in real and reactive power set points. Figure 2-12 demonstrates the transient response for a 2kVAR change in the reactive power setting. The top graph shows the real power, which remains constant during this transient. The bottom graph shows the step change in KVAR_set (in blue) as well as measured inverter output reactive power (in green). Figure 2-13 displays the inverter response to a step change in real power settings. In this case, the reactive power remains constant and the inverter tracks the step change with a highly damped response. Again, the top graph shows the real power and the bottom graph shows the reactive power.

It should also be noted that there is a small, steady state error for both the real and reactive power output. This has not been entirely resolved, but it is speculated to stem from the difference between the controller sensing point in the circuit and the output power measuring location. Also, there are non-ideal components between these two points, which would account for at least some of these differences.

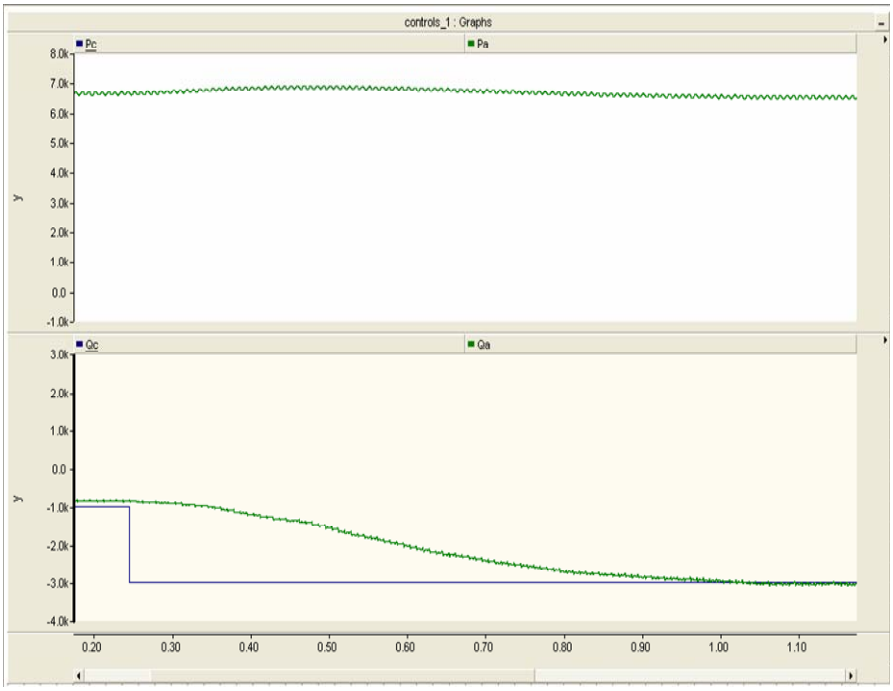


**Figure 2-12 Inverter Response for a Step Change in Reactive Power Setting**

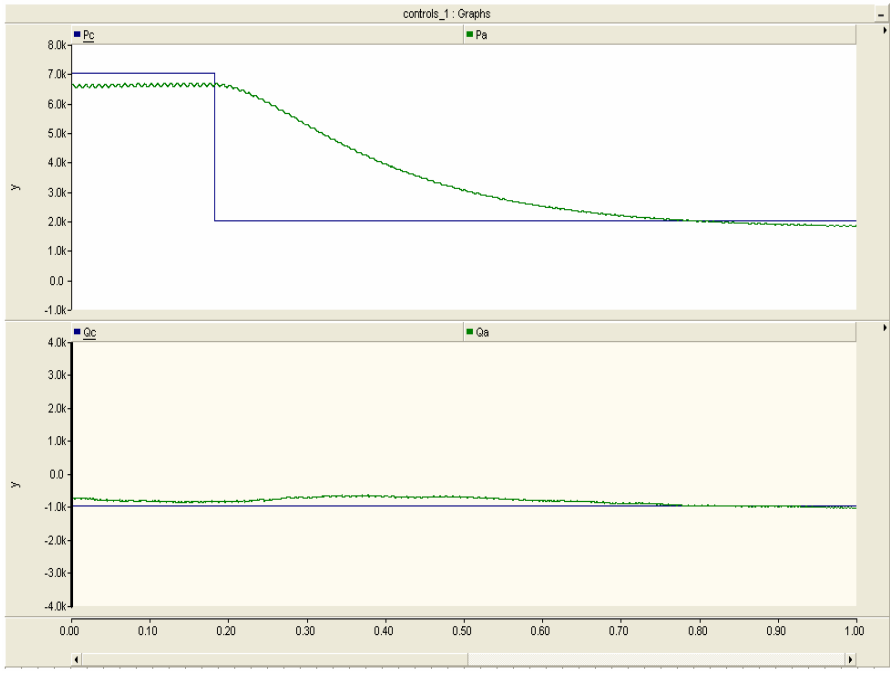


**Figure 2-13 Inverter Response for a Step Change in Real Power Setting**

### 2.2.5 Phase Compensator

The model schematic for the phase comparator is given in Figure 2-14. The measured inverter output current or voltage, and the utility voltage are filtered and fed into a fast Fourier transform blocks. Phase angles for the fundamental frequency components of these input signals are compared and used to generate an output phase compensation signal (phase). When the inverter is in current control mode, an additional phase angle adjustment is added to utility phase based on the real and reactive power references. Preferable compensator response characteristics are obtained using a PI compensator with proportional and integral gains of 0.5 and 1.0, respectively.

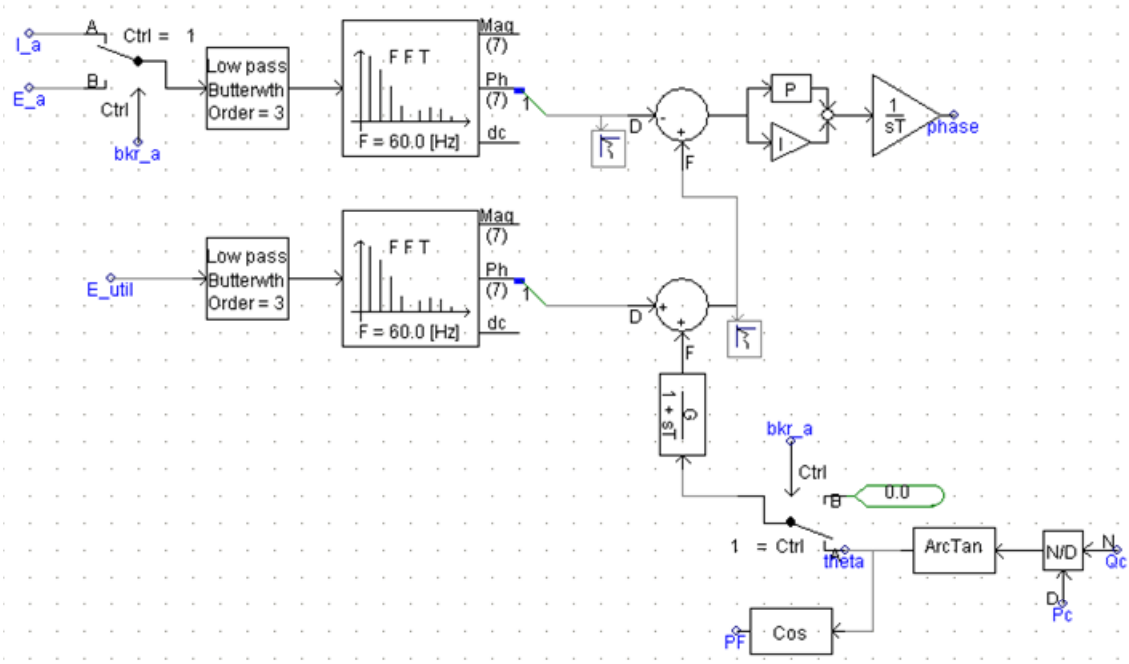


**Figure 2-14 Phase Compensation Network**

Model performance is validated by evaluating the response of the phase compensation controller for step changes in utility voltage phase angle for voltage control mode and reactive power settings for current control mode. Figure 2-15 shows a simulation result for the voltage control mode. Phase angle adjustment is not possible for the utility voltage source during a simulation, so its phase is set prior to the simulation. The inverter voltage can be observed to adjust itself back into phase with the utility. Although this is not a typical step response evaluation, the results that are obtained are adequate for ensuring proper performance. On the graph, the constant, -130 degree line is the phase angle for the utility voltage. The inverter output voltage starts at +20 degrees and matches utility phase in approximately 0.35s.

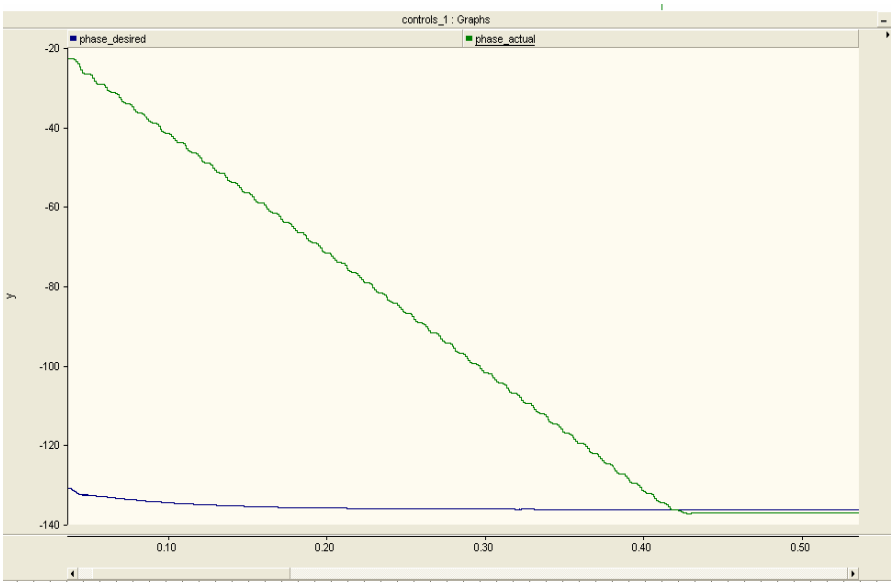


**Figure 2-15 Phase Compensation in Voltage Control Mode**

Phase compensation during utility connected mode is also performed satisfactorily. In Figure 2-16, the inverter output current phase angle (green) is compared with desired phase angle based on a change in desired reactive power settings. It can be observed that the desired phase angle (blue) has an exponential response as well, with a step change in the reference. This is due to the design and is deliberately performed by a real pole block in series with the desired phase signal. It is found that without this mechanism, the FFT blocks will saturate causing instability problems.

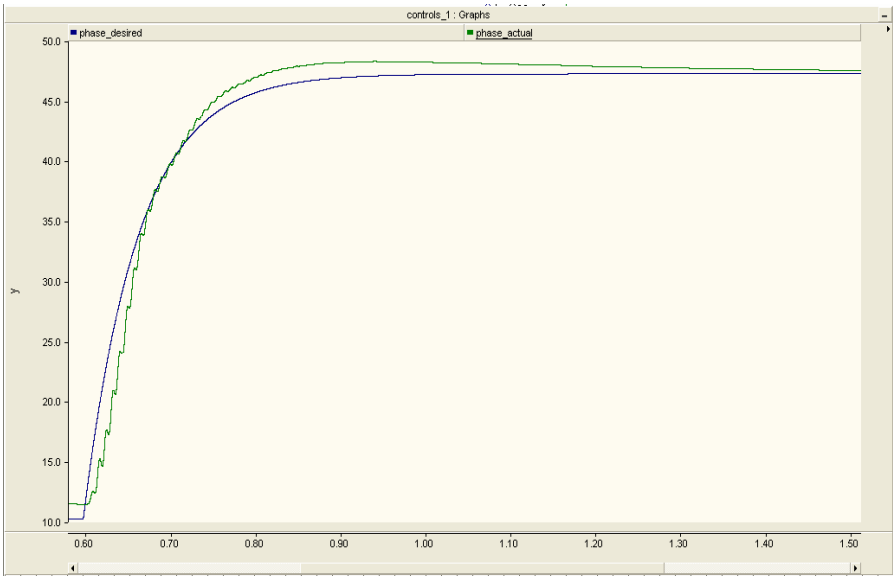


**Figure 2-16 Phase Compensation in Current Control Mode**

# 3 Hardware Design

In parallel to the modeling and simulation of the advanced power electronics interface (APEI), NREL also built a generic inverter platform for evaluating the performance of new controls and protection algorithms as related to a utility connected inverter. The inverter hardware and controls are designed to ensure modularity and flexibility of the power electronics system. The integrated power electronic modules with IGBTs are used for the power circuit, whereas a DSP based controller is designed to facilitate the universality of the hardware platform so that it can be used to experiment with different distributed generation sources or control and/or protection objectives.

## 3.1 Inverter Power Circuits

The power circuit of the inverter platform consists of a Semikron [5] IPEM along with sensors, auxiliary power supplies, and relays. At this initial phase of development, a California Instruments [6] AC electronic load was used for testing. A DC power supply was used as the input of the inverter.

### *3.1.1 Integrated Power Electronics Module*

IPEMs that have recently come on the market consist of power electronic switches, DC-link filter capacitors, current and temperature sensors, gate drivers, heat sinks, and optional DSP controllers are combined into a single highly optimized module [7]. The inherent advantages provided by the IPEMs are shorter time to market, easier system design and assembly, reduced number of components, economical, standard interface design and reliability.

In the hardware platform, a Semikron Advanced Integration (SKAI) module manufactured by Semikron has been used that consists of six 1200 V, $300A_{rms}$ IGBT switches arranged in three-phase bridge format. The DC bus filter capacitor, voltage and current sensors, auxiliary power supply, and gate drivers are all included inside the IPEM on a common heat sink. Though an optional DSP controller can also be included inside the SKAI module, an external DSP is selected for this particular design to have more flexibility. The structure of a Semikron IPEM is shown in Figure 3-1. The presence of 1 mF capacitance inside the IPEM eliminates the need for external DC bus filters [8].

The manufacturer for this particular IPEM claims that some novel packaging and assembly techniques result in higher reliability within the modules. For example, pressure contact technology eliminates the large solder interfaces typically seen between the direct-bonded copper and the module base plate. Greater reliability also is achieved by using an aluminum-nitrite substrate rather than the less-expensive alumina ($Al_2O_3$) [7]. Although the modules are highly integrated, off-the-shelf products, the underlying technology lends itself to the development of several standard configurations such as different heat sinks, additional output sensors and a wide selection of switching devices to populate the module.

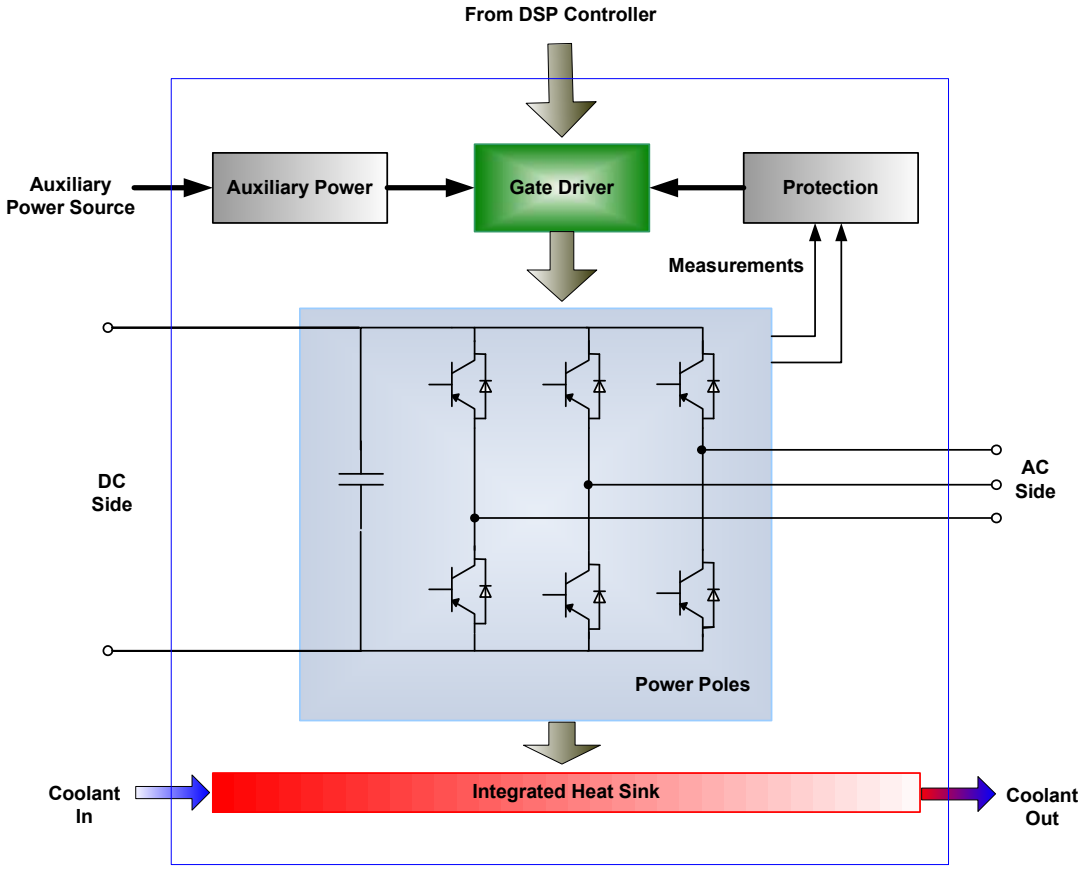


**Figure 3-1 Block Diagram of Semikron HV SKAI Module**

### *3.1.2 Auxiliary Power Supplies*

Different DC voltage levels are necessary for the operation of different parts of the hardware. The HV SKAI module requires 24 V DC, the DSP board requires 5V, and additional 3.3V is required for all the electronic ICs. A small DC power supply is used for generating 24V from 120V utility. The 5 V is developed from the 24 V using a buck converter, and a linear regulator circuit is used to develop 3.3 V from the 5 V. Besides, the DSP requires two reference voltages, nominally at 1.0 and 2.0 volts. The accuracy of the DSP A/D converter depends upon the difference between these voltages being precisely 1.000 volts +/- 0.1 %. A precision micro-power, low dropout voltage reference IC is used for generating the voltage references for A/D converters in the DSP. Also, level shifters from 3.3 V to 5V are utilized to match the control outputs to the SKAI input requirements.

### *3.1.3 External Sensors and Relays*

The phase current sensors, DC bus voltage sensor and heat-sink temperature sensor are integrated in the SKAI module. In addition to those sensors, voltage and current sensors are added to different parts of the hardware to achieve control and protection requirements. Relay circuits are incorporated in to the system in order to facilitate different modes of operations such as utility-connected or islanded operation of the inverter. There are two types of relays used in the setup. The pilot relay contacts are closed by the controller circuit, which are then used to supply the 120 V AC to the power relay coils and thus closing the power relays.

A picture illustrating the front side of the inverter platform is shown in Figure 3-2. The detailed circuit diagram for the power circuit and its connection to the control board are shown in Figure 3-3. The circuit in Figure 3-3 is for the single-phase inverter where two legs of the three-phase IGBT bridge are utilized.

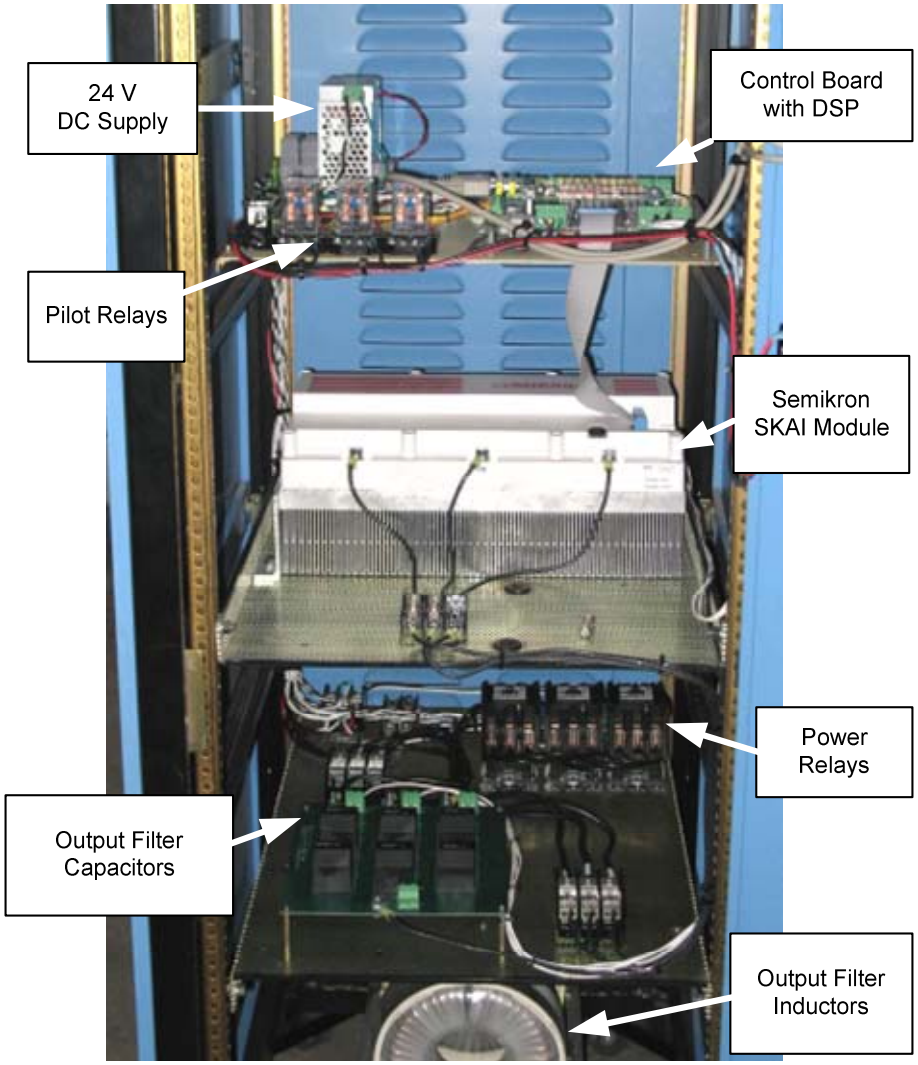


**Figure 3-2 Picture of Front Side of Inverter Platform**

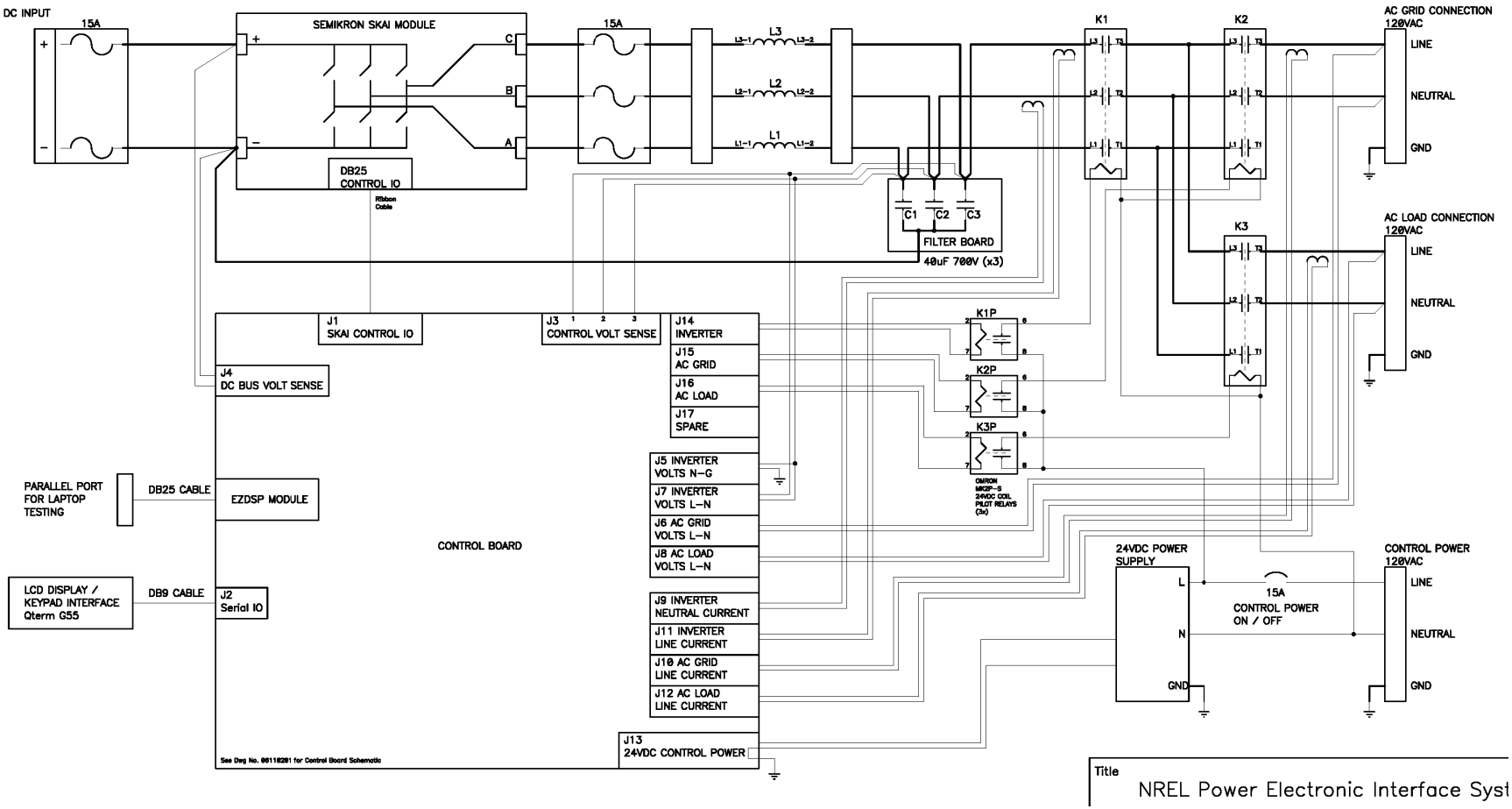


**Figure 3-3 Detailed Power Circuit Diagram and Connections (Drawn in P-CAD)**

## 3.2 Inverter Control Design

There are three significant parts in the inverter control design. The design revolves around the control board, which includes the DSP. Also the interface between the control board and the hardware setup is the part of control design. An interface is also required for communication between the control board and the higher level CPU based controller. The final component of control design is the development of software codes both for the local DSP controller and for the higher level CPU based controller.

### *3.2.1 Control Board*

The control board is designed with a Spectrum Digital eZdsp™ F2812 evaluation module [9]. This module contains the TMS320F2812 DSP by Texas Instruments. To simplify code development and shorten debugging time, a C2000 Tools Code Composer Studio [10] driver is provided with the eZdsp module. In addition, an onboard joint test action group (JTAG) connector provides interface to emulators, operating with other debuggers to provide assembly language and 'C' high level language debugging. The eZdsp F2812 with TMS320F2812 DSP has the following features:

- 150 MIPS operating speed
- 18K words on-chip RAM
- 128K words on-chip Flash memory
- 64K words off-chip SRAM memory
- 30 MHz. clock
- 2 expansion Connectors (analog, I/O)
- Onboard IEEE 1149.1 JTAG controller
- Onboard IEEE 1149.1 JTAG emulation connector
- TI F28xx Code Composer Studio tools driver

All the auxiliary power sources, which are discussed in the previous sub-section, are developed inside the control board. The control board gets a single 24 V DC supply and it then generates all other voltage levels. The inputs to the control board are DC bus voltage, phase currents, heat sink temperature and fault signals from the SKAI module; voltage and current measurement signals from the external sensors; mode selection and startup signals from the external CPU. The main outputs of the control board are the gate drive PWM signals for the SKAI module. Additionally, the control board also provides enabling signals for the SKAI; PWM status signals to the external CPU; operating signals for the pilot relays. Also instead of the startup and mode selection signals from the CPU, it can be provided using a human machine interface (HMI). The local controller is designed to provide control and communication functions for the IPEM it is associated with. As the DSP module has sufficient calculation power, it is preferred to carry out the voltage and current control inside the local controller in addition to the PWM generation for the switches. A simple block diagram of the control board is given in Figure 3-4.

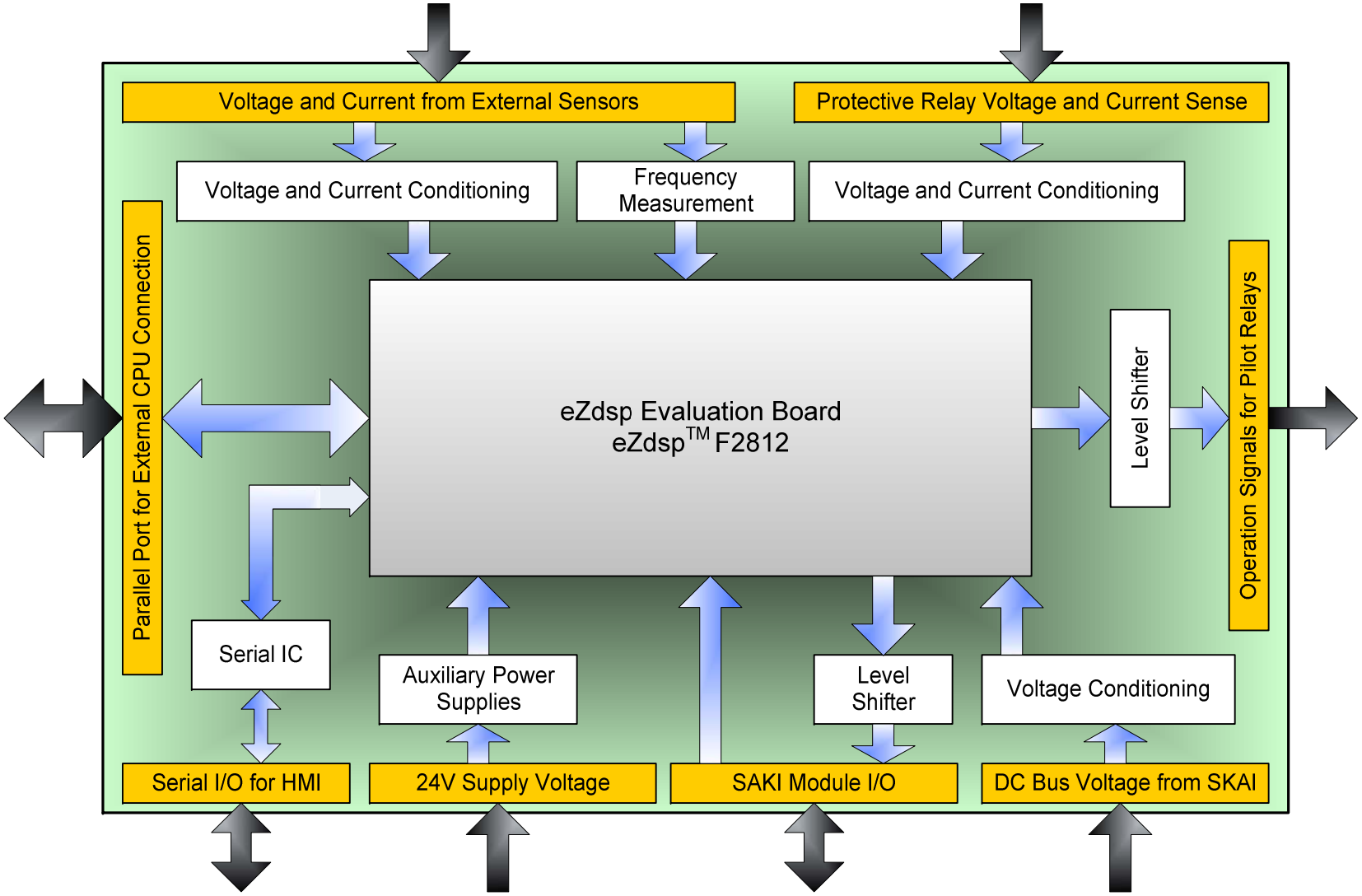


**Figure 3-4 Block Diagram of Control Board Showing Input/Output Connections and Components**

### 3.2.2 Control Interfaces

From Figure 3-4, it can be observed that the control board has different types of interfaces with the hardware, external HMI and external CPU. The power is supplied to the control board by an AC/DC converter that converts 120 V, 60 Hz AC into 24 V DC. The signals from the voltage and current sensors are directly fed into the control board, as it has several voltage and current conditioning systems that converts the measured voltage/current into DSP input compatible quantities. The connection between SKAI module and DSP is obtained using D-sub 25 pin connector with ribbon cable. The higher level controller in CPU is currently connected to the DSP board through JTAG compatible parallel port. But later this interface may need to be replaced by using controller area network (CAN) or asynchronous serial communication. The HMI is connected to the panel-mount graphic operator interface terminal. A picture of the control board is given in Figure 3-5.

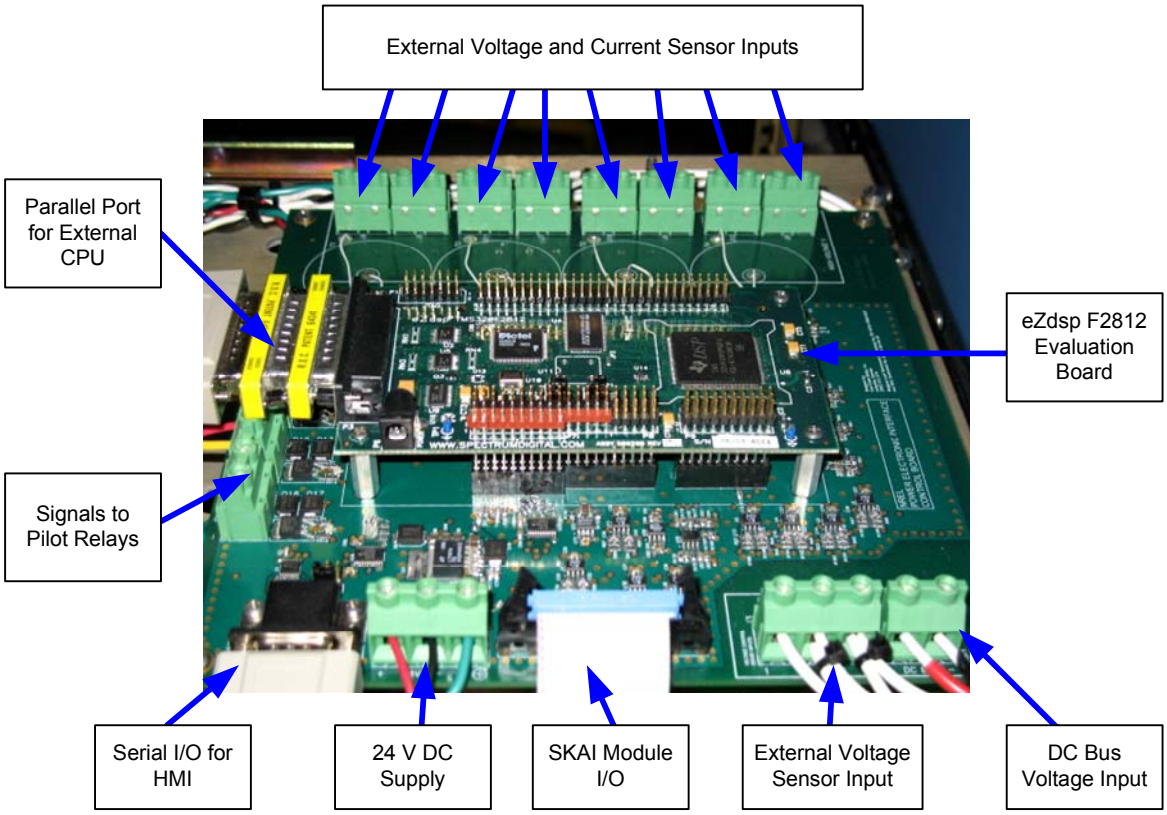


**Figure 3-5 Picture of Control Board with Input/Output Connections**

### 3.2.3 Software Development

Up to this point, the voltage and current control for the inverters are implemented in the DSP controller. The program for the DSP is written using Texas Instruments' Code Composer Studio™ IDE, which offers robust, mature core functions with easy-to-use configuration and graphical visualization tools for faster system design. The codes are written based in C programming language and then compiled and load into the DSP on-chip random access memory (RAM) using Code Composer Studio. Then the controller is activated using the

serial interface. In future, the on-chip flash memory will be used for utilization of larger codes and retaining the compiled codes in the DSP. The program code is interrupt driven and runs at fixed sampling frequency of 10 kHz based on the interrupt set up. For the inverter platform, the switching frequency is set at 10 kHz. The actual program codes for PWM calculations are written inside the interrupt service routine. This service routine runs once in each PWM cycle and is used to compute duty cycles for the next cycle.

## 3.3 Experimental Results

The hardware design was verified with step-by-step testing of different components from the power circuit and the control board. After the individual components were tested for proper functionality, the voltage control and current controls were tested and results were obtained during this preliminary investigation phase, where the main goal was to develop a platform to evaluate the performance of new controls and protection algorithms as related to a utility connected inverter.

### *3.3.1 Testing of Control Board*

Several tests were done during the construction of the control board to check all the intended operations. A list of the tests performed and the results are given below.

- The 24 V to 5 V buck regulator was tested first. All 5 V loads were disconnected from the output of the regulator so that, in cast of regulator non-functionality, there would be no damage. The regulator was powered up from a current limited supply to prevent the possibility of damage. The regulator was tested from no load to 2.0 A and short circuit at 25 V DC input and with constant 1 A load that operates from 8.0 to 40.0 V DC input. It was observed that the turn on and turn off into 1 A load is very well behaved with no over shoot. Rise time of 5.85ms and fall time of 6.98ms.
- The 5 V to 3.3 V linear regulator was checked next. The regulator was tested to operate properly from 0 to 100mA of load.
- The auxiliary control outputs were tested by running test code in the DSP that toggled the control pins on and off.
- The voltage reference circuits were tested next. The DSP requires two reference voltages, nominally at 1.0 and 2.0 volts. The accuracy of the DSP A/D converter depends upon the difference between these voltages being precisely 1.000 volts +/- 0.1 %. The measured voltage differential is observed to be 0.9990 V, an error of – 0.10 %. The two reference voltages were measured as 2.0460 V and 1.0470 V.
- The 3.3 V to 5 V level shifters were tested by running test code in the DSP that toggled the PWM and control output pins. The corresponding signals were traced to the SKAI module connector and the Aux Control Outputs. Normal operation was observed.
- Protective relay voltage measurements were tested next. For voltage sensors, the scales and offsets of their amplifiers was adjusted to better fit the analog input range of the DSP of 0.0 to 3.0 V. The resulting full scale voltage input was +/- 200 V. Each voltage sense input was fully differential with an input impedance of 2.0 MΩ. These signals were tested with a signal generator that only goes to 20 $V_{pk\text{-}pk}$.

- Protective relay current measurements were tested next. The initial intent was to use a trans-conductance input amplifier configuration from the current transformers (CT), but it was found that under full load, secondary CT current would be 33mA, *and* that coil resistance roughly equals the burden resistor in the CTs. These CTs have a built-in burden resistor so that the full scale output is 0.333 V AC. Therefore, component values in the circuit ware changed to scale the voltage gain to 3.00x with a 1.50 V output offset. These circuits were tested before the CTs were installed to ensure proper operation with a full scale 0.333 V AC input.
- Power module voltage measurements differ from the protective relay voltage measurements because all of the latter inputs were referenced to the DC negative terminal. In order to make full use of the A/D input range, these circuits were also rescaled and the offset was set to analog ground. The voltage can range from 0 to 400 volts (peak) on the phase and DC voltage inputs. These signals were tested using a low voltage signal generator.
- The frequency measurement circuit was tested next. RC filtering was added at the input to the comparators. The fast filter was intended to filter out the effects of high frequency noise and the slow filter was used to nominally track the DC offset of the signal. These comparators do not precisely detect the zero crossings, but they give a good indication of signal frequency.
- The RS232 hardware testing was completed. For this test a null modem cable was connected between one of the serial ports on a PC and the serial connector on the control board. A DSP board that was not programmed was used, which leaves the RX and TX pins as high impedance. Then, using the terminal software on the PC, the connection was tested and probed with a scope on the control board to verify proper operation.

### *3.3.2 Voltage Control*

For all utility connected inverters, the loads can get power from either the utility grid or from the distributed source's inverter depending on the state of the utility connection and/or the available distributed generation. In case of grid failure (i.e. grid faults, maintenance, etc.), the connected loads have to be supplied by the inverter. In such a scenario, which is often referred to as the islanded operation, the inverter has to maintain the amplitude and the frequency of the voltage so that the connected consumer loads are not affected by the utility interruption. The voltage control loop for the inverter is designed for such islanded mode of operation.

Though constructed for the three-phase inverter, the actual hardware used for the inverter can also be configured to operate as a single phase inverter. During single phase inverter operations, two of the six IGBT switches were disabled. For testing the basic functionality of the inverter platform, single phase connections are considered. The DC supply is left floating and one leg of the inverter is switched by a PWM with 50% duty cycle to create the neutral. The other leg is controlled by PWM to have the controlled voltage at the inverter output. The advantages of such topology, which is known as the half-bridge, lies in the simplicity of its structure and ease of implementation. However, the voltage transfer ratio from DC to AC is only one-half, which means without considering any voltage drops and losses, the peak amplitude of the output AC voltage is limited to one-half of the input DC voltage.

For this experiment, a Sorensen DHP series [11] 400 V, 10kW DC supply is used to generate the DC bus voltage. This is a general purpose DC power supply specifically designed for laboratory tests that requires variable DC with good ripple and regulation characteristics. The input to the power supply is three-phase, 4-wire, 208 V (L-L), 60 Hz AC. The output is either a constant voltage or constant current DC with an automatic crossover feature.

The output of the inverter is connected to a California Instruments 3091LD Series 3kW AC Load [6]. The 3091LD is designed to provide precisely controlled non-linear loads for testing AC power generation equipment such as uninterruptible power supply, AC sources, electrical switches and circuit breakers. The ability to simulate high crest factor and variable power factor AC load conditions provides an effective method of testing these and other AC products against real-world conditions and can significantly increase product reliability.

A block diagram of the test setup is given in Figure 3-6. The relay between the inverter and the utility is open so that the load gets power only from the inverter. The control board gets the power from the AC/DC supply, which generates 24 V DC from the input of single-phase 120V AC. Though the inverter power circuit is electrically islanded from the utility, the control circuit monitors the grid voltages via voltage transformers and synchronizes the inverter output to the utility.

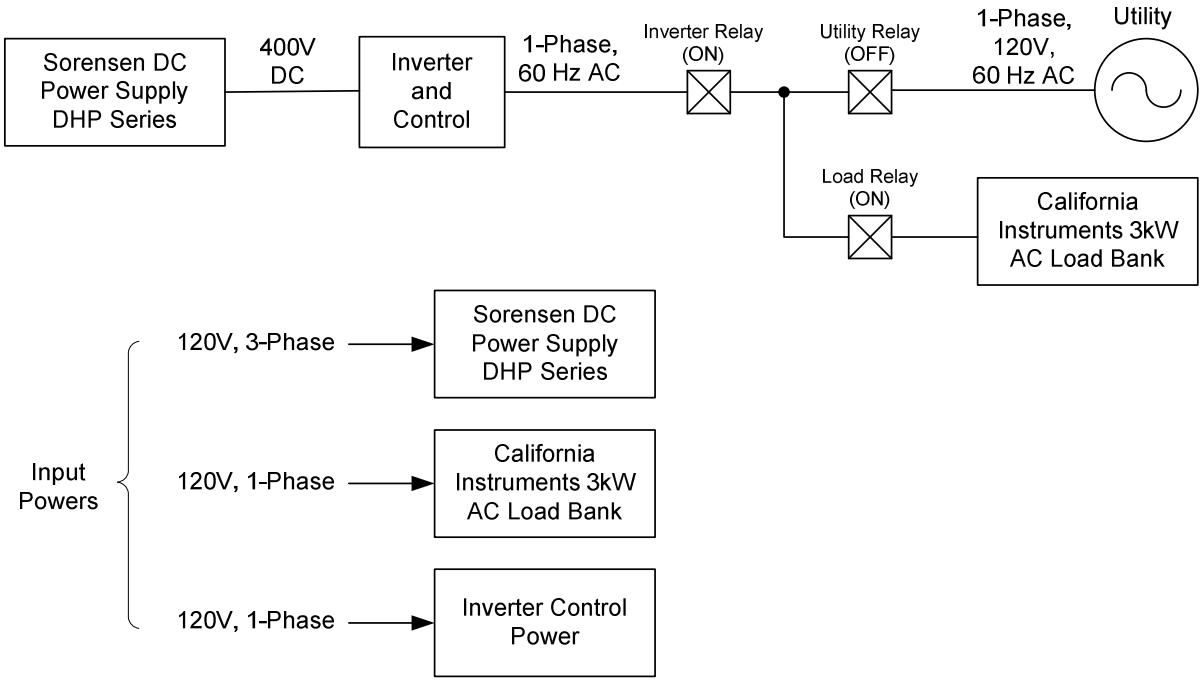


**Figure 3-6 Block Diagram of Voltage Control Test Setup**

Initially the inverter is run open loop with a DC bus voltage of 400 V. The variable resistive loads are used to observe the voltage regulations with the load as shown in Figure 3-7.

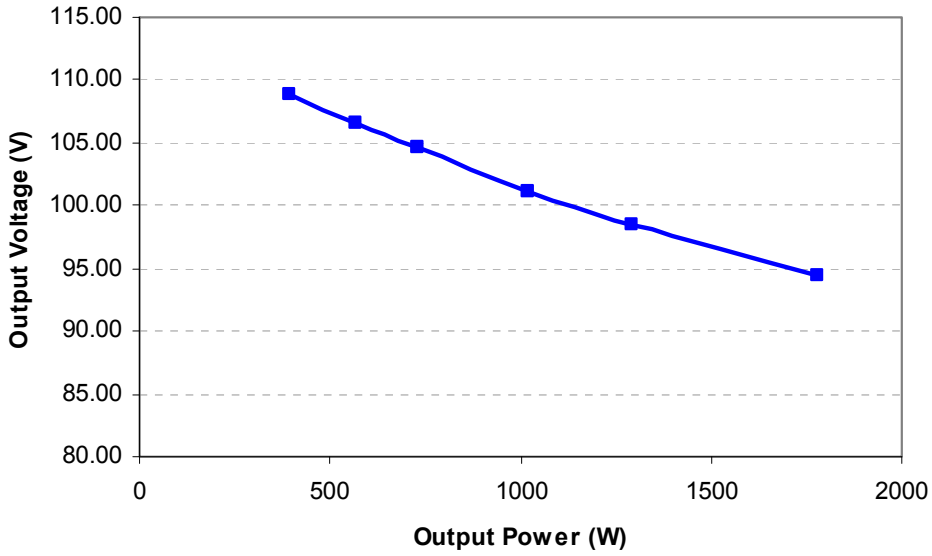


**Figure 3-7 Voltage Regulation of the Open Loop Inverter**

The results produced some important observations. The efficiency of the inverter system was low in the range of 80%. This can be attributed to the fact that the IGBTs are rated for 300 A continuous current and 1200 V RMS and they are optimized around the full-load operating point. But in the inverter platform, the maximum current is limited by the wiring and other components ratings and is limited to 30 A. The results also show that ideally the maximum amplitude of the output voltage is 200 V, although in the experimental system, the voltage ratio only causes around 110 V RMS (i.e. 156 V peak) of the AC voltage available. The inverter platform is built to have some flexibility so that different distributed energy sources can be connected to it in future. The obvious tradeoff to ensure the flexibility is the unutilized design of the system and components; especially, the output L-C filters are not optimized due to generalized design. This is probably what is causing the inverter voltage ratio to be poorer than expected.

In the next phase, a proportional controller was designed to act on the error between the reference voltage and inverter output voltage and adjust the duty cycle. The reference voltage has an RMS value of 120 V and a 60 Hz frequency. The controller operates at each sampling period and the duty cycle values are updated based on the controller output. The voltage regulation for the load is shown in Figure 3-8 when the controller proportional gain ($K_p$) is 0.2. In Figure 3-9, the oscilloscope screenshot of the inverter output voltage (first channel) and load current (second channel) are shown. The load is a simple 10 ohms resistive load. The harmonic analyses of the output voltage and load current are given in Figure 3-10. It can be observed from these figures that, although the control is partially working, there still remains a steady state error on the output voltage. Increasing proportional gain will saturate the duty cycle values and become ineffective. The conclusion from these results is that the proportional controller alone is not sufficient enough to maintain the output voltage RMS value at 120V.

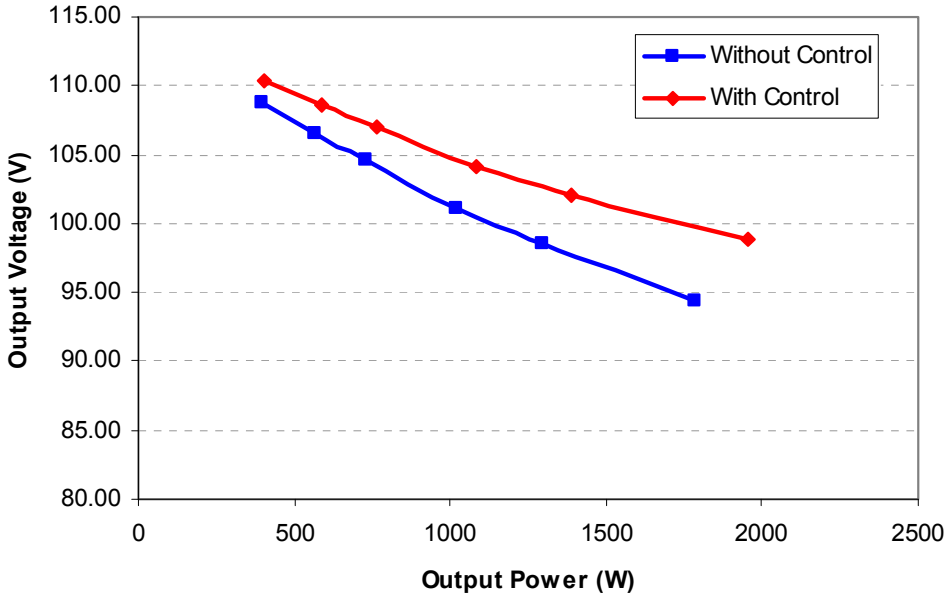


**Figure 3-8 Voltage Regulation of the Voltage Controlled Inverter with $K_p$ = 0.2**

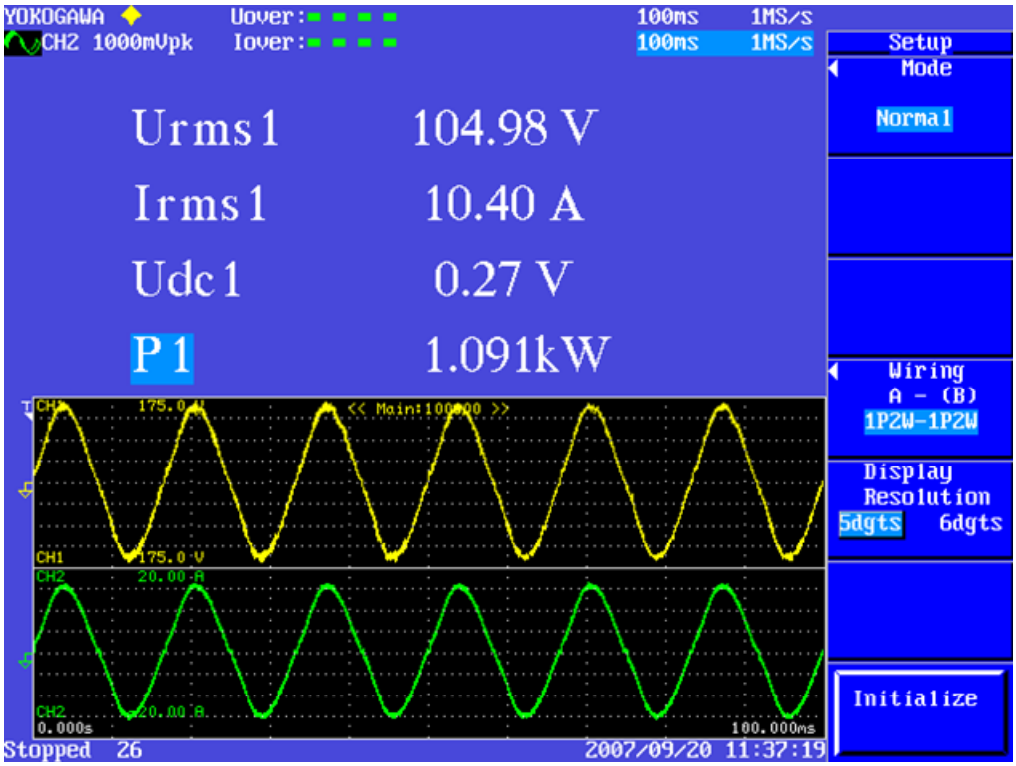


**Figure 3-9 Screenshot of Inverter Output Voltage and Load Current**

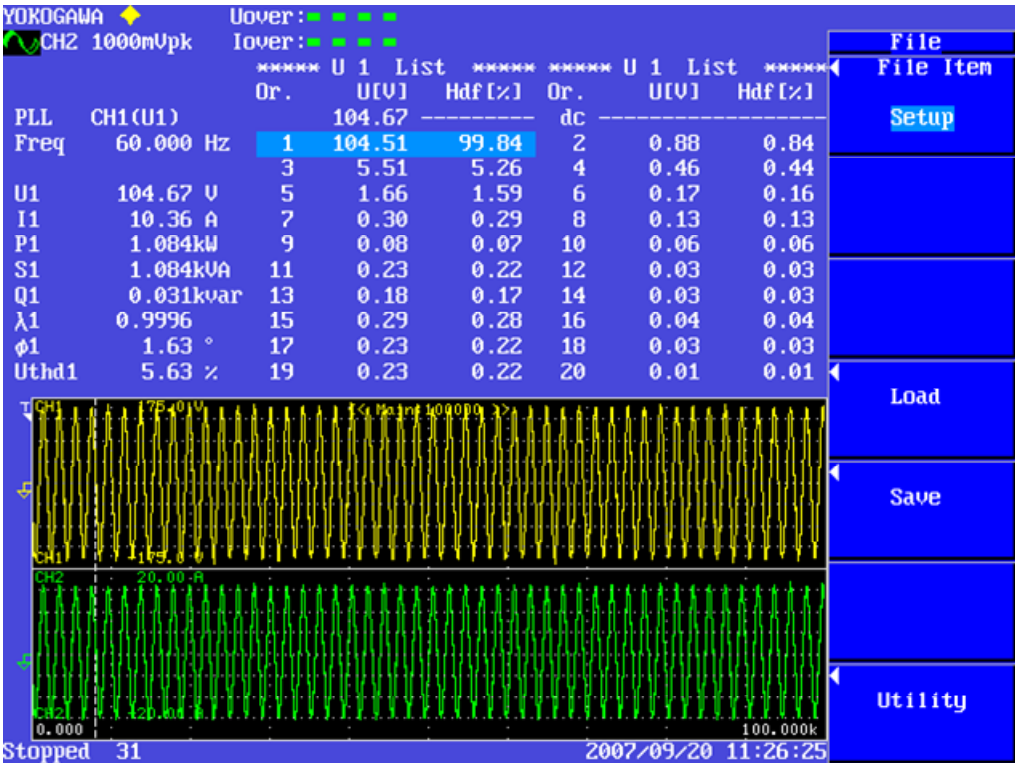


**Figure 3-10 Screenshot of Harmonic Analysis of Inverter Output Voltage and Load Current**

To overcome the steady-state error problem, another slow voltage control loop was developed to compare the output voltage to the reference voltage amplitude and change the reference voltage amplitude based on the error. This control loop works once in each voltage cycle (i.e. it runs at 60 Hz frequency) and is termed as a slow control. The inverter system is first run to generate 120 V RMS AC, but it was found that although the RMS value of the output voltage is close to 120 V, the voltage waveform has significant amount of peak chopping making the total harmonic distortion (THD) quite high. As mentioned earlier, the unoptimized design can be blamed for a high voltage drop so the 400 V DC is not sufficient to generate 120V RMS output. The DC supply is limited to 400 V maximum; so, in order to test the voltage control, the reference signal's RMS value is reduced to 110V. The voltage controls were found to be working perfect as the reference RMS value was reduced to 110V. From the experimental results, as shown in Figure 3-11, it can be observed that the RMS value of the output voltage is very close to the reference RMS of 110V. The first channel in the screenshot shows the inverter output voltage and the second channel shows the load current for a 10 ohms resistive load. Also, from the harmonic analysis, provided by the Yokogawa scope, the voltage THD is around 5%.

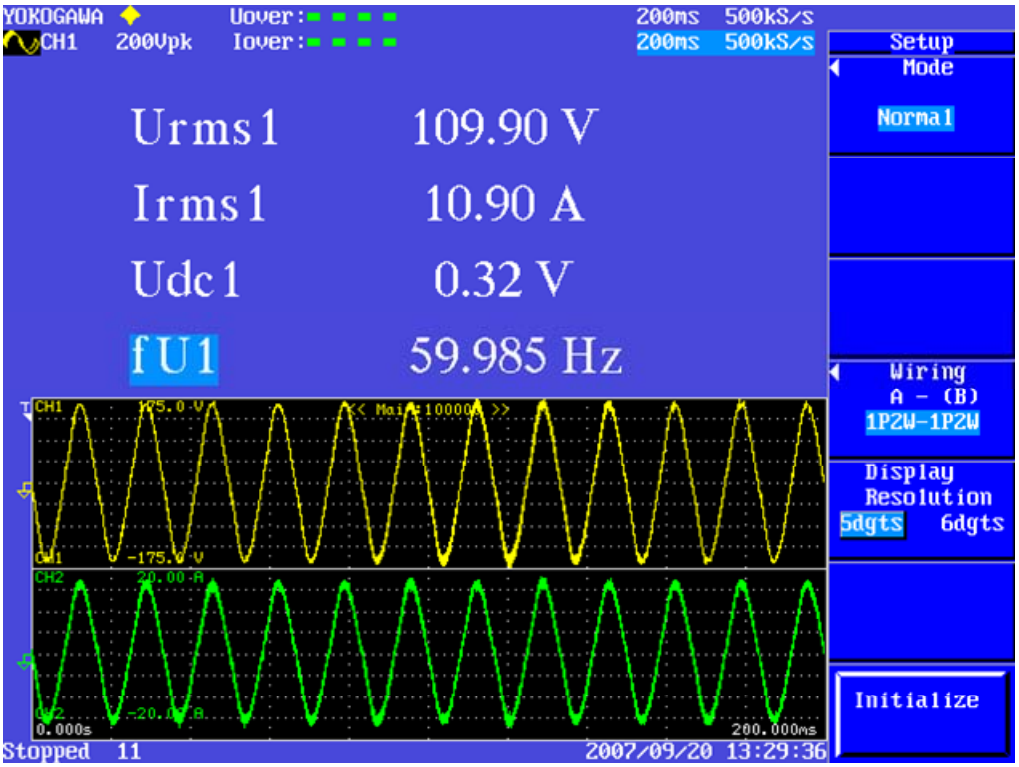


**Figure 3-11 Screenshot of Inverter Output Voltage and Load Current**

### *3.3.3 Current Control*

When the inverter is connected to the utility, the grid controls the amplitude and frequency of the inverter output voltage, and the inverter itself operates in the current control mode. It is still debatable whether an inverter should be allowed to regulate voltage during grid-connected operations. The existing IEEE 1547 Standard does not allow distributed generation to actively regulate voltage, but there is some evidence that active voltage regulation may have some positive benefit to the grid [12].

To test the current controlled mode of operation, it is necessary to make sure the current control loop is working before actually making utility connection. In this test setting, the inverter output terminals are shorted and, as in real grid connection, the grid resistance will is very small. This short is done by removing the California Instrument AC load bank and using a wire jumper to short the line and neutral terminals of the inverter output. To make sure that the short circuit is not harmful to the inverter switches, the current limit of the DC supply is set to a low value of 2 A, while the DC supply voltage remains at 400 V. First, the reference current is set to zero, then the system is turned on and the response is observed. When it is certain that the system is stable, the reference value is increased to a higher value of 15A. The experimental setup used for the current control test is shown in Figure 3-12.

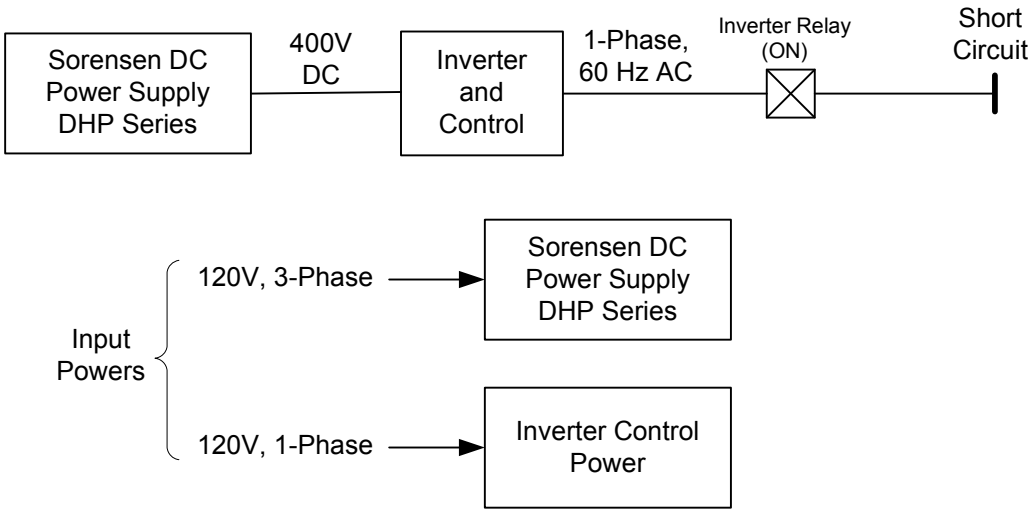


**Figure 3-12 Block Diagram of Current Control Test Setup**

The current control loop compares the inverter output current with the reference current and the error is used to change the duty cycle of the inverter switches using proportional control. During the duty cycle calculation, the output inductance values are also considered in order to find the voltage drops across them.

The results of the current control test are shown in Figure 3-13. The first channel in the screenshot the utility voltage and the second channel is the inverter output current. Though the system is not utility connected, the utility voltage is monitored and used to synchronize the inverter current. It is observed that the inverter output current is following the reference current ms value with a small steady state error. Additionally, the phase angle of the current reference is set to a $90^{o}$ lead with respect to the utility voltage and, as can be seen in Figure 3-13, the output current is tracking the phase angle.

Concluded from the harmonic analysis of the current waveform, the output current has high harmonic pollutions mainly in the form of third harmonics. Further investigation revealed that the SKAI module current sensors are 10% inaccurate with high noise content. The external current sensors that are present in the hardware are CT based. They are mainly for relay control and can be saturated by the DC components in current. Therefore, they are not good for control purposes. In the future, LEM Hall-effect current sensors will be included in the hardware to provide precise current control.

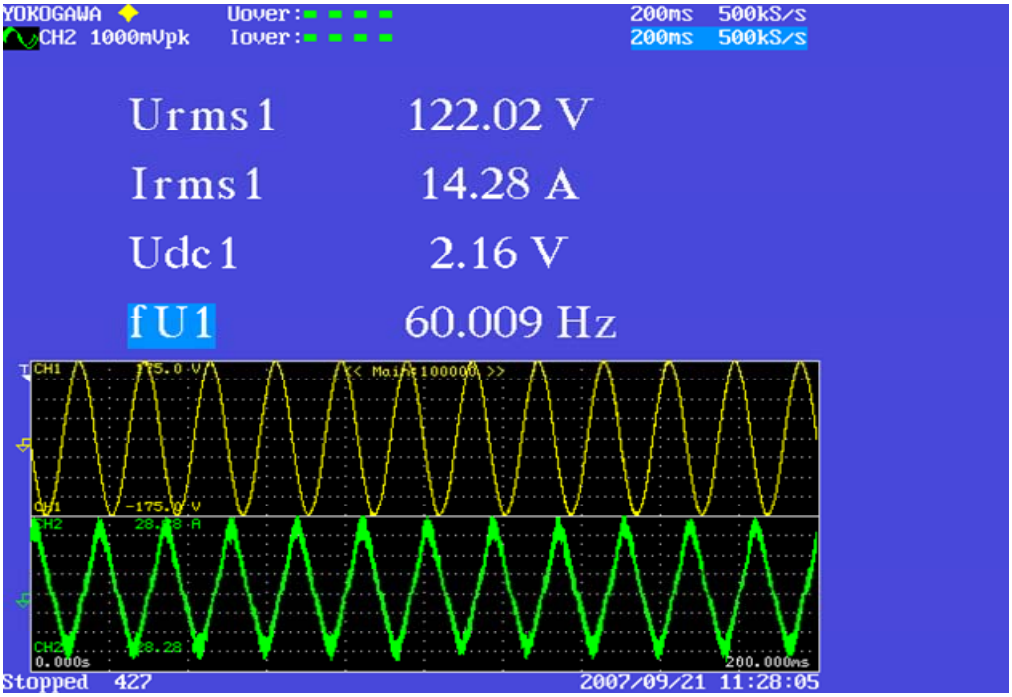


**Figure 3-13 Screenshot of Utility Voltage and Inverter Output Current**

Different phase angles were also imposed on the reference current with respect to utility voltage waveform and the inverter output current was observed. Figures 3-14, 3-15, and 3-16 show that the inverter output current is following the phase angle with considerable accuracy. In these three figures, the yellow curve shows the utility voltage and the green curve shows the output currents.

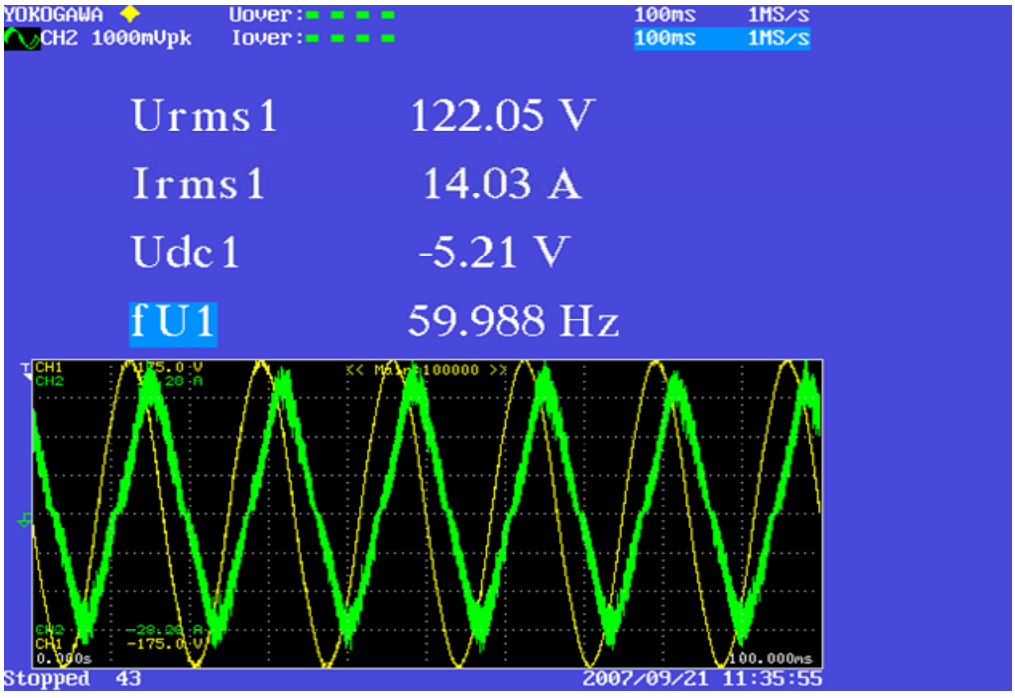


**Figure 3-14 Screenshot of Utility Voltage and Inverter Current (Current Lags by 60°)**

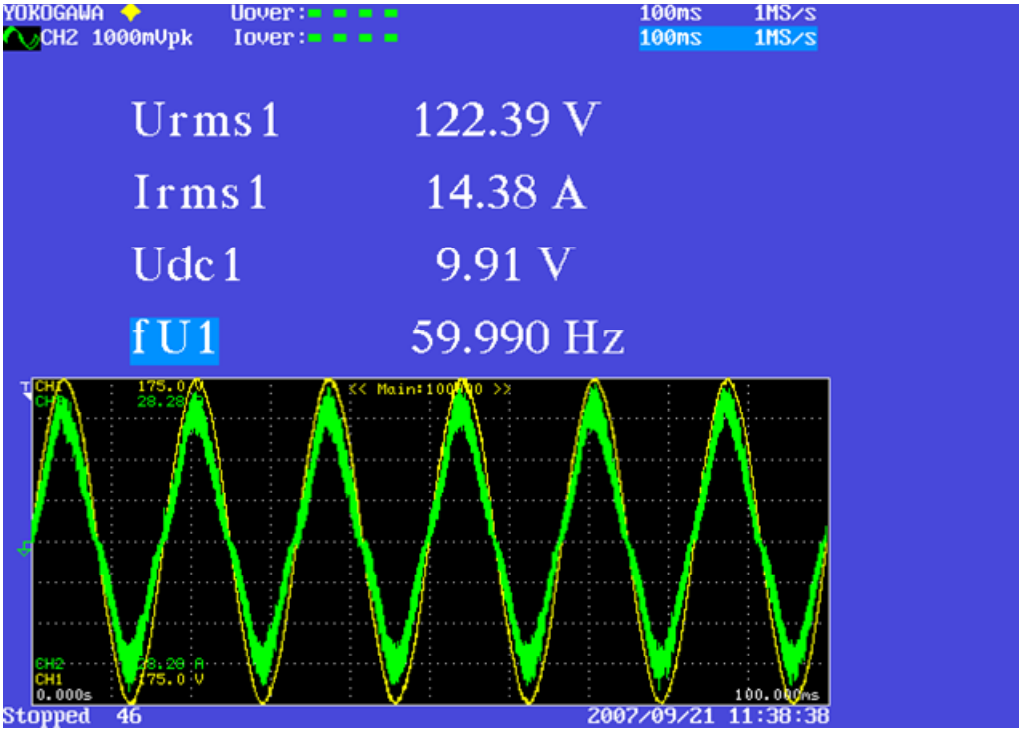


**Figure 3-15 Screenshot of Utility Voltage and Inverter Current (Current in Phase)**

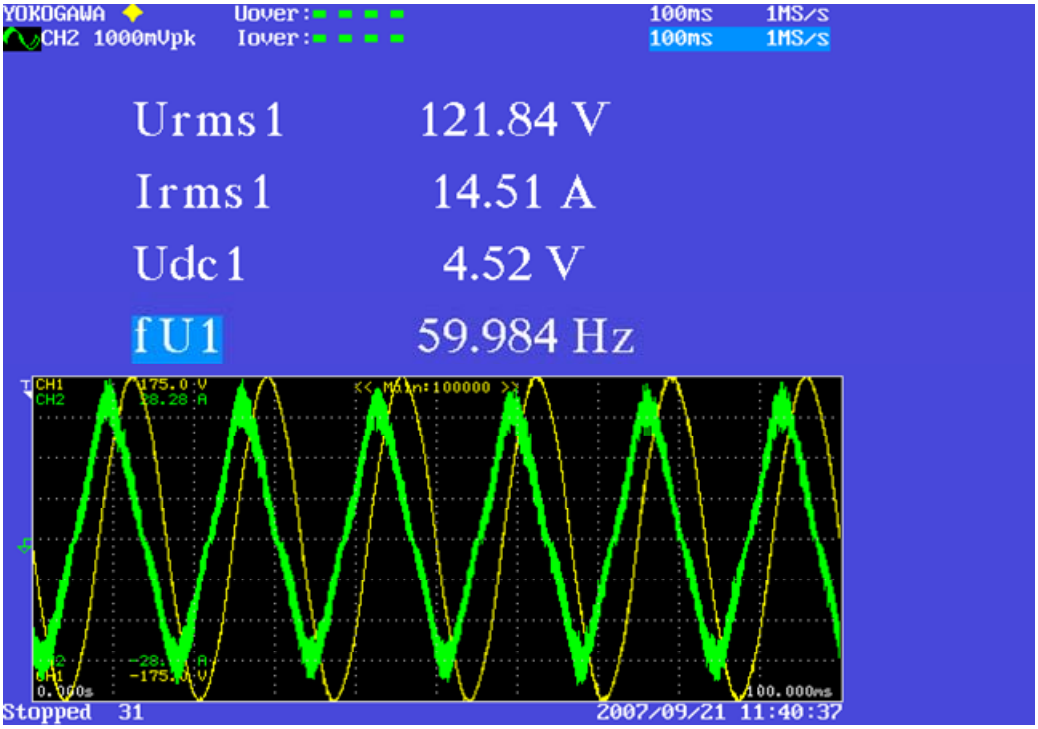


**Figure 3-16 Screenshot of Utility Voltage and Inverter Current (Current Leads by 60°)**

# 4 Modularity in Power Electronic Systems

## 4.1 General Description

Power electronics can account for up to 40% of the costs of a typical distributed energy system and are often the least reliable part in the entire system design. Therefore, from a commercialization perspective, the key business needs for distributed energy power electronics are reducing costs and improving reliability. Associated with these cost and reliability issues, three major technology challenges exist when discussing power electronics for distributed energy applications [13].

1. There is a lack of standardization and interoperability among power electronic components and systems. This increases the cost of manufacturability and reduces volume and reliability.
2. Power electronic devices must be modular and scalable. This will simplify applications and designs, leading to increased use; higher production volumes will lower costs and improve performance.
3. Current research focuses on power electronic subsystems and component rather than the DE system package. Improvements in the system package are greatest need for distributed energy.

The Power Electronic Building Block (PEBB) concept revolves around designing modular power electronics systems that integrate power devices, gate drives, and other components into functional blocks [14]. By integrating them into building blocks, a designer of these blocks addresses the device stresses, switching speed, switching losses, and thermal management with functional specifications that relate to the performance requirements of intended broad set of applications [14]. Adoption of functional building blocks that can be used for multiple applications could result in high volume production, reduced engineering effort, reduced design testing, and lower onsite installation and maintenance work for specific customer applications. The value of integration can be enhanced with standardization of interfaces of the building blocks, control, or protections requirements.

Power electronics devices have evolved tremendously from the familiar plastic package form toward the integration of more components into a module. The module package initially combined discrete switching devices to form a half-bridge, then evolved to include H-bridge circuits, three-phase bridges (six-packs), and, more recently, gate drives and sensors. IPEMs, such as the SKAI modules or the PM1000 by American Superconductor, have also recently entered the market [15]. In this approach, along with the power electronic devices, the DC-link filter capacitors, current and temperature sensors, gate drivers, heat sink, and the optional DSP controller are combined into a single, highly-optimized module [7]. The DSP based local controller can communicate with a higher level controller through different communication interfaces.

New IPEMs allow designers to use a building-block approach when designing APEIs, with software and wiring defining the function of each identical block. The versatility of the module for different applications also facilitates the economics of production. Additionally, because the module integrates many of the subcomponents, the user is getting a fully

integrated and tested package that is already qualified to meet some of the stringent specifications. [7]. All of the advantages of using IPEMs in power electronics design, make IPEMs exciting candidates for addressing the reliability, modularity, scalability, and standardization issues for the distributed energy applications.

## 4.2 Modular Power Electronics Topologies

Different distributed energy systems require various power electronics topologies for converting the generated power to the utility compatible power. The photovoltaic (PV) and fuel cell systems generate DC power that needs to be converted to single-phase or three-phase AC for utility connection. Additionally, an isolated DC/DC converter is often used before the DC/AC inverter in order to avoid bulky line frequency transformers for isolation and voltage boost. Wind and microturbine systems generate variable frequency AC output that needs to be converted into 60 Hz AC for utility connection. The use of back-to-back converters is the most efficient way to utilize the generated power. Typically, most internal combustion (IC) engines are interconnected to the utility through a fixed speed synchronous generator with protective relays. Using a power electronics interface with an IC engine offers the advantage of having variable speed operation of the IC engine, which, in turn, optimizes fuel usage for varying loads. A back-to-back voltage source converter is the most suitable choice for IC engine applications. Inclusion of storage in the distributed generation system actually provides dispatchability of its distributed resources—generally renewable energy sources with no dispatchability of their own, such as PV and wind. The stored energy can then be used to provide electricity during periods of high demand or low resource. Depending on the type of storage, power electronics converters are required for utility connection. The most unique aspect of power electronics for energy storage is that it must be bi-directional—taking power (during charging) and providing power (during discharge) from/to the grid. For battery energy storage systems, a bi-directional DC/DC converter followed by a DC/AC inverter is the most general choice, whereas for the flywheel system a back-to-back converter can be utilized for utility connection. A diagram showing the use of IPEMs with different distributed generation systems is given in Figure 4-1. IPEMs, as discussed in Section 3 of this report, is the basic building block for all these topologies. The inherent advantages provided by the IPEM are shorter time to market; easier system design and assembly; reduced number of components; economical and standard interface design; and reliability.

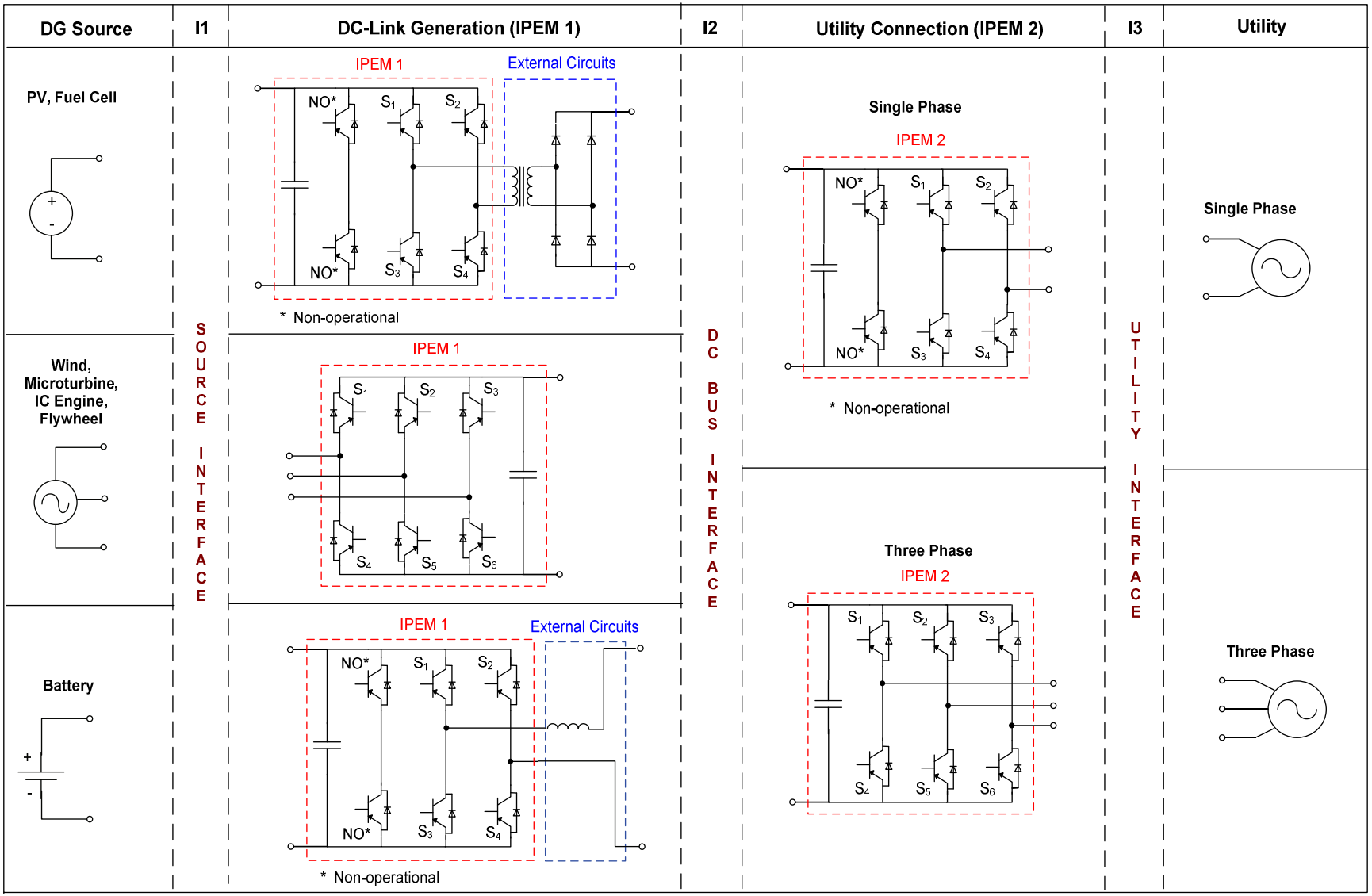


**Figure 4-1 Generalized IPEM Based Power Electronics for Different Distributed Energy Systems**

In Figure 4-1, two IPEMs are used for the distributed energy systems. Each IPEM includes six IGBTs along with gate drivers and sensors. In some cases, additional hardware components are required for designing the converter. Additionally, three power interfaces (I1-I3) that are essential to the operation of the complete system are shown in Figure 4-1. The source interface for such systems typically consists of EMI filters, and the utility interface includes the line frequency filters. The DC bus filter may also be required if the capacitor inside the IPEM is not sufficient. The DC/AC inverter can be single-phase or three-phase depending on the utility connection type.

The most generalized form of power electronics topology for the PV and fuel cell system is the DC/DC converter with an embedded high frequency transformer along with the DC/AC inverter as shown in Figure 4-1. In both of these applications, the IPEM-based solution is not optimal, as one-third of the switches are not used in the H-bridge configuration. However, the IPEMs offer cost savings due to the commonality of the hardware and short development time for the system [7].

For sources like wind, microturbines, and IC engines that generate variable frequency AC, the most generalized and versatile power electronics topology is the back-to-back rectifier/inverter connection, which provides improved power flow control and increased efficiency. The voltage-fed converter scheme used in such a system is shown in Figure 4-1. The same topology can be used with the flywheel energy storage system as the back-to-back converter scheme is inherently bi-directional. In these power electronic topologies, line frequency transformers are often included in the utility interface for galvanic isolation.

For the battery energy storage system, the most generalized form of power electronics topology is the bi-directional DC/DC converter cascaded with the DC/AC inverter, as shown in Figure 4-1. The full-bridge DC/DC converter can operate with any voltage and current polarity. The voltage polarity and amplitude can be set irrespective of the current direction to provide bi-directional power flow [2]. In this topology, a line frequency transformer is often included in the utility interface for galvanic isolation.

Based on the power electronics topologies, as shown in Figure 4-1, controllers can be designed for the APEI systems. These control functions are implemented for the APEI systems either by using the local DSP controller or by utilizing the higher level controller and the communication. An example of the higher level control functions (such as VAR control) can be found in Section 2 of this report, and the design of the local DSP controller for basic voltage and current control of the utility connected inverter can be found in Section 3.

## 4.3 Requirement of Standard Interfaces for Power Electronics

In traditional centralized digitally controlled power electronics systems, construction, debugging, and maintenance of the power electronics systems are complicated and difficult due to a lack of standardization and modularization and a strong dependence of control design on system hardware. The PEBB concept provides a way to hardware standardization of power electronics systems, including power flow and the signal distribution network, which, in turn, allows for an open architecture distributed controller approach. Standardization of the communication interface would allow partitioning of the power electronics into flexible, easy-to-use, multifunctional modules or building blocks that can

significantly ease the task of system integration. By using control software that is functionally divided into hierarchical levels and by standardizing interfaces between levels, the application software becomes independent of the hardware specifications of power stage; as long as supporting the standardized interfaces between levels, products from different vendors can communicate and work with each other [16]. Furthermore, if both sides of an interface support device self-identification and system resources assignment, then the so-called plug-and-play implementation is feasible for future APEI systems.

### *4.3.1 Power Interfaces*

A simplified block diagram of the power electronics for the different distributed energy systems is shown in Figure 4-2. The following characteristics should be made available for designing the standardized power circuits.

- Each IPEM should have two ports; one named DC Port and the other named AC Port.
- Both ports are to be bi-directional and should be able to work as buck or boost mode.
- Device ratings for the IPEMs are limited by manufacturer datasheet. Paralleling of the converters is necessary for high power applications.
- The wiring should be based on the operational power.
- Filters, transformers, and other external circuit designs should be dependent on the operational power. It is always possible to design the circuit for higher power and use it for low power applications, but obvious drawbacks will be inefficient design and higher cost.
- For single phase applications, the utility connected IPEM (i.e. IPEM 2) should only use four switches. However, the IPEMs offer cost savings due to the commonality of the hardware and short development time for the system.
- Combining multiple sources and/or storages should be done using the DC bus. In such case, a single IPEM should be used for DC/AC inversion [17].

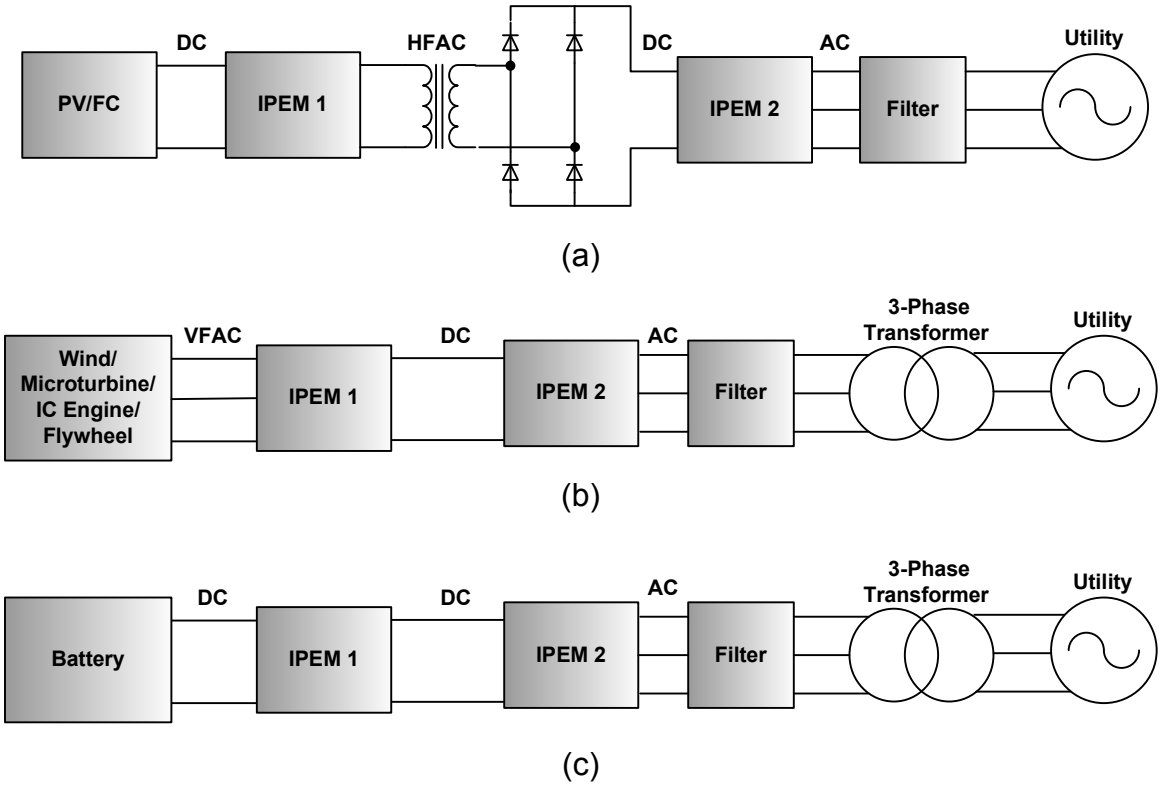


**Figure 4-2 Block diagrams of Power Electronics for (a) DC Sources, (b) Variable Frequency AC Sources and Storages, (c) DC storages**

### *4.3.2 Control Interfaces*

Control of today's medium and high-power converters is primarily based on a centralized digital controller with several drawbacks. One drawback is the large number of point-to-point signal links that connect power stage and sensors on one side with the centralized controller on the other [18]. Additionally, the signals in typical power electronics systems are of different formats and are transmitted through a variety of physical media. This makes the standardization and modularization of power electronics systems and subsystems very difficult [18].

For the modular design of the power electronics for distributed generation applications, the control of the power electronics system can be functionally divided into hierarchical architecture as shown in Figure 4-3. The hardware level controller, which is the inherent part of the IPEM, is defined as a local controller. In literature, it is often called a hardware manager [18], [19]. The higher level controller is defined as the application manager. This is the controller external to the IPEM that establishes the functions that are the main mission of the power electronics system. In order to achieve the goals required at the system control level some standard control functions must be performed inside applications manager. If more than one application is combined, i.e. a hybrid system with different distributed energy sources, a higher level system manager is required that coordinates the operation and maintains the system data bus for communicating with the individual application managers.

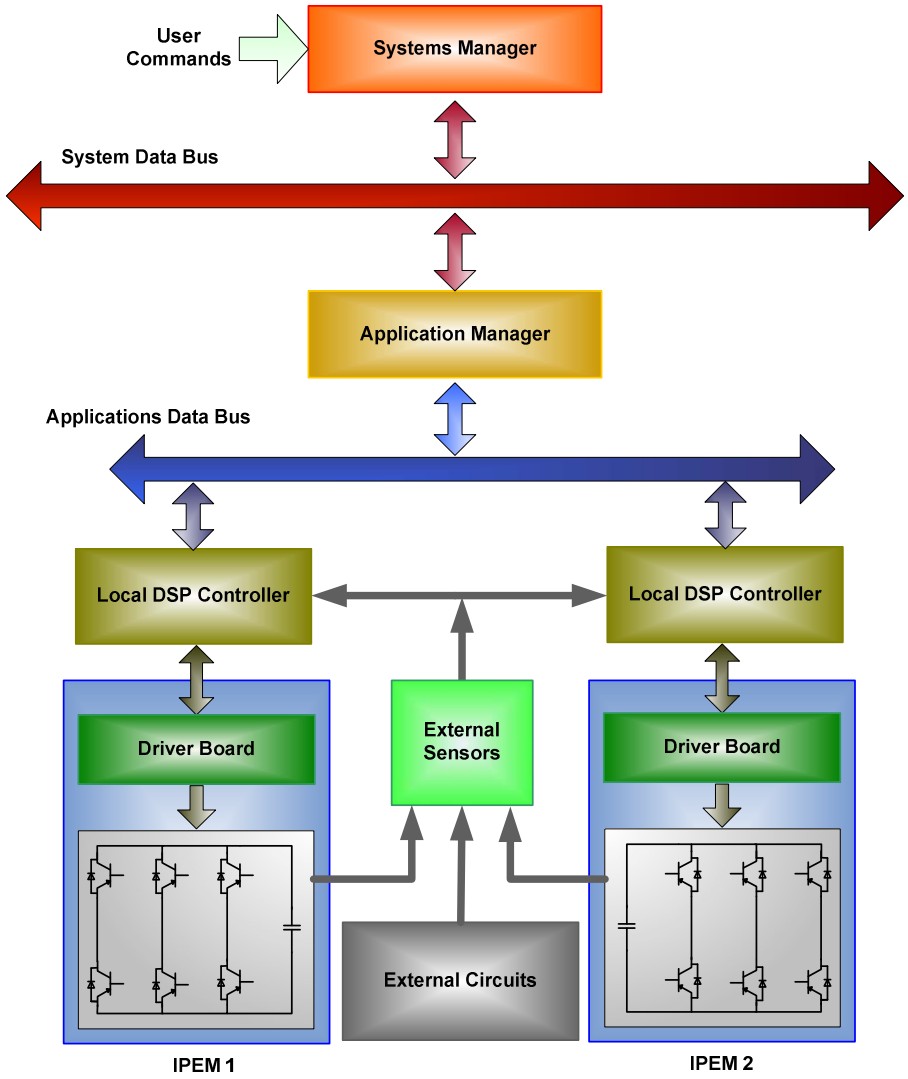


**Figure 4-3 Hierarchical Division of Control Functionality for IPEMs**

The local controller is designed to provide control and communication functions for the IPEM it is associated with. It is designed to support all module specific control tasks, making the module specific functions (such as soft switching) invisible to the application manager. As the DSP modules provide enough calculation capabilities, it is preferred to carry out the voltage and current control inside the local controller in addition to the PWM generation for the switches. From a generalized evaluation of different converters, it can be found that there is a set of common functions shared by all of them and also these common functions are related to the lower levels [19]. For distributed energy applications, the PWM generation at the lower level is always related to either voltage or current control for the particular converter. For this reason, it is desirable to achieve these controls inside the local controller to make the system more modularize.

In addition, the local controller can be used for over-current protection and indication; current, voltage, and temperature sensing with A/D conversion; and communication of

PWM, status, and measurements. Some IPEM manufacturers also offer the IPEM with a built-in DSP controller, which provides greater compactness in design. In such cases, the interface for the local DSP controller is limited by the manufacturer's specification.

The application manager is the external controller establishes the functions that are the main missions of the power electronics system. For example, in microturbine applications, the power circuit consists of two IPEMs connected in back-to-back formation having a common DC bus. The application manager operates the individual local controllers in such a way that the source IPEM (IPEM 1) works for DC link voltage control and the utility IPEM (IPEM2) controls the power flow to the grid. In order to achieve these goals required at the system control level, some standard control functions must be performed by the application manager. The application manager controls the local controller through standard interfaces. It also controls the communications data bus for the local controllers.

The top level system manager performs the controls tasks at the system level, such as responding to users' commands, coordinating performances between different applications, and monitoring system execution. Additionally, the system manager can also be utilized to determine the mode of operation for each of the distributed energy system individually so that the issues related to islanding and energy cost optimization can be resolved.

The input-output signals and control interfaces for a typical IPEM hierarchical controller are summarized in Table 4-1. For the IPEM in this table, it is assumed that the local DSP controller is outside the power electronics module and is connected to the power electronics module through a D-sub 25 pin connector with ribbon cable. Furthermore, it is assumed that the external sensors are connected directly to the local controller's analog input ports. The connection between the local controller and the applications manager is assumed to follow typical IPEM manufacturers CAN interface [15]. But different open architecture communications protocols can also be used, as will be discussed later. Both the system manager and application manager is developed in CPU and named as external controllers in the table. All the measurement signals are routed to the external controllers via local controller.

**Table 4-1 Input-Output Signals and Control Interfaces of a Hierarchical Controller in an IPEM**

| IPEM | Interface 1 | Local Controller (LC) | Interface 2 | External Controllers (EC) and External Sensors (ES) |
|---|---|---|---|---|
| Inputs:<br>• PWM signals (5V CMOS level)<br>• Enabling signals<br><br>Outputs:<br>• DC bus voltage<br>• Phase currents<br>• Heat sink temperature<br>• Fault signals<br>1. Excessive switch current<br>2. Phase over-current<br>3. DC bus over-voltage<br>4. Power supply under-voltage<br>5. Over-temperature at heat sink | ⟺<br>D-sub 25 pin connector with ribbon cable | Inputs:<br>• Phase currents<br>• Phase voltages<br>• DC bus voltage<br>• Heat sink temperature<br>• Relay sense signals<br>• Encoder inputs<br>• Zero-crossing detection<br>• Fault signals from IPEM<br>• System operation mode signals from EC<br>• Protection signals from EC<br><br>Outputs:<br>• Gate drive PWM signals<br>• Communication signals for IPEM<br>• Enabling signals to IPEM<br>• PWM status signals to EC<br>• Fault signals for EC | ⟺<br>Measurement signals from sensors to analog input of DSP<br><br>⟺<br>Control signals from external controller by CAN or asynchronous serial | Inputs:<br>• Measurement signals from LC<br>• Measurement signals from ES<br>• Encoder signals<br>• Fault signals<br>• User Inputs<br>• PWM status signals<br><br>Outputs:<br>• Reference voltage and current signals to LC<br>• Communication signals for external data bus<br>• Relay contactor signals<br>• Protection signals to LC<br>• System operation mode signals to LC |

The communication between the IPEM and local DSP controller is obtained through a D-sub 25 pin connector with ribbon cable. If the DSP controller is inside the IPEM, this communication interface is not available to the user. The application manager and the system manager are generally implemented in CPU. The communications between the local controller and the CPU is typically achieved by CAN or asynchronous serial using fiber optics. From [19], it can be observed that the bandwidth of the analog type signals depends on number of signals; switching frequency; and number of bits representing the duty cycle. Analog signals that are not directly related to the switching frequency may require a lower bandwidth. On the other hand, the channel bandwidth requirement for the digital type signal depends on number of signals; ratio of sampling period to transmission time; sampling frequency; and number of bits representing the variables. In most of the APEI applications, the CAN communication is sufficient for data transmission as it can support up to 1 Mbit/s bit rate at network lengths below 40 meters. But using IPEMs for other type of applications such as active filtering may require new communication protocols as described in [18], [19].

### 4.4 Modularity in the NREL Inverter Platform

The NREL inverter platform is built with modularity and flexibility in mind. The integrated power electronic modules with IGBTs are used for the power circuit, while the DSP based controller is designed to facilitate the universality of the hardware platform. The design tries to standardize the components and interfaces so that a wide range of voltage and current settings can be tested using the same platform. Currently, the main goal is to test the control and protection objectives for the utility connected inverter. As this work progresses, the use of the same platform can be extended for integration of the distributed energy into the utility. In such case, another SKAI module has to be installed and connected to the inverter platform in back-to-back converter configuration. The new SKAI should have its own local DSP controller so that the distributed energy connected converter can be operated per the requirements of that particular distributed source. The higher level external controllers are also required to coordinate between two IPEMs and their local controllers. As the IPEM technology evolves, the possibility of having both the converters inside a single IPEM will reduce the size and complexity of the APEI systems and will provide greater modularity and flexibility.

## 5 Conclusions

In this report, a PSCAD-based model of a generic, single-phase inverter platform is presented. The basic circuit operations and the control functions are described. The inverter operates in both utility connected and stand-alone modes and the model validates methods to ensure the smooth transition between them. Some interesting simulation results are given to show the effectiveness of the model in controlling the power flow by the inverter in the utility connected mode, as well as the voltage and frequency control in the islanded mode of operation.

A generic hardware platform is built in parallel to the modeling initiatives for practical verification of the APEI operations. The inverter design includes IPEMs with DSP based controls to ensure modularity and flexibility of the system. After completion of the hardware

development and construction of the inverter platform, basic functionalities are tested. Simple initial experiments are designed to verify the operation of the voltage control when the inverter is supplying an AC load. To test the current controlled mode of operation, it is necessary to make sure the current control loop is working before actual utility connection is made. In this test setting, the inverter output terminals are shorted and, as in real grid connection, the grid resistance will is very small. Though the controls are not perfect yet, with some existing issues in terms of steady-state errors and noises, the experimental results are promising for testing more complicated control and protection in the future.

The future scope of this work will evolve into developing advanced controls and protections for the power electronics interfaces associated with distributed applications to provide increased functionality (such as improved power quality, voltage/VAR support), compatibility (such as reduced distributed energy fault contributions), and flexibility (such as operation with various distributed energy sources). This will, in turn, facilitate the development of APEIs that are efficient, cost-competitive, and have substantially faster response times than conventional technologies.

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Power electronics devices hold substantial promise for making distributed energy applications more efficient and cost effective. This project is motivated towards developing and testing inverters that will allow distributed energy systems to provide ancillary services such as voltage and VAR regulation, and increased grid reliability by seamlessly transitioning between grid-tied and stand-alone operation modes. The objectives of this project are to identify system integration and optimization issues and technologies and to provide solutions through research, analysis, and testing of power electronic interfaces for distributed energy applications that are cost-competitive and have substantially faster response times than conventional technologies. In addition, the testing of power electronics interfaces will develop a technical basis for performance assessment for distributed energy systems, subsystems, and components that will finally create a foundation for standardized measurements and test procedures. The ultimate goal for this research is to advance the potential benefits of distributed energy to provide ancillary services, enhance power system reliability, and allow customer choice.

**15. SUBJECT TERMS**
Distributed energy; power electronics; inverter; inverter circuit; integrated power electronics module; voltage control; modularity; power electronics building block; PSCAD

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