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Ge Interface Engineering with Ozone-oxidation for Low Interface State Density

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***Abstract*— Passivation of Ge has been a critical issue for Ge MOS applications in future technology nodes. In this letter, we introduce ozone-oxidation to engineer Ge/insulator interface. Interface states (D_{it}) values across the bandgap and close to conduction bandedge were extracted using conductance technique at low temperatures. D_{it} dependency on growth conditions was studied. Minimum D_{it} of of $3x10^{11}$ cm^{-2} V^{-1} was demonstrated. Physical quality of the interface was investigated through Ge 3d spectra measurements. We found that the interface and D_{it} is strongly affected by the distribution of oxidation states and quality of the suboxide.**

***Index Terms*—Germanium, oxide, surface passivation, interface state density extraction**

I. INTRODUCTION

Future CMOS scaling requires introduction of new channel materials and innovative device structures [1]. Ge has been considered as a promising candidate as channel material for future technology nodes because of its lower effective conductivity mass. However, passivation of Ge interface has been a critical challenge. Direct formation of a high-k dielectric on Ge has not given good results in the past. Many attempts have been made with different high-K dielectrics including HfO_2 [2], ZrO_2 [3], Al_2O_3 [4], $LaAlO_3$ [5] to find a suitable passivation for Ge. Mobilities above $300cm^2V^{-1}s^{-1}$ have been reported for Ge PMOS while Ge NMOS in the past exhibited poor drive current and low mobility by several demonstrations worldwide [6,7]. Better characterization and understanding of interface traps is required. Also, a good quality interface layer is required before the deposition of a high-K dielectric to improve PMOS performance and to solve Ge NMOS problem.

Although Ge is a column IV semiconductor like Si, it behaves different from Si when oxygen or hydrogen reacts with its surface. The electrical quality of Ge interface is strongly affected by the oxidation states. Therefore, understanding the early stages of oxidation is important to control the Ge interface. Ge has a smaller bandgap than Si. Therefore interface trap time constants are much shorter, which makes density of interface states extraction more complicated than Si. Conventional D_{it} extraction methods can not be directly applied to Ge. In this work, we show that Ge interface can be improved and D_{it} can be reduced by controlled ozone oxidation. Also, conductance technique at low temperatures can be used to get accurate distribution of D_{it} across the bandgap of Ge.

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II. EXPERIMENT

Direct formation of a high-k dielectric on Ge has not given good results in the past [2-5]. A good quality interface layer is required before the deposition of a high-K dielectric. Ozone oxidation can be helpful in thermal oxidation of Ge at lower temperatures because ozone is more reactive than oxygen. Also it has been shown for Si that ozone oxidation at lower temperatures results in lower density of intermediate oxide states [8]. We have investigated Ge/GeO_2 interface using ozone oxidation of Ge. MOS capacitors (MOSCAPs) were built on n-type Ge substrates with (100) surface orientation. Ge wafers were thermally oxidized with ozone at 15torr in 200-450°C range to form passivating interlayer. Oxidation was followed by depositions of two different dielectrics. On some wafers LPCVD SiO_2 was deposited at 300°C followed by Al sputtering and photolithography to make the MOSCAP patterns. On other wafers HfO_2 was deposited by ALD at 150°C with precursor tetradiethylaminohafnium (TDEAH) and Pt was evaporated using shadow masking to form the gate electrodes.

III. RESULTS AND DISCUSSION

In the MOS capacitor study, to target Ge NMOS problem we focused on n-type substrate and measured D_{it} in the upper half of the bandgap. D_{it} distribution for various samples is shown in Fig. 1.Conductance method is a reliable way to extract D_{it} but it can not be directly applied to Ge. At room temperature, due to thermal generation and weak inversion response, conductance doesn't show typical interface trap behavior. Time constants for capture and emission processes of carriers through interface traps are much shorter for Ge than for Si, due to smaller bandgap. Hence, the conductance was measured in the temperature range of 77-250K, to determine D_{it} distribution across the bandgap, including close to bandedges. Measurements at several temperatures in the range of 77-250K allow sampling of the D_{it} distribution within the bandgap because each temperature monitors a limited part of the bandgap as pointed out in Fig. 1. D_{it} distribution shows a minimum close to midgap and increase closer to the bandedge as expected theoretically. Minimum D_{it} of $3x10^{11}$ $cm^{-2}V^{-1}$ is obtained for samples oxidized at 400°C, both with LTO and HfO_2 as top dielectric. These numbers are the lowest reported for Ge and are similar to the reported values for high-k dielectrics on Si. Asymmetric D_{it} distribution or higher D_{it} close to the conduction bandedge was reported previously for different pasivation techniques like thermal GeON [9] and silicon

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passivation [10]. In our samples with GeO_2 passivation, we didn't observe that trend in D_{it} distribution.

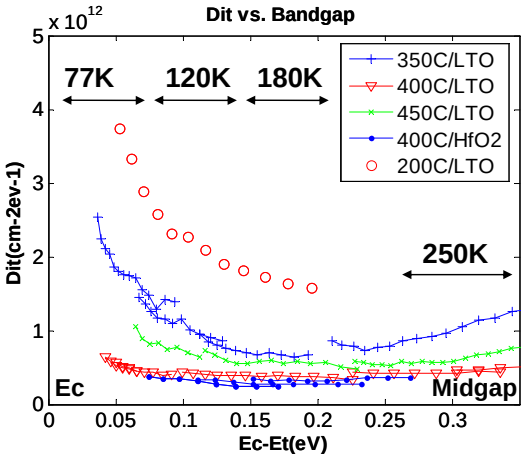

Fig. 1: D_{it} distribution for samples ozone-oxidized in 200-450°C range is shown (legend). Legend shows ozone oxidation temperature and the insulator deposited at the top of grown GeO_2. N-type Ge substrate is used to cover upper half of the bandgap. Minimum D_{it} of $3x10^{11}cm^{-2}V^{-1}$ is obtained for samples grown at 400°C. At different temperatures, traps at different parts of bandgap respond. So conductance is measured 77,120,180 and 250K to cover the bandgap.

Oxidation can result in various Ge suboxide (GeO_x) states which can strongly affect the electrical quality of the interface. Controlling the early stages of oxidation is important to engineer the GeO_x layer. The quality of Ge interface passivation strongly depends on oxidation conditions, pressure and temperature since they affect the surface bonding. D_{it} dependency on oxide growth temperature is shown in Fig. 2. Dependency of D_{it} values on oxide growth temperature, measured at midgap and conduction band edge, is shown in Fig. 2. Samples oxidized at 400°C show minimum D_{it} at the midgap and the bandedge. For growth temperatures lower or higher than 400°C, D_{it} increases. Comparison of the electronic structure and distribution of intermediate oxidation states can be useful to understand passivation issues and also to investigate the reason for the growth temperature dependency in Fig. 2.

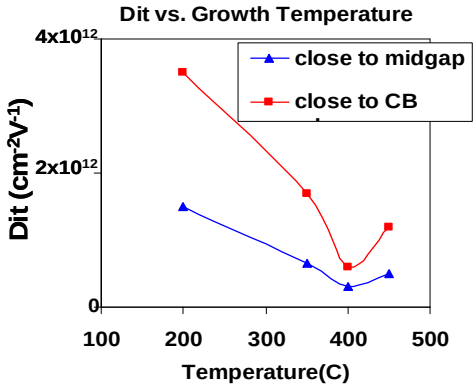

Fig. 2: D_{it} dependency of oxide growth temperature is shown.

Obtaining higher oxidation states requires energy to break more Ge bonds, which can be supplied by thermal energy or activated oxygen. Therefore, use of ozone at appropriate temperatures can favor the formation of higher oxidation states. The synchrotron radiation photoelectron spectroscopy measurements are done on various samples and Ge 3d spectra are examined at 400eV bem energy to find the distribution of oxidation states. As shown in Fig. 3, the intensity of spectral component due to dioxide species increases with oxidation temperature while the intensity of the peak due to suboxide species (GeO_x) decreases. This results in a shift of the overall oxide peak towards higher binding energy. Also, DI water etch removes the higher binding energy oxide peak, confirming that the grown oxide is GeO_2, which is soluble in water.

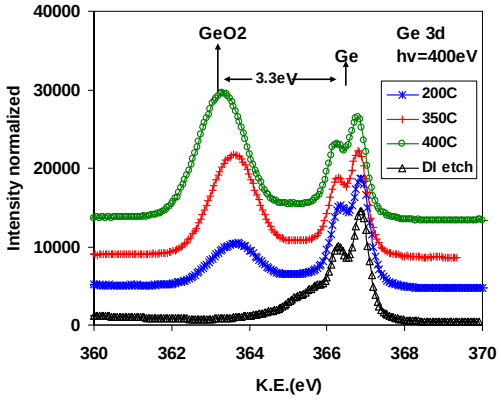

Fig. 3: Ge 3d spectra obtained with synchrotron radiation at 400eV are shown. The shift of oxide peak towards GeO_2 as increasing growth temperature indicates the increase in the rate of higher oxidation states. 3d spectrum after DI water etch of 400°C sample confirms that grown oxide was GeO_2.

Decomposing the oxide peaks into oxidation states [11] it is found that oxide grown at 400°C (as compared to lower temperatures) has less intermediate oxidation states and more 4+ state (Fig 4). Sample prepared at 350C showed higher emission from 3+ state besides 1+ and 2+ states than the sample prepared at 400°C. The process of obtaining higher oxidation states is competing with the stability of 2+ state. So at higher temperatures like 400°C, no emission from 3+ is observed because the reaction at the interface favors 4+ states. As the contribution from higher oxidation states increase and intermediate oxidation states suppressed, optimum passivation and D_{it} is reached. This occurs at 400°C for ozone oxidation of Ge. At higher temperatures, transformation of GeO_2 (4+ state) to GeO (2+) state occurs at the interface [12],

$GeO_2 + Ge \rightarrow 2\ GeO$

which causes increase in D_{it} (Fig 2, for 450°C). The difference between the reaction with oxygen of Ge and Si interfaces can be explained as follows: For Si, only 4+ oxidation state is stable among four oxidation states and the suboxides are easily converted to SiO_2 with annealing. On the

other hand Ge is known to form GeO as well as GeO_2 (Ge in 2+ and 4+ oxidation states respectively). Annealing of Ge favors 2+ state. This behavior is different from Si where it easily forms SiO_2. At ~420°C desorption of GeO from the interface takes place, leading to an increase in D_{it}.

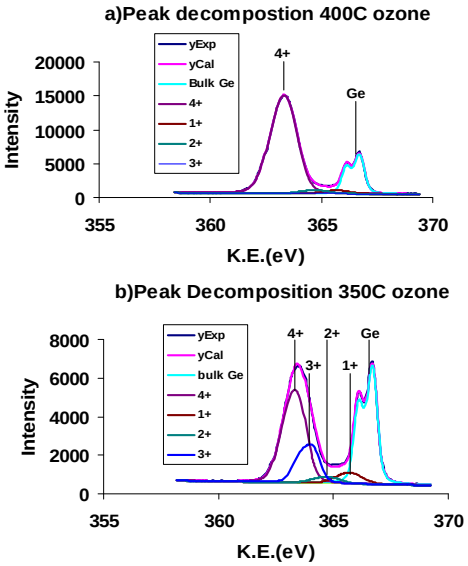

Fig. 4: Ge 3d spectrum is measured and fitting analysis are done. Main oxide peak and interfacial oxide is decomposed to oxidation states. Intensities are compared to bulk Ge peak. Oxide grown at 400° C has mainly 4+ state and less intermediate states while oxide grown at 350° C has significant 3+ state and other intermediate states.

IV. CONCLUSION

A new technique to passivate the interface of Ge using thermal oxidation in ozone prior to a dielectric deposition has been developed to improve CMOS performance. D_{it} distributions over the bandgap and close to band edges were extracted using conductance technique at low temperatures to avoid short time constants for capture and emission processes of carriers through interface traps due to smaller bandgap of Ge. A minimum D_{it} of $3x10^{11}$ cm^{-2} V^{-1} was obtained for samples oxidized at 400°C in ozone ambient, which is in the range of state-of-the-art Si/High-K dielectric interface quality. Lower or higher oxidation temperatures showed increase in D_{it} values due to formation of Ge suboxide (GeO_x) states. Incorporation of optimized oxidation of Ge surface should further improve the current transport in Ge FETs.

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