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X-Ray Active Matrix Pixel Sensors based on J-FET Technology Developed for the Linac Coherent Light Source

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[M]***Abstract*–An X-ray Active Matrix Pixel Sensor (XAMPS) is being developed for recording data for the X-ray Pump Probe experiment at the Linac Coherent Light Source (LCLS). Special attention has to be paid to some technological challenges that this design presents. New processes were developed and refined to address problems encountered during previous productions of XAMPS. The development of these critical steps and corresponding tests results are reported here.**

I. Introduction

X-ray Active Matrix Pixel Sensors (XAMPS) are currently under development for the Linac Coherent Light Source (LCLS). In particular, the sensor is intended to support the X-ray Pump Probe experiment (XRPP) [1]. Ultra-short (100 fs at 120 Hz) pulses from the LCLS will be used to probe the transient state of matter excited by using a fast optical laser. Depending on the experiment needs, X-ray absorption and emission or X-ray scattering and diffraction will be recorded. These last two measurements will require an area detector. The characteristics of the XRPP instrument demand extremely challenging specifications: 1) a readout noise better than 1 photon, 2) 10^4 photons full-well and 3) readout time of a few milliseconds. XAMPS, originally conceived for protein crystallography, can meet these requirements. In fact, it is fully efficient at the energy of interest (8keV). It has 100% fill factor, low noise, fast readout, single photon sensitivity and a dynamic range of more than 10^4 photons.

The XAMPS is a position sensitive ionization detector made on high resistivity n-type silicon typically ~400µm thick [2, 3]. It consists of a pixel array detector with integrated Junction Field Effect Transistor (JFET) switches. Pixels are isolated from each other by a potential barrier formed by a narrow deep boron implant. The device is fully depleted by applying a high negative voltage bias (~ -200V) to the p-n junction on the entrance window side of the device. When the photon is absorbed, the generated electron charge (~2200 electrons for an 8keV photon) is drifted to the exit side of the device and collected by a floating electrode (phosphorus implant) of the pixel that is the source of the JFET. Thus, the charge is stored on the capacitor consisting of this phosphorus implanted region that occupies most of the pixel area, a dielectric layer (SiO_2) covering it, and a metalization layer on top of the dielectric layer (Fig. 1 and Fig. 2).

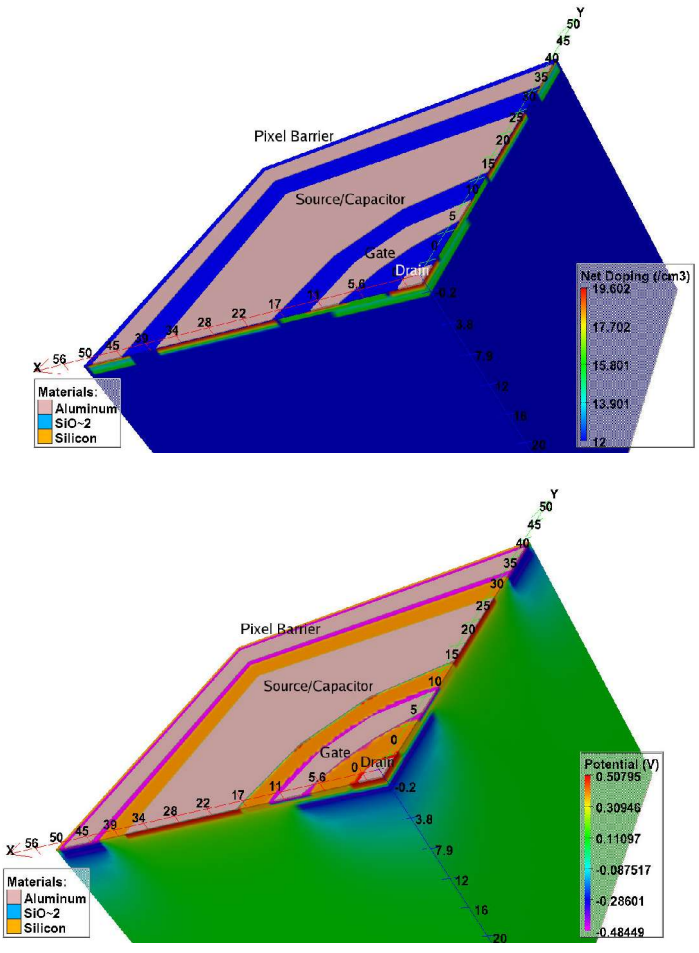

Fig. 1. Results from SILVACO - ATLAS simulations. 3D view of a pixel section. This structure, showing the net doping (top) and built-in potentials (bottom), has the same implants as the actual device but is much thinner to reduce the complexity of the simulations.

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During the data accumulation phase (charge drifting, collection, and storing), the gate of the JFET is biased to keep the transistor in a high resistance (off) state. During the data readout phase, the JEFT gate is biased to switch the transistor to low resistance (on). The stored charge thus flows to the drain that is connected to readout lines. A deep boron implant prevents any charge from flowing directly from the bulk to the drain.

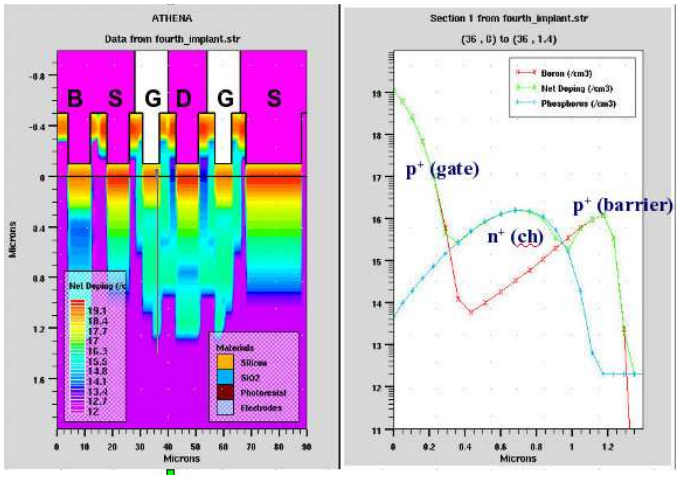

Fig. 2. Results from SILVACO - ATHENA simulations. 2D (left) and 1D (right) cross sections. This structure shows the implants as simulated with the processing simulation tools.

II. Simulation and results

Processing and device simulations were performed using the SILVACO simulation tools. In terms of processing development, it offers the possibility of simulating most fabrication steps before the start of actual detector processing. The results of these simulations constitute an estimation of the starting process parameters.

The structure resulting from the process simulation is usually simulated as working device allowing a close feedback between fabrication and operating conditions.

The full pixel structure of XAMPS was simulated and some results are reported in Fig. 3. The figure shows a 2D cross section with electron concentration for the two switch's conditions, open and closed with the device fully depleted.

III. Fabrication

The first prototypes are made on 100mm wafers and this format allowed the production of XAMPS of different sizes up to 512 x 512 pixels; each pixel is 90µm x 90µm. The final detector specification for the XRPP detector is an XAMPS containing 1024 x 1024 pixels and built on 150mm wafers. A few key technological steps had to be implemented to address some problems experienced during the production of the previous XAMPS. The main issue was achieving good contacts through small features and small diameter vias in the oxide layers, that is the contact between silicon and the first metalization layer (Al/Si contact) and the contact between the two metalization layers (1st Al/2nd Al).

A combined strategy adopting Reactive Ion Etching (RIE) and back-sputtering has been applied. The RIE improves the lithographic resolution and removes the oxide remaining after the previous steps of wet etching (~100nm SiO2), while the back-sputtering, performed immediately prior to metalization, in the same machine used for the sputtering of the metal contact, ensures that any native oxide regrowth is removed from the silicon-aluminum interface. Both processes have been extensively characterized in terms of etching rate and uniformity and the parameters resulting from these studies used in the production.

The RIE and the sputtering processes inevitably introduce excess charge accumulation in the oxide film, which must be removed for correct device operation. Rapid Thermal Process (RTP) has been used for annealing of the damage and has produced very good results, bringing the oxide charge density back to the initial as-grown levels (Fig. 4).

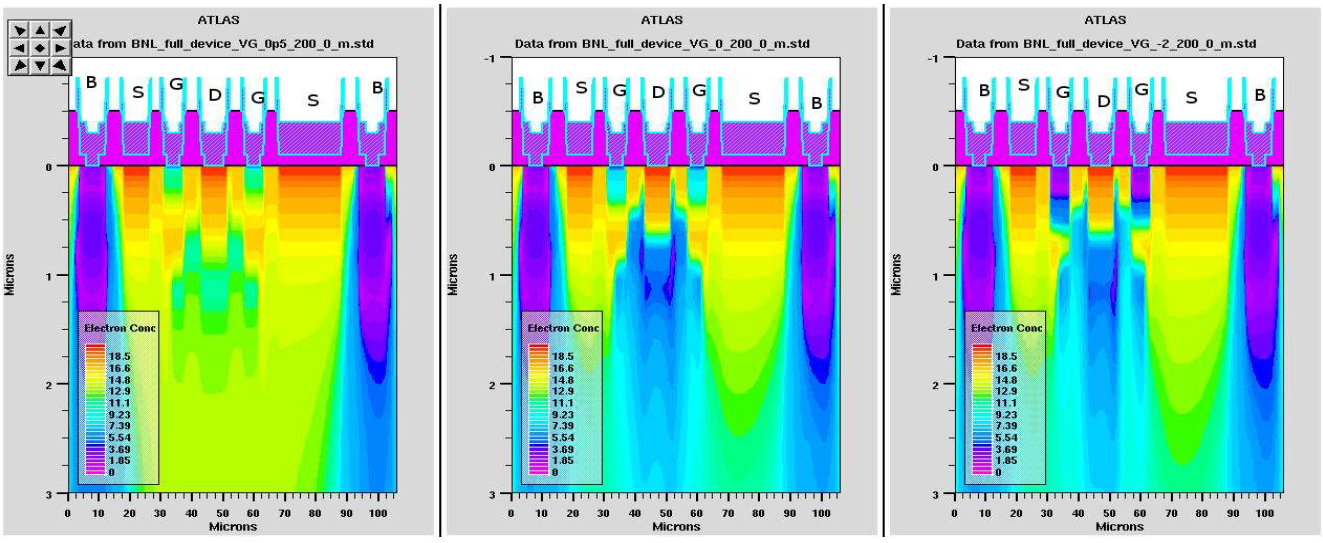

Fig. 3. Results from SILVACO - ATLAS simulations. Detail of a cross section. The device is simulated in the following conditions: Vdrain=0V, VSource=0V, VBar=-3V, VBackside=-200V and from left to right VGate=0.5V (OPEN) VGate=0V VGate=-2V (CLOSED).

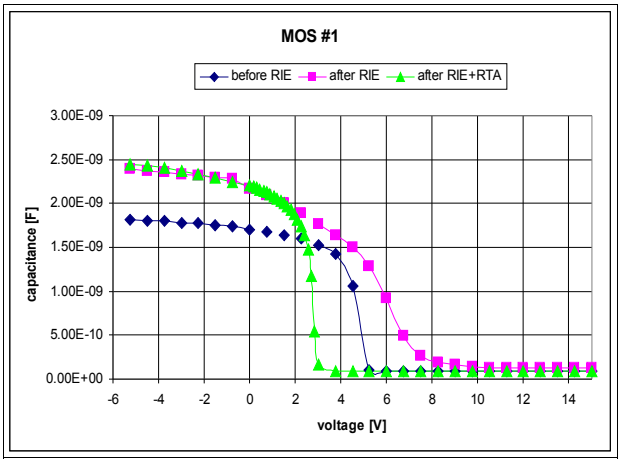

Fig. 4. Result from C-V measurement on a MOS diode (0.25cm^2). 120nm of the original 450nm oxide were etched with an 0_2/Ar/ChF_3 mixture, an etch rate of ~4Å/s and a selectivity SiO_2:Si of 1:10. The contacts were thermally evaporated and the wafer was RTP annealed.

Another issue seen with the previous production of XAMPS (pixel size 180µm x 180µm) is related to the polyimide vias. Also in this case dry and wet etching processes have been characterized for a 2µm-thick polyimide film. Both processes have been implemented and produced very good results with all the vias tested fully opened. However the dry etching not only offers the possibility of smaller features but has shown also more uniformity (Fig. 5).

Finally the contact between the two metal layers is achieved by removal of the native aluminum oxide with the same technique used for the native silicon oxide, that is back-sputtering performed immediately prior to metalization, in the same machine used for the sputtering of the metal contact. The process is finalized by RTP.

Further improvements can be achieved using an oxide layer as dielectric between the two metal layers, rather than the current polyimide insulator. This step is considered for the next production.

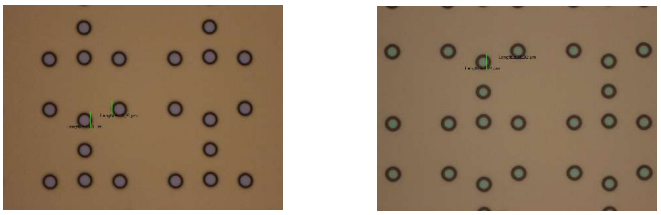

Fig. 5. The images above show results from dry (left side) and wet (right side) etching processes implemented for vias in polyimide.

IV. Test Results and Discussion

A few tests have been performed to ensure the quality of the contacts Si-Al and Al-Al. In a first run the old masks (180µm x 180µm pixel size) were used to produce devices which implement all the steps of the standard fabrication except the two deep implants. Several devices in two different wafers were tested showing pretty uniform performances (Fig. 6). The test structures, which have the same dimensions in the new set of masks, are typically close to the edge of the wafer where controlling the quality of the process is usually more critical.

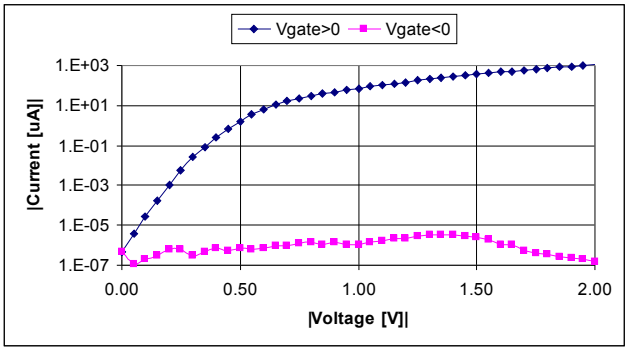

Fig. 6. Characteristic of a transistor. The measurements was performed applying voltage at the gate and measuring current at the drain. The source was left floating.

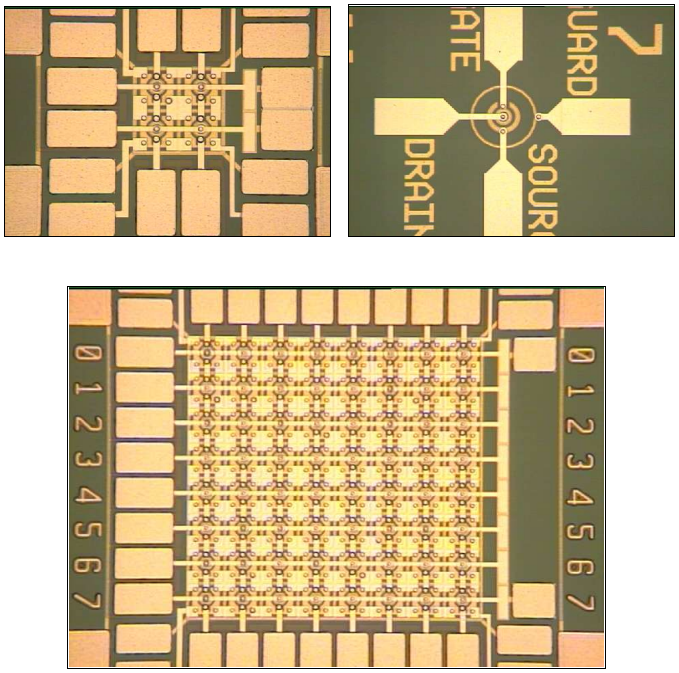

Fig. 7. Features from some devices fabricated for contact tests study.

In a second run the new masks (90µm x 90µm pixel size) were used to produce devices which again implement all the steps of the standard fabrication except the two deep implants (Fig. 7). In this case a problem with the contact pads of the test structures didn't allow to perform measurement in the test transistor. I-V characteristics of pixels boundary are shown in Fig. 8 for arrays ranging from 64x64 elements up to 512x512. During these tests the voltage (negative) was applied at the guard ring and the current probed at the anode.

The resistivity of a switch-line was measured for a 16x16 array and was ~300Ω.

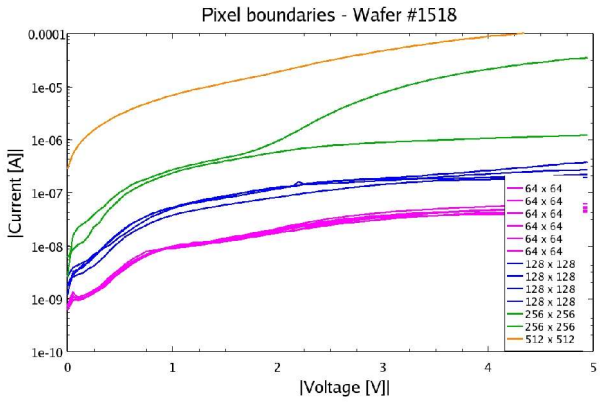

Fig. 8. I-V characteristics of pixels boundary: the voltage (negative) was applied at the guard ring and the current probed at the anode.

A final group of wafers was produced to further investigate the quality of Al-Al contacts. In this case the process was greatly simplified aiming to the fabrication of wafers with the two metal layers and the insulating interlayer. In fact, these tests would give us information about the whole process involved in this last part of the fabrication. Moreover, being the tested structures in different regions of the wafer, we have also a feedback about the uniformity of the process.

The resistivity of the switch and readout lines was measured and results reported in Table I.

Table 1	**64x64 matrix**	**128x128 matrix**	**256x256 matrix**
readout lines	37 Ω	67 Ω	111 Ω
switch lines	135 Ω	454 Ω	1100 Ω

Table I. These values are calculated applying 10mV at the two bonding pads of the switches' lines and reading the corresponding current. Calculations for a line of a 32 pixels give 13.7 Ω (r_{Al}=4μΩ cm).

V. Conclusion

The actual production of the prototypes in 100mm wafer has being completed and will be tested soon. Solutions to the problems encountered during previous production of XAMPS have been extensively implemented and tested. The full-size (1024 x 1024) arrays do not fit on a 100mm wafer, and we have been qualifying our 150mm wafer processes. All of the basic processes are under control, and a test run of diodes and test structures is being processed.

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