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Automated Manufacturing of High Efficiency Modules

Final Subcontract Technical Status Report 21 March 2005 — 31 August 2007

D. Rose, T. Jester, and G. Bunea
SunPower Corporation
San Jose, California

Subcontract Report
NREL/SR-520-42767
February 2008

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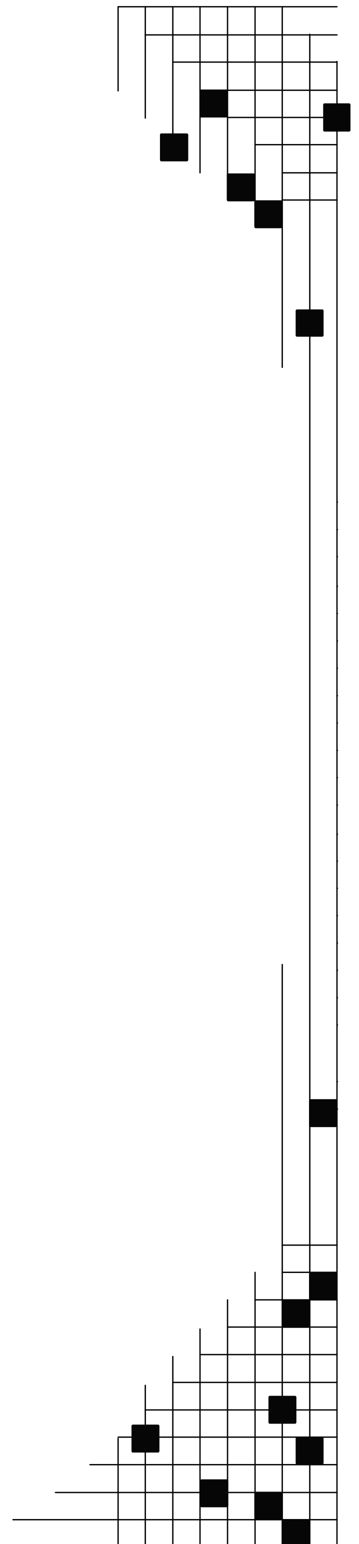

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PREFACE

This Final Technical Progress Report covers work performed by SunPower Corporation under DOE/NREL Subcontract #ZAX-5-33628-05. The subcontract, entitled "Automated Manufacturing of High Efficiency Modules," is under the Photovoltaic Manufacturing R&D Program. The work was performed from 3/28/05 to 9/30/07.

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EXECUTIVE SUMMARY

This report presents results from the two year subcontract entitled "Automated Manufacturing of High Efficiency Modules". The final objective of this research effort was to develop low-cost, next-generation SunPower modules, with 30-year warranties and at least 50% higher energy production per area relative to today's typical multi-crystalline silicon modules. This subcontract constitutes SunPower's portion of the Photovoltaic Manufacturing R&D Program administered by the National Renewable Energy Laboratory.

Significant accomplishments were made during the contract, culminating in the world's highest efficiency production PV module. A SunPower production-ready module was measured by Sandia National Laboratories to have a <u>total-area efficiency of ***20.10%***</u>. High efficiency enables higher energy production per area, which results in decreased manufacturing and system-related cost. The new modules are free of hazardous materials and have aesthetic characteristics which facilitate customer adoption. Excellent progress was also made on several module technologies and manufacturing automation.

Phase I consisted of nine tasks. A summary of task goals and results follows:

Task 1: Development of an understanding of the susceptibility of wafer fracture through theory, metrology, and modeling, to support the planning and implementation of wafer-thickness reductions.

Based on a literature review, two wafer strength metrology systems were chosen for testing: a twist tester and a load frame with four-beam bending. Due to superior repeatability, ease and accuracy of calculation, and tester robustness, the four-beam system was purchased. It was used to measure fracture strength for wafers with various characteristics and processing histories. Conclusions included:

- Damage etching improved fracture strength more than expected, evidently by etching edge damage from wire saw that extends beyond the depth of surface damage.
- To reduce breakage in manufacturing, wafer crystallographic orientation should be chosen such that handling equipment bends wafers off axis from the fracture planes.

Task 2: Identification of handling approaches for thin wafers to pursue in Phase II.

Research into state-of-the-art handling systems for automated wafer processing resulted in defining the critical requirements for handling very thin wafers (150 μm thickness after damage etch). The preferred automation was judged to be composed of robots for handling and transport, with automated optical inspection systems for metrology, and cassettes or coin-stack buffers for storage.

Task 3: Determination of the possible cost advantages derived from the use of edge processing and/or alternative damage etches to reduce breakage of thin wafers during processing.

Ingot-level etching was investigated as an alternative to single-wafer treatments. It was determined that etching of the ingot at various depths prior to wafering does not significantly impact the wafer strength or mechanical yield. An important factor affecting breakage of thin wafers was found to be the damage etch post sawing.

Task 4: Identification of a low-cost metallization technique capable of processing large, thin wafers.

Several approaches for a low cost metallization technique suitable for very thin wafer processing were evaluated, including entirely new metallization schemes and modifications of our current process. The results indicated that there is a distinction between the appropriate metallization technology that is based on the wafer size and thickness. A modification of our existing plating process was identified as being the cost effective solution for processing very thin wafers (150 micron thickness, 5 inch semi-square size) to fulfill the contract objectives.

Task 5: Development of a basis for improved automated soldering of back-contact cells and the selection of bonding approaches to pursue for the production of very thin wafers.

Six alternative soldering methods were investigated: magnetic induction, hot bar, laser, flame, hot air, and IR. All bonding methods investigated underwent systematic evaluation via post-bond joint analysis, including visual examination, X-ray, and environmental testing, with primary importance being placed on thermal cycling results. Soldering methods were also evaluated through cost analysis, throughput potential, and thin-cell damage potential. Based on these studies, magnetic induction soldering was selected as the new baseline automated bonding technique.

Task 6: Development of alternative interconnect materials and designs for cell-cell tab and string-string connection in order to reduce related costs, improve reliability, and eliminate Pb.

During Phase I SunPower developed new processes for cell-cell interconnect and string interconnect that meet the contract requirements: cost reduction, improved reliability, and the elimination of lead. Structural and finite element analysis was used to characterize the forces on the solder joins and solder pads. New interconnect designs with improved compliance decrease the force on the solder joints and solder pads, which reduces solder fatigue that results from thermal cycling and thus improves the reliability of the joint. A new lead-free soldering process was developed. The use of a SnAg system instead of a Pb-solder system addresses RoHS requirements and improves the reliability of the interconnect.

Task 7: Development of alternatives to standard encapsulation materials.

Extensive research was performed on alternative encapsulation materials. Non-EVA encapsulants such as Ionomer, TPU, PVB and silicone were investigated

through accelerated tests along with alternative EVA's. A UV-stable EVA (STR 15420P/UF) that satisfies the contract goals was selected as the baseline encapsulant to be used in next generation PV module. Research on silicone-based encapsulant will continue due to potential for significantly enhanced performance at module level.

Task 8: Investigation of alternative diode configurations, junction boxes, glass coatings, and other package-related features to reduce manufacturing costs and improve product quality.

Substantial progress was made during Phase I of the contract regarding packaging configuration. Modeling of alternative diode configurations revealed the potential for significantly increased energy production in partially-shaded applications. Investigation of new junction boxes resulted in a new baseline selection plus the identification of possible next-generation alternatives. Investigation of plastic frames showed promise for some applications. Several anti-reflection coatings were investigated. Concerns regarding the 30 years reliability and aesthetics led to continuing the investigation for appropriate coating during second phase.

Task 9: Reliability testing of the new module designs and concepts.

Extensive reliability testing was done in each of the areas investigated with the intent being to develop modules with a 30 year lifespan. Experimentation and modeling was done to define specific failure modes and develop accurate testing for each aspect of module reliability. The lifetime of our modules under accelerated testing was greatly improved, especially through progress on soldering materials, parts design, and processes. Other improvements to encapsulant and junction box designs were screened using accelerated tests.

Phase II consisted of six tasks.

Task 10: Automation Development: Alternative Equipment Design

Automated handling of ultra-thin wafers is a challenge in the manufacturing environment. During Phase II, SunPower selected four equipment vendors for development collaboration: vendor 1 for SCARA robots to transport, hand-off, and store thin wafers, vendor 2 for parallel robots, vendor 3 for wafer stringing, and vendor 4 for string handling. Testing on all four tools with wafers as thin as 150 μm gave promising results and further work on ultra-thin wafers automatic handling will continue under the SAI contract.

Task 11: Pilot-line Implementation of Wafer Edge & Surface Modification

Considerable progress was made under this task for optimization of the sawing process to minimize the wafer thickness of the as-sawn wafers (down to 160 μm) and reduce the damage to the wafer. It was found that the input factors of feed speed, input slurry flow, and output slurry flow have a significant impact on the wafer quality. Experiments using laser-guided water jet to shape the edge of thin as-sawn wafers showed insufficient benefit relative to the cost. Additionally, an in-line system for wafer damage etch removal was designed and tested.

Experiments showed that thin wafers (165 μm thickness as sawn) are more sensitive to maintaining the spacing relative to each other in the tool at high speed.

Task 12: Pilot-line Implementation of Metallization of Thin Wafers
A modified plating jig was designed. Tests showed that the new design enables metallization of wafers as thin as 100μm with no wafer breakage and no edge chipping during the test. Finished wafers showed no difference in aesthetics as compared to standard processed wafers. Significant warping (up to 2mm) was measured on wafers and we have an ongoing effort under SAI to understand the stress in the plated metal as a function of wafers thickness and plating conditions. An alternative metal finger design with similar metal resistance losses has been proven more resilient to the metal/Si cracking. Coupons using cells with this alternate metal finger design and a metal to silicon thickness ratio 58% *more* than our standard were found to have less than 2% (relative) efficiency degradation from 200 thermal cycles (+90C/-40C).

Task 13: Pilot-line Implementation of Alternative Interconnect & Encapsulation
Pilot implementation of a new bus interconnect design found that changes were needed to allow high-yield fully-automated manufacture. Tests confirmed the redesign was successful. New cell-to-cell interconnects with smaller tab area were also a success, with tests showing less than 3% degradation in 900 thermal cycles. Implementation of high-speed lamination with ultra-fast-cure EVA established a baseline of 10.5 minutes, which provides a 5 kW/hour manufacturing throughput. The majority of the encapsulation work, however, continued to be exploration of additional alternatives, primarily silicone. It was found that the composition of silicone encapsulants has a significant impact on reliability. The benefit from improved transmission of silicone was demonstrated with a 1% increase in Jsc post-lamination on coupons with silicone as compared to those laminated with EVA.

Task 14: Pilot-line Implementation of Modified Package Configuration
Excellent progress was made during Phase II on identifying new packaging methods that lead to improved efficiency and reduced cost/rated Watt. New JBoxes with improved cost, suitable for automation and compatible with 30 years reliability, were identified and tested. Prototype modules with in-laminate diodes were manufactured and evaluated. Consistent energy production gain of 4% from sol-gel ARC was demonstrated. Challenges in manufacturing and shipping of ARC glass were identified and addressed. A new module design led to a champion 20.1% total-area efficiency module measured at STC by Sandia National Laboratory.

Task 15: Reliability & Field Testing
Important progress was made both in increasing the life expectance and failure rate of our modules, and in gaining confidence that the quality of is consistent with a thirty-year warranty. A combination of finite element analysis and experiments led to the development of a model for solder joint fatigue which gives the global

acceleration factor between the lab conditions and the field conditions. Modules with technologies developed under the contract fielded in three different climatic conditions showed superior kWhr/kW performance and confirmed short-term reliability.

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1.0 INTRODUCTION

Increased conversion efficiency has long been recognized as a powerful lever to decrease the cost of energy generated by a photovoltaic system. The value of high efficiency is recognized in the DOE Solar Program Multi-year Technical plan [1]. High efficiency reduces per-watt shipping and installation costs and provides strong leverage to reduce manufacturing costs per kW-hr of energy produced by the module. It has further been recognized that higher efficiency modules allow for larger capacity PV arrays to be mounted within the optimally-oriented portion of a roof, thereby amortizing fixed installation and sales costs over more total system watts [2].

The benchmark, goal, and progress for efficiency are as follows:

- The efficiency goal for crystalline silicon modules in the DOE plan is 14% for 2005 and 20% for 2020. [1].
- The goal for this contract is > 50% improvement of energy yield/area vs. typical multi-crystalline silicon modules at the start of the contract, which translates into total-area efficiency of 17.5 – 18%.
- The total-area efficiency achieved in this work is 20.1% (a world-record for a production-ready module) as verified by Sandia National Laboratory. Not only does this exceed the contract goal, it meets the DOE goal for the year 2020 established in the 2003 plan.

Another strong lever for cost reduction is reduced cell thickness. Due to their architecture, SunPower cells actually have a slight increase in efficiency at 150µm thickness compared to 220µm [3]. This is in contrast to traditional silicon cells which suffer decreased efficiency from this reduction. A portion of this subcontract is working on tasks that enable the use of thin cells, and modules with cells of 150µm (the target for the subcontract) were made successfully.

The subcontract also has significant tasks to increase module reliability and other module-related improvements that decrease cost and increase the market acceptance of modules. Progress, including the successful elimination of hazardous materials from the module, is summarized in the Executive Summary and detailed in section 2 of this report. Excellent progress was made on identifying automation and other module technologies, and we are on track to bring low-cost, next-generation SunPower modules into full production on a new U.S. module manufacturing line which will be implemented under the Solar America Initiative program as a follow on to this contract.

2.0 PVMR&D PROGRAM EFFORT

2.1 Task 1. Mechanical Strength Analysis

The goal of this task was to gain an understanding of wafer-fracture susceptibility through literature, use of modeling, and experimentation to support planning and implementation of wafer thickness reduction. We have evaluated different fracture testing systems and tested wafers with different characteristics and processing histories.

Literature search

A literature search concerning fracture testing methodologies and commercially-available wafer fracture test systems was completed. Key findings were split into four categories: comparative data, load frames, techniques for damage detection, and experimental findings on wafer strength.

Comparative data deals with the measurements and standards used in the study of fracture mechanics. It was found that the standard testing format is bend testing, ideally reporting displacement and force at the breakpoint, which can be used to calculate the mechanical properties of the test subject.

Load frames tend to be the standard in force-measuring tools, a force gauge/load cell being used where the sample is mounted. A compressive force is applied in a controlled manner with data being derived from the resistive force and bending distance of the sample. Experimental trials on wafers at SunPower in a manual load frame demonstrated a large dependence of break-point force on fixture orientation and loading rate.

Several techniques for damage detection exist, allowing the relationship between damage and strength to be defined. Damage is generally measured in terms of its depth and orientation, and roughness. Two main methods of damage detection are ultrasonic scanning, and nano-intenders (test the hardness of silicon). No vendor survey was done concerning damage detection, as priority was placed on load frame acquisition and the defining of mechanical characteristics.

Some key experimental findings on wafer strength include: strength is impacted by damage etch, grinding and damage etching processes directly correlate to breaking strength, the strength of edge dislocations is impacted by the type and concentration of impurities, and that strength is also impacted by the crystallization process, ingot cutting, wafer sawing, and mechanical handling.

Fracture Strength Testing Method

Wafer strength testers are configured to support individual wafers in various ways and apply a controlled force onto the wafer, deflecting the wafer such that one side is in tension. Both displacement and force are directly measured. When wafers are bent, one side is in tension and the other in compression. Brittle materials, such as silicon, are significantly stronger in compression than in tension, therefore surface flaws on the side in tension will induce failure in the material. Strength testers that bend wafers repeatable and monotonically allow for strength testing of just one side of wafers. This is useful for evaluating the strength effects of one-sided surface treatments.

Two wafer strength testing techniques were evaluated using monocrystalline silicon wafers:

- Twist tester offered by GP Solar of Konstanz, Germany
- Load frame, with a four-beam bending fixture, used by Institut für Experimentelle Physik at Freiberg, Germany

The twist tester (Figure 2.1-1 left) is primarily designed for integration in-line as a go/no-go test of individual wafer substrates at the beginning of the solar cell manufacturing process. Each wafer is twisted to a pre-determined load by pressing down on two of the four corners while supporting the other two. 'Weak' substrates will break and drop into a broken wafer receptacle. Output values are limited to force and displacement. No stress data is generated and all comparative studies would be based on the assumption that the groups were of equivalent thickness.

The second system is a conventional load frame with a four-beam bending fixture (Figure 2.1-1 right). The area under test lies between the span of the support beams, the surface and edges outside this span experience no stress, and are therefore not tested. Finite element modeling of the wafer stress distribution is performed with reference to the fixture's support beam distance. This model is used to calculate the real critical stress [δ in MPa] at wafer breakage. The algorithm calculates a characteristic failure stress (to which 63% of the samples survive) and the Weibull modulus (m), which is the width of the distribution for the test population. Using the stress data, a Weibull breakage probability estimate for the population can be generated from each sample group. The 4-beam bender is self-aligning.

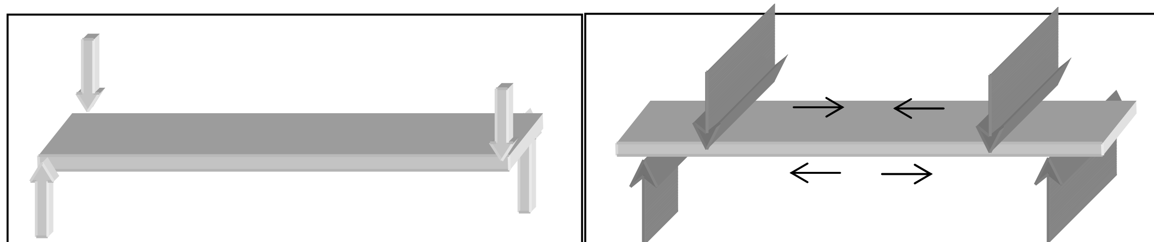


Figure 2.1-1: Twist tester force diagram (left) and four-beam bend tester force diagram (right)

Besides 4-point bending and twist testing, our literature search showed that most fracture strength experiments on silicon were done with either 3-point bending or concentric loading setups. Concentric loading setups involve a load being applied by a ball bearing on a point on the sample supported by an o-ring centered on the ball bearing. This method is used to eliminate edge effects and was therefore not chosen for our tests. 3-point bending is similar to 4-point except that the stress is concentrated on the one point between the two supports that is impinging down onto the sample. 4-point bending was chosen over 3-point since the stress is evenly distributed between the two inner spans.

Extensive testing lead to the conclusion that the four-beam bending technique is preferred over the twist testing apparatus due to: better repeatability, alignment and control of curvature of the wafers. Simple formulations allow the calculation of stress distribution based on the 4-beam bending data.

Stress Calculations

When comparing strengths of various wafers, stress is a more useful metric than force as it is not dependent on wafer thickness. Simplified four-beam bending models lead to the standard formulation for maximum tensile stress:

$$\sigma_{\max} = \frac{6Fl}{wt^2} \qquad \text{(Eq.1)}$$

Where F is the force applied, *l* is the length of the support span, *w* is the width of the wafer in the direction parallel to the beams, and *t* is the thickness. This formula works well for small deflections such as those experienced by brittle materials, but begins to lose accuracy when the amount of deflection approaches the dimensions of the wafer. To ensure our stress calculations using Eq.1 were reasonable, we compared our stress values on samples tested in Freiberg to the FEM stress calculations performed by their research group, which can accurately calculate stress at larger deflections. Our stress values were generally 5% lower than those obtained by FEM.

Experiments

In evaluating the load frames described above, we have measured sets of wafers with different processing at: ingot etching, damage etching, and fracture plane orientation. All reported results are from Freiberg's FEM.

Ingot Etching

Etching the ingot after it has been slabbed is intended to remove surface damage from slabbing. This only affects the quality of the edge of the final wafer. Table 2.1-1 compares samples with the same crystal orientation that have undergone similar damage etching, but had different ingot etch depths. No correlation is observed between ingot etch depth and fracture stress, suggesting that ingot etching does not affect wafer strength as determined by four-beam testing.

Table 2.1-1: Analysis of ingot etching on wafer strength. 95% confidence limits are shown (e.g. for the sample #1 95% of the characteristic fracture stresses will be between 267+9 and 267-8.7 MPa).

Ingot etch	s_0 (MPa)	95% confidence (-/+)
87 µm (#1)	267	8.7/9.0
87 µ m (#2)	247	9.8/10.4
57 µ m (#1)	264	13.3/14.3
0 µ m (#1)	276	11.3/11.9
0 µ m (#2)	271	9.2/9.5

To test for any overall benefit of ingot etching, we tracked mechanical performance on the manufacturing line for over 900 wafers. No significant mechanical yield improvement was seen specifically due to ingot polishing.

Damage Etching

Previous literature indicates that significant strength differences arise between wafers etched in acid versus alkaline solutions, with acid etched wafers having significantly higher fracture strengths [4].

Detailed results of the influence of different wet damage etch on wafers strength is presented in Task 3 report. Both etching solutions significantly improved wafer strength beyond the as-sawn wafers. This is further emphasized in Table 2.1-2, which shows the strength of wafers from a single-side etched sample set when the etched side is put in compression versus tension. It is well known that brittle materials are much stronger in compression than in tension, so the almost 100% improvement in fracture stress when flipping the wafer over demonstrates the dramatic strength improvements obtained from damage etching.

Table 2.1-2 Analysis of single sided acid etch on wafer strength.

	s_0 (MPa)	95% confidence (-/+)
Non-etched side in tension	154	4.3/4.5
Acid-etched side in tension	290.6	18.4/20.0

Fracture Plane Orientation

Silicon is an anisotropic material and it is well known that the two easiest cleavage planes are {111} and {110}. In Figure 2.1-2a, for example, the {110} fracture planes run parallel to the flats of the wafers, making it much easier to fracture by bending the wafer parallel to the flats. In Figure 2.1-2b, the {110} planes are rotated by 45^0, so the wafer is easier to fracture along the diagonals as shown in Table 2.1-3. In our bending setup, all wafers are loaded such that the flats are parallel to the 4 beams. Table 2.1-3 shows that when the {110} fracture planes are rotated by 10° from parallel with the 4 beams there is a slight increase in the fracture load, and when they are rotated by a full 45° (i.e., Figure 2.1-2b), there is a more dramatic increase. Note that in all tests the wafers are inserted into the load frame with flats parallel to the beams – "rotated" simply means that the ingot is cut at different orientations.

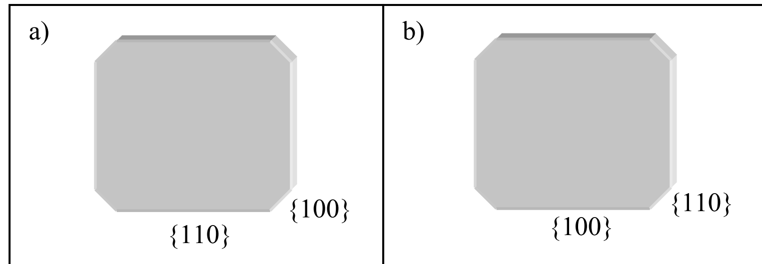


Figure 2.1-2: Wafers with the face parallel to the {110} (a) and {100} (b) family of planes

Table 2.1-3: Fracture strength of wafers with 3 different flat orientations.

	s_0 (MPa)	95% confidence (-/+)
0°	277	11.3/11.9
10°	294	9.8/10.5
45°	423	7.4/7.5

<u>Summary</u>

A literature search and on-site testing of different loading tools led to the acquisition of a 4-point bending setup to test wafer strength. Wafers with various processing histories were tested. The results show that an ingot etching step has no effect on wafer strength in 4-beam loading when damage etch is also done on the wafers. Damage etching was shown

to significantly increase the strength of wafers. The crystal orientation of wafers also has a significant impact on wafer strength, wafers with a {100} flat edge having significantly higher fracture stresses in our loading geometry.

2.2 Task 2. Handling and Automation Development

We have investigated state of the art techniques concerning the handling of very thin (150μm) wafers using automated systems. Mechanical yield testing of wafers of various thicknesses was done on SunPower's cell manufacturing line. The critical factors concerning the handling of very thin wafers were identified and are listed below:

- Avoid contacting the wafer edges to prevent micro-chips and micro-cracks.
- Avoid sudden impact on the wafer surfaces and on the wafers edges such as snubbing actions.
- Minimize applied forces along the wafer surface and always apply an even distribution of force by means of mechanical or vacuum contact.
- Avoid bending-induced stress and vibrations to minimize stress and propagation of micro-cracks.
- Avoid surface and edge friction to prevent scratches and micro-crack formation.

The main areas of investigation included: wafer handling and hand-off mechanisms, metrology and storage/buffering.

<u>Investigation of State-of-the-Art Handling Methods</u>

Automation
Robots are the chosen medium for automation, providing the necessary throughput along with the sensitivity required for the handling of thin wafers. There are six types of robots available for industrial use: Cartesian, cylindrical, spherical, articulate, SCARA (Selective Compliance Articulate Robot Arm), and parallel. The most applicable robots for thin wafer handling applications are Cartesian, SCARA, and parallel robots, shown in Figure 2.2-1, because comparatively, they offer the best compromise between cost and performance.

Figure 2.2-1: Left to right: Cartesian, SCARA, and parallel robots

<u>Wafer Storage</u>
Wafer storage tends to be very general, with no next-generation solutions being readily available. In general, there are three modules involved: a cassette transport system, an elevator system, and a wafer indexer. The three key issues concerning buffer and storage systems are:

- Difficulty driving the wafers at high speed due to misalignments, which leads to breakage.
- Integration with continuous processing can lead to buildup; when breakage occurs in the buffer it results in compounding damage.
- Systems are large and expensive, and can complicate entire procedures especially when associated with high UPH tools and multiple lanes.

Investigation into Current Capabilities

Groups of ~700 wafers of 155μm, 145μm and 110μm thickness were run through the standard process in our manufacturing facility. It was determined that, with some modifications, current processes can be used to produce very thin 150μm wafers that will meet the contract goals. However, the results show that producing wafers with thicknesses less than 150 μm would require resources and a timeframe inconsistent with the contract objectives. Figure 2.2-2 presents mechanical loss in the first trial for six critical process steps for 145μm, 155μm, and 220μm thick wafers. The main areas requiring development for the high yield production of very thin 150μm, 125μm semi-square wafers are: ingot sawing, cassette design, load/unload method, print, transportation, and end effectors.

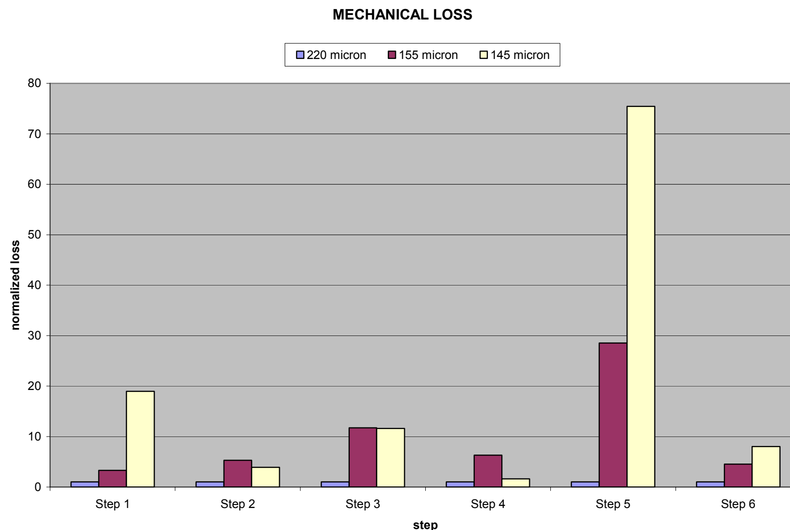


Figure 2.2-2: Mechanical Loss

Summary and update

An investigation of state-of-the art handling, metrology, and storage systems lead to the conclusion that the key constraints for high yield, thin wafer manufacturing include the avoidance of wafer edge contact, sudden impact, bending-induced stress and substrate friction, and the minimization and even distribution of applied forces. It was determined that, with some modification, SunPower can fabricate very thin (150μm thick) wafers that will meet contract goals, while thinner wafers will require extensive development and changes in fabrication methods that are inconsistent with the contract scope and timeline. Changes made outside of the contract resulted in mechanical yield for 165μm thick wafers comparable to the control wafers.

2.3 Task 3. Edge Processing and Damage Etch Development

Monocrystalline silicon ingots generally have grooves and striations on their outer surface which remain after sawing has occurred. These striations characterize the surface damage on the wafer edge. Additional damage is incurred on the wafer surface and along the apex of the edge from wafer-slicing. Examples of edge damage can be seen in figure 2.3-1.

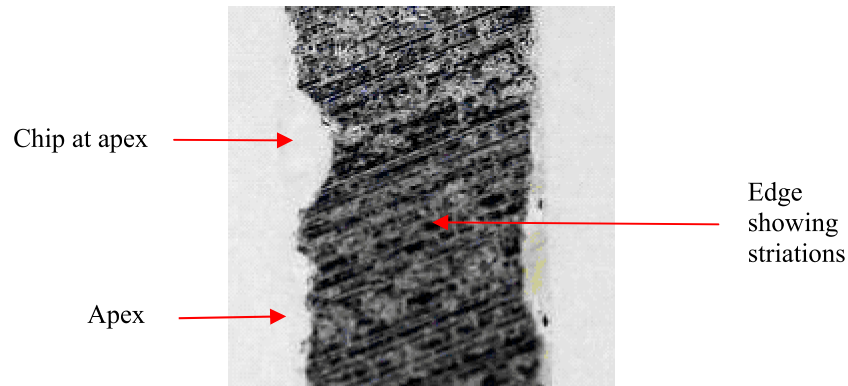


Figure 2.3-1: Wafer edge showing striations and chips at the apex (where the edge meets the face of the wafer). Image is inverted for clarity

<u>Edge Processing Literature Survey</u>

A literature survey on wafer edge processing was performed. Two non-etching methods were found which can be used for focused material removal at silicon wafer edges once the wafers have been cut. Two general types of etching are also presented.

1. Laser: State-of-the-art. Trade-offs include cutting speed versus kerf width. Some methods claim to address the particle generation issue. Silicon dioxide is transparent to many laser sources. A comparison study of edge isolation techniques for conventional mc-Si solar cells cites lower fill factor as a disincentive for use on edges [5].

2. Mechanical Grinding: Mechanical grinding is the conventional method for processing standard semiconductor wafers. Complementary technologies are needed for grinding thin wafers. Today's production limit for grinding is about 150μm. Yield loss considerations from grinding have made it very difficult to use this method below 150μm.

3. Wet Etching: This step is used to remove surface or sub-surface damage (SSD) and/or stress in production of thin and ultra-thin wafers. Wet etching is the simplest etching technology as it requires only a container with a liquid solution to dissolve the material. The etching agents for silicon are mostly mixtures of HF and HNO_3. Etching rate of silicon is about 1.5 μm/minute. For anisotropic silicon etching, NaOH or KOH are used.

4. Dry Etching: Dry etching technology can be split in four categories: reactive ion etching (RIE), sputter etching, vapor phase etching, and atmospheric downstream plasma (ADP) dry chemical etching (DCE). RIE is a combination of chemical and physical etching. The wafer is placed in a reactor with a mixture of several gases. Plasma is struck in the mixture, breaking the gas molecules into ions. The ions are accelerated, and react at the surface of the material being etched. By changing the chemical and physical balance it is possible to control the anisotropy of etching. Sputter etching is actually RIE without

reactive ions. In the vapor phase etching, the wafer is placed inside a chamber in which one or more gases are introduced. The material is dissolved at the surface in a chemical reaction with the gas molecules. For SiO_2 etching, HF is used. For silicon etching, XeF_2 is utilized. ADP-DCE is an ion-free chemical etching process that uses Ar/CF_4 plasma. Here, chemical sputtering is the process where plasma produced radicals cause chemical reactions on the silicon surface.

<u>Ingot and Damage Etching Effects</u>

Ingot Etching

It is feasible to remove edge damage prior to wafering by brushing or etching the ingot. Etching was chosen as a method to test whether the removal of striations and grooves would improve wafer strength and manufacturing mechanical yield. The acid etch referred to below is achieved by immersion in a nitric-HF acid mixture at room temperature. The ingot is etched to remove defects to produce a mirror finish.

The following images are each of a single wafer viewed edge-on under microscope magnification. Clearly, ingot etching produces a less damaged surface (left).

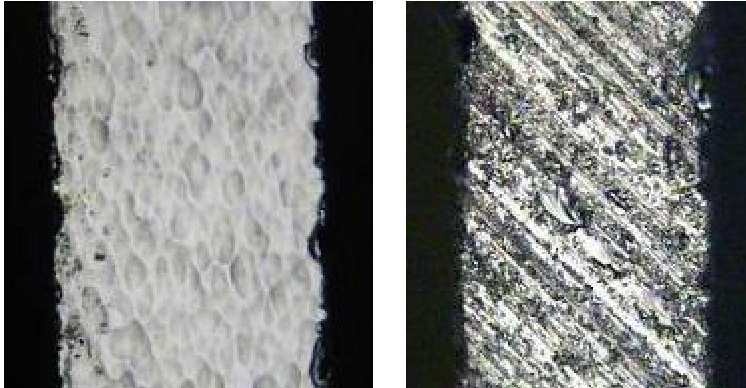


Figure 2.3-2: Edge of wafers sliced from a polished ingot (left) and an unpolished ingot (right).

Ingot Etching and Damage Etching

Once the wafer is sliced, the damage from saw and the ingot shaping can both be removed from the wafer with acid or alkaline damage removal etching.

The effect on wafer fracture strength due to ingot etching was detailed in section 2.1. No effect on fracture strength from ingot etching is observed. There was, however an improvement in wafer strength after saw damage removal. This suggests that damage etching (etching of individual wafers after the ingot is sliced) etches away damage in all directions of the silicon rendering ingot damage-removal steps unnecessary.

Damage Etching

Two groups of wet damage etchants were tested: acid and alkaline. Table 2.3-1 below shows average fracture stress versus type of damage etching. The groups of 30 wafers in this test were all sawn in the same wire saw load. The alkaline and acid etched groups had the same depth of damage removed by their respective etchants. Again, the stress on the tensile surface at fracture was calculated using a finite element model. There is

significant effect on fracture strength between as-cut and etched samples and a slight increase in strength between alkaline and acid etched samples.

Table 2.3-1: Fracture stress of acid versus alkaline damage etching.

Wafer damage etch	s_0 (MPa)	95% confidence (-/+)
As-cut	134	3.8/4.1
Alkaline	276	8.7/9.0
Acid	284	19.3/20.9

Based on literature search, initial cost analysis and expected yield improvement, we have removed single-wafer processing techniques such as edge grinding from our consideration. Other known methods that shape the wafer edges without introducing additional damage are water jet guided laser and Ar-plasma etch. Results of water-jet/laser are shown in Task 11.

Summary
Result from our literature investigation and experiments was that damage etching significantly increases the strength of wafers. In terms of different damage etch solutions, an acidic solution was found to be slightly more effective than alkaline solutions. The focus during Phase II was on reducing the damage depth of the as-sawn wafers.

2.4 Task 4. Metallization of Thin Wafers

The purpose of the work performed under this task in Phase I was to test the viability of current and alternative metallization techniques in terms of the contract goals of processing thinner and possibly larger wafers. The conclusion of the work was that a variation of the current plating process was the preferable approach for the contract goals of 150µm-thick cells.

Metallization Development

The results of our investigation indicate that there is a distinction between the appropriate metallization design technology that is based on the wafer size and thickness. The distinction occurs between wafers:

- Size ≤ 125mm semi-square and ≥ 150µm thickness (wafers thickness after damage etch)
- Size > 150mm semi-square at any thickness

Wafer thickness of 150µm and wafer size of 125mm semi-square was selected as the optimum to be pursued in Phase II based on the following:

- Expected decrease in wafer costs (from cost reductions of raw Si, sawing fabrication, saw yield) which cause wafers larger than 125mm square and wafers thinner than 150µm thick to be less critical for solar cell development.
- Yield losses increase from processing wafers significantly thinner than 150µm can offset part or all of the savings from the reduced Si.
- Potential improvements in cell efficiency due to alternate cell designs are more beneficial than improvements in cell efficiency due to alternative metallization methods.

- Combining alternative metallization methods with alternate cell designs only enable small efficiency improvements at the expense of a more complex and costly processes.
- Efficiency as determined by cell design peaks at 145-160μm and drops off below this thickness.
- Relatively the same amount of metal must be used in any module for sufficient conductivity.
- Some technical considerations, such as dimpling of the wafer under solder joints with wafers ≤ 120μm thick, make thinner wafer assembly much more difficult.

Experiments

All of the proposed metallization techniques were evaluated using wafers ranging from 120μm to 220μm, each examined in terms of wafer bow and output.

Alternative Metallization

Six other metallization approaches were identified as possible enabling processing methods of wafers lower in thickness than 150μm and larger in size than 125mm. Two of the metallization approaches at cell level were reduced to practice on device wafers. Experimental cells with >21% efficiency were manufactured using this method. The results of electrical performance matched the simulation results as can be seen from Table 2.4-1. However the cost analysis for the alternative approaches indicates increased cost as compared to the current metallization process.

Table 2.4-1: High efficiency results on alternative metallization processes

sample	Eff (%)	Voc (V)	Jsc (mA/cm2)	Vmp (V)	Jmp (mA/cm2)	FF
1	20.6	0.667	39.7	0.546	37.7	77.9
2	**21.1**	0.668	39.7	0.562	37.5	79.5
3	19.5	0.664	38.1	0.55	35.4	77.0
simulation	**21.2**	0.673	39.7	0.564	37.6	79.3

Warping

A group of ~700 wafers of 155μm thickness were run through the standard process in our manufacturing facility. The wafer warpage after metallization was 1-2mm as compared to our current thickness wafers which have <1mm warpage. The yield loss at the metallization step increased 5x when compared to loss of our standard thickness wafers, but the yield loss mechanisms were identified. Work outside of the contract resulted in reduced warping and breakage in production, with the resulting mechanical yield of 165μm thick wafers the same as for 240μm thick wafers that we were processed at the beginning of Phase I.

Summary

Alternative metallization methods suitable for thin wafers processing were investigated through performance and cost analysis. Although cells with >21% efficiency were manufactured, the cost analysis showed these alternatives too expensive compared with current baseline. The metallization method selected to be pursued in Phase II of the

contract is a metallization process similar to our existing process that will allow for the cost effective fabrication of 150µm thick, 5 inch semi-square cells which will meet the contract energy production requirements.

2.5 Task 5. Bonding Process Development

Alternative high-volume bonding approaches were investigated with the goal of achieving high high-quality automated connection with thin back-contact cells. All bonding methods investigated underwent systematic evaluation via post-bond joint analysis, including visual examination and environmental cycling, with primary importance being placed on thermal cycling results. Methods were also evaluated through cost analysis, throughput potential, and cell damage potential.

<u>Soldering Approaches</u>
Next-generation bonding approaches were investigated, with the following requirements:

- Low cost
- High-throughput automated process
- High module reliability
- High yield with thin cells
- High module efficiency

Six alternative soldering approaches investigated: magnetic induction (ML), hot bar, laser, flame, hot air, and IR. The following paragraphs present a brief description of each type of soldering.

ML (Magnetic Induction) Soldering
A soldering head is composed of copper conduction loops that create a magnetic field due to alternating current passing through the coil. Ribbons beneath the loop experience eddy currents as a result of the alternating field which heats the ribbon in a controlled manner. ML soldering is a non-contact method, causing low stress to the cell while enabling very low cycle time

Hot Bar Soldering
A contact method with a low cycle time of about 1.5 seconds per joint, hot bar soldering produces very localized heating. However, thermal cycling performance is not as good as ML soldering limitations may be reached for very thin cells, so further development was discontinued.

Laser Soldering
This is a non-contact method using a laser to produce very controllable and localized heating. Laser soldering heads are expensive and so it was determined that having more than one would not be economically viable, as such the cycle time would be about double that of ML soldering. Due to these economic constraints, development of laser soldering was discontinued.

Flame Soldering
A mixture of oxygen and acetylene is used to create an approximately 1000 deg C flame, which provides a non-contact soldering method with very localized heating. The soldering cycle time is very low with the flame method, about 0.2 seconds per joint. Although it is

the fastest soldering method of those investigated it provided poor reliability results and therefore development of flame soldering was discontinued.

Hot Air Soldering
A non-contact method using hot air to solder the joint, heating is not very localized and leads to cell warping. Cycle time for this soldering method is fairly high at about 5 seconds per joint. Due to the poor performance and low throughput potential of hot air soldering, development was discontinued.

IR Soldering
IR soldering is non-contact, but does not allow for localized heating and as such causes cell warping to the point that cells cannot be laminated. Development of IR soldering was discontinued.

Magnetic Induction (ML) soldering was selected as the baseline bonding approach. Advantages include short cycle time, localized heating, low force on cell, and high process repeatability. It was found to be the most consistent in providing joints with excellent thermal cycling performance.

Basic design and improvements
The induction heating system is composed of an induction coil, an AC power supply, and a water cooling system which maintains optimal operating temperature. In order to optimize the induction soldering system, several modifications were made, including changes to the heat zone in order to create a more localized heating effect and thus reduce the potential for cell damage. Coil design and orientation were also altered, including alterations to coil diameter; joined coils were replaced with individual coils due to differences present between positive and negative sides of the cells. The frequency of the alternating current has a strong relationship with the depth to which the magnetic field penetrates the material being heated – higher frequency results in fast, shallow heating, while lower frequency is the inverse. SunPower has optimized the frequency (power), along with force and coupling distance in order to reduce cycle time and provide joint consistency. The tab hold-down pins were replaced with a very low thermal conductivity material in order to ensure proper joint quality.

Cell heating
As part of the investigation of induction soldering, an experiment was conducted to determine if pre-heating the entire cell before soldering would reduce micro-cracks (which can cause efficiency loss in thermal cycling). Preheating was done at 60ºC and 100ºC (plus a no-preheating control), with a total of six 3-cells coupons (230µm cells, 3 with normal metal thickness, 3 with 10 µm thicker metal). As can be seen in Figure 2.5-1, testing to 400 thermal cycles (-40ºC to +90ºC), for this limited sample size, showed no significant difference in efficiency drop between pre-heated cells and non-pre-heated cells. It should be noted that the below tests were done before other improvements that further improved the baseline thermal cycling performance.

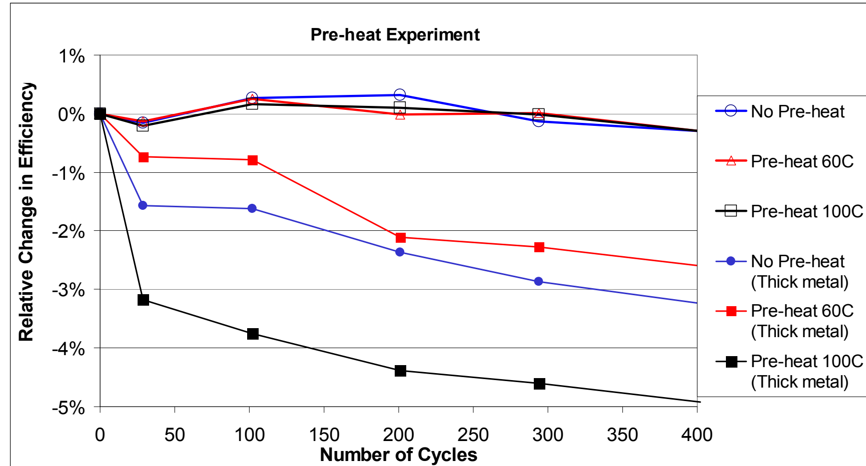


Figure 2.5-1. Thermal cycling of pre-heated cells.

The results of induction soldering are very promising. Temperature cycling resulted on average in < 1% efficiency reduction after 400 cycles (-40ºC to +90ºC) (IEC standard is <5% efficiency degradation after 200 cycles (-40ºC to +85ºC)). Detailed results on voiding and reliability testing of various bonding methods are presented in details in section 2.9.

Conductive Adhesives

The potential use of conductive adhesives as an alternative contacting method to conventional soldering has been investigated. The key benefit from using conductive adhesives is the creation of a low-stress process for the interconnection of cells in a module, which can eliminate or significantly mitigate the risk of high thermal shock that can damage cells. The factors driving the potential transition to adhesives are: the trend towards thinner wafers, the move to Pb-free solders that results in increased soldering temperatures, the desire for very high numbers of contacts for some next-generation cell designs, and the desire for reduced-step module manufacturing.

Initial testing of conductive adhesives indicated that they would not provide acceptable performance for PV interconnect bonding applications. Failure was noted in terms of shear strength, and efficiency drop due to thermal cycling. The main reasons for these initial failures were deemed to be the inflexibility of the adhesive, and difficulty in simultaneous curing of the adhesive and the encapsulant. Improvement was noted with the use of silver plating on contact areas.

Originally, the use conductive adhesives necessitated the simultaneous curing of the adhesive and the EVA (i.e. the adhesive cannot be cured separately and before the EVA lamination because this would effectively result in double curing of the adhesive which would lead to its failure). Recent progress on the encapsulation task has determined that this is no longer necessary. Work on development of conductive adhesives continued in Phase II due to recent advancements that remove some of the previous limiting factors including the ability to form good contacts to non-noble substrate surfaces and diminished bulk resistivity.

Summary

Different approaches for automated soldering of back-contact cells were investigated. Based on its high level of performance, induction soldering was selected as the bonding

approach for next generation module fabrication for both cell-cell and string-string interconnect. A robust induction soldering process was developed by making improvements in the design of the induction tool, and this resulted in consistently good quality solder joints as demonstrated by an average of <1% efficiency degradation after 400 thermal cycles.

2.6 Task 6. Interconnect Design and Materials

This report describes SunPower's effort during Phase I of the contract towards developing next generation cell and string interconnects. The goals for next generation interconnects are:

- Cost reduction
- The elimination of lead and other hazardous materials
- Reliability improvement
- Compatible with full automation, and able to sustain a high throughput

During Phase 1 SunPower established a new baseline for cell-cell interconnect and string interconnect that meet all of the contract requirements: cost reduction, improved reliability, and the elimination of lead.

Original Interconnect Design

SunPower's previous interconnect design is featured below in Figure 2.6-1.

Figure 2.6-1 Original interconnect design

From previous testing using the old design, SunPower discovered a potential problem concerning the loss of fill factor due to damaged solder joints as a result of thermally induced stress. Temperature cycling showed that while these interconnects and joints were well within industry standards, joint failure could occur before 25 years.

Next Generation Tab

The initial step in developing a new interconnect design was to characterize the forces on the joints in the old interconnect design by means of finite element analysis. A representative output of the FEA is shown in Figure 2.6-2.

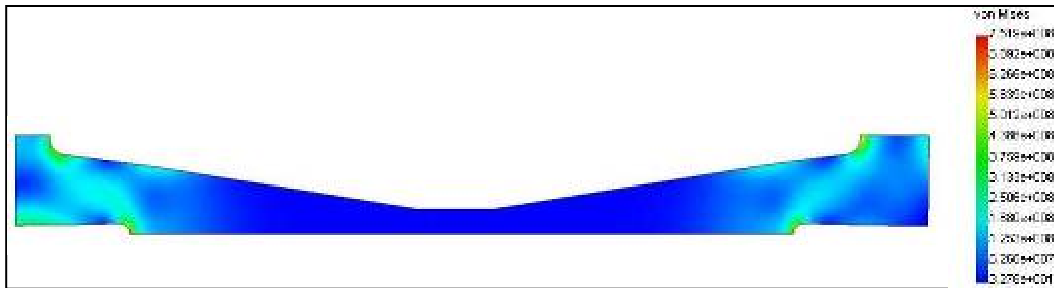


Figure 2.6-2: FEA of partial interconnect

A new interconnect was developed to address the shortcomings of the original design. The new interconnect design has greatly improved compliance, thus significantly decreasing the force on the solder joints and solder pads. This reduced force limits the cumulative solder fatigue that results from thermal cycling and thus improving the reliability of the solder joint.

A significant effort was made concerning the removal of lead from the interconnects. This addresses RoHS requirements and improves the performance of the interconnect. Different runs of samples were fabricated with both SnAg and SnPb interconnect. The samples were tested in environmental chambers for performance degradation in thermal cycling. When using SnAg plated interconnects, the fill factor losses were 4x smaller than SnPb interconnect after 500 thermal cycles. Reduced fill factor loss noted is consistent with literature on lead-free materials. Details of the experimental results are presented in Figure 2.6-3. [6]

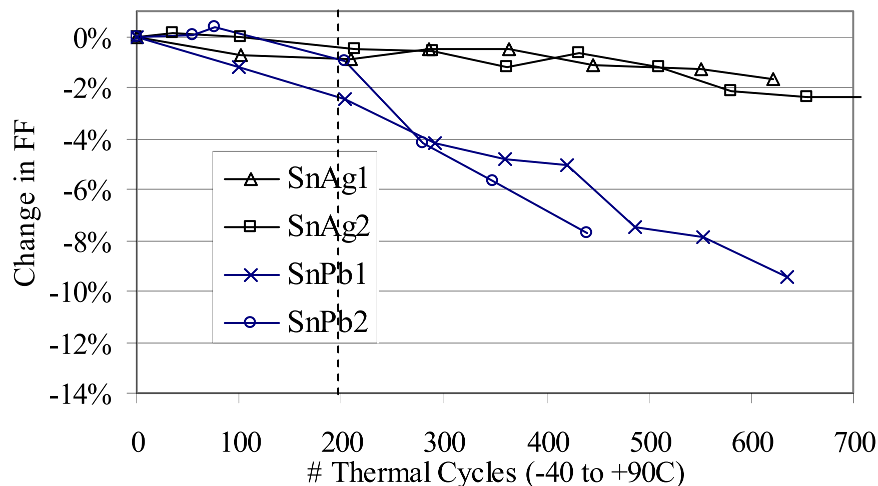


Figure 2.6-3: Fill factor with regards to thermal cycling, different interconnect materials

The next generation interconnect, as described above, has been implemented as the new production baseline and modules using it have been qualified by TÜV and UL.

<u>Next Generation String Busing</u>

A new bus design was developed, enabling fully-automated assembly, preventing cell breakage, and reducing busing costs.

<u>Summary</u>

During Phase I, new cell-cell and string interconnect designs were developed that satisfy all contract requirements:

- Developed and implemented Pb-free interconnect material system. Result was elimination of all hazardous materials AND improvement of reliability
- Improved cell-cell interconnect to decrease force on joints by > 50%
- Developed new circuit formation interconnection suited for automation

2.7 Task 7. Alternative Encapsulation Materials

A comprehensive study of alternative encapsulation materials was performed during the first year of the contract. The materials were evaluated based on electrical, optical, mechanical, and chemical properties, as well as for potential reliability improvement at the module level and cost savings. This effort led to choosing an ultra-fast-cure EVA, STR 15420, as the baseline encapsulant to satisfy the contract goals. Research on silicone based material continued into Phase II due to potential of this encapsulant for enhanced performance at the module level.

Evaluation of alternative encapsulants and justification of material selection

The following materials were selected for experiments based on literature search:

- Silicone
- EVA15420 and other alternative EVA
- Polyvinyl butyral (PVB)
- Thermoplastic polyurethane (TPU)
- Ionomer

EVA 15420

EVA 15420 from STR fulfills the contract requirements of a next-generation encapsulant due to ultra-fast curing that makes it a viable option for a fully automated production line, (50% throughput increase compared to fast-cure EVA 15295) and its high level of UV resistance. 72-cell modules were fabricated and then certified at TÜV to IEC 61215 Edition 2 and UL to UL1703. Figure 2.7-1 shows an EVA 15420 encapsulated coupon.

Figure 2.7-1: EVA laminated cells

EVA 15420's coefficient of thermal expansion is compatible to that of solar cells, which helps avoid delamination and breakage due to prolonged thermal cycling. EVA 15420 is also elastomeric across a desirable temperature range which provides increased

accommodation for expansion related stress. Damp heat testing shows that EVA 15420 undergoes < 5% efficiency degradation after almost 5000 hours of exposure and further reliability testing (UV Exposure, Temperature Cycling, Humidity Freeze Cycling) data proves it to be an acceptable encapsulant, suffering only a 0.94% efficiency drop.

Silicone

Silicone was evaluated due to its potential for high transparency and superior reliability. It has somewhat higher transmission than EVA in the visible range of the solar spectrum and much higher transmission in the UV region, cumulative a 2-4% relative gain compared with EVA based on optical modeling. Alternative encapsulation procedures can be used with silicone, which contains no peroxide catalyst in its formulation. The lack of this catalyst eliminates degradation of the vacuum pump and laminator diaphragm due to peroxide compounds. Silicone does not generate an acetic acid byproduct which could provide a long term reliability increase over current encapsulation materials. Silicone is generally fire resistant (class A rating) which would allow more variability in module design and PV applications allowing for possible simplification and cost reduction.

Silicone encapsulation was found to perform very well in extended damp heat testing, but during Phase I significant challenges remained. In particular, delamination in extended humidity freeze testing, and cell power loss from thermal cycling and humidity freeze testing. Some approaches with Silicone such as liquid Silicone/EVA were eliminated due to significant degradation of efficiency under UV exposure, and work continued into Phase II.

Alternatives

The table below summarizes the results of testing on all alternative encapsulation materials.

Table 2.7-1: Summary of testing of alternative encapsulation materials

		Alternative EVA					
Critical to Quality	**Merit**	**EVA 1**	**EVA 2**	**EVA 3**	**PVB**	**TPU**	**Lonomer**
Efficiency gain	Higher transparency	=	=	=	?	?	=
Process improvement	Vacuum free roll to roll lamination	=	=	=	+	+	+
	Re-workability	=	=	=	? +	? +	? +
	Higher throughput	? +	=	?=	? +	? +	? +
No corrosion to manufacture equipment, diaphram and the final modules		=	=	=	+	?	+
Improved reliability		=	?	=	-	-	?
Lower cost	Direct material cost	=	=	=	?	-	=
	Simplified design	=	=	=	?	?	=

"+": possible gain
"-": possible loss
"=": possibly equivalent to current EVA15295 or 15420

Evaluation results of alternative techniques

"New Industrial Solar Cell Encapsulation" (NICE) is a non-polymer alternative to the traditional EVA module encapsulation developed by Apollon Solar. Initial investigation at small size modules level show that the NICE approach has the following advantages:

ability to process ultra thin wafers, potential for superior reliability and potential for lower cost. However, our tests also show two strong disadvantages: the reflection from the back surface of the front glass reduces module efficiency by more than 5% relative, and there is risk that the package would not by reliable in the field. Based on the data we have at this time and given the timeline of the contract, we believe there is a low probability that the NICE approach will be the best choice for next-generation encapsulation for our cells.

2.8 Task 8. Modified Packaging Configuration

Alternative diodes configurations, junction boxes, glass coatings and other package related features to reduce manufacturing costs and improve product quality were investigated during Phase I of the contract.

Bypass Diodes

Based on the results obtained during investigation of bypass diodes, we eliminated on-cell bypass diodes from consideration as a result of power loss from the accumulation of forward voltages in conditions were much of the module is shaded. However, analysis showed the potential for increased energy output in partial shade conditions with the addition of bypass diodes in certain configurations. During Phase II, work continued on in-laminate bypass diodes.

Junction Box Selection

Evaluation of junction box alternatives led to the selection of the MIM Tecnosolar as a new baseline. The box is non-potted, IP-65 rated, and is injection molded with a UV stabilized polycarbonate blend. A Gore-Tex breather patch allows any moisture that penetrates the plastic to escape. Plastic moldings prevent water from entering where the cables penetrate the box and a gasket on the lid prevents water from entering the box.

Glass/Superstrate

The reflection from the front surface of uncoated glass is ~4%, therefore extensive studies were done to evaluate anti-reflective glass coatings (ARC) for improved value and reduced cost. One candidate was found to be unstable in accelerated tests. Two candidates were down-selected for further studies: vendor 1 (multi-layer sputtered ARC) and vendor 2 (single layer sol-gel ARC). Testing showed both to have a benefit at standard-reporting conditions of ~2.7% (i.e., reduction of reflection in normal incidence to 1.3%). Outdoor and accelerated testing results are in section 2.14. Additionally, glass thickness for 72-cell modules was reduced from 4mm to 3.2mm – it provides cost reduction and a 0.13% relative efficiency increase.

Figure 2.8-1: Field testing of modules with various ARC glass at Sandia National Laboratories.

Frame
Traditional frames extend above the front plane of the glass surface, which leads to soil accumulation at the bottom edge of the module. Field testing of small prototypes verified that no-edge frames eliminate this problem. Investigation into plastic frames revealed that significant potential exists because of the flexibility of new module features and the elimination of the need for grounding, but simple replacement of existing metal frame with injection molding using current frame design is not advantageous. Work with plastic frames continued in Phase II.

2.9 Task 9. Reliability Testing of Improved Modules

The PV industry possesses only a small amount of long-term field data, which poses a challenge concerning accurate reliability testing in line with the contract goals of 30 year warranty. PV modules are generally measured in terms of failure rate and lifetime, the failure rate being the percentage of modules that fail before the lifetime. The focus of reliability testing is on product lifetime, as failure rate is a process control matter.

The key issues surrounding accurate reliability testing are that it removes all subjectivity, and is based purely on the physics of failure. As such, testing is based on failure analysis, degradation analysis, accelerated testing, and failure mode interaction. The categorization of failures into failure modes allows for direct associations between cause and effect to be made.

Testing Protocol
Testing protocol is built around failure analysis, degradation analysis, accelerated testing, and failure mode interaction. There are three main methods of failure analysis: I-V curve assessment, alternative non-destructive methods, and destructive methods. I-V curve assessment involves viewing the output of the panel, and can be further subdivided into the I-V components such as Isc, Voc, FF, and dark I-V characteristics. Non-destructive techniques being investigated in Phase II include IR imaging, which could potentially show any cell possessing abnormal thermal characteristics. Destructive techniques allow for complete analysis of individual components within the solar module
Interaction between failure modes can be problematic because their mixed effects are unknown and very difficult to predict. Because of this there must be a high degree of isolation in order to properly define each failure mode.

<u>Reliability Results for Module Modifications</u>
Reliability testing in Phase I included the following

Solder Fatigue
An important effort was devoted to solder joint failure and even more work was done in Phase II. Solder fatigue was evaluated via examination of solder voids and creep.

Solder voiding is a procedural defect impacting the rate of failure before the maximum lifetime achievable for a certain module design. Voiding was evaluated concerning manual soldering, and ML soldering using vision analysis. Figure 2.9-1 demonstrates good and poor voiding of a magnetic induction solder bond. A clear correlation was demonstrated between the importance of voids and the time to failure.

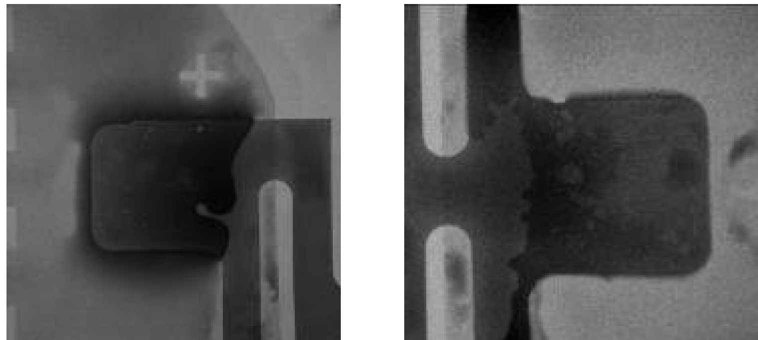


Figure 2.9-1: Good and poor voiding

Different soldering techniques give different degrees of control on the formation of voids, leading to different practical lifetimes. Figure 2.9-2 shows the results for the technology we chose to pursue in Phase II (magnetic induction) and one that gives very variable results (hot air, Figure 2.9-3).

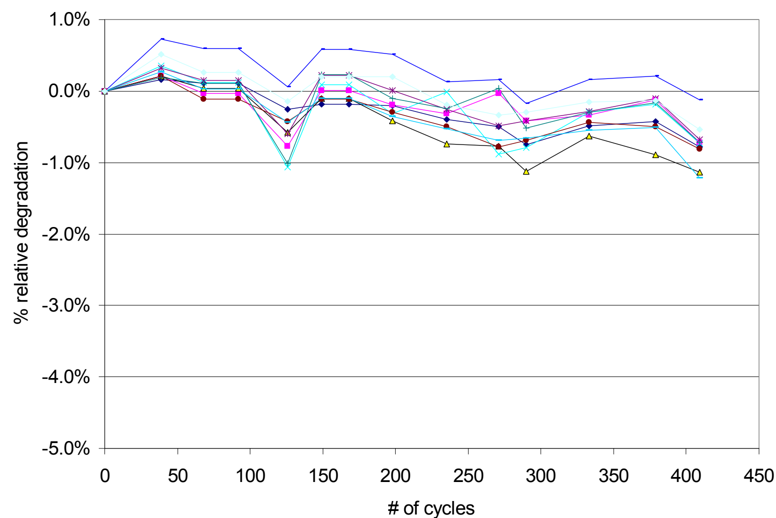


Figure 2.9-2: Thermal cycling results for magnetic induction soldering.

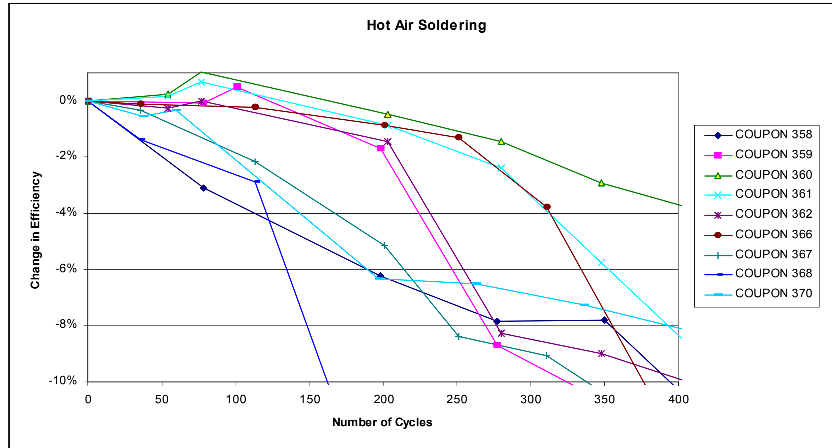


Figure 2.9-3: Thermal cycling results for hot air soldering.

Creep mechanisms determine the maximum lifetime of solder joints for a certain design, regardless of the process. Our modules are unique because of the use of back-contact cells allowing solder joints to be much smaller than required of standard solar cells. Creep is induced by thermal cycling. Acceleration of solder fatigue is one of the most studied reliability topics for semiconductor components and assemblies, however it is still very difficult to get accurate predictions of real performance in the field based on accelerated tests. The acceleration factor depends on the other parameters of the design: the thermal mismatch between the different materials and their relative elasticity. The combination of these sets of parameters determines the stress that will be exerted on the solder joints during thermal cycling. Due to improved reliability performance (see section 2.6), SnAg solder joints have been adopted, using a magnetic induction soldering process, with further refinement occurring in Phase II.

Many samples made with different processes and designs have been tested to failure. Since the beginning of the project, the lifetime of the samples under thermal cycling has increased by a factor of five, considerably lengthening the tests. To accurately study the acceleration factor of solder failure under thermal cycling, we recognized that it is not enough to monitor the output power of complete modules because of the parallel-series connections that complicates the analysis. Also, the series resistance of solder joints in thermal cycling is known to fluctuate somewhat chaotically instead of increasing monotonically. For these reasons, the proper way to study solder joint degradation is to monitor individual joints. The difficulty is that we still need to make sure the solder joints in the experiment see the same stress as in complete modules. In Phase I an experiment was started wherein 104 solder joints are monitored on 12 mini-modules. The goal is to compare the acceleration factors for different solder materials and module designs.

Encapsulant Degradation

The main tests concerning encapsulant reliability are humidity freeze (HF) and damp heat. HF is the fastest test to show possible delamination, which is the most significant failure mode. .Figure 2.9-5 shows an example of delaminated encapsulant following HF testing.

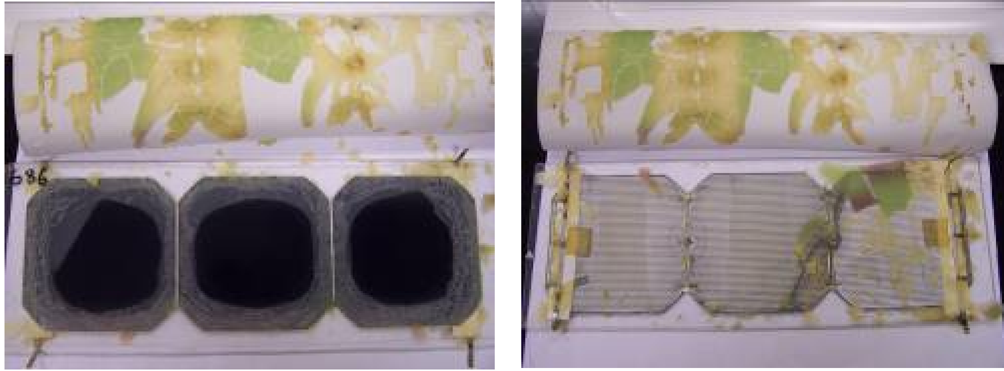


Figure 2.9-4: Humidity-Freeze delaminated this TPU encapsulated coupon (front view-Left; back view-Right)

Other encapsulation reliability tests, such as qualitative color/bubble analysis, and UV related degradation were applied also, however good adhesion tended to be the governing principle concerning encapsulants.

Junction Box
Junction box failure analysis is based around heat dissipation, adhesion and leakage. These are all tests that can be directly applied and yield very accurate results. We have investigated junction boxes from various vendors. We have tested the parts using different reliability tests, which include: humidity freeze, thermal cycle, damp heat, pull test, heat test.

2.10 Task 10. Automation Development: Alternative Equipment Design

At the end of Phase I SunPower had identified the state-of-the-art technologies for successfully handling very thin wafers. The enabling technologies include both: pick and place robot systems with end effectors and wafers aligners. This section outlines the vendor collaboration for testing thin wafer handling automation. Preliminary tests with prototype units are showing promising results in handling wafers as thin as 140 μm.

Vendor collaborations:
SunPower has selected four equipment vendors for development collaboration: vendor 1 for SCARA robots to transport, hand-off, and store thin wafers, vendor 2 for parallel robots, vendor 3 for wafer stringing, and vendor 4 for string handling.

The SCARA robots with special end effectors are designed to replace most of the previous generation handling automation such as belts and conveyors. The design of these robots has been demonstrated to be very efficient for pick and place operations because of the limited mechanical stress transferred to the wafer surface. Moving slower and diminishing the number of steps for transferring the wafers avoids both indirect stress such as vibrations, and direct stress such as sudden impacts. For this reason the SCARA robots have been designed to pick up and place multiple wafers simultaneously.

We tested the performance of a SCARA robot on a multi-lane system at the vendor 1 site. During the test, 100 wafers were run in each lane. Wafers with different thickness and diameter were positioned on each lane. Most of the breakage that occurred was not due

to the wafer thickness but instead to incorrect motion of the robot and improper wafer alignment at the unloading module.

Parallel robots systems are being developed and tested by vendor 2. The parallel robots are designed to move one wafer at the time at very high acceleration and speed. This approach, while opposite to the one previously described, is necessary for those operations that require the extreme versatility of a single wafer processing. A small numbers of wafers as thin as 150 µm were run with a prototype test bed (shown below in Figure 2.10-1). The results are promising and the vendor is currently finalizing the set-up.

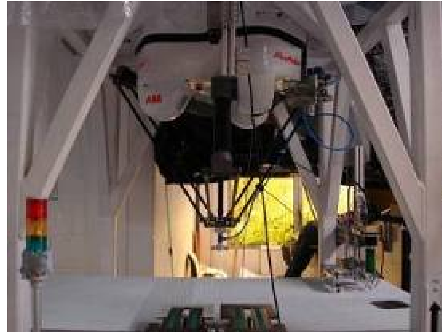


Figure 2.10-1: Set up with buffer system and parallel robot

We are collaborating with vendor 3 to develop stringing tools capable of handling with very high yield wafers as thin as 150 µm. Among the features designed for thin wafers handling are the special grippers that pick the solar cells from a stack format. The wafers are separated by interleave paper in the stack, so a special design was made that allows the cells to be mechanically separated while air is flowing in between. Other features for thin wafers handling are: the design of the vacuum cups to avoid overstressing the wafers and timing of the vacuum between grippers and surfaces. A picture of a gripper is shown in Figure 2.10-2.

Figure 2.10-2: Wafer gripper used for cell stringing

String handling and placement is done with 6-axes articulated robots developed by vendor 4. These robots give us the flexibility to handle the string with a very high speed during transfer, but also allow for a reduced speed during pick-up and placement of strings. A picture of such a robot is shown in Figure 2.10-3. This string pick head will pick up the string, hold it in midair at the vision inspection stage and dial in the accurate position of string before placing it on the soldering table. Initial tests at vendor's site handling 25 strings with 166 µm thick wafers resulted in 100% yield.

Figure 2.10-3: Robot for string handling

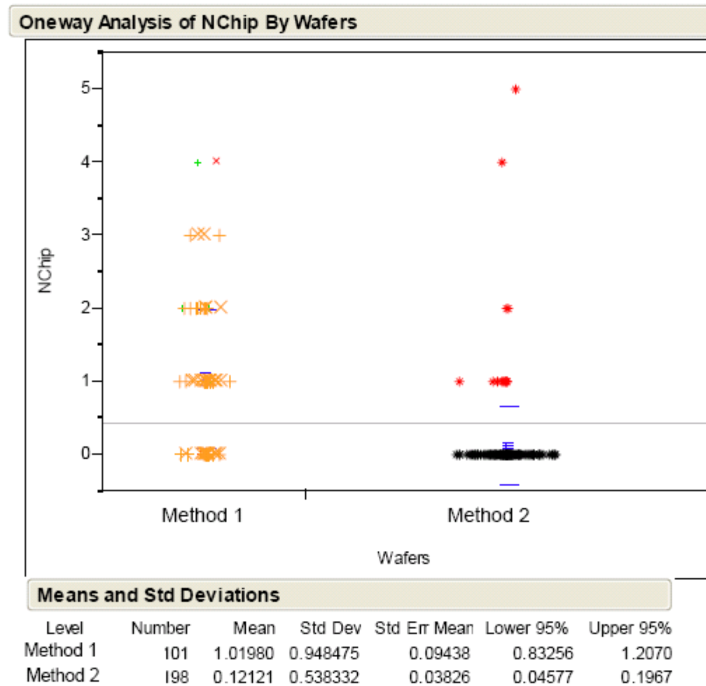
Summary
Automated handling of ultra-thin wafers is a challenge in the manufacturing environment. SunPower selected four equipment vendors for development collaboration: vendor 1 for SCARA robots to transport, hand-off, and store thin wafers, vendor 2 for parallel robots, vendor 3 for wafer stringing, and vendor 4 for string handling. Testing on all four tools of wafers as thin as 150 μm have resulted in promising results and further work on ultra-thin wafers automatic handling will continue under the SAI contract.

2.11 Task 11. Pilot-line Implementation of Wafer Edge & Surface Modification

For this task we have continued the work started in Phase I Task 3, focusing on optimizing the process for sawing thinner wafers, reducing the damage of the as-sawn wafers, and on designing and testing a pilot line tool for wafer damage etch optimization.

Wire Saw optimization for thin wafer cutting
Literature searches were performed for understanding and testing the effect of the wire saw process on the edge and surface modification of very thin wafers in order to optimize wafer breakage in subsequent processing steps.

Experiments were performed with a new wire saw tool purchased by SunPower outside the contract. Analysis of the effects of various parameters from the slicing process was done using an automated visual inspection tool, also purchased outside the contract. The metrology tool is designed to detect and quantify "groove" defects on the wafer surface, and chip and crack defects on the wafer edge. An analysis of the edge chips on the wafers sawn by two different sawing tool and processes is presented below (Figure 2.11-1).



Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
Method 1	101	1.01980	0.948475	0.09438	0.83256	1.2070
Method 2	198	0.12121	0.538332	0.03826	0.04577	0.1967

Figure 2.11-1: Comparison of edge chips for wafers sawn with different processes.

A seven factors designed experiment was conducted to determine the effect of wire saw parameters on the surface quality (magnitude of saw marks and waves) and the Total Thickness Variation (TTV) of the wafer surface. The machine, slurry and initial wire conditions were controlled to minimize run-to-run variation that could affect the results. 140 sample wafers, distributed across the ingot length were taken from each cut. The resulting model predicts that the input factors of feed speed, input slurry flow, and output slurry flow have a significant impact on the wafer quality. As expected we did see significant differences in the model parameters for the position of ingots, likely due to the changes in wire quality throughout the cut.

Experimental data suggests that minimizing the feed speed, input slurry flow and maximizing the output slurry flow will minimize the overall TTV of the wafer. We have found that reducing the wire speed also reduces the wafers TTV. The model predicts that a higher slurry temperature will also minimize the wafers TTV. We theorize this is due to the effect of temperature on slurry viscosity: as the temperature of the slurry increases, the viscosity decreases which may decrease the impact energy of the slurry on the ingot and the hydrodynamic pressure in the sawing channel. Both of these effects may decrease the amount of material removed by the wire/grit in the process, and thus alter the thickness and TTV of the wafers.

<u>Wafer edge shaping</u>

During Phase II we investigated the effect of shaping the wafer edges by using laser guided water jet. 125-mm pseudo-square silicon wafers processed through wire saw were used. Samples with a particular type of edge defect were selected for water-jet process. These defects were quantified prior to water-jet processing at the vendor. Three tests were conducted: group A) removal of entire wafer edge perimeter; Group B) removal along all four wafer straight edges only (i.e. excluding the corners); and Group C) removal

of the one wafer edge corresponding only to the epoxy-side ('epoxy-side' refers to adhesion-side of ingot during wafer saw operation). Outcome of the tests were as follows:

1) Edge chipping quantification before and after the water-jet process showed an overall reduction in chipping.
2) However, significant chips remained and some areas possibly experienced added chipping in new areas:
    a. New chips were present near the corners along the straight edge after water-jet on Group B. Process optimization may eliminate straight-edge chipping.
    b. Chips remained on Group A corners. Process optimization is needed with non-straight edges.
3) Morphology changes were significant.
    a. The resulting wafer dimensions were impacted when more than 1 side was processed, listed by group: A) non-signficant, B) 2 mm, C) 0.2 mm.
    b. Additional rounding of corners resulted on Group A.
4) Other: Some burn marks and residues appeared on some samples along the processed straight edges.

Based on these experimental results we concluded that wafer edge processing using laser guided water jet is not a cost effective solution to improve the mechanical strength of the ultra thin wafers.

<u>Pilot line tool for damage etch optimization</u>
Wet processing of solar wafers is practiced mostly for cleaning and surface modification purposes, both of which are critical to high efficiency solar cell performance. Currently, these processes are generally conducted in batch mode where an entire cassette of 50 wafers is processed from one step to the next (or one bath to the next bath). This manufacturing technique has many limitations including high cost of the tool, consumables and PM cycles due to draining and filling large baths. An in-line version of a clean step and/or a surface modification provides considerable improvement but comes with the added risk of thin-wafer handling in an in-line transport system.

Having concluded at the end of Phase I that acid damage removal is an important step for strength and performance, and that an in-line system is the most cost effective manufacturing method, we have identified a vendor and specified a prototype tool design for conducting tests with appropriate materials, chemical and mechanics for effective handling of very thin wafers.

The pilot horizontal etch tool for experiments on optimization of acid damage etch removal is currently being built at the vendor site. In order to address high throughput thin wafer (post sawing) processing needs, we have done tests with the vendor's existing wet processing tools to study the performance of thin wafers at different transport speeds. Water was used as the processing liquid since simply wafer movement was being studied. While this data will certainly vary somewhat as different chemicals are used for various process steps, the overall behavior of the wafers can be generalized from studying their movement in water.

Two different wafer thicknesses were tested (190 μm and 165 μm), and two different speeds, one 60% more than the other. Wafers were fed one after the other, first at speed 1 then repeated at speed 2. The thicker wafers moved consistently through the wet processing tool, maintaining the wafer to wafer distance and remaining aligned independent of speed. The thinner wafers, however, showed similar consistent behavior at speed 1, but at the faster, speed 2, the wafer to wafer spacing began to vary to the point that there was overlap of some wafers as well as the wafers became skewed relative the transport direction, further disturbing the movement. The solution that will be explored to address this issue for thin wafer handling will be slightly more weight of the rollers that lightly hold the wafers down in the wet processing tool.

2.12 Task 12. Pilot-line Implementation of Metallization on Thin Wafers

Phase II work was focused on testing the modifications to the metallization process that enable very thin wafers (150μm) processing in manufacturing; namely, modifications of the plating equipment and mask changes at the solar cell level.

Modifications of Plating Equipment

The plating process involves successive dipping of the wafers in various chemical solutions. By experimentation it was found in Phase I that very thin wafers bow more than standard thickness wafers during metallization process. A modified metallization jig was designed that enables cost-effective processing of wafers with a thickness ≤150 μm.

A total of 144 wafers were used in the pilot runs of the new jig. Three different wafers thicknesses were tested: 100 μm, 125 μm, and 150 μm. The wafers were divided in two batches, with each wafer thickness group processed in each batch. The resulted metal thickness was measured at the center of wafers.
Wafer bowing measurements for batch #1 and #2 wafers are showed in Figure 2.12-1.

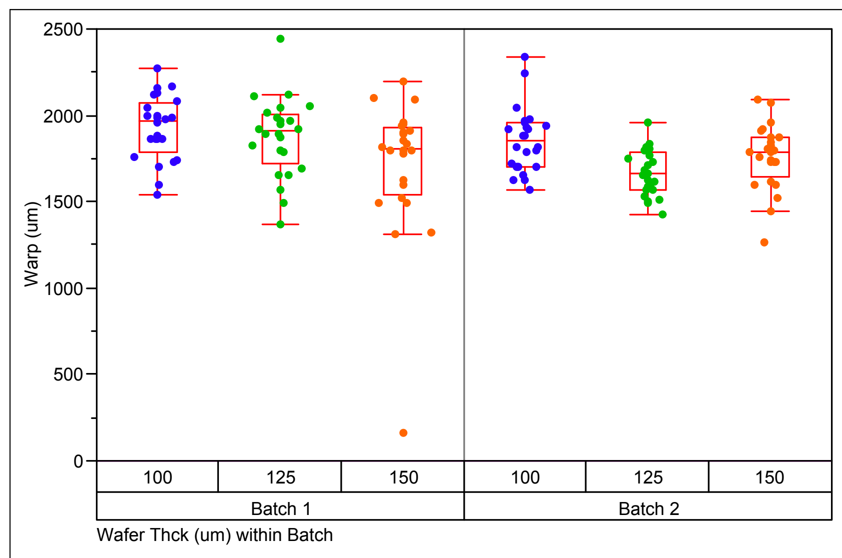


Figure 2.12-1: Wafer bowing/warp measurement on pilot run wafers.

Trials of jig modification were successful for wafers as thin as 100μm. No wafers breakage and edge chip was noticed during the pilot plating runs. Pilot run wafers show no chemical staining. Warping of the wafers was not observed in the plating tank or immediately after unloading wafers from plating. Wafer warping started slowly overnight and the warping itself could clearly be observed. There is only a slight difference in warping degree among 100, 125, and 150 μm thick wafers. This indicates that our current design rule on mask pattern and required plating thickness are near upper limited.

2.13 Task 13. Pilot-line Implementation of Alternative Interconnect & Encapsulation

EVA 15420 was selected as the new baseline encapsulant at the end of Phase I as it fulfills the contract requirements of a next-generation encapsulant. During Phase II the key focus was on developing a silicone based encapsulant offering higher light transmission (2-4% relative gain) and improved environmental protection.

Silicone

SunPower has continued work on silicone encapsulants with Dow Corning, including several silicone cross-linking recipes designated as "soft", "medium" and "hard".

For first-cut reliability testing of silicone encapsulant evaluation, coupons using medium crosslinking density silicone passed visual test after 10 cycles of humidity freeze but had 2 to 20% efficiency degradation (Jsc, Voc and FF degraded up to 6~8% relative). Failure analysis indicated that this was not due to shunt resistance degradation, but a mechanism that increased recombination.

Suns-Voc studies indicated that the lifetime of cells after 10 cycles of humidity freeze encapsulated with silicone degraded significantly. Three configurations passed this test with no degradation:

- SunPower Gen B cell with a "hard" silicone on the backside,
- SunPower Gen B cell with high Tg (soft) silicone on the backside,
- SunPower Gen C cell even with "soft" silicone on the backside.

The result indicated that degradation of silicone coupons is not due to CTE difference of encapsulant.

Reliability testing for coupons laminated with "hard" silicone indicated that the lamination process of the backsheet is very important. Crosslinking density of silicone was tuned trying to improve reliability. With high silicone crosslinking density, the coupon didn't show any delamination after 10 cycles of humidity freeze. However, efficiency degraded significantly.

We observed a trade off between improving "hard" silicone adhesion to the backsheet through incorporation of certain adhesion promoters and its subsequent performance in reliability testing. The incorporation of an adhesion promoter led to bubble formation in the laminate. Work continues to understand the optimum lamination process for these materials as the improved adhesion is a desired quality. Initial results also indicate that the type of backsheet used influenced the cell reliability performance of those silicone coupons. Further work to understand this interaction is planned.

Transmission

The benefit from improved transmission of silicone was demonstrated. We have measured a 1% increase in J_{sc} post-lamination on coupons with silicone as compared to those laminated with EVA. Optical modeling was done to investigate the reflection between silicon/cell and silicone/glass. The results indicated that the reflectance from silicone/cell interface is small. Calculation also showed that the reflectance from glass/silicone interface is negligible. The impact of refractive index of silicone on current was also evaluated. With AFG stippled glass, SunPower cells laminated with a high refractive index silicone showed a higher J_{sc} change pre- and post-lamination. The conclusion is that this gain is due mainly to improved transmission of the silicone itself compared to EVA.

Polarization

A two factor, two level DoE was designed to study the polarization effect of silicone coupons. The factors were: silicone composition and layer thickness. Initial result indicated that silicone with a low polarity layer showed less polarization effect and that thickness is not a significant factor.

Three repeats of 3-cell coupons with silicone encapsulant were tested against polarization. The initial good result was not repeatable. Root cause is under investigation. Cell strings were sent to Dow Corning for 32-cell module fabrication with silicone. Also, about 50 single cell structures were sent to Dow Corning to facilitate this reliability study.

Interconnect

Re-design of the cell-to-cell interconnect was accomplished during Phase II of the contract. This tab shape change is expected to deliver improved electrical performance with no cost increase. Two versions of interconnect tabs with smaller joint area were designed and prototypes were fabricated.

Test results at 900 temperature cycles (-40C/+90C) shows performance for one pad size that is comparable to the control group. The tabs with the smallest joint area (1.5mm) are showing larger drop in performance after 800 cycles, but the tabs with the 2.0mm joint area continue to perform as well as the joints with the standard joint area after 900 temperature cycles as shown in Figure 2.13-1. Note that the performance far exceeds that of international PV standards (e.g., IEC 61215 allows a 5% loss in 200 thermal cycles).

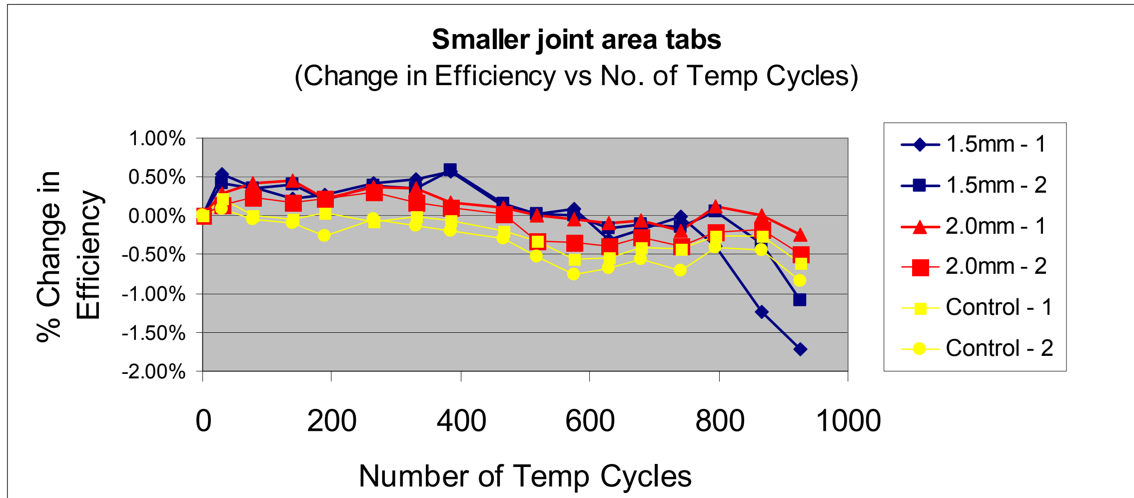


Figure 2.13-1: Performance of smaller joint area tabs in temperature cycling

Additional experiments were conducted to evaluate the use of pre-forms of solder with flux core as an alternative to solder paste (solder paste has high surface area so it requires a high flux percentage, which increases cost and can cause splattering during some soldering process). The work was discontinued after the initial evaluation due to the resulting increased process complexity in using solder pre-forms and the confirmation that splattering is not a problem with high-throughput magnetic-induction soldering.

2.14 Task 14: Pilot-line Implementation of Modified Package Configuration

Work performed under Task 14 was directed at upgrading the module package configuration by developments in junction boxes, glass, in-laminate diodes and frames, as well as new module design.

Anti-Reflective Coated Glass

Extensive accelerated and field testing continued on anti-reflection glass in Phase II. The work focused on testing of the single layer sol-gel ARC since the side-by-side comparison of the coatings performed by Sandia National Labs shows a 4% energy gain relative to uncoated glass for the sol-gel coating as compared to 2.7% from multi-layer coating, as shown below in Figure 2.14-1. Additionally, field testing of the multi-layer product revealed a failure mode from water on the surface of the coating. The higher energy gain from the single-layer sol-gel coating is due to better performance with off-axis illumination. More field data on ARC from both Sandia and NREL are presented in Task 15 report.

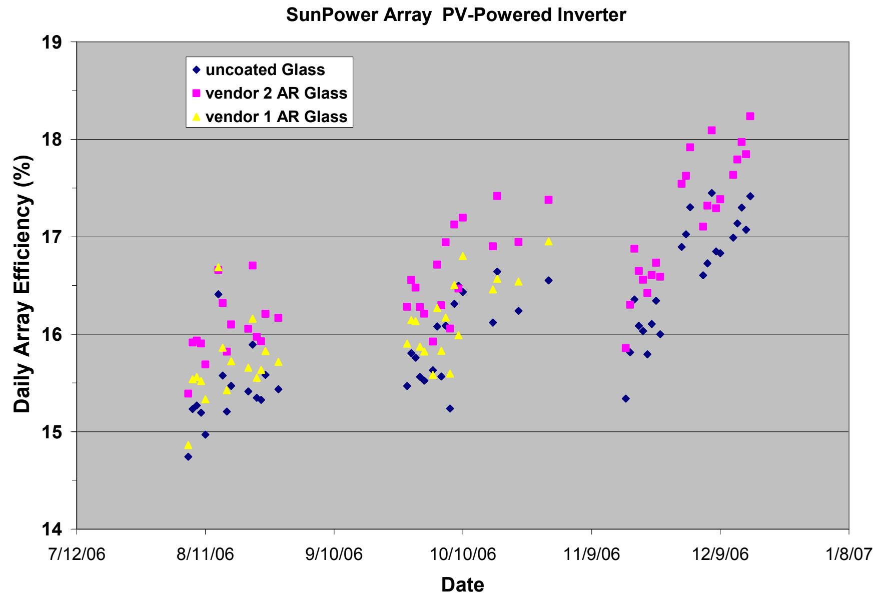


Fig 2.14-1: Field test data from Sandia Laboratories.

Additional beta site were installed in San Jose, CA. We have found that vendor 2 ARC produces consistent 4% gain in energy production as compared to uncoated glass. The modules were inspected for any defects that might have developed over 6 months of installation. On close observation it was reported that there were localized spots on the ARC glass that might have resulted from some kind of debris accumulating on the glass. FTIR analysis confirmed the debris to be plant residue. Discussions are underway with the vendor to better understand the failure mechanism and improve field reliability in a globally deployed product.

We are also testing anti-soiling properties of the sol-gel ARC since the coating is expected to have some level of self-cleaning. It is interesting to note that the data so far suggest that the ARC does have less soiling loss (with about a 1.5% relative loss advantage) compared to un-coated glass (data are shown in the graph below for coupons in flat mounting). Additionally, the ARC glass performs to date better than any off-the-shelf anti-soiling coating that we have studied.

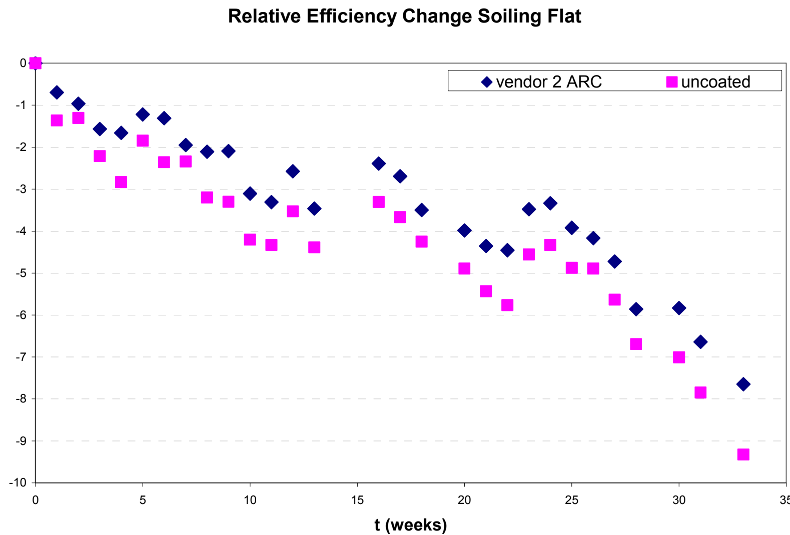


Figure 2.14-2: Soiling test results of AR coated glass and non-AR coated glass

In-laminate Diodes

During Phase II, we constructed two modules with in-laminate diodes, one with diodes in the standard positions and the other with diodes in both the standard positions and in positions which provide shade protection for the bottom half of a module. In installations of modules with a portrait orientation, the top half of a module continues generating power while the bottom part of the module is shaded. The in-laminate diodes performed well in outdoor testing, with no signs of degradation. These results can have a significant effect on system energy delivery by allowing modules to continue producing power in non-optimum conditions.

We received quotations for automated equipment for manufacturing in-laminate diode assemblies which could be integrated into the module during circuit formation. Based on these quotations and other cost estimates, we plan to assess the ROI and benefits of in-laminate diodes in the context of our next-generation products.

Alternative Frames

During Phase II, we held extensive discussions with three plastics vendors. Complying with UL requirements has proven difficult, especially with some design concepts that involve integrated wiring. It is still not clear if any of the available materials are suitable for the demanding requirements of PV modules.

High Efficiency 96-cell Module:

During Phase II, we designed a 96-cell module that has many benefits: higher area efficiency, lower cost and better installation costs. The cell side edge gap was reduced to 13mm from current 16mm. This provided an additional 0.1% absolute efficiency gain, which along with interconnect improvements made within the contract and cell improvements (outside the contract) was critical for the path to 20% total-area module efficiency.

A champion 96-cell module has been measured by Sandia National Laboratory. The data at 1 Sun STC shows a power output of **327.6 Watts** and a total-area-efficiency of **20.10**%. Figure 2.14-3 shows the confirmation of this new record achievement, with the inset showing a picture of the module.

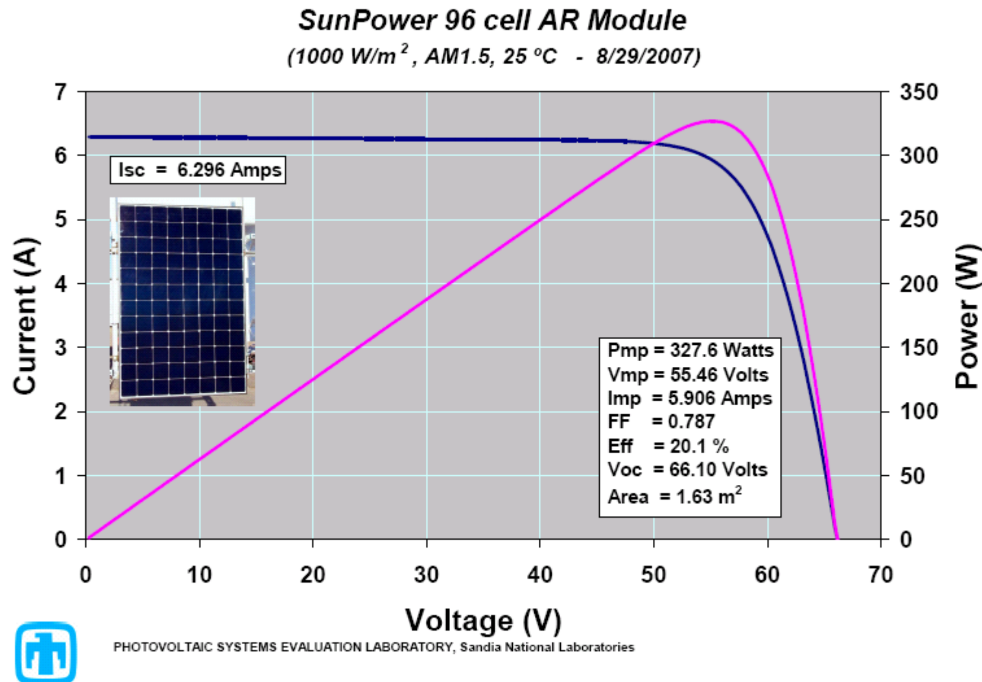


Figure 2.14-3: STC results for 96-cell champion module

The rated output power of the 1st generation at STC will be **325W.**

Summary

Excellent progress was made on this task during Phase II on identifying new packaging methods that lead to improved efficiency and reduced cost/rated Watt. New JBoxes with improved cost, suitable for automation and compatible with 30 years reliability were identified and implemented. Prototype modules with in-laminate diodes were manufactured and evaluated. Consistent energy production gain of 4% from sol-gel ARC was demonstrated. A new module design led to a champion 20.1% total area efficiency module measured at STC by Sandia National Laboratory.

2.15 Task 15. Reliability & Field Testing

The work under this task was focused on reliability testing of various technologies developed during Phase II. Test to failure was also performed to develop models that predict reliability of the next generation modules in the field.

Micro-cracks

A characteristic of our cells is the presence of a thick layer of metal covering most of the backside of the wafer. This configuration results in large stress during thermal cycling and can cause cracks in the silicon substrate during manufacturing as well as in the field. Both theoretical and experimental studies have been conducted to understand this cracking

mechanism and the important parameters that influence its amplitude. Several modifications in the cell design have been implemented and have allowed us to increase the thickness of the metal layer without causing degradation during the life of the module.

Cell interconnect and solder joint configuration

At module level, the biggest difference between our modules and conventional ones is the way the cells are stringed from one to the other. Our cell interconnects are all on the backside instead of being interwoven from back to front. We have determined the life expectancy of a new interconnect design by using a combination of theoretical and experimental studies.

1. *Modeling of solder joint fatigue*

Finite-element analysis was used first to calculate the stress in the cell and interconnect system as a function of temperature. Then, specialized software calculated the stress-strain relationship during thermal cycling for different thermal profiles applied. The area enclosed by the stress-strain cycle is the strain energy ΔW per cycle for a particular profile. Experiments with integrated circuits soldered on printed circuit boards have shown that the damage to a solder joint is proportional to this strain energy per cycle. As a consequence, the inverse ratio of the strain energy for two different thermal profiles gives the acceleration factor between these two profiles [7]

Tin-Lead Eutectic Solder

For the eutectic solder, we have used the software SRS to calculate the strain energy for different thermal profiles. We simulated thermal profiles both for several locations in the world and several programs used for accelerated tests. Figure 2.15-1 shows a typical hysteresis loop obtained with the software. Table 2.15-1 shows the result of the modeling for two locations and three accelerated test conditions.

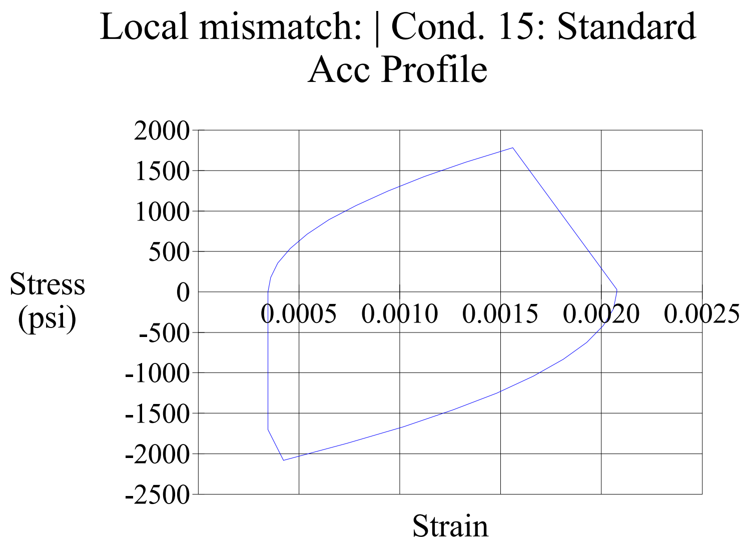


Figure 2.15-1: Hysteresis loop for SnPb solder joint modeled with SRS software

Table 2.15-1: Results from AF modeling with the SRS software package for SnPb solder joints.

Phoenix

Profile	Max temp C	Min temp C	dwell time min	Cycles Per Day	Joint Location	Acceleration Factor	# of cycles for 25 yrs	# of days
Standard	90	-40	40	6	Inner	**5.4**	1692	282
					Outer	**4.1**	2253	375
High Temp	125	-40	40	5	Inner	**19.4**	471	94
					Outer	**19.1**	477	95
Long Dwell	90	-40	80	4.5	Inner	**5.8**	1568	348
					Outer	**4.4**	2063	459

Weisbaden

Profile	Max temp C	Min temp C	dwell time min	Cycles Per Day	Joint Location	Acceleration Factor	# of cycles for 25 yrs	# of days
Standard	90	-40	40	6	Inner	**10.1**	902	150
					Outer	**8.7**	1050	175
High Temp	125	-40	40	5	Inner	**36.4**	251	50
					Outer	**41.1**	222	44
Long Dwell	90	-40	80	4.5	Inner	**10.9**	836	186
					Outer	**9.5**	962	214

Lead-Free Solder

For the lead-free solder hysteresis loops were modeled for 21 accelerated lab and 25 field profiles. Strain energies were calculated for each of these loops. In order to generalize these results to any lab and field profile, we fitted them to algebraic models with input variables describing the shape of the profiles. We now have a spreadsheet calculator where the inputs are ambient temperature and irradiance for each hour of the year, as well as the characteristics of the accelerated test profile, and the output is the global acceleration factor between the lab conditions and the field conditions for one year. We are using this spreadsheet to study the effect of different climates around the world and to search for ways to further accelerate our thermal cycling tests.

2. *Experimental study of solder joint life*

    a. Test set-up

Two experiments were performed to evaluate solder degradation behavior. Both experiments used the same thermal cycling profiles as seen in Figure 2.15-2. Two interconnect designs (A and B) which relieved different thermo-mechanical stress on the joints, were evaluated. PV module construction with conventional cells typically does not use any interconnect stress relief between solder joints. Because of size restrictions it was not feasible to use full size PV modules. Three-cell PV minimodules were used as the test vehicle.

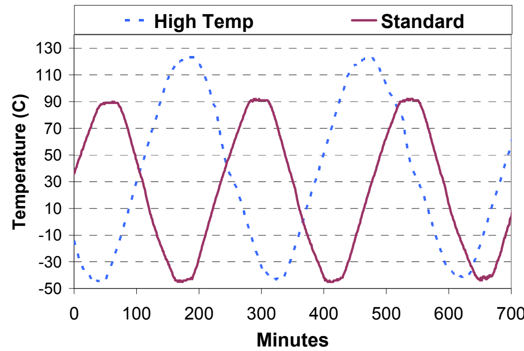


Figure 2.15-2: Thermal cycling profiles
High Temp Profile: -40 to 125˚C
Standard Profile: -40 to 90˚C

In the first experiment, individual solder joints were monitored in-situ as the PV minimodules were subjected to thermal cycling. A four wire resistance measurement of each joint was performed in real time to monitor joint failure as seen in Figure 2.15-3. This technique is the most direct way of detecting failure of individual joints.

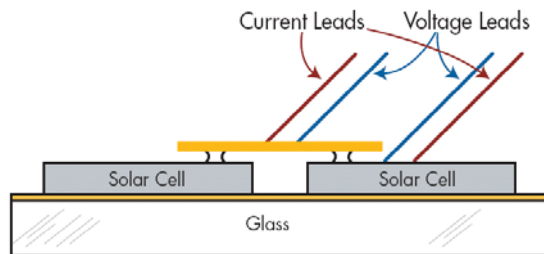


Figure 2.15-3: Monitoring setup

In the second experiment, a set of PV modules was subjected to thermal cycling and periodically flash tested. To evaluate the effect of different solder alloys on module series resistance degradation, PV minimodules were thermally cycled and periodically flash tested. PV minimodules were built with SnPb63 and SnAg3.5 using interconnect A. Ten PV minimodules of each solder alloy were built for each profile.

b. Results

The results of individual joint monitoring are outlined in Table 2.15-2. To date about 50% of the SnPb63 joints built with interconnect B have failed. Very few joints built with interconnect A have failed.

Table 2.15-2: Individual monitoring results for SnPb63 joints

		Interconnect A	Interconnect B
Profile	**Cycles Completed**	**Joints Failed**	**Joints Failed**
Standard	2300	0.0%	50.0%
High Temp	1130	2.5%	47.5%

Cumulative failure of solder joints built with interconnect B is seen in Figure 2.15-4. The interconnect design has proven to have a significant impact on solder joint life.

A model was developed in Spice to demonstrate the effect of individual joint failure on PV minimodule series resistance. A two diode equivalent model was used for the solar cell and an equivalent resistor network was used to model the interconnect and solder joints. Measured solder joint resistance values were used as inputs to the model. Steps in the series resistance curves indicate individual joints reaching end of life. One joint reaching end of life has a significant impact on PV minimodule series resistance, as seen in Figure 2.15-5.

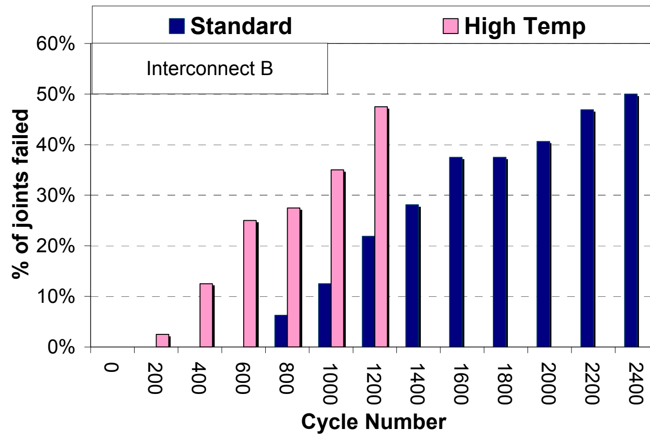


Figure 2.15-4: Joints failed with interconnect B

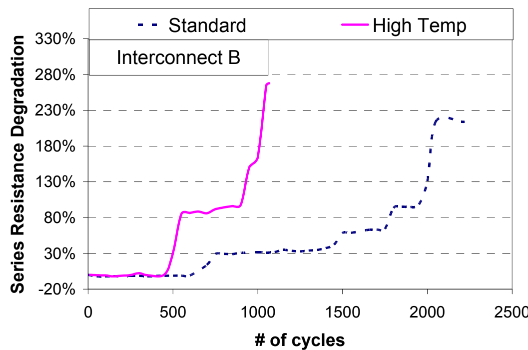


Figure 2.15-5: PV minimodule modeling results

Flash test results from thermally cycled PV minimodules of the second experiment are shown in Figures 2.15-6 and 2.15-7. All of these PV minimodules were built with the more robust interconnect A. Each data set is the average degradation of ten minimodules. In both thermal profiles, thermal cycling induced higher increases in the series resistance of SnPb63 minimodules compared to SnAg3.5 minimodules. No degradation of the PV minimodules built with SnAg3.5 was observed after about 2000 cycles. This is 10 times the duration of industry standard certification tests. As expected from literature data, the SnAg3.5 solder is more sensitive to high temperature. Nevertheless, even at 125˚C the SnAg3.5 minimodules retain their performance significantly better than the SnPb63 minimodules.

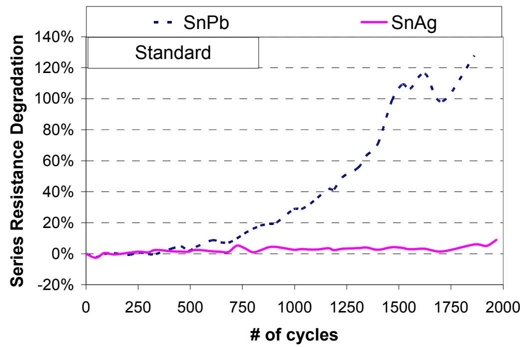


Figure 2.15-6: Standard profile flash test results with interconnect A

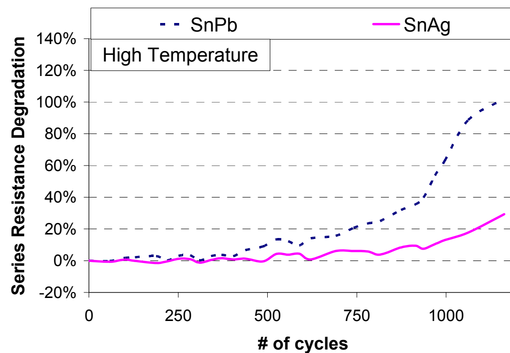


Figure 2.15-7: High temp profile flash test results with interconnect A

Most of the studies explained above rely on accelerated tests to get answers to our questions in a short time. However, testing in actual field conditions is an indispensable complement to these artificial tests. Experience has taught us that three months of field exposure can reveal failure modes that are missed by highly accelerated tests.

Energy production

Theoretical analysis and field measurement showed an energy-production per rated Watt advantage of SunPower modules compared to typical mc-Si modules [3]. The energy production per rated watt (kW-hr/kW) advantage is in addition to the higher output due to higher SunPower efficiency. The kW-hr/kW advantage was found to be ~2-5% (depending on the climate and the comparison module) for 17-18% efficient SunPower modules. In addition, the gain from the use of ARC glass and higher V_{oc} cells should increase the kW-hr/kW advantage by another ~3%.

Arrays at Sandia, New Mexico

Three side-by-side arrays of three different modules are exposed outdoors at Sandia National Lab. One array has modules with no AR glass. Another one has multi-layer AR-coated glass (old AR). The last one has sol-gel single layer AR-coated glass (new AR). Even though the rated reflectance of these two glasses is comparable, the sol-gel coating gave a higher boost in energy production than the multi-stack coating: +3.9% instead of +2.7% (Figure 2.15-8).

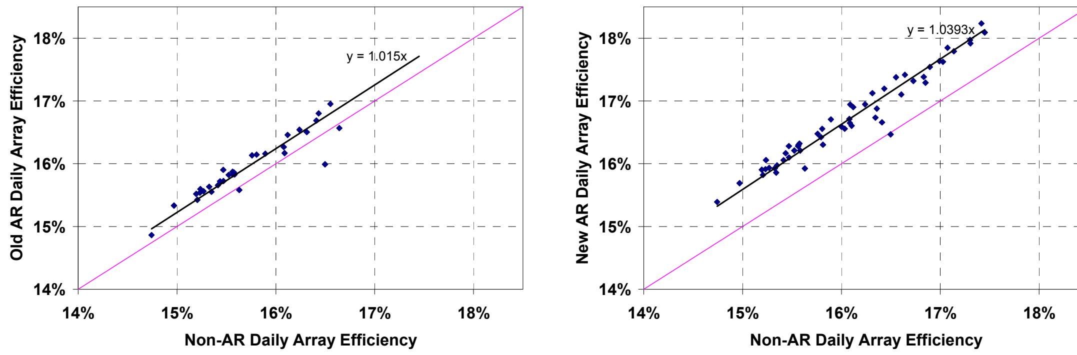


Figure 2.15-8: *Comparison of Non-AR and AR glass performance*

The additional difference between the two types of AR coating is due to a better angular response of the new material compared to the old one (Figure 2.15-9).

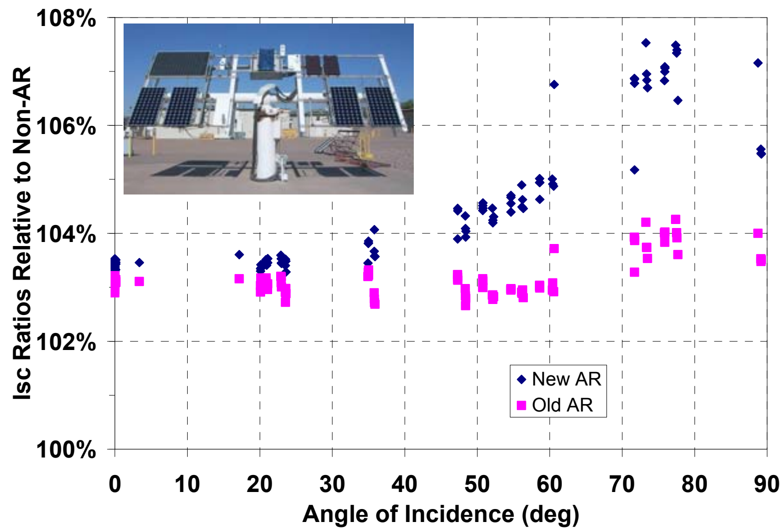


Figure 2.15-9: *Angular response comparison between AR glasses*

Array at NREL, Colorado

This is a five-module array with continuous monitoring of both DC and AC parameters for non-AR and sol-gel AR coated glass. DC data for each month were used to calculate a PTC power for the month by regression. The results to date are summarized in the Table below.

Table 2.15-3: Comparison of monthly PTC at NREL

Data from NREL, calculated monthly PTC regressing ratings

	ARC	NON-AR	
Month	**SP2 DC (W)**	**SP3 DC (W)**	**% AR Gain**
May	1037.9	997.2	**3.92**
June	1043	1001.3	**4.00**
July	1030.3	1011.9	**1.79**

Array in Japan
This is a larger array of 56 modules with monitoring of both DC and AC parameters every minute. This time, the DC data was filtered to discard times when the irradiance was below 850 W/m^2. Figure 2.15-10 shows the results for two consecutive years. In spite of the noise, it is clear that there was no significant degradation over the course of two years.

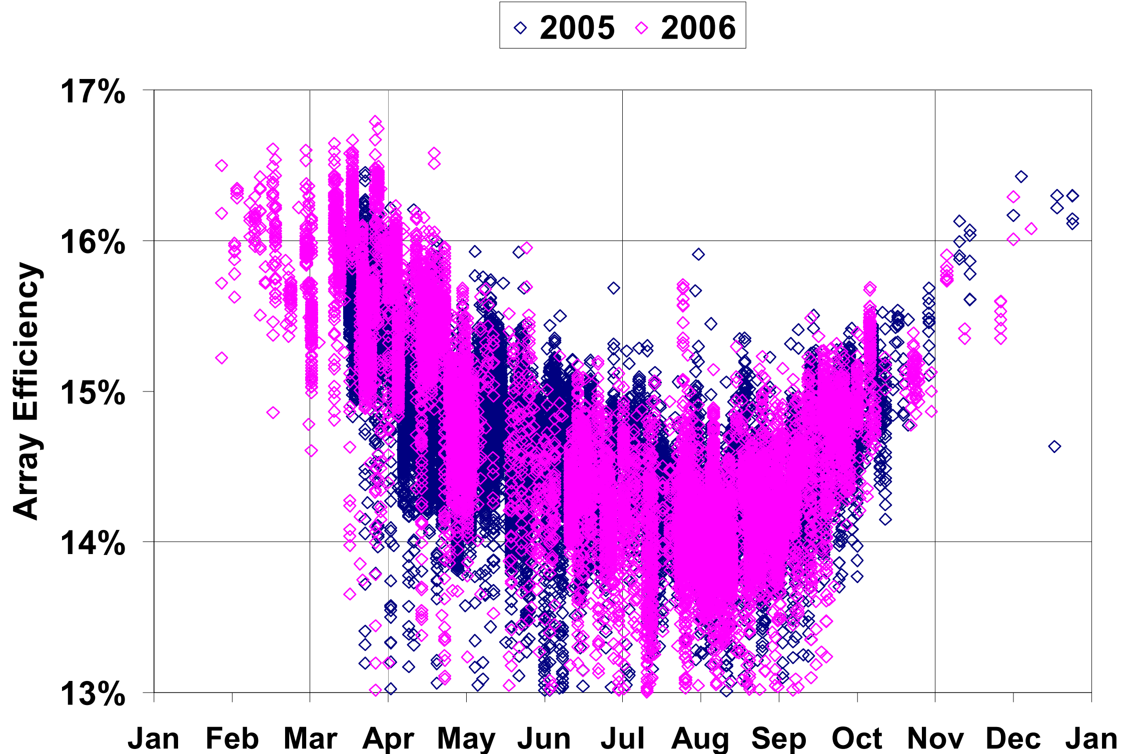


Figure 2.15-10: Instantaneous array efficiency in fair weather conditions for the array in Japan

Summary
Important progress was made both in increasing the life expectance and failure rate of our cells and panels, and in gaining confidence that the quality of our products is consistent with a thirty-year warranty. Models and test methodologies for accelerated tests developed to increase our ability to predict 30 years reliability of our products.

REFERENCES:

[1] www.nrel.gov/docs/fy04osti/33875.pdf

[2] D. Rose, et al., “Mass production of PV modules with 18% total-area efficiency and high energy delivery per peak watt,” *Proceedings of WCPEC-4,* Hawaii (2006).

[3] D. Rose, “Progress toward Automated Manufacture of 19% Efficient Photovoltaic Modules,” *Proceedings of DOE Solar Program Review,* Denver, CO (2005).

[4] M. Stefancich et al., *Solar Energy Materials and Solar Cells pg. 371-377 (2001)*.

[5] A. Hauser, G. Hahn, et al.*, Munich 2001.*

[6] D. Rose and S. Daroczi, “Development and Manufacture of Reliable PV Modules with > 17% Efficiency,” *Proceedings of the 20th European Photovoltaic Solar Energy Conference, Barcelona*, Spain (2005)

[7] Y. Meydbray, et al., EPSEC, Milan, Italy (2007).

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14. ABSTRACT *(Maximum 200 Words):* This report describes SunPower Corporation's final objective of the research effort to develop low-cost, next-generation SunPower modules, with 30-year warranties and at least 50% higher energy production per area relative to today's typical multi-crystalline silicon modules. A SunPower production-ready module was measured by Sandia National Laboratories to have a total-area efficiency of *20.10%*. High efficiency enables higher energy production per area, which results in decreased manufacturing and system-related cost. The new modules are free of hazardous materials and have aesthetic characteristics that facilitate customer adoption. Excellent progress was also made on several module technologies and manufacturing automation.

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