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Silicon detectors at the ILC ☆

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This paper was presented at an event in the celebration of Abe Seiden's 60th birthday. Abe has been a driving force in the development of silicon detectors as well as a major contributor generally to experimental particle physics. We wish him continued success.

Abstract

Silicon detectors are being developed for several applications in ILC detectors. These include vertex detection, tracking, electromagnetic calorimetry, and forward detectors. The advantages of silicon detector technology have been incorporated into a full detector design, SiD (the Silicon Detector). A brief overview of this effort is presented.

1. Physics of the ILC

The International Linear Collider (ILC) will be a powerful tool for exploring Terascale physics. If a Standard Model-like Higgs boson is responsible for electroweak symmetry breaking (EWSB), the mass and width will be measured precisely ($\delta M_H \sim 50$ MeV for $M_H = 120$ GeV), the branching ratios for many channels will be measured with few percent uncertainty, the spin and parity will be checked, and self-coupling will be measured. Should alternative EWSB scenarios be the choice of Nature, the ILC has virtual sensitivity to strong coupling up to several TeV, exceeding the reach of the LHC in some scenarios. The ILC is very strong in its access to the slepton, neutralino, and chargino measurements, if the masses permit. The polarized beam capabilities of the ILC are particularly useful for these measurements. Extra dimensions can be probed. Measurements of the top mass (sub-100 MeV precision), the top Yukawa coupling, and the W mass broaden the ILCs physics impact.

These important physics measurements are empowered by the knowledge of the constrained initial state of the ILC interaction, including the energy and helicity of the interacting leptons. Furthermore, the interactions are simple processes with comparable cross-sections. For example, the Higgsstrahlung process ($e^+ e^- \to Z H$) for $M_H = 120$ GeV at $\sqrt{s} = 500$ Gev, has a cross-section that is roughly half the diquark ($e^+ e^- \to d\bar{d}$) cross-section. With an inclusive trigger and highly polarized beams (80% for electrons, as well as positron polarization), the events are clean and revealing. Detectors should realize powerful flavor tagging, with exquisite vertex detection, and quantitative jet measurements, enabling a precision test of the Higgs boson for Standard Model properties. Discovery of non-Standard Model properties will be possible with precision that goes well beyond the LHC [1].

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2. Detector requirements and advantages of silicon

The detector requirements for the ILC include:

(1) Two-jet mass resolution comparable to the natural widths of W and Z for an unambiguous identification of the final states.
(2) Excellent flavor-tagging efficiency and purity (for both b- and c-quarks, and hopefully also for s-quarks).
(3) Momentum resolution capable of reconstructing the recoil-mass to di-leptons in Higgsstrahlung with resolution better than beam-energy spread.
(4) Hermeticity (both crack-less and coverage to very forward angles) to precisely determine the missing momentum.
(5) Timing resolution capable of separating bunch crossings to suppress overlapping of events; better than 150 crossings, ideally fewer for robustness against backgrounds.

The jet energy resolution requirement is a factor of 2 better than SLC and LEP calorimeters, and even comparable to the ZEUS uranium-plastic scintillator calorimeter. The momentum resolution required for the tracker is a factor of 10 better than LEP experiments and a factor of 3 better than CMS at LHC, and the impact parameter resolution is a factor of 3 better than what SLD achieved. In the ILC nominal beam parameters set, there are five trains of 2820 bunches, separated by 308 ns, every second, setting the timing requirement for bunch number sensitivity.

Silicon detectors will contribute important capabilities in realizing all of these requirements. They inherently suppress backgrounds due to their fast response, yielding single bunch sensitivity. The pileup of hits can be a major issue particularly in the inner layer of the vertex detector, given the long bunch trains planned. The applications of Silicon Detectors will likely include precision vertex detection, with $(20\,\mu\text{m})^3$ or smaller sensitive volumes, fine tracking precision enabled by silicon strip detectors, and high granularity ($\sim 10^8$ cell) "tracking" electromagnetic calorimetry, as well as specialized forward detectors. The Silicon Detector (SiD) ILC detector concept integrates these capabilities into a full-scale experiment.

3. Silicon vertex detectors

Tracking for any modern experiment should be conceived as an integrated system. Following this philosophy, the linear collider detectors aim for a combined, integrated optimization of inner tracking (vertex detection), central tracking, forward tracking, and a highly granular electromagnetic calorimeter. Pixelated vertex detectors are capable of track reconstruction on their own, as was demonstrated by the 307 Mpixel CCD vertex detector of SLD [2] with three barrel coverage. An advanced, pixelated, multi-layer vertex detector is being planned for the linear collider.

The ILC environment offers a unique environment in which to achieve exceptional physics goals due to the modest event rates, relative rates of background to signal, and relatively low radiation levels. Precision measurements of the branching ratios for many of the Higgs decay modes are a primary goal, and superb flavor tagging is needed to achieve this. The goal for the impact parameter resolution is $5\,\mu\text{m} \oplus 10\,\mu\text{m}/(p\sin^{3/2}\theta)$, which will require spacepoint precision of better than 4 μm. The transparency requirement on each layer of the vertex detector is $\sim 0.1\% X_0$. The spacepoint precision of 3.9 μm and transparency of $0.4\% X_0$ that were achieved by SLD encourages this.

Several concepts for vertex detector sensors are under development. The operating environment of the ILC, with bunch trains of about 3000 bunches separated by about 300 ns, is a demanding constraint on the design. The concepts under active development include Charge-Coupled Devices (CCDs), CPCCD (column parallel CCDs), monolithic active pixels based on CMOS technology, DEPFETs (DEpleted P-channel Field Effect Transistor), SoI (Silicon on Insulator), ISIS (Image Sensor with In Situ Storage), and Hybrid Active Pixel Sensors (HAPS).

During the past two years a feasible conceptual design for a monolithic CMOS device that should meet the ILC vertex detector requirements has been developed in collaboration with the Sarnoff Corporation [3] through an R&D contract. In this design each $10\,\mu\text{m} \times 10\,\mu\text{m}$ pixel contains electronics to store the bunch number (time) of up to four hits above an adjustable threshold (thus "Chronopixels"). Hits are read out during the 199 ms between bunch trains. The 10 μm pixels achieve 3–4 μm precision without analog information. The design is shown schematically in Fig. 1.

The highest hit rates and occupancies result from the estimated $0.03\,\text{hits/mm}^2/\text{bunch crossing}$ for the innermost layer, for a bunchtrain pixel occupancy of about 1%. The time information (i.e., bunch crossing number) reduces the occupancy to $<10^{-5}$ per pixel. The functionality of this design has been verified by an hspice simulation.

The analog components of the circuit are estimated to consume most of the power, $\sim 15\,\text{mW/mm}^2$, which can be reduced by turning analog power off between bunch crossings. This reduces the average power consumption to about 0.5 W per chip or about 100 W for the vertex detector, at the margin of an acceptable level. The associated currents will need to be dealt with.

Initial fabrication is planned with 0.18 μm process technology with somewhat larger pixels, eventually moving to 45 nm process technology to achieve ~15 μm pixels.

All of the vertex detector sensor approaches mentioned above either compromise knowledge of the bunch timing or cause concerns for the magnitude of the current required to power all the pixel front ends simultaneously. CCDs passively retain information as to when charge was deposited in the pixel (if the image clock speed is at least equal to the bunch frequency). A possible approach recently under consideration is to extract that information

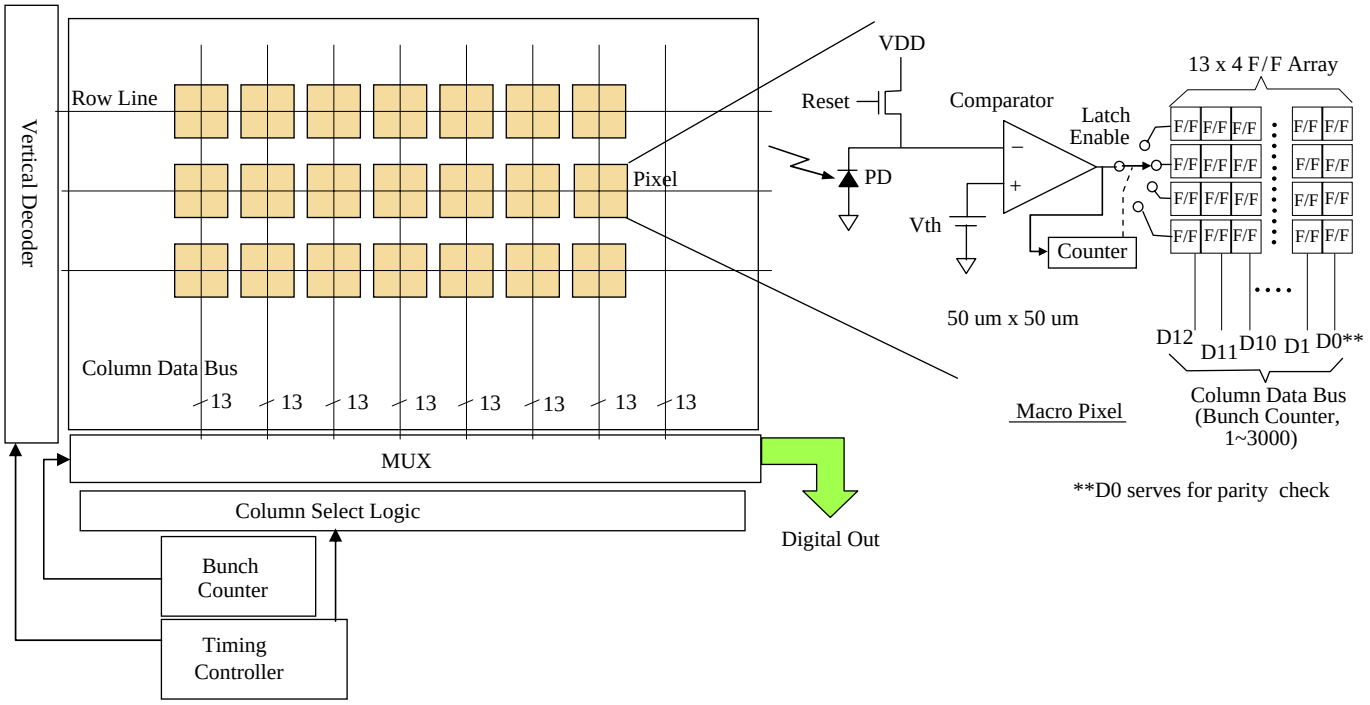

Fig. 1. Chronopixel array architecture.

almost unambiguously with quite modest image clock speed is the Short Column Charge Coupled Device (SCCCD). The SCCCD is a two layer device, having a CCD layer and a CMOS readout layer bump bonded together. The CCD layer consists of only columns, perhaps 512 pixels long, that terminate with a readout node and bond pad. There is no row structure. The CCD is arranged so that adjacent rows clock in opposite directions, and that charge is likely to be shared in pixels of adjacent rows. The CCD might be clocked at 3 clocks per bunch crossing ($\sim$10 MHz) during the train. The column length and clock frequency are selected so that the occupancy of a short column of about 500 rows on the inner layer ($r = 1.2$ cm) is estimated to be <1. The readout layer would discriminate pixels with charge above a threshold, and record the amplitude and clock time of those pixels in a multiple buffer scheme. (This architecture is similar to that being developed for the Si–W calorimeter described here). It is expected that the readout layer could be fabricated from 0.25 μm CMOS. Matching the pixel hits in adjacent rows should yield unique positions and bunch times, while avoiding very fast image clocks and large front end current, and utilizing approximately current technology. Further development of this device is being considered. It addresses the issues of bunch timing retention with limited current flow.

4. Silicon calorimetry

To complement LHC capabilities, ILC detectors must reconstruct hadronic final states, including reasonable separability of $W \to$ jets from $Z \to$ jets. An attractive solution for the electromagnetic calorimetry is based on the silicon–tungsten (Si–W) approach [4]. With high density and segmentation, Si–W plays a critical role in the physics goal to realize jet energy resolution of $\approx 30\%/\sqrt{E_{\text{jet}}}$. The few mm segmentation possible with a Si-W ECal provides outstanding reconstruction and isolation of individual photons, with good electromagnetic energy resolution of $\approx 15\%/\sqrt{E}$. Also, excellent lepton reconstruction results from this "imaging" calorimeter, crucial for many new physics signatures.

An outstanding technical issue is integration of silicon detectors, containing about 50 million pixels, with readout electronics, and the associated integrated power. The need for sensitivity to muon tracks and the full pulse height of electromagnetic showers leads to a dynamic range requirement of 2×10^4. The solution described here naturally allows high transverse segmentation (currently 3.5 mm) and a small readout gap (currently 1 mm), while maintaining a small Moliere radius. Thirty longitudinal sampling layers are planned, 20 of thickness $\frac{5}{7}X_0$, followed by 10 of $\frac{10}{7}X_0$. The readout gap is illustrated in Fig. 2.

Important progress has been achieved during the past year. The most significant development has been the completion of the design of the readout chip (KPiX) and the fabrication and testing of the first three rounds of prototype chips. The power budget is limited by power pulsing, and the dynamic range requirement is achieved by dynamic switching of amplifier gain ranges. A recent discussion of the KPiX functionality can be found in Ref. [5].

Progress in characterizing prototype silicon detectors and preparing for the integration has also been made.

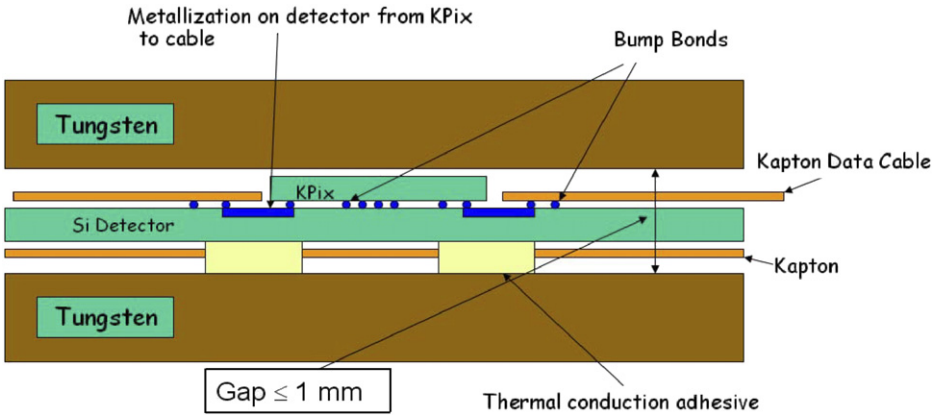

Fig. 2. Schematic of the readout gap. With power cycling of the readout chip, the heat load of the KPiX readout chip can be handled by passive conduction through the tungsten.

Measurements on 6 in. Hamamatsu prototypes emphasize parameters relevant to the use of the sensors with the electronics design. The most important measurements in this regard are stray capacitance and leakage current. An absolute calibration with a radioactive source has also been investigated.

In most cases the noise of a pixel charge measurement is directly proportional to the total capacitance input to the amplifier, dominated by the stray capacitance of traces connecting pixels to the bump-bonding array. Hamamatsu detectors with oxide metal layers about 0.9 μm thick and 6 μm thick traces give a theoretical capacitance of approximately 3.1 pF/cm. The total stray capacitance of a given pixel has two comparable contributions, one from the capacitance of the traces connecting the pixel to the bump-bonding array, and a second due to traces from other pixels which cross the given pixel.

A small fraction of the pixels have a very large number of crossing traces, resulting in capacitances of somewhat more than 100 pF. The larger stray capacitances will be reduced in a future version of the sensors by narrowing the traces in the vicinity of the bump-bonding array.

Another important property of the detectors is trace series resistance (R_s), with a noise contribution (for a given bandwidth) proportional to $C_{tot}\sqrt{R_s}$, where C_{tot} is the total input capacitance. It is desirable to keep this noise term comparable to the input FET noise, or $R_s \sim 300\,\Omega$. The measured trace resistance is $57 \pm 2\,\Omega$/cm. For the longest traces (~10 cm) the measured value implies a maximum resistance of ~600 Ω. Leakage current measurements indicate the noise contribution to be minimal, ~250 electrons.

Silicon calorimeters are quite stable. Since the largest change in response is due to the electronics, it is designed with an internal calibration system, accurate within a chip to ~1%. Chip-to-chip variations could be larger. Each sensor might be calibrated, after the readout chip has been bump bonded, with 60 keV photons from ^{24}Am. Measurements indicate it should be possible to calibrate each pixel to 1%.

The cross talk by capacitive couplings between the channels has been found to be at or below the 1% level. The cross talk dependence on capacitive coupling and readout electronics is under investigation.

5. The Silicon Detector

SiD has been conceived as a state-of-the-art detector to meet all the ILC physics requirements with built-in robustness against machine-induced backgrounds [6]. Starting with the all important calorimetry performance, particle flow calorimetry is needed, with the coil located outside the calorimeter. Fine granularity is required for the particle flow calorimetry, leading naturally to the choice of the finely grained silicon–tungsten electromagnetic calorimeter. Since this calorimeter is expensive, the detector architecture calls for a compact geometry. Tracking precision can be achieved in this model by a large magnetic field and high spacepoint precision silicon tracking. A benefit of the large magnetic field is the tighter envelope of the beamstrahlung pairs, leading to a possibility of a smaller beampipe with very close vertexing. SiD consists of cylindrical geometry (barrel and end caps) vertex detectors, silicon strips trackers [7], silicon–tungsten electromagnetic calorimetry, and a hadronic calorimeter—all inside the 5 T solenoid—and followed by a flux return with additional muon identification. Disk detectors in both the vertex detector and the tracker will be deployed to provide good tracking coverage down to 140 mrad, and forward calorimeters will extend detector below 140 mrad to measure the luminosity normalization with Bhabha pairs, to measure the instanteous luminosity with beam-strahlung pairs and gammas, and to extend the calorimetry hemeticity. Silicon technology is integral to achieving the requirements. SiD is fast, robust against machine-induced background, fine in segmentation and, by now, a mature concept.

6. Conclusion

The ILC will be a powerful tool for exploring Terascale physics. Silicon detectors are being developed with good

progress for several applications in ILC detectors, including vertex detection, tracking, electromagnetic calorimetry, and forward detectors. The advantages of silicon detector technology have been incorporated into the SiD (Silicon Detector) full detector design.

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