REAL TIME RF SIMULATOR (RTS) AND CONTROL*

G. Cancelo[#], C. Armiento, K. Treptow, A. Vignoni, T. Zmuda, FNAL, Batavia, IL 60510, U.S.A.

Abstract

The multi-cavity RTS allows LLRF algorithm development and lab testing prior to commissioning with real cavities and cryomodules. The RTS is a valuable tool since it models the functions, errors and disturbances of real RF systems. The advantage of a RTS over an off-line simulator is that it can be implemented on the actual LLRF hardware, on the same FPGA and processor, and run at the same speed of the LLRF control loop.

Additionally the RTS can be shared by collaborators who do not have access to RF systems or when the systems are not available to LLRF engineers. The RTS simulator incorporates hardware, firmware and software errors and limitations of a real implementation, which would be hard to identify and time consuming to model in off-line simulations.

RTS ARCHITECTURE

The RTS simulates the amplitude and phase dynamics of the RF carrier in the RF system. It does not simulate the RF behavior of RF components such as up and down converters, klystron, waveguides and cavities. However, since the LLRF control is performed over the RF envelope, most errors and disturbances are incorporated. As shown in Figure 1 the multi-cavity simulator and the LLRF control are connected in a loop. The RTS can be operated in any combination of feedforward (FF) and feedback (FB) modes.

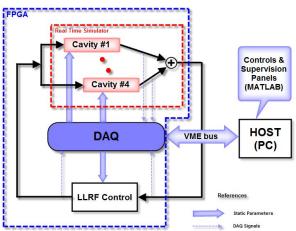


Figure 1: RTS and LLRF Control basic scheme.

The RTS and the LLRF control interface to a host computer via a real-time DAQ. The computer server hosts the control software and applications so as perform the RTS and LLRF control initialization, acquire statistics

and perform data analysis. The DAQ acquires data during the simulation/control pulse. The data is locally stored into a memory which is readout by the Control server in between RF pulses.

RTS MODELS

Cavity Models

The RTS models some of the electrical and mechanical fundamental cavity modes. The electrical model is a $1^{\rm st}$ order approximation of the cavity's Π mode in the complex plane (1) [1,3]. The mechanical mode, models the Lorentz force detuning [3]. The total detuning from the mechanical model is the linear sum of three mechanical resonances (2). The differential equations for such behaviours are:

$$\begin{bmatrix} \dot{V}_r(t) \\ \dot{V}_i(t) \end{bmatrix} = \begin{bmatrix} -\omega_{1/2} & -\Delta\omega(t) \\ \Delta\omega(t) & -\omega_{1/2} \end{bmatrix} \begin{bmatrix} V_r(t) \\ V_i(t) \end{bmatrix} + \begin{bmatrix} \omega_{1/2}R_L \\ \omega_{1/2}R_L \end{bmatrix} \begin{bmatrix} I_r(t) \\ I_i(t) \end{bmatrix} \quad (1)$$

$$\begin{split} \frac{d^2(\Delta\omega_m)}{dt^2} + \frac{\omega_m}{Q_m} \frac{d(\Delta\omega_m)}{dt} + \left(\omega_m\right)^2 \Delta\omega_m &= \left(\omega_m\right)^2 2\pi K_m V^2(t) \\ \Delta\omega_m &= \sum_{m=1}^3 \Delta\omega_m \qquad m = 1, 2, 3 \end{split} \tag{2}$$

The electrical and mechanical cavity models combined behave as a linear time variant system. The detuning coefficient in the electrical model's transition matrix is a function of the mechanical model's dynamics, which has the cavity gradient as an input. The RTS can also simulate the cavity's $8/9\Pi$ mode whose response is added to the Π mode response.

BEAM LOADING

The beam loading is implemented by a table, which is preloaded by the Control server before run time. Each cavity has its own table allowing individual cavity beam loading conditions. This feature is particularly important when the RTS simulates a beam traveling at non relativistic velocities, with β changing at each cavity or when the synchronous phase between the cavity and the beam changes along the simulated cavities.

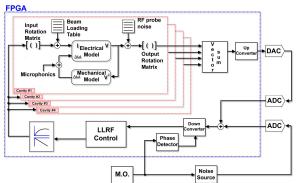


Figure 2: Real Time Simulator.

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#cancelo@fnal.gov

KLYSTRON AND RF COUPLERS

Klystron characteristics have a nonlinear behavior in amplitude and phase as a function of the input drive. The RTS models the klystron's nonlinear behavior with amplitude and phase tables. Since a typical klystron bandwidth is on the order of 5 MHz, at least an order of magnitude faster than the cavity closed loop bandwidth, its dynamic behavior has not been modeled.

The distribution of RF power into each cavity is a function of the waveguide tuners and RF couplers. The RTS simulates those functions with a 2x2 input matrix per cavity. The input matrices set the amplitude and phase of each cavity. The numbers in the input matrices represent a fixed RF configuration, and are usually kept constant during an individual run.

OUTPUT MATRICES AND TABLES

The RTS also implements a matrix and a table at the output of each cavity. These matrices and tables are used to introduce noise, disturbances and misalignments of the RF output system such as RF cavity probes, down converters, cables, LO jitter, etc.

RF pickup probe

Cavity gradient levels are measured by RF probes whose transfer function gains exhibit notable dispersion from probe to probe.

The output matrices can also account for random static errors in gains, phase rotations and reflections in attenuators and down-converters. These errors along with simulated microphonics can be used to test vector sum calibration algorithms.

CAVITY FIELD VECTOR SUM AND DIGITAL UP CONVERTER

The Vector Sum adds the field of each cavity. Then, is up converted in frequency to an intermediate frequency (IF). The IF, currently set to 13 MHz, is tuned from a Control panel. Different IF values can be used to determine an optimum one in terms of ADC, DAC and filter noise.

ADC AND DAC NOISE

The system formed by the multi-cavity simulator and LLRF control can be entirely implemented inside of an FPGA. Alternatively, the simulator's output, after the up converter (Figure 2), is sent to a DAC and looped back into an ADC. The loopback add the DAC and ADC noises and limitations into the RTS and LLRF control loop.

The RTS also features a noise input connected to an ADC channel. This input can be used to simulate external disturbances, correlated and uncorrelated noise, such as high harmonic content from the down converter which is aliased back into the control bandwidth.

HARDWARE IMPLEMENTATION

The RTS core has been implemented in a Xilinx Virtex4 FPGA (XC4VLX80) using the tools provided by Simulink/Matlab/System Generator and the Xilinx ISE compiler. The RTS can be easily compiled for other Xilinx FPGAs. An Altera based implementation would require more work, although now similar interfaces to Simulink/Matlab do exist. The current version of the RTS runs on the VME based ESECON LLRF controller [2]. The ESECON (Figure 3) is connected to a VME processor running the Control server and applications (Figure 1).

DAQ AND COMMUNICATION

At runtime the DAQ saves the status of simulator and control variables on the ESECON local RAM. The data is retrieved by the host processor between RF pulses and displayed using the Control and RTS simulator panel applications. The Control and Simulator panels are also used to initialize the hardware, and firmware. The parameters of the RTS cavity models and other variables can be manually set using the panels or loaded from a CSV type file.



Figure 3: ESECON Board.

RTS AND LLRF CONTROL EXAMPLE

In order to illustrate the RTS with an example we have configured 4 cavities using the values in Table I [5]. Notice that the cavities are configured with different synchronous phases and beam loadings. Each synchronous phase will determine the values of the cavity input rotation matrix, each beam loading condition will translate into a different beam loading table per cavity (Figure 2).

The Feed Forward (FF) and PID controls are set to the Control Panel values as shown in Figure 6. The ESECON Control Panel is used to initialize the ESECON board, set the FF and PID controller values, set the IF reference channel, etc. The Control Panel also allows opening the cavity parameters panel editor and displaying individual cavity responses as shown in Figure 4.

Table 1: Set cavities parameters.

Cav Nº	Amplitude	Phase	TTF	N_coupler	Beta	Rl	Ql	w12	delta_fo	Ig	theta
182	23.22	-20	0.7358	5471.6	3473.8	1.50E+09	2.87E+06	225.8	-186	14.8678	-35.54
188	24.66	-19	0.7762	5438.92	3515.67	1.48E+09	2.84E+06	228.52	-176	15.8279	-33.72
195	26.82	-18	0.8156	5244.08	3781.76	1.38E+09	2.64E+06	245.81	-165	17.6222	-31.69
201	26.1	-17	0.844	5637.16	3272.75	1.59E+09	3.05E+06	212.73	-159	16.3261	-30.41

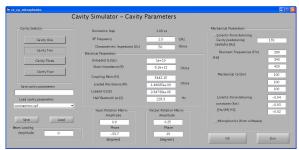


Figure 4: Cavity Parameters panel.

Figure 5 shows the amplitudes and phases of 4 simulated cavities when only FF control is applied. During this simulation the Lorentz force detuning has been turned off. Figure 7 shows real time oscilloscope traces of the simulator's vectorsum in IF domain (yellow) along with the I (purple) and Q (green) components using the DAC output.

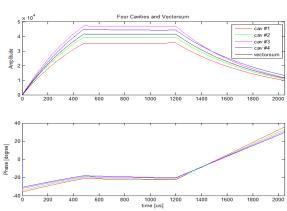


Figure 5: Individual response of the four cavities

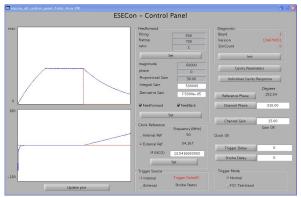


Figure 6: ESECON control panel showing vectorsum in amplitude and phase in closed loop.

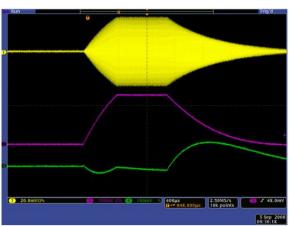
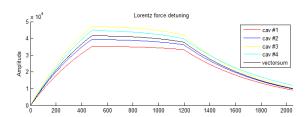


Figure 7: Scope plot of Vectorsum (I and Q) and IF signal (yellow).

Real Time Simulation and control including Lorentz force detuning

Figures 8 and 9 show the Lorentz force detuning effect on the amplitudes and phases of the simulated cavities and vectorsum respectively. The detuning steers the amplitudes and phases away from their goals and flattops. Figure 9 shows the mixed I and Q effects caused by the increased detuning $(\Delta\omega)$ due to the Lorentz force.



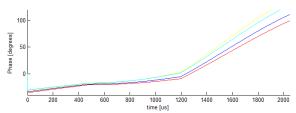


Figure 8: Individual response of each cavity with Lorentz force detuning.

Figure 10 shows the amplitudes and phases of the simulated cavities when the PID feedback control is applied. The controller has been set with the parameters shown on Figure 6. The PID compensates for the Lorentz

force detuning restoring the flattops and bringing the amplitudes and phases close to their goals.

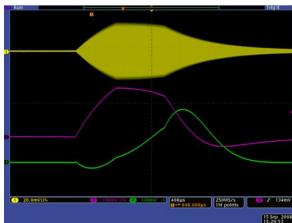


Figure 9: Vectorsum and IF signal for the Lorentz force detuned cavities

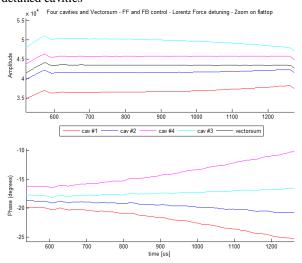


Figure 10: Close loop (PID) with Lorentz force detuning response.

CONCLUSION

The multi cavity RTS is still a work in progress but it has matured enough to be an interesting tool to help in the development and testing of LLRF algorithms. The RTS can also help understanding some of the noise components in the control loop and suggest mitigation techniques.

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