Towards quantum information processing with impurity spins in silicon

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The finding of algorithms for factoring and data base search that promise substantially increased computational power, as well as the expectation for efficient simulation of quantum systems have spawned an intense interest in the realization of quantum information processors [1]. Solid state implementations of quantum computers scaled to >1000 quantum bits ("qubits") promise to revolutionize information technology, but requirements with regard to sources of decoherence in solid state environments are sobering. Here, we briefly review basic approaches to impurity spin based qubits and present progress in our effort to form prototype qubit test structures.

Since Kane's bold silicon based spin qubit proposal was first published in 1998 [2], several groups have taken up the challenge of fabricating elementary building blocks [3-5], and several exciting variations of single donor qubit schemes have emerged [6]. Single donor atoms, e. g. ^{31}P, are "natural quantum dots" in a silicon matrix, and the spins of electrons and nuclei of individual donor atoms are attractive two level systems for encoding of quantum information. The coupling to the solid state environment is weak, so that decoherence times are long (hours for nuclear spins, and ~60 ms for electron spins of isolated P atoms in silicon [7]), while control over individual spins for one qubit operations becomes possible when individual qubits are aligned to electrodes that allow shifting of electron spin resonances in global magnetic fields by application of control voltages. Two qubit operations require an interaction that couples, and entangles qubits. The exchange interaction, J, is a prime candidate for mediation of two qubit operations, since it can be turned on and off by variation of the wave function overlap between neighboring qubits, and coherent manipulation of quantum information with the exchange interaction alone has been shown to be universal [8]. However, detailed band structure calculations and theoretical analysis of J coupling between electrons bound to phosphorus atoms at low temperatures in silicon revealed strong oscillations of the coupling strength as a function of donor spacing on a sub-nm length scale [9]. These oscillations translate into scattering of interaction strength for ensembles of qubit spacings which in turn poses a serious obstacle to scalability [10]. Two alternatives to J coupling are dipolar coupling [11] and spin coherent shuttling of electrons between donor sites [12].

Readout of single electron spins poses another critical challenge [13, 14], and inferring spin orientations from charge measurements in spin dependent charge transfer reactions seems to be viable route to single shot single spin readout. This readout can be accomplished with single electron transistors, which are used as sensitive electrometers [15].

Impurity spin based qubit schemes in silicon have to overcome a significant nanofabrication challenge so that a test bed regime can be entered where fundamental properties and rudimentary operations can be investigated.

In order to form such test devices, three key components have to be integrated.

1) an array of single dopant atoms has to be formed were
2) single dopant atoms are aligned to control gates and
3) single dopant atoms are also aligned to a readout device

Scanning tunneling microscope based hydrogen lithography [3, 4] and single ion implantation are two methods for formation of single atom arrays [4, 5]. The former has the advantage of near atomic resolution, but requires atomically flat and clean surfaces, and well tuned surface chemistry, while the latter is rather universal in ion species, but is limited by range straggling to a placement resolution of at least several nanometers. Width and pitch of control gates are very sensitive to the envisioned two qubit operation scheme. Direct exchange coupling requires a qubit spacing of ~20 nm with a gate pitch of about 7 nm, while electron shuttling would allow qubit spacings of ~100 nm. Alignment of gates, SETs and single donors

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represents the task for the formation of single atom devices.

Figure 1 shows the concept for our single ion implantation system with scanning probe alignment for single atom placement [5, 16]. The piezoresistive Scanning Force Microscope [17] images the device region to be implanted in a high vacuum chamber. Following imaging, sites for implantation are selected, and ions are allowed to reach the probe tip. The probe tip is

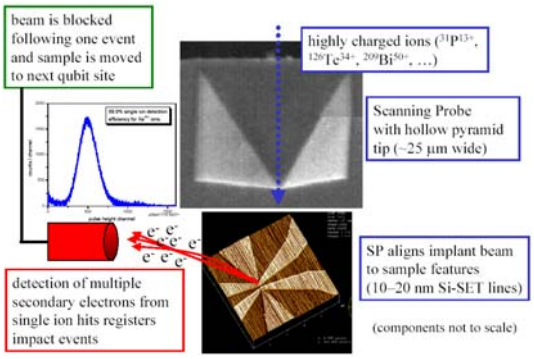

Figure 2: Schematic of the setup for single ion implantation setup with scanning probe alignment.

pierced with a hole (diameter ~5-10 nm) [18], allowing it to transmit ions at a rate of a few Hz. Secondary electron bursts from the impact of individual highly charged dopant ions (e. g., $^{31}P^{13+}$) are detected in a scintillator coupled to a photo multiplier tube. Pulse heights from detection of multiple electrons from one highly charged ion impact are well separated from single electron background events. Secondary electrons are guided to the detector with electrical and magnetic fields, so that the probe tip can be held in close proximity (<1 µm) to the sample. Following each ion impact, the beam is blanked within a few µs, and the process of imaging and alignment is repeated. To date, we have achieved single ion detection efficiencies >85% for highly charged dopant ions with implant energies of ~10 keV, and implantation of readout structures is in progress.

Pairs of SETs in silicon on insulator (SOI) have been formed by Electron Beam lithography and we achieved silicon wire widths of ~10 to 20 nm. An example is shown in Figure 2, with an I-V curve showing Coulomb blockade at 4.2 K in Figure 3. Coulomb blockade has been observed in silicon nanostructures for many years. In our SETs the silicon island region was undoped and we did not apply stress limited oxidation to further shrink the silicon wire width. Typical charging energies in devices with ~15 nm wide wires were about 8 to 10 meV. Electron spin coherence times for P doped Si are ~60 ms at 7°K [7], and single spin device physics thus becomes accessible at LHe temperature for silicon SETs with charging energies $E_c=e^2/2C>3.4$ meV$=10\ k_BT$ (with C, junction capacitance, T, temperature and k_B, Boltzmann constant).

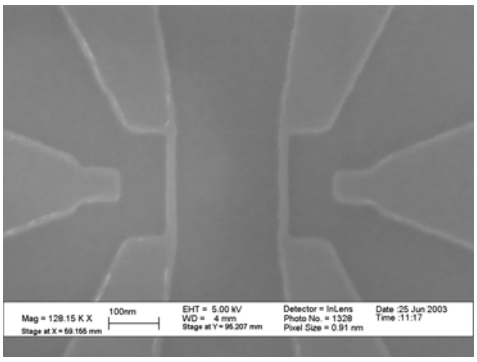

Figure 2: SEM image of a Si-SET pair in SOI

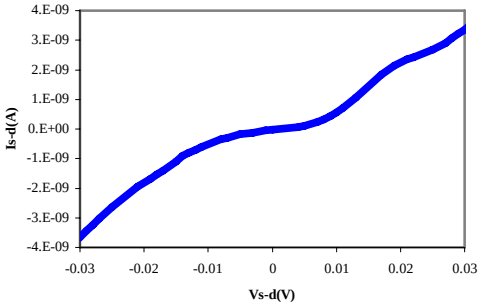

Figure 3: I-V curve of source-drain current as a function of source drain voltage for a silicon SET with 14 nm wire width showing Coulomb blockade.

SOI yields the fastest path for silicon based SET formation, but the quality of the SiO_2/Si interfaces poses two crucial challenges. One is the presence of traps and defects. The CMOS standard for defect density is ~10^{10} cm^{-2} V^{-1} for a gate oxide, and an order of magnitude higher for the device layer to box interface. This translates into 1 to 10 defects per SOI SET. The second issue is segregation of P dopants to the SiO_2/Si interface during the thermal annealing step that is needed to achieve full electrical activation of implanted dopants. In a process related to oxidation enhanced diffusion, interstitials are injected into the silicon during annealing, and

these interstitials aid the segregation of the dopants to the interface. The P atoms are then bound at the interface and are not electrically active [19]. Not only has the dopant array dissolved, the dopants are also bound such that their electrons do no longer exhibit the quasi hydrogenic wave function that makes them so attractive for quantum information processing. In Figure 4 we illustrate this effect with Spreading Resistance Analysis depth profiles of the carrier concentration for a 60 keV, 10^{11} cm^{-2} P implant into silicon with SiO_2 (dashed) vs. Si_3N_4 (solid) barrier layers. The electrical activation fraction was 80% for both wafers, but nitride injects vacancies, retarding P segregation, while the oxide enhances segregation to the interface.

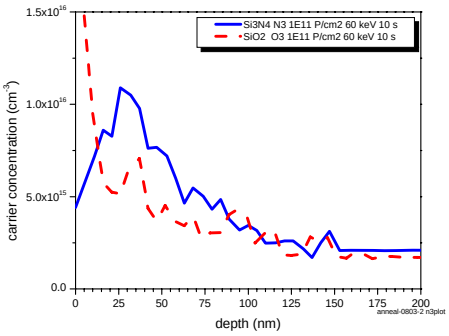

Figure 4: Carrier concentration as a function of depth from SRA for a 10^{11} cm^{-2}, 60 keV P implant in silicon for SiO_2 and Si_3N_4 layers.

An alternative to the use of any dielectric layer is the formation of control gates and SETs from metal silicides. The silicon matrix is undoped and insulating at low temperatures, while the Schottky barrier to PtSi (0.87 eV) provides carrier confinement. SETs can be formed from PtSi lines patterned to constricted conductors, and gate modulation of source drain current is expected without tunnel junctions [20]. Integration with epitaxial silicides (such as PtSi on Si(111)) would also allow a possible path to three dimensional quantum circuit integration [21].

In our presentation we will report on the status of our single atom device integration effort and discuss paths to proof of principle experiments for tests of quantum information processing proposals with impurity spins in silicon.

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Acknowledgments We thank R. de Sousa, J. Tucker, T. C. Shen, and E. Weber for stimulating discussions and the staff of the UC Berkeley Microlab, and the National Center for Electron Microscopy for their support. This work was supported by NSA and ARDA under ARO contract number MOD707501, and by the U. S. DOE under contract No. DE-AC03-76SF00098.