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ILC Vertex Tracker R&D

LBNL and UC Berkeley
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1 Introduction

This document summarises past achievements, current activities and future goals of the R&D program aimed at the design, prototyping and characterisation of a full detector module, equipped with monolithic pixel sensors, matching the requirements for the Vertex Tracker at the ILC. We provide a plan of acivities to obtain a demonstrator multi-layered vertex tracker equipped with sensors matching the ILC requirements and realistic light-weight ladders in FY11, under the assumption that ILC detector proto-collabrations will be choosing technologies and designs for the Vertex Tracker by that time.

The R&D program discussed here started at LBNL in 2004, supported by a Laboratory Directed R&D (LDRD) grant and by funding allocated from the core budget of the LBNL Physics Division and from the Department of Physics at UC Berkeley. Subsequently additional funding has been awarded under the NSF-DOE LCRD program and also personnel have become available through collaborative research with other groups.

The aim of the R&D program carried out by our collaboration is to provide a well-integrated, inclusive research effort starting from physics requirements for the ILC Vertex Tracker and addressing Si sensor design and characterisation, engineered ladder design, module system issues, tracking and vertex performances and beam test validation. The broad scope of this program is made possible by important synergies with existing know-how and concurrent programs both at LBNL and at the other collaborating institutions. In particular, significant overlaps with LHC detector design, SLHC R&D as well as prototyping for the STAR upgrade have been exploited to optimise the cost per deliverable of our program. This activity is carried out as a collaborative effort together with Accelerator and Fusion Research, the Engineering and the Nuclear Science Divisions at LBNL, INFN and the Department of Physics in Padova, Italy, INFN and the Department of Physics in Torino, Italy and the Department of Physics of Purdue University.

2 Overview

2.1 Benchmarking and Physics Tools for Optimisation

The definition of physics benchmarks sensitive to the details of the Vertex Tracker design and response, their study with realistic full simulation and reconstruction packages and the development of software tools for the reconstruction of the relevant physics objects are key components of the process of performance assessment and optimisation. While

much has been learned from the experience with physics at LEP and SLC, simulation for the LHC and physics studies for TESLA, NLC, JLC, CLIC and now the ILC, much work still needs to be done. We need to study physics channels as well as sets of particles which probe the details of detector specific performances. We need to study processes, which are important physics-wise, so we can evaluate the ILC sensitivity vs. the key Vertex Tracker parameters. This program is not a task for one or few groups. A world-wide, organised effort, which adopts a coherent set of benchmark processes and uses compatible simulation and reconstruction software and parameters is required. The ALCPG07 workshop offers a forum for continuing this process.

In 2005 a benchmark panel was convened by the WWS with the charge to "aid the process of optimisation of the detector concepts by providing a minimum set of physics modes that cover capabilities of a detector such as tracking, jet reconstruction etc. such that each concept studies can use these modes to evaluate and optimize given detector designs". In Spring 2006, a report, detailing a set of physics benchmarks central to the anticipated ILC physics program, with well-defined target goals for measurement accuracy and manifest effect of the performance of the individual detector components, was released [1]. Benchmarking the Vertex Tracker was explicitely discussed and the proposed list of benchmark reactions included several processes relevant to a detailed study of the Vertex Tracker performance. Beyond the well-known Higgs branching fraction measurement, the attention was drawn on other, complementary processes such as the determination of A_{FB} in $e^+e^- \to b\bar{b}$, $c\bar{c}$ at the highest energy, which requires not only jet flavour tagging but also vertex charge determination, $e^+e^- \to H^0A^0 \to b\bar{b}b\bar{b}$, $\tau^+\tau^-b\bar{b}$ in a dark matter-motivated MSSM scenario, requiring highly efficient b and τ tagging and $e^+e^- \to \tilde{\tau}_1\tilde{\tau}_1 \to \tau^+\tau^-\tilde{\chi}^0_1\chi^0_1$ again in the MSSM, where τ identification against both jets and light leptons is crucial.

Our group has promoted the study of benchmark reactions and has been pioneering the study of physics processes relevant to the optimisation of the Vertex Tracker. Recently much effort has been invested in the development of dedicated processors in the `Marlin` C++ reconstruction framework. These processors can be used for the analysis of particle tracks in simulated physics processes and real data from beam test alike. This offers an important opportunity to validate our simulation and to adopt the sensor response measured for real detector prototypes in the analysis of these benchmark processes.

2.2 Monolithic Silicon Pixel Sensor *R&D*

2.2.1 Overview of *R&D* directions

Physics requirements push the vertex tracker sensor specifications to new levels. In nearly two decades of R&D on Si detectors for the LHC experiments much has been learned. Now, the ILC requirements motivate new and complementary directions for the detector development. The key features steering the activities and ultimately defining the figures of merit against which a choice of the technology will be performed, may be outlined as follows:

- single point resolution of $\approx 2-3\ \mu m$, at least for the innermost layer;
- single layer thickness of $\approx 0.1\%\ X_0$, again with emphasis on the innermost layer;
- design compliant with a sensor occupancy at the 2-3% level;
- radiation tolerance to neutron fluxes at the level of few times $10^9/cm^2/year$ and electron fluxes of about $5 \times 10^{12}/cm^2/year$;
- Electro-magnetic interference compliance;
- availability and stability of the technology over the timescale of the development and production.

The required spatial resolution sets a tight limit to the pixel detector granularity and the signal-over-noise performance. We have used beam test data and detailed `Geant-4`-based simulation and a custom digitisation package implemented in `Marlin` to study the interplay of pixel size, S/N and single point resolution. A pixel on a 20 μm pitch, which provides a point resolution of 3.2 μm with a S/N ratio of 16, as measured by our group, gives 2.4 μm at S/N=23 and 1.9 μm at S/N=45. These figures set an upper limit on the pixel pitch of $\simeq 20\ \mu m$ for the innermost layer and a S/N in excess of 10, in case analog readout and charge center-of-gravity reconstruction is performed. If the pixel readout is binary a pixel size of $\leq 10{\times}10\ \mu\mathrm{m}^2$ is required, as well as a mean of limit the charge dispersion.

The cell size by itself constrains the possibility to embed advanced functionalities on pixel. Moreover, other limitations may be due to specific sensor technologies and ultimately define the sensor architecture. The required material budget excludes hybrid pixels, where the front-end electronics is integrated on a separate application specific integrated circuit with a matrix of cells mating the sensor and typically interconnected

by bump-bonding, as adopted for the LHC detectors. The architecture and the related power dissipation do have an impact as well on the material budget. Low power designs, both in terms of single cell and peripheral electronics and the possibility to exploit the ILC low duty cycle, reducing the bias during the 199 ms elapsing in between two bunch trains, could result into a detector not requiring a sophisticated active cooling system. This would reduce the material on the ladder support and end-caps and simplify the detector integration and its robustness. Occupancy at the few percent level is definitely a concern, in order to guarantee the required pattern recognition efficiency and purity. The ongoing R&D activites are essentially pursuing two different strategies based either on a fast readout during the train or on a high frequency sampling (in space or time) of the information, storage and subsequent readout in between bunch trains. Our R&D activity is addressing both options: CMOS pixels with fast readout and in-chip digitisation for the first architecture and SOI pixels with time stamping and binary output for the second. Radiation levels are low by LHC standards; nevertheless, a full assessment needs to be constantly performed as the fabrication technology and the design evolve. Moreover, tolerance to ionizing radiation is an issue which should not be neglected.

2.2.2 CMOS pixels with fast readout and in-chip digitisation

A promising architecture for a monolithic sensor has small pixels, readout at high speed during the long ILC bunch train. Signals are digitised at the end of the columns with enough accuracy to allow charge center-of-gravity interpolation to optimise the spatial resolution. Digitising at the required speed (25-50 MHz) and within the maximum tolerable power dissipation ($\simeq$ 0.4 mW/column) poses major design challenges. A detailed study of data collected with a CMOS pixel test chip designed by our group (LDRD-1) [2], with 10×10 μm^2, 20×20 μm^2 and 40×40 μm^2 pixels (see Figure 1) shows that 5-bit ADC accuracy with 20×20 μm^2 pixels is sufficient, provided the pixel pedestal is removed before digitisation (see Figure 2.2.2). This can be achieved by performing correlated double sampling (CDS) in-pixel. A chip with 20×20 μm^2 pixels and in-pixel CDS (LDRD-2) was designed and successfully tested. CDS is performed by storing the reference level on an in-pixel capacitor, the signal level is then stored on a second capacitor and the pedestal can be subtracted before digitisation [3]. The chip has been successfully tested in the lab and in beam tests at readout frequencies up to 25 MHz [4].

The required readout speed is determined by the level of pair background. Detailed simulation has been performed by various groups, including ours [5, 6, 7, 8, 9]. Most of the recent results are based on the `GuineaPig` program [6], which generates electrons

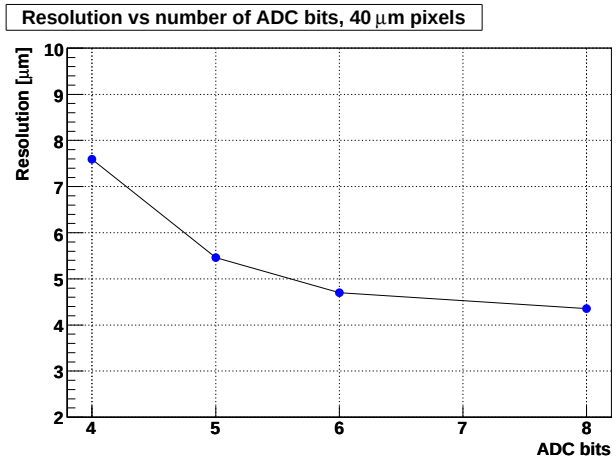

Figure 1: Point resolution vs. number of bit accuracy measured for a 40 μm pixel with a focused IR laser.

and positrons from both coherent and incoherent pair production taking into account the details of the colliding bunch dynamics. This accounts for the transverse momentum acquired by the electrons in their interaction with the intense electric field generated by the opposite bunch. These particles are then tracked in the solenoidal field through a specific detector geometry using `Geant-4`-based simulation. We have used several Vertex Tracker geometries implemented in the `Mokka` program for the LDC detector concept, which has a 4 T magnetic field.

These simulations show that the expected rate on the innermost layer, where the pair background is largest, is 900 hits BX^{-1} or 5 hits cm^{-1} BX^{-1}. The safety margin to be added here has been the subject of wide discussion at Snowmass 2005. Different beam parameters corresponding to the same luminosity give a spread of this rate by a factor of $\simeq$ three. Operation at $\sqrt{s} = 1$ TeV adds a factor of two. On the other hand, the physics uncertainties from cross sections, higher order corrections, etc. have been shown to be small and pair simulation using different, independent programs give comparable results.

Finally, some caution should be used since pair production at the ILC probes a beam regime away from those tested at other colliders. Using our beam test results for CMOS pixel sensors with low momentum e^-s we estimate an average multiplicity of 9 pixels/cluster, i.e. 45 pixels cm^{-1} BX^{-1}. For a 20×20 μm pixel geometry, i.e. 2.5×10^5 pixels cm^{-2}, this gives an occupancy of 2×10^{-4} BX^{-1}. It is generally considered that with an occupancy up to a few %, the pattern recognition is not significantly affected

by this background, as long as independent tracking information is available from the main tracker.

More detailed studies will be needed to exactly quantify the occupancy threshold at which the impact parameter develops significant non-Gaussian tails and how this varies for the detector concepts, which adopt different main trackers. If the threshold is below 2 % (3 %), the maximum number of ILC bunch crossings which can be integrated in the readout is $\simeq$ 85 (170), which corresponds to a readout time of the full chip of 25 μs (50 μs). On the three outer layers, these requirements can be relaxed and a readout time up to 200 μs appears to be adequate.

We recently developed a new CMOS pixel chip with digital output, based on the pixel cell of the LDRD-2 chip, by adding 5-bit ADCs at the end of each column. The chip can be read out at speeds up to 50 MHz, thus matching the ILC requirements in terms of readout speed and digitisation accuracy [4].

2.2.3 SOI pixels

Silicon on insulator (SOI) technology allows to fabricate CMOS circuits on a thin layer of silicon electronically insulated from the rest of the Si wafer. The isolation of the electronics layer from the detector volume offers clear advantages for designing monolithic pixel sensors for particle detection, compared to MAPS pixel devices, realized in standard CMOS bulk processes. First, both nMOS and pMOS transistors can be built without disturbing the charge collection and then the detector wafer can be biased, thus improving the efficiency of charge carriers collection. There have been already few attempts of developing SOI pixel sensors for charged particle detection with a high resistivity bottom wafer. Recently OKI Electric Industry Co. Ltd. and KEK have developed a 0.15 μm FD-SOI process where a low resistivity SOI wafer is bonded to a detector-quality, high-resistivity Si wafer. In addition substrate implants and contacts have been developed, which allows to use the lower wafer as detection volume and the top wafer for developing the associated readout electronics [12]. The availability of this process has opened up new, exciting possibilities for SOI pixel sensors with small pixel pitch and in-pixel data processing, such as digital output and time stamping, useful for the ILC as well as other applications in imaging and beam diagnostics.

A monolithic pixel sensor chip, with 10$\times$10 μm^2 pixels developed by our group in this process, which features but analog and digital pixels, has recently provided the first signal of high momentum particles on an SOI pixel device, in a beam test with 1.35 GeV electrons from the LBNL Advanced Light Source (ALS) booster [13]. While

many problems need to be addressed, the SOI technology appears particularly well suited for developing a pixel sensor with in-pixel time stamping and on-chip data sparsification, which represents an attractive option for the ILC Vertex Tracker.

2.3 Module Engineering Design

2.3.1 Sensor back-thinning

The material budget of the ILC Vertex Tracker should not exceed ∼0.1% X_0 per layer. This is mainly motivated by the need to efficiently identify all of the secondary particles in hadronic jets initiated by heavy quarks in order to distinguish c from b jets but also to determine the vertex charge. This translates into a requirement for the Si pixel chips not to exceed $\simeq 50$ μm in thickness. Below this thickness the contribution of the support structure becomes dominant. This is shown in Table 1 where the impact parameter resolution measured for tracks from fully simulated and reconstructed $e^+e^- \rightarrow Z^0H^0 \rightarrow \ell^+\ell^- b\bar{b}$ events at $\sqrt{s} = 0.5$ TeV are summarised. In this simulation, the Vertex Tracker consists of five layers of CMOS sensors with a 150 μm carbon fiber support, the measured impact parameter resolution is parametrised as $\sigma_{IP} = a \oplus \frac{b}{p_t}$. CMOS monolithic active

Table 1: Impact parameter resolution for fully simulated and reconstructed $e^+e^- \rightarrow Z^0H^0 \rightarrow \ell^+\ell^- b\bar{b}$ events at $\sqrt{s} = 0.5$ TeV for different values of the active sensor thickness.

Sensor thickness (μm)	a (μm)	b (μm GeV^{-1})
25	3.5	8.9
50	**3.7**	**9.6**
125	3.8	11.7
300	4.0	17.5

pixel sensors are ionising radiation detectors featuring a field-free, un-depleted sensitive volume. Because charge generation is confined primarily to a thin epitaxial layer of just 10-20 μm, it is possible to remove most of the bulk silicon using a back-thinning process without significantly affecting the signal charge collected. This makes CMOS detectors an appealing candidate for meeting the ILC physics requirements in terms of material budget. There has been some successful experience in back-thinning full wafers of CMOS pixel structures, but there have been questions on the actual effect of back-thinning on charge collection [11, 10]. A detailed study of charge collection and signal-to-noise performance of CMOS monolithic pixel sensors before and after back-thinning

has recently been carried out at LBNL. The results of tests with laser and ^{55}Fe show no significant degradation in the amount of collected charge after back-thinning to 39 μm and 50 μm and that the gain is not significantly affected. Beam test data confirm that neither the charge collection nor the signal-over-noise ratio of the detectors for energetic charged particles are affected by the back-thinning process down to thicknesses below 50 μm [14].

2.3.2 Engineered Ladder design

For sensors with thickness $\leq$ 100 μm, the contribution of the ladder support becomes important in the definition of the material budget. A crucial question is the definition of the optimal choice for sharing of the material between the sensor itself and its mechanical support. Further, the specifications on the sensor power dissipation depend on the stability of the mechanical support under thermal cycling and on the requirements for the cooling system. These considerations make the engineered design of the detector ladder an integral part of a program of R&D on sensors for the Vertex Tracker. An activity on the engineered ladder design at LBNL is supported in part by an LCRD grant and profits from significant synergies with the design of the HFT detector for the STAR upgrade and experience gained on the use of composite materials for the ATLAS Pixel detector. In particular the STAR HFT, based on the use of thin CMOS monolithic pixel sensors, has developed and characterised the lightest vertex ladder designed to date (see Table 2), which has a material budget within a factor of two from the assumed ILC requirement. Their project represents a natural precursor for the ILC Vertex Tracker. The possibility of sharing prototypes, engineering and testing equipment allows us to carry out this activity in an extremely efficient and cost-effective way. In order to signif-

Table 2: Material budget of the STAR HFT ladder prototype

Component	X/X_0 (%)	Si Equivalent Thickness (μm)
Sensor	0.053	50
Adhesive	0.014	14
Kapton cable	0.090	84
Adhesive	0.014	14
CF Support	0.110	103
Total	0.282	264

icantly improve on the STAR HFT material budget it appears necessary to reduce the

thickness of the carbon composite support and to develop alternative schemes for chip interconnect and routing signals to and from the chips on the ladder. Another important consideration comes from the ladder width. If the chip is readout during the bunch train using a column parallel architecture, the readout speed limits the number of pixels across the chip width. Chips with 256 pixels arranged on a 20 μm pitch on a single column have been proposed. Digitisation and sparsification will take place along a strip at the chip edge. We have already designed a chip with 5-bit ADCs at the end of the column which match the 20 μm pitch. This strip is estimated to have a width of $\simeq$ 2 mm, which brings the sensitive width = 256$\times$20 μm to 70 % of the overall width of the chip. This requires a significant overlap of chips on neighbouring ladders and increases the material traversed on average by particles. Longer columns are preferable, provided the readout speed can be increased accordingly to keep the occupancy constant. These issues are all significantly inter-related and are best addressed by integrating tracking simulation and ladder design with the chip design.

2.3.3 Ladder cooling

Cooling represents an important component of the ILC Vertex Tracker design. On one hand most technologies, including the CMOS and SOI sensors we are developing, may find it advantageous to cool the sensor. This reduces the leakage current and improves the signal-to-noise peformance, which benefits both the hit reconstruction efficiency and its resolution. On the other hand, it is essential to avoid active ladder cooling to keep the material budget low. This requirement sets a tight constraint on the chip power dissipation. Measurements carried out by our group in collaboration with LBNL STAR group on a HFT thin sensor ladder prototype show that a 1-3 m/s airflow removes $\simeq$ 70-100 mW/cm^2 without inducing significant vibrations. Assuming a ladder to be 10 cm long and 1 cm wide with 2 mm of electronics at the edge and 20 μm wide pixels, we have 5000 columns of pixels with ADCs at their end. The maximum power dissipation per column is 0.4 mW. Chip power cycling is being considered as a mean to reduce the total power dissipation. The LDRD-2 chip developed by our group features power-off of the pixel transistors when the chip is not read out. It has to be taken into account that other components contributing to the power budget, such as the ADCs, will only be clocked during readout. The gain from the low ILC duty cycle has to be estimated on real prototypes. These limitations on the chip power consumption has been taken into account as a requirement in the ADC design for the new chip with on-chip ADCs (LDRD-3).

Further studies are needed. The measurements carried out so far used a single ladder with an almost laminar airflow. In the real Vertex Tracker there will be five, closely spaced ladders, mounted on end-rings with cables and services attached at both ends. Therefore it is important to re-assess the amount of dissipated power which can be removed by airflow in a setup as realistic as possible.

2.3.4 Power distribution

As the operating voltage of the electronics decreases and the size of particle detectors increases, the problem of power distribution must be addressed in a systematic way. It is no longer sufficient to develop a system in the laboratory and transplant it to a detector environment by simply replacing the cable plant. The power efficiency of a conventional system scales like $V_d/(I_d R)$, where V_d and I_d are the operating voltage and current, and R is the total load resistance of the system, including the cable plant. It is clear that as V_d approaches zero, power efficiency becomes a problem even for low power (small I_d) systems. For conventional systems this problem results in massive cable plants (small R) which in addition typically require dedicated cooling. The problem is compounded by large ratings that force a very low IR drop on cables passively connected to the chip in order to avoid damage due to transient over-voltage. These are universal issues, affecting the ILC detectors as well as those planned for the SLHC, which need to be addressed at the time of the engineered design of the detector ladder.

2.4 Tracking and Vertexing: Reconstruction and Simulation

2.4.1 Tracking Pattern Recognition

Track reconstruction in an ILC detector depends on the Vertex Tracker not only for a precise extrapolation to the point of origin but also in the pattern recognition. Charged particles with low momentum or at small polar angle benefit from the Vertex Tracker points in addition to those available in the main tracker. In the past there have been different approaches for including the ILC Vertex Tracker in the track pattern recognition and on the need to achieve self-consistent pattern recognition capabilities. In particular, a detailed study was performed based on the anticipated performances of a CCD-based detector at the stage of R&D work in 2000 [15]. This study found that the amount of fake tracks obtained by standalone pattern recognition in presence of pair background ranged from 0.1/event to 0.5/event, depending on the assumed readout frequency. An extrapolation from the main tracker was then needed to remove them. An update of these

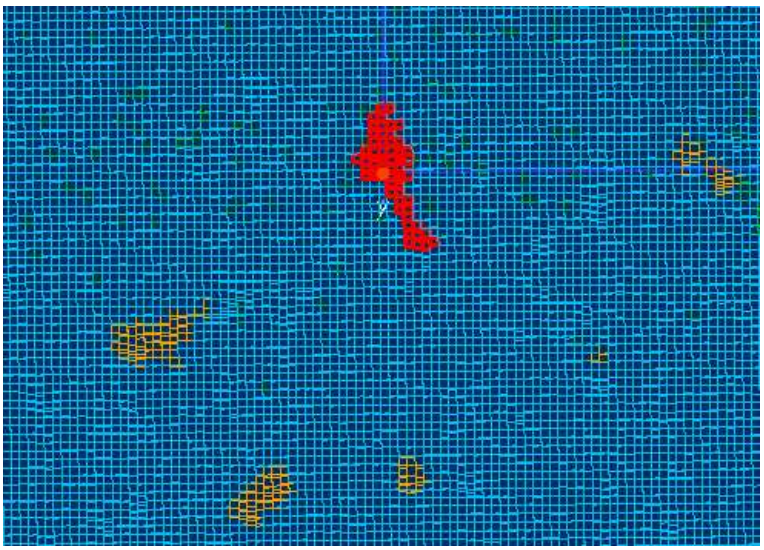

Figure 2: CMOS pixel sensor response to low momentum electrons. This event display shows clusters recorded with the LDRD-2 chip on the 1.5 GeV ALS beam after an Al scraper. The clusters from low momentum electrons are evidently broad and asymmetric.

studies is now needed using full simulation and dedicated pattern recognition algorithms, optimised for the different pixel architectures and detector concepts. We have already developed standalone track pattern recognition processors which can be applied to simulated ILC events and real beam test data. We intend to continue this development, incorporating effects from improved detector response and results from beam tests.

2.4.2 Effect of Low Energy Electron Background

The low energy electron background, originating from pair production processes in the beam collision is the largest source of particle background for the Vertex Tracker. Significant efforts have been carried for characterising this background, as mentioned above, and some ideas have been put forward to reduce its effect on track pattern recognition, by applying a cluster shape filtering. Low momentum electrons, spiraling in the solenoidal detector field are expected to hit the Vertex Tracker sensors at smaller dip angles compared to particles emerging from the high energy e^+e^- collision. Pair electrons would give broader and asymmetric clusters which could be identified and rejected. We have started a program of study of the cluster shape of low momentum electrons in CMOS pixel detectors. The study is carried out using both fully simulated and beam test data. These data are collected at the ALS by either positioning the detector in the halo of the 1.5 GeV e^- beam by placing an Al scraper on the beam line (see Figure 2). In

the near future we intend to use also the LBNL LOASIS facility, which studies plasma acceleration of electron beams and is equipped with a magnetic spectrometer at the end of the beamline. This will make possible to study the response to a momentum-selected e^- beam with energy ranging from 50 MeV up to $\simeq$ 1 GeV.

2.4.3 Tracking Performance Validation at Beam Tests

The R&D program needs beam test data for system tests, simulation validation and assessment of single sensor and tracking performance. Plans for beam tests have been discussed at a workshop held at Fermilab in January 2007.

We have been performing beam tests at two facility: the BTS beamline at the LBNL Advanced Light Source (ALS), which provides electrons at energies between 1.2 GeV and 1.9 GeV and the MTest facility at Fermilab, which offers 120 GeV protons, as well as lower energy particles. Data taking at the MTest is performed as part of the T-966 beam test experiment. The availability of reconstruction processors, which can be applied to ILC simulated events as well as real data from beam test make possible to carry out detailed simulation validation and test reconstruction algorithms in realistic conditions.

3 R&D Program and Work Packages

3.1 WP-1: Benchmarks and Physics Tools for VTX Optimisation

WP-1 aims at providing a consistent set of physics benchmark processes, simulation and reconstruction tools to support the optimisation of the Vertex Tracker from sensor design to ladder layout and tracker geometry. Much work has already been devoted to studying the ILC physics program, developing tools to reconstruct physics objects, optimising algorithms and modelling the Vertex Tracker in simulation. But we still need a definitive assessment of the impact of the basic Vertex Tracker performances on the ILC physics reach. Therefore, we propose to carry out a systematic investigation of a small but representative set of physics processes, with well-defined accuracy requirements, using a full chain of sensor simulation and digitisation, pattern recognition, tracking and jet flavour tagging, implemented in the C++ `Marlin` framework. Each software package will be validated using beam test data for various sensor and ladder prototypes and will be updated with new designs as these are becoming avaliable. We intend to provide a simulation and reconstruction environment open to contributions by other groups and adaptable to different detector parameters. The work carried out by the LCFI group

for jet flavour tagging and the MPI, Munich group for sensor digitisation represent valid examples.

3.1.1 Recent Progress

The LBNL group promoted the definition of a set of benchmark of reactions for the optimisation of the detector concepts [1]. More recently, a broad effort on simulation and reconstruction of particle tracks, including detailed charge generation in the detector layer, clustering and hit reconstruction, background hit rejection, pattern recognition, track and vertex fit and jet flavour tagging, has been deployed. The `Marlin` C++ framework is used for digitisation and event reconstruction and consists of a set of processors performing dedicated reconstruction tasks, based on the `lcio` persistency classes. This makes possible to use the objects generated by these processors also in conjunction with reconstruction frameworks based on Java. We have developed custom processors for hit digitisation for CMOS pixels, pattern recognition and track fit. The response of CMOS

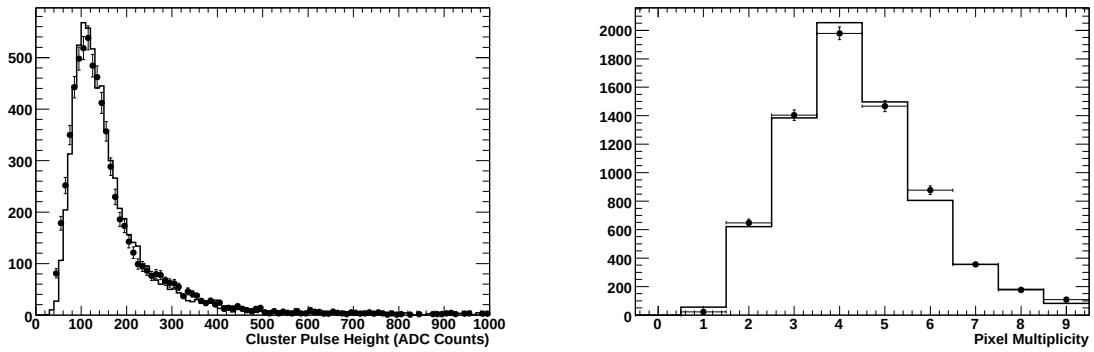

Figure 3: Detector response to 1.5 GeV e^-s in data (point with error bars) and in the `Geant-4+Marlin` simulation and reconstruction. The cluster signal pulse height (left) and pixel multiplicity in a cluster (right) are shown for clusters associated to reconstructed particle tracks (from [18])

pixel sensors has been simulated starting from energy deposits modeled using the `Geant 4` package [16]. Charge collection is modelled by the diffusion of charge carriers generated in the epitaxial layer and collected at the pixel diode. The epitaxial layer thickness is taken from the process specifications and the diffusion coefficient is treated as a free parameter, tuned to reproduce the observed pixel multiplicity in a cluster. A dedicated cluster reconstruction program has been implemented as a separate processor and test beam data have been converted to the `lcio` format, thus allowing analysis of both real

data and simulation with the same framework and code. The pixel response simulation has been validated for various sensors and beam particles and energies in terms of the cluster size, cluster pulse height and cluster shape [17]. Simulation accurately reproduces the data response. Results for the LDRD-2 chip on the ALS 1.5 GeV e^- beam are shown in Figure 3.

Standalone pattern recognition and track fit have been developed both for an helix and a straight track model for LDC simulation as well as simulated and real beam test data. We are currently finalising the development of additional processors which take advantage of the reconstruction accuracy of the ILC vertex tracker. These include jet flavour tagging, using algorithms already applied at LEP, neutrino energy recovery in b jets with semi-leptonc decays, based on topological reconstruction and kinematical constraints of events with leptons, and vertexing algorithms. The vertex fit processors are based on the porting of algorithms developed for CDF, for helix track representation, and HeraB/LHCb, for straight track representation. We have also developed a `Marlin` processor based on code ported from the DELPHI experiment, which performs constrained kinematic fitting. These processors are currently being released in the `MarlinReco` distribution.

These efforts are matched by a program of physics benchmarking based on the study of Dark Matter-motivated SUSY scenarios. The selected processes rely heavily on jet flavor tagging to suppress background and enable us to assess the Vertex Tracker performance and to optimise its design. The first channel under study is heavy Higgs boson pair production, $e^+e^- \rightarrow H^0A^0 \rightarrow b\bar{b}b\bar{b}$, $\tau^+\tau^- b\bar{b}$, $\tilde{\tau}\tilde{\tau}b\bar{b}$ at $\sqrt{s} = 1$ TeV. This process is crucial for understanding the observed Dark Matter in the Universe in Supersymmetric scenarios where its relic density is controlled by the ratio of the masses of the lightest neutralino and of the pseudo-scalar A^0 boson. In these scenarios LHC data will most likely be inconclusive for testing the compatibility between collider data and Cosmic Microwave Background measurements. Instead, the ILC should supply the data to predict the DM density with a precision nearly matching that from the current WMAP measurements, provided we can measure the A^0 boson mass and the H^0 boson decays accurately enough [19]. This channel is a good exemplification of a process which is challenging for the ILC detector and has well-defined requirements in terms of measurement accuracy. It has been already studied using parametric fast simulation [20]. Now, we perform a re-analysis based on full `Geant-4` simulation and `Marlin` reconstruction. Signal and background events have been generated at LBNL, DESY and Fermilab and using GRID resources. The simulation is based on the LDC detector concept and a

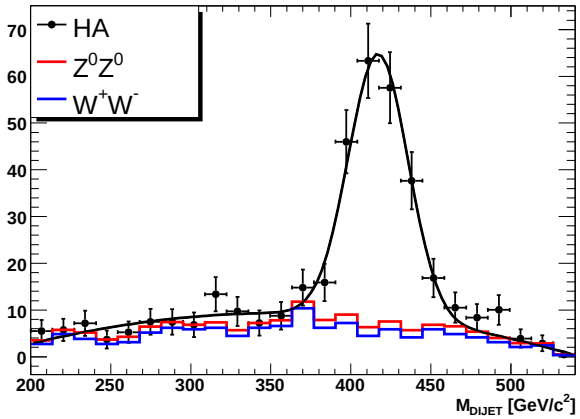

Figure 4: Di-jet invariant mass for fully simulated and reconstructed $e^+e^- \to H^0A^0 \to b\bar{b}b\bar{b}$ events at $\sqrt{s}$=1 TeV, in the LDC with a CMOS Vertex Tracker. b tagging achieved with the Vertex Tracker is essential to suppress the ZZ and WW backgrounds. (from Ref. [21]

five-layered Vertex Tracker, based on 50 μm-thick CMOS pixel sensors with 17×17 μm^2 pixels, analog readout and charge centre-of-gravity determination. Preliminary results of the $e^+e^- \to H^0A^0 \to b\bar{b}b\bar{b}$ analysis have been presented at LCWS07. The di-jet invariant mass distribution for the signal and the main SM background sources are shown in Figure 4. The measured A^0 mass reconstruction accuracy of 0.3 % matches that obtained with the parametric fast simulation [20] and validate the anticipated ILC role in understanding the DM nature in these scenarios. Studies are currently underway to assess the sensitivity on variations of the detector design (layer thickness and forward coverage) and response (pixel size and readout speed). With the completion of this analysis, our group has put in place the full simulation, reconstruction and analysis software chain which bridges from pixel sensor response to ILC physics potential.

3.1.2 Future Work

WP-1 should extend over three years. In year 1 we foresee the main task to be the tuning and optimisation of reconstruction packages, a comparative study with other algorithms (such as `ZVTOP` for jet flavour tagging) and a study of the changes in performances on simple objects (such as single particle and single jets) by varying the Vertex Tracker parameters. Results from the T-966 and ALS beam tests will be implemented and a detailed study of the effect of pair background will be carried out. Concurrently two

benchmark processes will be studied, $e^+e^- \rightarrow H^0A^0$ at 1 TeV and $e^+e^- \rightarrow b\bar{b}$, $c\bar{c}$ at 0.5 TeV and 1 TeV. In year 2 a larger set of benchmark reactions will be studied. These should include Higgs decay branching fractions for $M_H = 120$ GeV and 160 GeV, $e^+e^- \rightarrow H^0H^0\nu\bar{\nu}$ for $M_H = 120$ GeV and $e^+e^- \rightarrow \tilde{\tau}_1\tilde{\tau}_1$ at $\sqrt{s} = 0.5$ TeV. This activity will allow to map precisely the effect of Vertex Tracker performances on the ILC physics reach. By year 3, the sensor R&D should have progressed to a point where a set of preferred designs will start to clearly emerge, ladder prototypes will have been characterised and new beam test data will be available. The characterisation of the ladder mechanical stability will allow to include such effects as detector alignment. At that point the analysis of those benchmarks found to be most sensitive to details of the detector response should be repeated for these sensor options. The results of these studies also depend on the detector concept adopted. However, by keeping the response of calorimetry and central tracker constant, it will be possible to highlight the effect of the variation in the Vertex Tracker, through an analysis of relative differences of accuracy and sensitivity of the physics measurements.

3.2 WP-2: Development of Monolithic CMOS Pixel Sensor with in-pixel CDS, in-chip ADCs, Data Sparsification and Fast Read-Out

WP-2 consists of the activities needed to develop a reticle-size CMOS monolithic pixel sensor with in-pixel CDS, on-chip ADCs and data sparsification, which can be readout in 25-50 μs and with power dissipation kept to a level $\leq$0.4 mW/channel. The performance of this chip, with 15×15 μm^2 or 20×20 μm^2 pixels and thinned to 50 μm, should be assessed in a test on a high momentum particle beam by 2011-2012.

3.2.1 Recent Progress

Over the past 3 years, a Laboratory Directed Research and Development (LDRD) grant has funded the design, fabrication and test of 3 generations of CMOS monolithic pixel prototypes. At each step of the development, various pixel architectures and layout options have been explored, driving the choice for the design of subsequent prototypes. The first two prototypes, described in the following, featured a serial analog readout; on-chip digitisation was then implemented in the third and latest prototype which will be described afterwards.

The LDRD-1 chip was designed and fabricated in 2005 in the AMS 0.35 μm CMOS-OPTO technology, which provides an epitaxial layer with a nominal thickness of 14 μm.

It featured 3 sections with pixels of 10, 20 and 40 μm pitch, all equipped with a 3×3 μm^2 charge-collecting diode and a standard 3-transistor (3T) architecture for the in-pixel readout circuitry [2] This chip, with its relatively simple architecture, was intended as a first technology evaluation, using a process optimized for imaging applications. The sensor allowed the parametric study of cluster multiplicity and point spread function as a function of pixel pitch, and also provided a test-bench for the development of the readout system and of the test setups employed in the various measurements.

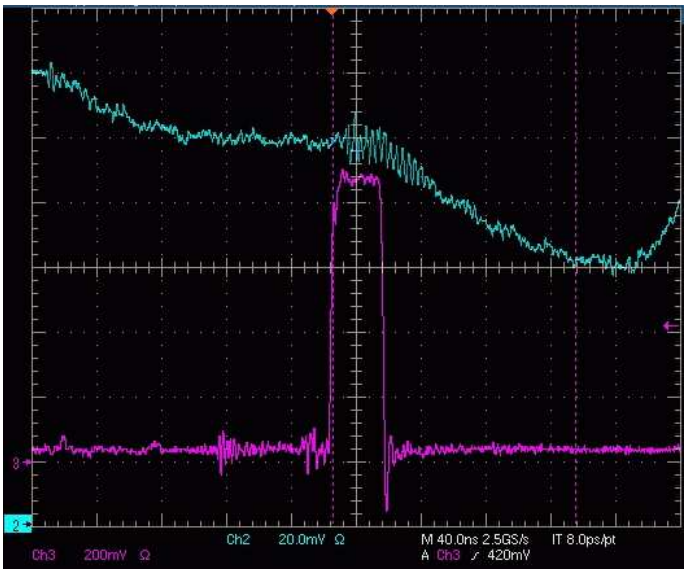

Figure 5: Charge collection time measurement for the LDRD-1 CMOS pixel chip. The analog signal from a single pixel is shown by the upper trace while the pulse indicates the time when the laser pulse is sent on the pixel. The trace is stretched compared to the laser pulse duration. The pixel level reaches a plateau after 150 ns.

The sensor charge collection time has been determined using a fast (0.5-5 ns) IR laser pulse focused on a single pixel and by following the collected charge signal. The result of ∼150 ns agrees well with the expectations coming from the resistivity of the epitaxial layer (see Figure 5).

The LDRD-2 chip is a more advanced prototype fabricated in 2006, also using the AMS 0.35 μm technology. The array of 96×96 pixels of 20 μm pitch is divided in 6 subsections implementing different sizes of the charge collecting diodes (3×3 μm^2 and 5×5 μm^2), 3T or self-bias pixel architecture and presence of guard-ring or not around the charge collecting diodes, in order to evaluate possible beneficial effects of the guard-ring against radiation damage. All sectors implement in-pixel CDS: the pixel dark level and

charge signal are consecutively stored on 2 capacitors integrated in the pixel; both signals are then clocked to the chip analog outputs, after which the CDS difference is obtained either via FPGA or via the online DAS [3]. Pixel transistors are switched off outside the readout cicle to limit power consumption. The readout scheme is based on the rolling-shutter scheme, i.e. rows are reset and read out in sequence, so that integration time is the same for all pixels. The chip was designed to be operated up to a clocking frequency of 25 MHz and has been successfully tested under these conditions both with radioactive sources and high-energy particle beams [4]

The prototype chips have been mounted on a proximity board providing the necessary power supplies and a first amplification of the chips analog signals, and read out by a dedicated DAQ modules with an FPGA board which provides the clock patterns to the chips and also drives four 14-bit ADCs for the digitization of the chip output. The board is then interfaced with the DAQ PC by a National Instruments PCI card, controlled by a LabView-based online data acquisition program.

The LDRD-1 and LDRD-2 detector have been extensively tested using the same test protocol, starting from lab calibrations with a ^{55}Fe source and laser beams of different wavelengths to beamtests performed with the 1.25-1.9 GeV electron beam of the BTS facility at the Advanced Light Source (ALS) and with the 120 GeV proton beam at the MTBF facility at FNAL. For the LDRD-2 chip, signal-to-noise ratios between 15 and 20 have been obtained for minimum ionising particles, with average cluster multiplicities between 4 and 5 depending on the size of the charge collecting diode (see Figure 6). A larger charge collection diode proved to be more beneficial in terms of charge collection efficiency and more limited signal spread.

Tests have been performed comparatively before and after irradiation experiments performed mainly with 30 MeV protons and 1-20 MeV neutrons at dedicated lines at the 88-inch Cyclotron at LBNL. The technology was proven to be radiation hard against moderate doses of non-ionizing radiation ($\sim 10^{12}$ neutrons/cm^2). It nevertheless showed to be sensitive to ionizing doses of the order of few 100 krad, equivalent to several years of operation at the ILC at the position of the first layer of the Vertex Tracker. The main effect observed was a significant increase of the pixel leakage current, which could be partially recovered by means of cooling. The sensors nevertheless retained acceptable particle detection capabilities, despite the degraded noise performance.

A third protoype, the LDRD-3 chip, has been submitted for fabrication in Summer and has just been received back from the foundry. The chip features the same in-pixel CDS as in the LDRD-2 prototype, combined with a column parallel readout and

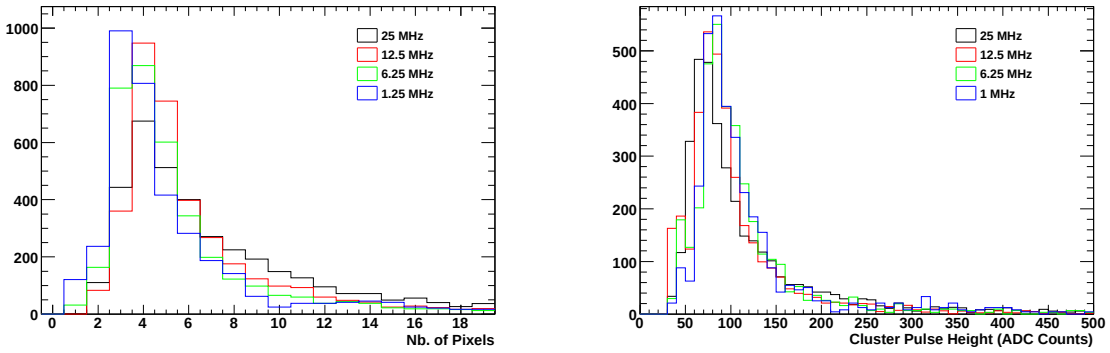

Figure 6: Performance of the LDRD-2 chip on the ALS 1.35 GeV beam for various readout frequencies. (Left) Pixel multiplicity in e^- clusters. (Right) Cluster pulse height. These plots show that the chip performs properly at 25 MHz.

integrated ADCs at the end of each column. Figure 7 (a) shows a sketch of the chip architecture. The array consists of 96×96 pixels on a 20 μm pitch. The pedestal and signal levels from each pixel in the column are sent to the bottom of the column, the CDS difference being performed by a 5-bit successive approximation, fully differential ADC running at 300 MHz clock frequency, which fits a 20 μm × 1 mm footprint (see Figure 8).

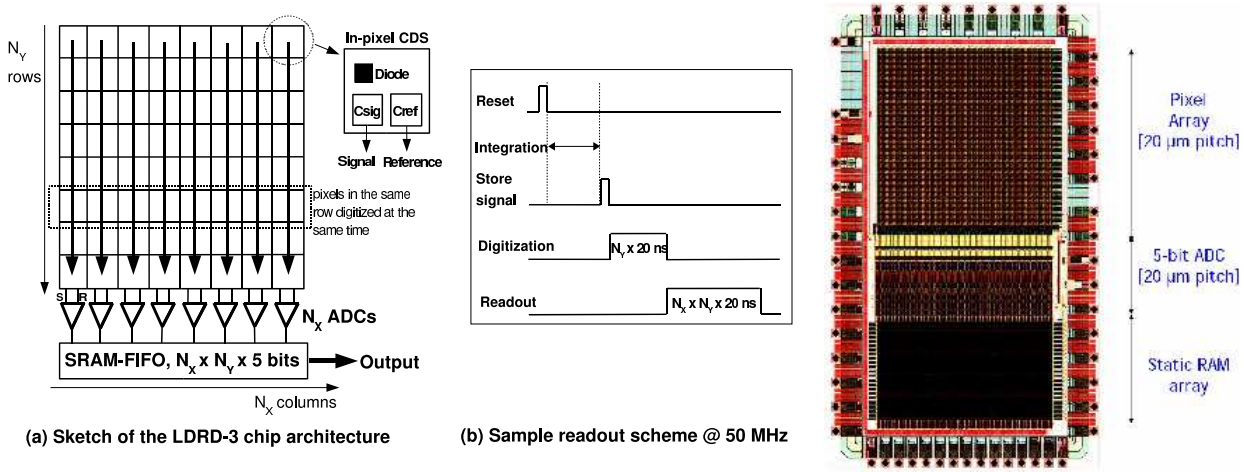

Figure 7: Schematic of the LDRD-3 chip, readout timing diagram and layout.

At the bottom of the pixel matrix and after the array of ADCs, an SRAM memory

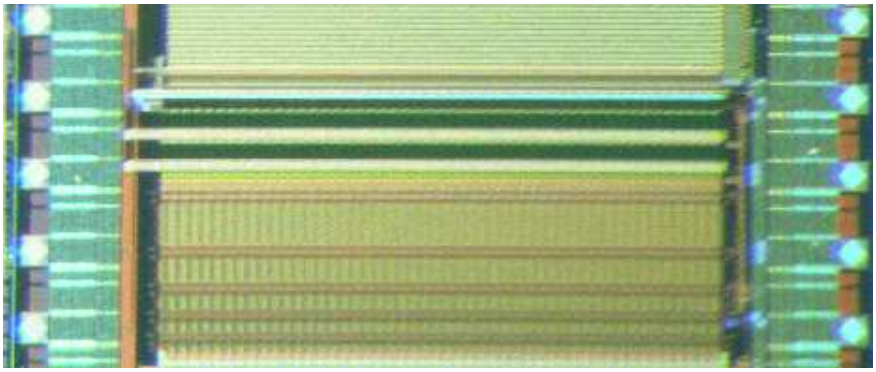

Figure 8: Photograph of the ADC section of the LDRD-3 chip. The height is 1 mm.

cell stores the digital image from the pixels, which at the end of the digitization time is then transferred serially to the chip output. Figure 7 (b) also illustrates the basic timing sequence for the chip readout. After a global reset, the image is integrated for a certain amount of time, at the end of which the signal is stored in the capacitor present in each pixel. This is then followed by a column-wise digitization of the pixel signals with concurrent storage in the SRAM-FIFO. The image is then read out from the SRAM-FIFO memory using a 50 MHz clock. The design of the LDRD-3 chip was driven by the results of a detailed study of data collected with the LDRD-1 chip for different pixel pitches, which had shown that 5-bit ADC accuracy is sufficient to achieve the desired single point resolution, provided that the pixel pedestal can be removed before digitisation.

3.2.2 Future Work

Future work for WP-2 should extend over a period of three years (FY08-FY10) for the optimization of the sensor architecture through prototype chips implementing more advanced functionalities. This will lead to a choice for the final architecture to be adopted around FY11 for the fabrication of a large scale prototype. This will be used for a tracker demonstrator as described in WP-5.

In year 1 a modified version of the LDRD-2 chip with an improved pixel layout featuring a radiation hard design for the charge collecting diode will be submitted. The chip will be used to test the radiation hardness limit of the technology. This is of interest for our application as well as for applications for electron microscopy currently being tested at the LBNL NCEM facility. Tests are expected to be performed in FY08 in parallel with the test of the LDRD-3 prototype.

The further continuation of the LDRD line will have to address the optimization of

the readout architecture. The architecture of the LDRD-3, with a global integration time and then a column-wise digitization with storage in memory and delayed readout, is well tailored to beam test applications. Power cycling tests will also be carried out. If the LDRD-3 chip performs according to design specifications we plan to produce a scaled up version (LDRD-3+) in year 2. This chip would have 512×512 pixels on an active surface of 1×1 cm^2 and should have column parallel readout at 25 MHz. This would offer an opportunity to study the chip performances with scaling its size. In particular, it will be important to assess speed issues, arising from driving signals down long lines. The LDRD-3+ chip would be an ideal candidate for a new beam telescope with fast readout, as discussed under WP-5.

In parallel we shall address in-chip data reduction. This would be done with a new chip (LDRD-4), to be fabricated possibly in year 2, which will include column-parallel sampling with concurrent digitisation and zero suppression by digital comparators placed after the ADCs. This will also allow to reduce the size of the SRAM-FIFO needed to buffer the data at the chip output.

After the LDRD-4 chip, the further step we envisage is the introduction of more advanced on-chip data sparsification capabilities, such as hot pixel removal, cluster search and, possibly, cluster shape analysis. Work on data sparsification algorithms will start in year 1, ranging from conceptual design to FPGA implementations. Experience has already been gained in the collaboration with the STAR HFT group. This has developed a DAQ system featuring FPGA-based data sparsification. In their system the pixel data, digitized to 8 bit after CDS and pedestal subtraction, are sent to a hit finding algorithm based on the simple readout of the address of a center pixel high threshold hit with the surrounding 8 pixels meeting additional cluster selection criteria. Once the criteria for a cluster are met, the center pixel address is stored into a readout FIFO. The method is extendable to allow for multiple simultaneous thresholds and geometric pattern triggers. Starting from the STAR experience, new cluster finding algorithms will be studied and implemented in the FPGA-based DAQ system used for prototype tests. A first real world test of candidate algorithms in the presence of a large number of pixels/readout channels will be performed using the TPPT-2 telescope at the FNAL MTBF facility in Summer 2008 (see WP-5). Data from the TPPT-2 is currently being sparsified at the DAS level, and the implementation of FPGA-based data sparsification algorithms is foreseen in the upgraded DAQ system which is currently being developed.

Once a suitable algorithm is defined and successfully tested, work will start for porting it into a feasible logic circuitry to be implemented in a prototype chip. This

should happen in year 3 with the fabrication of a new chip (LDRD-5) with in-pixel CDS, fast column parallel readout and integrated digitization and data sparsification. If successful, the LDRD-5 architecture can be scaled up to a reticle size sensors to be used in the fabrication of the TPPT-3 telescope and in the integration of a Tracker Demonstrator.

An open issue is the choice of the fabrication technology. Indeed, sensor architecture development needs to be constantly accompanied by the search for a suitable fabrication process providing a small enough feature size that allows the integration of in-pixel functionalities within a small pixel pitch, enough number of metal layers and sufficient thickness of the epitaxial layer. While the AMS 0.35 μm OPTO technology, which so far has shown the best performances, is expected to remain available for a few years to come, novel processes in 0.18 μm feature size with thick epi layer and an increased number of metal layers are becoming available. Submissions probing these new processes should be considered alongside the main architecture development work.

3.3 WP-3: Development of SOI Monolithic Pixel Sensor with Binary Output and Time Stamping

The SOI technology offers the opportunity to increase the complexity of the pixel cell and therefore the functionalities implemented in-pixel. WP-3 aims at developing a concept for an SOI sensor with 10×10 μm^2 or 15×15 μm^2 pixels with binary output and time stamping capabilities. The development of SOI monolithic pixel sensors is much more recent compared to more conventional MAPS sensors in CMOS bulk process. This work-package will represent a research activity starting from the OKI 0.15 μm FD-SOI process and exploring various designs and also alternative processes. The activity will be carried out in close contact with the R&D effort starting at LBNL and aimed at the application of SOI pixel sensors to beam diagnostics at a Free Electron Laser demonstrator to be built as part of the LOASIS facility. This program is supported by a strategic LDRD grant at LBNL starting in FY08. Further there is a significant interest in SOI technology for applications at SLHC. The INFN groups of Torino and Padova are interested in pursuing these activities with special attention to these applications. In particular, the INFN Padova group can provide detailed characterisation of radiation hardness at the INFN Legnaro National Laboratory, using a γ ray source which is complementary to the p and n irradiations available at LBNL.

3.3.1 Recent Progress

LBNL has designed and recently tested, jointly with the INFN Padova group, the first SOI pixel chip to obtain a signal on a a high momentum particle beam. The chip (LDRD-SOI) has been produced in the 0.15 μm FD-SOI process by OKI Electric Industry Co. Ltd. , Japan. It features an array of 160×150 pixels on a 10 μm pitch (see Figure 9). The OKI SOI technology includes thin-oxide 1.0 V transistors and thick-oxide 1.8 V transistors. The left-most 50 columns are simple analog pixels constructed with 1.0 V transistors. The centre 50 columns are constructed with 1.8 V pixels, and the right-most 50 columns are clocked, digital pixels. The transistor characteristics have been studied as a function of the sensor substrate bias, V_d, in order to evaluate possible back-gating effects, which are expected to be significant due to the relatively small thickness of the buried oxide. The measurements are performed with the transistor biased in saturation region. The threshold voltages shift from 0.24 V at V_d=1 V to 0.07 V at V_d=15 V, consistent with an increased back-gating effect. The response of the analog sections of the chip has been tested with an 1060 nm IR laser, for different V_d values. The laser is focused to a $\simeq$20 μm spot and pulsed for 30 μs between successive readings. We measured the signal pulse height in a 5×5 matrix, centred around the laser spot centre. The measured signal increases as $\sqrt{V_d}$, as expected from the increase of the depletion region, until $V_d \simeq 9$ V, where it saturates, to decrease for $V_d \geq 15$ V. We interpret this effect as due to the transistor back-gating which affects the 1.0 V transistor pixels at lower values of V_d. The pixel chip has been tested on the 1.35 GeV electron beam-line at the LBNL ALS for depletion voltages 1 V$\leq V_d \leq$15 V, corresponding to an estimated depletion thickness from 8 μm to 56 μm. There is only a small background arising from noisy pixels, which survives the bad pixel cut and the cluster quality criteria. We observe a clear signal from the beam particles. Figure 9 shows the cluster pulse height for data taken with beam at $V_d = 10$ V. Further, irradiation with 30 MeV protons and 200 keV electrons have revealed that the structure is sensitive to radiation damage for doses of several hundred kRad. Preliminary results from a neutron irradiation at a fluence of 10^{11} n cm^{-2} do not show any significant noise performance degradation. These results are very encouraging for the perspectives of developing a monolithic pixel chip in SOI technology for application at the ILC. The LDRD-SOI-1 chip also includes a sector with digital pixels. This sector has been tested with a focused laser IR beam and with 200 keV e^-s on an electron microscope and we have signals both from the laser and the electron beams. A beam test at the ALS is currently in preparation. The design of these pixels is quite attractive, since it does not require a preamplification stage; therefore it has only

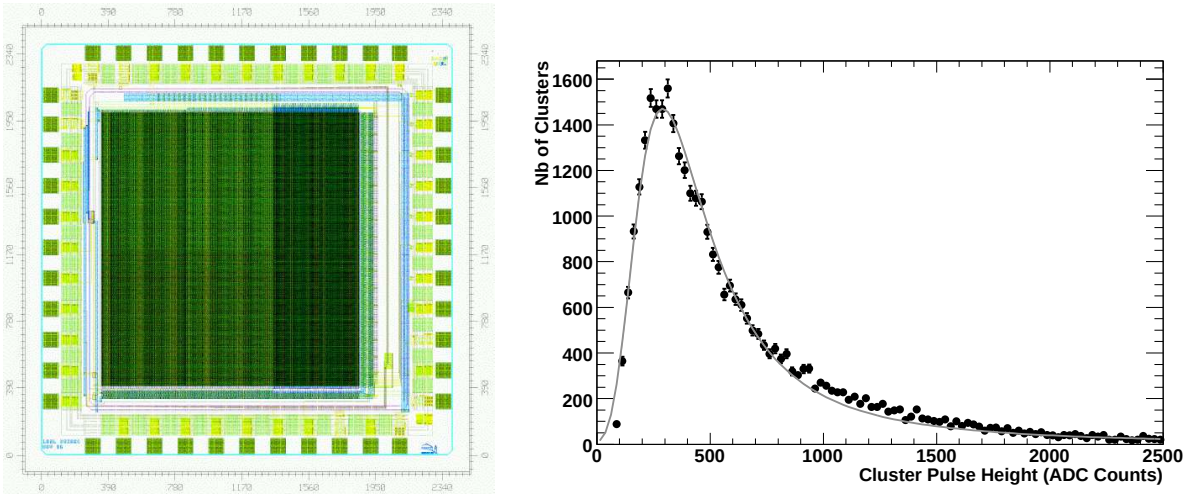

Figure 9: (Left) Layout of the LDRD-SOI-1 pixel chip. (Right) Cluster pulse height distribution for 1.35 GeV e^-s for V_d = 10 V, V_{DD}=1.8 V. The slight excess of events above the fitted Landau function is interpreted as due to low momentum electrons in the beam (from Ref. [13]).

minimal power dissipation. The data collected consistently shows that the SOI pixels are functioning but the back-gating effect is significant. This currently limits the depletion voltage that can be applied. Solving this issue is crucial for a successful exploitation of the SOI technology.

3.3.2 Future Work

The R&D on SOI sensors still entails more research than development. While the first results from test of the LDRD-SOI chip are very promising, there are several issues which need to be addressed. The first is the problem of back-gating. Here, we plan to carry out extensive device simulation to find a pixel layout which minimises the effect. Other options should also be considered and might include tests using different processes. For example the FLEXFET SOI design by American Semiconductor, with dual-gate transistors, has been claimed to be an effective way to reduce the back-gating effect since the bottom gate shields the transistors in the top layer from the voltage in the substrate, but this has not been demonstrated yet. A second issue is the minimisation of the leakage current. A next submission in the OKI 0.20 μm process is already expected to give improved performances in this respect. A third issue is radiation hardness. In this area LBNL is especially well suited for carrying out irradiations using the proton beam of the 88" cyclotron and a new neutron source, providing both thermal and 14 MeV neutrons.

In year 1 we plan to have a second chip produced with a new OKI process ensuring low leakage current. The chip will consist of an analog and a digital section. Different guard-ring designs will be implemented to limit the transistor back-gating effect. The chip will be fully characterised including a beam test with the TPPT beam telescope. In year 2 design activity will start for the implementation of in-pixel time stamping capabilities.

There is already a significant number of groups active in SOI pixel R&D and more are considering joining the R&D effort. At this stage, we feel that it would be highly desirable to share know-how and carry out a coordinated program to cover different technological paths, avoiding duplications and offering to all partners shared benefits.

3.4 WP-4: Development of Engineered Vertex Tracker Ladder based on Thin Pixel Sensors

WP-4 aims at the development of a Vertex Tracker ladder based on thin pixel sensors, with an overall material budget compatible with the ILC requirements. We intend to characterise carbon composite prototype structures and deploy a fully equipped prototype on the Fermilab MTest beamline. This work-package bridges between sensor development and detector design and it is intended to match the sensor performance with an advanced engineered design which addresses sensor thinning, mechanical support, thermal management and power distribution.

3.4.1 Recent Progress

There has been some significant progress on four main areas relevant to WP-4. These are chip back-thinning, ladder design, cooling studies and R&D on DC-DC converters.

The LBNL group has carried out a program of back-thinning studies in partnership with Aptek Industries [22]. Aptek uses a proprietary hot wax formula for mounting wafers and die to stainless steel grinding plates. The use of wax as an adhesive offers greater flexibility for handling thinner parts as well as eliminating the effects of ESD damage. The back-thinning is performed by a wet grind process with a rust inhibitor for cooling the chips and keeping the grind wheel free of debris which could cause damage when thinning below 100 μm. The process allows accurate thickness measurements in-situ. After the grinding a polish process is performed which minimises the stress from the backside of the device and allows to achieve thicknesses below 50 μm. Yields are dependent on various factors related to the quality of the silicon, including where in the ingot the wafers are taken from. Over twenty-five MIMOSA-5 chips, designed by the IReS, Strasbourg group and produced in AMS 0.6 μm CMOS process have been

Table 3: Summary of the results on back-thinned chip tests, given as average percentage changes of signal pulse heights after and before back-thinning, quoted uncertainties are the r.m.s. values of the results for the different sectors of the chip. (from Ref. [14])

Thickness (μm)	**Noise**	**^{55}Fe**	**850 nm**	**1060 nm**	**1.5 GeV e^-**
50	(+3±7)%	(-7±8)%	(-16±6)%	(-16±10)%	(-9±7)%
39	(+8±13)%	(+2±2)%	(-10±6)%	(+130±42)%	(+2±4)%

back-thinned by Aptek. The overall yield is 90 %. Four chips have been characterised, back-thinned and re-characterised as part of our study [14]. Three have been thinned down to 50 μm while a fourth sensor has been thinned to 39 μm. At this thickness, chipping of the sensor edges was observed and the process was stopped. Results of the tests carried out with ^{55}Fe, collimated IR laser beams and 1.5 GeV e^-s are summarised in Table 3. These results confirm that neither the charge collection nor the signal-over-noise ratio performance for energetic particles of CMOS pixel sensors are affected by the back-thinning process down to thicknesses below 50 μm.

After having assessed the reliability of CMOS monolithic pixel back-thinning to 50 μm, a program was started to design a ladder to support the thin sensors, which starts from the STAR HFT design (see below) and meets the ILC requirements. The limited (and declining) LCRD funding which has been made available to this program in the past two FYs has significantly slowed down the progress in this area.

Several designs have been considered. These take into account the data collected on the distortions and mechanical stress of a 50 μm thin CMOS chip (see Figure 10), on airflow cooling of a detector ladder and on ladder vibrations.

An interesting concept, which has emerged as a leading candidate for prototyping, is the so-called cool core ladder (see Figure 11). In the cool core ladder a carbon foam layer with pixel chips mounted at both sides is a sandwich structure that acts both as mechanical support and as a guide for the airflow cooling. This design offers the appealing opportunity to place thin chips back-to-back on the same carrier, thus reducing the material budget per active layer or increasing the number of measurements. A possible arrangements of the ladders in the barrel section of the Vertex Tracker is shown in Figure 11. The optimisation of this geometry now requires detailed simulation, which is currently starting, and prototyping.

The cool core ladder concept incorporates several potential improvements over ex-

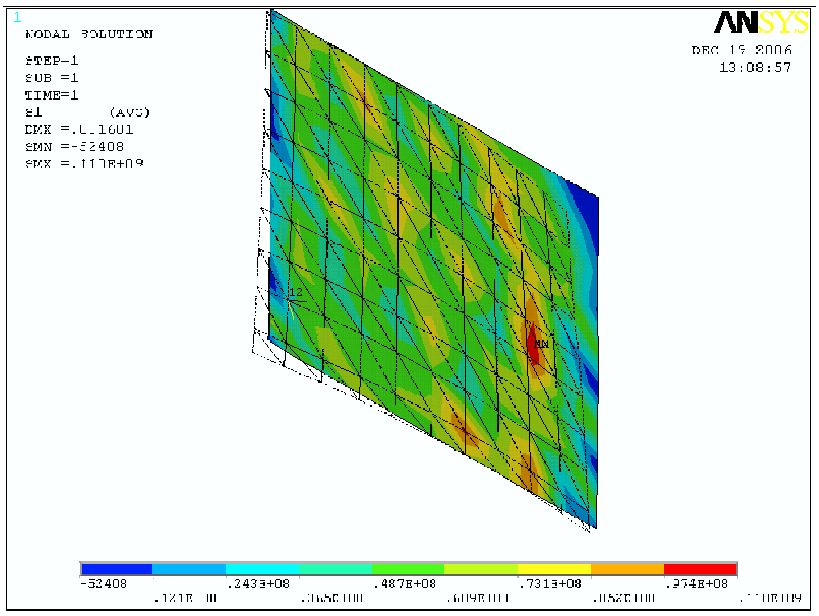

Figure 10: FEA study of the stress of a flattened 50 μm thin pixel sensor based on the measurements of the shape of a free standing chip.

isting ladder designs. First the structure is completely symmetric about the two longitudinal midplanes; this eliminates ladder bending, which is the major source of pixel displacement, in response to uniform temperature changes. By using the detector chips as facesheets in a sandwich structure further material reduction is obtained. The design meets the 0.1 % X_0 per layer requirement. Pixel layers are grouped in pairs, with no significant relative movement between them, giving additional information on any overall distortion of the ladder. The thicker core reduces bending from thermal variations between the top and bottom detector chip layers. The design also allows air cooling to be delivered through the RVC (reticulated vitreous carbon foam) core, potentially improving the overall heat transfer, reducing detector temperature, air flow requirements and large scale air turbulence associated with external air cooling. The feasibility and potential performance of this through-core cooling concept have been analysed. In this concept, a channel is cut longitudinally through the middle of the core in such a manner as to form an air-feed manifold while still providing sufficient support to the facesheets. Air is fed into the manifold from both ends of the ladder and then flows transversely out through the RVC foam, cooling the underside of the detector chips. The air then flows longitudinally in between the ladders, in both directions, to the ends of the ladder, providing some additional convective cooling. The RVC foam both induces small scale

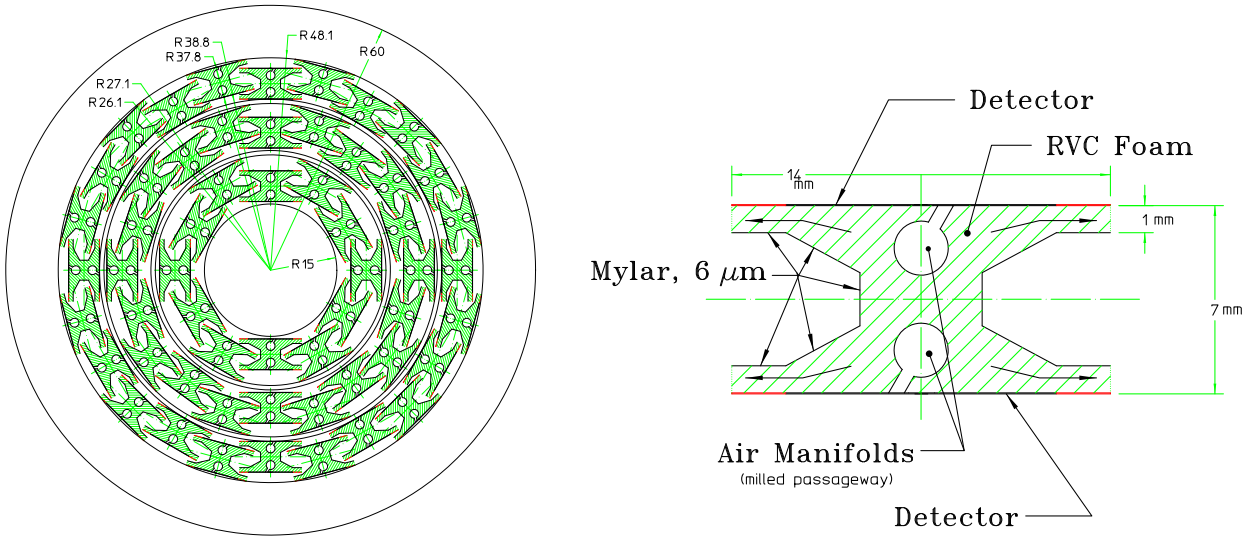

Figure 11: Vertex Tracker concept based on the core cool ladder (right). Cross section of the core cool ladder concept (left).

air turbulence and acts as a network of fins, substantially improving the effective areal heat transfer coefficient. Further, graphitic carbon foams have recently been obtained which offer low densities (0.2-0.6 g/cc) and high thermal conductivity (40-180 W/m K) which may be more effective than RVC for thermal management [23]. A flow equalizer in the manifold is needed to assure uniform transverse flow.

Previous experience in the assembly and test of the mechanical and thermal properties of low mass ladder prototypes has been gained by the corresponding developments for the STAR HFT upgrade project. A low mass ladder prototype has been developed by the LBNL STAR group, achieving a total material budget below 0.3 % X_0. The carrier consists of a sandwich of 3.2 mm thick RVC foam in-between two 50 μm thin layers of CFC. A cable assembly made of four layers of 25 μm kapton and 20 μm Al or Cu conductor is glued with film adhesive on top of the carrier. The cable assembly is used to drive the sensor power lines and analog outputs allowing on-ladder functionality tests. Several 50 μm thin MIMOSA-5 chips have been positioned on top of the cable assembly and glued to it also by means of film adhesive. The chips have been positioned using a custom-made vacuum chuck with an alignment bump edge and individual vacuum valves. Up to eight chips have been mounted on the ladder using this technique. Measurements of the chip positions have been performed with an optical survey machine. The chip corner positions were found to be accurate to 20 μm. A study of the chip elevation profile

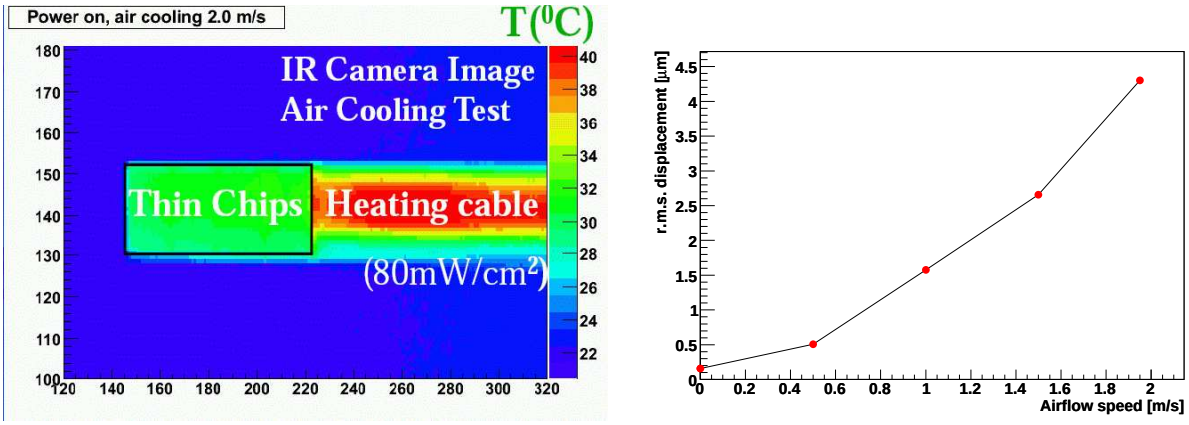

Figure 12: Cooling tests of prototype ladder. (Left) Temperature map of a prototype ladder equipped with 50 μm-thin CMOS pixel sensors under a laminar airflow of 2.0 m s^{-1}. (Right) R.m.s. of ladder displacement vs. airflow speed measured for a ladder prototype supported only at one end.

along the carrier showed that the chips were flat within 30 μm.

The ladder prototype is supported only at one end, consistently with the side-mount foreseen in the STAR HFT upgrade. Studies of ladder vibrations have been performed using a capacitive probe with sub-μm resolution for position measurement and a bandwidth of 1 kHz, above the typical resonant frequencies of ladders. The displacement of the unsupported ladder end has been measured as a function of time and the fundamental resonance frequency has been extracted from the FFT of the oscillations. The measured value of 139.2 Hz agrees well with the expected value of 135 Hz.

Studies of heat removal using low speed, quasi-laminar air flow have been performed by placing the ladder assembly in a wind tunnel box where air was flown onto the ladder surface by a fan placed at an angle with respect to it. An air speed measurement device was placed close to the unsupported end of the ladder. The ladder assembly used for these tests included a kapton heater cable between the ladder beam and the four 50 μm thin MIMOSA chips mounted on top of it, so that power could be provided to different areas of the silicon in order to more closely mock up different heat loads from pixel and digital processing parts of the chips. A power density of 80 mW cm^{-2} was provided, and thermal images for different speeds of the air flow were taken by means of an infrared camera, so that the temperature on different points of the ladder surface could be monitored. Figure 12 shows an example temperature map taken for a speed of the laminar flow of 2.0 m s^{-1}, with the fan placed at an angle of 3 degrees with respect to the ladder.

One can observe that the silicon temperature remains within 1 °C over the surface of all the chips. An average temperature of 30.4 C was measured at the silicon surface, 9 °C higher than the 21 °C ambient temperature. During a preliminary set of these test, the vibrations induced by the air flow were also measured by means of a capacitive probe. At the unsupported end of the ladder, with the fan placed at a 10 degree angle with respect to it, the r.m.s. displacement induced by the airflow was measured to be 1.6 μm for an air speed of 1.0 m s^{-1}, to be compared with the 0.16 μm r.m.s. displacement measured in absence of airflow. For increasing airflow speeds, the free end of the ladder bent away from the capacitive probe and the magnitude of the vibrations induced by the airflow increased, up to a r.m.s. displacement of 4.3 μm for an air speed of 2 m s^{-1} (see Figure 12). The fourth area where relevant activities have been deployed is that of power distribution. R&D to address this problem in the context of ATLAS upgrades has already been gathering momentum over the past two years. Development of a standard, radiation hard, magnetic field compatible, low mass, DC-DC converter which can be used as an off-the-shelf component has the potential for widest applicability across future detectors, including the ILC Vertex Tracker. LBNL has been leading this effort in the area of capacitive charge pump converters, which are naturally magnetic field compatible and compact. A first proof of principle prototype of a switched capacitor DC-DC converter has been designed at LBNL, produced in the AMS 50 V 0.35 μm HV-CMOS process and tested. A second prototype, intended to be usable in test applications, is currently in fabrication in the same process and it is expected back from the foundry in late Fall 2007.

3.4.2 Future Work

WP-4 should extend in parallel with the sensor R&D and provide prototype support structures for characterisation. LBNL is very well equipped both for carbon composite structure fabrication and their characterisation. In year 1 we would like to acquire and characterise RVC samples with high thermal conductivity and build a prototype ladder based on the cool core concept, equipped with dummy 50 μm thin silicon chips and heating cable. This prototype will enable us to perform extensive studies of the ladder stability under thermal and humidity cycling, airflow induced vibrations and gravitational sagging. These tests can be performed with the equipment available to our group, ensuring a very cost effective activity. In year 2 possible revisions of the project will be applied, based on the data acquired. A prototype ladder could be equipped with active thin CMOS pixels, possibly using the same chips adopted for the STAR HFT and the

functional ladder would be characterised in a beam test. A mock-up of the vertex tracker will be built to allow a study of heat removal and vibrations in a realistic environment. The mock-up will consist of Aluminium-lined carbon composite dummy ladders which can be individually replaced with real prototypes and a system of capacitive probes allows to monitor deformation. In year 3 an advanced prototype ladder should be available to be equipped with the sensors resulted by the WP-2 development. These modules would be the basis of the tracker prototype, discussed as WP-5 in the next sub-section, which will be assembled in year 4 after completing the development of reticle size sensors with data sparsification. In parallel, we propose to strengthen and expand the DC-DC converter design and prototyping effort in order to produce additional devices and consider their applicability beyond ATLAS. In particular, the possibility of pulsed power operation mode for the ILC Vertex Tracker introduces special considerations, which need to be addressed by a dedicated design. This work can be most effectively carried out in conjunction with the ATLAS SLHC R&D effort, which is at present centred at LBNL. DC-DC converter would be installed and evaluated on module prototypes. This part of WP-4, which is not currently covered by our estimated funding, should be seriously considered for funding opportunities, aimed at promoting coherent instrumentation efforts for SLHC and ILC.

3.5 WP-5: Development of Vertex Tracker Prototype

WP-5 covers the design, prototyping and deployment of a Vertex Tracker Demonstrator, based on reticle size monolithic pixel chips, matching the ILC requirements in terms of single point resolution, readout speed and power dissipation, mounted on a light- weight mechanical support, scalable to a full ladder, and equipped with power distribution and heat management systems. We would like to assemble at least four of these structures in a beam telescope with a geometry compatible with that of a Vertex Tracker at the ILC. Its performance should be validated on both a high energy beam, such as the Fermilab MTest 120 GeV proton beam, and a lower energy beam, such as the ALS 1.5 GeV or the LOASIS 1 GeV e^- beam, in terms of track extrapolation resolution to a reference plane located 15 mm upstream from the tracker prototype, corresponding to the extrapolation to the ILC beam collision point.

3.5.1 Recent Progress

In the last year our group has pionereed the design, assembly and test of prototype trackers based on thin CMOS pixels sensors. Two beam telescopes have been designed,

assembled and operated. The first system (TPPT-1) has been the first beam telescope made of thinned CMOS sensors. It consists of three planes of thin pixel sensors, each spaced by 17 mm with a fourth layer made by a full-thickness detector. The TPPT-1 was designed for tracking low-momentum particles and took data in Fall 2006 at the ALS with 1.5 GeV e^-s (see Figure 13), at different beam intensities ranging from 0.5 particles mm^{-2} up to about 5 particles mm^{-2}. After data taking, the beam telescope geometry has been surveyed using an optical metrology machine. The results of this survey have been used as starting point of the alignment procedure, performed on a sample of approximately 20000 well-isolated particle tracks with four correlated hits. The extrapolation resolution of the TPPT-1 on the first telescope plane, located 17 mm upstream, has been measured to be 9.4 μm (see Figure 14) [14, 18]. This result matches the ILC performance requirements in this low momentum region. An improved version, the TPPT-2, was designed for the T966 beam test experiment at Fermilab. The TPPT-2 consists of four layers of 50 μm-thin MIMOSA-5 sensors mounted on new mezzanine cards with low profile components and larger clear areas in the PC board below chip. The four layers are mounted using precision mechanics and are spaced by 15 mm. The chips have been positioned on the mezzanine boards using a precision vacuum chuck which ensures a mounting accuracy better than 50 μm. Downstream from the TPPT-2, a detector under test (DUT) can be mounted on a computer-controlled XY stage which allows to remotely align it to the telescope. The DUT spacing from the TPPT-2 can be varied from 5 mm to 20 mm. The TPPT-2 has been tested first in May 2007 on a 1.23 GeV e^- beam extracted from the ALS. The TPPT-2 operated at Fermilab MTest with 120 GeV protons in June and July 2007 (see Figure 13). The system was operated at $\simeq$ 20°C by forced flow of cold air. The data analysis is still in progress. Due to a significant day-night effect in temperature change, the software alignment is performed separately for each day. The first result, obtained with a preliminary alignment, is shown in Figure 14; the distribution gives a residual resolution of 5.7 μm. We expect the results from the analysis of the first run of T966 to be finalised by early 2008.

3.5.2 Future Work

The next step of development of the thin pixel beam telescope is a replacement of the readout and cooling systems, in order to improve the S/N ratio and reduce the integration time. In the current FY we shall deploy a new readout system based on a commercial FPGA development board, equipped with the Virtex 5 chip, and a custom ADC card, developed by the Padova group. The new system is currently under test and has lower

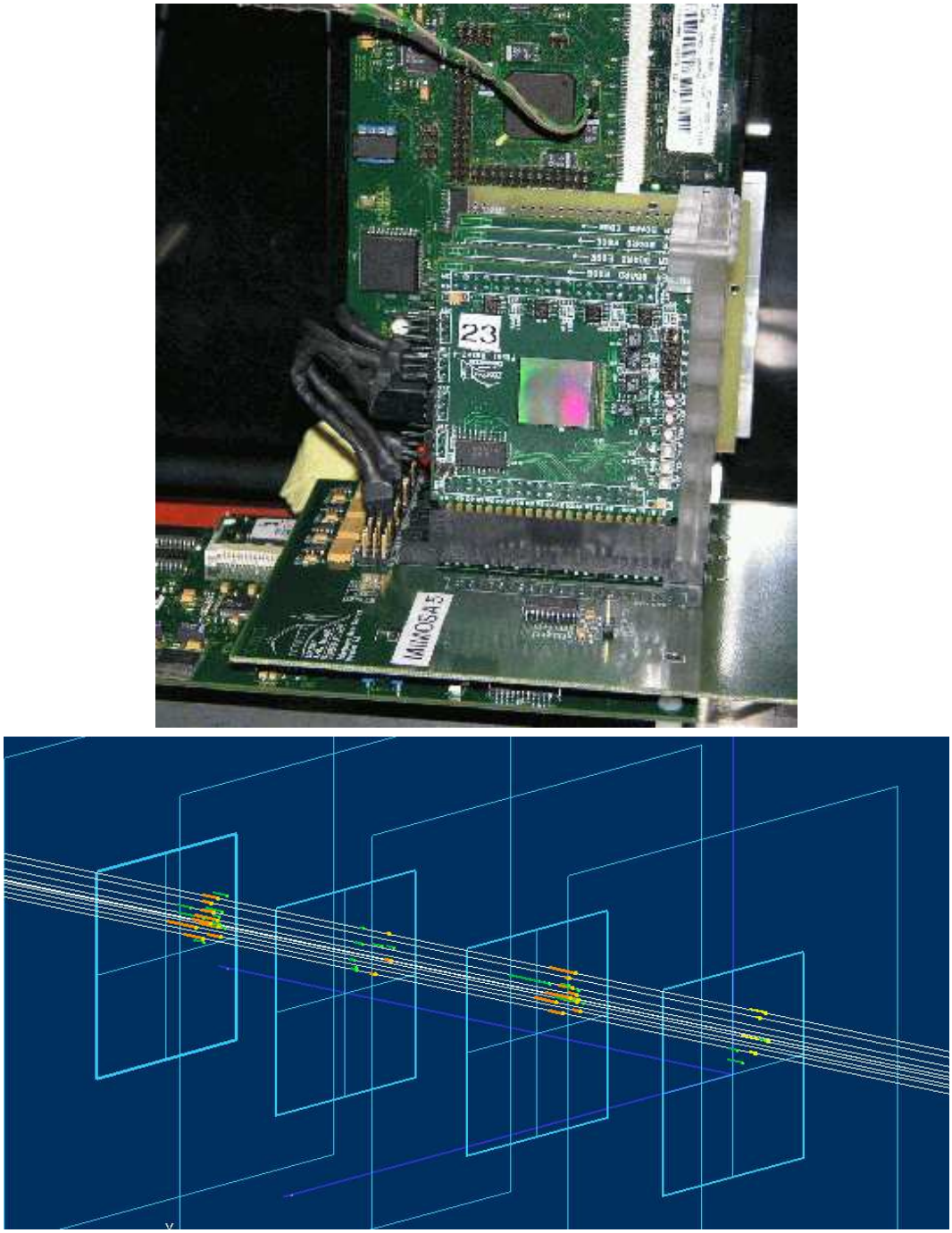

Figure 13: The Thin Pixel Prototype Telescope: (Top) TPPT-2 before installation in the MTest area at Fermilab in Summer 2007 and (Bottom) Display of an event recorded on the ALS beamline in Fall 2006.

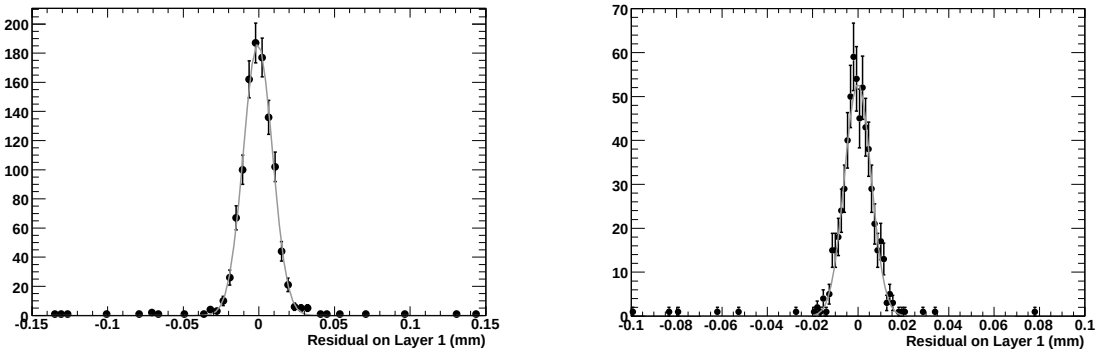

Figure 14: Distribution of residuals between the track extrapolation in the vertical coordinate and the reconstructed hit position on the first detector layer upstream from the telescope. Left: TPPT-1 performance for 1.5 GeV electrons at LBNL ALS. Right: TPPT-2 performance for 120 GeV protons in T966 at FNAL MTest.

noise and larger bandwidth. This will allow to clock the MIMOSA-5 chips in the telescope at 10 MHz, thus reducing the integration time. A second development is the design and construction of a telescope enclosure with a light-weight cryostat, to operate the telescope at temperatures of $\simeq$ 5-10°C. This will allow us to achieve a S/N ratio better than 20. We plan to operate the TPPT-2 with the new DAQ and cooling system at the ALS and then again at MTest in Summer 2008 for the second data taking of T966.

A second project, which should be developed in the course of the current FY, is the addition of a plane of thin MIMOSA-5 pixels to the pixel telescope, based on the BTeV hybrid pixels, currently being setup on the MTest beamline. The inclusion of a single high resolution point, provided by the thin MIMOSA-5 chip, in front of the detector under test will allow to improve the extrapolation resolution from $\simeq$ 10 μm to a few microns. We plan to use here the same readout electronics being developed for the new DAQ system of T966.

The TPPT-2 should remain available for several years for the characterisation of new detectors both at the ALS and in T966. At the same time we shall be considering developing a new tracker prototype using a chip with performances closer to the ILC requirements, in particular in terms of readout speed. If the LDRD series chips perform according to expectations, we shall consider the production of a scaled-up version with at least 1×1 cm^2 active surface, possibly in year 2 by adopting the LDRD-3+. After back-thinning this chip will be an excellent candidate for a new telescope to replace the TPPT-2 by the end of 2010. At that time a ladder design will have emerged from

the design, prototype and test effort. The new telescope (TPPT-3) could be based on chips glued not on PC boards but on carbon composite structures, using a kapton for the interconnects similarly to the solution successfully adopted in the STAR HFT. The TPPT-3 will allow us to test tracking and vertexing performances on low and high momentum beams with a setup closely resembling a section of the multilayered barrel part of the Vertex Tracker. This will not only be important for a system test and for assessing the extrapolation resolution, but also for studies of stability and alignment using particle tracks. Finally the Vertex Tracker Demonstrator should be based on a reticle size chip with functionalities and performances matching the ILC requirements as it will emerge from the activity of WP-2. These chips would be mounted on the carbon composite ladders developed under WP-4. The resulting multi-layered tracker should allow detailed system tests and performance assessment on the time scale of interest for the detector concepts to make an informed choice of the technology and architecture for the Vertex Tracker.

3.6 WP-6: Tracking and Vertexing for the ILC: simulation, reconstruction and validation

WP-6 aims at developing a program of simulation, reconstruction and validation with beam test data for standalone pattern recognition, track reconstruction and vertex fit.

3.6.1 Recent Progress

The analysis of the TPPT-1 data at the ALS and of the T966 data already offers possibly the most realistic results on tracking with thin pixel detectors with a geometry and occupancy level closely resembling that expected at the ILC. Since the integration time for both the TPPT-1 and the TPPT-2 are long, each beam test data records hits from multiple tracks: about 2 to 10 in T966 and up to 50 at the ALS. Additional hits originate from secondary, low momentum particles and noise. The resulting track density is comparable to those expected in the core of collimated hadronic jets at the ILC. Figure 15 shows the closest distance between the hit associated to a reconstructed track and any other hit on the same detector layer for simulated Higgs decays at the ILC and the ALS data. The intensity of the ALS booster beam can be tuned to reproduce quite closely track densities characteristics of various physics processes. The extrapolation resolution measured for 1.5 GeV e^-s has been studied separately for runs taken at different intensities. Up to 3 particles mm^{-2} no significant increase of mis-measured tracks has been observed. Unfolding the detector resolution, the extrapolation accuracy measured

at the ALS for 1.5 GeV particle tracks with the TPPT-1 matches the ILC requirements (see Figure 16). The T966 beam test experiment devoted a fraction of the beam time to data taking with a 4 mm-thick copper target placed 25 mm upstream from the telescope. These data will allow to perform vertex search for events with proton interactions in the target and to obtain interesting information on vertex finding efficiency and vertex resolution and compare them with Monte Carlo simulation.

3.6.2 Future Work

We plan to develop WP-6 over the next three years. In year 1 the T966 telescope data will be fully analysed. These data will provide results on tracking resolution for high momentum protons and vertexing resolution for p-Cu interactions. In year 2 the data from the second T966 data taking, planned in Summer 2008, will be analysed. We intend to improve the T966 setup by including one MWPC plane upstream and at least two planes downstream from the TPPT-2 in the data stream. The MWPC data will allow to independently validate the particle tracks reconstructed in the TPPT and to use these track elements as seeds for the track search in the silicon planes, similar to what would be done in an ILC detector. The readout of the TPPT at higher frequency will reduce the number of protons recorded in a single events, thus allowing to operate at larger number of particles/spill and acquire higher statistics for the p-Cu interaction events. We also intend to study the effect of pair background in track pattern recognition and reconstruction. First we plan to generate libraries of clusters produced by low energy

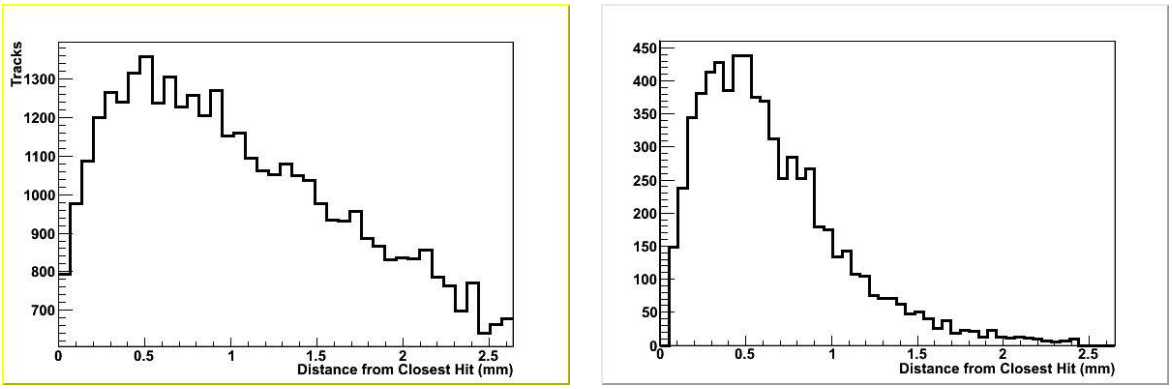

Figure 15: Distribution of closest distance between a hit associated to a reconstructed particle track and any other reconstructed hit for $e^+e^- \rightarrow Z^0H^0 \rightarrow \mu^+\mu^- b\bar{b}$ at $\sqrt{s} =$ 0.5 TeV (left) and 1.5 GeV e^-s at the ALS in one run of the first TPPT-1 beam test (right).

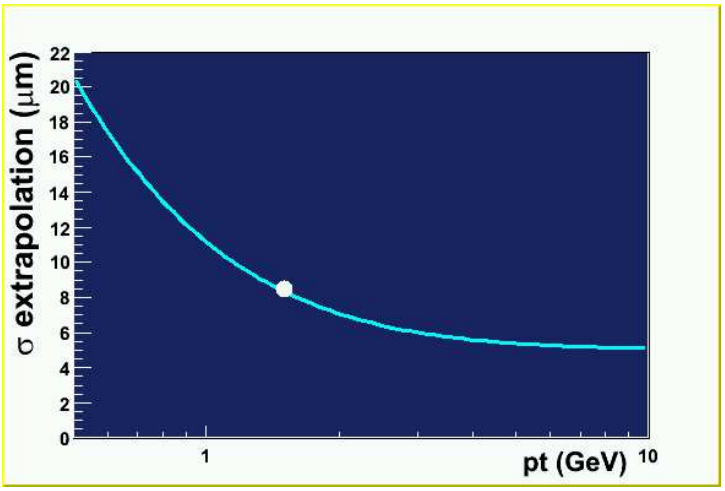

Figure 16: Track extrapolation resolution to the beam collision point obtained for simulated events with a CMOS Vertex Tracker at the ILC as a function of the particle momentum (shown by the line) compared to the extrapolation resolution measured with TPPT-1 on the ALS beam (shown by the dot).

electrons incident at small dip angle on the detector plane. These data can be collected at the ALS using an Al beam scraper. Low energy e^- clusters can be mixed to the T966 data, using the same procedure used for overlaying pair background to ILC events in simulation. The resulting overlapped events will make a very realistic environment for assessing the impact of pair background at varying densities on the ILC tracking accuracy.

The availibility of realistic background descriptions and detailed simulaton will be crucial for a study of the tradeoff between chip active area and complexity implemented on chip and between number of pixels in a column and readout speed. More complex functionalites require larger surfaces, which increase the amount of inactive silicon on the ladder. On the other hand wider ladders will be limited in readout time, thus increasing the integrated background. The problem has many parameters and the optimisation requires detailed studies both in simulation and on prototype chips. We intend to carry out these tests using `Geant-4` simulation and the simulation and reconstruction processors validated using beam test data, to guide the optimisation of the chip design. In year 3 tracking studies will be repeated on the data collected with the TPPT-3 tracker. In addition, we shall develop dedicated Kalman-filter processors for both track and vertex reconstruction, optimised and validated for treating low momentum particles.

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Summary of R&D Activities per Year

WP	FY08	FY09	FY10	FY11
WP-1	Reco Tuning Bkg Studies HA, $b\bar{b}$, $c\bar{c}$	 $HH\nu\nu$, $\tilde{\tau}\tilde{\tau}$	Implement new performances Alignment Review Physics	
WP-2	LDRD-3: ADCs, Fast r/o LDRD-2 Rad Hard Study 0 suppression	LDRD-4: 0 Suppression LDRD-3+: 1 cm^2 active area Test CMOS processes	LDRD-5: data sparsification	LDRD-5+: reticle size
WP-3	SOI-2: OKI 0.2μm Low leakage study back-gating test rad hardness	SOI-3: binary study time stamping	SOI-4: time stamping	
WP-4	characterise RVC Prototype Dummy Si DC-DC converter	Backthinning Prototype w/ active Pixels Test DC-DC converter	Ladder w/ LDRD3+	Tracker Ladders
WP-5	TPPT-2 w/ New DAQ Thin MIMOSA in FNAL Telescope T-966 w/ LDRD-3, SOI-1	Light Cryostat T966 w/ LDRD-4, SOI-2	TPPT-3	Demonstrator Tracker
WP-6	T966 data analysis Bkg Cluster Library Optimise chip design	T966 data analysis Bkg studies Optimise ladder design	T966 data Analysis Trk & Vtx KF Fit	T966 data analysis