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Planar LTCC Transformers for High Voltage Flyback Converters Part II

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Abstract

This paper is a continuation of the work presented in SAND2007-2591 "Planar LTCC Transformers for High Voltage Flyback Converters." The designs in that SAND report were all based on a ferrite tape/dielectric paste system originally developed by NASCENTechnoloy, Inc, who collaborated in the design and manufacturing of the planar LTCC flyback converters. The output/volume requirements were targeted to DoD application for hard target/mini fuzing at around 1500 V for reasonable primary peak currents. High voltages could be obtained but with considerable higher current. Work had begun on higher voltage systems and is where this report begins. Limits in material properties and processing capabilities show that the state-of-the-art has limited our practical output voltage from such a small part volume. In other words, the technology is currently limited within the allowable funding and interest.

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1. Introduction

The most cost efficient high voltage supply for capacitive discharge applications for miniature and/or ruggedized use is the flyback converter. The converter's applications range from military to civilian fuzing for high explosives to oil exploration, respectively. These systems usually are powered from a voltage source under 50 V and require an output greater than 1 kV. The flyback converter's draw is the low part count, thus increasing reliability and minimized circuit volume. However, in all configurations, the transformer has been themost expensive part and also most prone to failure due to its many parts: core, coil, pins , bobbin, solder joints and the often fine gsuges of wire used. The introduction in 1997 of a planar LTCC transformer and the follow on of a high voltage flyback LTCC transformer in 2003 has drastically increased the reliability and minimized the volume for certain applications [1,2]. This work on high voltage flyback planar LTCC transformers was started as a collaborative effort between Sandia National Laboratories and NASCENTechnology, Inc. (formerly Midcom, Inc.) in 2003. This earlier work studied the design space and the driving factors for efficient high voltage output [3]. Transformers that could readily output 2.5 kV were manufactured that would easily meet 1.5 kV charge requirements for CDU applications. However, applications requiring higher than 3 kV could not reliably use existing designs.

This paper discusses an alternate design approach for low-temperature (850°C to 950°C) co-fired ceramic (LTCC) transformers for use in greater than 3 kV flyback converter systems. Modeling explaining the reason behind this approach will first be explained. Material properties and processing studies will be discussed. Finally, data on this new LTCC planar transformer system, called the dielectric ring-coil transformer, will be presented.

1.1. Flyback Converter Fundamentals

The flyback converter is very different in operation to the other class of converters known as forward converters (simple schematics shown in figure 1). Forward converters allow current flow when the switching element is on, so that energy is allowed to continuously flow from the primary to the secondary of the transformer, by a well-known physics principle called Lenz's Law. As current flows through the primary, current must flow through the secondary to balance the energy in the transformer. This also limits the voltage on the output by the transformer

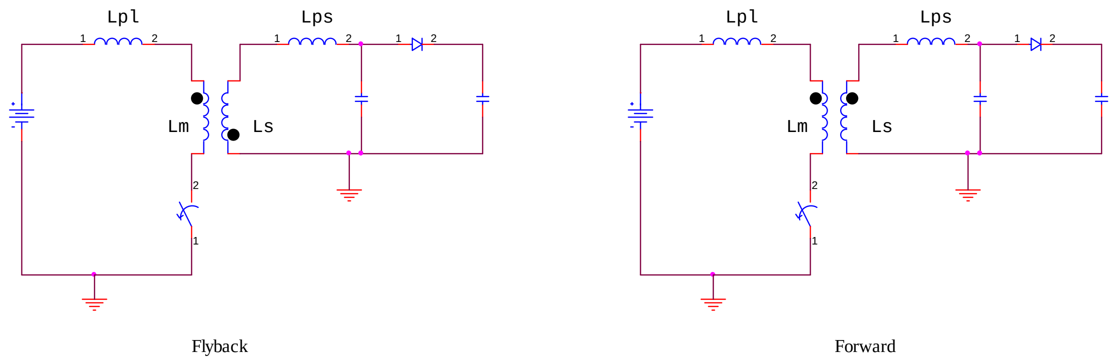
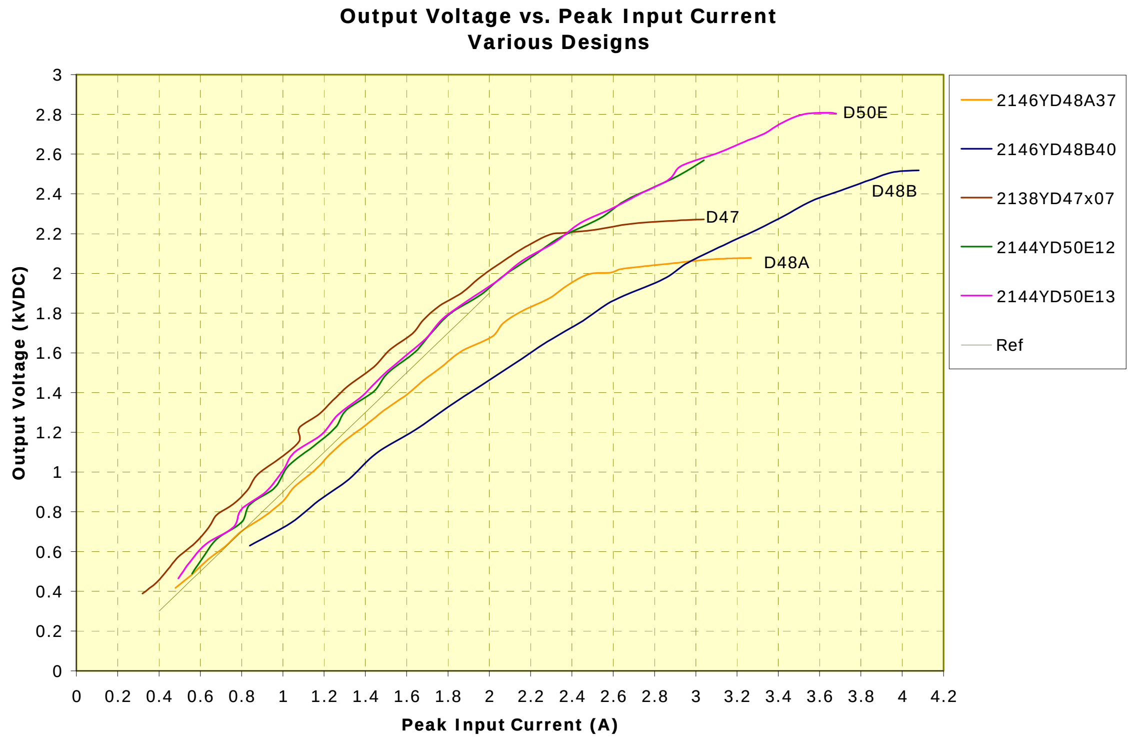


Figure 1. Flyback and forward converters.

turns ratio. The flyback converter topology, in contrast, does not permit current to flow through the secondary while current flows through the primary by way of winding polarity and a high voltage diode. The result is the transformer acts as a simple inductor and stores the energy. When the switch opens, the current that was flowing through the primary must continue to flow since current cannot switch instantaneously as this would result in an infinite voltage spike. The result is that the voltage polarity switches direction in both windings allowing current to flow out the secondary through the high voltage diode, that is, energy is released. The advantage of the flyback is that the output is not related to the turns ratio but to the energy transferred. The energy transferred to the secondary will induce a voltage to ensure that the current flows to transfer the energy out of the transformer. This results in potentially very high voltage spikes. The major factor that limits this output voltage spike is the secondary winding capacitance. A more detailed analysis of flyback converters is in Roesler et al. [3].

1.2. Previous LTCC Work

Previous work by Roesler et al. [3] led to a highly optimized design for LTCC planar flyback transformer with a size up to 0.36” x 0.36” x 0.1”, such as the D50E LTCC transformer. Parameters such as winding strategy, gap structure and location, end margin distance and end cap thickness were all investigated. All of these parameters affect the reluctance path for the flux just as in traditional wire wound transformer technology. A summary of the high voltage capabilities is shown in figure 2. The high voltage capability for a given input energy (current) was increased significantly from the earlier D47 and D48 designs (for a given input current).



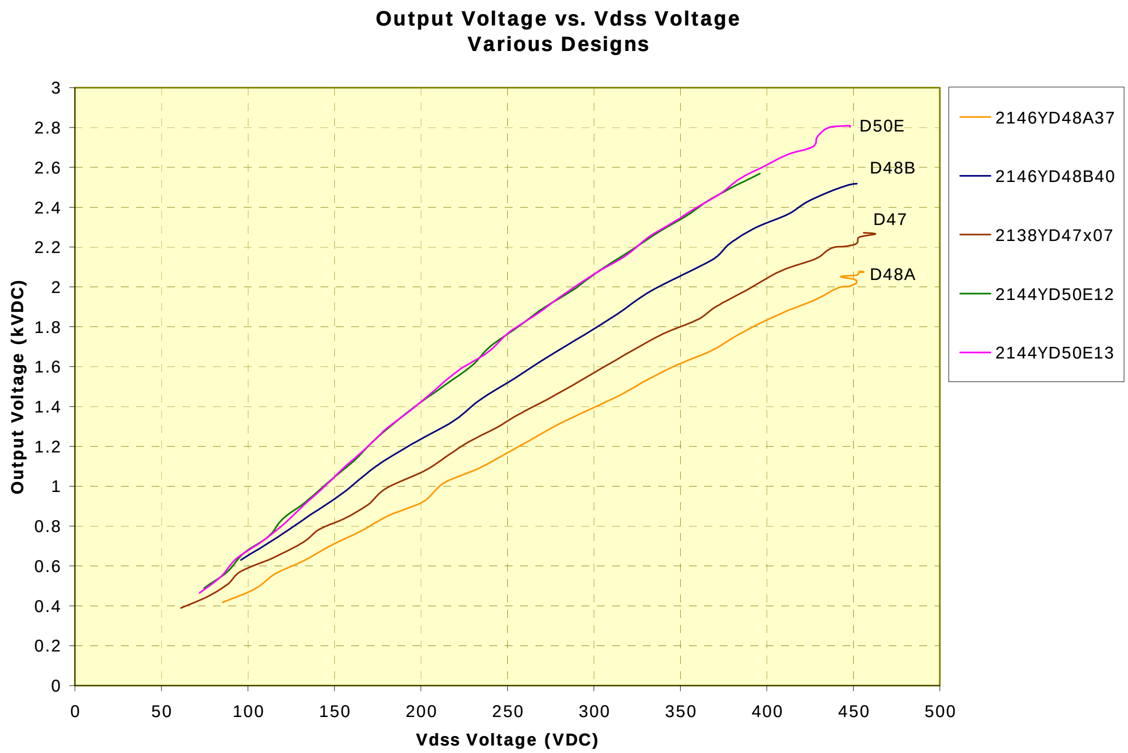


Figure 2. Output comparisons of LTCC transformers from previous work.

Also, the coupling factor was increased as shown by the lower flyback FET voltage stress for a given high voltage output. The test data in figure 2 was limited by the use of a FET with a 450 V breakdown and with the use of a different FET, higher voltage could be possible. However, the data does indicate that the coupling factor is low as compared to traditional wire wound standards. The measured coupling factors are approximately 0.75 to 0.90. This high leakage inductance leads to power conversion inefficiencies and higher voltage stress on the flyback FET. For example, the D50E, which has a turns ratio of eight, gives a voltage stress of 400 V at 2.6 kV of output. If the coupling was perfect (coupling factor of 1), then the voltage stress should be 325 V. The obvious fix to this dilemma would be to increase the turns ratio, however, the volume is limited with the current processing techniques. In addition, as the turn ratio increases, the leakage inductance increases by the square of the turns ratio. If the winding length is increased, the leakage inductance is decreased by decreasing the reluctance of core. This would indicate a thicker part which would reduce the increased leakage inductance due to the turns increase is desireable.

In comparison to the LTCC planar transformers, wire wound transformers usually have coupling factors greater than 0.95. An example of a small wire wound transformer's output is shown in figure 3. For a given input current, the wire wound has a higher output voltage with a lower voltage stress on the FET. This is because of the higher coupling factors (more efficient) and lower Eddy current losses from using higher permeability cores in comparison to the LTCC counterparts. The downside of the wire wound transformer is that its volume is larger, separate pieces and there are solder joints. For the wire wound transformer used in figure 3, the part was approximately 2.25 times larger in volume than an equivalent LTCC transformer. Each design has its unique application and has a tradeoff.

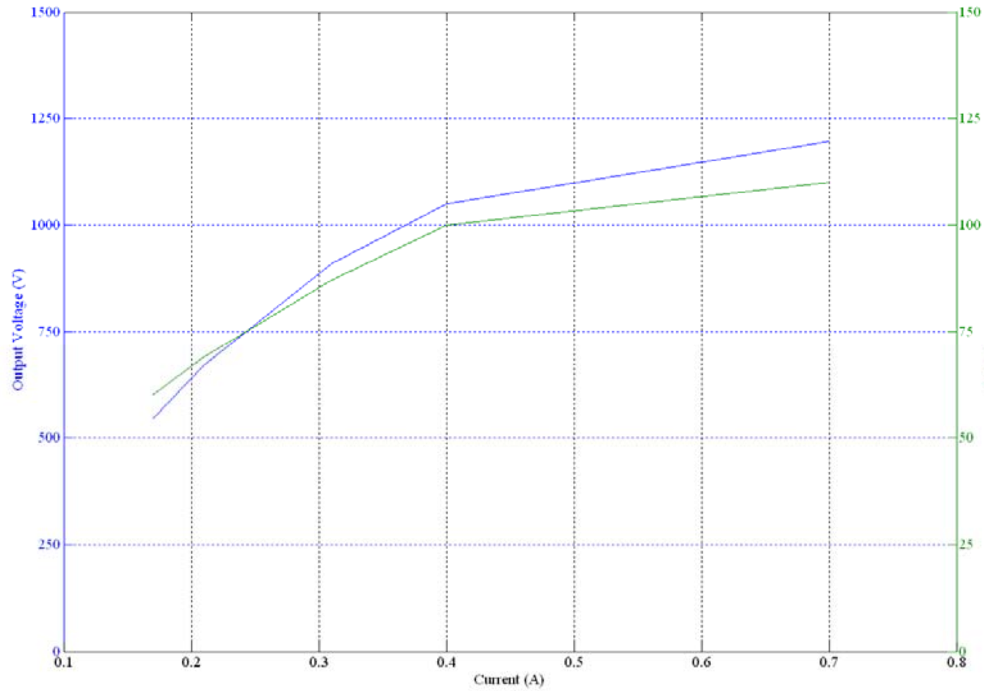


Figure 3. Wire wound transformer outputs

2. D51 – A larger LTCC Transformer

2.1. Group 1

2.1.1. Modeling

One of the most straight forward changes to the LTCC planar transformers in the previous work was to increase the X and Y dimensions so as to increase core area to increase the onset of saturation. This indirectly increases the inductance of the transformer primary thus storing more energy per pulse. Certain applications for a higher voltage could handle a larger transformer (the transformer was not limiting). For instance, the size that would work for a particular 3 kV fuzing application required a capacitor 0.5" x 0.5" in length and width. This was the starting point for a larger transformer called the D51 transformer. The model design parameters for the D51 and D50 and the parameters are shown in table 1 for a comparison. All modeling was done using the 2D solver of Maxwell by Ansoft Corporation (Pittsburgh, PA).

Figure 4 shows the flux density plots for both he D51 and D50 designs. In one variation, the D51 part was made thicker to increase inductance and to reduce core saturation. As can be seen, there is less saturation in the end cap region (above and below the planar coils) with the D51 design. Since a higher inductance is maintained across the input current range, a higher output should be possible.

Table 1. D50E and D51F model parameters.

	D50	**D51**
Primary Width (mils)	12	20
Secondary Width (mils)	4	4
Secondary Pitch (mils)	8	8
Coil Pattern (Sec-Pri-Sec)	4:1:4	4:1:4
Primary-Secondary Spacing (mils)	15	15
Primary Turns (Layers)	16 (16)	16 (16)
Secondary Turns (Layers)	128 (16)	128 (16)
Number of Gaps (mils)	12 (0.5)	12 (0.5)
Part Diameter (mils)	180	250
Part Thickness (mils)	70	98
End cap Thickness (mils)	8	22
End Margin (mils)	21	44

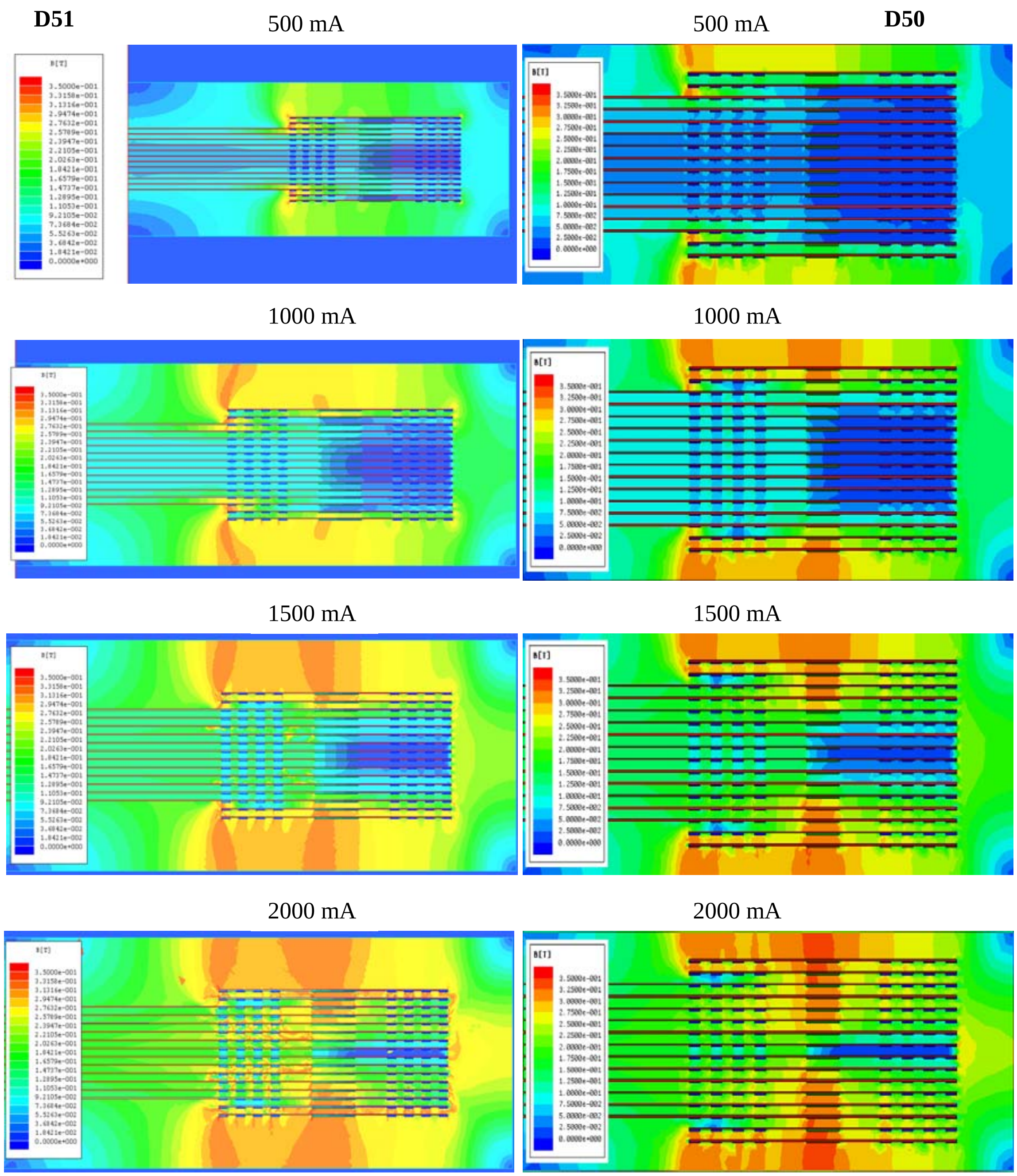


Figure 4. D51 and D50 flux density maps.

The inductance of the two designs is shown in figure 5. The D51 design has a larger inductance across the input current range when compared to the D50 design by about a factor of 2.5. The secondary capacitance will scale by about a factor of 1.5 (average coil circumference difference).

This leads to about a 30% increase in voltage for the D51 design using the relationship $V_{max}=I_p*sqrt(L_p/C_s)$.

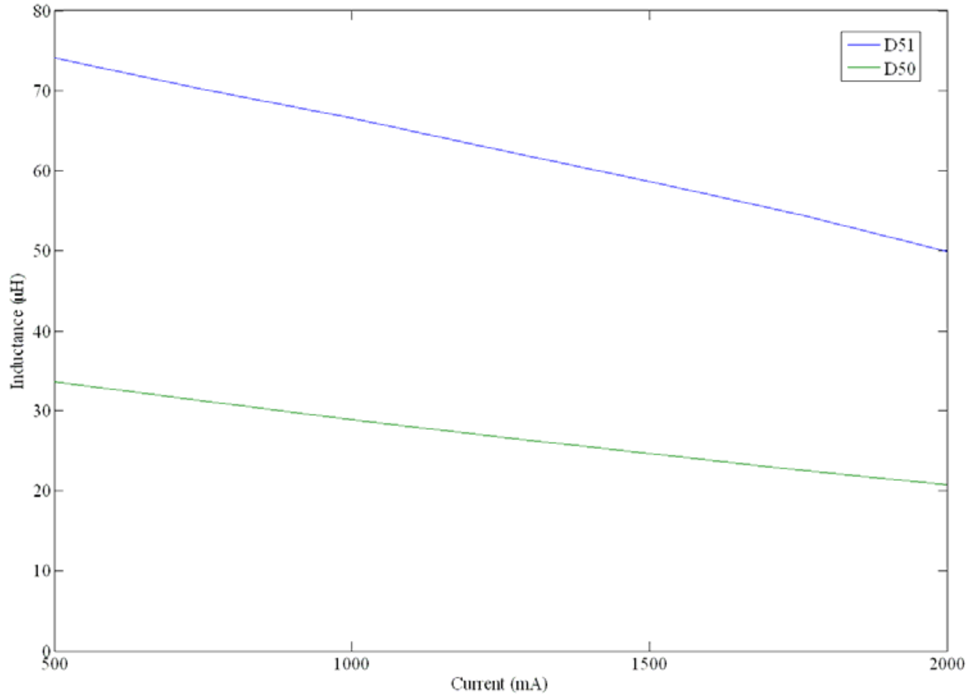


Figure 5. D51 and D50 inductance comparison.

The leakage flux (inductance) can be compared by looking at the flux density through the center of the long axis of the part and is shown in figure 6. According to the plots, the total leakage inductance will be higher for the larger D51 design when driven hard. This will induce a higher voltage stress on the FET during flyback operation since currents approaching 2 Amps are common.

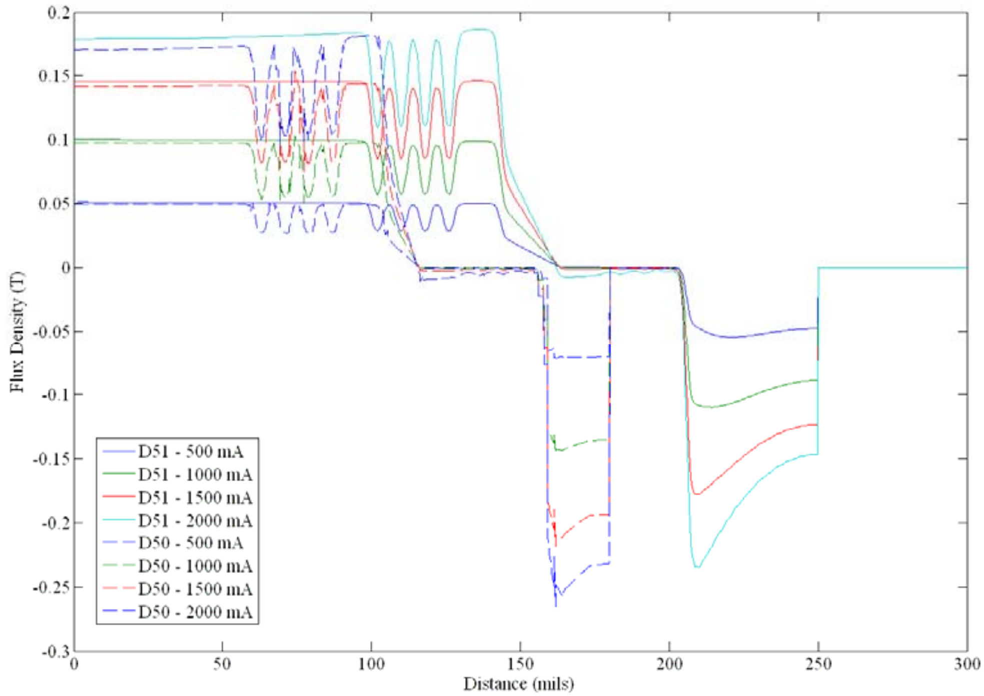


Figure 6. D51 and D50 flux density (leakage inductance) comparison.

2.1.2. Fabrication and Test

This group is considered the baseline group of the D51 design. Its purpose was to make a comparison to the D50E design with only slight modifications to the coil spacing and an increase in the center core area. The first panel of group 1 had an inductance three times higher than expected. Such a higher inductance than desired would allow the transformer to saturate early, i.e. lower currents, reducing the flyback voltage. This led to the addition of a second center gap only print to the standard unigap prints for the rest of the panels. The result was an inductance that was still high but within reason to the estimated value (at about half the value of the first panel). The downside of the center gap only addition was an increase in cracking, especially concentric cracks at the edge of the winding on the top and bottom surfaces. This is most likely due to large pressure variations at the winding edge because of the uneven buildup due to the center gap additions. Pictures of the cracking is shown figure 7. Amazingly, for parts sampled for cross-sectioning, the structure was solid with no voids or internal cracks as shown in figure 8.

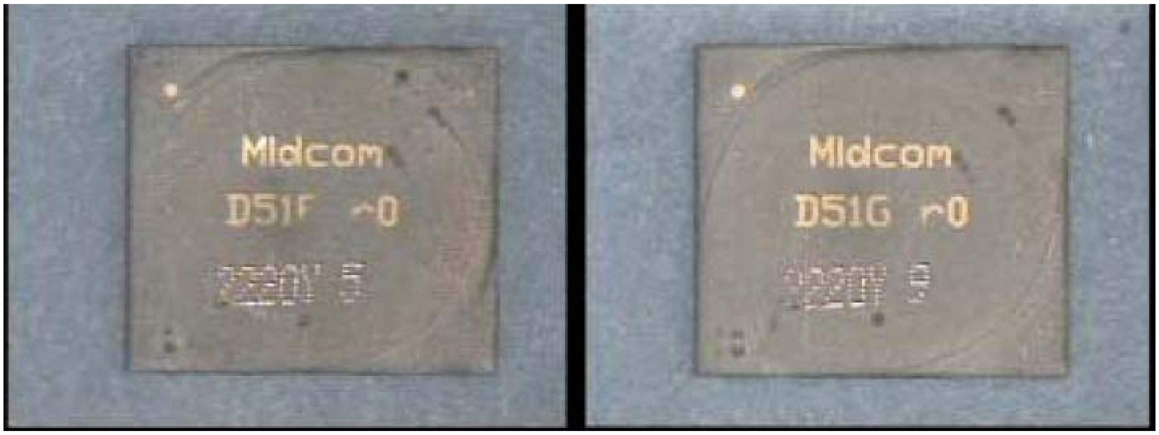


Figure 7. Concentric cracking around the winding edge.

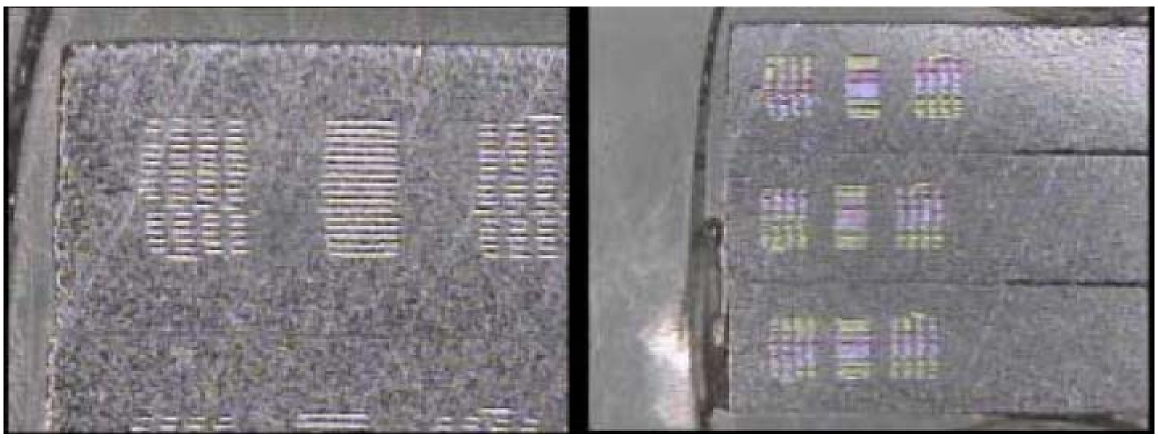


Figure 8. Cross-sections of the D51 transformers.

The rest of the panels of this group had different numbers of layers and/or primary windings to alter turns ratios with similar cracking issues. In addition, there were different coil patterns as listed in table 2 Table 3 lists all the different panels and their averaged measured parameters from panel 2220Y. Obviously, some of the parts had thinner gaps than other resulting in much higher inductances. Others had a large leakage inductance which is indicative of cracking (increase in effective gap length). One would expect all the numbers to be reasonably close and not vastly different. The D51F variant has the highest coupling since the coil window was the shortest because of the tighter primary-to-secondary distance.

Table 2. D51 coil patterns.

Coil Configuration	Primary-Secondary Separation	Inside Secondary-Primary-Outside Secondary Coil Layout
F	15	4-1-4
G	20	4-1-4
H	25	4-1-4
K	15	5-1-3

Table 3. Group 1 builds and measured parameters (averaged).

Build – D51F	**L_p (μH)**	**L_s (mH)**	**L_{lp} (μH)**	**Rp (Ω)**	**Rs (Ω)**	**k**
16W,12G,39L	325.56	18.92	28.60	1.45	56.94	0.96
16W,12G+12CG,39L	145.10	6.16	30.86	1.44	55.81	0.88
20W,16G+12CG,39L	259.98	12.33	63.71	1.73	69.14	0.87
10/20W,16G+12CG,39L	78.50	14.33	28.72	0.97	71.98	0.81
24W,20G+12CG,43L	437.32	21.49	176.40	2.06	86.15	0.80
12/24W,20G+12CG,43L	145.54	22.72	106.07	1.17	86.18	0.78
Build – D51G	**L_p (μH)**	**L_s (mH)**	**L_{lp} (μH)**	**Rp (Ω)**	**Rs (Ω)**	**k**
16W,12G,39L	317.40	17.13	67.47	1.41	54.59	0.89
16W,12G+12CG,39L	168.06	6.84	63.56	1.40	53.94	0.82
20W,16G+12CG,39L	317.30	13.47	166.95	1.68	66.56	0.63
10/20W,16G+12CG,39L	96.14	15.22	62.49	0.95	69.89	0.66
24W,20G+12CG,43L	542.72	23.04	381.53	2.00	82.86	0.61
12/24W,20G+12CG,43L	173.69	22.04	110.94	1.11	82.96	0.61
Build – D51H	**L_p (μH)**	**L_s (mH)**	**L_{lp} (μH)**	**Rp (Ω)**	**Rs (Ω)**	**k**
16W,12G,39L	346.50	16.10	152.22	1.39	53.52	0.75
16W,12G+12CG,39L	208.15	7.70	132.64	1.37	52.75	0.70
20W,16G+12CG,39L	380.07	13.05	244.89	1.64	64.89	0.64
10/20W,16G+12CG,39L	110.88	14.59	79.42	0.93	67.98	0.60
24W,20G+12CG,43L	702.58	22.77	573.90	1.96	80.65	0.48
12/24W,20G+12CG,43L	215.98	25.95	163.53	1.09	80.97	0.50
Build – D51K	**L_p (μH)**	**L_s (mH)**	**L_{lp} (μH)**	**Rp (Ω)**	**Rs (Ω)**	**k**
16W,12G,39L	323.70	18.20	34.78	1.51	55.42	0.94
16W,12G+12CG,39L	123.98	6.24	47.15	1.50	54.55	0.84
20W,16G+12CG,39L	254.20	10.64	62.03	1.80	67.60	0.88
10/20W,16G+12CG,39L	101.90	15.12	39.26	1.04	70.85	0.78
24W,20G+12CG,43L	450.50	17.68	196.05	2.16	84.95	0.76
12/24W,20G+12CG,43L	133.15			1.18		

Note: W=winding layers, G=gaps, CG=center gaps, L=total layers.

The maximum output and voltage stress plots are in figure 9. The thicker parts with 43 layers total all had cracks and high leakage inductance. The coupling was much worse than the previous work. The G variant had a higher voltage output but had a higher voltage stress since it had lower coupling than the F variant. The H variant had similar output to the G variant but its lower coupling factor was apparent in the higher voltage stress. The transformers with half the primary turns produced less output voltage for a given current as is expected (less inductance equals less energy per pulse) and had larger voltage stress. Even though the turns ratio increased by a factor of two, the gain in voltage stress reduction due to increased turns ratio was overshadowed by the increase in leakage inductance. This would only get worse with the increased energy required to make up for the lost input inductance to achieve similarly high output voltages.

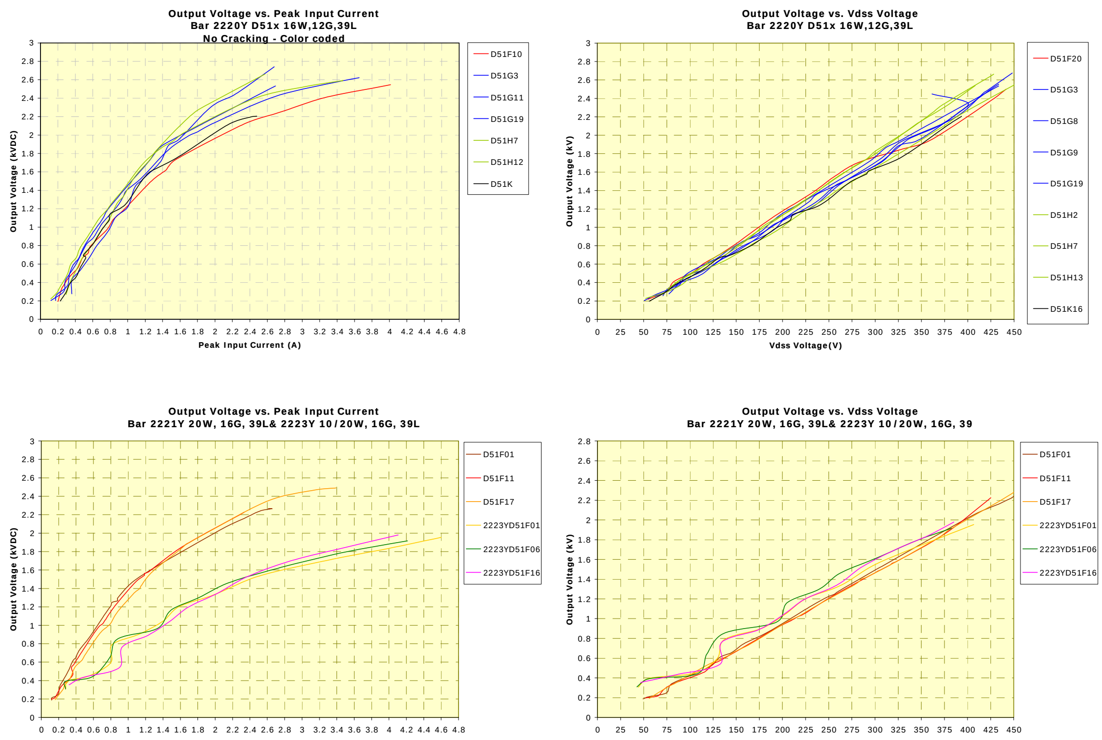


Figure 9. Group 1 performance data.

2.2. Group 2

The group 2 panels extended on the knowledge gained from the group 1 panels. Some of the panels explored an increase in the end cap thickness while others looked at other gap structures. Miscommunication of the gap requirements, however, led to panels incorrectly gapped, thus some of these results will not be discussed in this subsection, but in the third group of panels subsection.

2.2.1. Modeling

Modeling from section 2.1.1 indicates that the end cap was showing some saturation effects. This saturation has been shown by theory and experimentation to lower the output voltage and increase leakage inductance. It was determined in the previous work that the ratio of end cap thickness to center core radius determines whether saturation in the end cap region is a limiting factor [3]. The modeling done for this work supports this and will also explain the desire for experimental work to increase stack buildup that is discussed later. The D51 model used in section 2.1.1 was varied in end cap thickness with results for flux density map shown in figure 10. For the lower current case, there is a visible difference in the saturation levels. There is also less flux crossing into coil indicating lower leakage inductance. For the higher current case, the saturation patterns do not change that much in the core. However, there is a decrease in leakage flux. The results of this modeling indicates that there might be more of an affect on leakage inductance versus output soft saturation.

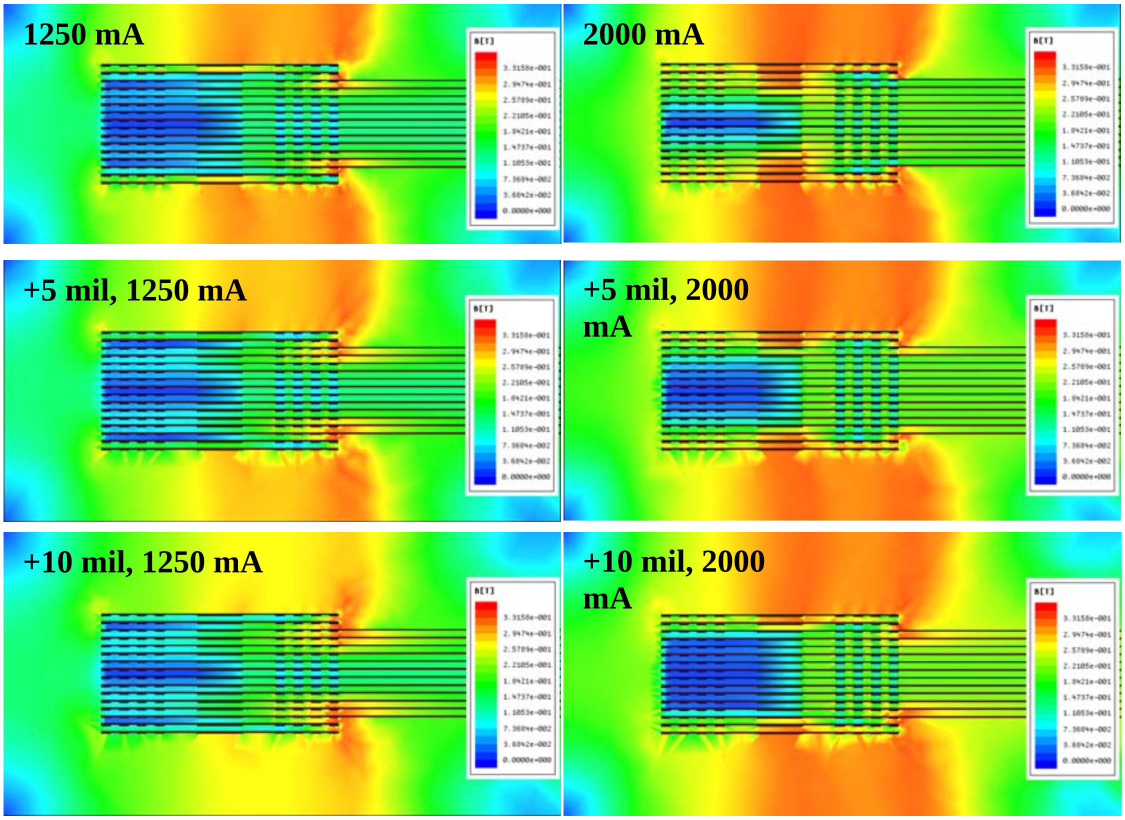


Figure 10. Flux density variation with end cap thickness and drive current.

Another model variation was the removal of the center dielectric gaps in the core center and the reduction of the end margin material. The reduction of the end margin area should simulate an outer gap which has been shown through modeling to be superior in coupling as compared to center gaps [3]. The idea behind the reduced end margin is that no dielectric paste would be at the edge of the device which could cause processing issues. Figure 11 shows the flux density pattern for the D51 transformer with varying end margin lengths. It is clear that there is less flux in the coil window as the baseline design in figure 4. Figure 12 shows the flux density pattern for the gap at the outside design from [3]. It shows lower flux in the coil window that indicates a higher coupling factor.

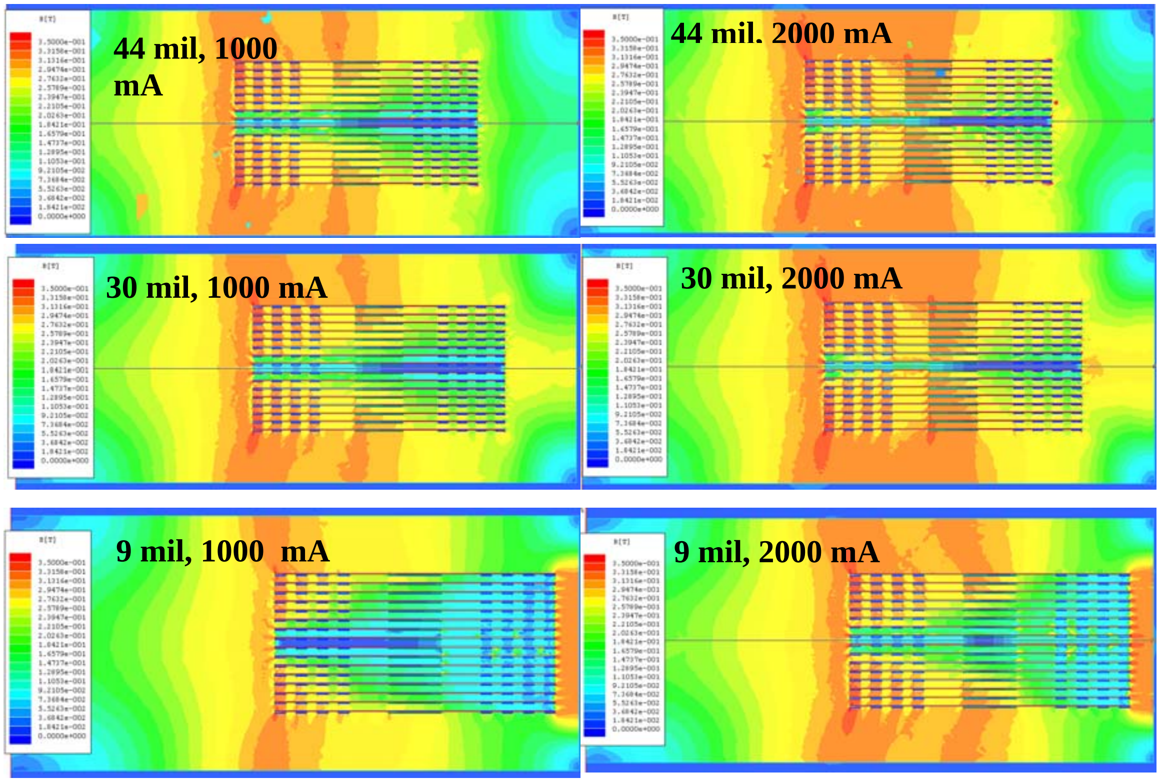


Figure 11. Flux density maps for variable end margin length.

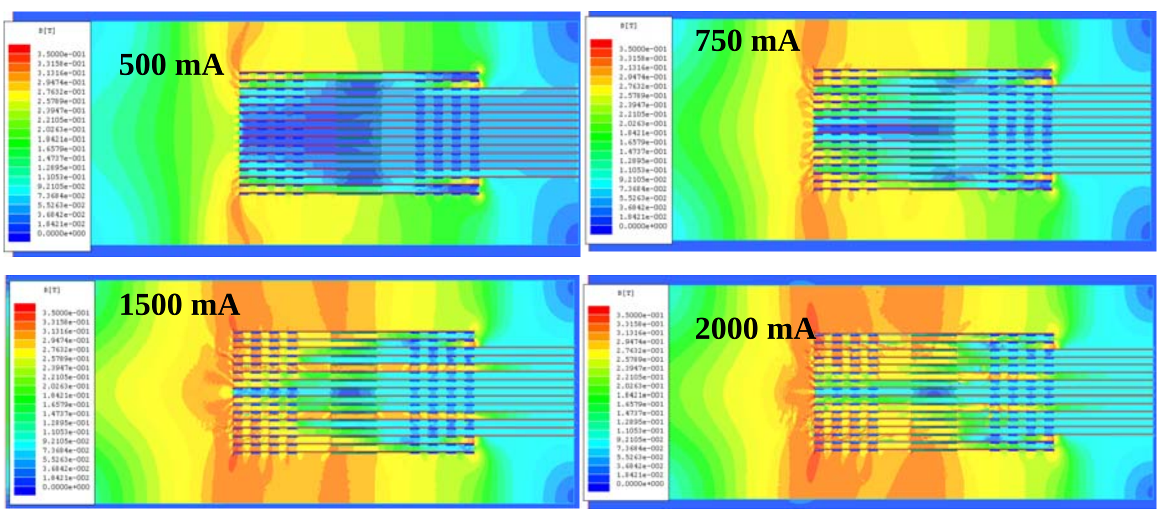


Figure 12. Outside gap design flux density patterns.

A direct comparison of the flux density is shown in figure 13. This plot is the flux density along the center of the long axis of the transformers. The leakage flux is comparable between the two designs although the design with the gap at the outside has a lower flux density than the variable end margin design for comparable currents in the end margin region. This indicates that the variable end margin will saturate earlier, however, it will exhibit lower leakage inductance, i.e. increased coupling. The presence of actual gaps is required to change the BH curve to prevent early saturation. The growth of a saturation region by increased flux density is not an effective gap for flyback operation. This is evident in the much larger inductance of the variable end margin design when compared to the outside gap design as shown in figures 14 and 15.

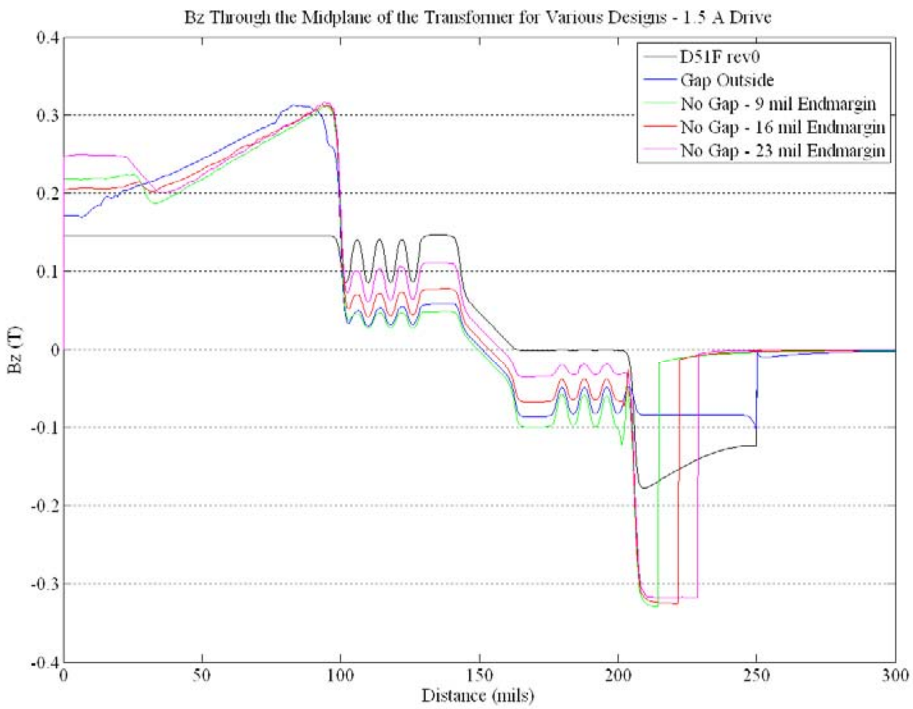


Figure 13. Flux density comparison for the variable end margin and outer gap designs.

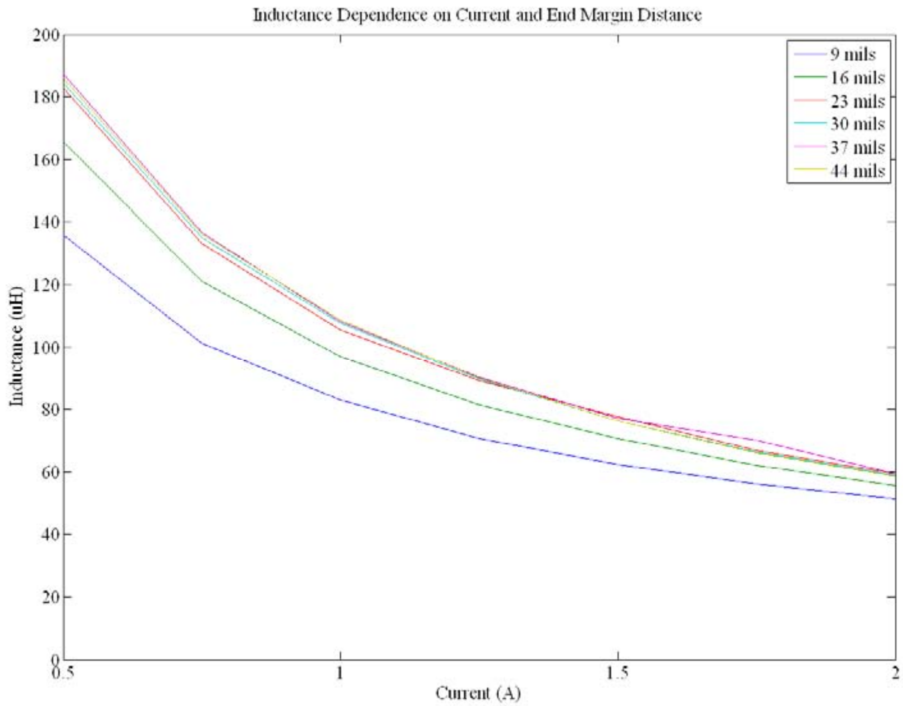


Figure 14. Variable end margin design inductance curves.

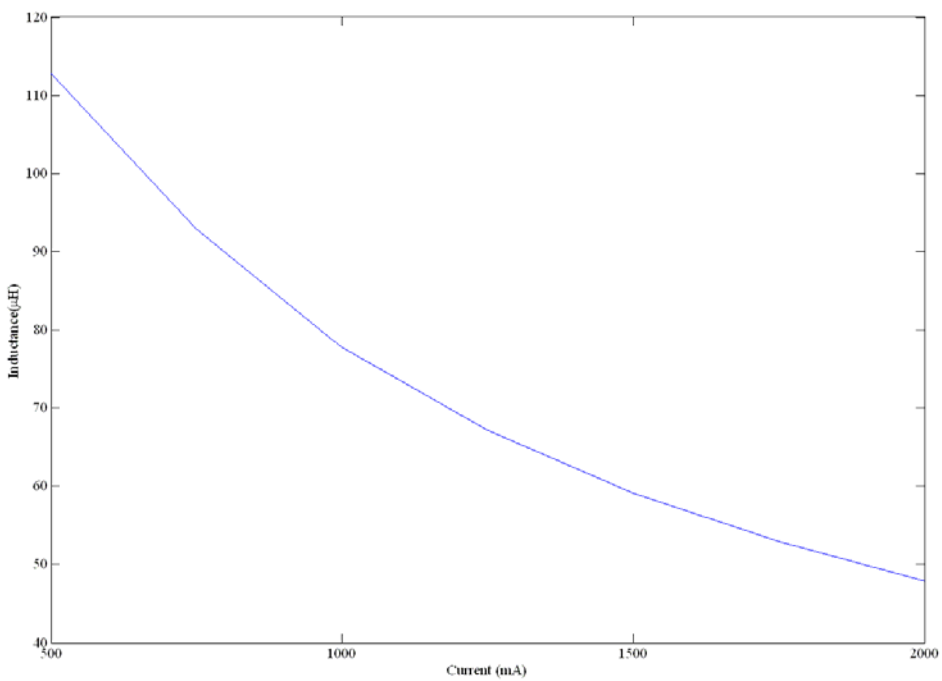


Figure 15. Outside gap design inductance curve.

2.2.2. Fabrication and Test

The group 2 panels are a realization of the modeling that was done in the previous subsection. In addition to the new designs, a different cutting method was explored. The traditional method of singulating transformers is to use a Guillotine method on the unfired bar. This method is well established for thin parts (less than 0.10"), but for thicker parts, side splitting and cracking can occur which lead to degradation in performance (increasing gap lengths) or part failure after firing is complete. The new method is the routing method. This tool uses a rotating bit to separate the pieces like a traditional wood working router. For this series of panels, some panels were selected for routing at an outside company since a router was not available (one was later bought). The problem with this scheme is that singulation of green panels and firing cannot be done in the same day which tends to increase side splitting.

A summary table of successfully process panels is shown in table 4. For panel 2277Y, the inductance was about the same as that from the group 1 panels. Even though the part was thicker, more gap layers were added resulting in an inductance that was roughly the same. Panel 2286 had a much higher inductance since there were no gap layers, only a small end margin length of 5 mils. The last panel, 2282Y, was suppose to be the outside gap margin design, however, miscommunication led to a design with the gap layers through the center of the whole transformer. The correct design with just outside gaps was done in group 3 of the D51 fabricated panels.

Figure 16 shows the output and voltage stress performance for the group 2 panels. The performance of the thicker parts was the same as the thinner parts as shown in the top two plots of figure 16. The middle two plots show the performance of the reduced margin design (no gap). The transformers worked but the parts saturated earlier. The coupling was higher, however, the leakage inductance was approximately the same, thus the increase was due to the larger inductance of the primary. The parts with the gap extended to the end margin did better then the center only gap with the plots shown at the bottom of figure 16. It appears that these parts saturate later as expected from an increase in effective gap length. The G variants perform the same as the regular gap D51 transformers but at higher currents, more output was possible due to the later saturation. The voltage stress was approximately the same even thought the outer gapped transformers had a larger leakage inductance which is interesting.

Table 4. Group 2 builds and measured parameters (averaged)..

Build – D51F	**L_p (µH)**	**L_s (mH)**	**L_{lp} (µH)**	**Rp (Ω)**	**Rs (Ω)**	**k**
2277Y (16W,16G,47L)	133.25	6.44	25.32	1.30	50.97	0.91
2286Y (16W, 0G, 47L,RM)	370.16	19.78	18.70	1.27	50.81	0.97
2282Y (16W, 16G, 47L, CG+MG)	120.89	5.66	23.50	1.34	51.52	0.90
2220Y (16W, 12G, 39L)	145.10	6.16	30.86	1.44	55.81	0.88

Build – D51G	**L_p (µH)**	**L_s (mH)**	**L_{lp} (µH)**	**Rp (Ω)**	**Rs (Ω)**	**k**
2277Y (16W,16G,47L)	178.90	7.55	74.55	1.29	48.23	0.76
2286Y (16W, 0G, 47L,RM)	396.70	19.98	72.36	1.34	46.58	0.90
2282Y (16W, 16G, 47L,CG+ MG)	202.44	6.90	91.58	1.35	49.27	0.75
2220Y (16W, 12G, 39L)	168.06	6.84	63.56	1.4	53.94	0.82

Build – D51H	**L_p (µH)**	**L_s (mH)**	**L_{lp} (µH)**	**Rp (Ω)**	**Rs (Ω)**	**k**
2277Y (16W,16G,47L)	351.63	8.57	175	1.28	47.62	0.67
2286Y (16W, 0G, 47L,RM)	-	-	-	-	-	-
2282Y (16W, 16G, 47L, CG+ MG)	283.70	7.39	179.82	1.31	48.47	0.61
2220Y (16W, 12G, 39L)	208.15	7.70	132.64	1.37	52.75	0.70

Build – D51K	**L_p (µH)**	**L_s (mH)**	**L_{lp} (µH)**	**Rp (Ω)**	**Rs (Ω)**	**k**
2277Y (16W,16G,47L)	132.48	5.44	21.61	1.38	49.08	0.91
2286Y (16W, 0G, 47L,RM)	376.80	20.02	21.40	1.34	48.33	0.97
2282Y (16W, 16G, 47L, CG+ MG)	126.87	5.45	24.29	1.40	49.67	0.90
2220Y (16W, 12G, 39L)	123.98	6.24	47.15	1.5	54.55	0.84

Note: W=winding layers, G=gaps, CG=center gaps, L=total layers, RM=Reduced Margin. 2220Y is from Group 1.

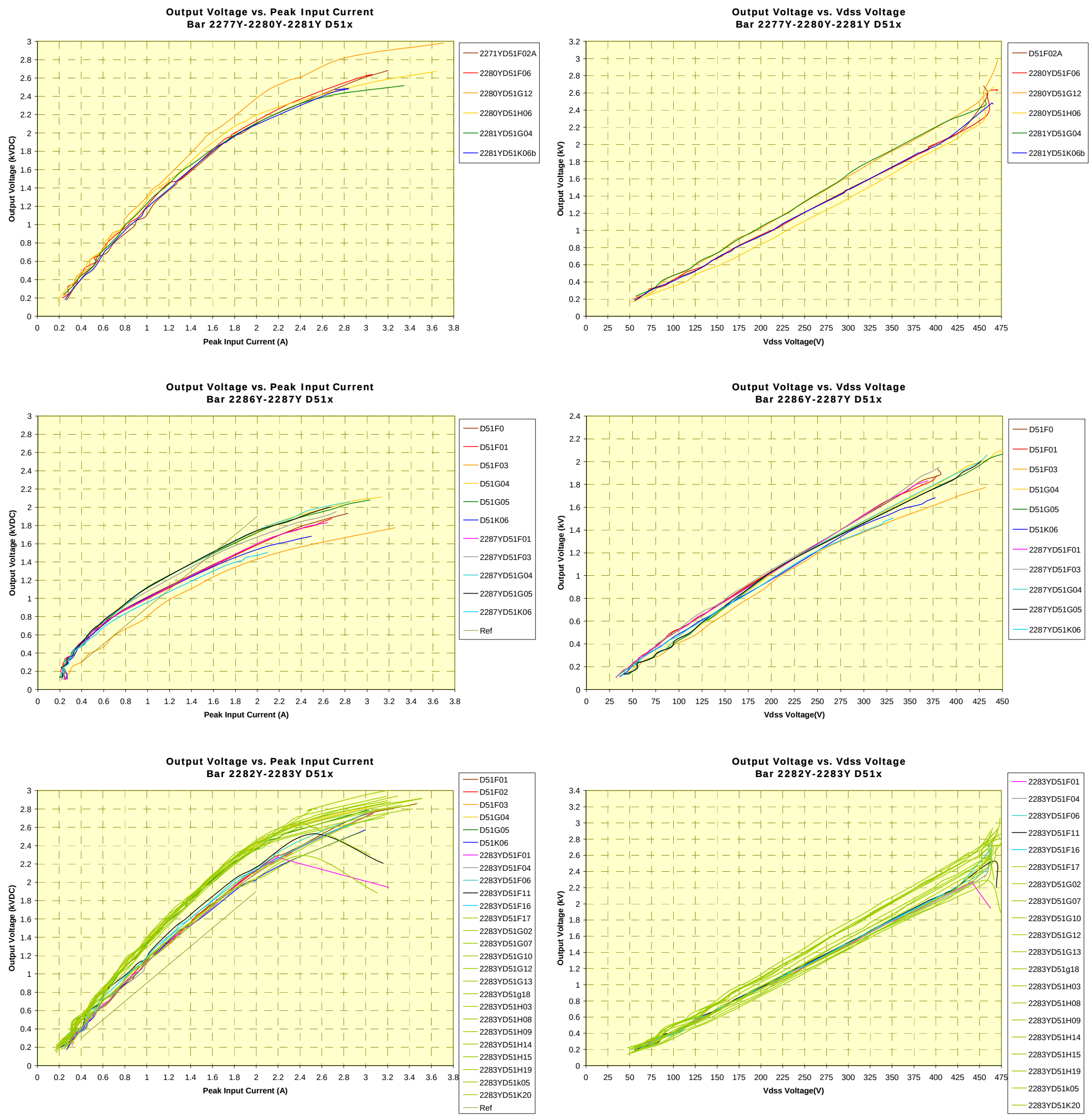


Figure 16. Group 2 panel output voltage and voltage stress performance.

2.3. Group 3

2.3.1. Fabrication and Test

The group 3 panels followed the intended design of having the outer gap with no gap in the center core area (see section 2.2.2). The J variant has the primary at the outside with 8 secondary turns per layer and the L variant had 9 secondary turns per layer. The measured parameters are given in table 5. The performance of the transformers is shown in figure 17. Panel 2323Y with the gap at the outside does not perform as well as the gap throughout the whole part (2283Y) or the thicker D51G variant (2280Y).

Table 5. Group 3 builds and measured parameters (averaged).

Build – D51G	L_p (µH)	L_s (mH)	L_{lp} (µH)	Rp (Ω)	Rs (Ω)	K
2323Y (16W,16G,47L,MG)	185.59	10.53	21.18	1.25	44.94	0.94
2283Y (16W, 16G, 47L, CG+MG)	202.44	6.90	91.58	1.35	49.27	0.75
2220Y (16W, 12G, 39L)	168.06	6.84	63.56	1.4	53.94	0.82
2280Y (16W,16G,47L)	178.90	7.55	74.55	1.29	48.23	0.76
Build – D51J	**L_p (µH)**	**L_s (mH)**	**L_{lp} (µH)**	**Rp (Ω)**	**Rs (Ω)**	**k**
2323Y (16W,16G,47L,MG)	172.18	10.47	41.13	1.51	41.17	0.87
Build – D51L	**L_p (µH)**	**L_s (mH)**	**L_{lp} (µH)**	**Rp (Ω)**	**Rs (Ω)**	**k**
2323Y (16W,16G,47L,MG)	168.94	14.05	41.85	1.51	45.03	0.88

Note: W=winding layers, G=gaps, CG=center gaps, L=total layers, RM=Reduced Margin. 2220Y is from Group 1 and 2282Y and 2277Y is from group 2

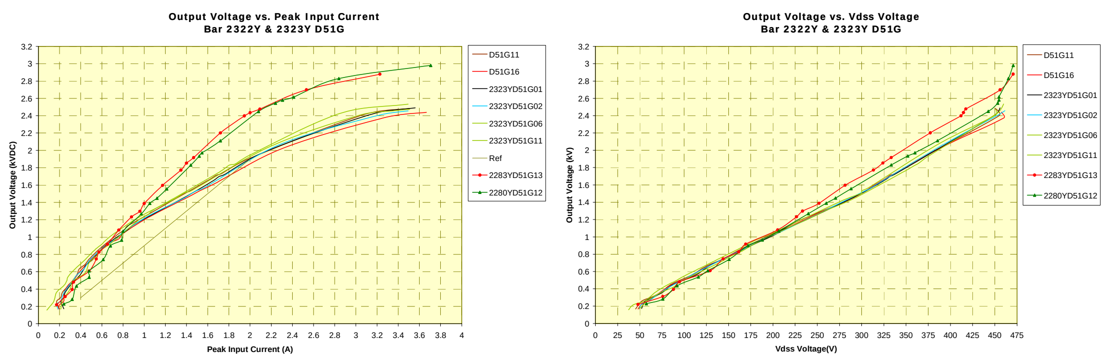


Figure 17. Group 3 output voltage and voltage stress.

2.4. D51 Summary

The D51 transformer, the larger cousin of the D47, D48 and D50 designs has demonstrated higher voltage outputs. The comparison of these design is shown in figure 18. For a 1500 V output, the D51G requires 0.3 A less current than the D50E and about 0.15 A less than the D47. Unfortunately, the D51 has significantly higher flux leakage leading to higher flyback FET voltage stress for a given output when compared to the D50E. The curve in the output voltage dependence on primary current at approximately 2 A shows saturation effects in the transformer. In order to increase the output, this saturation effect must be reduced. Part dimensions and gap structure need to be further explored to increase the saturation level.

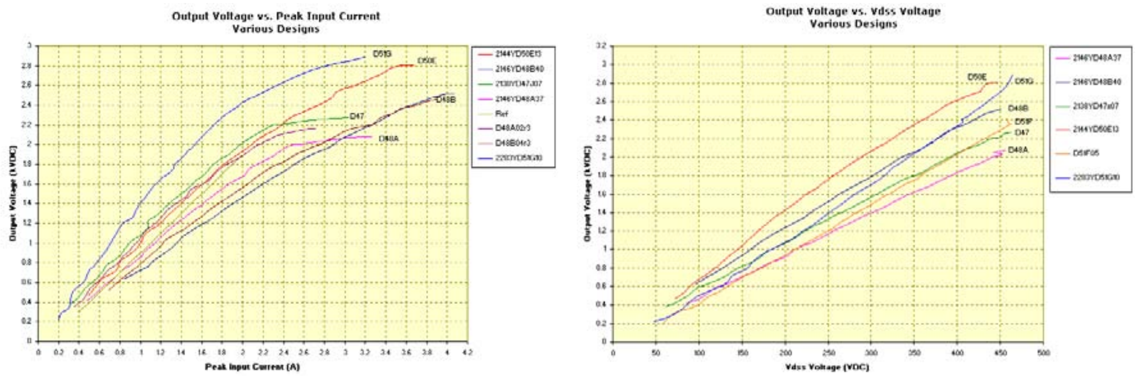


Figure 18. Comparison of D51 and previous designs.

There is still some work that can be done to further the design and knowledge of the D51 transformer and is as follows:

1. Optimize burnout profile using mock up bars to try eliminating cracking during firing.
2. Develop a ferrite paste to help even out pressed density.
3. Study effect on pressed density of a dielectric or ferrite paste pattern in the core and end margin areas.
4. Try isostatic lamination to improve green density uniformity.
5. Develop processing of thicker parts.
6. Study increased end cap thickness effects.
7. Study increased margin area effects.
8. Further study of the outside gap and gap throughout whole part design.

3. Insulation Resistance

Throughout the development of the LTCC planar transformers, the decrease in output voltage at high currents has not been well understood. There are two hypotheses with the first being that the transformer is saturating which would cause a drop in primary inductance thus lowering the transfer energy to the secondary during flyback. The second is a material property may be changing such as permeability or insulation resistance. A decrease in permeability would lower the inductance and would happen if the temperature increased due to internal Joule heating. The insulation resistance will depend on the temperature and with the increased currents to reach higher output voltages bring increases in Joule heating which could lower the insulation resistance.

To study the effects of temperature on the insulation resistance of the tapes used in the LTCC system, several test samples were fabricated. These samples involved different types and blends of ferrite and dielectric tapes (used in transformer structure to be discussed in a later section) with different layer counts. The test structure is shown in figure 19. A Fluke 1550 MegaOhmeter was used for all measurements with the results shown in figure 20-22.

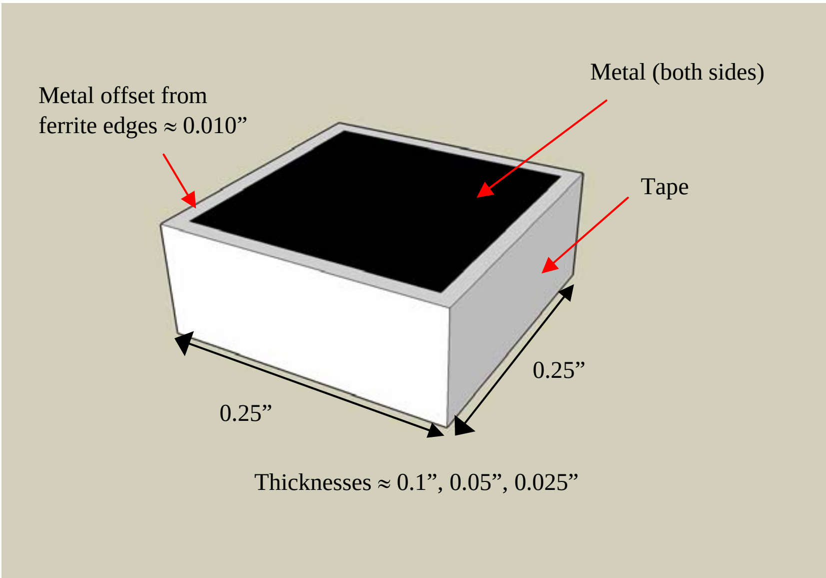


Figure 19. Insulation resistance test structure.

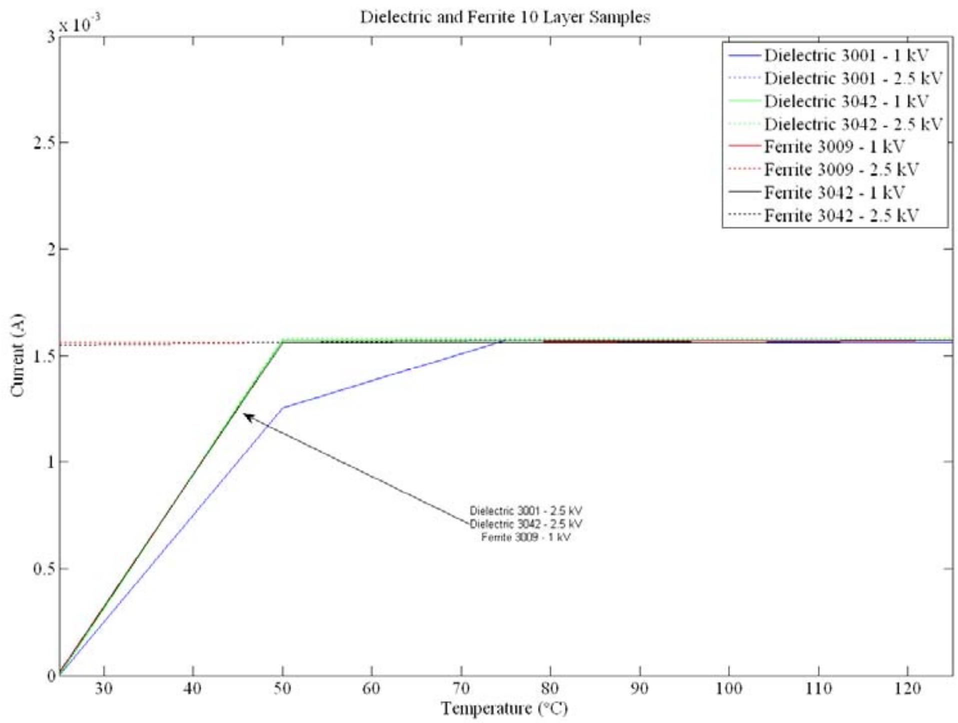


Figure 20. Leakage current for 10 layer samples.

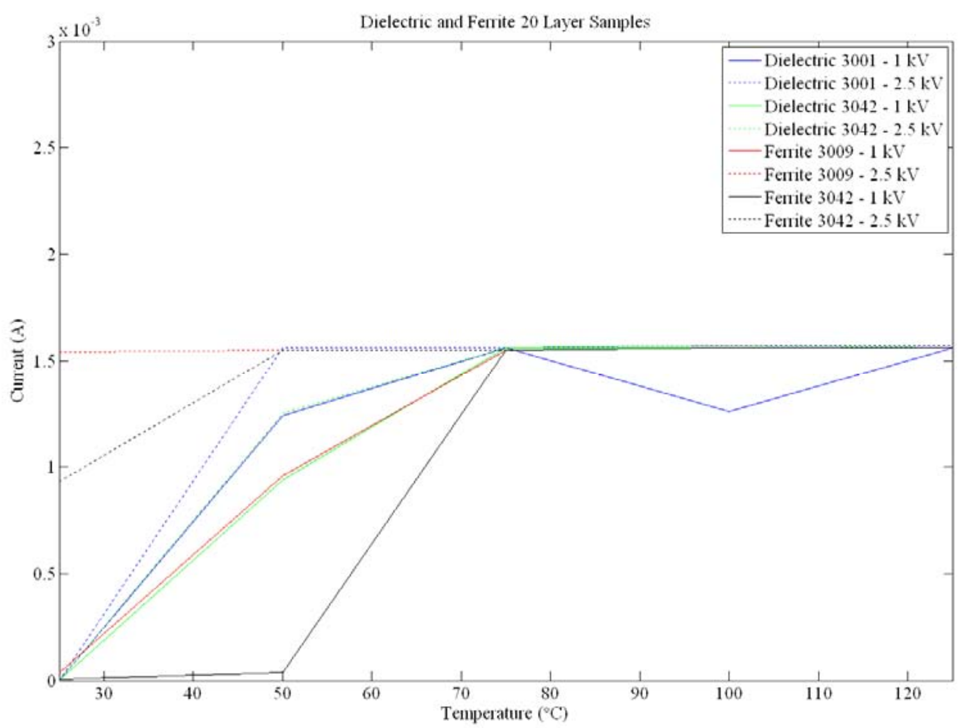


Figure 21. Leakage current for 20 layer samples.

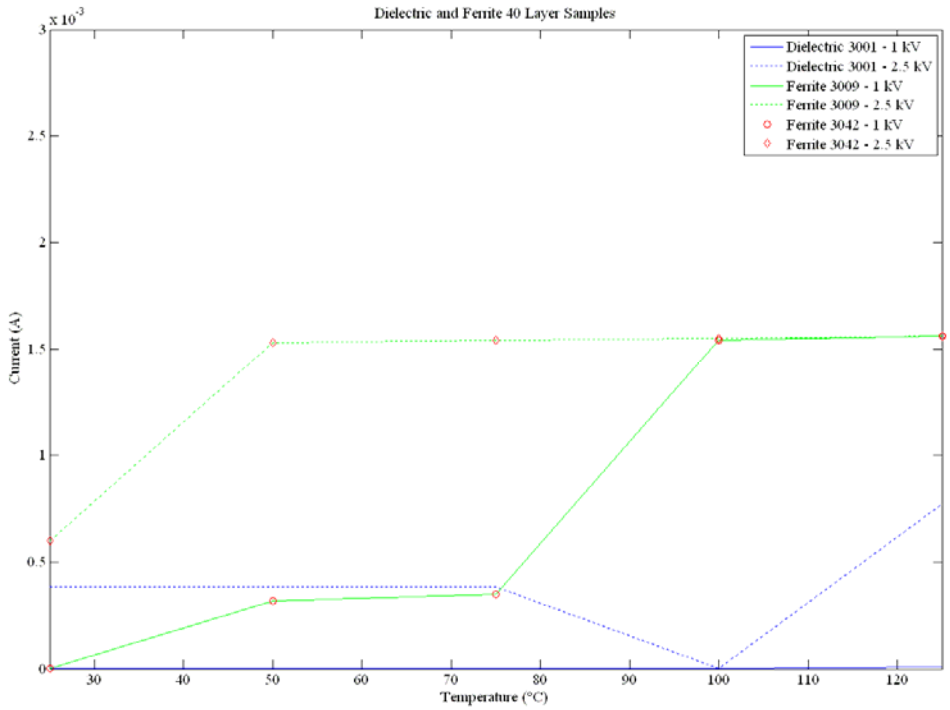


Figure 22. Leakage current for 40 layer samples.

The leakage current clearly shows a strong dependence on temperature. For the 10 layer parts, the ferrite samples with 2.5 kV applied hit the current limit of the tester at all temperatures. The other samples started to show increased leakage immediately above room temperature (25 ºC). The 20 layer samples showed similar performance to the 10 layer samples, but the temperature where the current was limited by the tester was pushed out in temperature. This makes sense since the parts are thicker. For the 40 layer samples, the limit was pushed even higher. The dielectric-3042 samples for the 40 layer case were suspect (sample preparation) and thus the data is not shown. In all cases, the ferrite appears to have larger leakage currents than the dielectric material.

What this data clearly shows is that temperature rise affects the losses in the material and that it could affect transformer performance and should be investigated further. For example, the 10 layer ferrite samples showed increasing leakage with increased temperature at similar volts/layer stress in LTCC planar flyback transformers. For the 10 layer sample, 250 V/layer had large leakages. For a 16 layer secondary transformer with an output of 2 kV, the stress is 125 V/layer. Data shows that this is possible with the existing design and technology. Experience has shown that higher outputs of 3 kV (187 Volts/layer for 16 layers) and higher require large currents and time at charge presents difficulties as in some instances the output voltage droops. This could be temperature related affects at these voltage stresses that approach a couple hundred volts per layer and would most likely be higher in a transformer application due to higher field stresses.

4. Dielectric Ring Coil Transformer

One of the limits of the LTCC planar flyback transformer is the leakage inductance. This leads to increased voltage stress on the flyback FET which leads to larger parts than necessary and increases power losses during switching. In addition, the efficiency of transfer is lowered, leading to higher input power requirements to meet charge time and output voltage requirements. The factors that lead to high leakage or low transformer coupling in planar LTCC transformer design are the materials and design itself.

The design, as shown in figure 4, shows a large amount of flux crossing the area traditional known as the winding window in wire wound designs. It is this flux which fails to link to the secondary turns that produces leakage inductance. The current design approach used for the LTCC transformer has a ferrite material layered with dielectric paste in this window to reduce this flux leakage. In traditional wire wound design, this area would be filled by air, wire, bobbin and insulating tape, all of which are nonmagnetic. In addition, the reduced thickness of this design and increased coil width of the window further increase the flux leakage as shown in figure 23 and given by equation 1 [4]. This equation is derived for a wire wound transformer with concentric windings, but can be applied to the LTCC design for qualitative purposes and to show the relationships between the geometrical dependencies. As the winding width, interwinding separation or mean insulation perimeter increases (h_1, h_2, h_3, P) the leakage increases because of increases area for flux to leak across the winding plane. On the other hand, if the coil thickness (D) increases, leakage decreases, because the path for the flux to cross increases. In other words, the flux would prefer magnetically to stay in the core instead of crossing the winding window. Thus, to minimize leakage, a tall and narrow winding window is optimal, but in LTCC transformer there is a limit due to process limitations.

The other factor is the material in the winding window area. Current LTCC process has layers of ferrite and dielectric paste across the winding area. The paste is used to decrease the amount of

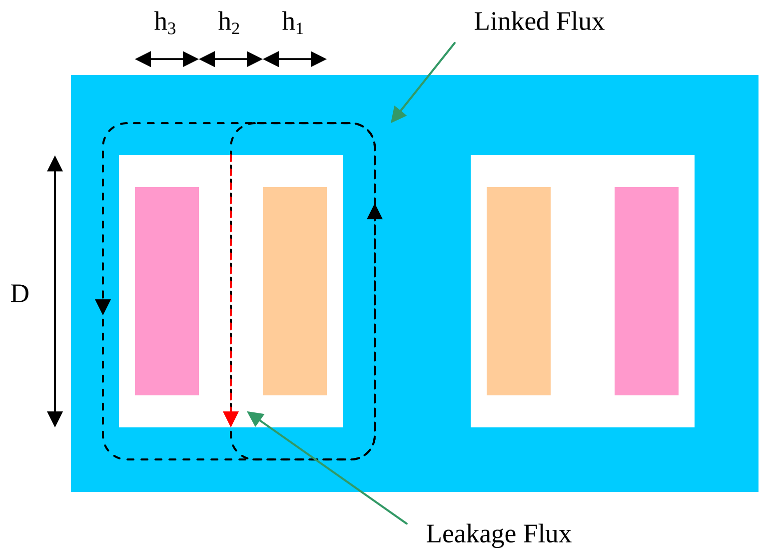


Figure 23. Concentric winding transformer.

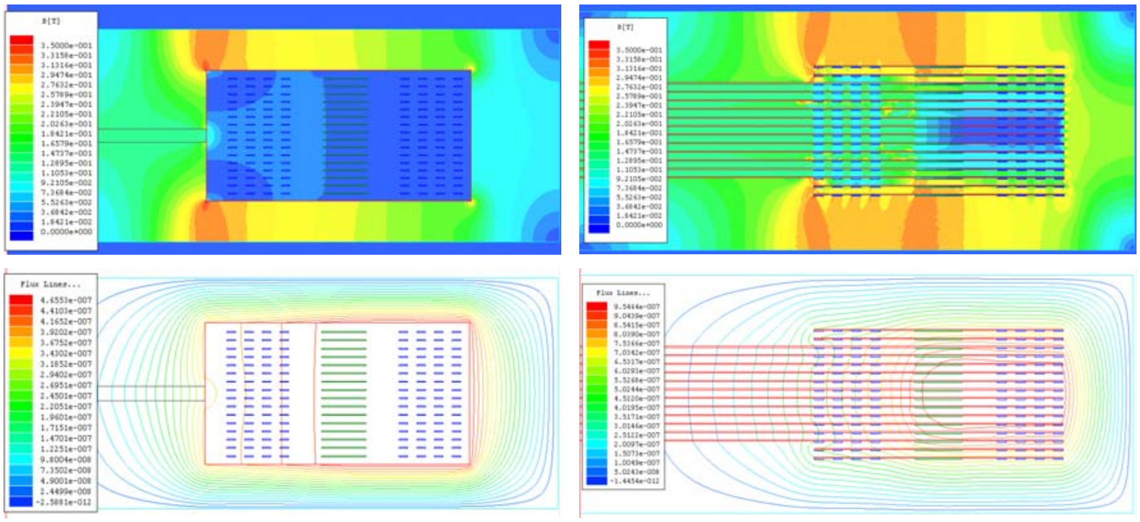
$$L_L = \frac{4\pi N^2 P}{D}\left(\frac{h_1 + h_3}{3} + h_2\right) \times 10^{-9} \qquad (1)$$

N = Number of turns of winding
P = Mean perimeter of insulation between windings
L_L = Leakage inductance in henrys

leakage by increasing the reluctance across the winding window. However, there is still ferrite material in this window which promotes flux leakage. To minimize leakage, a nonmagnetic material should be used in the winding window area as in traditional wire wound transformers. This section of the report will discuss a new process and material that demonstrates a significant increase in coupling factor by reducing the amount of leakage flux through the winding window area. The design is called dielectric ring coil LTCC planar transformer.

4.1. Modeling

The proposed designs to be studied were the same as the D50 and D51 transformers from previous work and in section 2 of this report. The only difference was the removal of all magnetic material from the winding window area to study the differences in flux leakage and to see if development for this process is beneficial. The area removed was replaced with a vacuum condition with a relative permeability of 1. Figure 24 shows the flux density for a D51 sized transformer with a nonmagnetic and magnetic material in the winding window area.



Nonmagnetic Material Magnetic Material

Figure 24. Flux patterns for nonmagnetic and magnetic material in winding window area for D51 size.

As figure 24 clearly shows, the presence of magnetic material in the winding window area has a major effect on flux generated by the primary coils (red) crossing the window area causing it to not link with all of the secondary coils (blue). This is what produces leakage inductance. Figure 25 shows a line plot of the flux density across the midplane of the transformer that clearly demonstrates the loss. The loss is similar in the outer secondary coil region only near the central axis of the transformer while at the inner secondary coil the losses are larger, especially at increasing currents. With the magnetic material in the winding window area, at large drive currents, the saturation in the end cap region increases, forcing the additional flux to cross the window. In the nonmagnetic case, the leakage increases, but not as on large scale as the magnetic case. The downside of this design is the lower flux density in the central core volume which will lower output. A thicker end cap would probably alleviate this issue by reducing the saturation there. The flux in the magnetic case at large currents, widens the central core volume allowing the flux density to increase there. Obviously, each design has its tradeoffs.

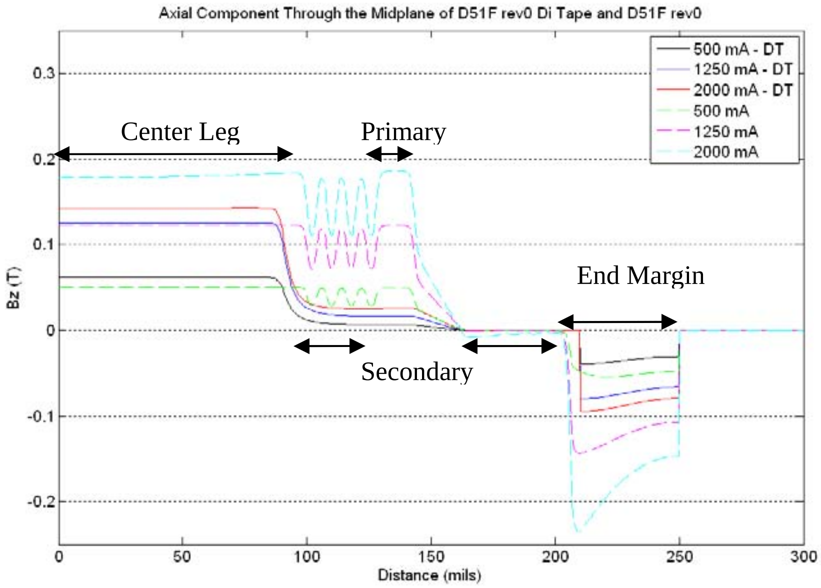
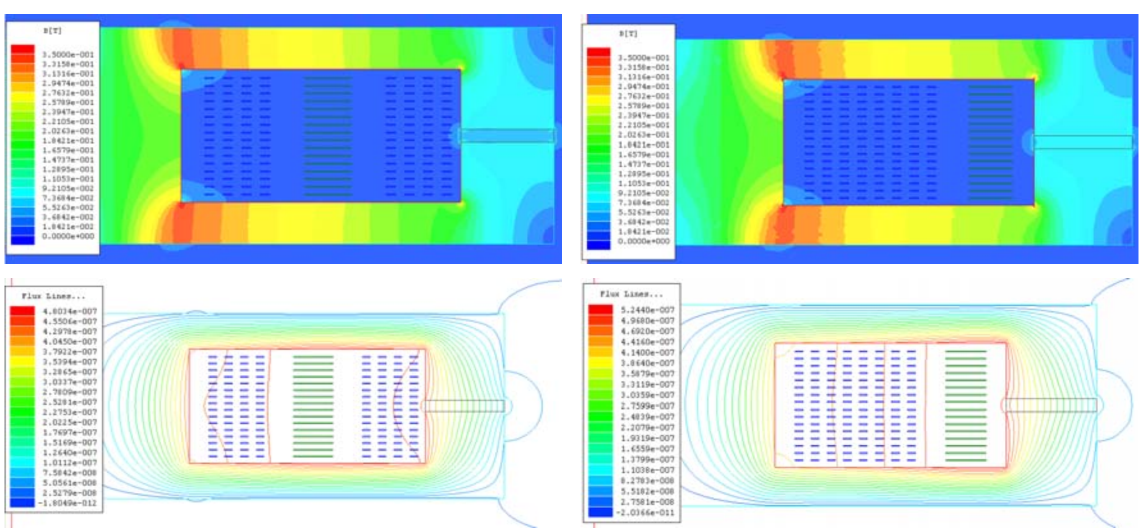


Figure 25. Flux density comparison along transformer midplane.

Another comparison was made with the outer gap design from section 2.2.1. That design showed improvement by reducing leakage inductance. The results are shown in figure 26. There was slight reduction in the leakage flux for the primary winding at the outside (closest to the gap). A comparison of this design with the magnetic material in the winding window area is shown in figure 27. The result is the same as in figure 25 for the traditional LTCC design (gap in the



Primary in the Center

Primary at the Outside

Figure 26. Gap outside designs with nonmagnetic material in window area.

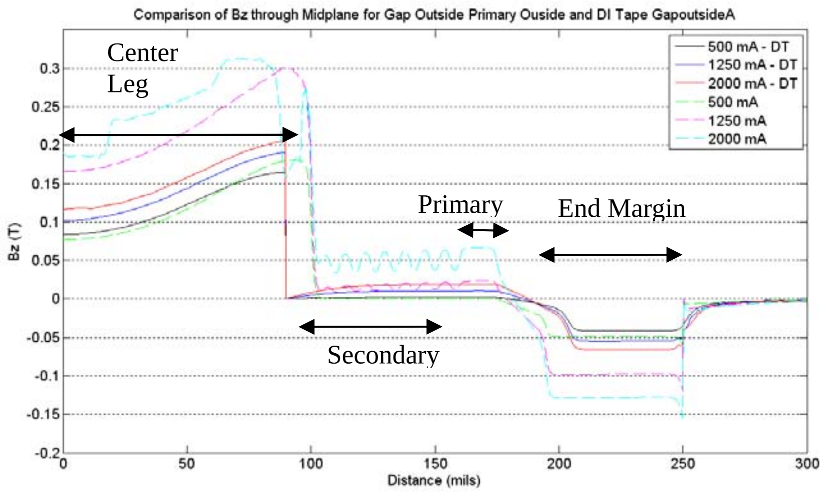


Figure 27. Comparison of gap outside design with and without magnetic material.

center). The major difference is the leakage flux is much lower for the design with magnetic material in the window. Only at very high currents do the difference become large for the secondary coil region. The region between the central core and the secondary coil still show a large difference in the flux leakage with the nonmagnetic material case superior.

4.2. Dielectric Tape Development

The obvious replacement for the nonmagnetic material in the winding window area is a nonmagnetic ceramic tape that can hold off high voltages (high electric field stresses). The material must be compatible with the LTCC process and more importantly, must be compatible with the LTCC planar transformer fabrication process. Since the LTCC transformer requires the use of magnetic ferrite tapes and conducting paste, the new material, a dielectric tape, must be able to be fired at the same time and form an adhesion layer with the ferrite tape and conducting paste to produce a monolithic structure, the goal of this project.

4.2.1. First Batch of Dielectric Tape

Dielectric green tape was procured from the same manufacturer of the ferrite green tape. The manufacturer cast a new tape to try and meet the following desired properties: approximate thickness and shrinkage rates to the ferrite with reasonable dielectric strength. The later does not require a high dielectric constant as would be desired for a high density capacitor but high voltage standoff. The tapes were then made into a series of test structures the same size as the D47, D50 and D51 planar transformers. Three different burnout profiles were tried to minimize cracking and delamination. The samples were microscopically inspected before and after burnout to check for delamination at the ferrite/dielectric boundaries. The post fired samples were cross-sectioned to better understand the burnout process and compatibility. The first batch of dielectric tape was done in three separate groups.

4.2.1.1. Group A – Layers

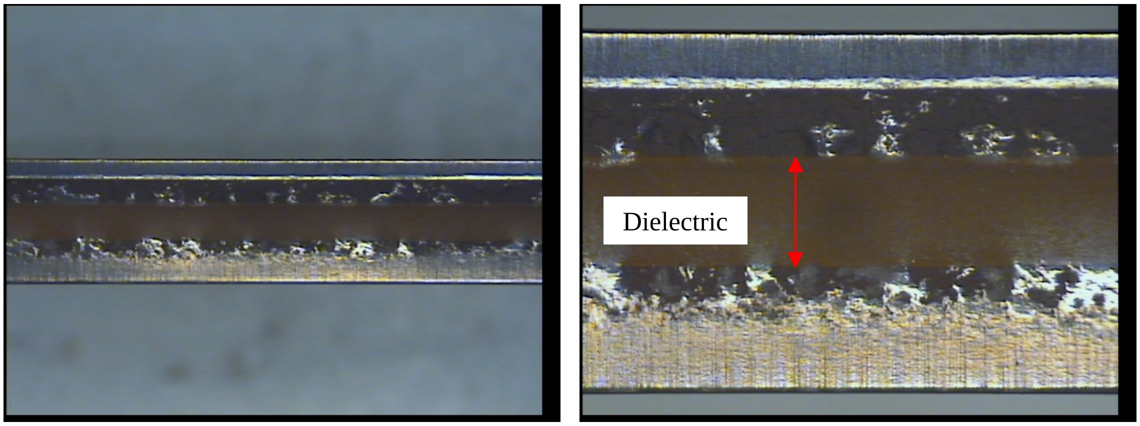
The first group of panels contained only ferrite and dielectric tape layers with no printed windings internally. This was to determine if the simplest of combined structure would work. All groups of panels had the following material stack up given in table 6. The results of the pressing of layers (green state, prefire) and the post firing are all similar for the different size panels. The results of the D51 size are shown in figure 28. All three panels had edge cracks for each separate burnout profile tested. These cracks indicate a mismatch in shrinkage rates between the ferrite and dielectric tape materials. Fortunately, all visual indications show good bonding.

4.2.1.2. Group B – Layers with Printed Conductors

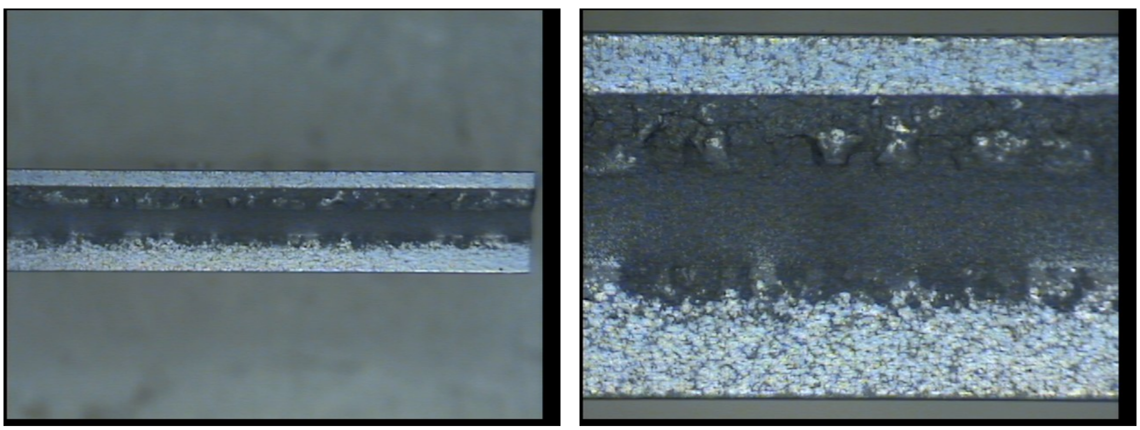
The group B panels are the same as the group A panels, however, there are printed conductors (windings) on the dielectric layers. This was done to see if the thick film conductor impacted the adhesion and firing of the mixed ferrite and dielectric panel system. Pictures of the cross-sectioned D51 post-fired panels are shown in figure 29. These panels had the same cracking as seen in group A (figure 28), however, the cracks seem to be concentrated more in the corners of parts. One hypothesis of this crack concentration is that the thick film conducting material is moderating the mismatch between tapes. The thick film is not present in the corners, thus the reason for a possible increase in crack concentration.

Table 6. Dielectric samples material and layer stack ups.

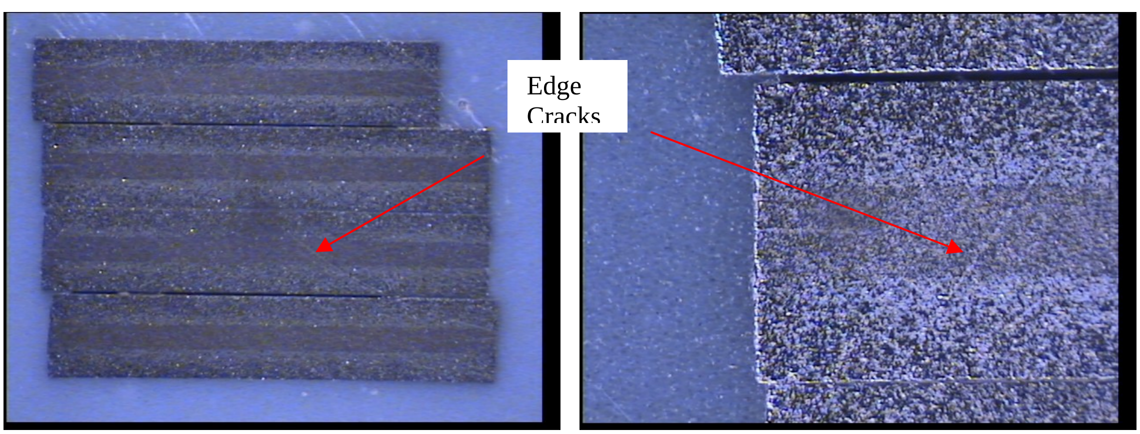
Sample	Top Material	Middle Material	Bottom Material
D47 (3640 Fired)	Ferrite (14)	Dielectric (11)	Ferrite (14)
D50 (3640 Fired)	Ferrite (12)	Dielectric (15)	Ferrite (12)
D51 (5055 Fired)	Ferrite (16)	Dielectric (15)	Ferrite (16)



Pre-Fired



Post-Fired



Post-Fired Cross-Section

Figure 28. Group A panel microscopic pictures.

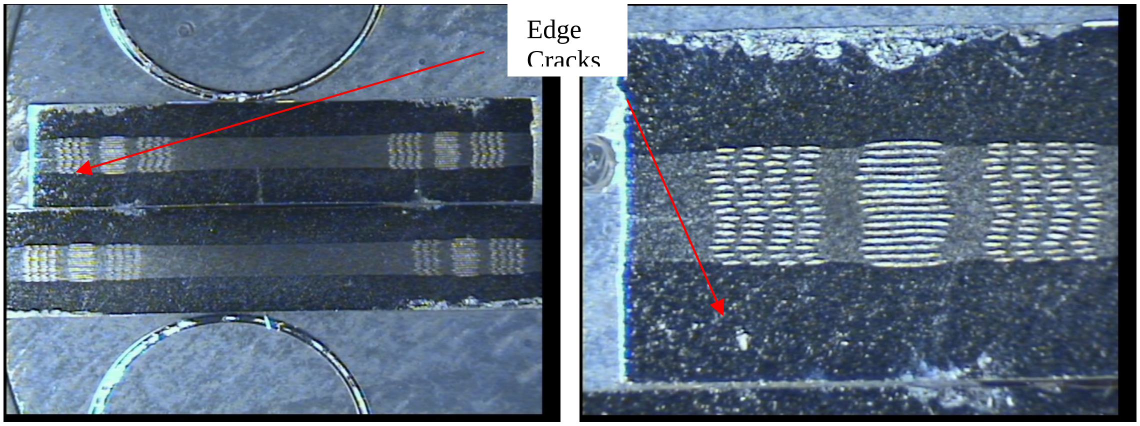


Figure 29. Group B cross-sectioned pictures.

4.2.1.3. Group C – Contingency Panels

Group C panels were built after analyzing the results from group A and B. There original intent was to be backups in case something catastrophic occurred in the first and second groups of panels. It was decided that group C was to be made into electrically functioning transformers. This was done again to test the process with fully connected vias between layers and connections to the external pads on the individual parts. One each of a D50 and D51 panel design were built. In addition, a special D51 sized panel was built that had a hole punched through the center of the dielectric layers and then a ferrite plug was inserted followed by loose end cap layers. The parts were then singulated and ferrite tape was wrapped around to form a closed magnetic. This was a simple and inexpensive method to test the concept of a dielectric material transformer.

The D50 panels did not turn out since none of the parts had continuity. There was similar cracking as observed in the previous panels and the cross-sections showed nothing that would indicate the cause for the lack of continuity. The D51 panel, however, had all but two of its parts have continuity. Pictures of the D51 transformers with the ferrite tape are shown in figure 30. Output voltage as a function of current for these first prototypes are shown in figure 31. The data clearly shows that transformers with the dielectric tape clearly work especially the designs with the separate slug and ferrite tape around the edge. The D51 parts with center slug showed more cracking since there is a tight fit which caused higher stress in this area than normal. There was some radial cracking on the top and bottom surfaces due to this increased stress which was not seen before. This knowledge will lead to the discussion of the separate pieces in the design described in a later section.

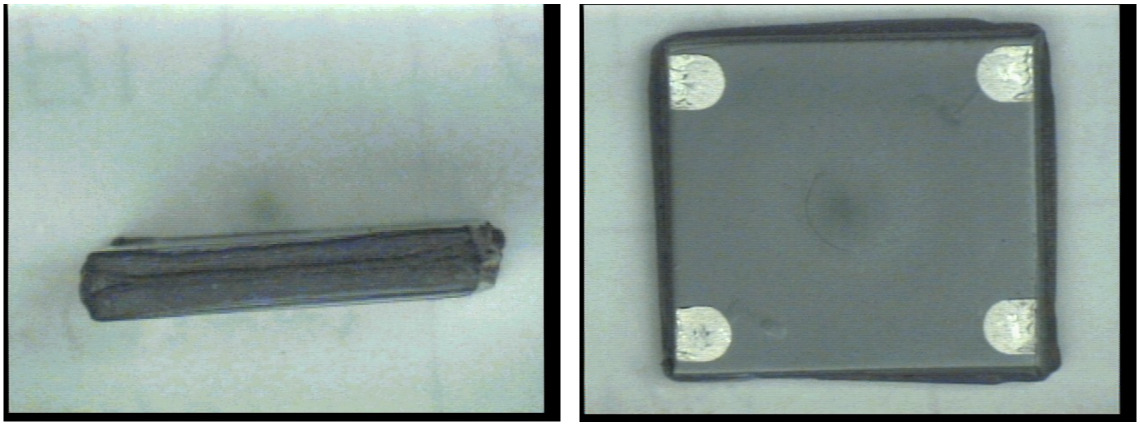


Figure 30. Special D51 transformers wrapped with ferrite tape.

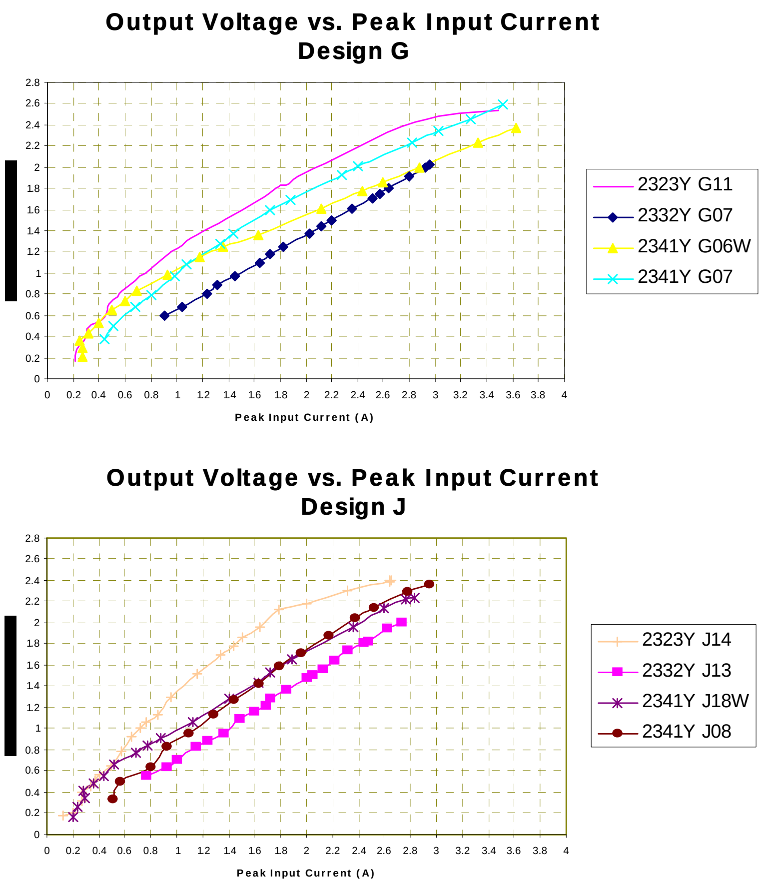


Figure 31. Special D51 transformer output plots. 2323Y is dielectric tape and 2341 is dielectric tape with center ferrite slug and external ferrite tape.

4.2.2. Second Batch of Dielectric Tape and Modified Ferrite Tape

The transformers and test samples made with the first batch of dielectric tape from the previous section showed cracking which could negatively impact the structural integrity and functionality of the parts. The main cause of the cracking is believed to be related to the mismatch in shrinkage rates between the dielectric and ferrite tapes. To minimize the cracking, another batch of dielectric tape was developed in addition to a modified ferrite tape. The dielectric tape shrinks more than the ferrite. In order to decrease the shrink rate, binder can be removed from the formulation; however, this may negatively impact the laminating and handling properties. To increase the shrinkage rate of the ferrite, binder can be added, however, this could increase cracking during firing because more organics need to be removed. The solution to this dilemma was to do a second batch of dielectric tape with decreased binder and a ferrite tape with increased binder. By not changing the dielectric drastically as desired and changing the ferrite, it was hoped that minimal issues would be encountered. Samples of the dielectric and ferrite tapes were made and their shrinkages were measured with data shown in table 7. The data shows that compared to the original lower binder content ferrite and first batch of dielectric tape, the modified ferrite and lower binder content dielectric tape (second batch) show a significant improvement in shrinkage difference. Further work on tape formulations could probably improve the shrinkage differences. Pictures of test structures with the new dielectric and ferrite tapes are shown in figure 32. Cracking is still an issue and is not that much different than the previous blends of tapes. Also tried were different cutting methods, the traditional razor-cut and routed with no significant differences observed. The hypothesis is the cracking is still due to mismatches in the shrinkage rates during firing even though the final shrinkage rates are better matched. Further analysis with thermo-mechanical analysis/thermo-gravimetric analysis (TMA/TGA) to measure shrinkage rates through time should be done.

Table 7. Dielectric and ferrite tape shrinkage rate differences.

Tape	X Shrinkage	Y Shrinkage	Z Shrinkage
Ferrite to First Batch Dielectric	1.78%	2.03%	2.20%
Ferrite (Higher Binder) to First Batch Dielectric	1.34%	1.59%	2.30%
Ferrite (Higher Binder) to Dielectric (Lower Binder)	0.99%	1.27%	1.76%

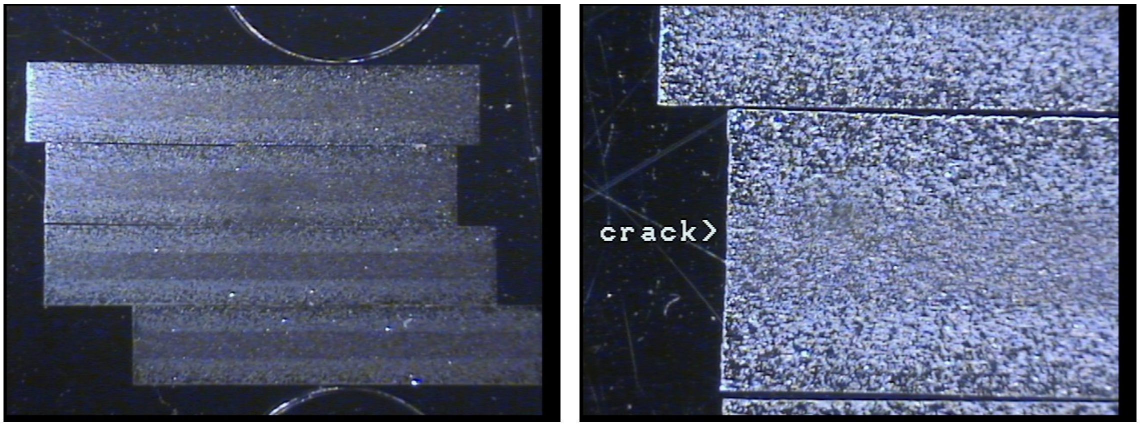


Figure 32. Cross-section of samples with new blends of tapes.

4.3. Dielectric Ring Coil Planar LTCC Transformer

4.3.1. Fabrication Process

In order to fulfill a true dielectric tape window winding area, separate pieces will have to be made and fitted together before firing of the tapes. Combing two different tapes on the same layer is currently not feasible due to lack of funds for equipment development.

The processing of the new dielectric ring coil transformers is shown in figure 33. The thick film silver conducting paste is printed on dielectric tape layers as would be done in the tradition LTCC process on ferrite tape. The dielectric ring coil structures are routed around the coil perimeter and in the center for central transformer core. The ferrite end cap has a pocket routed out so that the coil structure can be dropped in. The first attempt at this structure had the central core part of one of the end cap layers routed at the same time. A layer of dielectric tape was put in the routed end cap layer and thus goes across the whole part (gap is not just in the center transformer leg). In later design and process variations, the stack up and part count varies.

4.3.2. First Attempt – D50E Transformer

The first attempt at the dielectric ring coil transformer process mostly used existing print screens for the D50E transformer. Although this was not optimal for the new process, it presented an inexpensive way to obtain quick results to see if the proposed process was workable. The system used the first batch of dielectric and low binder content ferrite tapes. Cross-section of the D50E ring coil transformer is shown in figure 34. Note that there is large crack at the dielectric coil/ferrite interface at the center leg region. This cracking severely limits the output performance because it increases the effective gap of the structure and will be the focus of further process development described in later sections.

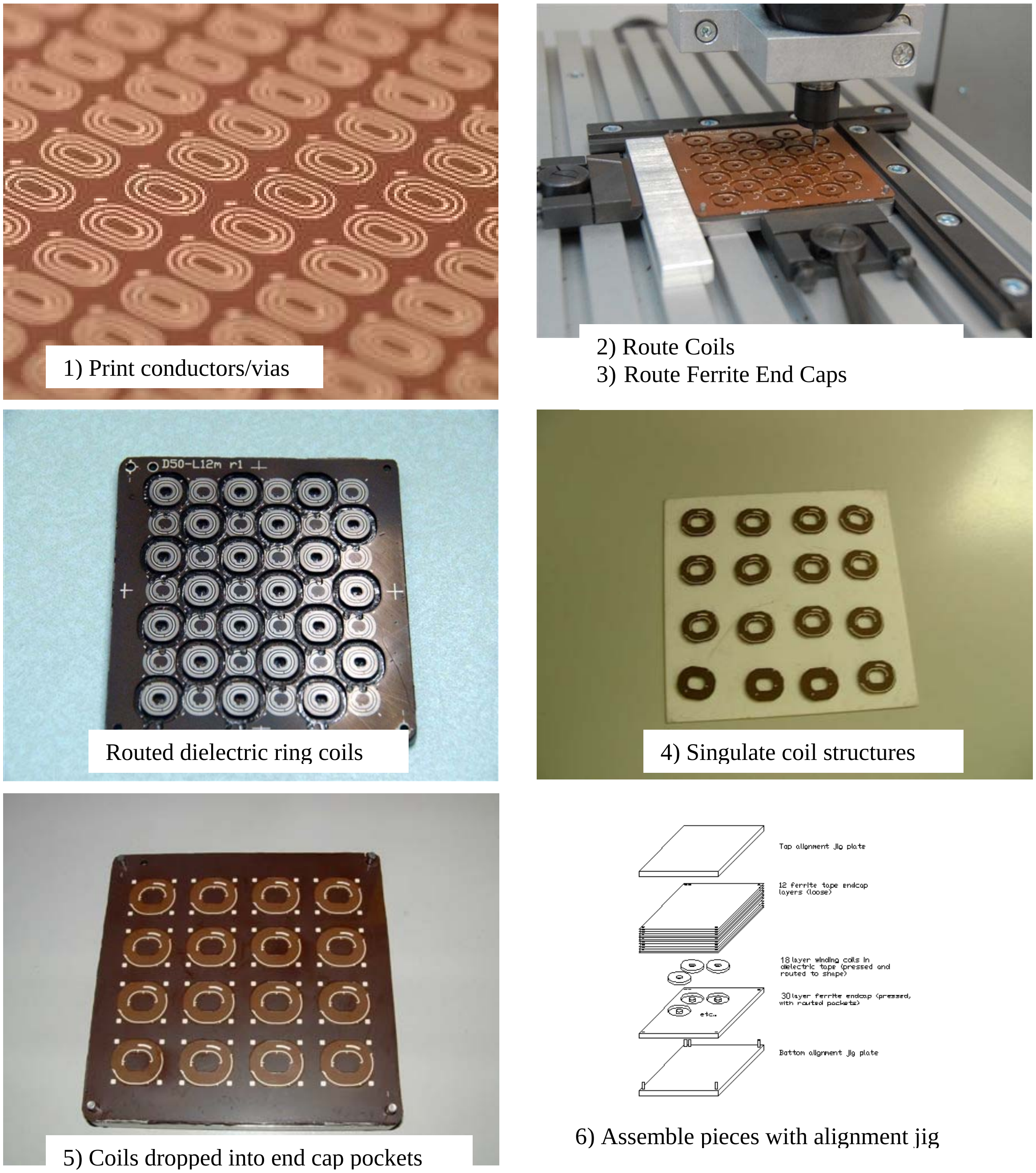


Figure 33. Basic process for the dielectric ring coil transformer.

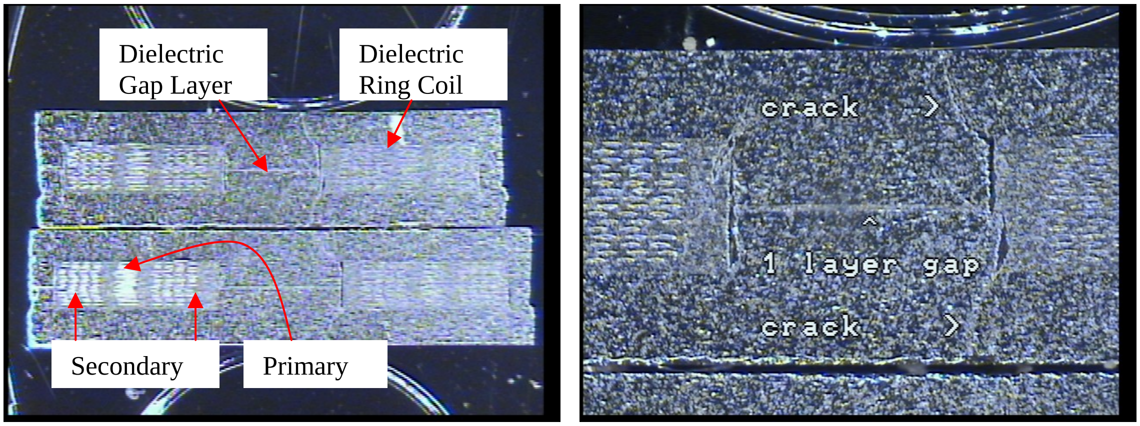


Figure 34. D50E dielectric ring coil transformer cross-section.

The parameter data for the D50 dielectric ring coil transformers is given in table 8 and the output charts are in figure 35. As the data clearly shows, working transformers have been produced using this new fabrication process. The coupling factor was not as high as predicted by modeling and this believed to be due to the internal cracks at the dielectric/ferrite interface at the center leg. The outputs are lower and there are earlier saturation effects than the standard D50E transformer, but it is clear that this process should be continued to be studied.

Table 8. D50 dielectric ring coil transformer measured parameters.

Build – D50E	L_p (µH)	L_s (mH)	L_{lp} (µH)	Rp (Ω)	Rs (Ω)	k
2354Y (16W, 1G, 42L)	24.80	1.33	3.40	1.18	28.30	0.93

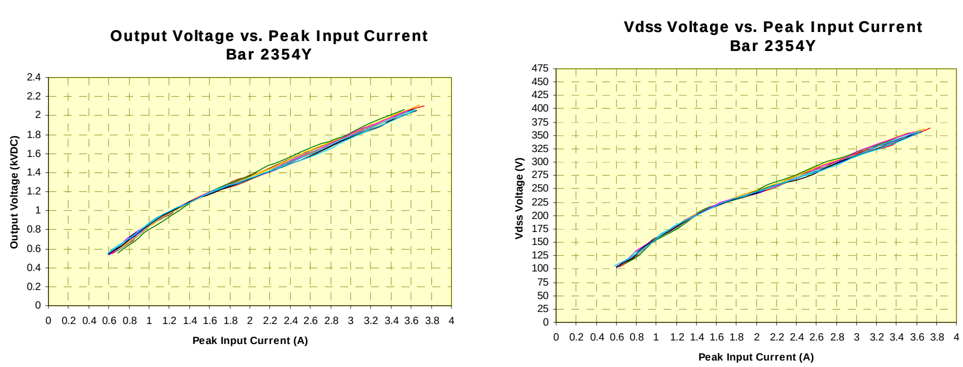


Figure 35. D50E dielectric ring coil transformer charts.

4.3.3. Second Attempt – D50E Transformer

The results from the first attempt above demonstrated the importance of resolving the internal central cracking issue to increase coupling/lowering leakages. It was thought that by increasing the end cap layer count, that equalization of the lamination pressure would be increased thus reducing stress cracks at the dielectric/ferrite interface. It was also thought that the increased end cap thickness would reduce the saturation affects there, increasing output potential for a given input current. A shallower pocket for the ring coil was also tried as this might reduce the internal stresses. The total layer count was increased to 88 thus requiring the use of a router for singulation. This used a 53 layer end cap layer structure for the dielectric coil with a dielectric tape at layer 44 for the gap. The final end cap had 35 layers of ferrite. This system used the original dielectric tape and low binder ferrite tapes. Two different firing profiles were used based on previous work on a 75 layer part and the current D51 studies.

Due to the thickness of the parts, all of the parts were nonfunctional as transformers. A few parts did have continuous primary coils. Pictures of the samples are shown in figure 36. The D51

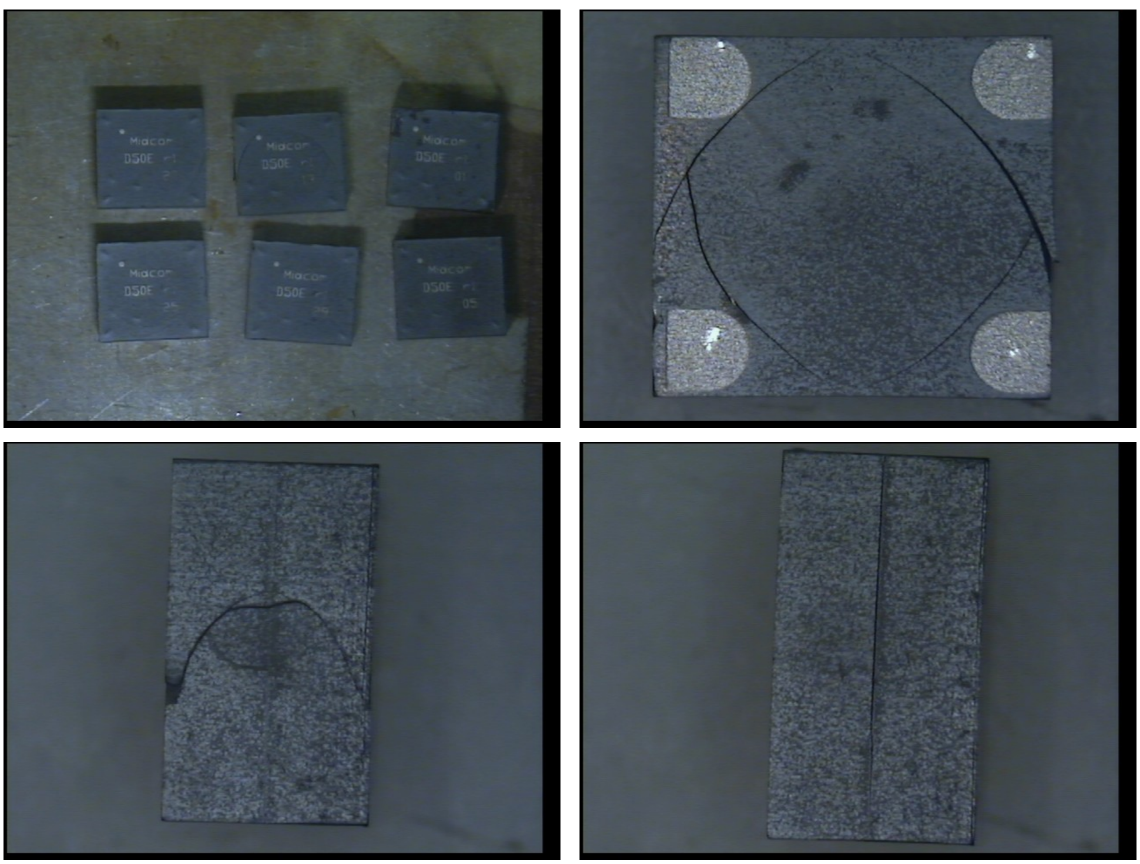


Figure 36. Thicker D50E dielectric ring coil transformer pictures showing cracks.

based profile demonstrated lesser cracking than the other. This indicates that more profile development might reduce cracking further. The severe cracking also shows that improvements in material shrinkage are needed and was the driver for the work on the dielectric and ferrite tapes described above.

4.3.4. First Attempt - D51G Transformer

The D51G was chosen since it has previously shown the highest output capability. This transformer build uses the original dielectric tape with the higher binder content ferrite tape. The thickness was reduced to 56 layers from 88 based on the thick D50E results. It is believed the cracking is due to the difficulty of removing organics out of thick parts, which leads to internal pressure buildup. All new artwork was designed to optimize yield for using the routing method which requires thicker cutting lanes than the traditional Guillotine method. The routed end cap (with pocket) is 37 layers with one layer of dielectric tape at layer 28 for the gap. The other end cap is 19 layers of ferrite.

Figure 37 shows photos of cracking experienced with most of the transformers post-firing. The routing of the green panels left very clean and neat edges which should decrease edge stresses which would be present in cutting thick parts. It is clearly evident that there are stresses formed at the dielectric ring coil and center post interface as there are concentric cracks that follow that outline. The cracking appears to be less than the D50E samples because of thinner parts and the higher binder content ferrite tape. This tape would be more pliable and flow better around the coil structure. Table 9 shows the measured parameter data for this transformer. Performance charts of the transformers are shown in figure 38. Note that the parts are similar in performance to the samples that have center gap and margin gap (2383Y, see section 2.2.2). However, around 1.4 A, the paste based design does better. The lower leakage inductance dielectric ring coil compared to the traditional planar LTCC D51G design performance is evident in the lower voltage stress for the same output voltage. The coupling factor was significantly increased compared to traditional LTCC processing and could be higher if cracking is minimized. There is also evidence of output fold back where the voltage decreases with decreasing current from higher voltages. The mechanism for this is unknown but one hypothesis is that the insulation resistance is changing because of heat buildup (increased temperature) or an unknown high voltage effect.

Table 9. Measured first attempt D51G dielectric ring coil parameters.

Build – D51G	L_p (μH)	L_s (mH)	L_{lp} (μH)	Rp (Ω)	Rs (Ω)	k
2421Y (18W, 1G, 56L)	80.15	4.44	8.45	1.41	54.29	0.94

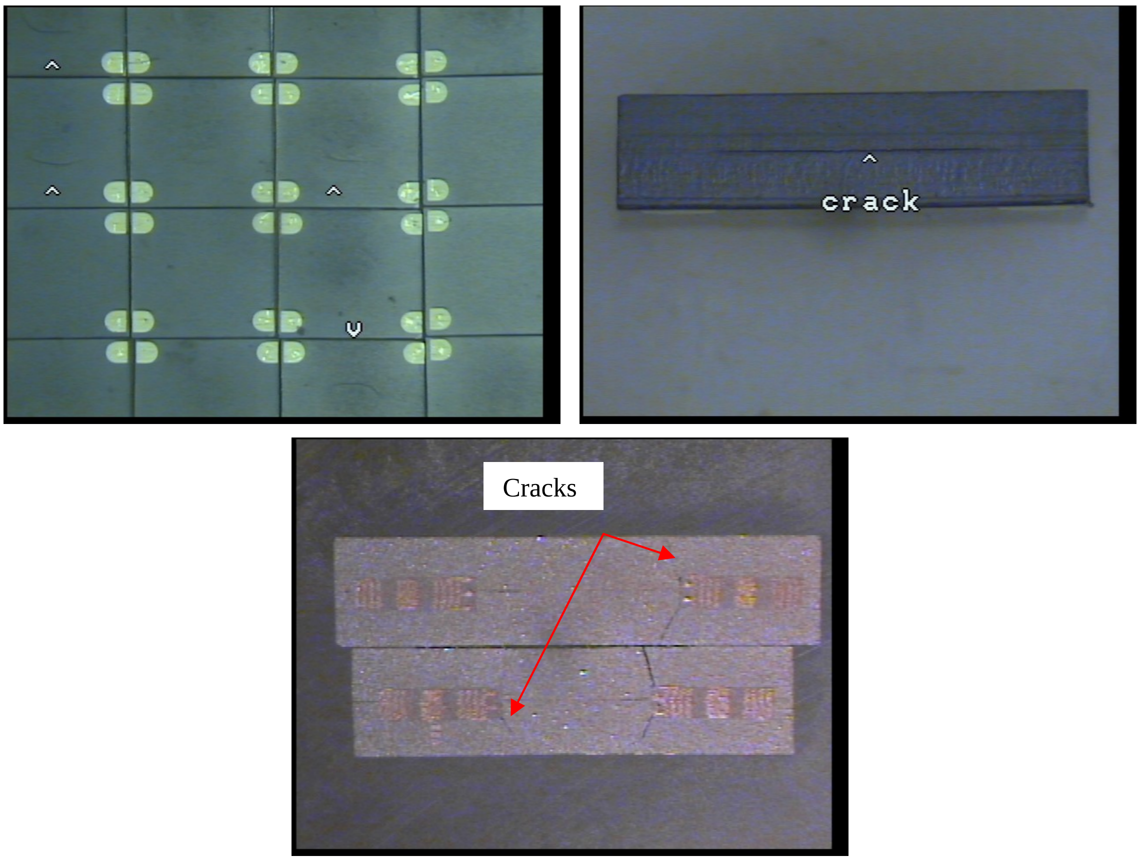


Figure 37. First attempt D51G transformer photos crack patterns.

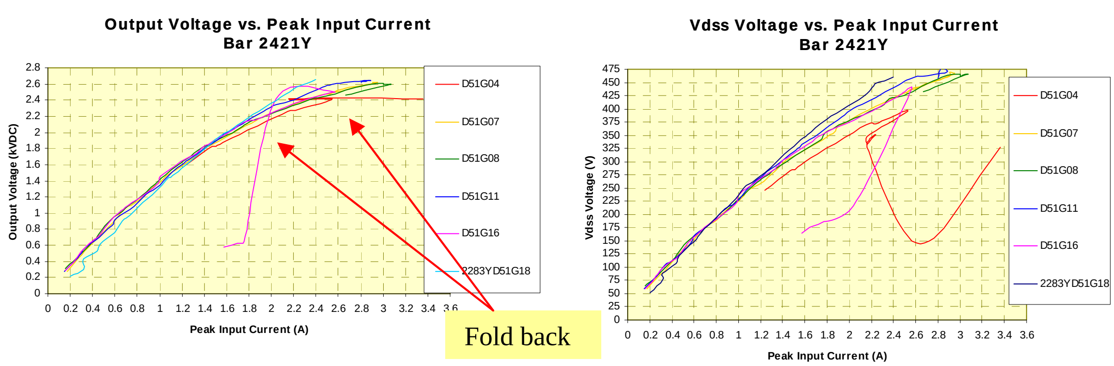


Figure 38. First attempt D51G dielectric ring coil charts.

4.3.5. D51G Transformer with Improved Dielectric and Ferrite Tapes

This set of D51G ring coil transformers used both the lower binder dielectric and high binder ferrite tapes described in section 4.2.2. In addition, a second dielectric gap layer was used throughout the parts in order to try and increase the saturation level as previous data appears to show relatively early saturation effects.

The post fire results are similar to the crack patters observed in section 4.3.4, concentric cracks with internal cracks at the center post/dielectric coil interface. These parts had more cracks then the first build and upon review of the firing conditions it was noted that the airflow was lower than before. This might have contributed to the increased cracking since the rate of organic removal would have been lower. Table 10 lists the parameters for these parts and figure 39 shows the output characteristics. The added gap layer and increased cracking lowered the primary inductance which contributed to the lower output compared to the previous batch. Output roll-off was not seen as in the first batch since the added gap thickness pushed out the saturation point.

Table 10. D51G parameters with improved dielectric and ferrite tapes.

Build – D51G	L_p (μH)	L_s (mH)	L_{lp} (μH)	Rp (Ω)	Rs (Ω)	k
2464Y (18W, 2G, 56L)	49.41	2.63	7.17	1.35	45.68	0.92

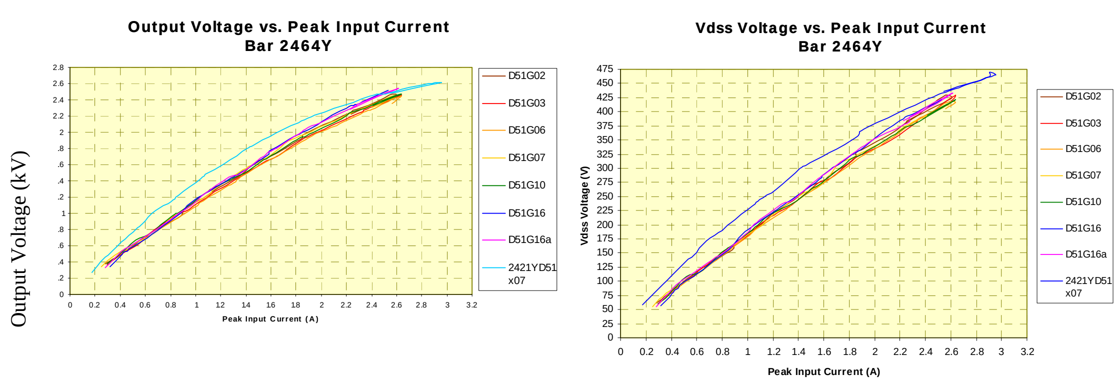


Figure 39. D51G improved dielectric/ferrite tapes output charts.

In order to see if the increased cracking seen on bar 2464 was due to the lower airflow during firing or the new dielectric/ferrite binder content tapes, the same process was done with a high airflow. The results were quite similar to that in table 10 and figure 39. The amount of cracking particularly at the edge was reduced, although still higher then the samples prepared in section 4.3.4 with the first batch of dielectric tape and high binder content ferrite tape.

After these first prototypes of D51G dielectric ring coil transformers, a number of possible sources of cracking are hypothesized. First, a tight fitting coil structure could be causing stress in the ferrite. Second, stress from a height mismatch between the routed coil and routed coil pocket in the ferrite end cap leading to stress during pressing. Third, any voids left during pressing cause a stress initiation site. Fourth, movement during the pressing step and release and cool down after force removal maybe causing small internal cracks that extend during firing. Fifth, the ferrite regions tend to shrink the most because of still slightly mismatched tapes. Some of these issue are investigated in the following sections.

4.3.6. D51G with Loose Routed Coil Pockets

As mentioned above, one hypothesis for internal stress crack formation is the tight fitting ring coil in the routed ferrite pocket. This sample uses the same stack up and process as the previous build but has an extra 3 mils of clearance to try and eliminate stress points. Pictures of the cross-sectioned are in figure 40.

The electrical performance is the same with previous builds. Test results indicate that there are more electrical opens than the previous builds. This could be due to increased coil misalignments due to the loose pocket design preventing the winding vias from connecting with the catch pads on the end cap. Additionally, the loose pockets did not make a difference in the cracking seen, so the loose pocket design might not be necessary. Cracking in the center region (ferrite) and appears to be pulling away from the dielectric material because of the increased ferrite shrinkage. Previous LTCC work has shown cracking similar to that seen with the dielectric ring coil but at the coil ends when no dielectric paste was used in the center area. This could indicate that dielectric paste might be required for the gaps to act as a moderator between shrinkage amounts. This could also eliminate some side splitting because of the dielectric tape gap layer which is through the whole part.

4.3.7. D51G with Separate Center Slug, Coil and Ferrite End caps

This part configuration looks to relieve stress built up during stack up and pressing by creating a separate center slug instead of having it routed out during the routed coil pocket process. The hypothesis is that by letting the center slug be unconstrained, that the part will be able to relieve

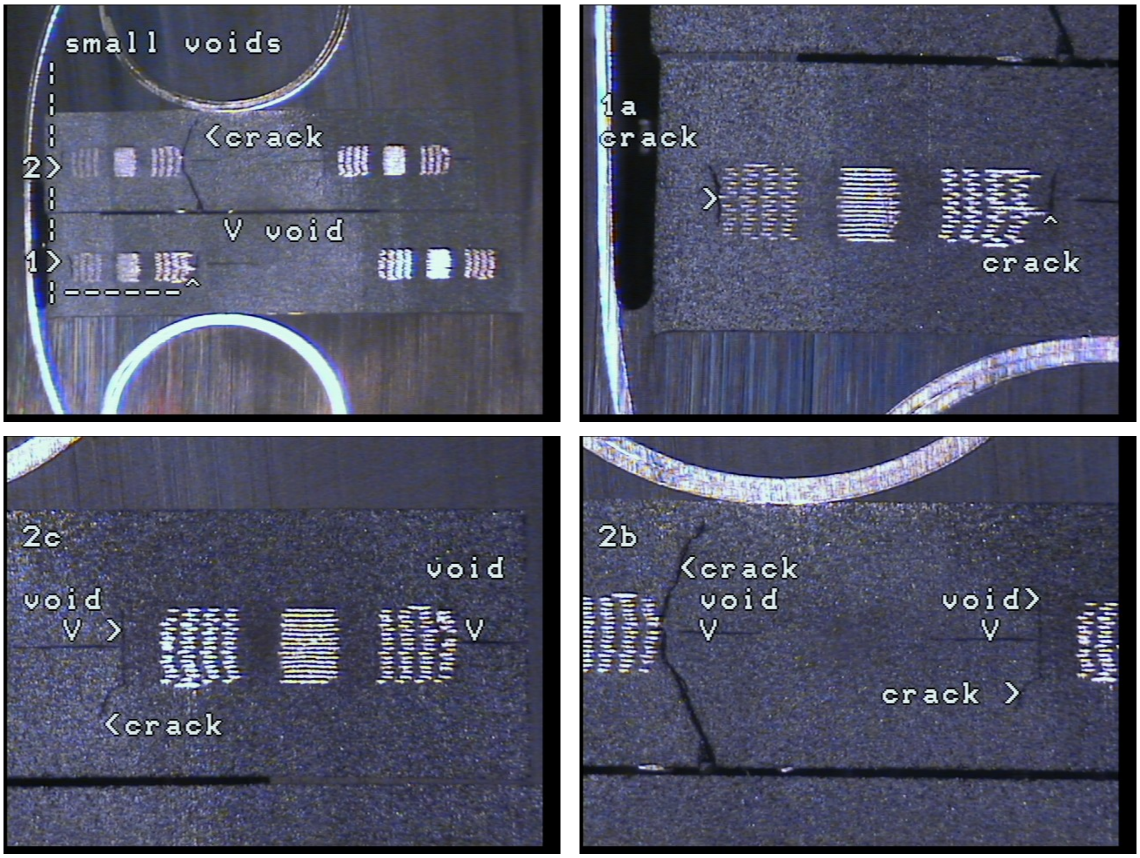


Figure 40. D51G with loose ring coil/routed pocket interface.

the stresses that build up. These parts will also go back to use the tight fitting coil by making all the layer counts match. A stack up diagram and picture of the center slugs are shown in figure 41.

The results for these samples are the same in that the amount of cracking has not been reduced from the previous builds. The process of re-pressing all the parts as a unit and the reversal to a tight fitting coil structure has reduced voiding at the coil edges. The electrical performance was similar to previous builds.

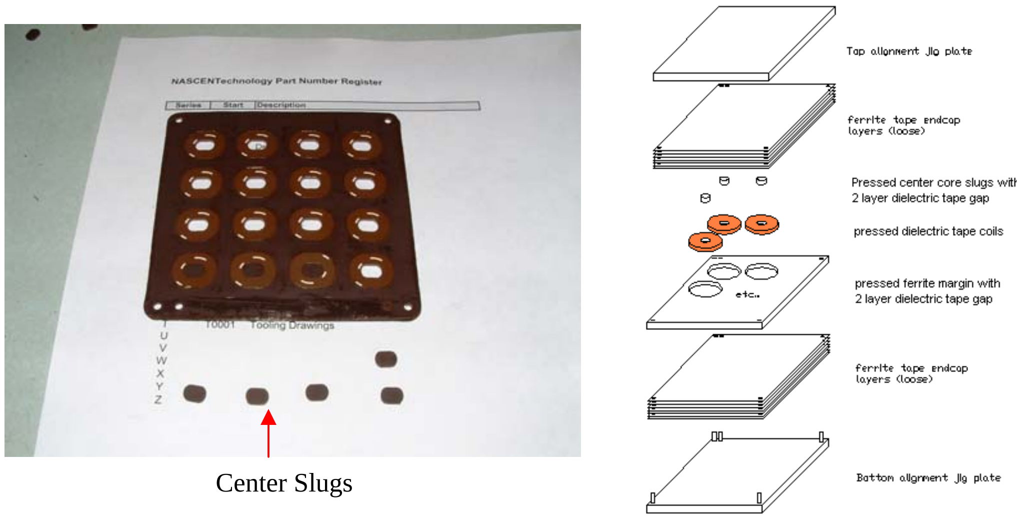


Figure 41. Center slugs and stack up diagram showing separate center slugs.

4.3.8. D51G with Coil, Ferrite End caps and Paste Gaps

The last process change tried in order to reduce cracks at the center slug/dielectric coil interface was the use of dielectric paste printed on 16 layers. The paste was used just in the center slug with no gap extending out to the edge of the part. The hypothesis is that the dielectric paste should moderate the shrinkage rate of the center slug ferrite to be closer to the dielectric ring coil thus hopefully reducing cracking. These parts had the center slug attached to the end cap (no separate center slug as described in section 4.3.7.

The cracking in these parts was still the same as previous builds. As figure 42 shows, there is a visible bump in the central region of the end caps. This is believed to be due to large voids created because of delamination near the loose end cap (without the central slug) as shown in figure 43. There was a small amount of edge cracking which was probably due to the lack of a dielectric paste layer to the outside edge. Electrical performance is the same as the previous D51G builds although the coupling factor was higher. This was mainly due to an increase in primary inductance since the leakage inductance was essentially the same.

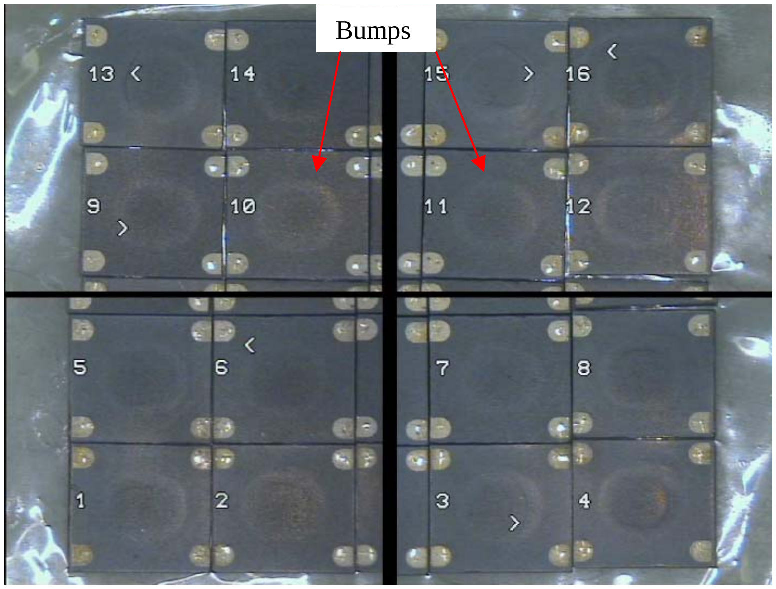


Figure 42. Bumps caused by large voids due to delamination.

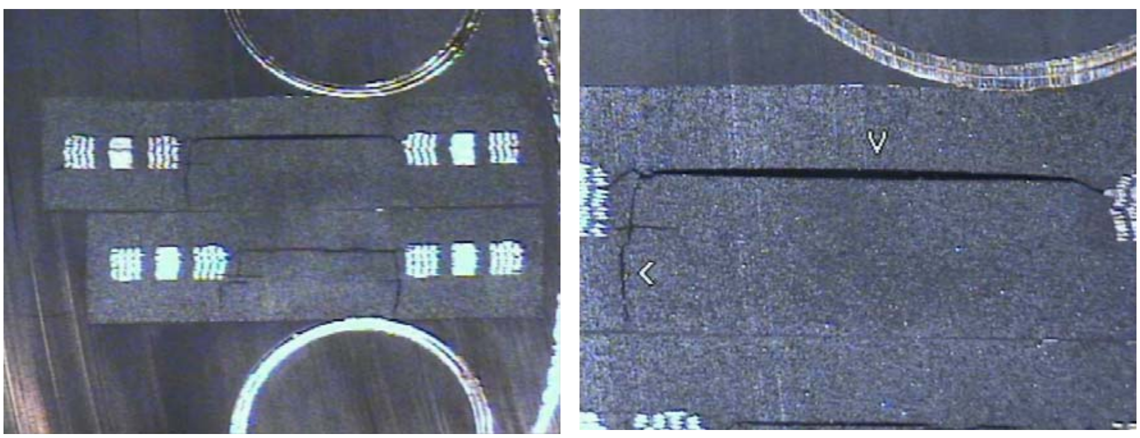


Figure 43. Cracks caused by delamination.

Another batch of panels was made using the same process but with high airflow during firing with the result being a reduction in end cap cracks. Edge cracking disappeared in this run compared to the first, due to the increased efficiency of organic removal from the structures. Electrical performance was essential the same as the first panel in this group which had higher primary inductance thus giving a higher coupling factor.

4.3.9. D51G with 1:9 Turn Ratio. All Separate Pieces

This panel was originally to be designed with 18 printed dielectric paste layers but the first two panels yielded no continuity even after revising screens to relax connection tolerances. A third panel was tried with 8 printed dielectric paste gap layers with some success.

Cracking did not seem to improve for this build and is comparable to previous builds. Electrically, the performance was similar to the previous builds with slightly lower voltage stress because of the increased turns ratio. The measured parameters are in table 11 and the output charts are in figure 44.

Table 11. D51G with 1:9 Turn ratio.

Build – D51G	L_p (μH)	L_s (mH)	L_{lp} (μH)	Rp (Ω)	Rs (Ω)	K
2712Y (18W, 8G, 56L)	139.49	10.76	7.92	1.28	54.78	0.97

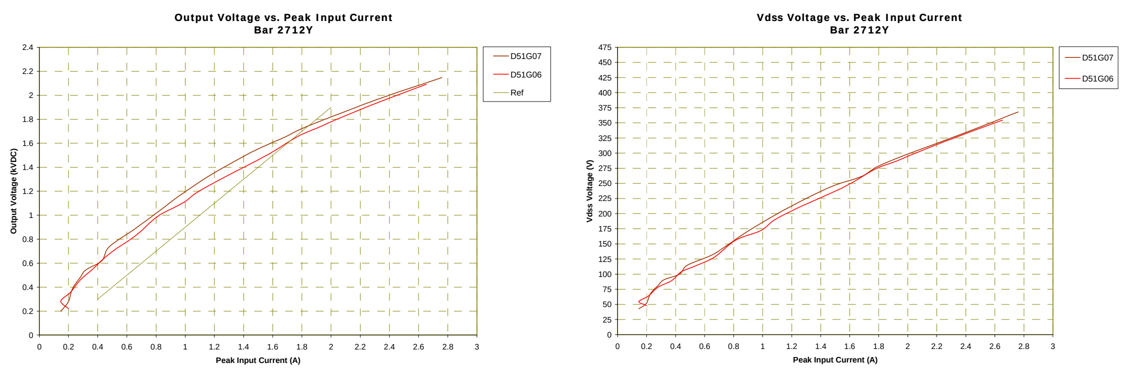
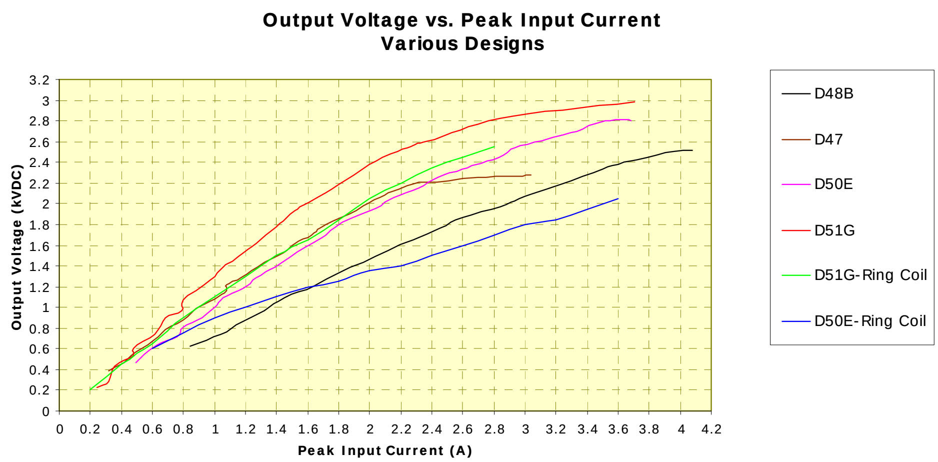


Figure 44. D51G 1:9 turn ratio output charts.

4.4. Dielectric Ring Coil Transformer Summary

The dielectric ring coil planar LTCC transformer has been shown to be possible to fabricate. Comparison of the dielectric ring coil and the traditional dielectric paste designs are shown in figure 45. The dielectric ring coil designs had lower outputs than their dielectric paste based design counterparts. For voltage stress for a given output voltage, the D50E dielectric ring coil was worse even though the leakage inductance was lower, while for the D51G was better for a lower leakage inductance. This discrepancy for the D50E case is that the voltage output for the same currents is much lower for the dielectric ring coil case. Since the leakage spike amplitude is proportional to the current, the voltage stress is dominated by it even though the contribution from the reflected output voltage is lower. The reason for the much lower output voltage for the D50E dielectric coil design is the lower primary inductance due to the removal of magnetic material in the winding window area and smaller ferrite central core. For the D51 size, this removal did not have a large an effect in comparison to the D50 size. The coupling factors are higher than both traditional process transformers described in the previous work and the larger ones in described in this report. These coupling factors are due to significant reductions in the leakage inductances because of the removal of magnetic material in the winding window area.



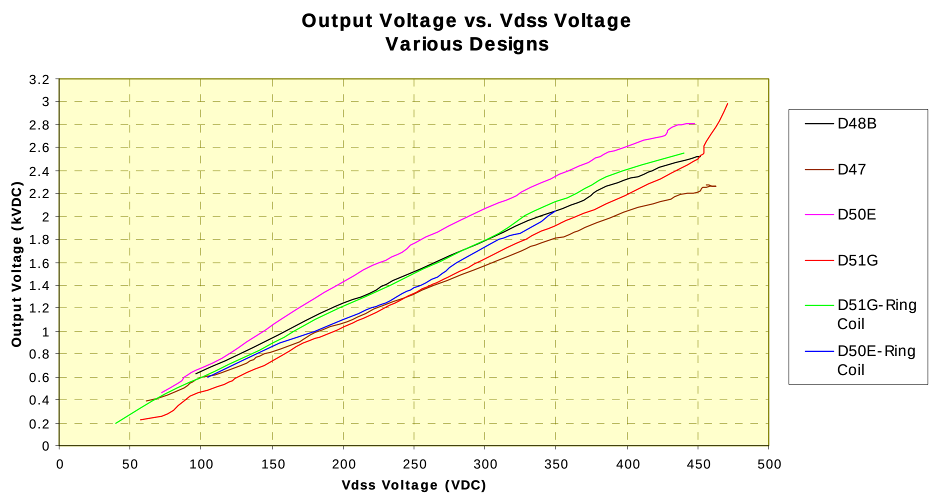


Figure 45. Dielectric ring coil and traditional LTCC transformer comparison.

There is still some work that can be done to further the design and knowledge of the dielectric ring coil transformer process and design and are is follows:

1. Optimize burnout profile using mock up bars.
2. Press parts in a well fitted design to improve tolerances.
3. Consider firing the coil structure separate from the core.
4. Study end cap thickness on cracking.
5. Use a separate pressed ferrite end margin with routed holes for the coil. Use with loose end cap layers.
6. Determine an optimum balance between dielectric tape/paste.
7. Try isostatic lamination to improve stress uniformity.
8. Develop processing of thicker parts to thicken end caps and winding window area.

5. Conclusions

The high voltage flyback planar transformer work started 5 years ago for DoD applications requiring output voltages of 1200 to 1500 V. Along the way, interest in transformers that could reach outputs of 2 kV, 3 kV and higher have driven design exploration and the limits of the traditional LTCC process developed by NASCENTechnology, Inc. In order to reach these higher voltages, larger parts will be needed. This involves process optimization for scaling from the existing smaller designs and possible new processes for radically different designs. One such novel design proposed in this report was the dielectric ring coil planar LTCC transformer. Simply scaling the existing smaller designs (D50 to D51) demonstrated higher voltage outputs with higher voltage stress per given output. But this is a tradeoff that must be considered for given application requirements.

The novel dielectric ring coil transformer has shown promise although it still in the prototype stage. For the D51 design, the voltage stress was lower for a given output voltage even though the drive current was higher for the dielectric coil design in comparison to the paste based design. This is a testament to much lower leakage inductance inherent to the novel design. It is not yet known if (with further process development), this concept can be taken full scale production. A list of recommendations has been given that should be considered if further interest and need develop.

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