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Abstract

Microfabrication methods have been applied to the fabrication of wire arrays suitable for use in Z. Self-curling GaAs/AlGaAs supports were fabricated as an initial route to make small wire arrays (4mm diameter). A strain relief structure that could be integrated with the wire was designed to allow displacements of the anode/cathode connections in Z. Electroplated gold wire arrays with integrated anode/cathode bus connections were found to be sufficiently robust to allow direct handling. Platinum and copper plating processes were also investigated. A process to fabricate wire arrays on any substrate with wire thickness up to 35 microns was developed. Methods to handle and mount these arrays were developed. Fabrication of wire arrays of 20mm diameter was demonstrated, and the path to 40mm array fabrication is clear. With some final investment to show array mounting into Z hardware, the entire process to produce a microfabricated wire array will have been demonstrated.

[1] Lmata Government Services
[2] Ktech Corporation

CONTENTS

FIGURES

1. INTRODUCTION

Most simply stated, the Z-machine ("Z") is a tool to deliver a fast, high-current pulse to a load. That load can take on several different forms for research on a variety of topics, such as z-pinch plasma physics and instabilities [1], material equation-of-state [2], and inertial confinement fusion [3]. For generation of intense pulses of x-rays, it was found that a Z-machine load consisting of a cylindrical array of wires is particularly effective [4]. An example of such an array is shown in Figure 1. These arrays are fabricated by manually stringing on the order of 10^2 wires over a machined mandrel. Weights on the ends of the wire serve to keep the wires taut and in their respective slots.

This wire array construction method is time-consuming and limited in geometrical structure complexity. The materials available are limited to those that can be drawn to fine wires and handled. Typical examples are tungsten and aluminum. Some materials which can be drawn to fine wires (e.g. gold), are too fragile to handle in wire form. There are conceptual experiments on Z that would benefit from a wider selection of materials for the wire material to tailor the x-ray spectrum and allow plasma diagnostics. There are also experiments that could investigate stabilization of the z-pinch implosion through geometrically structured targets. For example, a spherical implosion can be approximated using a cylindrical geometry with the mass density tailored along the radial axis. Furthermore, if a z-pinch driven fusion reactor was to be developed, it would require the production of large numbers of wire arrays at low cost.

This project addresses these problems by using planar microfabrication techniques followed by MEMS-like release of a structural handle layer to produce wire arrays to be used as loads for z-pinches. This report details the development effort chronologically. The first efforts were aimed at fabrication on semiconductor supports. The design procedure and process flow for these self-shaping structures is described. Four-millimeter diameter semiconductor supports are demonstrated. Next the development of plating processes is detailed. These processes are adapted to allow wire array fabrication without the most expensive part of the original proposal – the semiconductor support. Finally, the production of large (40mm diameter) wire arrays is demonstrated. The remaining challenges to implementation of these wire arrays for testing are described.

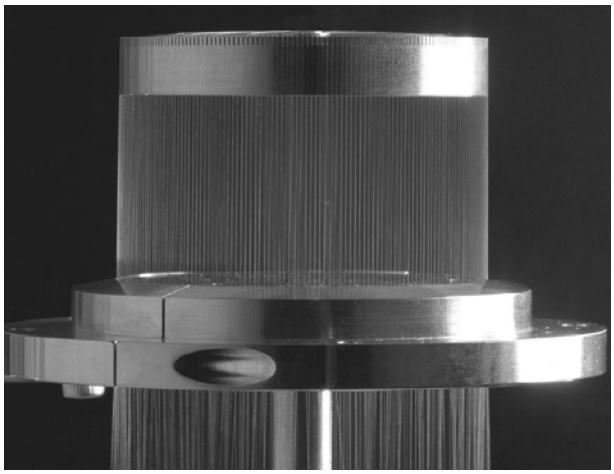

Figure 1. A photograph of a 4-cm diameter tungsten wire array with 240, 7.5 micron diameter wires. From [4].

2. RESULTS

The initial proposal concept used the following process flow. First a metal structure of the desired geometry is deposited on a substrate. This defines the axial and radial mass distribution and composition of the final wire array. This metal structure in its most simple form would be a set of parallel wires connected by a common anode bus on one side and a common cathode bus on the other. The substrate is of a particular structure – it has a surface layer ("the semiconductor support") that has a built-in strain gradient, above a sacrificial etch layer. Following the metal deposition, the semiconductor support is etched away around the edges of the wire array to expose the sacrifical etch layer. The sacrificial layer is selectively etched laterally to release the combination semiconductor support/wire array. These are handled as a unit and mounted on a support mandrel. Finally, the semiconductor support is etched away from the metal, leaving the wire array on the mandrel.

This proposed process flow led to the first year milestones:

1. Downselect metal technology: sputtered tungsten, molded tungsten, or other metal
2. Strain-relief wire designs demonstrated to accommodate 50 micron axial displacements on a 1-cm-length wire without wire buckling
3. Demonstrate free-standing GaAs support cylinder and characterize cylindrical symmetry

These three milestones are addressed in the following sections.

2.1. Metal Deposition Technology Selection

Selection of a metal deposition technology depends critically on the composition, processing and property requirements of the film to be deposited. For compatibility with microfabrication, there are a set of well-established methods, primarily classified as:

1. CVD
2. Evaporation
3. Sputtering
4. Electroplating

We examined each of these methods for applicability to this project, taking into account the anticipated process flow and material interactions during processing.

2.1.1 Chemical Vapor Deposition (CVD)

Chemical vapor deposition (CVD) is a well-established method to deposit thin films of certain materials. In particular, tungsten has a convenient precursor chemical – WF_6. This allows conformal deposition of tungsten films over various patterned structures. The conformal nature (and elevated temperature) of the deposition means the film would have to be blanket deposited and etched in order to form the wire array. Fortunately, tungsten can also be easily dry-etched with high aspect ratios and good selectivity. The current use of tungsten in manually assembled wire arrays made this an attractive option. On the other hand, the deposited metal is known to have extremely high residual stress levels. Tungsten films are likely to peel from the substrate during deposition, and would crumple the semiconductor support layer after release.

Furthermore, CVD (and dry etch capability) for other metals is less available. For these reasons, CVD was not selected as a primary deposition technique for microfabricated wire arrays.

2.1.2. Evaporation

Evaporation (electron-beam or thermal resistance) addresses the lack of flexibility of CVD deposition. Any metal can be evaporated onto the substrate, including very low vapor pressure elements like tungsten. In addition, the directional nature of deposition allows direct patterning of the metal film through the lift-off metallization technique. Therefore, there is no need to develop etching methods for the metal films. There are three main drawbacks. First, the material utilization rate is very low. The area of material used – the substrate area – is only a very small fraction of the total area coated. For precious metals, this inefficiency means very high cost for films deposited by this method. The second problem is lack of stress control. If an as-deposited film is found to be under a high stress level, there are very few parameters that can be adjusted to reduce the stress level. Finally, the deposition rate is relatively slow, so that deposition of thick films (> 1 micron) is not practical.

2.1.3. Sputtering

Even more materials are amenable to deposition by sputtering than evaporation. Sputtering particularly excels at deposition of alloys. It also allows tuning of the stress level by adjusting the bias, pressure, temperature, and power. The material efficiency is substantially better than evaporation. However, it likewise suffers from relatively low deposition rates that limit the total thickness that can be deposited. Also, as a conformal deposition technique, metal etch techniques would have to be developed.

2.1.4. Electroplating

Plating of metals is the final class of deposition techniques. It wins over plating and sputtering for two primary reasons: the plating rate can be relatively high (several microns/hour) and the stress can be controlled through chemistry, temperature, and bias. The main drawback is that the development of new plating materials is a difficult process. Fortunately, numerous plating chemistries have been developed over decades thanks to the high commercial application of plated films. It was concluded that electroplating offers the most flexibility and easiest path to demonstration of the wire array. More complex wire structures may select other methods or combinations of methods to generate compositionally-tailored wire arrays.

2.2. Strain-relief wire designs

The manually assembled wire array shown in Figure 1 has the advantage that its wires contact the anode and cathode simply by physically lying in positioning slots. While this means the electrical contact between the wires and the anode/cathode may not be as reliable, it does allow the wires to slip within their slots if there are relative displacements of the anode and cathode connections. In fact, such displacements do occur during the evacuation of the Z experimental chamber. The anode and cathode connections are cantilevered from the edges of the vacuum

vessel and are known to move on the order of 50-100 microns further apart as the chamber is evacuated. Therefore, one advantage of the proposed design for microfabricated wire arrays - solid connections to the anode and cathode through an integrated bus connection - must be engineered to allow for this displacement.

ANSYS finite-element mechanical modeling software was used to examine the possibility of designing a spring that could be fabricated in-line with each wire to absorb the anode-cathode displacement while keeping the stress on the wire below the yield strength. The problem was posed as follows: design a minimum-stress planar thin-film spring with a width (direction perpendicular to applied force) of less than the array wire pitch of 420 μm.

Analysis was performed on a "unit cell" spring that may be duplicated along the length of the available "spring region" in the microfabricated array. Only designs symmetric about the wire axis were considered. Simple hairpin designs with 17.5 μm (in-plane) x 31 μm (out-of-plane) cross-sections were considered, because this wire dimension is consistent with the mass loading required for Z assuming the material is gold with a density of 19.3 g/cm^3. A more complicated serpentine design was also considered.

Hairpin designs with smaller turn radii were found to produce lower maximum stress for equivalent cell strain. This suggests that the smallest turn radius compatible with the desired spring wire spacing should be used. Variations on the simple hairpin design using non-uniform wire cross-sections at turns did not yield improvements. A serpentine design was shown to result in approximately 20% lower maximum stress than a similarly-sized simple hairpin design, but at the expense of considerably greater mask layout difficulty.

The use of lateral ties between the necks of springs on adjacent wires should be considered to provide some stability against lateral and torsional distortions of the spring arrays. Since spring length occupied by these ties will reduce the number of spring cells that will fit into the allowed array length, consideration should be given both to minimizing the spring neck length added to accommodate these ties and to placing ties less frequently than between every cell.

One plausible design is shown in Figure 2. The material for the calculation is gold with a Young's modulus of 100 GPa and a yield strength of 140 MPa. The displacement at the elastic limit is 1.46 microns. Figure 3 shows the stress distribution when the stress reaches the elastic limit of 140 MPa. Note that this occurs on the inside of the hairpin, while the stress in the wire region is much smaller as seen in the top face of the spring. Allowing some plastic deformation would allow this spring to take up much more displacement. In addition, multiple springs may be stacked to generate more displacement. Since the total length per spring is small (~100 microns in this example), there is no problem with multiple springs in series. They can be placed near the anode or cathode connection next to shielding so the vaporization of the spring material has no effect on the rest of the wire array implosion.

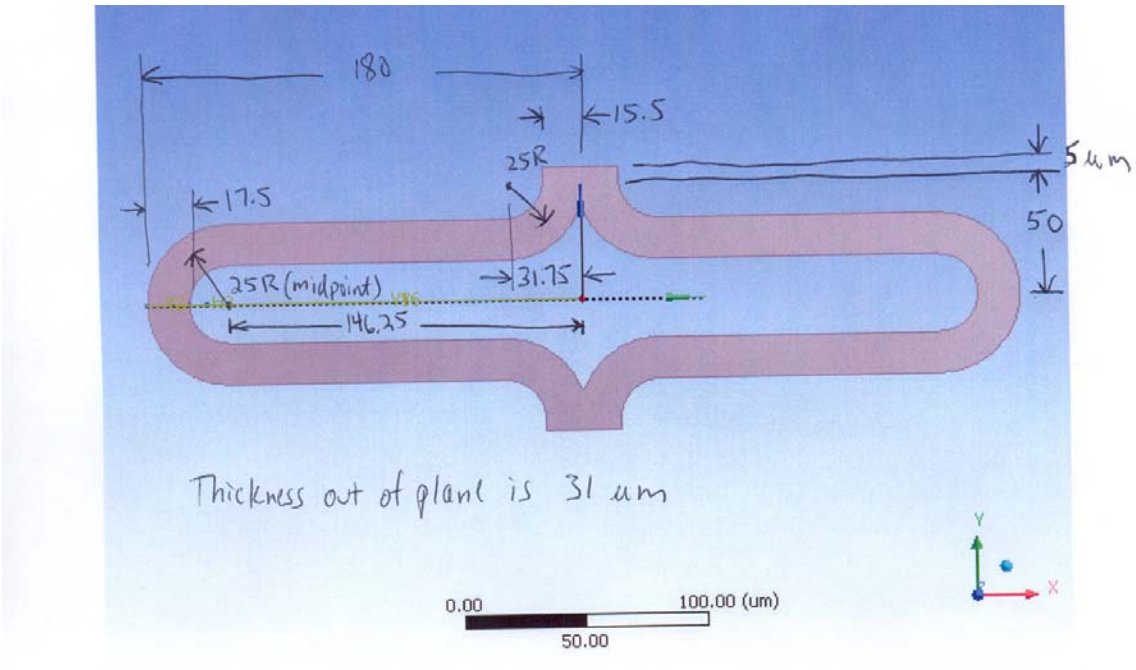

Figure 2. Layout of in-line spring to allow for anode-cathode displacements in Z.

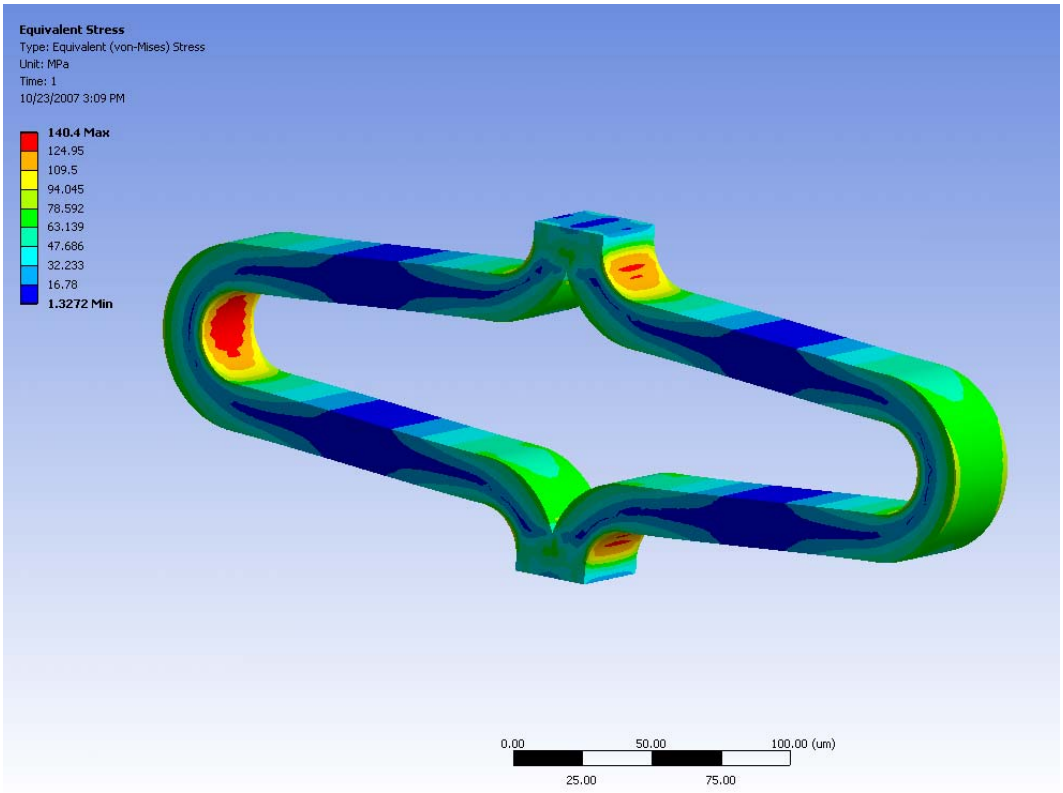

Figure 3. Stress distribution in spring when the elastic limit is reached (1.46 micron displacement).

Confident that a version of this design will serve to accommodate the strains during the loading of Z, this portion of the problem was set aside for inclusion when the remaining portions of the process were well established and scaling to larger arrays was underway.

2.3. GaAs Support Cylinder Characterization

The design of the semiconductor support was based on basic mechanics. A simple spreadsheet was used to implement the equations to calculate the equilibrium radius of curvature of a sheet subject to an internal stress gradient, following the method described in Timoshenko and Young [5]. Note that the stress gradient is the important parameter – any uniform uniaxial, biaxial, shear, or hydrostatic stresses will be relieved after removing the film from the substrate. A number of semiconductor systems and processes could be used to implement this kind of curved design. For example, the stress gradient could be implemented by implanting the surface layer of silicon above a SiO2 release layer in a structure very like that used in standard MEMS. Similarly, a silicon-germanium alloy or metal layer on the surface could supply the stress gradient. However, the most precisely controllable, repeatable, and uniform option is the well-known GaAs-AlGaAs system. The GaAs-AlGaAs alloy system is grown epitaxially on a GaAs substrate. The strain levels are extremely low which match well with the very small strain gradients needed to produce the desired deflections – the lattice constant of AlAs is only 0.13% larger than GaAs. To produce the desired strain gradient, the simplest growth structure consists of a bilayer – a GaAs layer over an AlGaAs layer. Because the AlGaAs has the larger lattice constant, the released structure will peel upward from the substrate, e.g., any surface patterning will the on the inside of the cylinder. This simplifies the removal of the semiconductor support after mounting on the hardware for Z. The free parameters are the GaAs thickness and the AlGaAs thickness and composition. The constraints are that total epitaxial growth much over 10 microns is undesirable, and that the AlGaAs composition should be as low as possible (below 40%) to ensure that it is not attacked during the etching of the underlying sacrificial AlAs layer. Figure 4 shows the calculated radius of curvature when a GaAs/$Al_{0.2}Ga_{0.8}As$ bilayer is released from the substrate. For this calculation the GaAs top layer is 2.5 microns thick. At very small AlGaAs thickness the curvature is small because the amount of AlGaAs providing the strain gradient is small. At the other end of the curve, the radius of curvature again increases. This can be seen as the amount of GaAs providing the strain gradient is small, plus the overall structure is getting stiffer. In the middle is a remarkably wide window of thickness that provides a consistent curvature. This shows the structure can be designed to be very tolerant of growth non-uniformity. By reasonable adjustments of the thicknesses and compositions, any radius of curvature can be obtained from <1mm to >6cm. This covers the full range of Z wire array applications. Other systems (InGaAs/GaAs) have been used elsewhere to generate much tighter curvatures in the sub-micron scale [6].

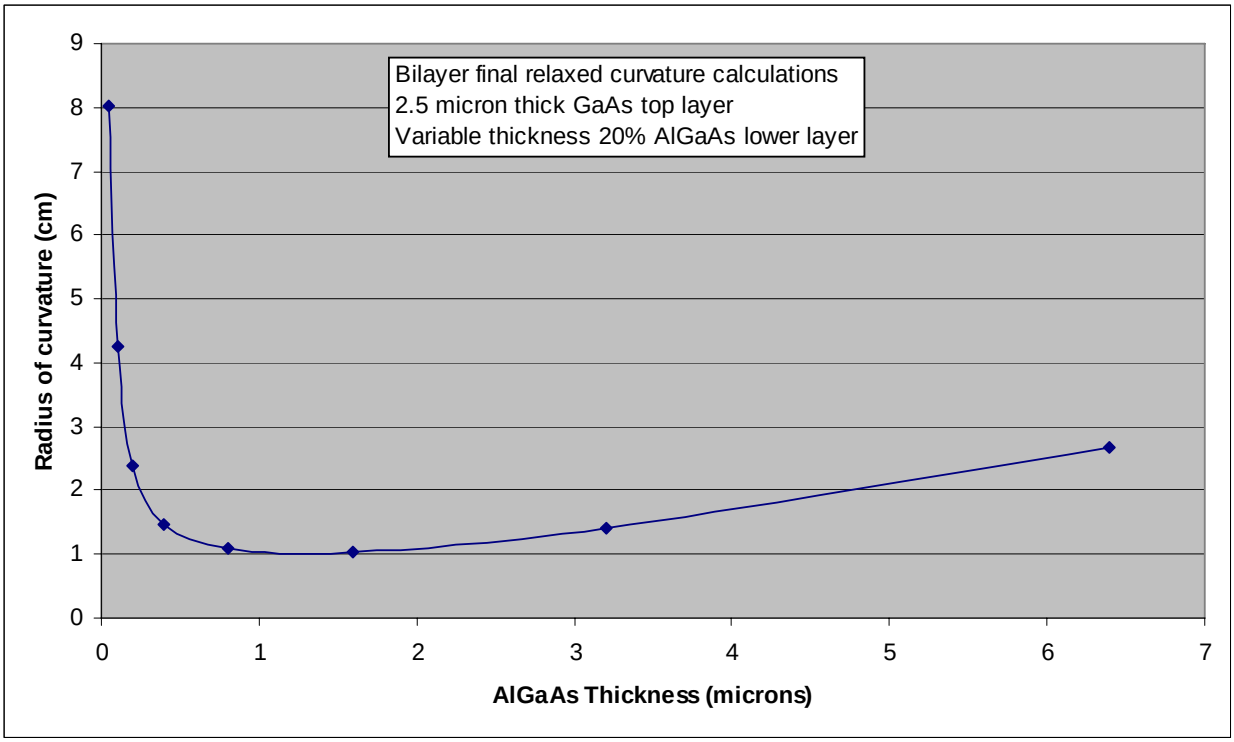

Figure 4. Released cylinder final radius of curvature as a function of AlGaAs thickness in a 2.5 micron GaAs/20%AlGaAs bilayer.

Several variations on the strained AlGaAs/GaAs design were grown and processed to test the fabrication of semiconductor supports prior to integration with metal wires. The key unknown issues were the ease of releasing the large area (order of square centimeter) supports from the substrate and the fragility of the semiconductor supports during handling.

Semiconductor support removal can be classified in three categories: bulk substrate removal (from the bottom), lateral undercut (from the edges), or through release holes (from the top).

From the bottom

The from-the-bottom approach is a brute force approach. After patterning and etching the mesas, the substrate is mounted face-down on a glass puck with wax and mechanically thinned from ~600 microns to 50-75 microns. A polishing step reduces the thickness to ~40 microns. A stream of selective etchant (NH_4OH (20%):H_2O_2 (30%) 1:10 by volume) is directed at the sample backside. The etch rate is ~7 microns/minute depending on the age of the solution and the flow rate. The etch continues until reaching the high-aluminum etch stop, which is clearly indicated by a dramatic change from a shiny to rough, brown surface. The etch stop is removed in 6:1 NH_4F:HF. The semiconductor support then needs to be released from the glass puck. The mounting wax is quickly removed with acetone. Because the designed direction of curvature is such that the front surface of the wafer forms the inside of the cylinder, the edges of the partially released structure are pushing down against the glass puck. This does not seem to cause any serious issues such as limiting the access of the acetone to continue the dissolution of

the mounting wax. The disadvantage of this approach is that it is a time- and material-consuming process.

From the side

This is the standard MEMS-release process for small structures. Following the mesa etch, the sample is immersed in a selective etchant that removes only the release layer. The top film is then removed from the substrate by the complete undercutting of the selective layer, starting at the edges of the mesa. The problem arises that if the structure is large, the etching time becomes very long. Furthermore, the supply of fresh reactant to the etch front through a long, narrow channel becomes very difficult, and the etch slows down further. Finally, there is a large probability of nucleating a bubble under the film. These bubbles can quickly grow and fracture the releasing structure. Therefore, for the large structures to be released in this project, the "from-the-top" method described below is preferred.

From the top

For large-area structures to be released in a reasonable amount of time, etching solely from the edges of the mesa is often not a viable option. To increase the etch rate, release holes can be added to allow the etchant access to the release layer at many locations throughout the structure. Thus, a structure of arbitrary size can be released in a small amount of time, limited by the distance between release holes, constrained only by the dimensional requirements of any structures to be placed on the top surface of the film. The release holes can take on a wide range of configurations and still meet this requirement. However, the chosen release geometry can dictate the final shape of the released structure. For instance, the slotted release holes in Figure 5 effectively turn the long strip into a series of short strips with their long dimensions perpendicular to the original strip. As a result, the structure minimizes its strain energy by curling in the short direction. In contrast, if the release holes are isolated holes as shown in Figure 6, the structure minimizes its energy by curling in the long direction as desired.

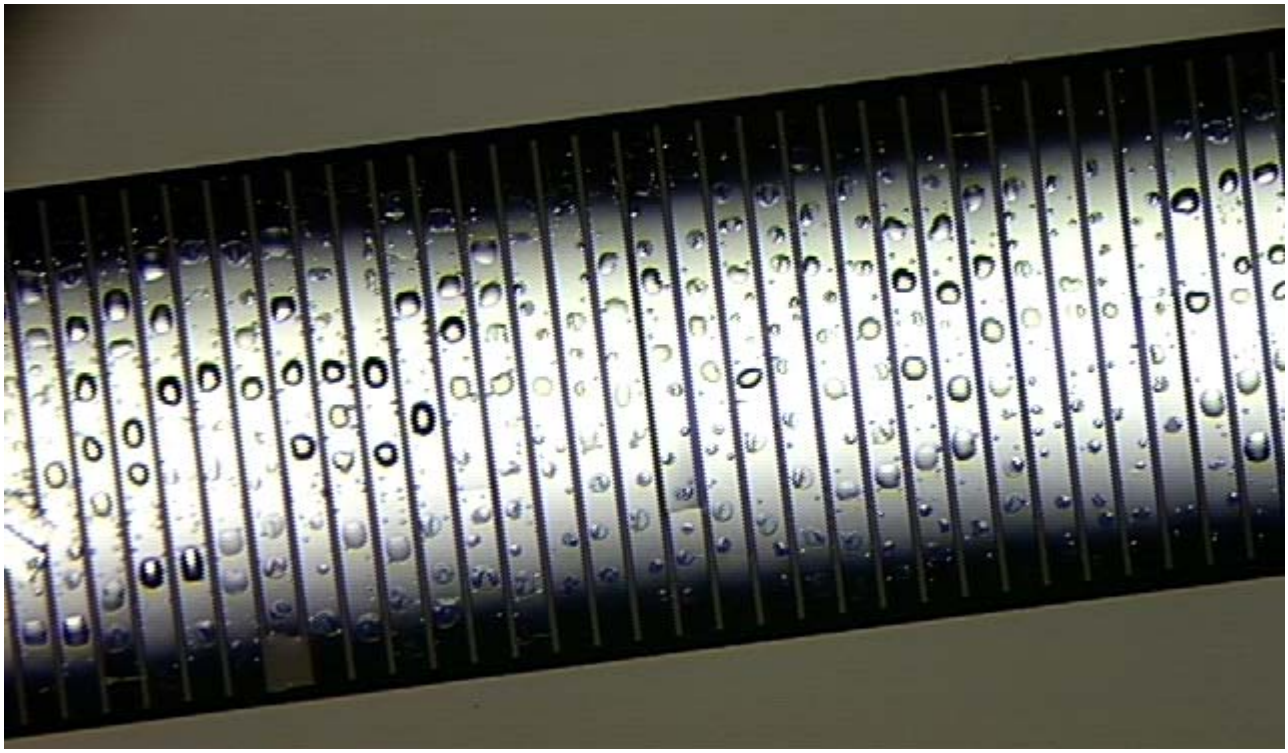

Figure 5. Released 1-mm tall strip with slotted release holes. Etchant is 1:3 HF(49%):H2O. This etchant results in some blistering due to bubble formation. Note the slots lead to curvature in the short (axial) strip direction instead of the long (desired circumferential) direction.

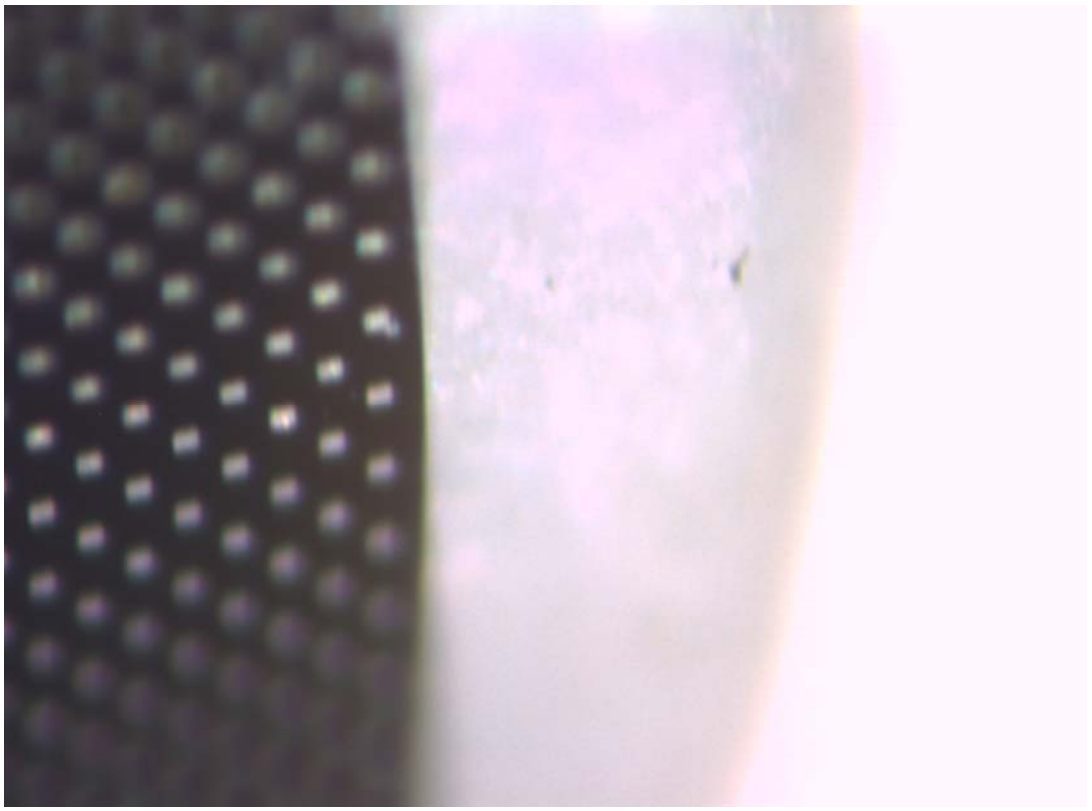

Figure 6. Released GaAs/AlGaAs semiconductor support showing isolated release holes. The holes are on a 50 micron pitch.

During the release process, the support cylinder exists in a partially-released state. This partially-released state may actually be more fragile than the fully-released state. In the edge-release process, the edges of the structure are unpinned while the center remains attached to the substrate. This results in the released area becoming severely buckled with locally concentrated high stress regions. The high stress makes the film susceptible to cleaving if the etched mesa has flaws, for example due to the presence of a small particle during lithography. It should be possible to alter the mesa pattern to favor a controlled buckling pattern and reinforce those areas to prevent fracture, if necessary. Typically this was not a serious problem.

More serious was the risk of fracture due to agitation of the release etchant. Relatively small disturbances in the etchant clearly led to extensive movement of the partially released film. In early attempts to release these large-area films, fracture resulted from moving the etchant container around to optimize viewing of the release process. This can largely be avoided by setting up the etchant bath at the start of work to best see the release process, if necessary.

A process development area was to compare buffered oxide etchant (BOE, a mixture of 6 parts NH_4F to 1 part HF by weight) to straight HF etching of the release layer. Both of these solutions etch high-aluminum AlGaAs fields with a high rate and high selectivity. So which is the best for release? Figure 7 shows a cross-sectional SEM image of a wafer etched with BOE for 90 minutes. The sacrificial etch layer has only etched approximately 12 microns, compared to ~180 microns that was etched in 90 minutes using HF (not shown). The reason for this difference is

the clogging of the etch channel with particulate generated during etch, as seen next to the mesa as small faceted crystals. Energy-dispersive x-ray analysis showed the presence of aluminum and oxygen in these particles, suggesting that BOE reacts with AlAs to form aluminum oxide (or AlO_xH_y species). The near-neutral pH of BOE allows the solid product to precipitate out of solution, while the highly acidic HF solution does not.

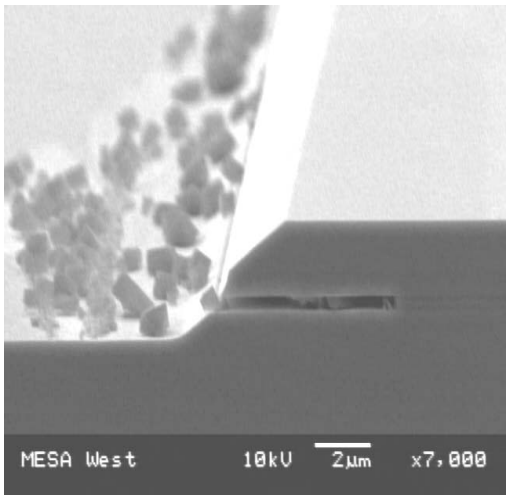

Figure 7. Cross-sectional SEM of sample with release layer etched in BOE.

Having determined the best release method and chemistry to remove the semiconductor supports from the wafer, we turn to the final task of characterizing the utility of the semiconductor supports to serve as "handles" for transporting the wire array. Figure 8 shows an image of several released semiconductor supports. The curling of these films due to the built in strain is apparent. The question is how well does the measured curl correspond to the calculation? It turns out to be difficult to measure. Each film is mechanically stable in 3 different configurations: curled axially, curled longnitudally, and curled in a spiral. In fact, the spiral shape seems to be most preferred. The films can easily be switched between these states with the application of a small force.

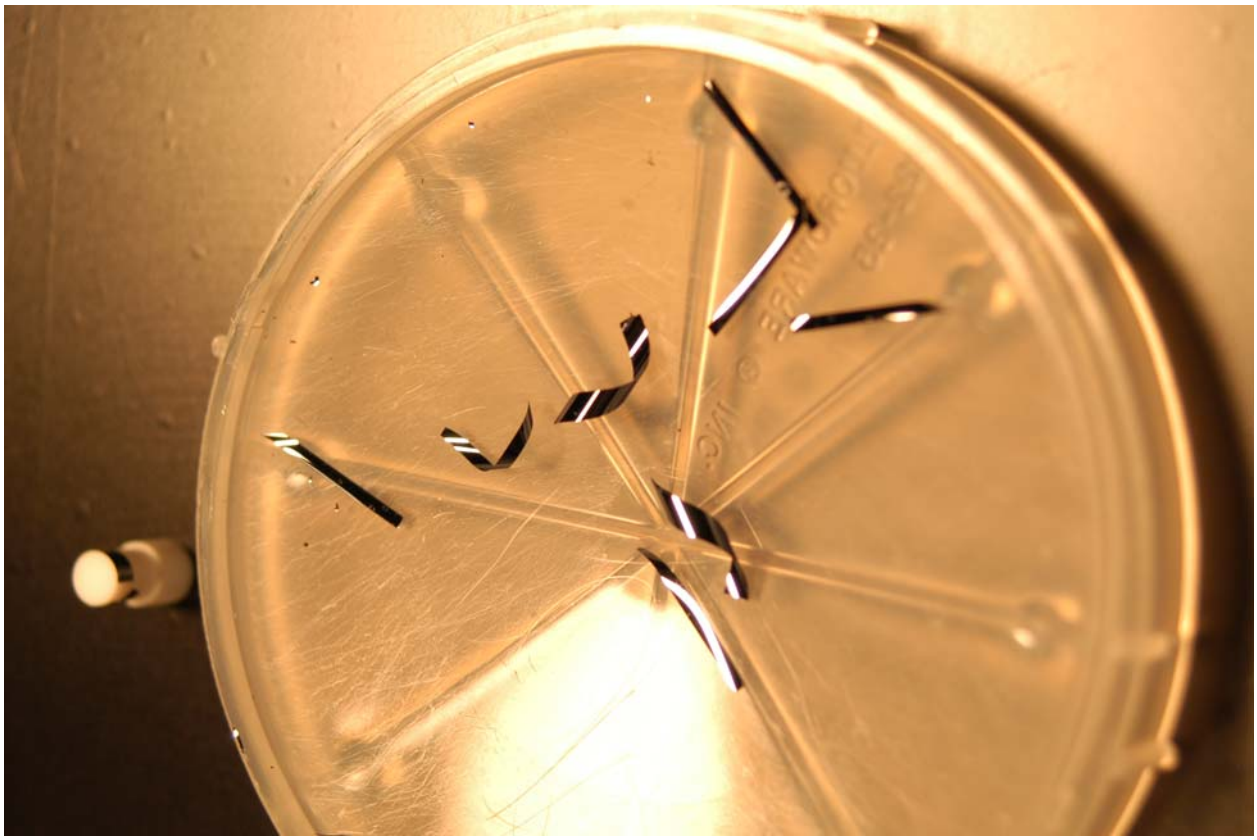

Figure 8. Several released semiconductor supports. The unrolled length of each film is 12.56 mm, and the strip height is 1, 2, or 4 mm.

Given that the film configuration is not well defined, how can these films be used as supports? It turns out that they are remarkably robust to handling. Whereas bulk substrates can support little deformation, these films can be easily bent, poked and generally manhandled without damage exactly because they are so thin. The following techniques were developed to handle the released films.

First, it was found that the films easily captured and held a static charge. A piezoelectric charge deposition device (Zerostat 3, made by the Milty Corporation) was used to deposit either a net negative or positive charge on the film. By charging an insulating rod with the opposite polarity, the film would easily attach itself to the rod. The film could then be easily moved to a new location and removed from the rod by providing a stream of negative and positive charges. Figure 9 shows the film electrostatically attached to a macor ceramic rod. A set of test mandrels was made with the correct diameter to accept the curled films as a first attempt at a mounting hardware design. A polyethylene version is also shown in Figure 9. By applying a small drop of water on the surface of the mandrel, the film could easily be manipulated on the surface of the mandrel and held in any position by surface tension.

Figure 9. A film electrostatically held on a macor rod (top of image).

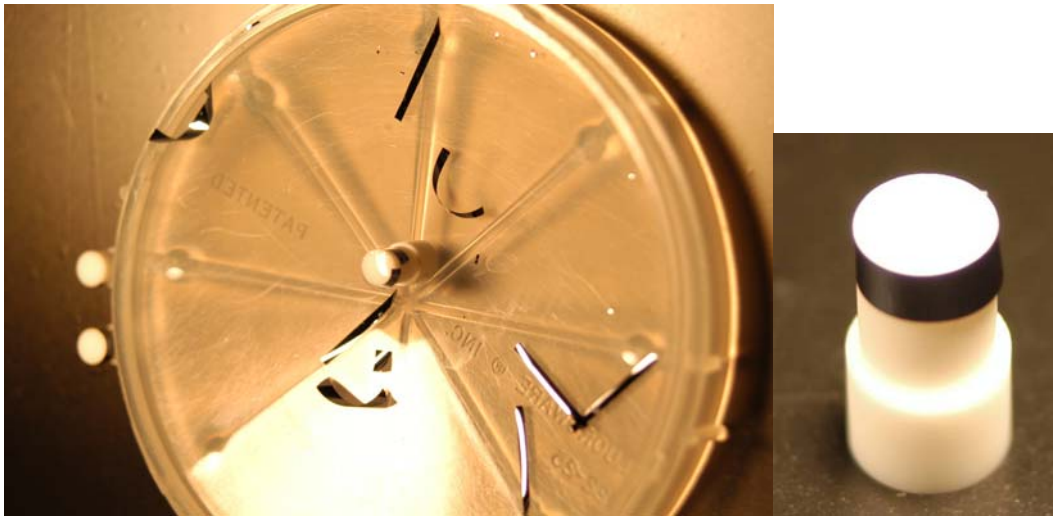

Figure 10. Film placed onto moistened mandrel for manipulation to desired cylindrical shape. Right, after manipulation to form final cylinder shape.

Figure 10 shows a film held by surface tension on a mandrel. From this development and test mounting it is apparent that the designed curvature doesn't have to be particularly accurate, but that some curvature does aid in the handling of the films. The right inset shows the film can be manipulated to align it with the top of the mandrel and align the ends of the film with each other.

Having completed the first year milestones, a second year set of milestones was proposed. These milestones took into account the process development from the first year. These milestones are:

1. High-quality gold plating process transferred to the Microfab.
2. Automated inspection of wire width and thickness.

3. Strain relief structures drawn and incorporated in wire arrays.
4. Mounting of wire arrays on mounting hardware.
5. Scaling of array from 4 mm to 40 mm.

2.4. Plating Process Development

Having selected plating as the best deposition technology for basic demonstration of microfabricated wire arrays, the task came to establish this process in the MESA Microfab. Gold plating had been well-established in the CSRL, but was unavailable for an extended period during the transition to the MESA Microfab. The Microfab setup has advantages in terms of simplified electronic controls and greater overall cleanliness compared to the CSRL. However, there was extended down time for exhaust modifications at the plating bench in order to meet safety requirements. The gold plating process was not available to users until mid-March 2008, even though the Microfab was mostly functional by February 2007. The CSRL plating capability was lost in April 2007 to allow fab demolition. To help bridge this nearly 1-year gap, samples were plated during this period by Adam Rowen and Christian Arrington (Org. 1725) in their 858EL Light Lab. Their prior experience with RF MEMS (low-stress) and LIGA (very thick, order of hundreds of microns) plating made the plating requirements for this project look comparatively simple.

Because manually-fabricated wire arrays with gold wires are not available, efforts were also made to look at plating other metals to allow direct comparison with available experimental wire array data. A platinum plating bath was established for this purpose. There is also experience with and ready availability of plating chemistries for nickel and copper, but platinum was preferred for comparison to existing Z data. In order to produce wire arrays to develop mounting processes, gold was chosen as the material because the process is well known and the stress level in the film is very low. Time was also spent on platinum plating in parallel. Bright platinum films could be deposited, but there was incompatibility of the bath chemistry and temperature (90°C) with the masking photoresist used. This area requires further development to field platinum arrays.

The gold plating solution used in the Microfab is a non-cyanide (sulfite) based bath with organic grain refiners. The plating bath temperature is 50 °C. The primary variable available to optimize plating deposition is the current density applied. Higher current density allows for faster deposition at the risk of roughened films and a less-dense microstructure. Through repeated depositions at various current densities, it was found that the film uniformity, locally and globally, was acceptable at 2 mA/cm^2. At perfect efficiency this would correspond to 7.62 microns/hour deposition rate. In practice the deposition rate was closer to 5 microns/hour. Also, The plating rate was found to be occasionally as low as 3.5 microns/hour. This was attributed to bath contamination and consumption. It is important for repeatability and yield that the bath chemistry and use be carefully monitored. These procedures are still under development for the Microfab.

While developing the plating process, most of the deposition was done on mechanical silicon wafers. Mechanical adhesion tests of the plated films showed that not only was the film

adhesion excellent, but the plated gold structures themselves were quite strong. A new process flow was then considered. Instead of plating the wires on a semiconductor support, the wires could be plated on a sacrificial support that is etched to "float" off the plated film. The film itself is then directly handled and mounted in the Z test fixture. The advantage of this method is that epitaxial semiconductor growth is no longer required – a huge cost savings. Instead, the sacrificial layer can be anything that can be selectively etched to remove the overlying metal and any substrate can be used. Therefore, the process can be scaled to a truly large scale if desired and the cost per array will drop enormously.

For fabrication purposes, 100 mm mechanical silicon and quartz substrates are convenient. These are easy to clean and reuse many times. The release layer required some development. The most convenient material is spun-on photoresist. This can be hard-baked to offer good chemical resistance and adhesion. Several resist release materials were tried. PMGI, a particular type of deep ultraviolet sensitive resist, has the added advantage of being able to withstand exposure to acetone. It is removed with NMP, which also serves well to clean up any residues left on the wire array. PMGI does have a tendency to form stringers during spin leading to particulate generation. Careful attention and inspection is needed to ensure these defects do not impact the wire array.

Continuing on with the semiconductor-support free process, the sacrificial layer is blanket coated with a conducting seed layer, typically 20 nm of titanium followed by 100 nm of gold. Evaporation of the seed layer is the preferred deposition technique because 13 100mm wafers can be deposited simultaneously. Also, an interaction between the sacrificial photoresist layer and sputtered titanium generated a difficult-to-remove scum on the backside of the plated arrays.

After seed deposition the wafer is masked with photoresist where plating is not to occur. This is another lithography area that required significant process development. The requirement for plating is that the photoresist is at least as thick as the desired plating thickness. Otherwise, the plating will mushroom over the top of the photoresist pattern. There were two designs settled on that would be suitable to be shot in Z. These wire arrays were 1 cm radius and had 150 platinum wires. The first design consisted of 30.6 micron square wires, and the second design consists of 15 micron thick and 62 micron wide wires. These specifications meet the mass density (mg/cm) of wires optimum for Z. Therefore, photoresist with at least 30.6 micron thickness with 1:1 patterning aspect ratio is needed. Several multiple-spin processes were attempted to build up sufficient thickness. The best results were obtained with a single spin, high viscosity resist – AX50XT. This resist can be spun at ~1000 rpm to produce ~35 micron thick films. The primary difficulty with this thick resist is proper solvent removal before exposure. Without careful baking, the film builds up a high tensile stress. The result, as shown in Figure 11, is cracking. This cracking will start at any small defect/particle in the spun film. At higher levels, the cracks will also start to appear at stress concentrations in the pattern such as corners. With careful baking, these defects can be avoided as shown in Figure 12. This wafer has already been plated to 15 microns gold thickness.

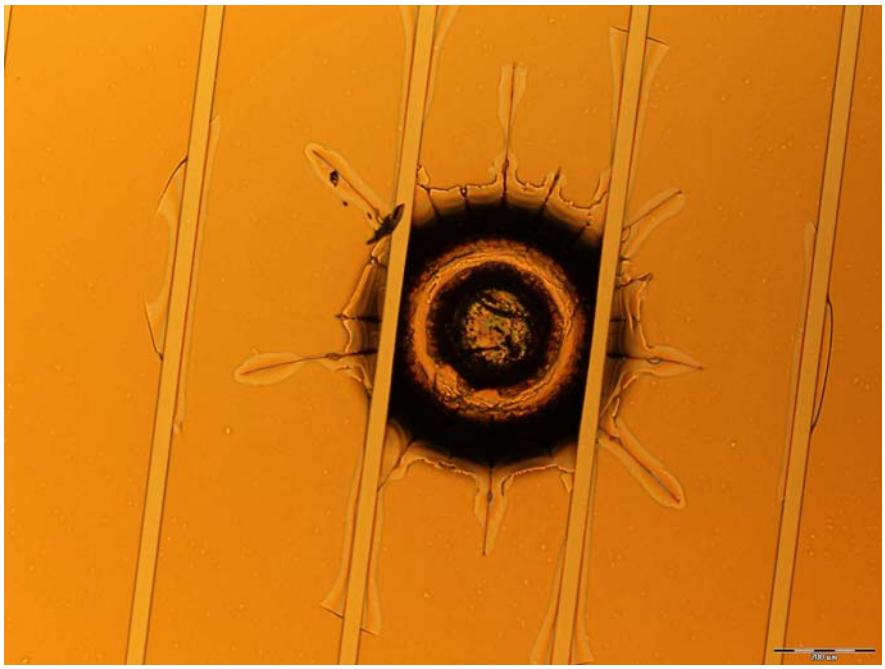

Figure 11. Particle-and-stress defect in 35 micron thick AZ50XT resist. Note the cracking emanating from the pattern edges. The open lines are 30.6 microns wide.

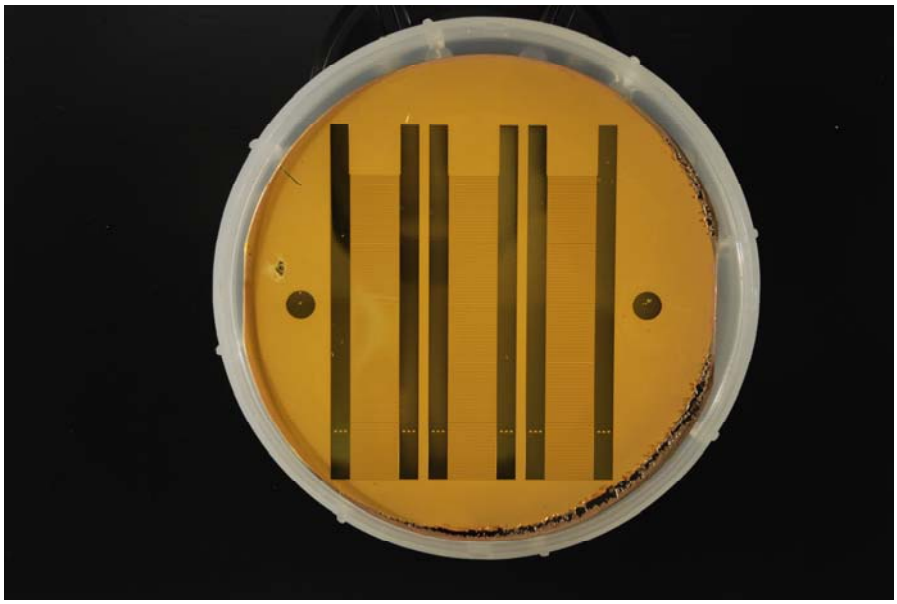

Figure 12. Patterned and plated film showing zero resist defects in the pattern area. There are three wire arrays with 150, 62 micron wide wires plated to 15 microns. The arrays are designed to roll up into a diameter of 20 mm. The two circles are for plating contacts. The mustard-colored field is photoresist. The wafer diameter is 100mm.

Following plating the plating resist is stripped in acetone. The seed metal is blanket etched using potassium iodide/iodine solution for gold etching followed by 1:100 HF (49%): deionized water for titanium removal. As an alternative, the seed may be argon ion-sputtered. The film is then removed from the substrate by soaking in solvent. The entire process is shown schematically in Figure 13.

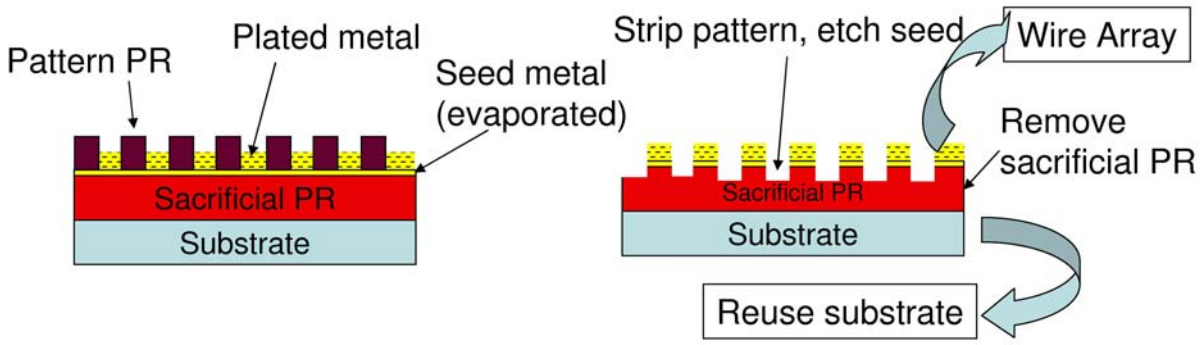

Figure 13. Schematic of semiconductor-support-free wire array process flow.

After the film is free from the substrate, it must be dried. Surface tension can be a destructive force on small structures. Plans were in place to utilize supercritical carbon dioxide to displace a methanol rinse solvent from the substrate and avoid deleterious surface tension effects. Amazingly, these wire arrays could be simply pulled out of solution by tweezers and air dried. There would be some sticking of adjacent wires together, but as the solvent evaporation progressed the stuck wires would separate. At this point the structure can be sent on for mounting. Mounting will be discussed following a discussion of automated wire inspection and strain relief integration.

2.5. Automated Wire Inspection

A real advantage to planar fabrication is the simplicity of inspection during fabrication. Of course, imaging of completed, mounted cylindrical arrays is needed as well, but the use of in-process inspection allows mounting of only “known-good die”. Furthermore, the data available about the wire shape is simply impractical to gather for conventional manually assembled wire arrays.

Excluding the standard use of lithography inspection in-process, two tools were applied to plated wire inspection. The first, the Rudolph NSX automated defect inspection tool, is simply a brightfield microscope that can rapidly scan a wafer while taking digital pictures. Each picture is compared to a standard, defect free image. Those pictures showing a substantial difference are flagged as defects for further disposition. This is particularly useful for identifying process problems that have a geometrical fingerprint causing failures in a particular pattern around the wafer. Some time was invested in this capability, but it was found to be most optimal for inspecting many small die with small defects. The type of defect issues we faced were more along the lines of Figure 11, which was easily spotted in routine lithographic inspection. In the case where many wafers have to be fabricated and compared, i.e. in a production mode the Rudolph NSX automated inspection tool should be useful.

Much more information than a simple pass/fail flag was available using the automation capabilities of the WYKO white-light interferometer. The height, width, and roughness of the wire all can be extracted in about 20 seconds for a selection of points along the wire. Figure 14 shows an example of a scan along a single wire. Automated stepping allows a map across and array. Data for wire width and roughness is shown in Figure 15. The sidewall and bottom roughness are set by the photoresist mask and the substrate, respectively, and are much smoother than the top surface roughness. Overall, the wire dimension uniformity and roughness are at least on the order of existing drawn tungsten wires, based on examination of a length of drawn tungsten wire in the SEM.

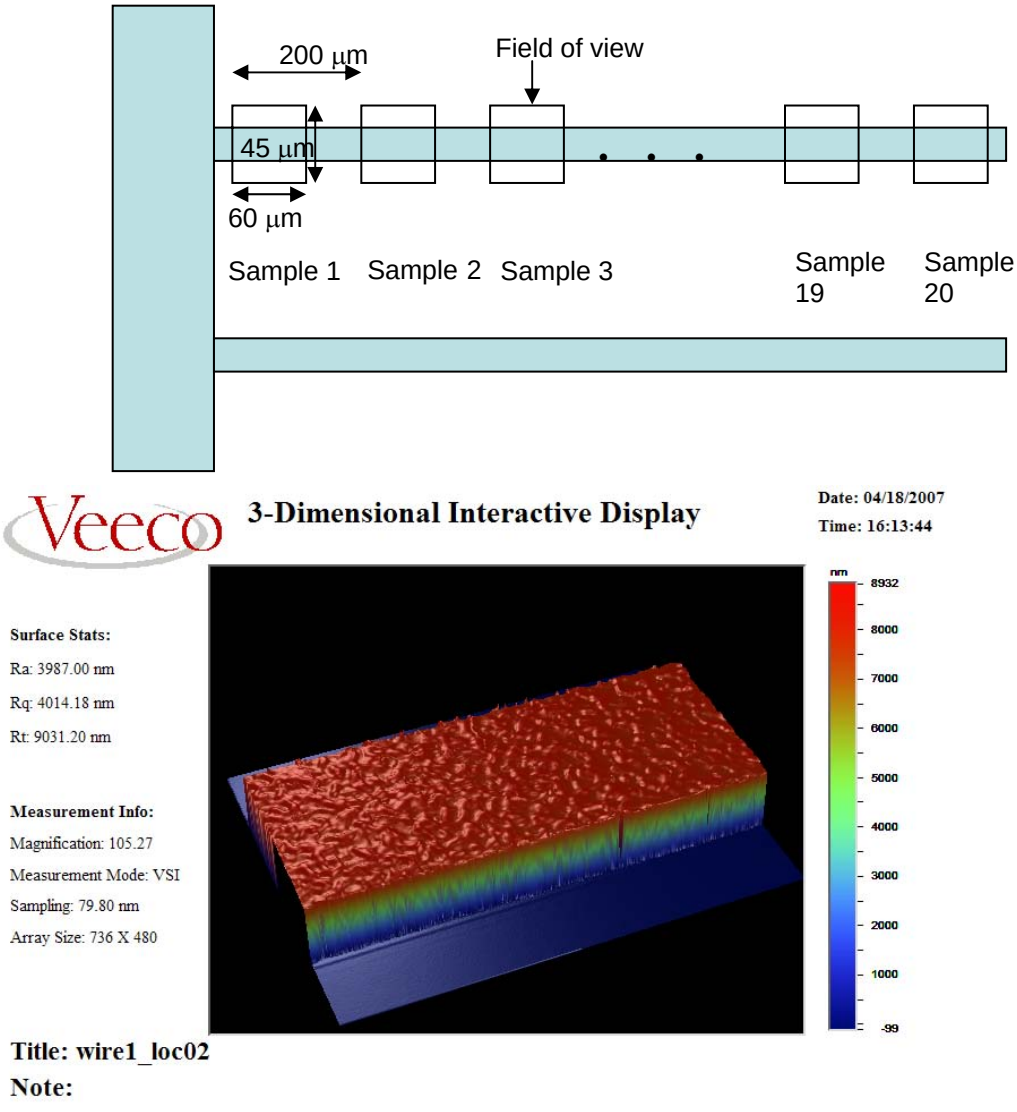

Figure 14. Measurement along the length of a wire. Top, measurement positions. Bottom, typical data.

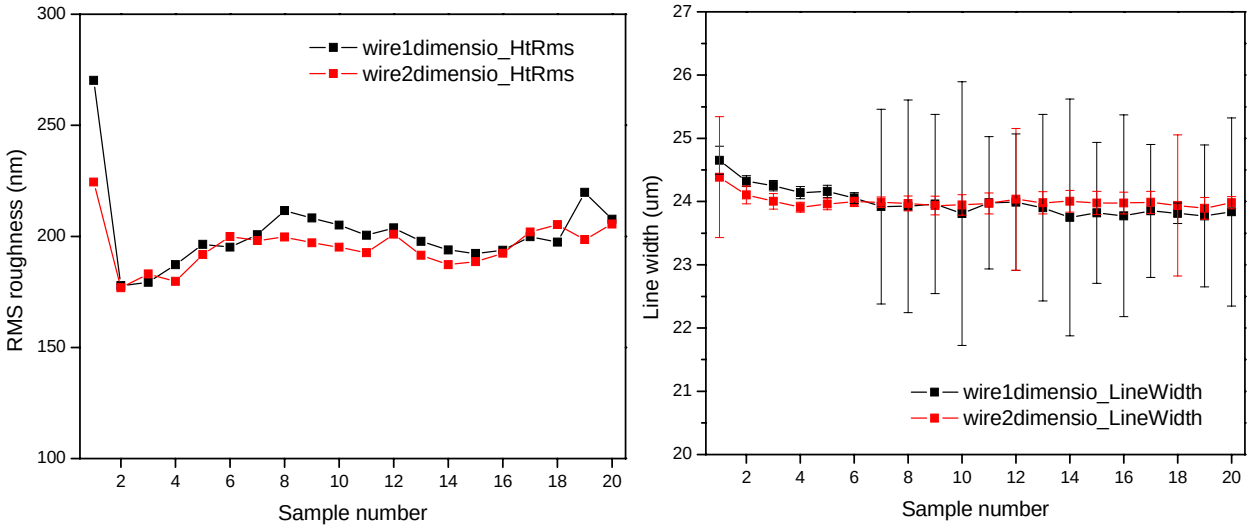

Figure 15. Roughness (left) and line width (right). The large error bars in the right hand figure are an artifact of the data extraction; the small error bars are more representative.

2.6. Strain Relief Incorporation into Wire Arrays

The strain relief section above showed a feasible design to accommodate the displacement of the anode-cathode gap during evacuation of the Z chamber. Because the wire array mounting was anticipated to be difficult, effort was focused on producing wire arrays for handling tests rather than drawing and ordering a new mask with the spring structure included. Therefore production of the spring design was delayed until wire array mounting could be worked out. This structure was not demonstrated before the decision to terminate the project.

2.7. Mounting of Wire Arrays

Having produced free-standing wire grids, it is necessary to mount them on hardware to form the required cylindrical shape. This task requires careful visualization of the process of loading the wire array into Z. A prototype mounting system was designed (Figure 16) and fabricated at Team Specialty Products. Similar sleeve and spacer systems have been used for loading wire arrays before. The challenge then is how to attach the wire array firmly to the anode and cathode hardware. The first generation hardware has an inset around the circumference of the anode/cathode where the wire array bus is supposed to attach. After fabrication of the hardware, it was clear that attaching the wire array bus to this 10-mil wide section was impossible. Learning from that lesson, the next generation of wire arrays – which as shown above scaled from 4mm diameter to 20mm diameter – incorporated a much wider bus (5mm wide on each side).

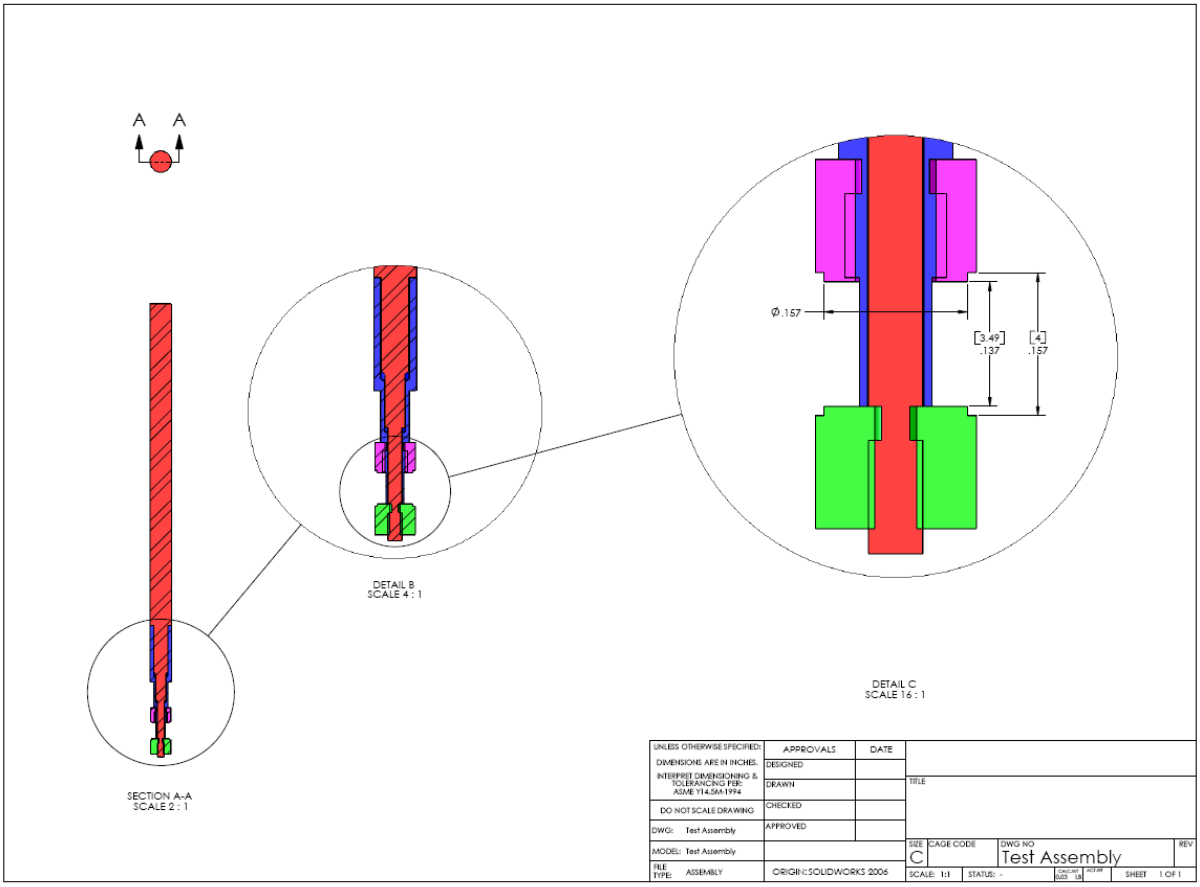

Figure 16. First generation mounting hardware for 4mm diameter wire arrays. The anode (green) and cathode (pink) contacts are held in place by a threaded rod (red) and separated by a threaded spacer (blue). These last two items are removed after positioning the wire array in Z, with the wire array attached at the inset in the anode/cathode circumference.

As can be further seen in Figure 12, the bus is made to extend far beyond the end of the wire array. The end of the bus extension, when wrapped onto the mounting hardware, should meet exactly in the center of the three holes patterned in the bus on the other end of the array. This will position the 150th wire in the array just the right distance from the first wire.

The first attempts at mounting the improved wire array design utilized a simple polyethylene rod machined on a lathe to 20mm diameter. Figure 17 shows a photo of a wire array mounted on such a rod. Playing with this rough approximation to the problem of mounting on real Z-machine compatible hardware showed some obvious problems. First, and most serious, is that control of the circumference of the machined part is critical to get the first and last wires in the array to line up. In order to overcome this problem, the mounting area should include a compressible material or flexible rim. This way, when the wire array is being rolled onto the support, pressure can be applied gradually. Releasing the pressure allows the mounting area to expand against the mounted array which is then automatically centered. Second, a means to

quickly tack the array into the correct diameter is needed. In Figure 17 the array was attached with low viscosity cyanoacrylate glue. This allowed for some working time to reposition the array after wrapping it, but it also tended to spread into undesirable areas. In addition, the wire array then would not have very good electrical contact. With proper fixturing, it could be possible to laser spot weld the films together after careful positioning. Unfortunately, time was not available to demonstrate such a method. Finally, it is apparent that the anode-cathode gap has to be set right to avoid slack in the wires as apparent in Figure 17. In practice, there would be no actual connection in the anode-cathode gap, so gravity would serve to automatically straighten the wires.

Figure 17. Wire array mounted on a 2 cm polyethylene rod.

2.8. Scaling of Wire Arrays to 40mm Diameter – and Beyond

The initial work on semiconductor supports was done with 75mm substrates. Geometrically, the maximum size array that could fit on a 75 mm wafer is about 20mm diameter. Figure 18 illustrates the packing of various size devices on various size wafers. A 75 mm wafer can hold 8, 10mm diameter arrays or a single 20 mm diameter array. The 100mm wafers used in the majority of this work could hold three 20 mm diameter arrays or a single 30 mm array. Going up the largest substrate size that can be fabricated in the Microfab, 150mm, a single 45mm diameter array is possible. 300mm equipment is readily available elsewhere, allowing production of 24 40mm diameter arrays or a single array of 95 mm diameter. The move to 450 mm production equipment will not take place for several years, though silicon substrates have been manufactured at this size.

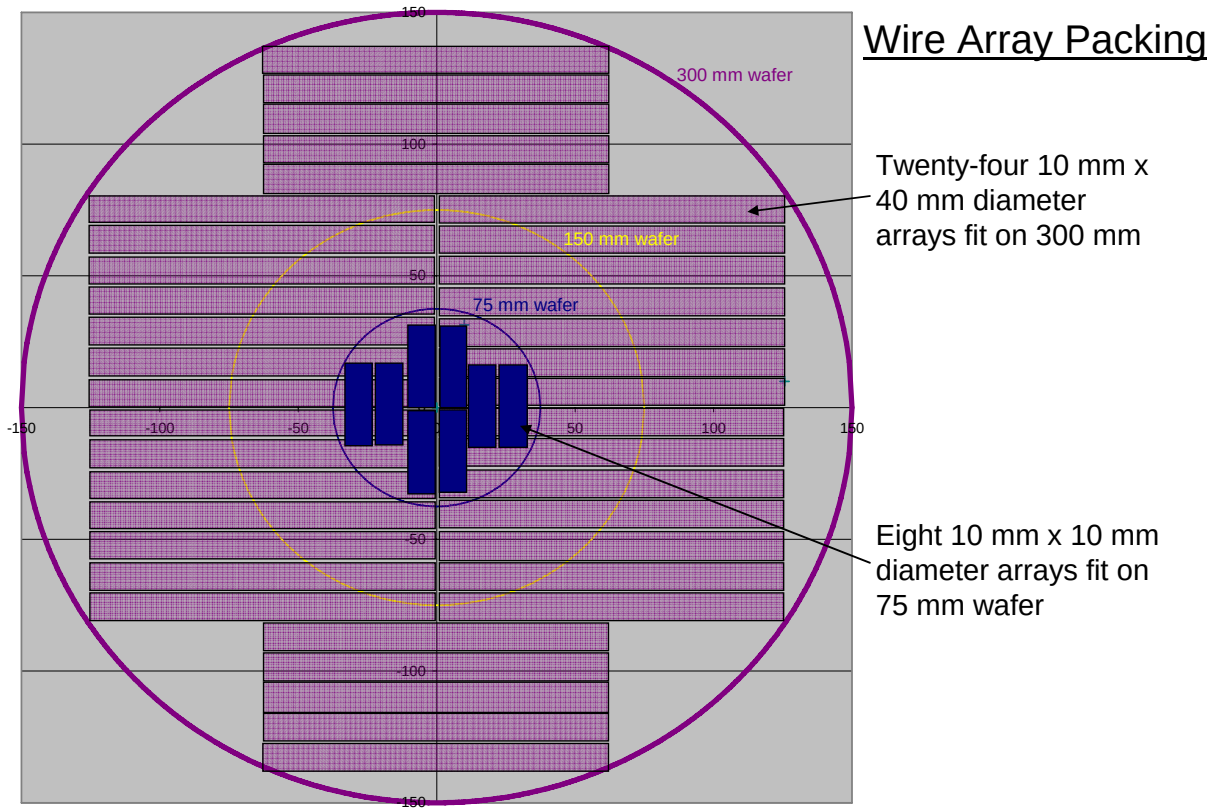

Figure 18. Schematic of packing different size arrays on various wafer sizes.

While 20mm diameter arrays were convenient for this demonstration node, it would be desired to produce the full array of sizes useful for Z. To scale up to larger sizes, the use of direct write laser lithography may be the most feasible option. This bypasses the need for mask fabrication, allowing for greater flexibility in design changes. The CINT facility at Sandia has a direct write laser tool that is accessible to project work. Otherwise, all processes demonstrated on 100mm wafers are just as easily done on 150mm wafers.

3. CAPABILITY SUMMARY AND FUTURE DEVELOPMENT NEEDED

Processes were established in the MESA Microfab to produce demonstration gold wire arrays. In addition, plating chemistries for other common Z wire arrays (platinum and copper) have been established and are available for integration into the same process flow. Figure 19 below shows the range of metals with existing or near-term process recipes in MESA. Addition of thin film capability for the remainder of the transition metals (excluding Zn, Cd, Hg) and rare earths is straightforward. Other plating options are tin and lead, but these may not be very useful as Z wire arrays due to excessive fragility.

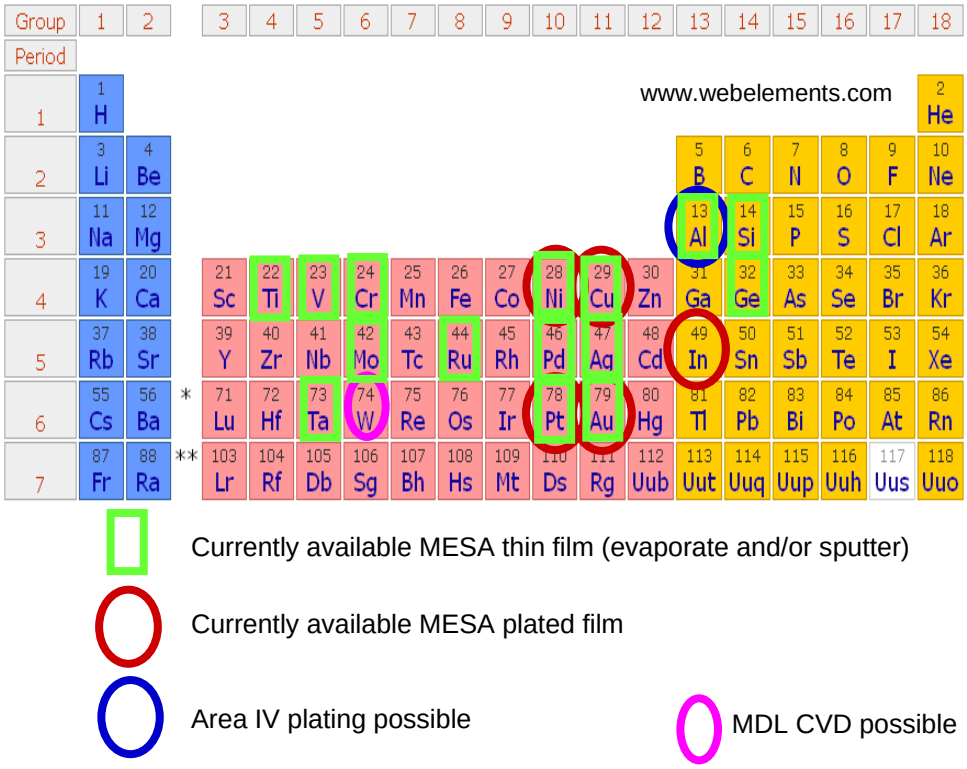

Figure 19. Periodic table showing current metal deposition options.

Beyond the final development needed for the mounting of the array, there are other process development tasks remaining. The variability and cross-contamination of the plating baths must be addressed though a process for regular sampling and reporting of the bath chemistry. Process parameters leading to the occasionally observed dishing of the plated surface should be identified. Less important but useful development would include a chemical-mechanical polish method to offer a damascene-like process for smoothing the top surface of the metal and improving uniformity. Finally, the sacrificial layer properties could be improved to simplify the cleaning of the backside residue off the plated array after removing it from the substrate.

4. CONCLUSIONS

The fabrication of wire arrays for Z using planar processing techniques has been shown to be a practical possibility. The microfabrication route offers additional possibilities for tailoring wire array designs to explore new aspects of *z*-pinch plasma physics. The total fabrication time for an array would be no greater than using manual assembly and the cost can be lower, especially if multiple copies of the same wire array design are needed. The most challenging part is the transformation of the wire array into a cylinder by attachment to Z mounting hardware. While this has not been adequately demonstrated yet, there are concepts to address the problems that have been identified to date.

This project was ended after two of three years. The third year was to be devoted to further size scaling and demonstrating the wire array in real test shots. Ongoing work in target development at Z, however, has led research away from wire arrays and toward targets made of solid metal cylinders.

While this project was not continued into its third year for demonstration of microfabricated wire arrays in real test shots, the technology to fabricate wire arrays of use to the community stands ready and available in the MESA microfabrication facility. These methods are in constant use for other microfabrication projects. Should the demand for wire arrays return, the MESA facility will stand capable of delivering these arrays in short order.

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