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Robust Hermetic Packaging Techniques for MEMS Integrated Microsystems

Brian H. Stark, Junseok Chae, Andrew Kuo, Andrew Oliver*, and Khalil Najafi

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Sandia National Laboratories
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Brian H. Stark, Junseok Chae, Andrew Kuo, Andrew Oliver*, and Khalil Najafi

Center for Wireless Integrated Microsystems, University of Michigan

*Sandia National Laboratory
Advanced Microsystems Packaging
Sandia National Laboratories
P.O. Box 5800
Albuquerque, New Mexico 87185-1076

Abstract

This work is the result of a Sandia National Laboratories LDRD funded fellowship at the University of Michigan. Although, guidance and suggestions were offered by Sandia, the work contained here is primarily the work of Brian H. Stark, and his advisor, Professor Khalil Najafi. Junseok Chae, Andrew Kuo, and their co-workers at the University of Michigan helped to record some of the data. The following is an abstract of their work.

We have developed a vacuum packaging technology using a thick nickel film to seal MEMS structures at the wafer level. The package is fabricated in a three-mask process by electroplating a 40 micro-meter thick nickel film over an 8 micro-meter sacrificial photoresist that is removed prior to package sealing. Implementation of electrical feedthroughs in this process requires no planarization. The large release channel enables an 800x800 micro-meter package to be released in less than three hours. Several mechanisms, based upon localized melting and lead/tin solder bumping, for sealing the release channel have been investigated. We have also developed Pirani gauges, integrated with this package, which can be used to establish the hermeticity of the different sealing technologies. They have measured a sealing pressure of approximately 1.5 Torr. Our work differs from previous Pirani gauges in that we utilize a novel doubly anchored structure that stiffens the structural membrane while not substantially degrading performance in order to measure fine leak rates.

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Introduction

This work is the result of a Sandia National Laboratories LDRD funded fellowship at the University of Michigan. Although, guidance and suggestions were offered by Sandia, the work contained here is primarily the work of Brian H. Stark, and his advisor, Professor Khalil Najafi. Junseok Chae, Andrew Kuo, and their coworkers at the University of Michigan helped to record some of the data. The following is a report on their work.

In the first year we developed a packaging technology that employs a thick nickel film to vacuum seal a MEMS structure at the wafer level. The package is fabricated in a three-mask process by electroplating a 40 micro-meter thick nickel film over an 8 micro-meter sacrificial photoresist that is removed prior to package sealing. Implementation of electrical feedthroughs in this process requires no planarization. The large release channel enables an 800x800 micro-meter package to be released in less than three hours. Several mechanisms, based upon localized melting and lead/tin solder bumping, for sealing the release channel have been investigated. Pirani gauges integrated with this package have been used to establish the hermeticity of the different sealing technologies and have measured a sealing pressure of approximately 1.5 Torr.

For the second year we refined the design of the Pirani gauges and implemented them into Sandia's SUMMiT V^{TM} surface micromachining technology. The integrated Pirani gauge that we have developed is crucial to package characterization. Fabrication of surface micromachined Pirani gauges is complicated by the need for precise stress control to prevent thermal shorting to the substrate. Our work differs from previous Pirani gauges in that we utilize a novel doubly anchored structure that stiffens the structural membrane while not substantially degrading performance in order to measure fine leak rates.

MicroPackages

For this project, we have developed a packaging technology that employs a thick nickel film to vacuum seal a MEMS structure at the wafer level. The package is fabricated in a 3-mask process by electroplating a 40-micron thick nickel film over an 8-micron sacrificial photoresist that is removed prior to package sealing. The large fluidic access port enables an 800x800 micro-meter package to be released in less than three hours. Implementation of electrical feedthroughs in this process requires no planarization. Device release is performed after the formation of the first level package. Several mechanisms, based upon localized melting and Pb/Sn solder bumping, for sealing low fluidic resistance feedthroughs have been investigated. This package has been fabricated with an integrated Pirani gauge to further characterize the different sealing technologies. These gauges have been used to establish the hermeticity of the different sealing technologies and have measured a sealing pressure of ~1.5Torr.

The process for manufacturing this package with an integrated Pirani gauge is shown in Figure 3. The Pirani gauge is defined in a 4-mask surface micromachined process that employs polysilicon both as a sacrificial material and for package feedthroughs. This is followed by deposition of an 8-micron thick sacrificial photoresist spacer that also defines a fluidic access port. This structure is then capped in 40-micron thick electroplated nickel. The photoresist and sacrificial polysilicon layer are then simultaneously etched in TMAH and dried in supercritical CO2. The polysilicon etch in the 800x800 μm package takes three hours and which is only about six times longer than unpackaged devices. The cleaning process in limited by etching the polysilicon, which dissolves at a rate of 0.75 μm/min inside the package, as compared to an etch rate of 1 μm/min in unpackaged devices. Figure 4 shows the package structure before sealing with a close-up of the fluidic access port. Figure 5 shows the polysilicon feedthroughs implemented in this process. Conformal covering of the feedthroughs occurs without the need for planarization. By increasing the vertical height of the fluidic access port from a few thousand Angstroms (previous work) to 6-8 microns (this work), the effective fluidic resistance into the package is dropped by at least three orders of magnitude. However, sealing this structure required extensive process development. The most promising method to seal the fluidic feedthrough utilizes Pb/Sn solder balls to encapsulate the package. After fabrication and release of the Pirani gauge, a 63Sn/37Pb solder paste was stenciled over the package by means of a custom stainless steel micro stencil. The package was then inserted into a vacuum chamber and heated past the soldering temperature (~230º C). The resultant structure (Figure 6) consists of a MEMS structure inside a cavity that is encased in solder. Figure 7 shows the thermal impedance of three different types of Pirani gauges before and after solder sealing. As the figure indicates, the thermal impedance increases after sealing, which is consistent with vacuum encapsulation. Based on the measure data, a pressure of ~1.5Torr exists inside the cavity.

Currently, we are also working on measuring long term reliability of active neural probes packaged with electroplated gold. We have developed a test probe (Figure 8) that utilizes test transistors and resistors (Figure 9) to measure the survivability of active electronics during accelerated testing in phosphate buffered saline. These accelerated tests should commence in the next few months. We are also developing a thin film package that is compatible with MEMS made in a foundry process. We have proposed a technique, based upon localized heating of polysilicon ribs, to seal MEMS at the die level after production in a foundry process, such as SUMMiT V™ as shown in Figure 10. This work will be conducted in conjunction with Sandia and will take advantages of their extensive facilities and expertise.

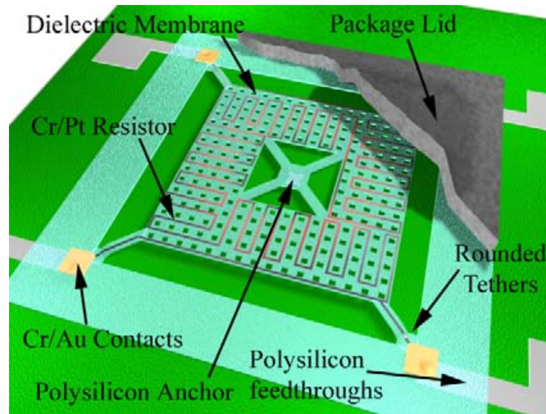

Figure 1: Diagram of doubly anchored Pirani gauge.

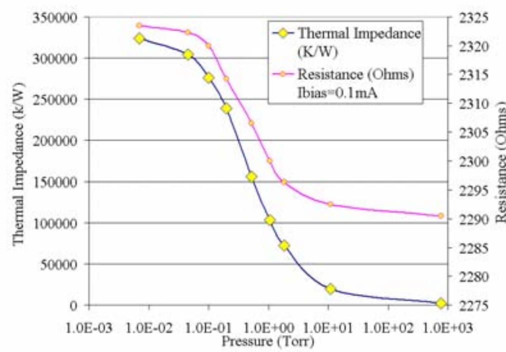

Figure 2: Thermal impedance and electrical resistance of the Pirani gauge vs. pressure.

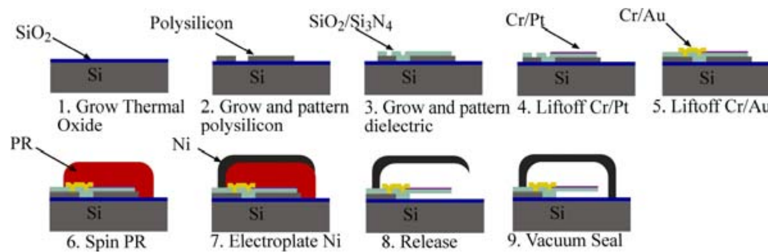

Figure 3: Process for manufacturing vacuum-sealed Pirani gauges

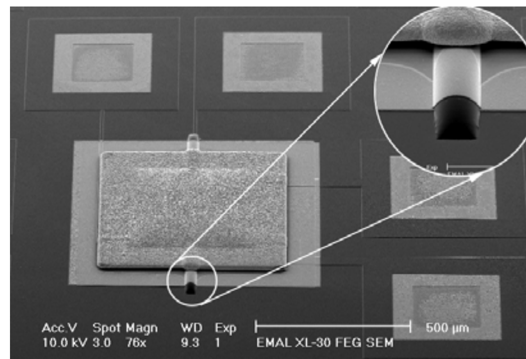

Figure 4: Package after fabrication but prior to sealing. Note the 6 μm high fluidic feedthroughs.

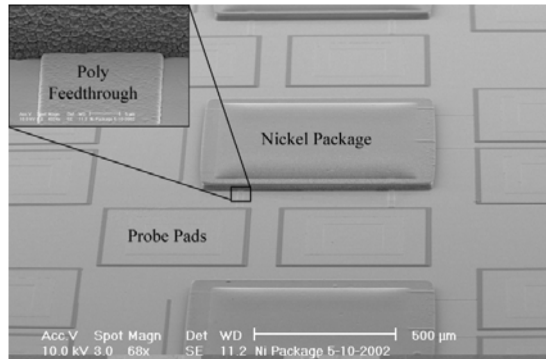

Figure 5: SEM of packaged Pirani gauge. Note the conformal covering of the feedthroughs. This is accomplished without planarization.

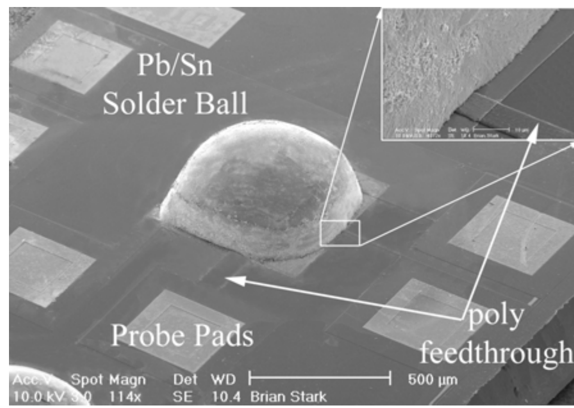

Figure 6: Pirani gauge encased in micro Pb/Sn solder ball

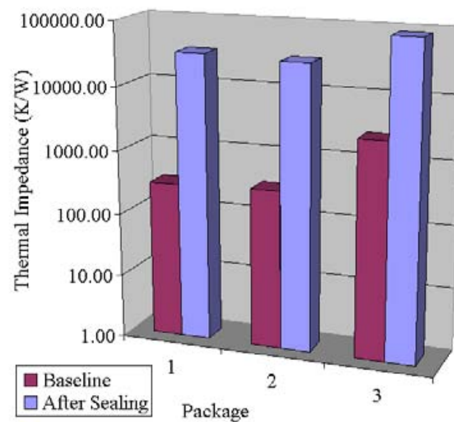

Figure 7: Thermal impedance of Pirani gauges before and after sealing with Pb/Sn solder bumps.

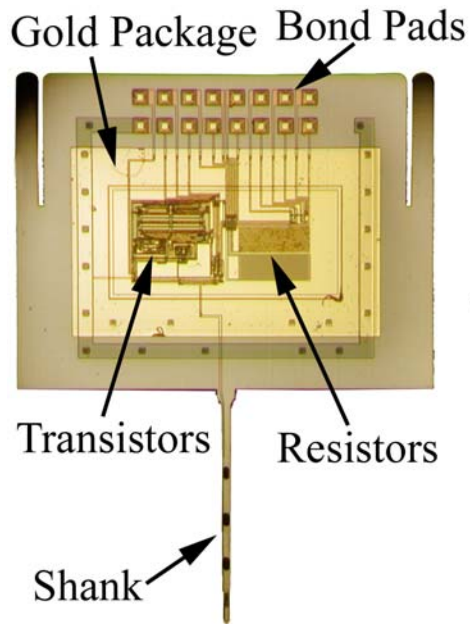

Figure 8: Picture of neural probe test structure

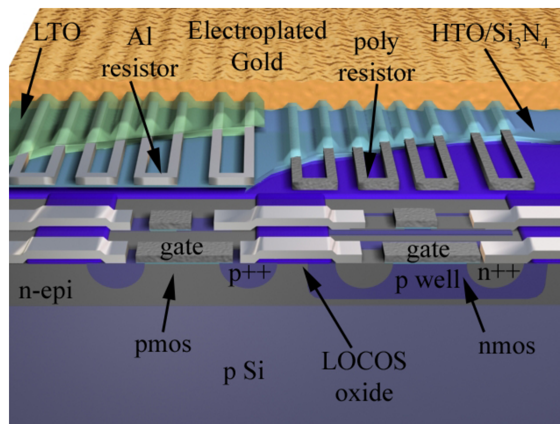

Figure 9: Schematic of Active Neural Probe Test Structure

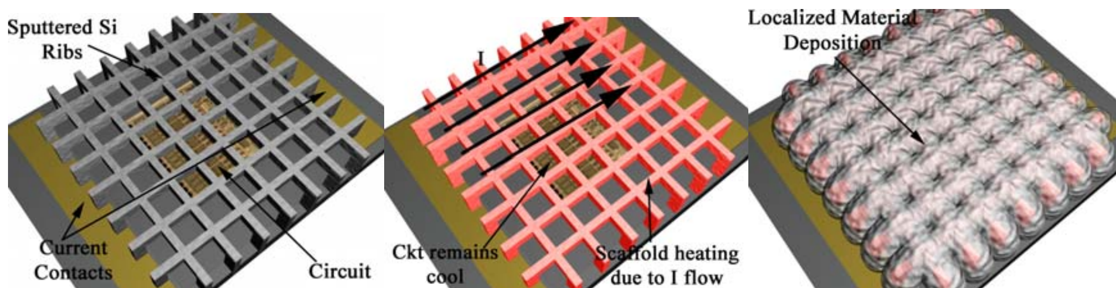

Figure 10: Schematic of Localized CVD for packaging

Pirani Gauges

There is a considerable ongoing effort to develop new sensor technologies for micropackage characterization. Common package characterization techniques (He leak testing, mass chromatography, moisture analysis) were all developed for macro scale packages and are too coarse for micopackages. To address this limitation, micro thermal vacuum gauges (Pirani gauges) have been developed to monitor internal pressure, and therefore leak rates, in hermetic packages [1-9]. While these gauges are effective at monitoring internal pressure, they require either a non-standard process [3-8] that is not compatible with many traditional MEMS technologies or a CMOS process [2, 9-16] that is not optimized for mechanical devices. A significant focus of MEMS technologies has been the push towards process standardization. To this end, producing a Pirani gauge in a standard MEMS process would facilitate a wider, more cost-efficient insertion of this technology into micropackage characterization applications.

There have been several MEMS process technologies moving towards a foundry model, including, but not limited to, the University of Michigan's Deep Boron Diffusion Process, DALSA's MEMS on CMOS approach, and Sandia's SUMMiT V™ process. Each technology has relative strengths and weaknesses. Of these processes, the SUMMiT V™ technology is the most readily accessible to outside users and offers considerable process flexibility along with well-developed design tools. For these reasons, SUMMiT V™ was selected to manufacture a micro-Pirani gauge. SUMMIT V™ is a five-layer polysilicon process with four sacrificial oxide layers. The sacrificial oxide layers can be thinned by an optional dimple etch that can create a poly-to-poly spacing as thin as 0.2 μm. Figure 11 shows the layers used in the SUMMiT V™ process and figure 12 is a pictorial view of a Pirani gauge.

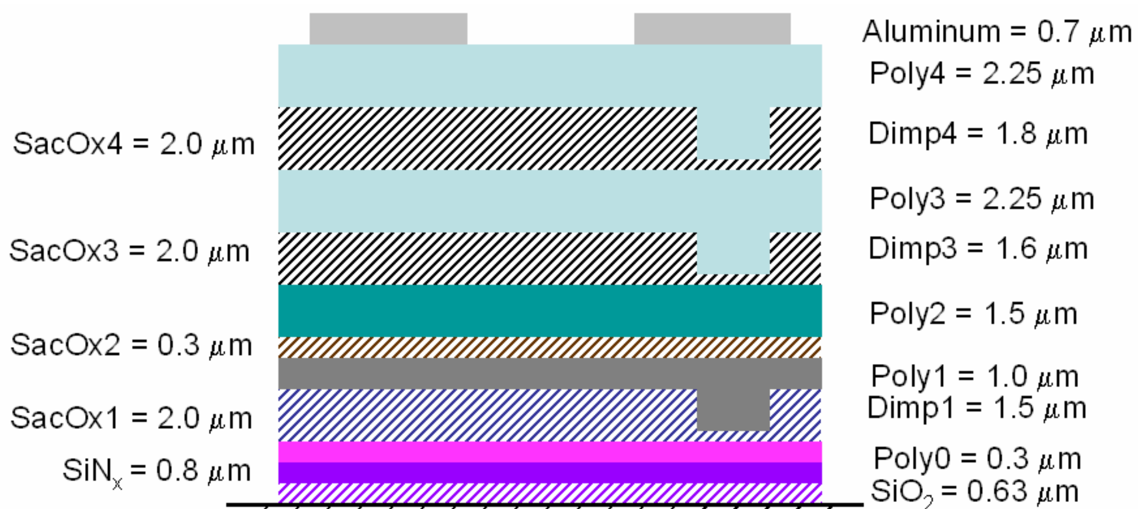

Figure 11: Layers in SUMMIT V™ process

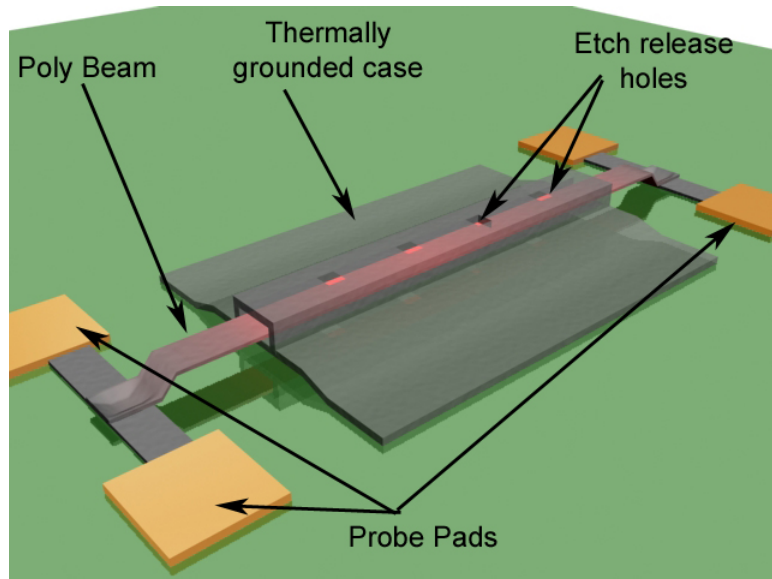

Figure 12: Diagram of polysilcon Pirani gauge made in SUMMiT V™

The design of a polysilicon Pirani gauge was first described by Mastrangelo in 1991 [4, 17-19]. Other Pirani gauges in the literature include Jacobs, Stark and Paul [20-22]. Mastrangelo established the model necessary to understand heat transfer in these devices. The shape of the gauge is a doubly clamped beam with electrical contacts at both ends and closely spaced heat sinks separated by a thin air gap as shown in Figure 12. Electrical current is driven through the device, causing it to heat. Cooling is accomplished by two mechanisms: heat transfer through the silicon (solid conduction) and heat transfer through the gas (gaseous conduction). Gaseous conduction is pressure dependent and varies according to the Knudsen number of the gas. As such, reducing the air gap spacing will increase the dynamic range of the gauge. The heat generated by the ohmic power dissipation, Po, is given as:

$$Po = \frac{Ib^2 R_0}{k_{si} whl}$$

where Ib is the bias current, R_0 is the room temperature resistance, k_{si} is the thermal conductivity of silicon, w is the width of the poly bridge, h is the bridge thickness, and l is the bridge length. The heat lost to gaseous conduction, L, is given as:

$$L = \frac{nk_{air}}{k_{si} hd_{gap}} - d * TCR$$

This gives a temperature distribution across the bridge, T(x) of:

$$T(x)=\frac{d}{e}\frac{1-\cosh\left(\sqrt{e}\right)\frac{x-l}{2}}{\cosh\left(\sqrt{e}\right)\frac{l}{2}}$$

Figure 13 shows the temperature distribution across a microbridge heated by an applied current. The electrical response of the gauge to pressure will be the same as in Chapter 5, with two limiting conditions. If the pressure is above the transition pressure or if solid conduction dominates, then thermal conduction will be pressure independent. The transition pressure is given as:

$$P_0=\frac{nk_{air}wT}{(w+h)d_{gap}v}$$

where n is the coefficient of extra conduction (~2) and v is the mean free path of the gas. Minimum detectable pressure occurs at the pressure at which solid conduction dominates gaseous conduction.

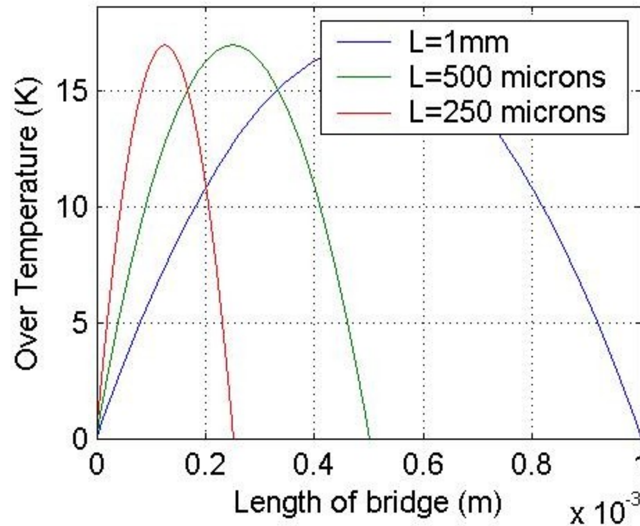

Figure 13: Temperature Distribution in Resistively Heated Microbridge Design

In order to maximize performance, three parameters must be optimized: the cross section of the heating element, the length of the element, and the air gap spacing. Decreasing the cross section or increasing the length of the bridge will give better low-pressure sensitivity, while decreasing the gap gives high-pressure sensitivity. However, the maximum length of the beam is strongly dependent upon the stress inside the poly layer. Each layer in SUMMIT V™ has a different amount of stress, although a general guideline is that the stress is compressive

and between 5-8 MPa. For doubly clamped beams under compressive stress, buckling will occur when the stress is:

$$\sigma_b = -\frac{\pi^2 h^2 E}{3L^2}$$

Figure 14 is a plot of buckling length versus intrinsic stress for poly1, poly2, and poly3. The thickness of the individual poly layers in SUMMIT V™ is given in Table 1. Table 2 gives interlayer spacing in the process. Beams may also deflect slightly before buckling. As such, long beams with narrow gaps may have limited sensitivity due to thermal shorting to the grounded case. There are a number of different sacrificial layers available in this process. To take into account beam warping, which varies from run to run, gauges were designed in several different layers.

Table 1: Poly Layer Thickness in SUMMIT V™

Layer	Thickness(μm)
Poly0	0.3
Poly1	1.0
Poly2	1.5
Poly3	2.25
Poly4	2.25

Table 2: Oxide Layer Thickness in SUMMIT V™

Layer	Gap Spacing(μm)
SacOx1	2.0
Dimp1	1.5
SacOx2	0.3
SacOx3	2.0
Dimp3	0.4
SacOx4	2.0
Dimp4	0.2

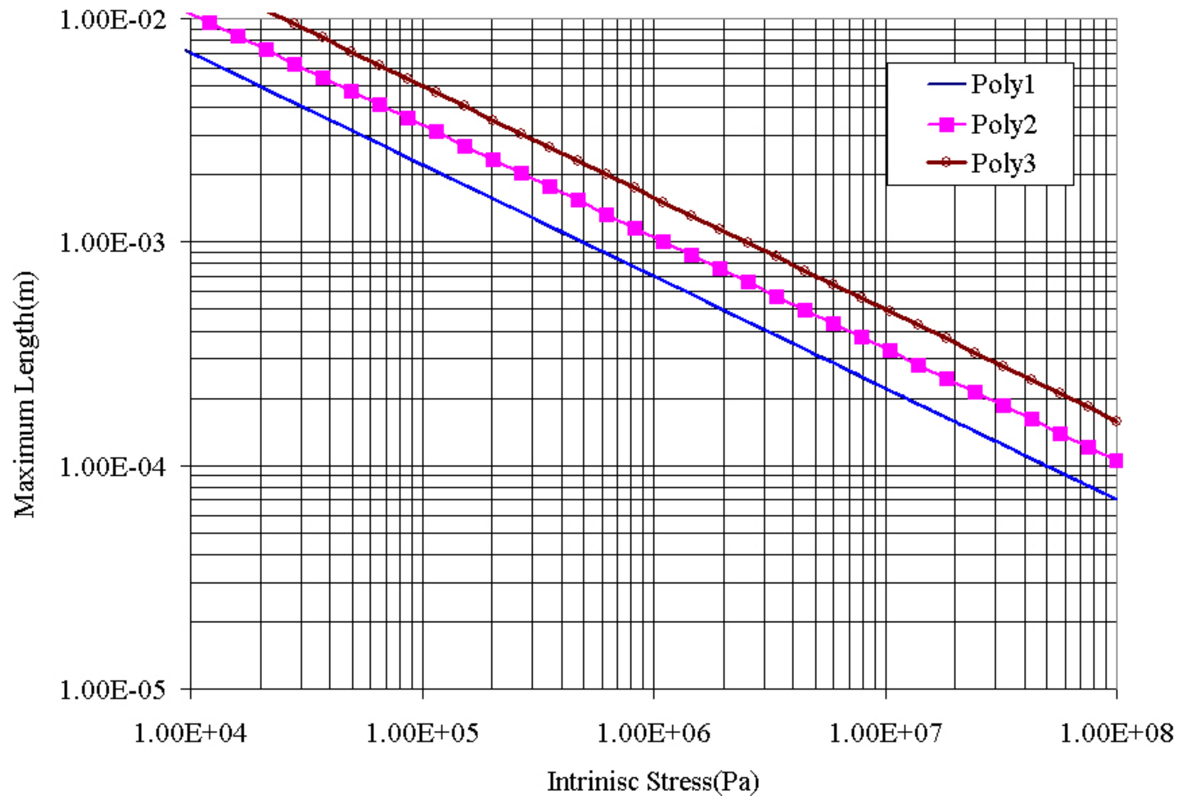

Figure 14: Maximum length beams in each Layer

As shown in figure 14 beam lengths larger than 1mm are likely to buckle and fail. So the maximum designed beam length is set at 1000 μm. Beams are designed at lengths of 1000, 750, 500, 250, and 150 μm. Performance is improved by shrinking beam widths as much as possible. Beam thickness, as the smallest dimension in the cross-section, will be limiting in terms of buckling. As such, beam widths are minimized (4 μm) to improve performance. The SUMMIT V™ process determines all other device parameters. Nine different designs are implemented to give the Pirani gauges the maximum performance opportunity.

Table 3 describes the different gauge designs. Figure 15 shows the cross sections of different designs.

A MATLAB script has been written to simulate the performance of the Pirani gauges. The nine designs are entered into the model. Figure 16 shows the maximum detectable pressure as a function of beam length and design while Figure 17 shows the minimum detectable pressure as a function of design. Figure 18 shows the predicted responses of a number of designs to pressure change. Both a single design at different length and all nine designs at the same length are plotted in the figure.

Table 3: Different Pirani gauge designs implemented

Design Number	Poly Level	Bottom Spacing	Top Spacing
1	1	Dimple1 (0.5μm)	SacOx2 (0.3μm)
2	1	Dimple1 (0.5μm)	None
3	1	SacOx1 (2.0μm)	SacOx2 (0.3μm)
4	1	SacOx1 (2.0μm)	None
5	2	SacOx2 (0.3μm)	Dimlpe3 (0.4μm)
6	2	SacOx2 (0.3μm)	None
7	2	SacOx1+SacOx2 (2.3μm)	None
8	3	SacOx3 (2.0μm)	SacOx4(2.0μm)
9	3	SacOx1,2,3 (4.3μm)	None

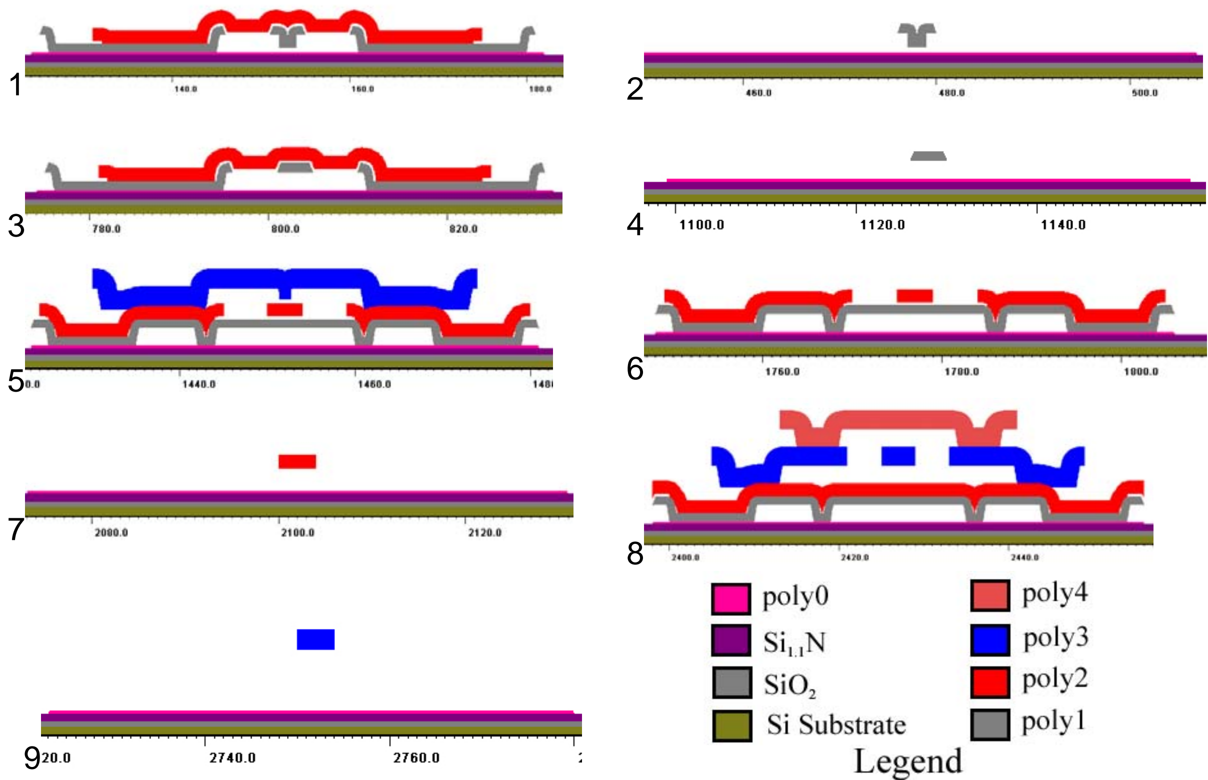

Figure 15: Cross Sections of Pirani Gauge Designs

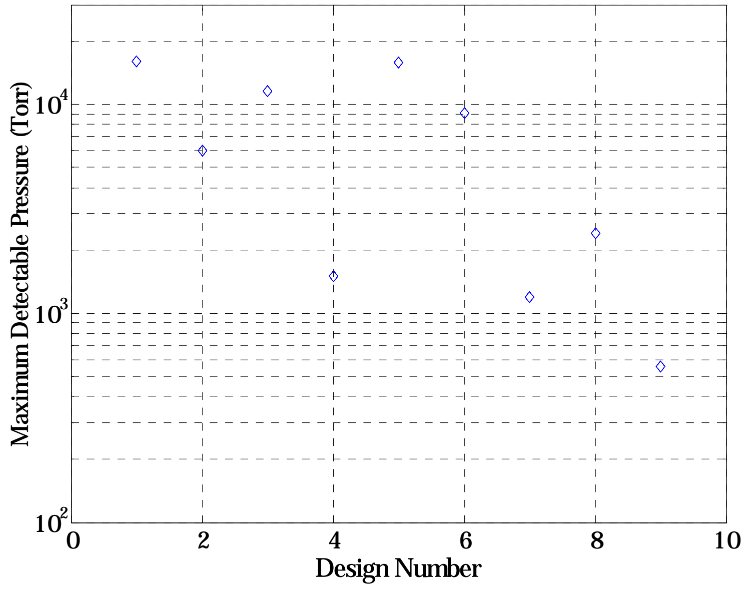

Figure 16: Maximum Detectable Pressure as a function of design number

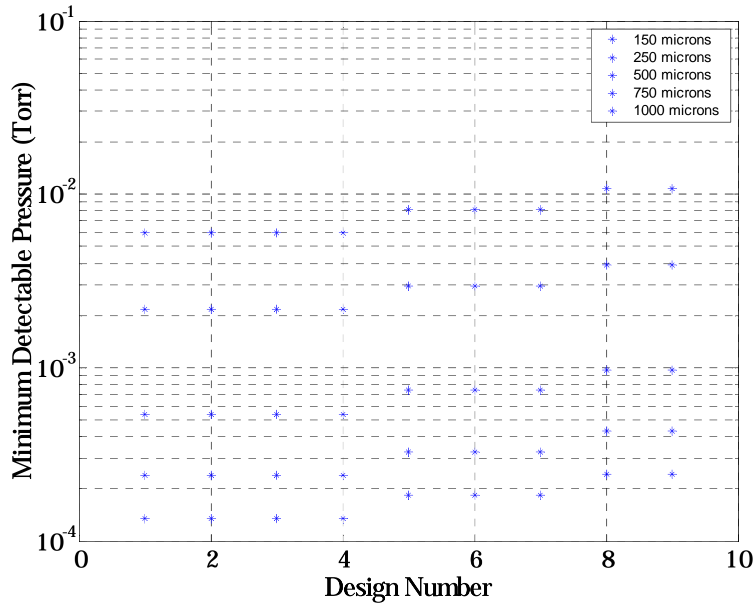

Figure 17: Minimum Detectable Pressure as a function of design number

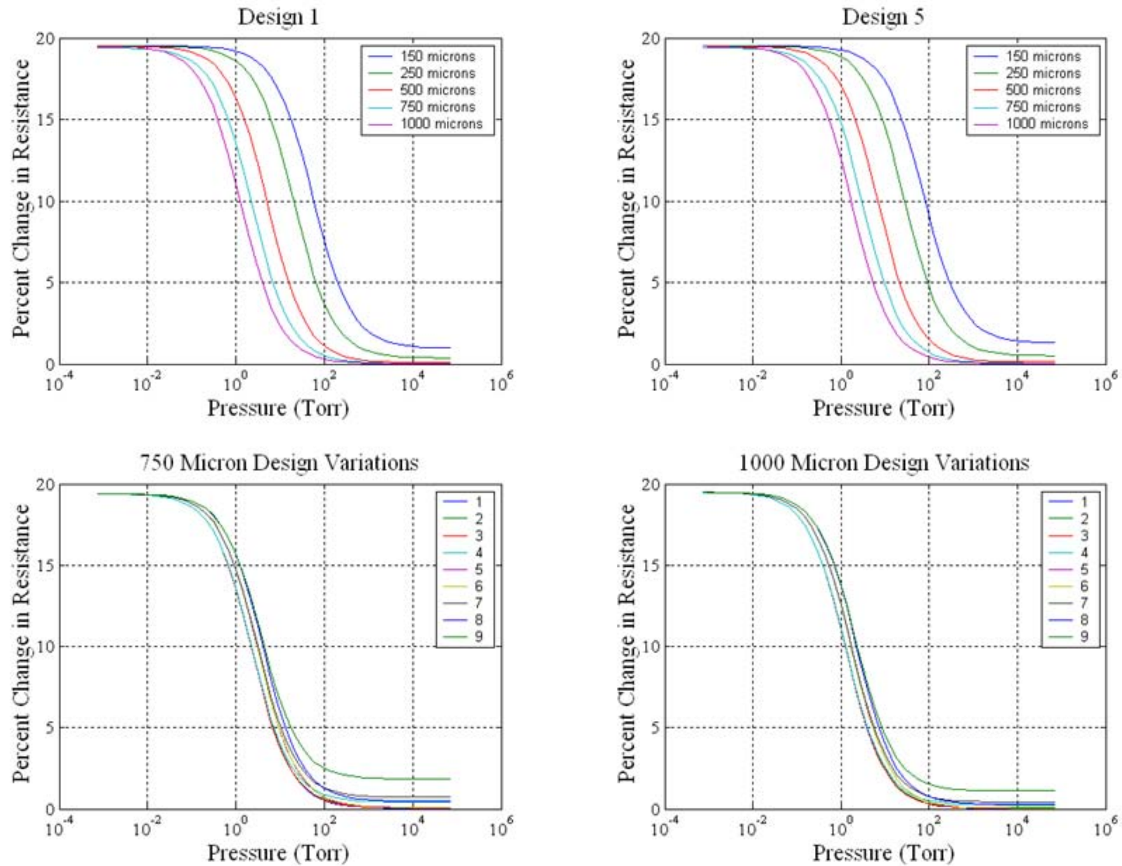

Figure 18: Predicted Response of various designs to pressure changes

Experimental Pirani Gauge Results

Recently, the Pirani gauges have been tested at the University of Michigan and we are including those results here. The devices were fabricated in the SUMMiT V™ process at Sandia National Laboratories on reticle set 416 module 8. To obtain the TCR, we initially tested each device and plotted the resistance vs. temperature. From this plot, we obtained the slope and the intercept and from the slope over the intercept we calculated the TCR. The TCRs for each device are shown in Table 3. The Pirani gauges are characterized with the system shown in Figure 19.

Table 4 TCR of Each Device

	TCR [ppm/°C]	Structural layer
Device #1	1.22×10^3	Poly 1
Device #2	1.30×10^3	Poly 1
Device #3	1.23×10^3	Poly 1
Device #4	1.26×10^3	Poly 1
Device #5	0.77×10^3	Poly 2
Device #6	0.59×10^3	Poly 2
Device #7	0.59×10^3	Poly 2
Device #8	1.33×10^3	Poly 3
Device #9	1.28×10^3	Poly 3

The existing setup uses a program in LabView to control a current source (Keithley 225A) and read voltage measurements off of a HP 34401A DVM, via GPIB. Initially, the thermal impedance extractor passes a small current through the device and measures the voltage (four point probe measurement). This four point probe measurement is used to set the R0. After this is set, the program continuously makes 4 point probe measurements while increasing the current each time. When the program reaches a certain temperature, the program will stop and calculate the thermal impedance. The way the program calculates the thermal impedance is by taking the voltage and dividing it by the current to determine the resistance of the device. The resistance is subsequently converted into a temperature value by multiplying by the TCR. The program will then plot the change in temperature against the change in power. From this graph, we are able to determine the line of best fit for our data, and the slope of this line is the thermal impedance. The thermal impedance varies from 1000K/W at atmospheric pressure to more than 320,000K/W at 10mTorr.

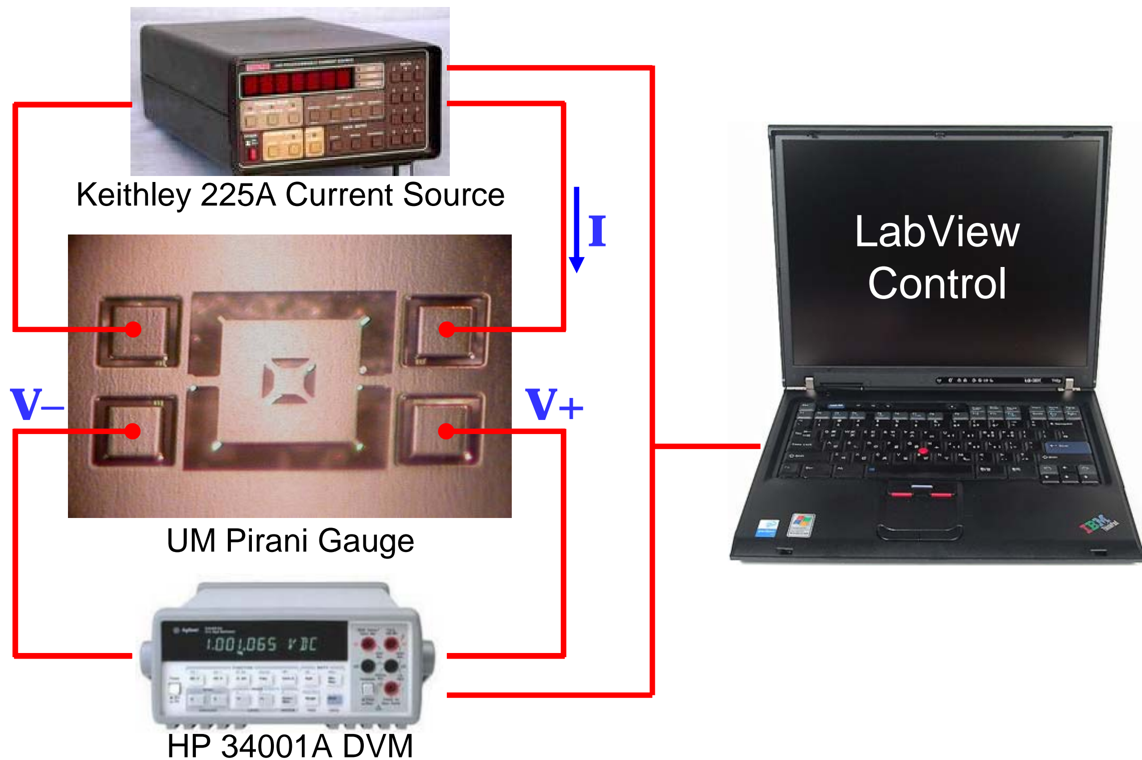

Figure 13: Setup Used to Test Pirani Gauges

Initially, the 9 different designs were tested in the 250 µm length only. This length was chosen because there would be enough sensitivity to observe the change in thermal impedance against pressure, and also the beam is short enough that stiction is not a problem. Figure 20 shows the plots of thermal impedance against pressure of all the different designs.

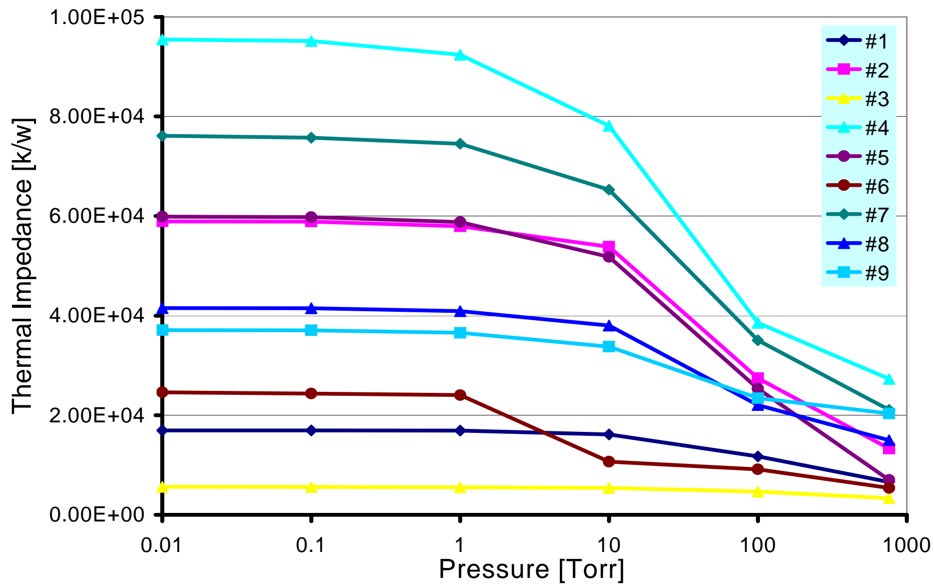

Figure 14: Thermal Impedance Vs. Pressure 250 µm Beams

After testing all the different designs, a conservative design and an aggressive design were chosen, and different lengths were tested. Design number 9 was chosen as the conservative design. This design is the most conservative design of the group, with the largest air-gap spacing. Figures 21 shows the results of testing device #9. Design number 1 was chosen for the aggressive design. This design has both top and bottom heat sinks and the air-gap spacing is very small. Figure 22 shows the results of this testing.

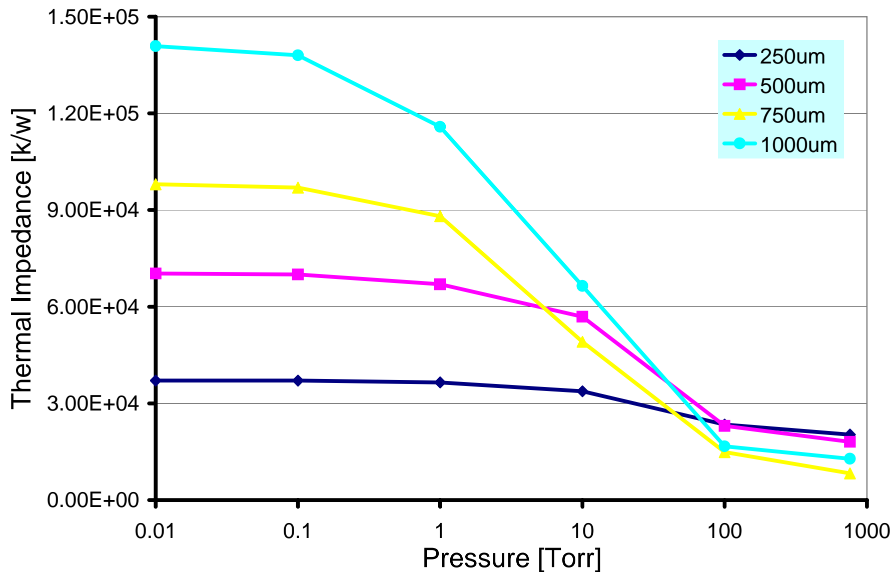

Figure 15: Device #9 Thermal Impedance Vs. Pressure for Different Lengths

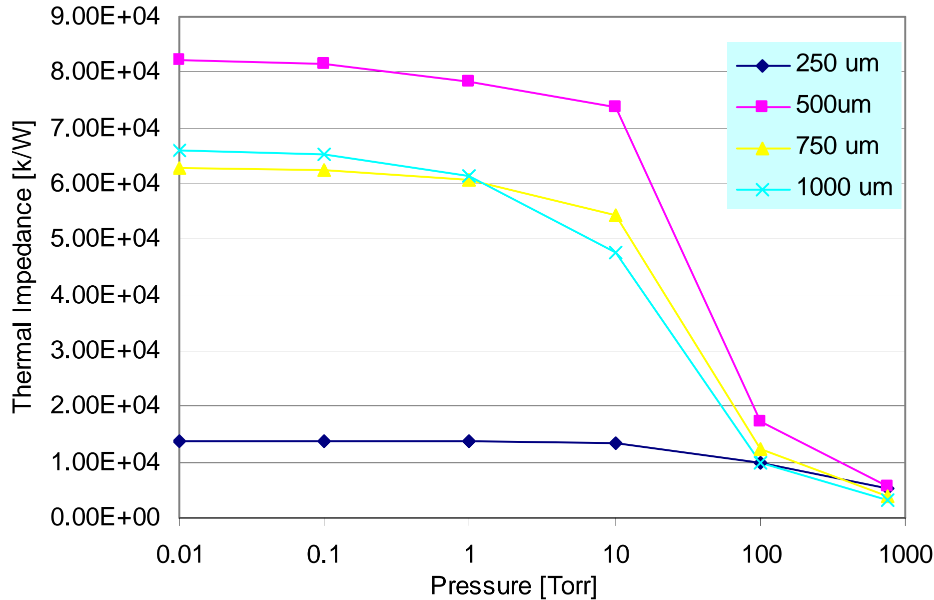

Figure 16: Device #1 Thermal Impedance vs. Pressure for Different Lengths

Discussion of Pirani Gauges

Overall, it appears that when comparing all the designs directly at 250μm length, there are no benefits to the top heat sink. Rather, it seems that the more aggressive designs demonstrated worse performance than the more conservative designs. One possibility for this is that the top casing that is supposed to help to dissipate heat is actually causing the heat to be trapped inside the casing.

When a very conservative design (design 9) was tested for all the different lengths, the longer lengths were much more sensitive than the shorter lengths. As shown in figure 21 the 1000μm device was more than one order of magnitude more sensitive than the 250μm device. Oddly, during testing, the more aggressive design (design 1) at longer lengths performed worse than the medium-length devices. This is most likely because the devices shorted to the thermally-grounded casing as they were heated. This caused the performance of the device to be decreased. Therefore in figure 22 the 750 and the 1000 μm devices did not perform as well as the 500 μm devices. In less aggressive designs with a greater top and bottom spacing, it is reasonable to predict that this problem will not be present.

Most of the Pirani gauges fabricated in the SUMMIT V^{TM} have been tested and characterized. The test data demonstrates that the thermally grounded casing on the top and bottom had very little effect on the devices, and in some cases actually hurt performance. In testing the different lengths, conservative devices with no grounded casing performed better for different lengths, while aggressive

designs with small gaps and thermally-grounded casing did not exhibit this trend. This is most likely because the beam deflected and shorted to the casing. Future work on this area includes testing other designs that are neither aggressive nor conservative in order to gauge their performance.

Conclusions

This report describes work done at the University of Michigan on micropackages and Pirani gauges as part of an LDRD funded university fellowship. The packages have been demonstrated to be hermetic with a base pressure of 1.5 Torr. The Pirani gauges have a measured sensitivity below 10 mTorr.

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