R146-05

Breaking Barriers to Low-Cost Modular Inverter Production & Use

Final Report

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Abstract:

The goal of this cost share contract is to advance key technologies to reduce size, weight and cost while enhancing performance and reliability of Modular Inverter Product for Distributed Energy Resources (DER). Efforts address technology development to meet technical needs of DER market protection, isolation, reliability, and quality. Program activities build on SatCon Technology Corporation inverter experience (e.g., AIPM, Starsine, PowerGate) for Photovoltaic, Fuel Cell, Energy Storage applications. Efforts focused four technical areas, Capacitors, Cooling, Voltage Sensing and Control of Parallel Inverters. Capacitor efforts developed a hybrid capacitor approach for conditioning SatCon's AIPM unit supply voltages by incorporating several types and sizes to store energy and filter at high, medium and low frequencies while minimizing parasitics (ESR and ESL). Cooling efforts converted the liquid cooled AIPM module to an air-cooled unit using augmented fin, impingement flow cooling. Voltage sensing efforts successfully modified the existing AIPM sensor board to allow several, application dependent configurations and enabling voltage sensor galvanic isolation. Parallel inverter control efforts realized a reliable technique to control individual inverters, connected in a parallel configuration, without a communication link. Individual inverter currents, AC and DC, were balanced in the paralleled modules by introducing a delay to the individual PWM gate pulses. The load current sharing is robust and independent of load types (i.e., linear and nonlinear, resistive and/or inductive). It is a simple yet powerful method for paralleling both individual devices dramatically improves reliability and fault tolerance of parallel inverter power systems. A patent application has been made based on this control technology.

Table of Contents

1. Introduction……………………………………………………………………..5
2. Executive Summary…………………………………………………………7
3. Capacitor Improvements……………………………………………………… 8
   3.1 Capacitor Background…………………………………………………… 8
   3.2 DC Bus Capacitor Requirements…………………………………………...9
   3.3 Electrolytic Limitations……………………………………………………10
   3.4 Hybrid Capacitor……………………………………………………….... 10
   3.5 Advanced Capcitor Research……………………………………………… 13
   3.6 Modeling/Simulation………………………………………………… .14
   3.7 Hybrid Capacitor………………………………………………………… 26
4. Heat Sink……………………………………………………………………… 30
   4.1 Objective…………………………………………………………………… 30
   4.2 Finned heat sink reaserch,analysis and design……………………………… .30
   4.3 Performance Verification…………………………………………………. 42
   4.4 Conclusion…………………………………………………………………. 46
5. Voltage Sensing……………………………………………………………….. 47
   5.1 Objective……………………………………………………………….. 47
   5.2 Galvanic Isolation Design…………………………………………………. 48
   5.3 Galvanic Isolation Methods……………………………………………… .49
   5.4 Performance Verification………………………………………………… .51
   5.5 Testing Results……………………………………………………………..51
6. Parallel Inverter Control………………………………………………….. 55
   6.1 Objective………………………………………………………………... 55
   6.2 Overview of Control Systems……………………………………………... 57
   6.3 Utility Interconnected (Grid-Connect) System………………………………. 57
   6.4 Stand-Alone System……………………………………………………….. 58
   6.5 Smart Gate Drivers……………………………………………………….. 60
   6.6 Fuzzy Control of Smart Drivers ………………………………………………61
   6.7. Simulation and Realization of mart Gate Drivers……………………………..65
   6.8 Conclusions ……………………………………………………………...87
   7. Program Acheivements ……………………………………………………88
8. Future…………………………………………………………………………88
Appendix A: Final Presentation………………………………………………………89
Appendix B: Baseline AIPM Heat Sink Layout Drawings...………………………… 101

1. Introduction

The depletion of hydrocarbons as an automotive fuel source is motivating new technologies associated with higher fuel efficiency hybrid-electric and fuel cell vehicles. Key components for these advanced vehicles include motors, inverters/converters, sensors, control systems, and other interface electronics. A key enabler of these advanced electric vehicles is development of new inverter technologies. These new technologies must be compatible with high-volume manufacturing and must ensure

- High reliability
- High efficiency
- Ruggedness

While simultaneously reducing

- Cost
- Weight
- Volume

Modular power electronics, based on a standard building block, will enable large-scale production and offer expandability, reliability and maintainability. Several obstacles to realizing the potential of modular power electronics include

- Cooling (liquid very difficult)
- Paralleling
- Volume, weight, cost, reliability

The Goals and Metrics for an inverter of the future are summarized as follows:

- Specific power at peak load >12 kW/kg
- Volumetric power density >12 kW/l
- Cost <$5/kW peak
- Efficiency >97%
  (10-100% speed and 20% torque for drive from DOE)
  DOE Freedom Car Inverter Goals

Over the last five years, SatCon has developed and produced a wide variety of power inverters for applications ranging from 50 kW hybrid electric vehicles, to 300kW fuel cell inverters for distributed power, to 600 kW shipboard power systems. Throughout these developments SatCon's goal has been to reduce the size and weight of the systems, while making optimum use of modularity and component standardization in order to reduce cost, and improve reliability and maintainability. SatCon's Advanced Integrated Power Module (AIPM) inverter (***Figure 1.0-1***) is an example of an inverter designed to meet the low cost, high power dense, rugged environmental requirements of automotive hybrid-electric drive systems. The inverter occupies 6.3 liters, provides 30kW continuous 3-phase output power and peak power of 55kW with 70ºC coolant fluid, and in 100k production lots, which is expected to have a material cost just over $7/kW. The inverter contains integrated power conditioning and DSP control, whereby a torque command input across the CAN bus will result in a 3-phase current and voltage output to a motor load. The cost includes bulk capacitance and bus bar assemblies that are integrated into the unit, reducing the end user's design and integration time.

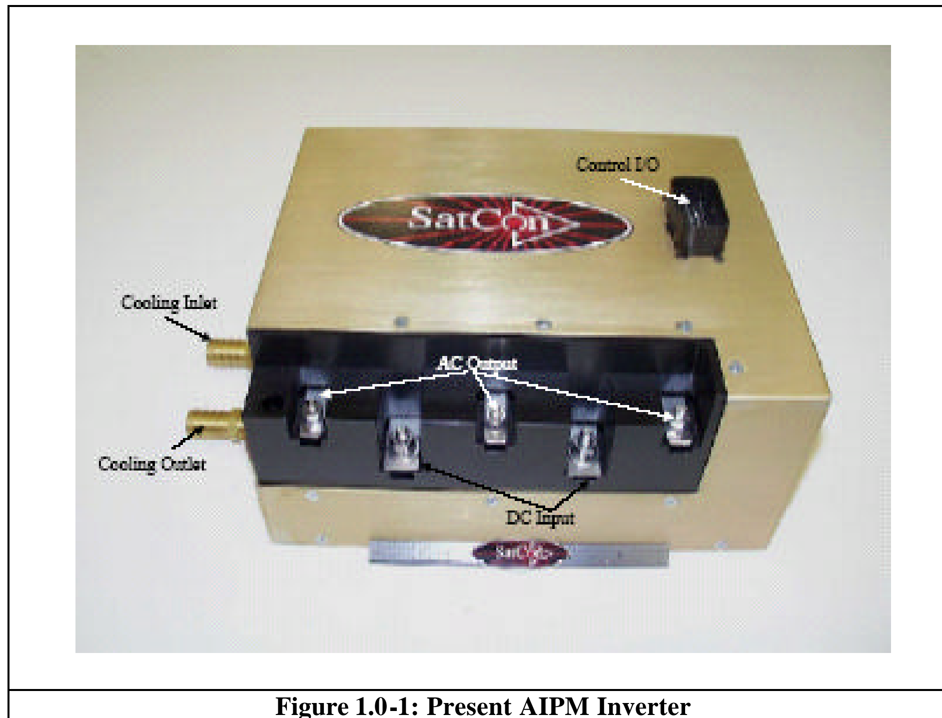


Figure 1.0-1: Present AIPM Inverter

Although this AIPM module is state-of-the-art with regard to packaging density and design for low-cost manufacturability, SatCon believes that by addressing key commercial component technologies and by expanding the markets for such devices, even further improvements can be realized. SatCon utilized the AIPM module as a test platform to investigate improvements, components, and the system design to reduce weight/volume, improve reliability, and fault tolerance. SatCon extended the application of this modular technology to a wider range of markets including our StarSine product.

The four tasks that have been investigated and reported in this report are:

- Improvements to Aluminum electrolytic Bulk Filter Capacitors
- Air Cooling
- Voltage Sensing for Parallel Module Operation
- Fault Tolerant Control for Parallel Modules

Each of these tasks are described in separate sections, followed by overall program achievements and summary recommendations for future work.

2. Executive Summary:

The goal of this cost share contract is to advance key technologies to reduce size, weight and cost while enhancing performance and reliability of Modular Inverter Product for Distributed Energy Resources (DER). Efforts address technology development to meet technical needs of DER market protection, isolation, reliability, and quality. Program activities build on SatCon Technology Corporation inverter experience (e.g., AIPM, Starsine, PowerGate) for Photovoltaic, Fuel Cell, Energy Storage applications. Efforts focused four technical areas:

- Capacitors
- Cooling
- Voltage Sensing
- Control of Parallel Inverters

Capacitor efforts developed a hybrid capacitor approach for conditioning SatCon's AIPM unit supply voltages by incorporating several types and sizes to store energy and filter at high, medium and low frequencies while minimizing parasitics (ESR and ESL).

Cooling efforts converted the liquid cooled AIPM module to an air-cooled unit using augmented fin, impingement flow cooling. The goal of this effort was to eliminate the need for liquid cooling and to demonstrate the performance using SatCon's AIPM module, with a goal of maintaining a peak power output of at least 35 to 40 kW and without increasing the module's footprint. An "augmented surface bonded fin heat-sink" replaced the AIPM liquid-cooled heat sink to accomplish the objective. The "augmented surface bonded fin heat-sink" fin dimensions were optimized for heat transfer in the AIPM application. Thermal modeling supported the optimum fin dimensions and spacing selection. Based on the optimized geometry and commercially viable heat sinks, a COTS heat-sink was identified, purchased, integrated and thermally tested, verifying the predicted performance.

Voltage sensing efforts successfully modified the existing HEV AIPM sensor board to allow several, application dependent configurations, including Distributed Generation (DG) applications. This was made possible by adding voltage sensor galvanic isolation. In DG applications, power-to-control isolation is a critical parameter in meeting UL and NEC requirements for grid operation. In HEV designs, galvanic isolation is normally not required for the voltage sensing system. The HEV application uses a single inverter for each load; therefore, the decrease in power-to-control isolation, caused by paralleled inverters in DG applications, is not an issue. Likewise, voltage sense signals do not extend beyond the boundaries of the inverter I/O, therefore, galvanic isolation is not necessary to meet conducted emissions requirements. In a distributed generation application, which utilizes a "standardized" inverter module, parallel operation will be required to provide the range of output power levels from 30kW to 500kW.

Parallel inverter control efforts realized a reliable technique to control individual inverters, connected in a parallel configuration, without a communication link. The control of individual inverters needed to be based solely on the information that is locally

available at the inverter. In practical distributed power systems, large physical distances between inverters makes a communication link tying the local controllers together impractical. Depending on the location of individual units or modules, the level of communication sophistication needs to degrade with distance. At physically disjoint units, the inverter control needs to be based only on terminal quantities (voltage, current). Individual inverter currents, AC and DC, were balanced in the paralleled modules by introducing a delay to the individual PWM gate pulses. The load current sharing is robust and independent of load types (i.e., linear and nonlinear, resistive and/or inductive). It is a simple yet powerful method for paralleling both individual devices dramatically improves reliability and fault tolerance of parallel inverter power systems. A patent application has been made based on this control technology

3. Capacitor Improvements

3.1. Capacitor Background

One element of this program is to address the issue of the DC BUS capacitance, aiming to improve the inverter performance without increasing cost. The original proposal had put forward the idea of improving the interconnection of electrolytic capacitors (***Figure 2.1-1***) to reduce the device parasitic inductance and resistance. We subsequently determined that this approach would not be of significant benefit, because lead inductance dominates (ESL), so paralleling leads to reduce ESR would not change the total impedance. Instead, we focused on meeting the goals by utilization of a hybrid capacitor in place of the existing electrolytic. Power Electronic practitioners do, de facto, use a hybrid approach today; they parallel bulk capacitors with high-frequency capacitors and place small snubber capacitors close to the switching devices to reduce device stresses. This part of the converter design process, however, lacks a systematic (and ultimately analytic) approach to the implementation of this hybrid capacitor. The DOE Inverter Roadmap has identified this issue. A consistent approach to hybrid capacitors could easily lead to an Industry Standard hybrid-capacitor package, which would become a standard device, and could achieve the economies of scale needed to drive the total price down to something considerably less than the sum of the parts. Coincidentally, the DOE and NREL have also recognized this need and published a roadmap for Inverter Electronics calling for work on Hybrid Capacitors while we were working on this program.[1]

[1] nrel.gov/ **vehicle**sandfuels/ power**electronics**/pdfs/**roadmap**

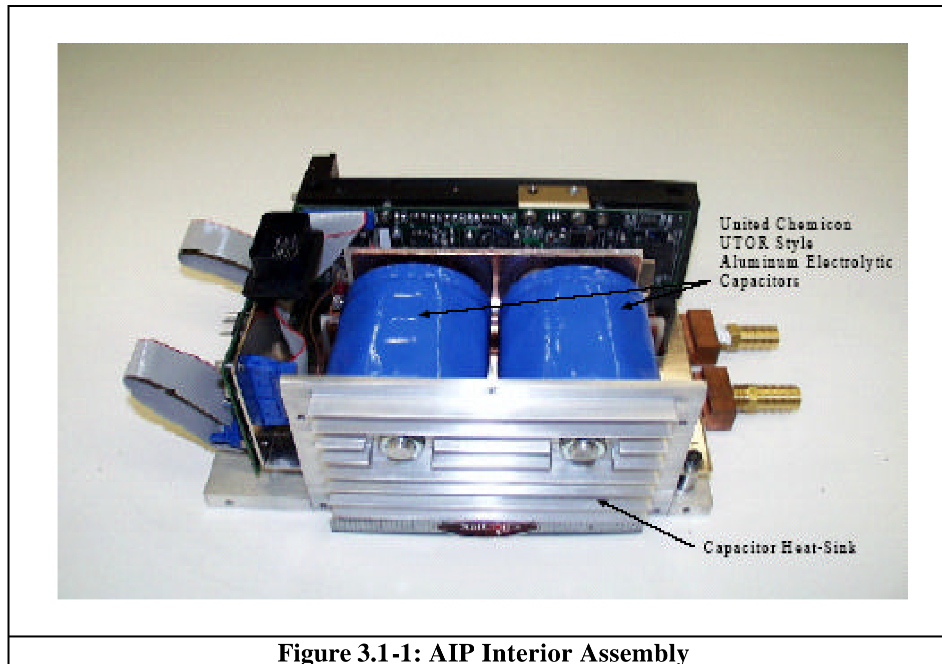


Figure 3.1-1: AIP Interior Assembly

3.2. DC Bus Capacitor Requirements

The DC Bus capacitor in an inverter provides three distinct functions:

1. Bulk Energy Storage (low frequency, load surge, harmonics of fundamentals due to imbalance)
2. A path for Hi-Frequency ripple current (switching frequency)
3. Another path for Very Hi-Frequency switching current (switching transients)

Capacitors come in different flavors but the technologies are broadly dividable into Electrolytic, Film and Ceramic. The most obvious metrics used to compare the technologies are the volumetric density of capacitance (and therefore stored energy) and per unit cost. The total amount of Bulk Energy Storage required is generally dictated by system considerations, particularly the effect of major load transients on the external high-voltage Bus (for a DC input single stage inverter). At the same time the capacitor, of a given technology, has parasitics that affect its ability to perform the second and third functions listed above.

Whenever current flows through the capacitor there is loss due to series resistance, ESR. When the current flowing changes, there is a voltage drop associated with the series inductance, ESL. A simple view of an inverter leg, showing the capacitor, is shown in ***Figure 32-1***. Here the total loop inductance is labeled L_{σ}, this is the sum of the parasitic inductances of the capacitor, the interconnecting bus work and the IGBT module. In general, the capacitor will contribute half of the parasitic inductance, which is typically on the order of 30-50 nH for a 50kW level inverter. The direct effect of the loop inductance is device over-voltage stress in the inverter leg.

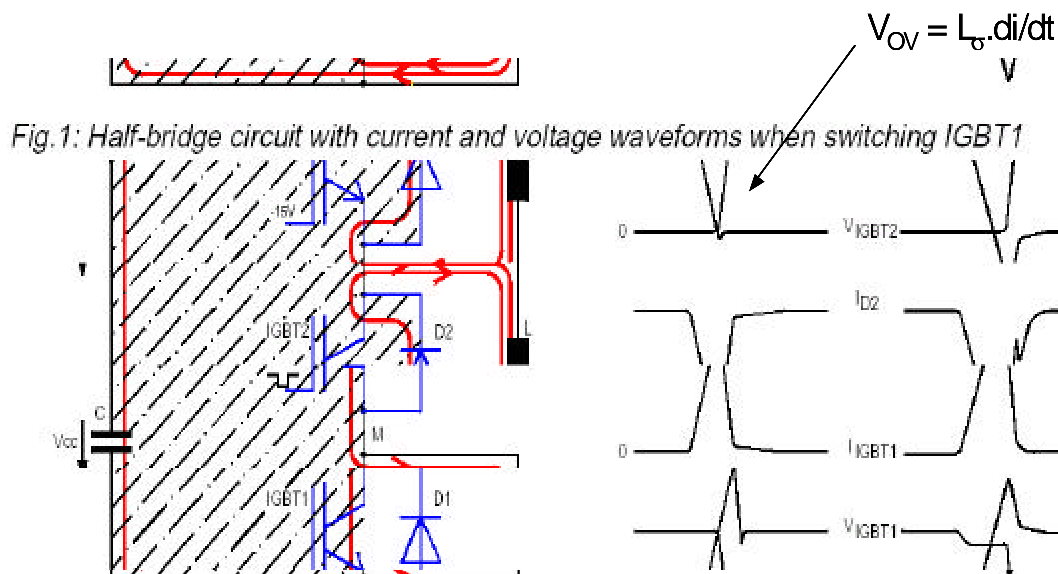


Figure 3.2-1: Loop Inductance for Inverter Leg

3.3. Electrolytic Limitations

While the Aluminum electrolytic capacitor has good volumetric efficiency, the very nature of electrolytic leads to a moderate level of ESR and ESL. The high value of capacitance is achieved through the very large surface area that comes from the etched surface of the Aluminum electrode. The resistance is attributable to the conducting electrolyte, which acts as the other electrode. The other parasitic of the electrolytic capacitor, inductance, is moderate to high due to the rolled foil construction and the large discrete terminals and ribbon interconnect. It is possible to reduce the inductance of the capacitor element through strip-line style termination, increased and planar interconnection to the spiral winding. The ESR is a function of the electrolyte and we believe can be reduced by a factor of approximately two. Considerable work has focused on gel types of electrolyte to create a "dry" electrolytic capacitor. This work may yield high conductivity of the electrolyte, but it will not be the primary focus of this work.

While any reduction in the parasitics is a good thing, one must beware of diminishing returns. An electrolytic with particularly low ESL is of limited value if the ESR is much higher than a much smaller ceramic that is placed in parallel. Of course the other limitation of the electrolytic is the poor lifetime and operating temperature range, which is motivating considerable work on bulk ceramics as described below.

3.4. Hybrid Capacitor

Many researchers have studied the trade-offs associated with Energy Storage, ESR and ESL and come to the conclusion that no one capacitor technology can win in all of these areas. While ceramics might seem to address all of these areas there are real problems in making large ceramics due to the brittleness of the material and the tendency for micro-cracks to form and propagate. The solution appears to be a hybrid approach combining all three technologies. What is lacking, which the DOE has recognized, is a systematic approach to determining the correct ratio and configuration of the capacitor elements. What we believe to be the solution is a combination of Electrolytic and Film for the low and medium frequency capacitor and a small amount of ceramic located proximally to the switching devices themselves to achieve the low high-frequency impedance. This should come as no surprise as most power electronic designers use a combination of at least two

of the three technologies as a standard. We are suggesting that all three should be employed for an optimized solution.

3.5. Advanced Capacitor Research

Considerable research is being focused on Power Electronic Capacitors, and particularly the DC Bus Capacitor. We show a comparison of the state-of-the-art in ***Table 2.5-1***. Much work is being done on high-temperature dielectrics, such as diamond-like-film, which uses graphite like film. Other high-temperature dielectrics include glass at 400°C and Metalized Teflon at 300°C. Just as with high-temperature magnetics there is a fundamental problem with the packaging of the element with insulation materials typically operating at 250°C and below.

Similarly, work is being done on hardening ceramic capacitors, with very good results coming from the inclusion of glass into the ceramic. Also, a special class of capacitor is being developed to have much higher energy density than polymer film capacitors based on bi-axially oriented polypropylene (BOPP, 1 – 2 J/cc) and ceramic capacitors based on $BaTiO_3$ (0.1 J/cc). Composite dielectrics of glass and anti-ferroelectric ceramics have been demonstrated with reliable energy densities in excess of 10 J/cc. This is a potential break through in capacitor technology and promises to dramatically reduce the size of power circuits.

Table 2.5-1: High-Voltage BUS Capacitors

Capacitor Type	Capacitance (uF)	Rated Voltage (VDC)	Energy Density (J/m^3)	Ripple Current (A rms)	ESR (mΩ)	Temperature Range (°C)
"Objective" HV BUS Capacitor	200 -- 250	400 -- 525	1.95×10^5	90	3	-40 to +85
Wound Polymer	230 ± 10%	500	8.01×10^4	48 (25°C) 21(75°C)	4.5	-55 to +85
Multilayer Ceramic	225 ± 10%	500	1.40×10^5	122 (25°C) 150(75°C)	3.4	-55 to +125
Aluminum Electrolytic	220	450	2.66×10^5	2.7 (85°C)	333	-40 to +105
Multilayer Polymer	240 ± 10%	400	1.16×10^4	353	0.25	-55o +105

Capacitors represent the second largest input to the cost of an inverter, and they also account for a major fraction of the volume and weight. For voltage levels below 450 V, motor inverters have predominately used aluminum electrolytic capacitors. Besides occupying about 60% of the volume of the inverter and a similar proportion of the weight, aluminum electrolytic capacitors cannot tolerate high temperatures, they tolerate very little ripple current, suffer from short lifetimes due to drying of the electrolyte, and when they fail, they sometimes do so catastrophically.

Polymer-film capacitors are used for voltages above 450 V. They have soft-breakdown (benign-failure) characteristics, and it appears that an affordable polymer-film capacitor can be manufactured with a volume about 40% of that of an equivalent aluminum electrolyte capacitor. However, polymer-film capacitors are more expensive than aluminum electrolytic capacitors for lower voltages, and they currently cannot tolerate sufficiently high temperatures for future applications.

Theoretically, ceramic capacitors have the greatest potential for volume reduction; they could be as small as 20% of the volume of an aluminum electrolytic capacitor. Ceramics offer high dielectric constants and breakdown fields and, therefore, high energy densities. They also can tolerate high temperatures with a low equivalent series resistance (ESR), enabling them to carry high ripple currents even at elevated temperatures, although the capacitance may vary strongly with temperature. There is a concern about the possibility of catastrophic electrical discharge and mechanical failure of ceramic capacitors. However, a technique similar to that used in polymer-film capacitors for ensuring benign failure has been developed, and at least two manufacturers have demonstrated graceful-failure of ceramic capacitors, although they have not yet been implemented into a product because there is no strong customer demand.
Until now, the EE Tech Team has treated the capacitor as an individual component. No one capacitor has been able to meet all the requirements of an automotive traction system. The solution for a traction application may come from using a combination of the capacitor types. A hybrid capacitor bank may be a solution that should be investigated. Treating the capacitor bank as a subsystem may yield the performance needed to make electric traction systems viable.

Anticipated requirements for a dc bus capacitor bank in 2010 are listed in ***Table 3.5-2***. The main technical targets for 2010 would be to reduce the weight, volume, and cost per micro Farad by a factor of 2.

Table 3.5-2. Desired DC Bus Capacitor Bank for Inverters

2010 Typical Capacitor Bank Requirements	
Capacitance, µF	2000+/- 10%
Voltage rating, VDC	600
Peak transient voltage for 50 ms	700
Leakage current at rated voltage, ma	1
Dissipation factor, %	<1
ESR, mohm	<3
ESL, nH	<20
Ripple current, amp rms	250
Temperature range of ambient air, ºC	-40 to +140
Weight requirement, kg	10.8

Volume requirement, l	0.4
Cost	$30
Failure mode	Benign
Life @80% rated voltage	>10,000 hr, 20 amps rms, +85°C

A qualitative summary of the advantages and disadvantages of the three types of capacitors is given in ***Table 3.5-3***.

Table 3.5-3. Qualitative Comparison of Candidate Technologies for Bus Capacitors

Parameter	Electrolytic	Polymer Film	Ceramic
Size, Weight	Poor	Good	Excellent
ESR	Marginal	Excellent	Excellent
Temp. Stability	Marginal	Good	Excellent
Reliability	Marginal	Excellent	Excellent
Ripple Current	Marginal	Good	Excellent
Failure Mode	Poor	Excellent	To be demonstrated
Cost	Excellent	Good	Poor

Because polymer-film capacitors and ceramic capacitors both have potential for large benefits but also face significant technical challenges, both technologies are being pursued. Recent research has produced polymer films with substantially higher temperature capabilities, but manufacturing problems have prevented the fabrication of large capacitors suitable for an inverter DC bus. The near-term emphasis is to solve those manufacturing problems, and longer-term efforts will be devoted to reductions in cost and further improvements in performance. The near-term emphasis for ceramic capacitors is to further demonstrate a design that will prevent catastrophic failures of thin-film capacitors based on ceramic ferroelectric materials, antiferroelectric/ferroelectric phase-switch ceramics, and glass ceramics. After benign failure modes are assured, future efforts will be devoted to material selection and processing methods to improve performance and reduce cost.

3.6. Modeling/Simulation

The issue of device-parasitcs is critically important, as we have said. We studied the effect of parastics on switching waveforms beginning with the simple switching cell of ***Figure 3.6-1***. In ***Figure 3.6-2*** we a simulated turn-off transition using a 15.7 nH loop inductance and an equivalent switch capacitance of 10 nF.

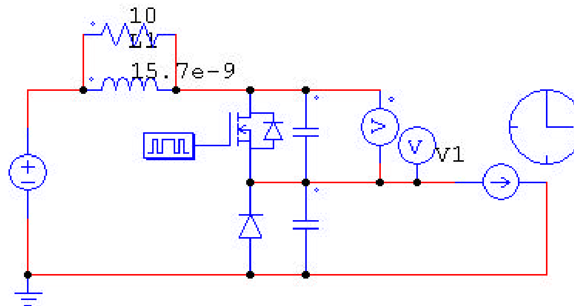


Figure 3.6-1: Simple Switching Cell

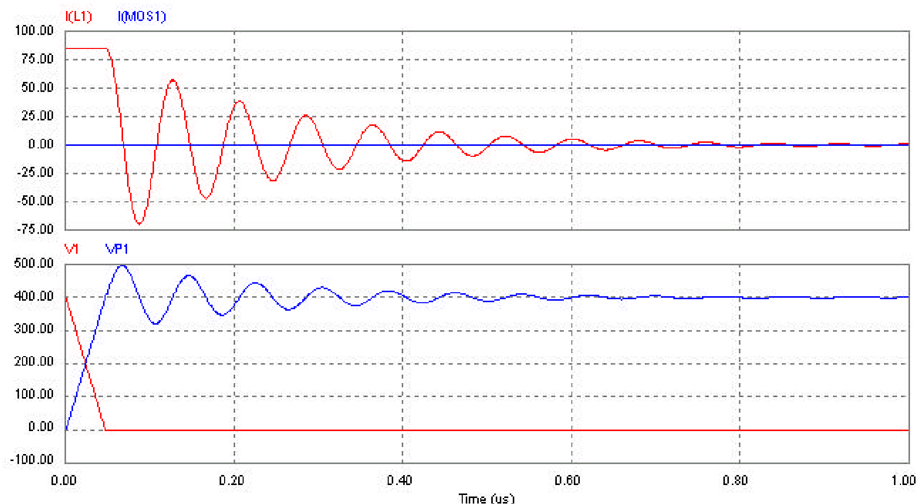


Figure 3.6-2: Turn-off Transition for IGBT

To see the effect of reducing the loop inductance to 10.7nH we ran the simulation for this condition with the result as shown in ***Figure*** . Note that the transient voltage is not reduced linearly (impedance goes as sqrt of L). To reduce the overvoltage transient by a factor of 2 we would need to reduce the inductance by a factor of 4.

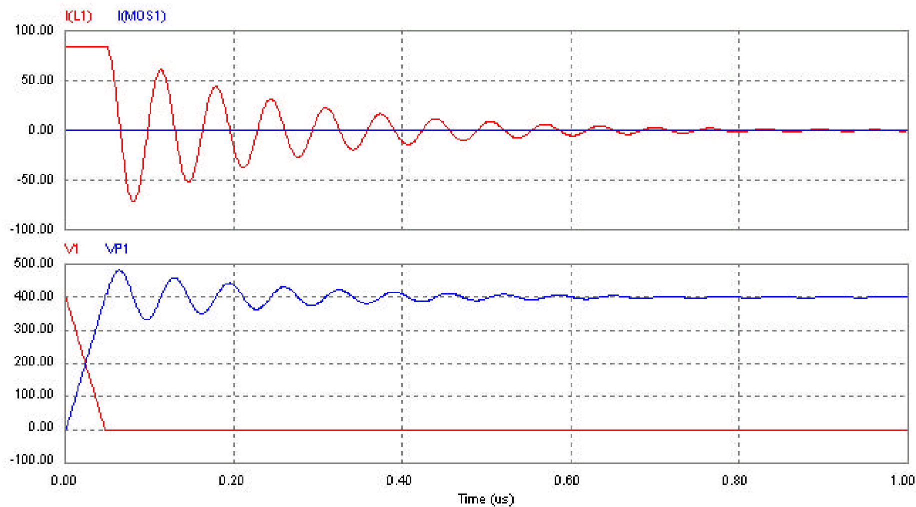


Figure 3.6-3: Turn-off with Reduced Loop Inductance

Now add a small by-pass capacitor near the main switching device, ***Figure 3.6-4***

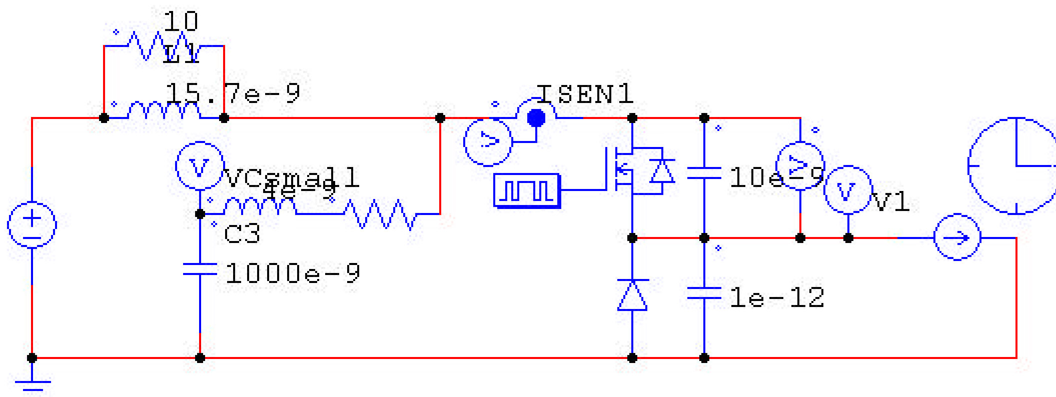


Figure 3.6-4: Switching Cell with small by-pass capacitor

With a bypass capacitor that is "large" compared to the device capacitance then can show that the effective inductance of the loop is now the inductance of this tight high-frequency loop.

So 4nH, 1uF for bypass capacitor (***Figure 3.6-5*** below)

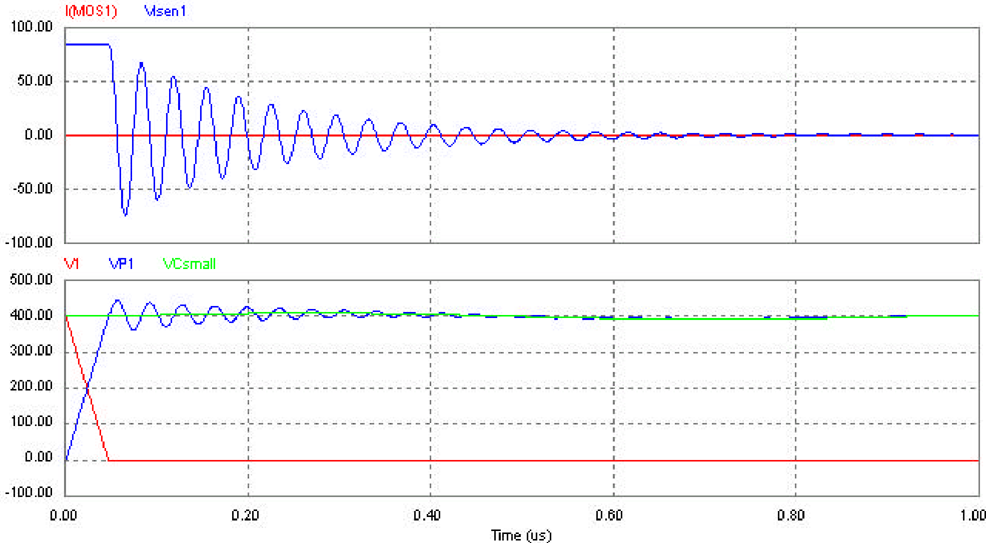


Figure 3.6-5

Now back off in size of bypass capacitor, 4nH, 0.1uF (***Figure 3.6-6*** below)

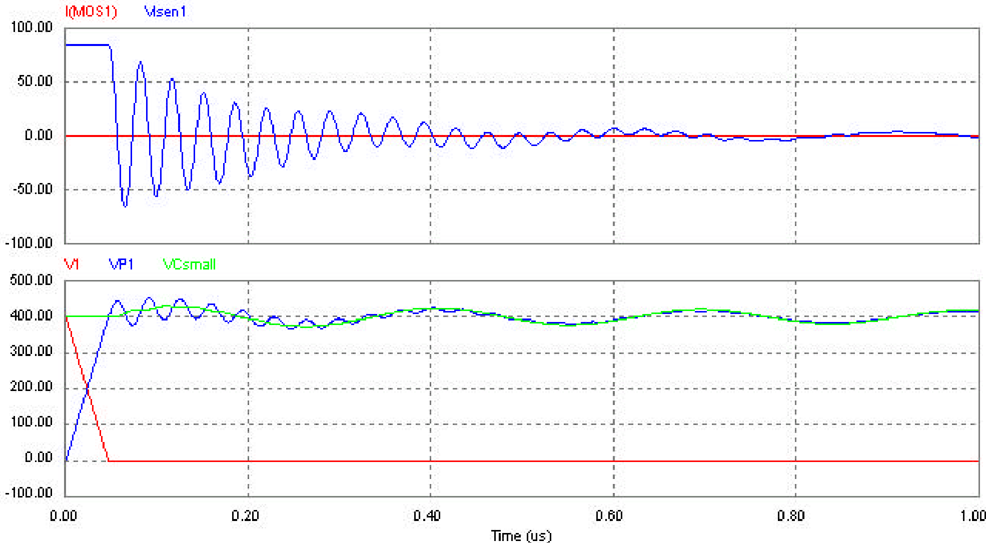


Figure 3.6-6

400nF, 4nH (***Figure 3.6-7*** below)

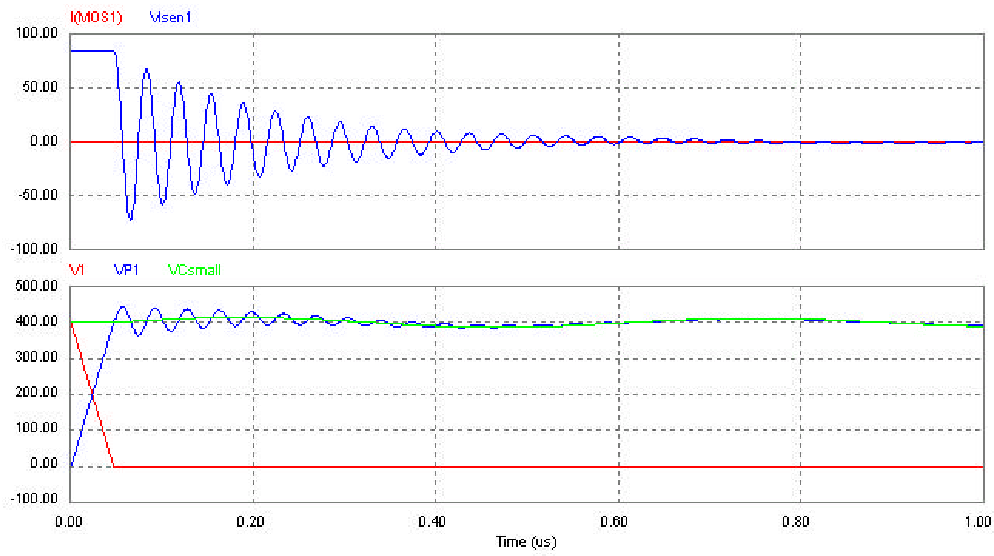


Figure 3.6-7

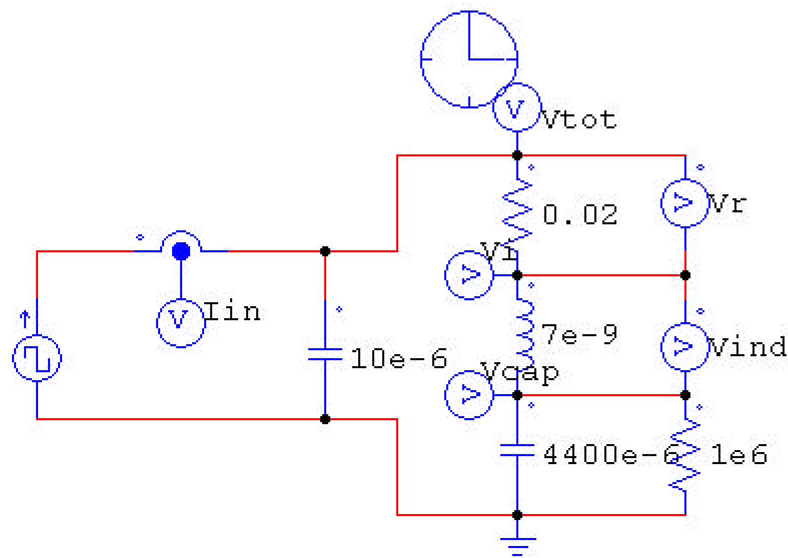


Figure 3.6-8

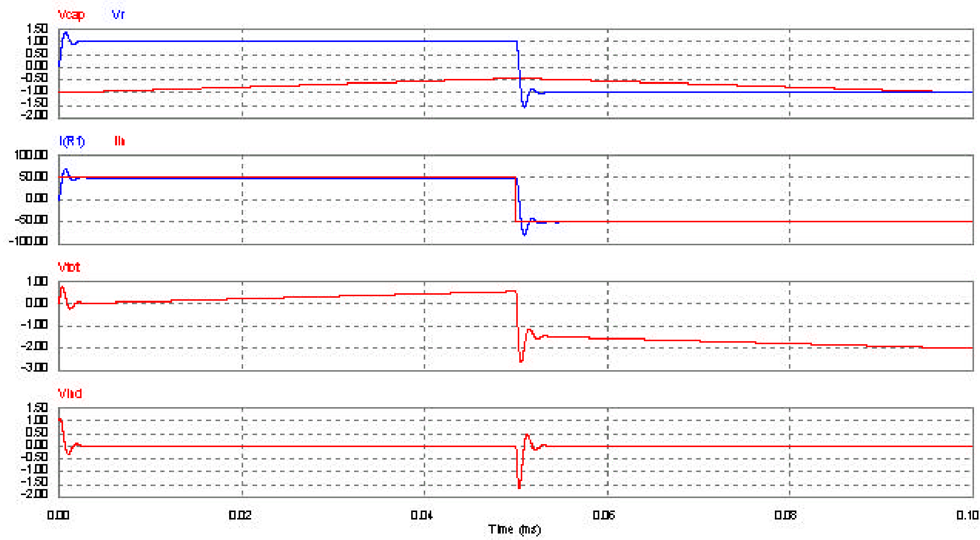


Figure 3.6-9

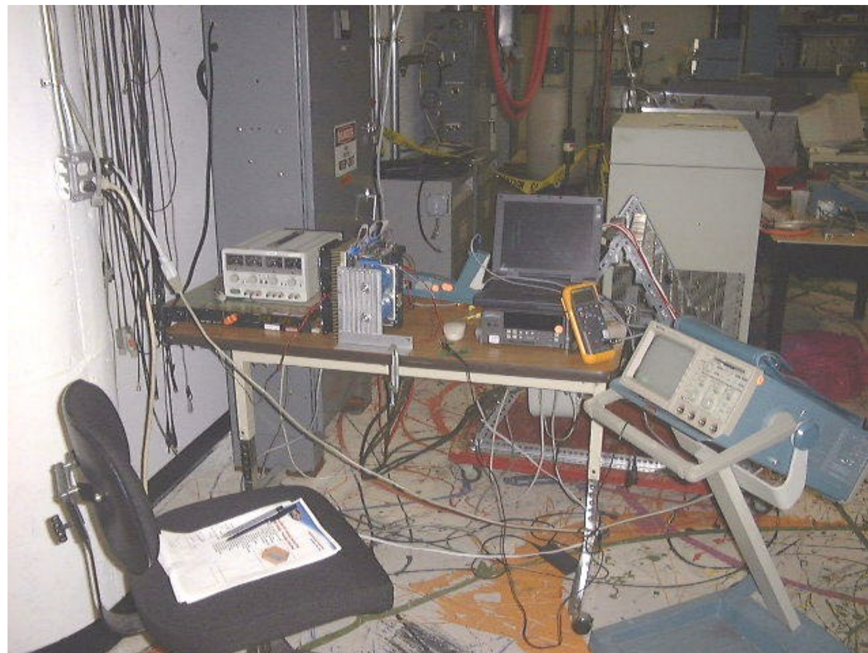


Figure 3.6-10: Switching Transient Test Setup - Air Cooled AIPM Unit

TDS420 Scope - TM 503A Current Probe - TEK 6112 100 mHz 10X Scope Lead

Rapid Power Supply

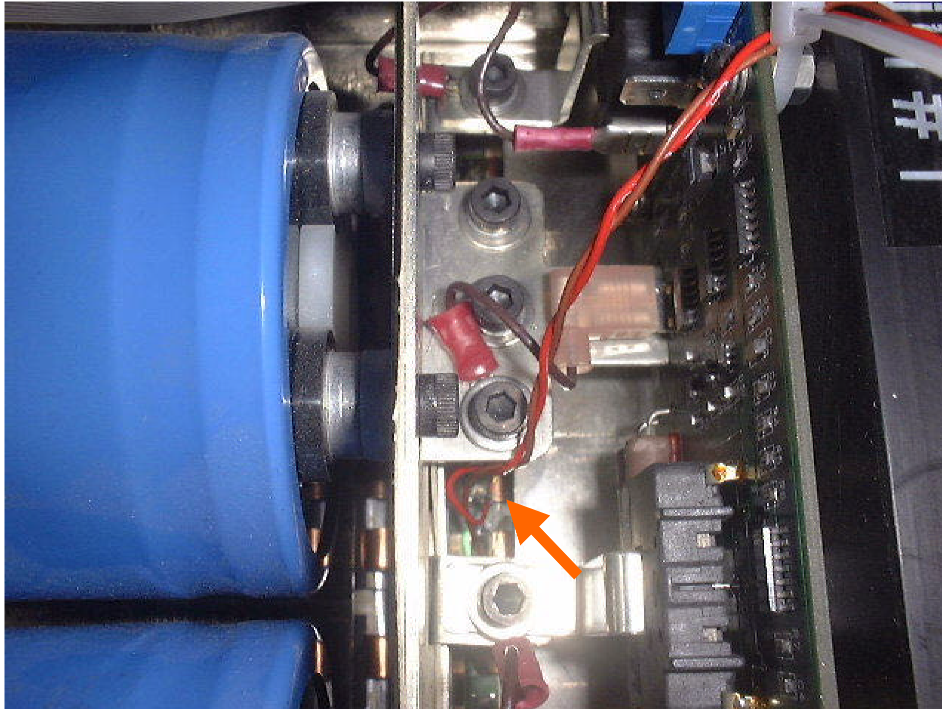


Figure 3.6-11: Voltage Probe Location

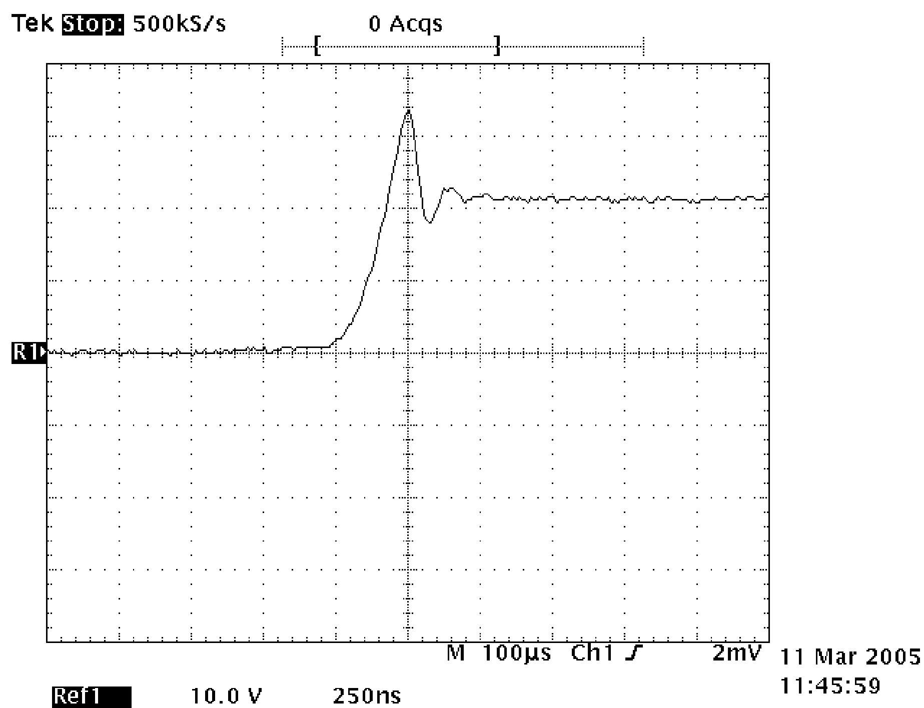


Figure 3.6-12: 200 V DC Bus - Voltage 10X Probe - 10V/Div = 100V/Div

Note the over voltage is approximately 130V with a DC bus voltage of 210V. The current meanwhile is shown below. This is the load current, not the switch current, which we measured with the voltage probe disconnected to permit a clean measurement. The di/dt of the load current is approximately 250A/2µs, or 125 A/us. The load current meanwhile commutates from the

IGBT to the Upper Diode. The total volt-seconds are approximately 130V x 75 ns and the current is 250 A, which gives us an estimate of the loop inductance, L_{σ}, of 39 nH.

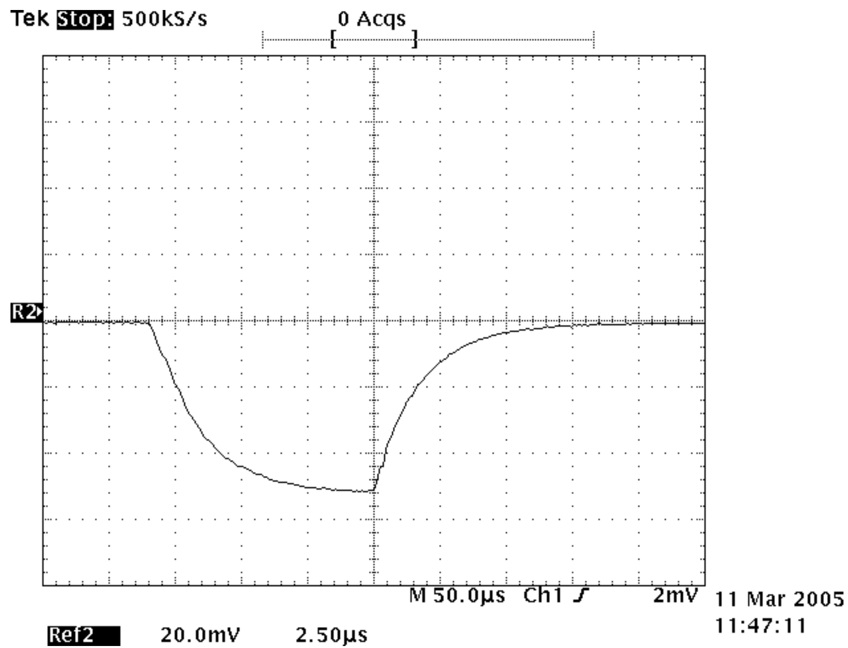


Figure 3.6-13: 200 V DC Bus - Current 50A/Div @ 20 mV/Div
10 kOhm Scope Termination

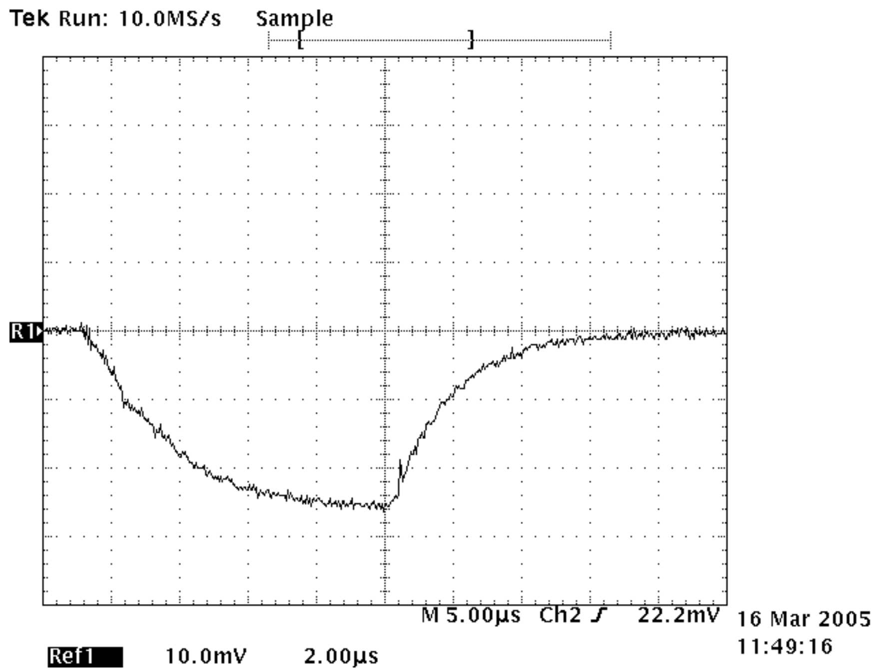


Figure 3.6-14: 200 V DC Bus - Current 50A/Div @ 10 mV/Div = 50 A/Div
50 Ohm Scope Probe Impedance

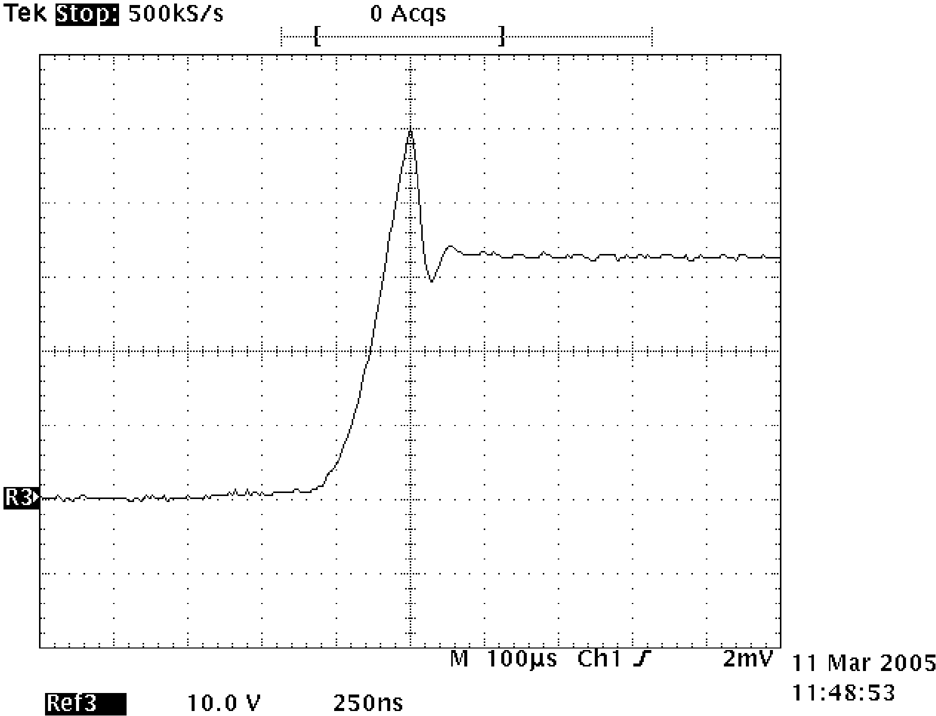


Figure 3.6-15: 300 V DC Bus - Voltage 10X Probe 10V/Div = 100V/Div
10kOhm Scope Impedance

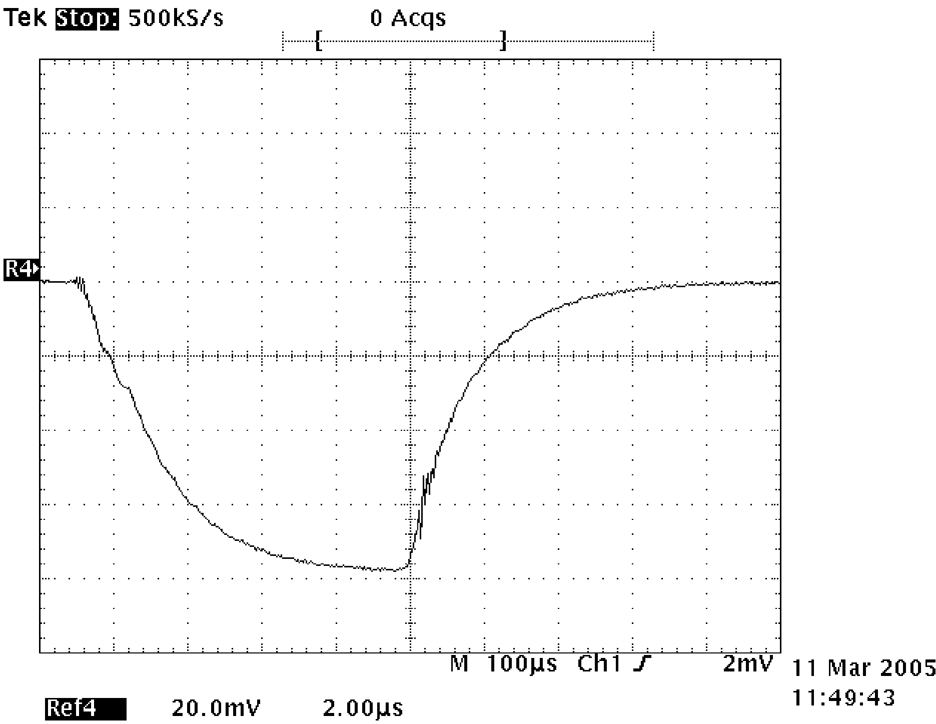


Figure 3.6-16: 300 V DC Bus - Current 50A/Div @ 20 mV/Div
10kOhm Scope Impedance

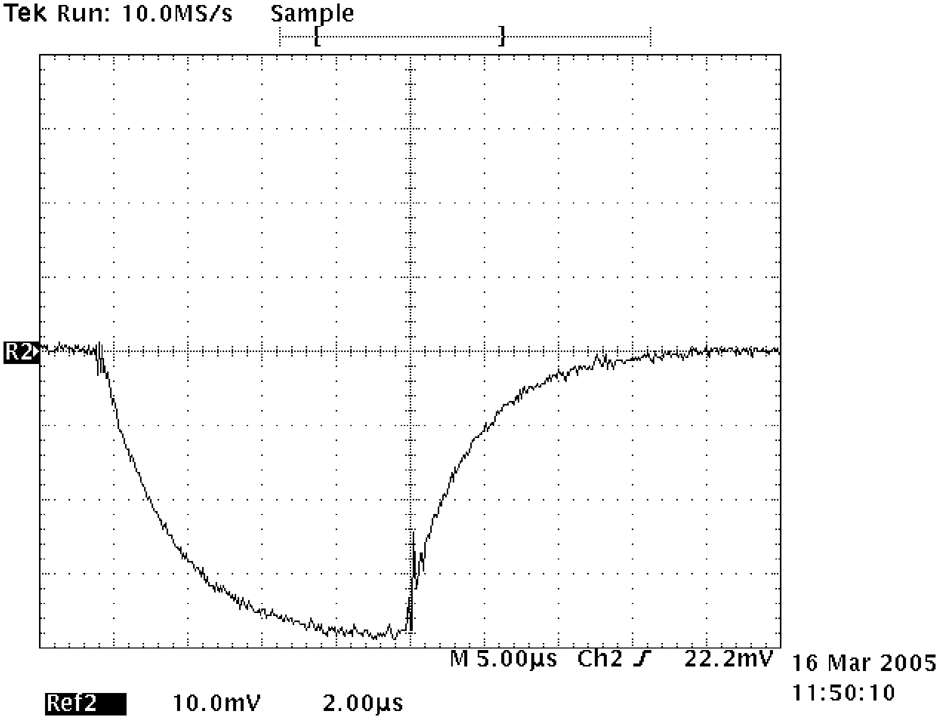
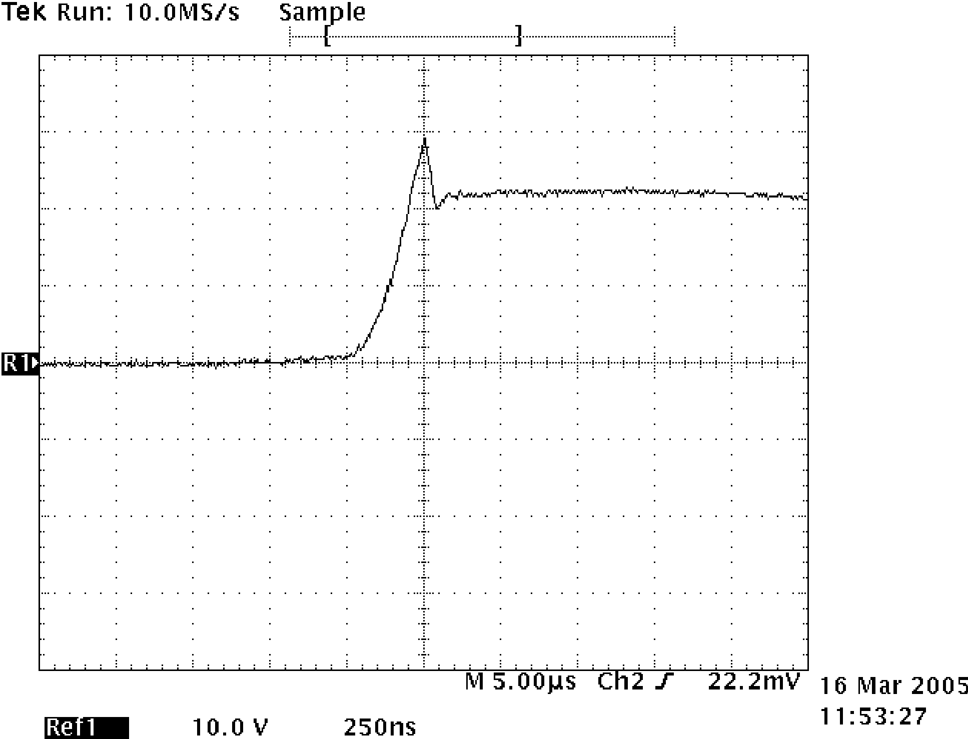


Figure 3.6-17: 300 V DC Bus - Current 50A/Div @ 10 mV/Div = 50 A/Div
50 Ohm Scope Impedance

Figure 3.6-18: 22 µF Capacitor Across Bus Test



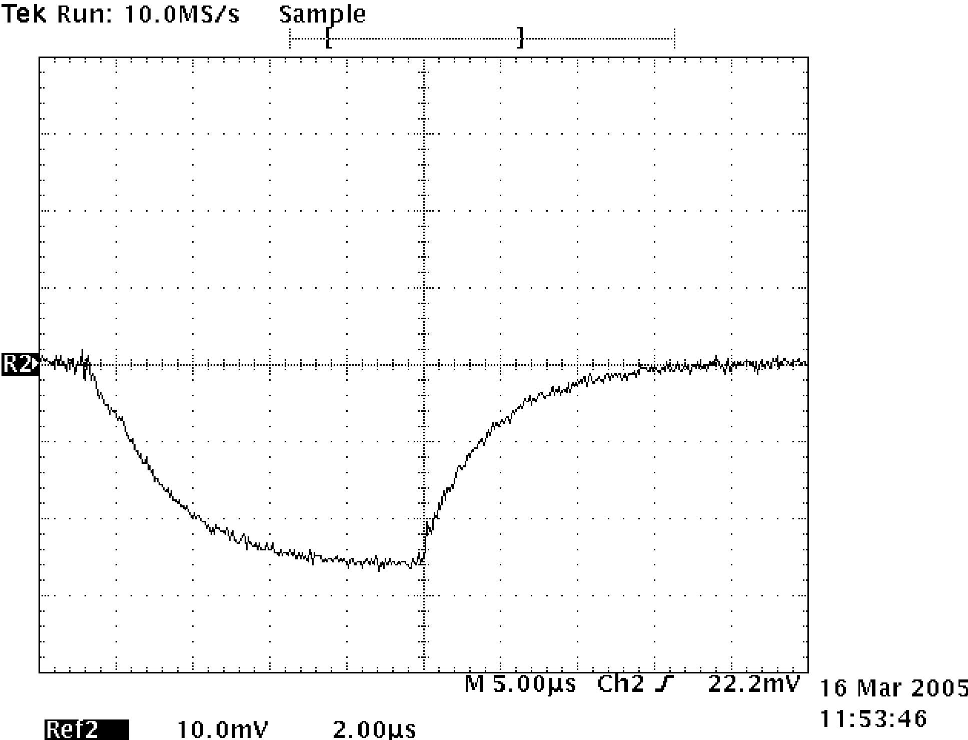
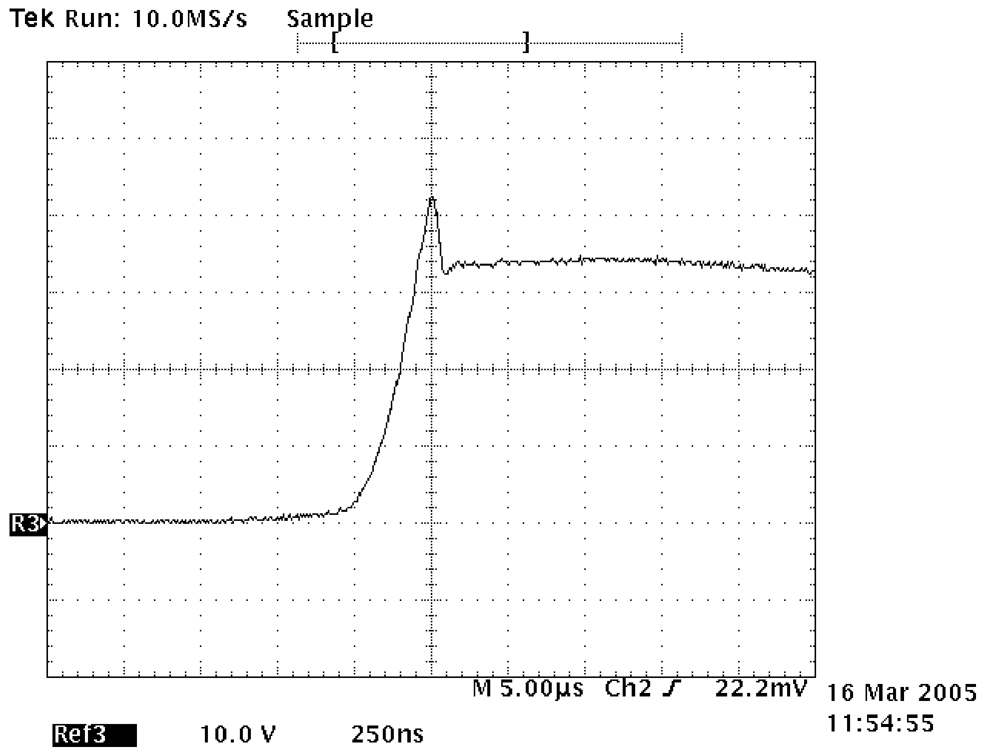


Figure 3.6-19: 200 V DC Bus 22 µF Capacitor Across Bus - Voltage 10X Probe 10V/Div = 100V/Div
Current 50A/Div @ 10 mV/Div = 50 A/Div
50 Ohm Scope Impedance



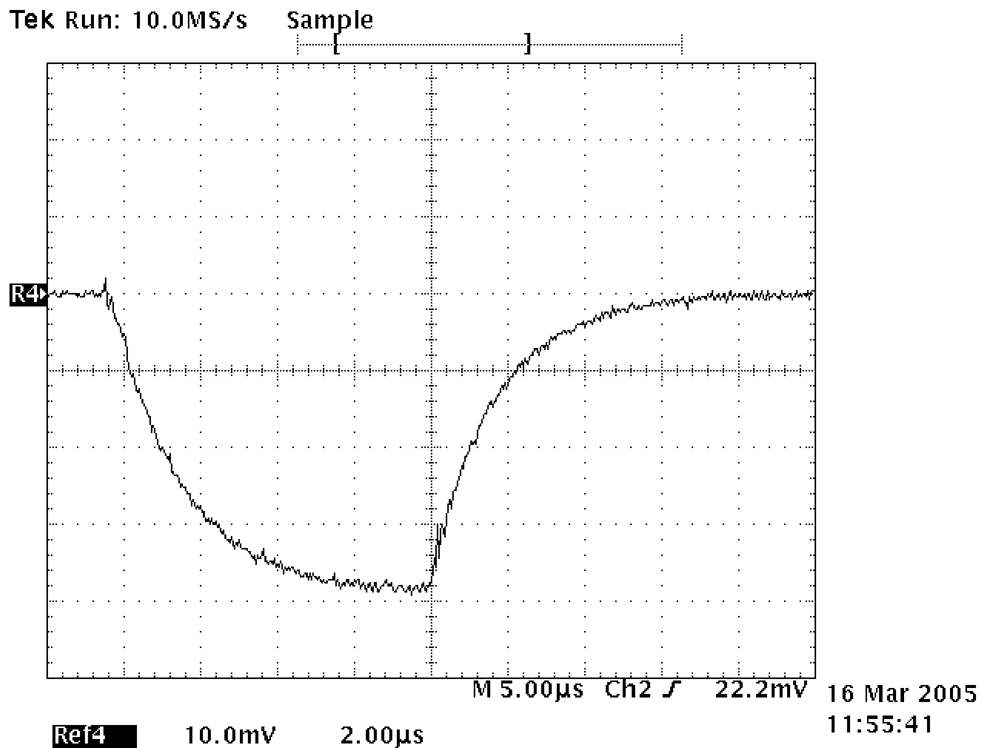


Figure 3.6-20: 300 V DC Bus - 22 µF Capacitor Across Bus - Voltage 10X Probe 10V/Div = 100V/Div
Current 50A/Div @ 10 mV/Div = 50 A/Div
50 Ohm Scope Impedance

3.7. Hybrid Capacitor

The AIPM module was operated at approximately 8 kW with a DC Bus voltage of 200V and a nominally balanced inductive load (lagging load). The DC Bus voltage ripple is shown in ***Figure 2.7-1***, expanded to a scale of 1V/Div.

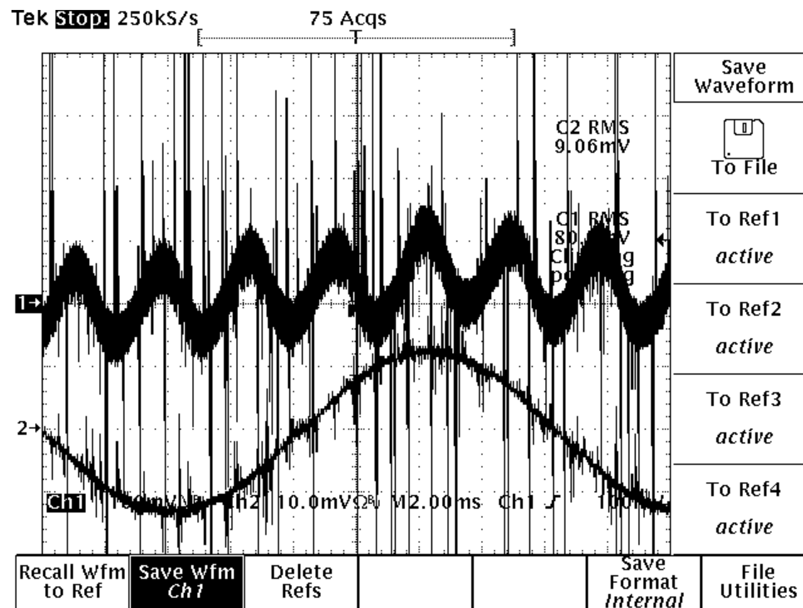


Figure 2.7-1: All Electrolytic Capacitor

The lower trace in the figure shows one of the phase currents at 50 A/Div. For this test the DC Bus Capacitor consisted of two 2200uF Electrolytic Capacitors in parallel. The DC Bus voltage can be seen to have a ripple at six times the fundamental, this is due to imbalances in the power (or equivalent current) being put out to each phase. The fuzz on the voltage waveform is the switching frequency (3 times switching frequency) ripple on the DC Bus.

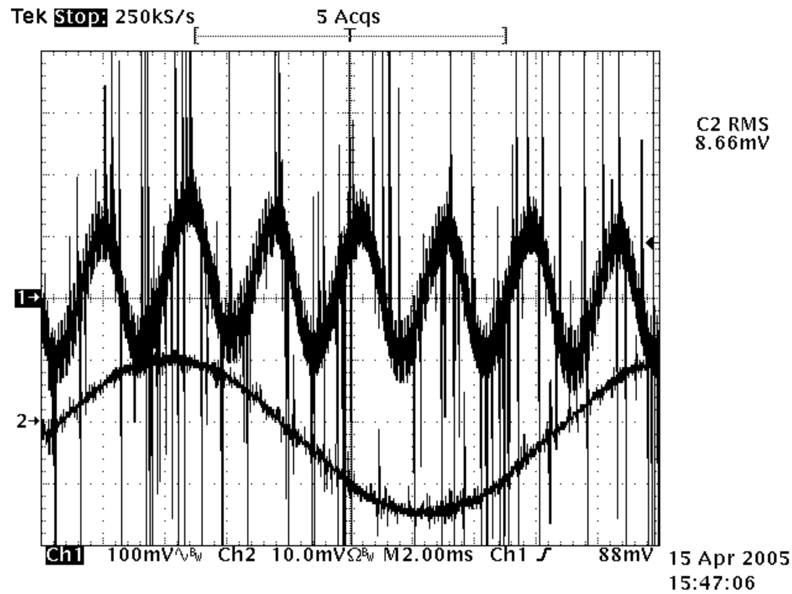


Figure 3.7-2: Hybrid Capacitor, Electrolytic and Film Matched by Volume

Figure 3.7-2 shows the corresponding waveform for the Hybrid Capacitor formed by sharing the AIPM Bus Cap volume equally between Electrolytic and Film Capacitor. The DC Bus capacitor is now formed by the parallel combination of one 2200uF Electrolytic and one 650uF Film capacitor.

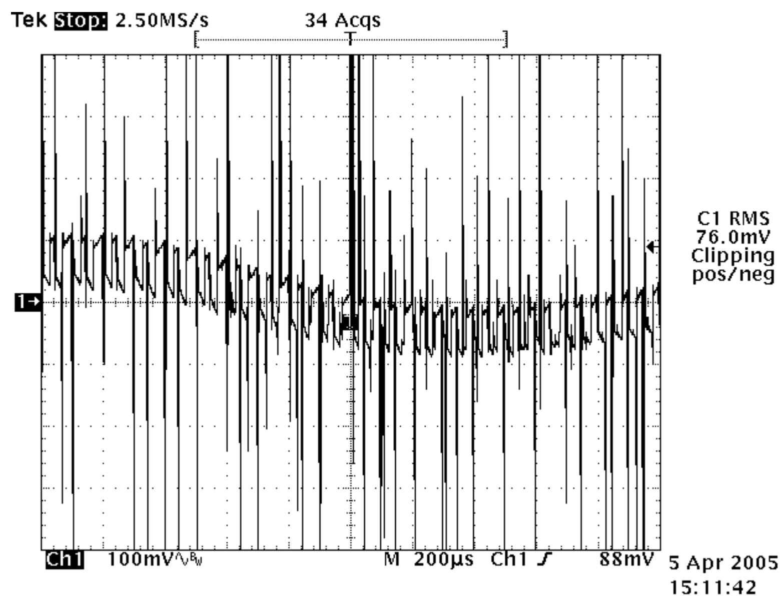


Figure 3.7-3: One Low Frequency Cycle All Electrolytic

Figure 3.7-3 and ***Figure*** 2.7-4 show the same waveforms for the Electrolytic and the Hybrid Capacitors respectively expanded out in time. One can begin to see that the wave-shape at the switching frequency is quite different, square for the electrolytic, and triangular for the hybrid.

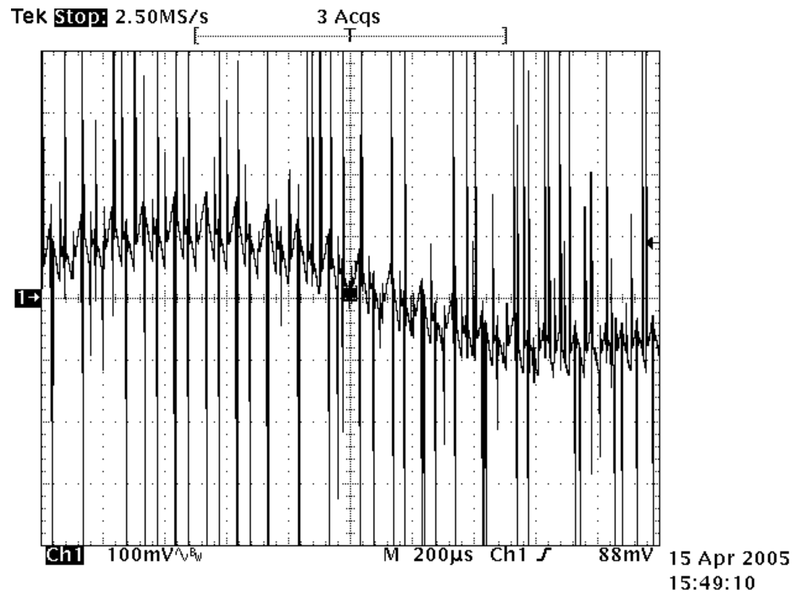


Figure 2.7-4: One Low Frequency Cycle Hybrid Capacitor

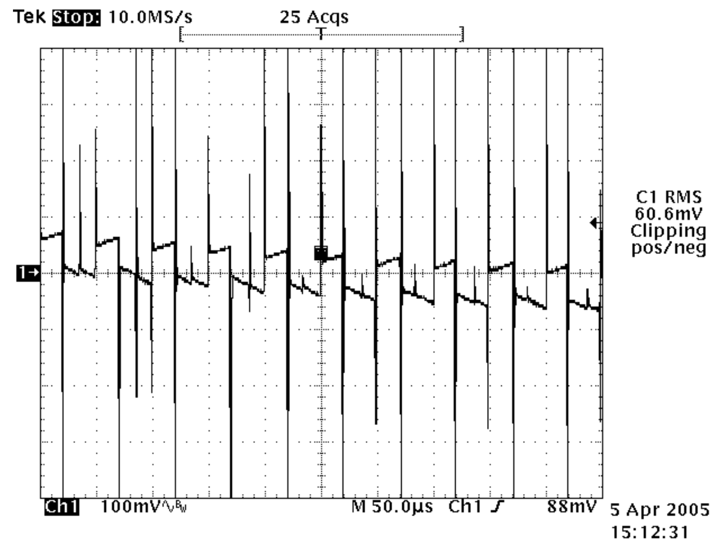


Figure 3.7-5: All Electrolytic Switching Frequency Wave-shape

Figure 3.7-5 and ***Figure 3.7-6*** show the same waveforms expanded out further. It is clear that the resistance of the Electrolytic Capacitor dominates the wave-shape, whereas the comparably smaller steps in the Hybrid Capacitor result indicate correspondingly smaller resistance and therefore loss. The reduced capacitance of course result in more ripple due to charge storage but this should not be regarded as a negative. There is no loss involved with this ripple. In fact we often design for 1% or less ripple to simplify the task of the controller. Utilizing modern control techniques and recent mixed signal controllers we can instead permit high ripple DC Bus and reject the disturbance using the controller.

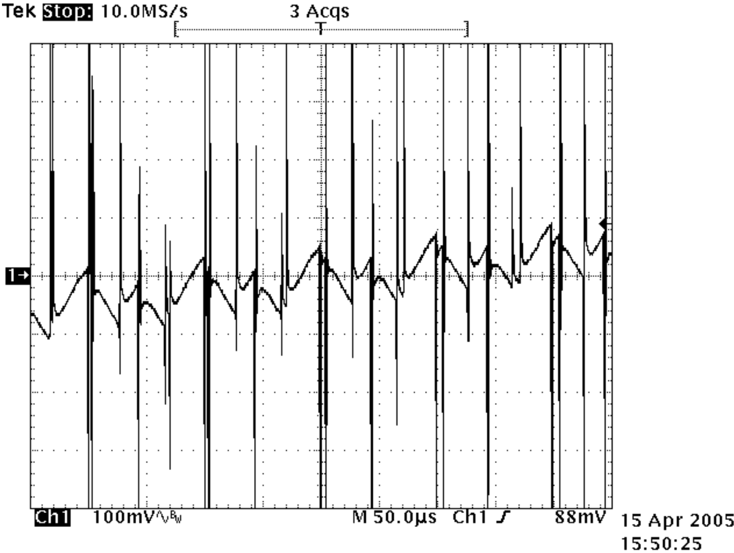


Figure 3.7-6: Hybrid Capacitor Switching Frequency Waveshape

4. Heat Sink

4.1. Objective

The objective of this portion of the report is to eliminate the need for liquid cooling and to demonstrate the performance using our AIPM module, with a goal of maintaining a peak power output of at least 35 to 40 kW and without increasing the module's footprint. An "augmented surface bonded fin heat-sink" replaced the AIPM liquid-cooled heat sink to accomplish the objective. The "augmented surface bonded fin heat-sink" fin dimensions were optimized for heat transfer in the AIPM application. Thermal modeling supported the optimum fin dimensions and spacing selection. Based on the optimized geometry and commercially viable heat sinks, a COTS heat-sink was identified, purchased, integrated and thermally tested, verifying the predicted performance. This section addressees the results achieved and the data collected during testing. The hardware design, analysis and testing were done at SatCon's new Boston, MA facility instead of the proposed Baltimore, MD facility.

4.2. Finned heat sink research, analysis and design

Our present high power density, low-cost inverters use liquid cooling to heat-sink the power devices. ***Figures 1.0-1*** and ***2.1-1*** show SatCon's Automotive Integrated Power Module (AIPM), developed under a DOE contract, and the unique, low cost, compression mounted power devices on a cooling manifold made from internally finned, rectangular cross-section copper tubes *(**Figure 4.2-1**)*.

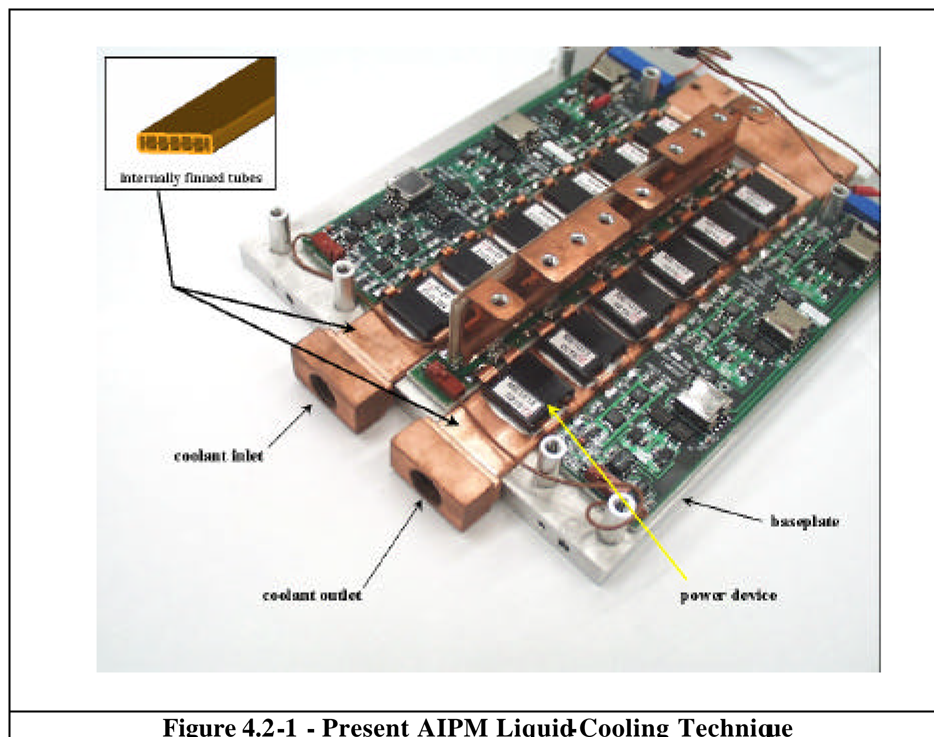


Figure 4.2-1 - Present AIPM Liquid-Cooling Technique

Although liquid cooling allows for very high and localized power densities, there are some drawbacks and limitations. Liquid cooled inverters must be connected to a pump and another heat exchanger in order to dump the heat removed to the atmosphere. Some applications may

have ready sources of extra available coolant which can be piped to the inverters, but that is not always the case. In some instances, a cooling loop may already be in place, but the coolant is at too high a temperature for electronics cooling, as is the case with automotive ethylene-glycol/water cooling loops. Typically, this means that the integrator must provide a radiator, pump and plumbing to complete the cooling circuit. All these items have volume and cost impacts that are typically not considered in inverter power density and cost calculations.

The Anticipated Benefits of Air-Cooled Power Devices are as follows:

Reduced weight: When the weight of the removed radiator, pump, coolant, and plumbing are considered, the proposed air-cooled inverter system will weigh less than a system using our liquid-cooled inverter. The savings should be in the range of 10% to 20% of the combined weight of the inverter, pump, radiator, and plumbing. The weight saving does not scale linearly. The greatest gains would be at the lower power levels (~30 to 50 kW).

Reduced system volume: When the volume of radiator, pump, coolant, and plumbing are considered, the proposed air-cooled inverter will take up less volume than the liquid-cooled inverter system. The volume savings could be as high as 10% to 20%. Like the weight savings, the volume savings does not scale linearly. The greatest gains would be at the lower power levels (~30 to 50 kW). This is also very dependent on how such a system is packaged. If the radiator is mounted far away and plumbing volume is considered, the volume savings can be large. Likewise, if the air-cooled inverter is located in an area with no airflow, special ducting may be needed to bring fresh air to the inverter with a corresponding impact on weight and volume savings. In most applications, it is reasonable to expect a net volume savings with the air-cooling.

Reduced manufacturing costs: Reducing the number of components lowers manufacturing costs. Customers will not have to source and inventory relatively costly pumps and radiators. Customers also will save on the labor costs of installing a radiator, pump, and plumbing.

Improved reliability: Removing parts, generally improves reliability, as there are fewer components that can fail. The proposed modification trades a fan for a pump, so there is no net reliability gain there. However, radiators and plumbing certainly succumb to environmental effects (corrosion, hose cracking, etc) and increase failure rate. Eliminating these components should therefore result in cost savings for customers through reduced warranty claims.

Reduced use of ethylene glycol in automotive applications: Liquid-cooling of inverters typically involves the use ethylene glycol and water as a coolant. Ethylene glycol is extremely toxic if ingested and old fluid cannot simply be dumped when it is replaced as it poses risks to animals and our water supply. Using liquid-cooled inverters will increase the use of ethylene glycol where as air-cooled inverters will not.

Reduced part cost: Reduced parts cost, is a benefit of the proposed modification, as the need for a pump, radiator and plumbing are eliminated. In some cases, due to ambient conditions, a one-to-one substitution of an air-cooled for a liquid-cooled inverter may not be possible as more silicon may be required, but in general a small part cost savings should be realized. It is important to look at the ripple effect on cost of going to air-cooling (see above).

Although liquid cooling is the usual choice for cooling of the highest power density power electronics, recent advancements in finned heat-sink manufacturing techniques allowed SatCon to reassess conventional design practice. Machined or extruded air-cooled heat sinks have cost, physical and/or fabrication limits which results in unsuitable performance for some high power density electronics. Limitations in the extrusion process severely limit fin height and/or the number of fins per inch. Machining from billet allows these limits to be pushed further, but they are labor and cost intensive. Several heat-sink manufactures are producing bonded fin heat sinks to eliminate these issues.

Bonded fin heat-sinks are made by machining, casting, or extruding shallow notches into an aluminum base plate. These notches are then filled with a small amount of a high strength adhesive and Aluminum sheets are press-fit into each notch. Since the notches are shallow, it is inexpensive to have many notches per inch, thus the fin density can be high. In addition, fins made from inexpensive Aluminum sheet stock can be thinner and taller than in extruded heat sinks. An alternate construction technique eliminates the epoxy by deforming the base plate, after assembly, with a high-pressure press. This process plastically deforms the base, locking the fins in place. Heat sink manufacturers are going a step further by enhancing the fin surfaces through cutting and offsetting them at uniform intervals forming a wavy profile down the length of the fins. These two tactics are “tried and trued” methods of enhancing heat transfer during forced convection – they are simply new to bonded fins. Our power device compression bonding approach allowed us to easily swap in alternatives for our liquid cooled design.

Our present AIPM inverter is designed to operate at 30 kW continuous with occasional 10-second 55 kW bursts at input voltages from 200 VDC upwards. This assumes a 50/50 mixture of ethylene-glycol and water supplied at 2 gpm at 70°C. In comparing air and liquid cooled inverters, one cannot use 70°C as the reference temperature for the air-cooled unit. If the liquid cooled unit gets 70°C coolant, it is physically reasonable to assume that the air-cooled unit will get 59°C air.

From the proposal, ***Figure 4.2-2*** shows a comparison of IGBT die temperatures for air-cooling and liquid cooling across a range of voltages from 200 VDC to 325 VDC. First order air-cooled calculations, done during the proposal assumed a COTS “augmented surface bonded fin” heat sink (Aavid Thermalloy p/n: 024564). This non-optimized heat sink estimate indicated that the AIPM could run at 30 kW down to 210 volts, assuming a 150C max IGBT temperature. With some fin optimization, it was predicted that 35 kW and possibly as high as 40 kW seemed achievable with AIPM inverter at voltages as low as ~200 VDC.

AIPM Power Dissipation Calculation

Tamb	59	C
# of Devices	12	
Rjc	0.456	C/W
Rcs	0.1	C/W
Req	0.04633333	C/W

J. Foshage
9/13/04

Data					Power Dissipation Calculation				AIPM Efficiency			
Max IGBT Die Temperature per Figure 4.3.3 of Proposal					AAVID P/N 24564 THERMAL RESISTANCE @ 150 CFM & 59C Air				AAVID P/N 24564 THERMAL RESISTANCE @ 150 CFM & 59C Air			
					Max		Min		Max		Min	
Battery Volt	T @30kW	T @55kW	Fit 30kW	Fit 55kW	0.067 C/W		0.051 C/W		0.067 C/W		0.051 C/W	
Vdc	C	C	C	C	30 KW	50 KW	30 KW	50 KW	30 KW	50 KW	30 KW	50 KW
200	153	265	154	267	840	1634	976	2135	0.97	0.97	0.97	0.96
225	145	248	143	247	737	1662	858	1935	0.98	0.97	0.97	0.96
250	135	230	133	230	655	1505	762	1753	0.98	0.97	0.97	0.97
275	125	211	126	213	592	1363	689	1587	0.98	0.98	0.98	0.97
280	124	208	125	210	582	1336	677	1555	0.98	0.98	0.98	0.97
300	122	197	121	199	549	1234	639	1437	0.98	0.98	0.98	0.97
325	120	185	119	186	526	1120	612	1305	0.98	0.98	0.98	0.98

Table 3.2-1

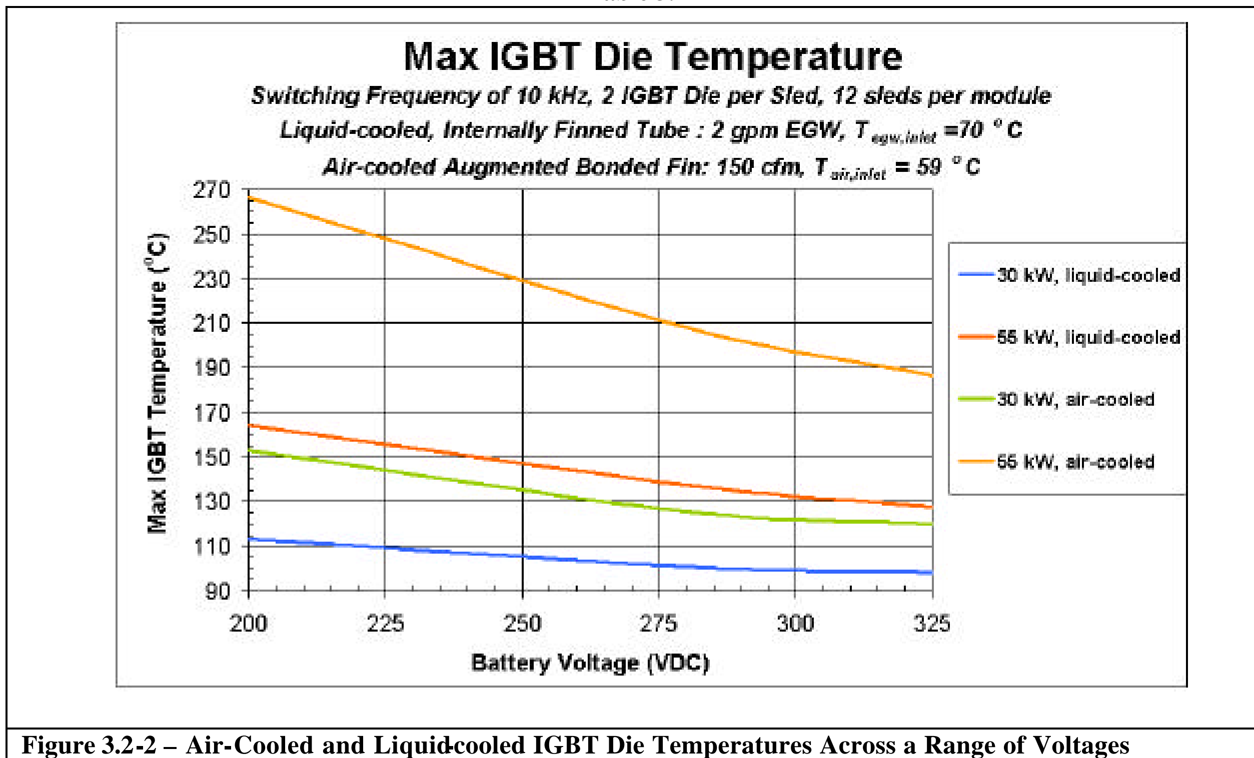
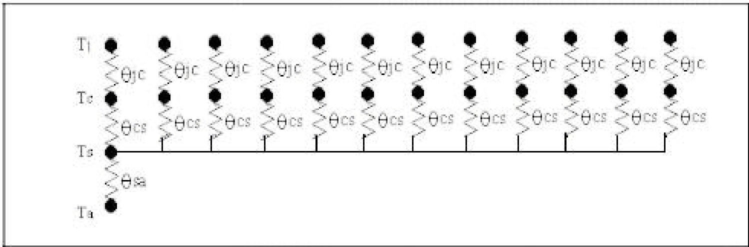


Figure 3.2-2 – Air-Cooled and Liquid-cooled IGBT Die Temperatures Across a Range of Voltages

From this curve, the thermal resistance network (***Figure 3.2-3***) and thermal resistances of the junction to case (R_{jc}), case to sink (R_{cs}) and sink to ambient (R_{sa}) (***Table 3.2-1***), a thermal resistance calculation provided an estimate of assumed power dissipations. These powers, in conjunction with the AIPM heat sink footprint, provided the basis for the heat sink specification (***Table 3.2-2***) and optimization. The temperatures provided in ***Figure 3.3-3*** were based on AAVID Thermalloy's P/N 024564 Augmented, Bonded Fin Heat Sink. A maximum of 0.065 C/W and minimum of 0.051 C/W Heat Sink (HS) thermal resistance are based on the AAVID's data sheets at 150 CFM. The thermal resistance published in the Electrical Specifications of SatCon's Sat Pack IGBT (***Appendix B***), typical industry thermal grease junction resistance.



Where

- Tj = Maximum semiconductor junction temperature
- θ_{jc} = Thermal resistance, junction to case.
- Tc = Case temperature
- θ_{cs} = Thermal resistance, case to heatsink (see Hot Tips)
- Ts = Heatsink temperature
- θ_{sa} = Thermal resistance, heatsink to ambient.
- Ta = Ambient temperature

Figure 4.2-3 –Thermal Model –

Lumped Parameter, Equivalent Circuit

Device Parameters
Power Dissipation: 1000 Watts/Sink or 83W/Device IGBT: Unknown Junction Temperature Limit: 150°C Junction Temperature Margin: Unknown °C Thermal Resistance to Case: IGBT Thermal R: 0.456 °C/W WC per Appendix B Diode Thermal R: 0.850 °C/W Per Appendix B Power Duty Cycle Steady State: 30 KW Transient: 30KW 25 Sec - 55 KW 15Sec Number of Devices: 12 Device Layout: 6 in a row running along 10" Dimension - 2 rows 1"apart Mounting Component to Sink: Thermal Grease Cooling Forced, Impingement Air Flow: 500 CFM Velocity: 7m/s Area: .034 m^2 Environment T ambient: 59°C Altitude: 0-4000 Ft Envelope Height: Minimize Width: 10 in Length: 8 in Corrosion Protection: Yes

Table 4.2-2 – Straw Man Heat Sink Requirement

Sink Size	10"W x 8"L				Fin Heigh (in)			
Parameter	**Symbol**	**Unit**	8	6	4	2	1	0.5
Temperature Drop	ΔT	C	15.2	15.1	15.5	17.4	21.1	27
Thermal Resistance	R_{SINK}	C/W	0.015	0.015	0.016	0.017	0.021	0.027
Reynolds No.	Re_{Dh}		1142	1185	1250	1387	1562	1779
Pressure Drop	ΔP	mm H20	7.6	9.2	12.2	20.5	36.3	66.4
Heat Flow	Q	W	1000	1000	1000	1000	1000	1000
Fin Thickness	t_{fin}	in	0.1016	0.0826	0.0595	0.0319	0.0164	0.0082
Number of Fins	N		61	69	84	114	150	189
Fin Density	FD	N/in	6.1	6.9	8.4	11.4	15	18.9
Air Velocity	V_{fs}	m/s	2.4	2.8	3.6	5.5	8.3	12.1
Entropy Generation	$S_{gen\ dot}$	W/C	0.18	0.181	0.188	0.217	0.268	0.347

Table 4.2-3 – Heat Sink Fin Optimization Summary for Several Fin Heights

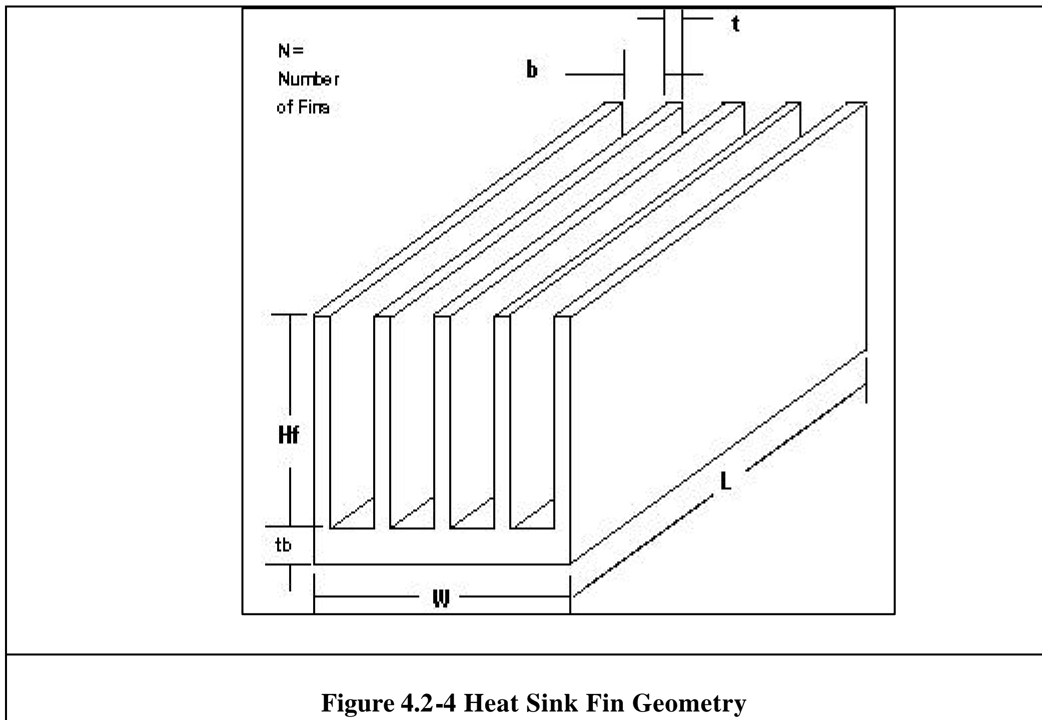


Figure 4.2-4 Heat Sink Fin Geometry

Using a worst-case power dissipation of 1000 Watts, optimized heat sink configurations were derived using an Entropy generation, minimization technique developed by Culham and Muzychka[2]. ***Table 4.2-3*** summarizes the results for a fixed 10" Wide, 8" Long heat sink, for various fin heights with the number of fins, fin thickness and air stream velocity varied, based on the heat sink geometry is defined in ***Figure 4.2-4.***

Three vendors were contacted to identify constraints (***Table 4.2-4***) to heat sink fabrication. In all cases, the optimum designs do not exceed the manufacturability limits. Per one sink manufacturer, the fin spacing depends on the width of the base. On bases up to 8.0" wide, 0.032" thick fins can be spaced 0.125" on center. For bases between 8.0" and 16.0", 0.05" thick fins can be spaced 0.20" center to center

Bonded Fin Specifications and Design Guidelines

Parameter	Specification
Materials	Aluminum, Copper
Minimum Wall Thickness	0.030 inches (0.76 mm)
Maximum Wall Thickness	0.100 inches (2.54 mm)
Maximum Fin Pitch	86
Maximum Aspect Ratio	30:1
Maximum Flowlength	24.0 inches (609.6 mm)
Maximum Height	8.0 inches (203.2 mm)
Length	Not Restricted
Width	Not Restricted
Attachment Methods	Epoxied, Brazed, Soldered

Table 4.2-4: Bonded Fin Design Guidelines

[2] "Optimization of Plate Fin Heat Sinks Using Entropy Generation Minimization", J. Richard Culham and Yuri S. Muzychka, IEEE Transactions on Components and Packaging Technologies, Vol. 24, No.2, June 2001,

In the case of 0.5-inch height, folded fin designs become cost appropriate. Augmentation is available in folded fin designs (***Figure 4.2-5***), but impingement flow is problematic; alternately for axial flow the shape factor requires ducting which increases the envelope and cost. While the folded fin is very attractive from an envelope standpoint, the higher temperature, air velocity and pressure drop across the heat sink are undesirable.

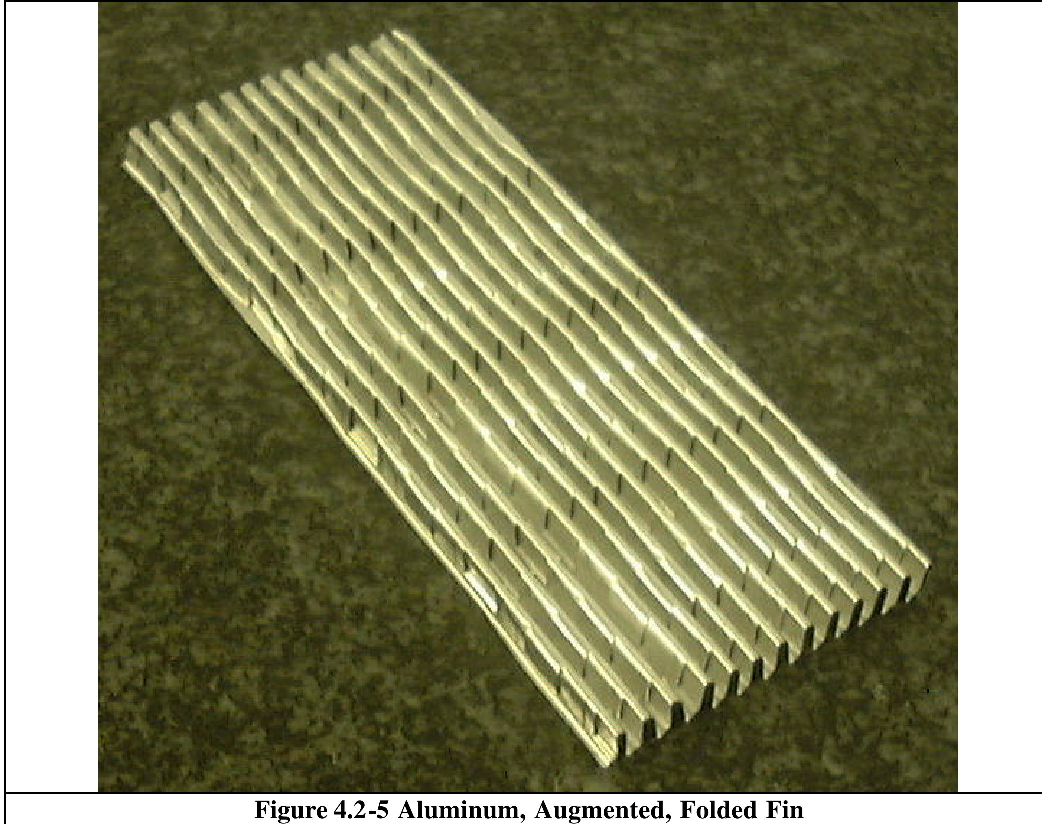
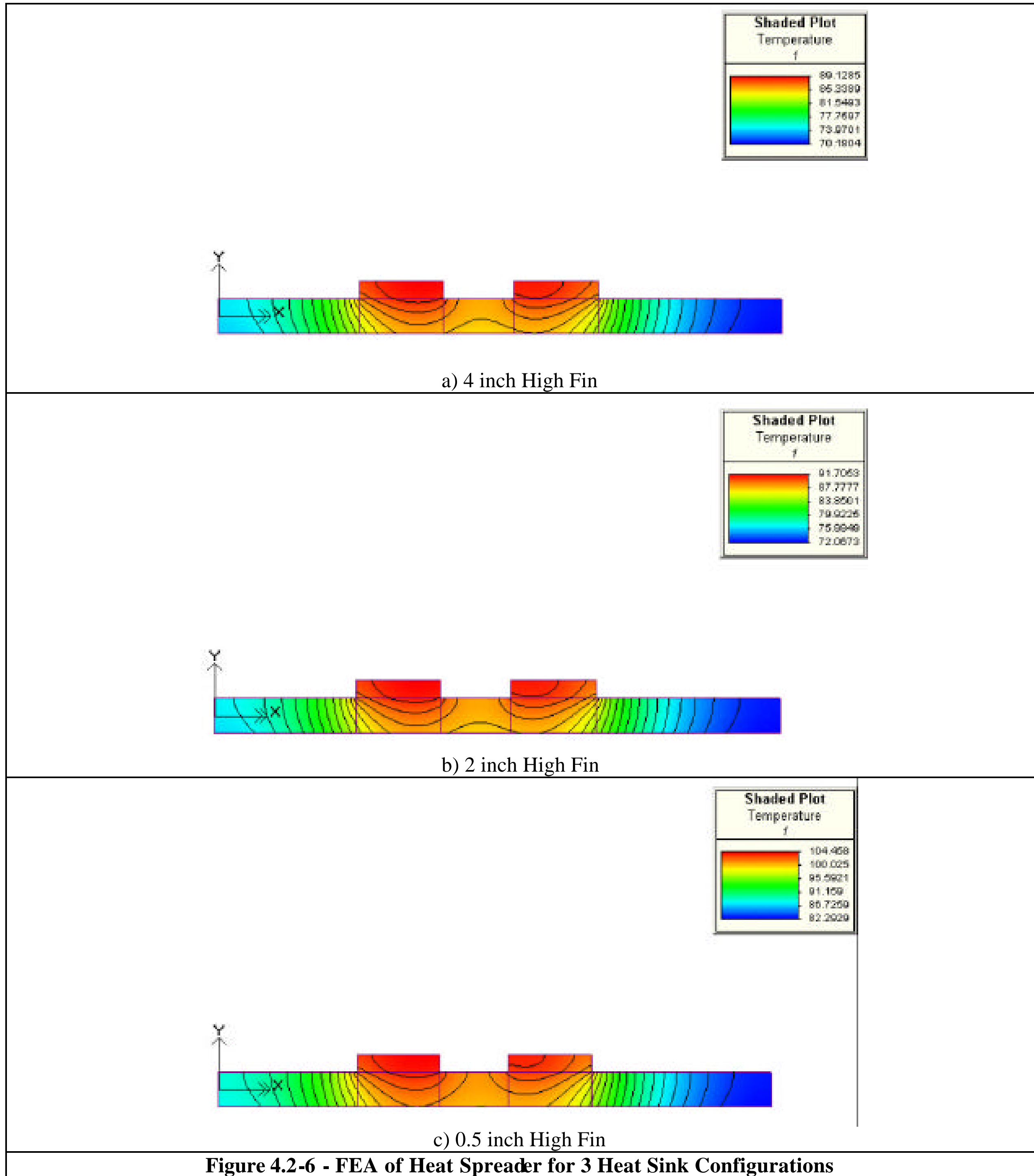


Figure 4.2-5 Aluminum, Augmented, Folded Fin

At the other extreme, 8-inch fin height, extrusions are impractical and bonded fin is the only option, however fin efficiency falls off significantly at long lengths and augmentation is not feasible with extrusions. As the fin height is increased, the Heat Sink ? T and thermal resistance decrease, until a fin height of 4" where they level off. Therefore, fin heights over 4" have such diminishing returns that they are eliminated from consideration. Three designs with fin heights of 0.5, 2 and 4 inches were selected for further study in this application.

A 2D Finite Element model of the heat sink base, assuming uniform heat transfer coefficients scaled from the results in ***Table 4.2-1***, was used to analyze the heat spreading in the 0.25" thick sink base. Results for the 3 cases are show below in ***Figure 4.2-6***. Note that the fins would be at the bottom of the plate extending out in the -y direction and the IGBTs mount on top of the steps. There is only a 2.5 degree temperature difference between the 4 and 2 inch high fin cases and a 13 degree temperature difference between the 2 and ½ inch high fins.



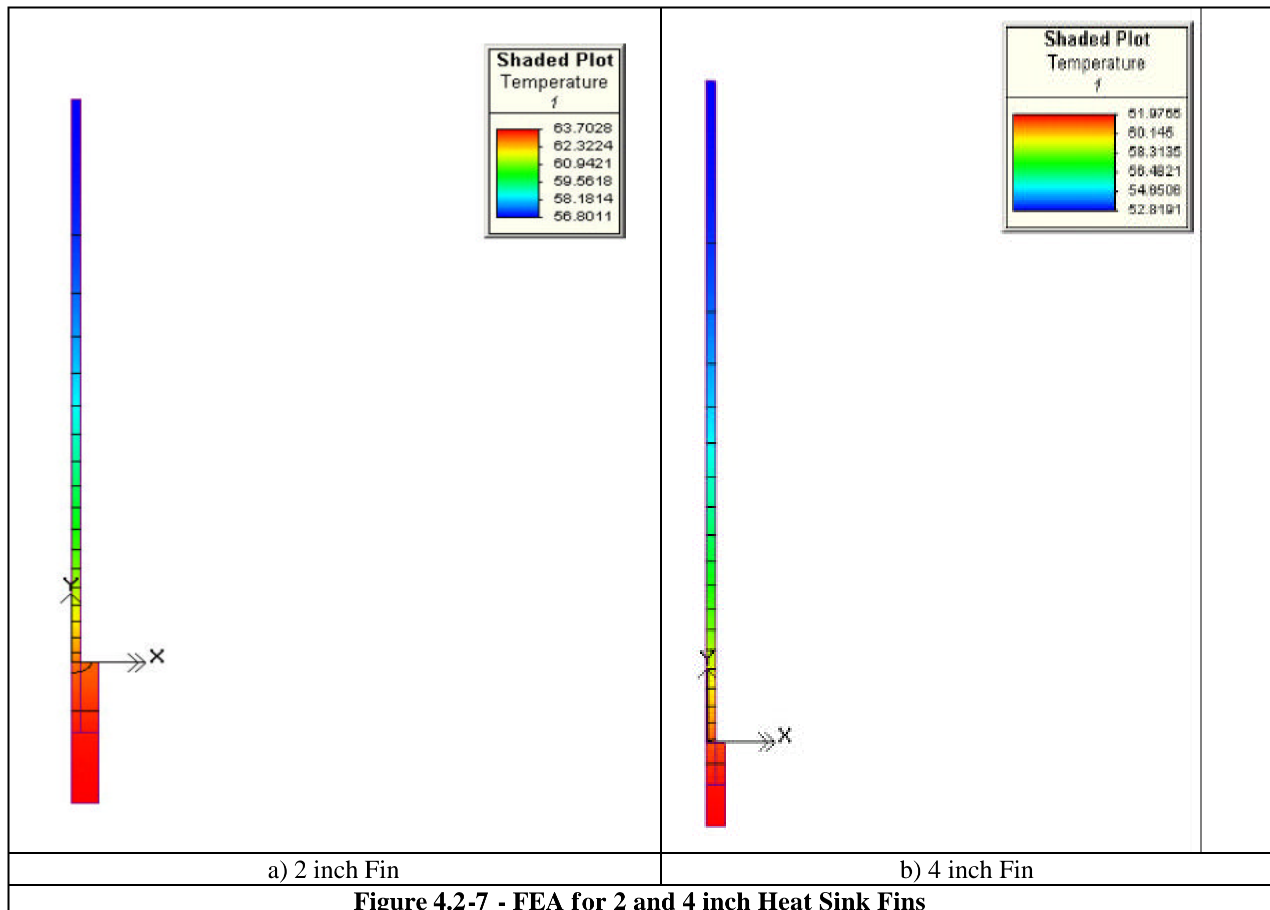
a) 4 inch High Fin

b) 2 inch High Fin

c) 0.5 inch High Fin

Figure 4.2-6 - FEA of Heat Spreader for 3 Heat Sink Configurations

From the optimization results and ***Figure 4.2-6*** it is apparent that the thermal resistance and temperature differential across the heat sink for the 0.5 inch high fin is much more significant than for the other two options. Based on this result, the 0.5-inch fin height case is dropped from further consideration. It is also apparent that heat spreading in the base is limiting the effectiveness of the outboard fins.



a) 2 inch Fin | b) 4 inch Fin

Figure 4.2-7 - FEA for 2 and 4 inch Heat Sink Fins

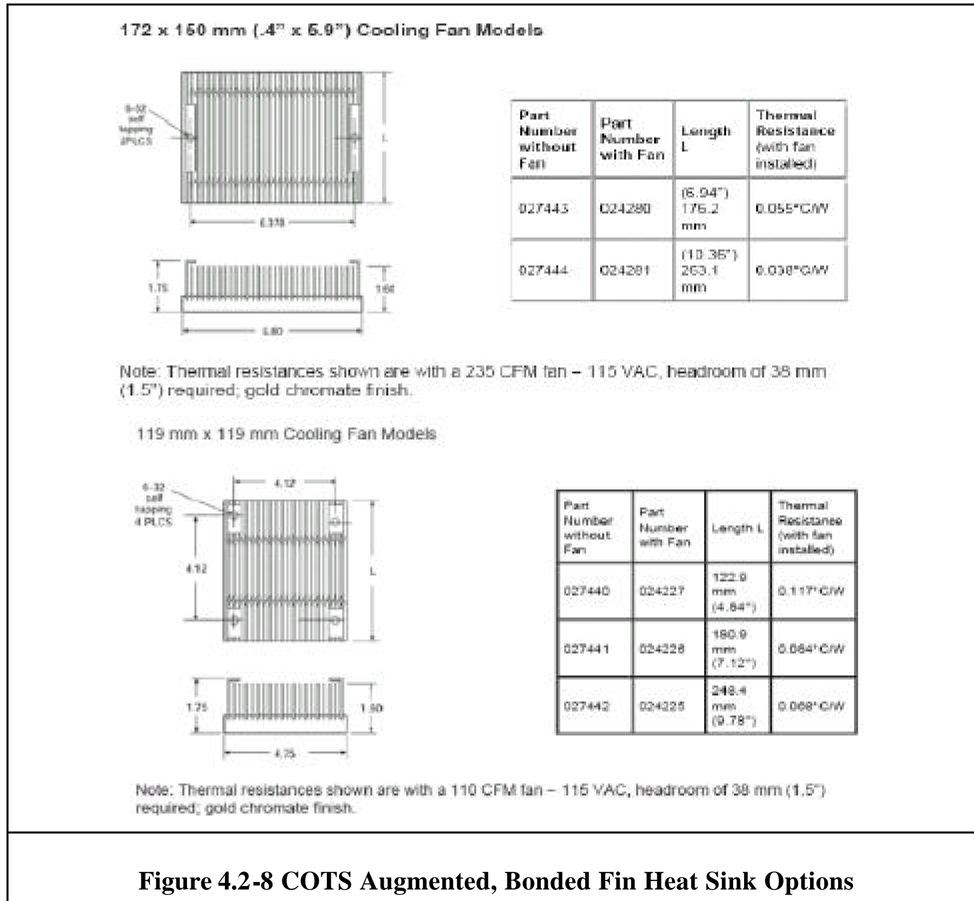
The base is also used for thermal capacitance in the transient case. For a 15 second transient at 50 kW, over and above the 30 kW steady state condition, the added power dissipation is 1135 Watts, worst case. Assuming that all additional heat is stored in the aluminum base, a 23°C heat sink temperature rise will result. This assumes no diffusion limit to the heat transfer in the heat sink and all added energy is stored, a reasonable assumption given the short transient time. Fin height was evaluated next. Finite element analysis of the fin options showed a 2-degree temperature difference between the 2 and 4 inch tall fins, as shown in ***Figure 4.2-7***. Given the small temperature reduction, and the large envelope impact of the 4-inch fin, the 2" tall geometry was selected as the optimal design for the AIPM.

In cases where augmentation is used, a 25% decrease in thermal resistance can be obtained, at the cost of increased pressure drop and Entropy. The purpose of augmentation is to bisect the airflow stream between fins to keep the laminar flow boundary layer from insulating the hot fin from the cooler air and to break up the laminar flow. However, these added transition regions add to the pressure drop across the heat sink. Per the heat sink manufacturers recommendations, the fin offsets should extend to the center of the upstream channel for optimum performance.

The augmentation pitch should be less that 2" because at greater pitch lengths, fully developed laminar flow exists. Between 2 and .04 inches the flow is in transition from turbulent to laminar. Further optimization requires Computational Fluid Dynamics (CFD) analyses of the augmented fin structure, but is not necessary in this case.

Further reduction in the heat sink thermal resistance can be achieved using impingement airflow on the heat sink. In this configuration, cooling fans are located at the mid point of the heat sink with airflow directed towards the heat sink base. This results in the airflow splitting in half and exiting out both sides of the heat sink. Another 25% reduction in thermal resistance can be obtained using this technique. Only one manufacturer was identified that offers commercial off the shelf (COTS) hardware optimized for this cooling system. ***Figure 4.2-8*** summarizes this impingement flow, augmented heat sink cooling system. AAVID's P/N 027444 heat sink has a (HxWxL) 1.6 x 10.35 x 6.8 inch envelope, which is very near the 2 x 10 x 8 inch design envelop, with a 0.038 C/W thermal resistance at 253 CFM and 5.4 fins per inch. For this application the 253 CFM corresponds to a velocity of 5.6 m/s. The fin density can account for the 2x difference in thermal resistance as compared to the optimum 2" high fin case design, which has 11.4 fins per inch.

In an effort to find a commercially viable fin heat sink solution, a COTS solution was sought. The AAVID P/N 027444 and P/N 27441 (***Figure 4.2-8***) augmented, bonded fin heat sinks were identified as the closest COTS heat sink options to the optimal design. ***Table 4.2-5*** compares of heat sink parameters of the COTS options to the optimized solution. Contacts with AAVID found their COTS design could be customized for higher fin density for the AIPM application. AAVID estimated a $5K cost for a CFD optimized design, from which a prototype could be fabricated and tested, at further additional cost.



Part Number without Fan	Part Number with Fan	Length L	Thermal Resistance (with fan installed)
027443	024280	(6.94") 176.2 mm	0.055°C/W
027444	024281	(10.36") 263.1 mm	0.038°C/W

Part Number without Fan	Part Number with Fan	Length L	Thermal Resistance (with fan installed)
027440	024227	122.9 mm (4.84")	0.117°C/W
027441	024228	180.9 mm (7.12")	0.084°C/W
027442	024225	248.4 mm (9.78")	0.068°C/W

Figure 4.2-8 COTS Augmented, Bonded Fin Heat Sink Options

P/N	Quanity	Fin Pitch	W	L	H	Tbase	V	R	Cost	Cost
	Qty	Fin/in	in	in	in	in	CFM	C/W	$ ea	$ ea @ 25
Optimized	1	11.4	10	8	2.25	0.25	200	0.017		
24281	1	4.7	6.8	10	1.6	0.5	235	0.038	166	85
27441 Scale	2	4.2	9.5	7.12	1.6	0.5	110 200	0.042 0.031	125	

Table 4.2-5 COTS Heat Sink Comparison with Optimized Solution

The thermal models were used to compare the junction temperatures for these different options at the 30 and 50 kW power levels and three different voltages (200, 280, and 325 VDC). ***Table 4.2-6*** summarizes the results, which shows an approximate 10°C difference in junction temperature between the optimum design and the pair of AAVID 27441 COTS heat sinks.

	R_{eq} js	0.046	$T_J$ss					
	# Devices	12	30 kW			50 kW		
	V	VDC	200	280	325	200	280	325
	P	Watt	978	677	612	2135	1555	1305
	Rhs	Rtot						
	C/W	C/W	C	C	C	C	C	C
Proposal	0.067	0.113	169	136	128	300	235	206
Proposal	0.051	0.097	154	125	118	266	210	186
AAVID 24281	0.038	0.084	141	116	110	238	190	169
AAVID 27444	0.031	0.077	134	111	106	223	179	159
Optimized	0.017	0.063	121	102	98	194	157	141

4.2-6 Junction Temperature Comparison of Heat Sink Options Proposed Power and Voltages

4.3. Performance Verification

To verify the air-cooled performance of the AIPM, selection a commercial off the shelf (COTS) heat sink demonstrator was made, in order to stay within cost constraints. A pair of AAVID heat sinks (P/N 27441) was identified as the most cost effective solution, with minimal impact in thermal performance as compared to the optimized design. Side-by-side comparisons of the AIPM with liquid cold pate and the pair of COTS Aluminum, augmented surface, bonded fin, heat sinks are shown ***Figure 3.3-1, Figure 3.3-2*** *and* ***Appendix B***. The air-cooled, heat sink assembly is fully interchangeable with the present liquid-cooled cold plate.

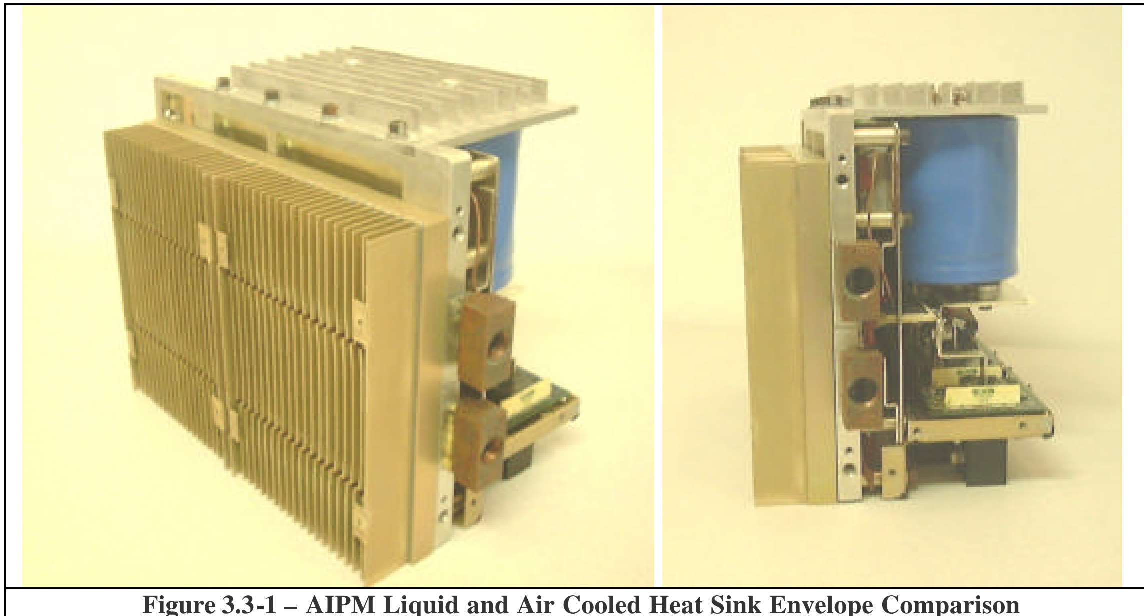


Figure 3.3-1 – AIPM Liquid and Air Cooled Heat Sink Envelope Comparison

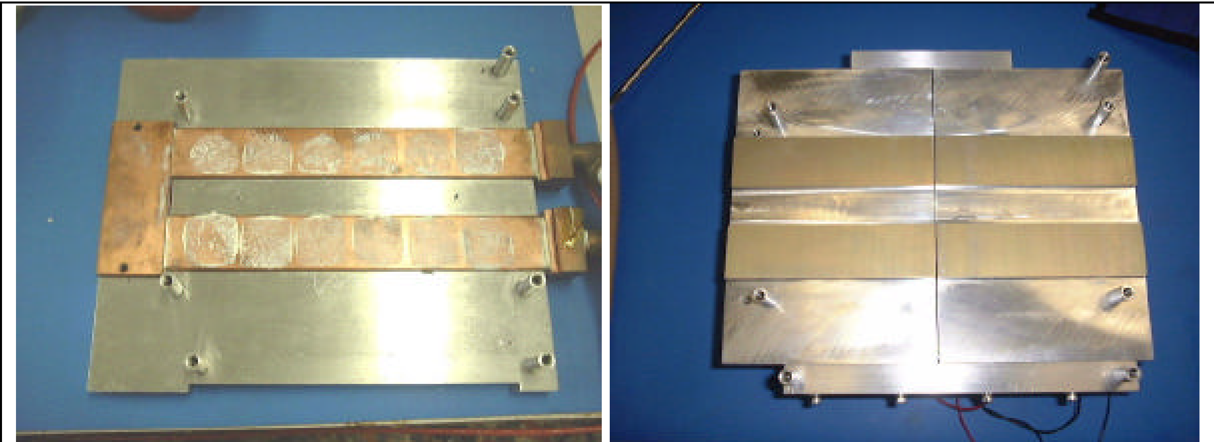


Figure 4.3-2 – AIPM Liquid and Air Cooled IGBT Mounting Interface Comparison

The AIPM inverter was successfully modified and tested (***Figure 4.3-3***) with an air-cooled heat sink using two COTS cooling fans, each rated at 200 CFM and 36 watts at 24V.

Figure 4-3 Integrated AIPM, Heat Sink and Cooling Fans

The AIPM testing was performed to establish:

- The actual power dissipated in the AIPM
- A direct comparison AIPM temperatures for liquid and air cooling
- Measured heat sink thermal resistance for analytical model validation

A baseline test of the AIPM unit with liquid water ethylene is shown in ***Figure 4.3-4***. ***Figure 4.3-5*** shows the test configuration for the liquid and air cooled tests.

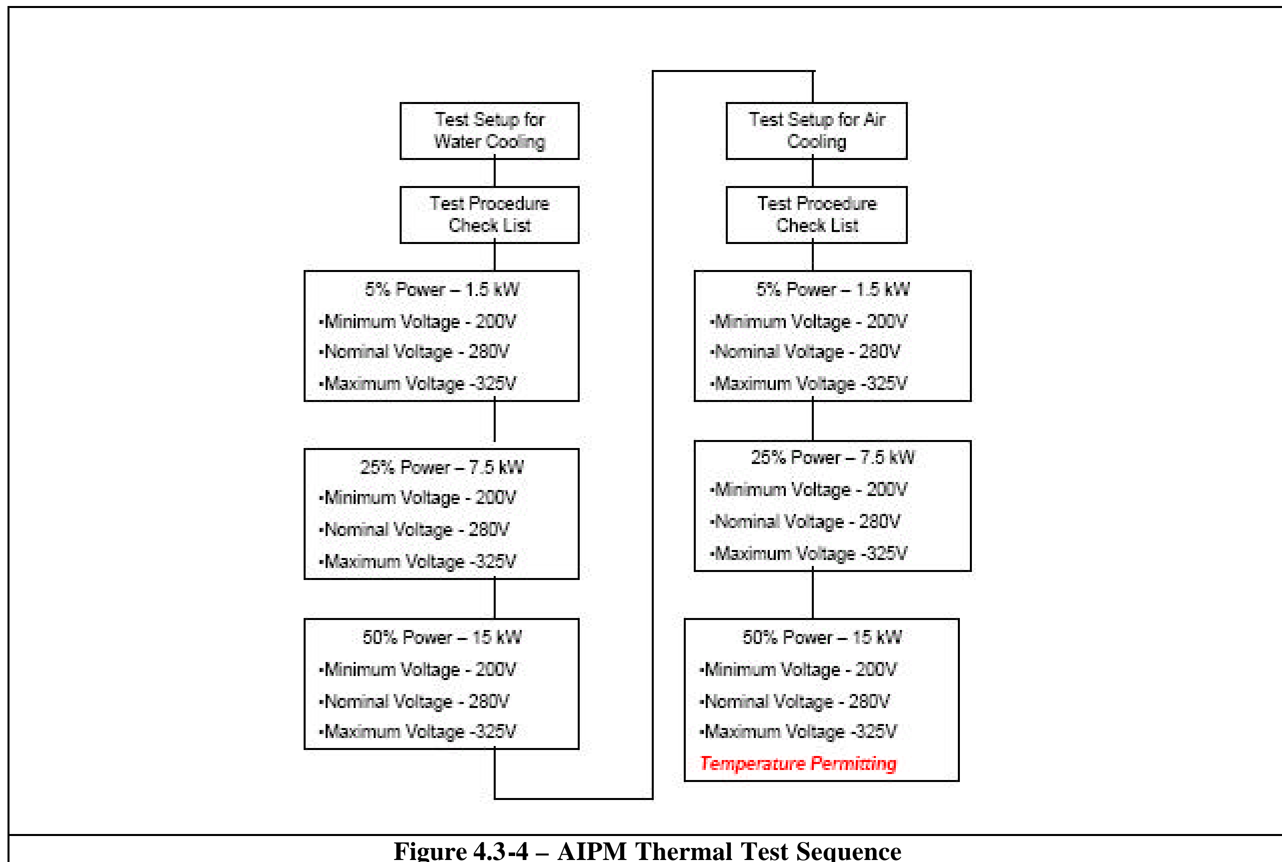


Figure 4.3-4 – AIPM Thermal Test Sequence

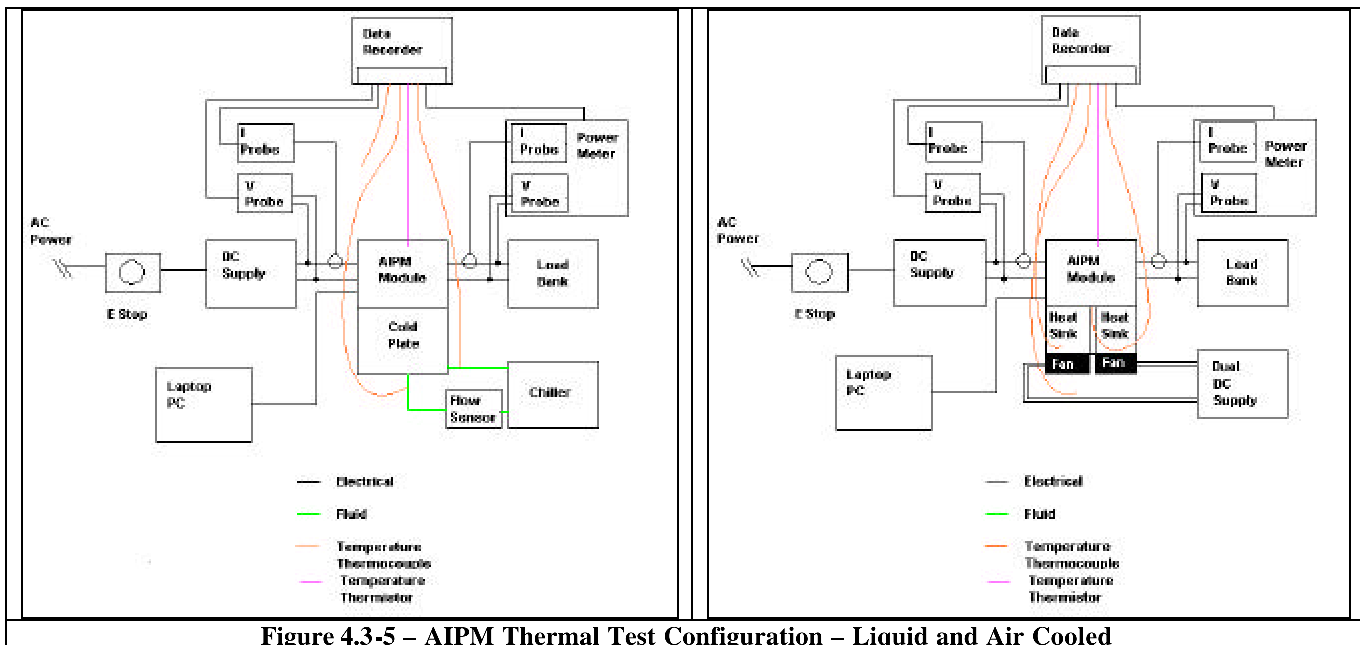


Figure 4.3-5 – AIPM Thermal Test Configuration – Liquid and Air Cooled

Temperature histories of the two test sequences are shown in the ***Figure 4.3-6***. ***Table 4.3-1*** summarizes the test results.

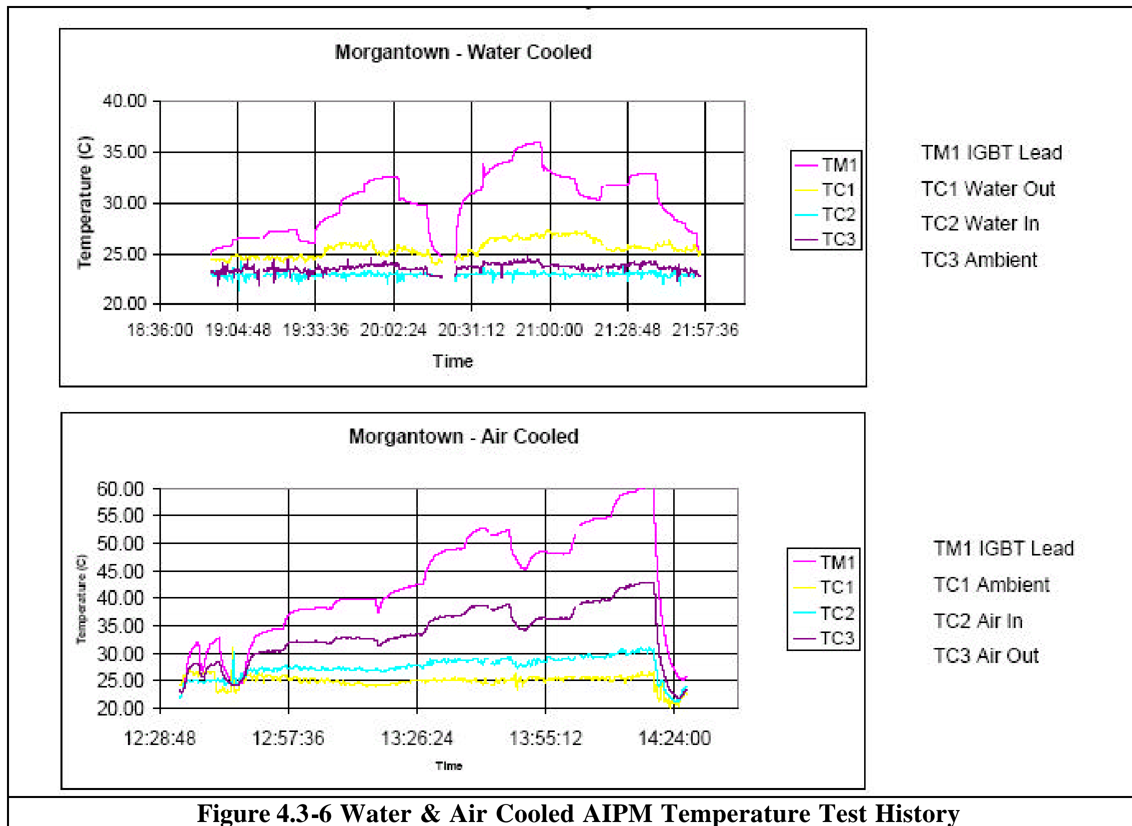


Figure 4.3-6 Water & Air Cooled AIPM Temperature Test History

Parameter	Tamb	Tss	Pin ss	Eff	del T	Ploss	R
Units	C	C	Watt	%	C	Watt	C/W
	23	36	15000	80	13	3000	0.004
Water Temp	23	34	15000	83	11	2550	0.004
To IGBT Lead	23	32	15000	88	9	1800	0.005
	23	33	7500	72	10	2100	0.005
	23	31	7500	75	8	1875	0.004
	23	29	7500	82	6	1350	0.004
						Avg	0.005
	25	60	15000	80	35	3000	0.012
	25	55	15000	83	30	2550	0.012
Air Temp	25	48	15000	89	23	1650	0.014
To IGBT Lead	25	53	7500	72	28	2100	0.013
	25	49	7500	76	24	1800	0.013
	25	42	7500	83	17	1275	0.013
						Avg	0.013
	25	43	15000	80	18	3000	0.006
Air Temp	25	40	15000	83	15	2550	0.006
To Heat Sink	25	36	15000	89	11	1650	0.007
	25	39	7500	72	14	2100	0.007
	25	37	7500	76	12	1800	0.007
	25	33	7500	83	8	1275	0.006
						Avg	0.006

Table 4.3-1 Water & Air Cooled AIPM Test Results at 200 V, 280 V and 325 V

Test data show the power dissipated in the AIPM is higher that predicted in the proposal. The results also show the thermal resistance of the heat sink is better by 4X than predicted. Direct

comparison of the Liquid and Air cooled tests show the air-cooling runs 16 to 26°C hotter than liquid cooling, over the tested voltage range.

4.4. Conclusion

SatCon's objective to implement an Augmented Surface Bonded Fin in our AIPM, as a direct substitute to our internally finned, rectangular cross-section copper tube cold plate, has been completed. This design eliminates the need for a radiator, pump, coolant and associated plumbing, thereby resulting in an overall cost, weight, and space savings at the higher assembly level. An optimized "augmented surface bonded fin heat-sink" was found for the AIPM application. Based on the optimized geometry and commercially viable heat sinks, a COTS heat sink as close to the optimal as possible was identified, purchased, integrated and thermally tested, verifying the predicted performance was conservative.

The *goal* of maintaining a peak power output of at least 35 to 40 kW and without increasing the modules footprint with air-cooling was not reached, due to lower efficiency and corresponding higher than proposed losses in the AIPM. A steady state operating limit of 20 kW at low voltage and 25 kW at high voltage is recommended, based on thermal constraints. Heat sink and cooling fans increased the height of the AIPM by 2.8 inches, resulting in a change in over all height from 5.44 to 8.25 inches. The weight increased from 16 ½ to 19 ½ Lbs, of which 1.8 Lbs are due to the fans. However, the total system weight impact must also consider the elimination of the radiator, pump, fluid and hose weights.

Suggested future development activity, related to air cooled heat sinks, should include:

- Improvement in the heat spreading capacity of the heat sink base (i.e., 2D heat pipes or AlSiC) and or a change in device layout on the heat sink (i.e., checker board pattern instead of the existing 2 rows of IGBT's, dictated by the fluid cooling packaging
- Reduction in the thermal resistance inside the IGBT's between the junctions and the heat sink mounting interface by improving the conduction path from the top as well as the bottom of the IGBT package
- Improving conduction between the chip and the heat sink with materials like GELVET thermal pads or PCM45 Phase Change Materials (PCM)

Investment in tooling needed to make a heat sink with a fin density as suggested by the heat sink optimization.

5. Voltage Sensing

Market volume will be a major factor in reducing manufacturing and purchasing costs for power conversion electronics. In order to meet the 30% cost reduction goals established by DOE, systems must be developed that are modular and therefore capable of being tailored to a variety of power levels and applications. Modular units can then be mass-produced and configured to meet the needs of broader markets. Two of those markets, the Hybrid Electric Vehicle (HEV) and the Distributed Generation (DG) markets would benefit from such a universal approach.
A key modification necessary to adapt HEV-size power conversion devices to DG is an upgrade of the architecture of the voltage sensing system. Standalone HEV-style inverters have no need for (and therefore do not include) galvanic isolation of the voltage sensors. Also, phase measurements can be made from the simple DC link voltage reference. SatCon proposed to develop and demonstrate modifications to HEV-style modules that will make the voltage and phase sensing systems suitable for DG applications. The details and results of the approach are discussed in this portion of the report.

5.1. Objective

The objective for this task was to extend the application of HEV-style inverters to Distributed Generation systems. In DG applications, power-to-control isolation is a critical parameter in meeting UL and NEC requirements for grid operation. In HEV designs, galvanic isolation is normally not required for the voltage sensing system. The HEV application uses a single inverter for each load; therefore, the decrease in power-to-control isolation, caused by paralleled inverters, is not an issue. Likewise, voltage sense signals do not extend beyond the boundaries of the inverter I/O, therefore, galvanic isolation is not necessary to meet conducted emissions requirements. In a distributed generation application, which utilizes a "standardized" inverter module, parallel operation will be required to provide the range of output power levels from 30kW to 500kW.
SatCon's work during this project began by searching for a solution that would satisfy the high temperature, low cost, reliability that the HEV marker demanded, and the isolation that the DG market required. It quickly became apparent that these four requirements could not be simultaneously fulfilled. Therefore SatCon took a different approach to the problem. Rather than finding a 'fit all' solution, SatCon decided to alter the automotive integrated power module (AIPM) to allow for the option of isolated voltage sensing. This allows it to be easily switched from HEV applications to DG applications.
In keeping with the modular theme, this new AIPM can be switched from DG to HEV applications with minimal cost. The AIPM has a single Sensor interface board, responsible for sensing the high power currents and voltages. Originally, this had been done using low-cost high impedance networks. This was suitable for HEV applications, but would not work for DG where galvanic isolation is required. Using the funding provided by this contract, SatCon modified this board to allow it to be populated in two different configurations. One configuration allows for ultra-low cost, automotive temperature, non-isolated sensing. The second configuration is for commercial grade temperature, low cost, isolated sensing. This solution adequately fulfilled SatCon's desires to penetrate both the HEV and the DG markets with a single product solution

Galvanic Isolation: In HEV designs (e.g. the AIPM), the DC bus voltage and phase voltages are measured using non-isolated differential amplifiers, which is the least expensive solution available. This approach yields satisfactory results in medium power, medium-complexity circuits with careful layout, proper grounding technique, adequate filtering and common mode noise suppression. In the proposed modular design, where power, ground and control connections between the paralleled modules are not well defined, interaction between the modules is almost inevitable. With this in mind, galvanic isolation between the power and control circuits is a must. Moreover, in the non-isolated circuit the sensor input impedance becomes a part of the power-to-control isolation impedance. In a modular system with multiple parallel-connected modules this impedance degrades proportionally to the number of parallel-connected modules and may easily fall below the minimum acceptable level.

Zero-Sequence Voltage Measurement: In HEV designs, the negative DC bus is used as a reference point for measuring phase voltages. This method permits the use of simple, non-isolated circuitry for phase voltage measuring and is sufficient for most motor drive applications. However, this simple scheme will not adequately measure zero-sequence voltages, which may occur for example in the case of a non-symmetric load typical of distributed generation applications. In motor drive applications a non-symmetric load represents an abnormal condition and can be detected by measuring phase currents.

During the course of the investigation SatCon looked at various methods for detecting zero phase voltages. The immediate method was to create a neutral by using a balanced wye resistive network on the sensor interface board. This would allow the voltages to all be referenced to a balanced neutral, and the zero phase sequence could be directly detected. However, in order to accomplish this successfully, the resistive network must be extremely precise, and repeatable from unit to unit. Very high quality components must come into use, which raises the cost of design, making it unacceptable for integration onto the sensor interface board.

If, in a distributed generation system two DC sources are floating from one another, a problem can occur from the zero phase voltages that would go undetected without an artificial neutral referenced measurement. However, in most distributed generation scenarios, the DC sources are usually referenced to a common earth ground. This earth ground effectively ties the DC sources together enough such that the impedances of the inverter units prevent large zero sequence effects.

The solution that SatCon used to address this problem was to use a dedicated net on the sensor interface board for the negative reference voltage sensing circuitry. This net is connected via a tab on the PCB. It is tied to the DC negative bus for HEV and most distributed generation applications. If zero sequences are identified as a concern, this net can be tied to an artificial neutral created by a balanced wye network exterior to the board. This design allows SatCon to keep the cost of the board down for HEV applications, while expanding the functionality to distributed generation.

5.2. Galvanic Isolation Design:

Galvanic isolation was achieved by using the ISO122 in addition to a custom low power surface mount Transformer. The Sensor Interface Board was carefully modified to allow for isolated and non-isolated voltage sensing using the same signal path. Very simply, the ISO122 is inserted into this signal path and the isolation transformers are installed when isolated voltage

sensing is required. No software or other hardware changes are necessary, as the option is functionally transparent. This approach allowed SatCon to save costs by manufacturing the same board, and populating it differently depending on the task. This effectively isolated the High power DC and AC electronics from the low power control electronics when installed at a low cost. ***Figure 5.2-1*** and ***Figure 5.2-2*** show the original sensor interface board, a non-isolated assembly of the new sensor interface board, and finally an isolated assembly of the new sensor interface board.

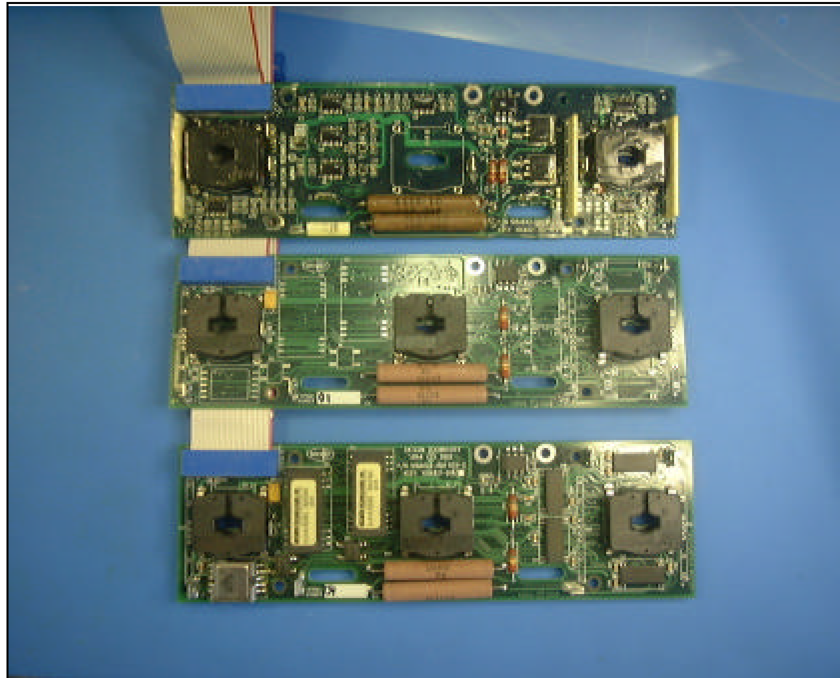


Figure 5.2-1: Top Side of Sensor Interface Board (Original on Top, New Non-isolated in middle, and new isolated on bottom)

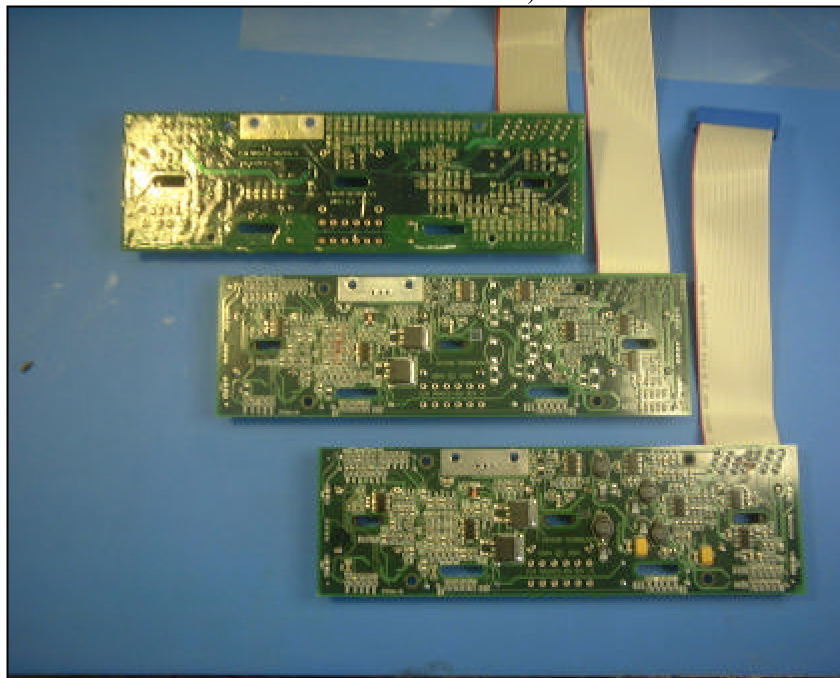


Figure 5.2-2: Bottom Side of Sensor Interface Board
(Original on Top, New Non-isolated in middle, and new isolated on bottom)

5.3. Galvanic Isolation Methods:

The selection of the isolation method is the key to achieving the necessary performance at low cost. There were several options available for implementing the galvanically isolated voltage sense circuit. By comparison, SatCon chose to implement the capacitively coupled amplifiers (ISO122) for the following reasons:

Optically isolated linear amplifiers: Optically isolated linear amplifiers exhibit good isolation characteristics with isolation voltages exceeding 6000V and dV/dt reaching 15kV/us. Until recently, there were drawbacks associated with optically isolated amplifiers, namely, limited temperature range (-40°C to +70°C or -40°C to +85°C) and high cost. Recently, low-cost alternatives with an operating temperature of 100°C have been developed for motor drive applications. These components have been developed for current sensing in low and moderate power commercial motor drives. However, they require careful circuit design and layout, when used in higher power applications. These isolators were not selected because of their high random failure rate. Optocouplers in general have FIT ratings in the thousands.

Modulation-demodulation type amplifiers: This type of isolation amplifier utilizes high-frequency modulation technique and transformer isolation. They provide good isolation characteristics and high accuracy, but their cost was prohibitively high and availability was poor.

Hall-effect sensors: Hall effect current sensors have found a widespread use in motor drives and other power conversion applications due to their relatively low cost, wide bandwidth (including DC), and inherent galvanic isolation. The recent introduction of the low-cost, high-temperature hall-effect current sensors for automotive applications from LEM, make hall-effect sensors an unsurpassed solution for current measurement in medium power inverters. However, hall-effect voltage sensors have not been used in high-frequency power converters, mainly because of their relatively high power consumption (especially at high voltage), large size, and limited temperature range. They are also physically bulky and prohibitively high cost.

Capacitively coupled amplifiers: This type of amplifier uses a voltage-to-frequency or PWM conversion technique and transmits the signal though a very small (2-3pF) capacitor. These devices have moderate isolation voltages, usually 1500V-3000V, but perfect dV/dt characteristics reaching 50kV/us. The cost is somewhat higher, compared to opto-amplifiers but is within the acceptable range for medium power inverters. The ISO122 was selected due to its availability, low-cost, and ease of implementation.

Isolated Power: All of the isolation schemes, with the exception of hall-effect sensors, require isolated power for operation. The need of a separate isolated power supply for each isolated channel increases significantly the overall cost of the isolated voltage sense circuit. The power of each power supply is very small – less than 0.5W, but the isolation and dV/dt requirements are as high as the measuring circuit itself. Some manufacturers offer isolated power supplies for their isolation amplifiers, but the combined cost may be prohibitive. SatCon has developed a high-frequency isolated power supply for use in the AIPM inverter gate drive circuit. This power supply has the necessary isolation and dV/dt characteristics and has been be used in the isolated voltage sense circuit.

5.4. Performance Verification

Better handling of asymmetric loads: The new voltage sense circuit will provide accurate measurement of asymmetric loads, nonlinear loads, DC offset etc. This feature is essential to extending the applications range of the HEV inverters, including the distributed power generation market. It will also facilitate better current sharing between the parallel modules and will make the inverter scaleable to higher power levels.

Improved noise immunity: Better noise immunity of the isolated voltage sense circuit improves the operating reliability of the power module and enables its operation in higher power, high voltage systems.

Better power-to-control isolation: The isolated voltage sense circuit provides guaranteed isolation between the power and control circuits. The isolation level complies with the NEC and UL requirements for grid-connected systems, which facilitates further market expansion for the proposed system. High isolation impedance is maintained regardless of the number of parallel-connected modules. This additionally supports the scalability of the modular system.

5.5. Testing Results

The revised version of the sensor interface board was tested using SatCon's laboratory supplies. The following procedure was used to verify the functionality of this board.

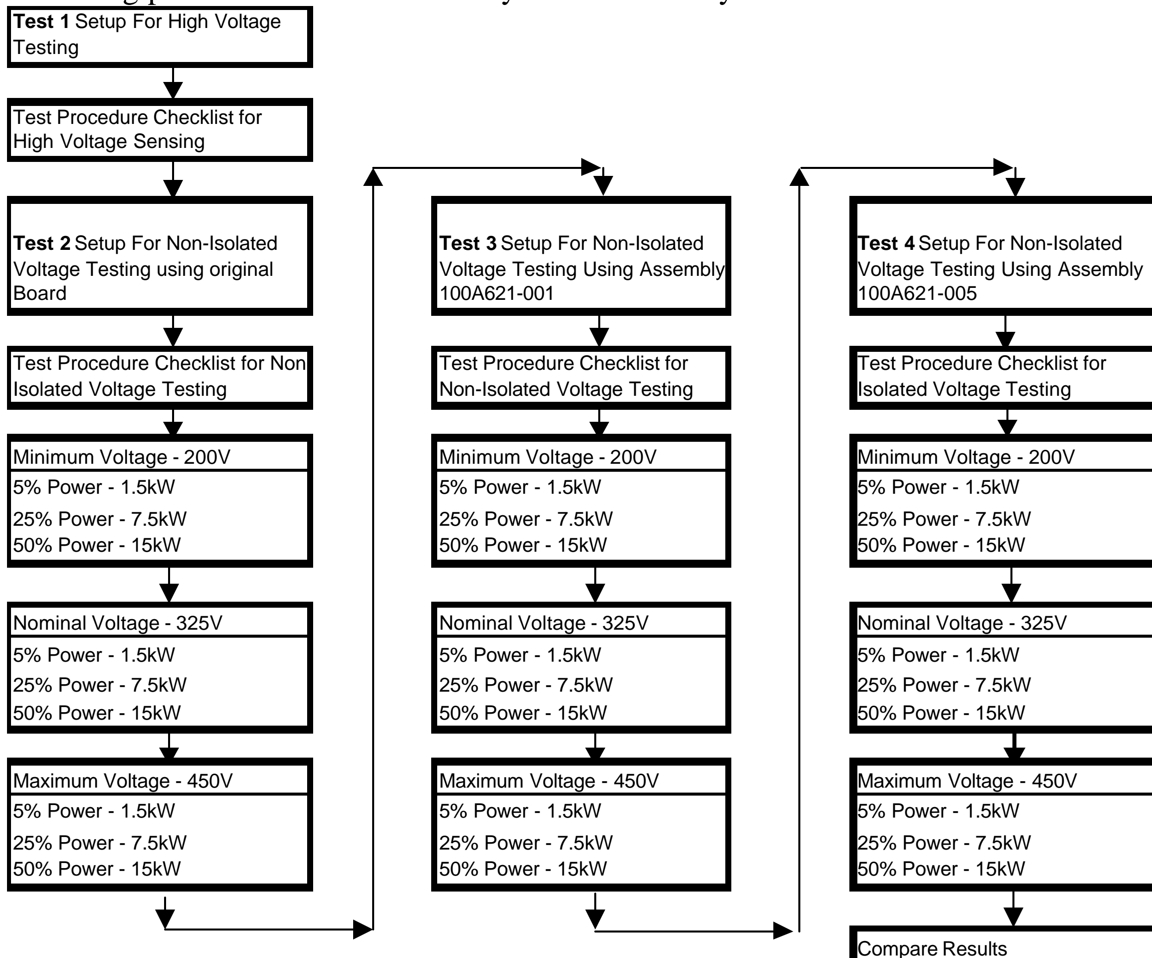


Figure 5.5-1: AIPM Isolation Test Sequence

For the first test, a high potential power supply (1.5 kV) is applied across the isolation barrier. The impedance is recorded while the voltage is incremented to the target 1.5kV and then as it is removed. The new isolated sensor board passed this test. A picture of the test is shown below:

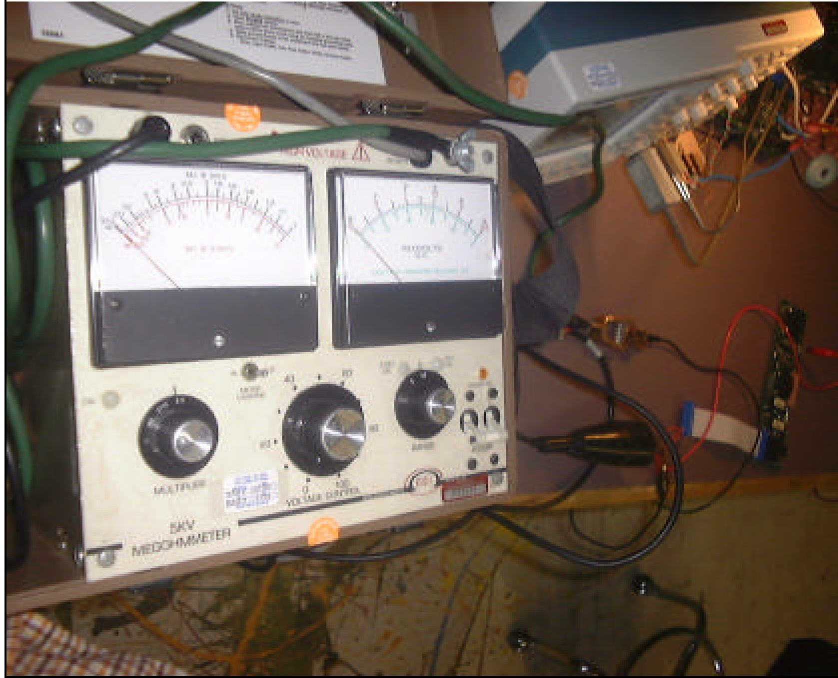


Figure 5.5-2: High Potential Test

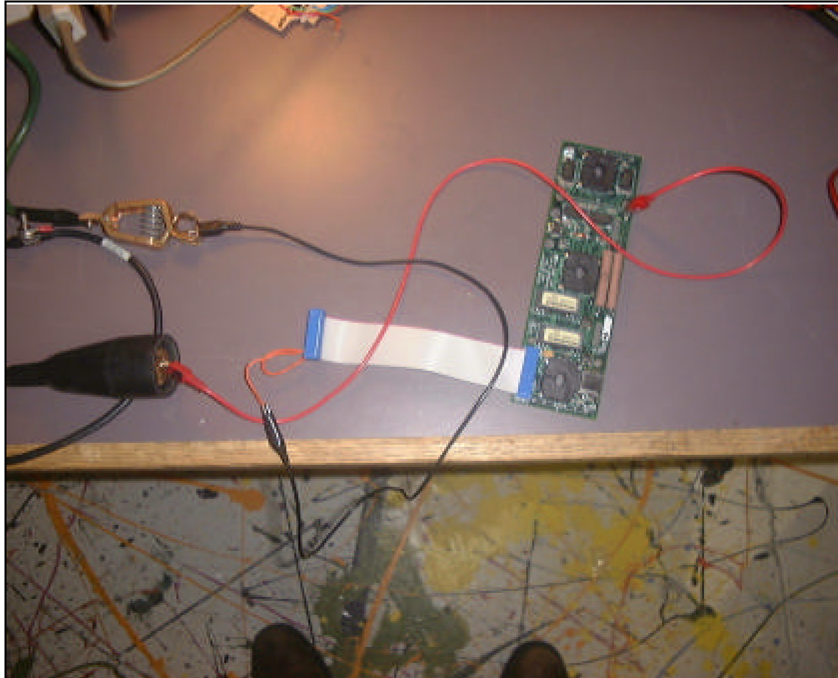


Figure 5.5-3: High Potential Test

For tests 2 through 4, the AIPM sensor interface board was installed into an AIPM module, and then run at various power levels. This test is shown below:

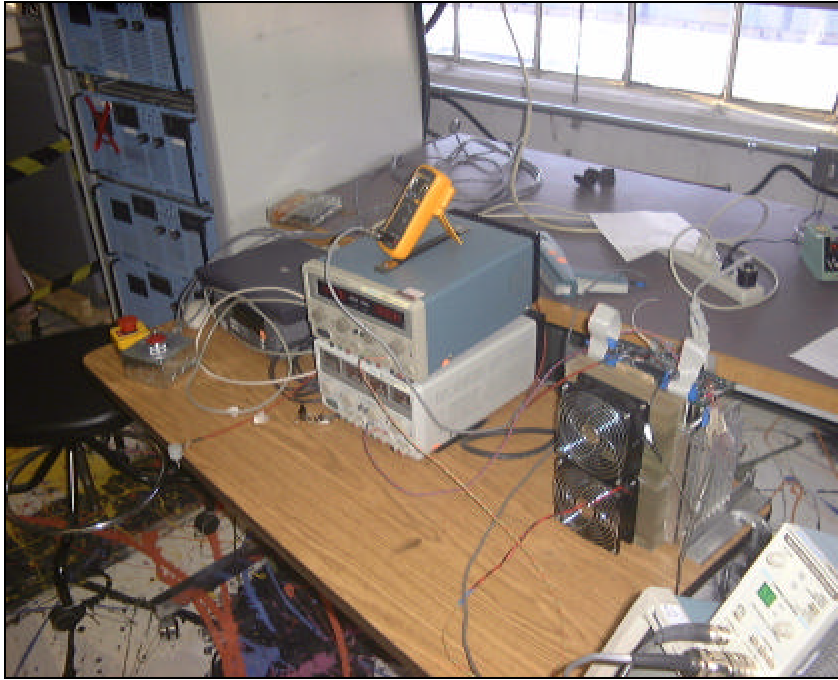


Figure 5.5-4: (left to right), 30kW power supply rack, logic power supplies, Air-cooled AIPM module, and Oscilloscope.

Figure 5.5-5: Inductive and Resistive load bank

During these tests, the following variables are monitored using the AIPM module with respective the sensor interface board installed:

Parameter	Units	Power: Amplitude	DC
Input Voltage	Volts		
Input Current	Amps		
Input Power	Watts		
V_Phase_A	Volts		
V_Phase_B	Volts		
V_Phase_C	Volts		
V_DC_Link	Volts		
I_Phase_A	Volts		
I_Phase_B	Volts		
I_Phase_C	Volts		

Table 5.5-1

These measurements are taken for nine different V-I levels using the original, non-isolated voltage sensing board. This board is then replaced with the 100A621-001 assembly, which is the new board, configured for non-isolated voltage sensing. After completing a second full set of measurements, the AIPM module is reconfigured with the 100A621-005 assembly, which is the isolated configuration of the new sensor interface board.

Comparison of these three configurations showed promising results. Each board showed comparable DC offsets with the others for given situations (within 100mV). Voltage and current measurements were accurate (within 200 mV). This test gives measurements that are within 5% of each other for given power levels using the different boards. Therefore, the new board produced in this research effort is drop-in-compatible with the previous boards, while providing means for power-control isolation.

6. Parallel Inverter Control

6.1. Objective

Replacing a single lumped power supply unit with multiple, smaller, units connected in parallel can increase both the reliability and the total power availability of the power system. The resulting distributed power system has a number of desirable features such as modularity, expandability, redundancy, and increased reliability. The parallel connected modules, however, need to share the load fairly equally. If the modules were absolutely identical, or absolutely ideal, this might occur naturally but the reality is a distribution of non-idealities such that the modules do not want to parallel naturally. Appropriate control schemes need to be provided so the load is properly shared. Such aspects as non-uniformity of the units, internal component tolerances, and variations of the interconnections and filtering affect the load sharing.

There are a number of techniques available to address the issue of paralleling. The most common approaches require physical interconnection of controllers among the units. This imposes a restriction on the location of units as well as the need for physical wiring, which can be a source of noise and potentially a cause of system failure.
In the case of parallel inverter modules fed from DC sources the choice of particular controller architecture depends on the following items:

- Characteristics of the input DC sources.
    - **Common DC Source:** all units are supplied from a common DC bus. Together with a common output all the units can form n(n-1)/2 independent loops for the currents to circulate among these units.
    - **Individual DC Sources:** each of the units has its own DC power source. If the DC voltage levels are significantly different, each unit will have a different PWM wave for identical output voltage. Resulting discrepancies in the harmonic content among units can cause harmonic crosscurrents to flow.
- Different module/unit designs
  The load sharing among units depends on:
    - The output impedance of the unit,
    - The impedance of the output filter,
    - Dynamic response of individual controllers
- Load connection:
  Three most common configurations of load connections are as follows.

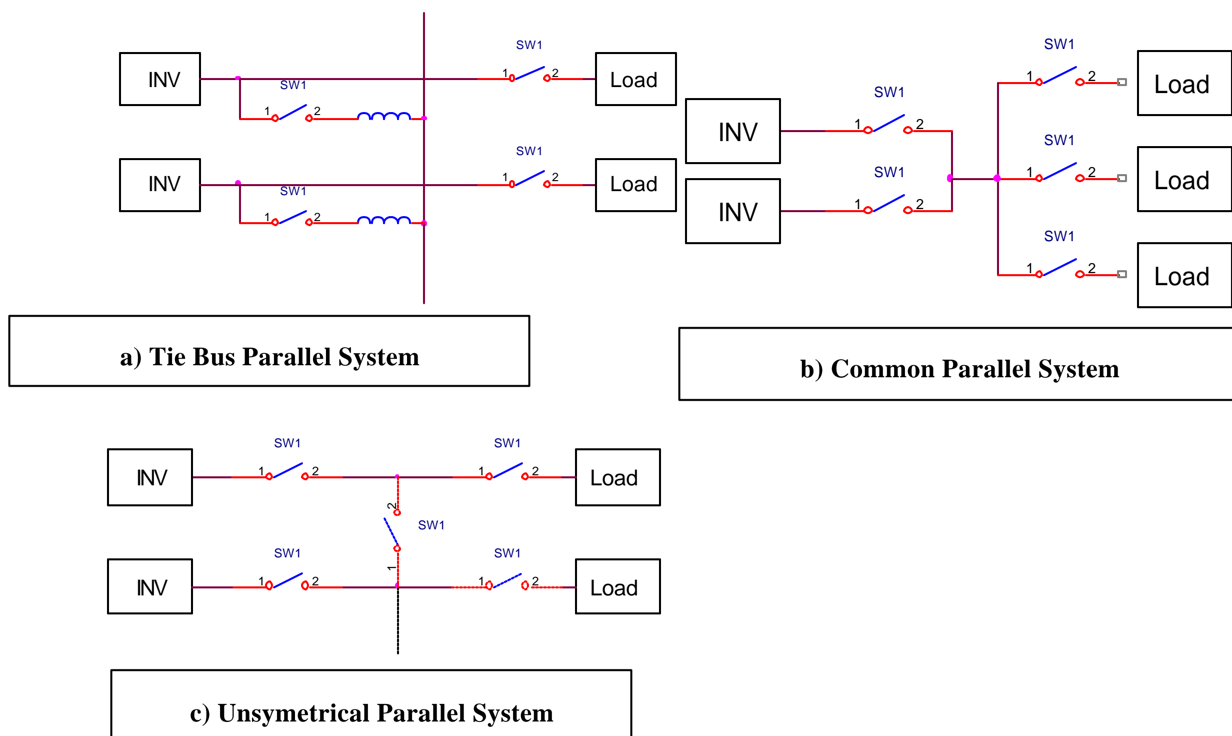


Figure 6.1-1. Parallel Configurations

6.2. Overview of Control Systems

The control of individual inverters needs to be based solely on the information that is locally available at the inverter. In practical distributed power systems, large physical distances between inverters makes a communication link tying the local controllers together impractical. Depending on the location of individual units or modules, the level of communication sophistication needs to degrade with distance. At physically disjoint units, the inverter control needs to be based only on terminal quantities (voltage, current).

6.3. Utility Interconnected (Grid-Connect) System

In the case of utility interconnected systems, the voltage of the output bus is externally provided and fixed. The control of paralleled units is therefore fairly simple. In the simplest, most common parallel topology, each inverter is configured as a current source. Since the stiff utility bus can be considered as a near-ideal voltage source with zero impedance, the paralleled units do not need to interact and can be considered independent. The overarching criteria is that each unit operate within its limits, at some level equal sharing is not that important provided each unit is operating within its Safe Operating Area. In fact, if the issue of sharing were paralleling voltage source inverters (VSI), the task of the controller would be to regulate the commanded reactive and real power injected into the grid. This method mimics the operation of synchronous generators interconnected with a grid. The current and the power quality to a large degree will depend on the grid voltage quality. If there is a slight distortion or imbalance in the grid voltage, the inverter output current will be distorted. The overall system power quality is further degraded since the inverter presents low impedance to already existing distortion voltage. The current source inverter is thus a better choice, as its output impedance is much higher within a bandwidth of the controller. This minimizes the voltage harmonics effect on the output power quality. The controller schematics are provided in ***Figure 6.3-1*** and ***Figure 6.3-2*** below.

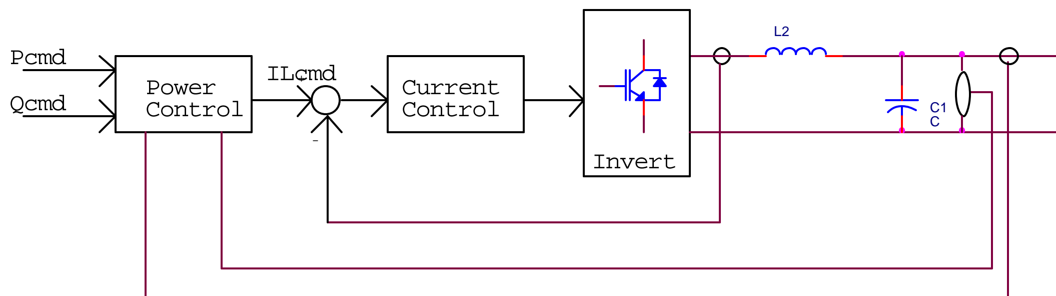


Figure 6.3-1. Current Controlled Utility Interconnected Inverter

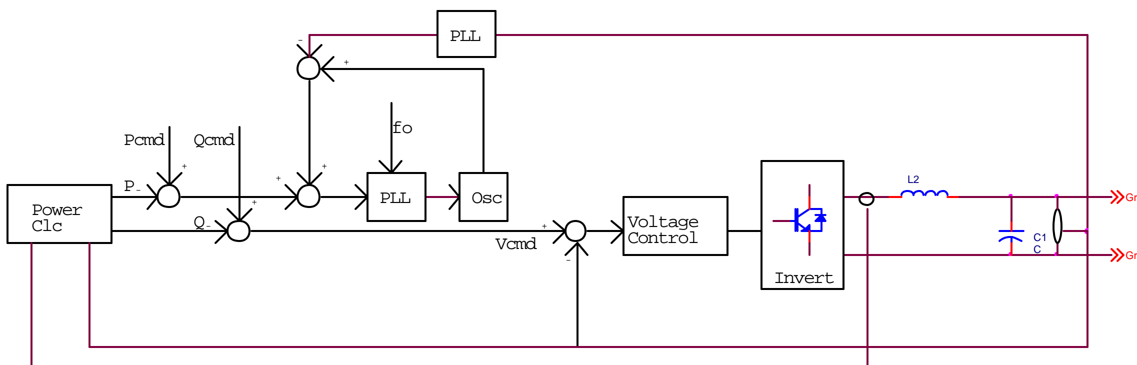


Figure 6.3-2. VSI Operating with Utility Line

Considering one might conclude that the best operating condition for the units to have in common is probably the operating temperature of the semiconductor junctions, therefore optimizing the total life of the system.

6.4. Stand-Alone System

The fundamental difference in the control technique of the stand-alone system from that of grid connected is the absence of AC side reference voltage. The interconnected inverters themselves produce the AC system voltage. This voltage is fed back to the control of each of the inverters. Emulation of parallel synchronous machines can be a way to interpret parallel connection of inverters. The inherent characteristics of such a system are:

- Fast frequency variation are limited by rotor mechanical inertia
- Synchronous machines connected in parallel tend to remain in synchronism due to the synchronizing torque attribute
- There is a natural correlation between the operating frequency (or power angle) and the output power. An increase in power angle or output frequency causes increase in output power.
- Output voltage is correlated with reactive power demand

In a stand-alone paralleled connected system the key to paralleling inverters lies in their control scheme modifications that the inverter can emulate a synchronous machine. The power electronics inverters are normally designed such that the output voltage and frequency factors are independent of load. Therefore, there is no natural self-synchronizing force present when two or more inverters are tied together. When the paralleled power electronics units have aforementioned characteristics of a synchronous machine, their paralleling becomes simple. There are several techniques that utilize the idea of synchronous machine emulation. They all share the essential premise of variation of output quantities of voltage and frequency with induced by deviations in both active and reactive output power. These are the three most commonly used control techniques:

Voltage and Frequency droop:

A droop in frequency and voltage accordingly to the output real and reactive power levels is utilized in this scheme shown in ***Figure 6.4-1***.

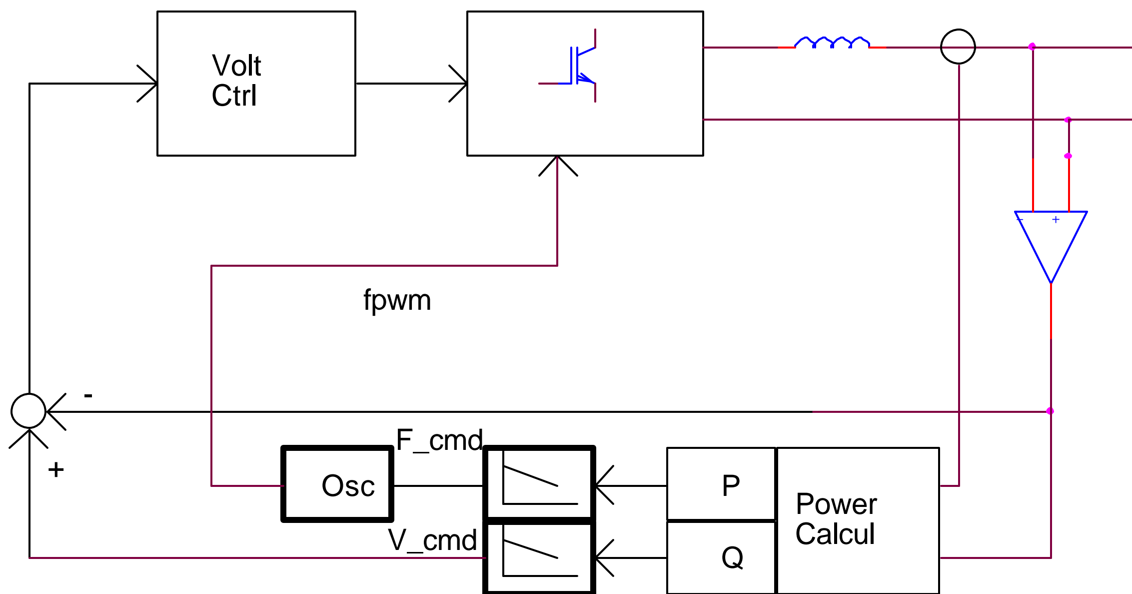


Figure 6.4-1. Droop Control

The droop characteristics reduce the frequency and output voltage commands with increase in output power P and reactive power Q, respectively.

Power Deviation Control:

This method is based on feeding information for a difference between inverter's own current and I_L/n (total load current, I_L, divided by the number of operating units). The objective of the controller is to adjust the frequency and voltage commands to minimize the active component ΔP and reactive component ΔQ of the current unbalance ΔI as shown in ***Figure 6.4-2***.

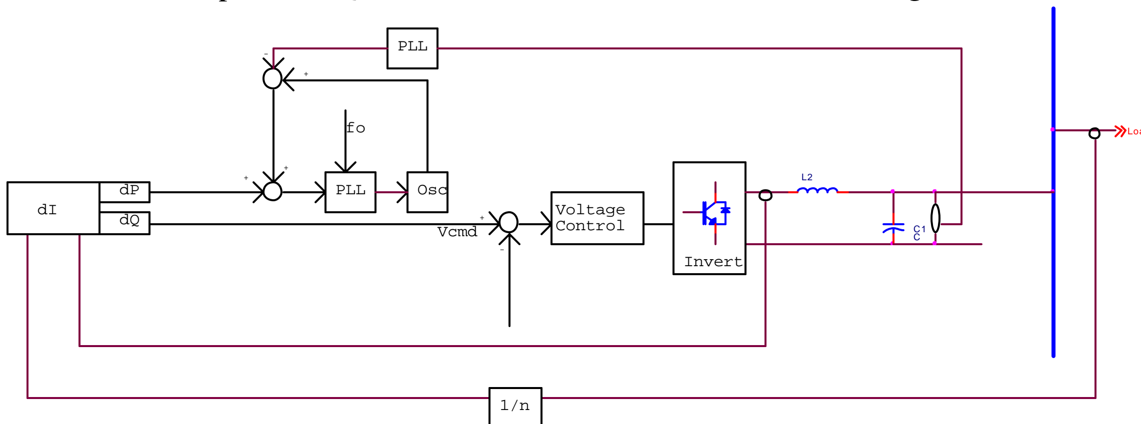


Figure 6.4-2. Power Deviation Control

Current Feedforward:

To produce a sinusoidal output voltage for the interconnecting bus, the current to flow through the output filter capacitor can be determined as follows:

$$i_c^* = \boldsymbol{w} * C_f * V_o * \sin(\boldsymbol{w}t)$$

Where V_o, C_f, and ω are output voltage, filter capacitance, and output frequency, respectively. The calculated filter capacitor current is fed-forward to the current controller. For a faster response to load current variations, additionally the inverter output current is fed-forward to the current controller. The deviation between the inverter current and a fraction of the load current the inverter is supposed to contribute is used to establish the phase and frequency quantities. The inner minor current loop limits to acceptable limits the inverter output current.
The configuration of this control implementation is shown in ***Figure 6.4-3***.

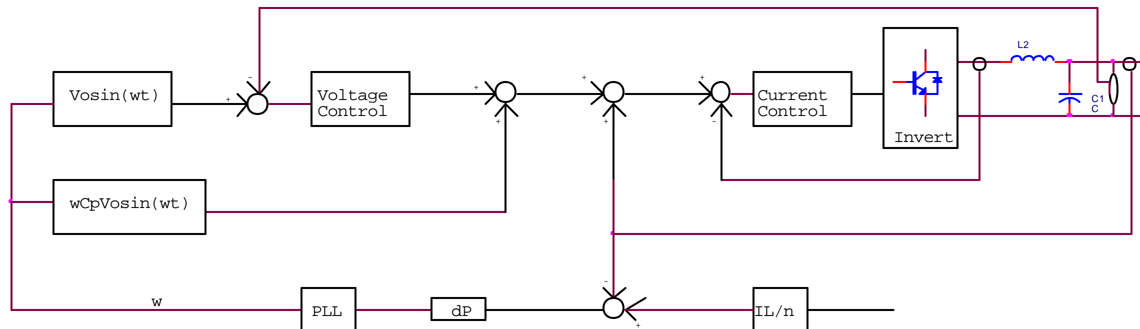


Figure 6.4-3. Feedforward Control

The most important aspects of a design of a parallel operation system should be dictated by protection, ease of operation, flexibility, and modularity.

The ultimate goal of the controller is to make the inverter capable of operating in parallel with no external communication link.

6.5. Smart Gate Drivers

The concept of paralleling can be extended to paralleling individual switching devices and/or switching modules within an inverter. The need for paralleling switching devices is mainly noticeable in high current conversion systems (transport applications, electrochemical processes, etc.). There are many reasons why there is a limit for the number of single IGBT chips that are paralleled. The main reasons are reliability and cost. The discrepancy in current among paralleled devices or modules, reduces reliability, and necessitates employing more devices in parallel, and contributes to increase the overall cost of the system. Modularity or devices paralleling concepts increase reliability. The paralleled modules may be designed to operate below current limit and during abnormal conditions or failures; the system can continue to operate at lower current ratings.

The goal of parallel operation between modules or discrete devices is to provide a mechanism that enforces the current to be balanced between the modules. Ideally, the currents need to be balanced at all times, i.e., during ON times as well as during transients (Turn -ONs and -OFFs). The static current sharing (ON of OFF times) is affected by differences in:

- The gate voltage levels
- Collector-emitter ON voltage drops
- Resistive part of device connection

The dynamic sharing of currents could be more difficult to achieve. This type of sharing is disturbed mainly by:

- Gate propagation delay
- Threshold voltage and Miller capacitance of individual IGBTs or modules
- Stray inductance of the individual devices connection

The discrepancies in dynamic sharing of current can accelerate aging of those devices that are the most exposed to higher dynamic stress. The static sharing asymmetries can cause destructing the devices due to excessive losses turned into heat.

As a part of this project, SatCon Applied Technology developed a "smart driver" technique for paralleling either single devices or the entire modules. The goal of the smart drivers is to balance the current in the paralleled devices/modules by conditioning the gate signals to avoid aforementioned problems. The technique is quite universal and it could be used in conjunction with equalization of individual devices/modules temperature balance.

6.6. Fuzzy Control of Smart Drivers

In the early stage of the smart drivers development, fuzzy logic was used to control the conditioning of the gate signals. A preliminary simulation model was developed. Initial results indicated that the idea behind introduction of delays to gate signals was fundamentally correct. The amount of delay introduced to the gate of the individual device is a function of both the temperature and the rate of change of the device temperature.

A simplified thermal model of two parallel-connected devices was developed. That model was next realized in a Matlab/Simulink environment. In this approach a Fuzzy System of control was introduced. Two external parameters were introduced in this model and were used as the state variables. These parameters are: Temperature and Rate of Change in temperature. The output of the controller is a delay that is applied to the PWM gating signal.

The initial choice of fuzzy logic control stems from the simple fact that in the case of "smart" drivers it is easier to express the amount of delay in linguistic terms than in classic ones (crisp terms). For example: one may like to introduce a "moderate" delay when the device is "warm" and the rate of change in its temperature is "positive small". These terms in quotas may be interpreted as those used by an experienced operator or expert. The distinction between "warm' and "hot" is rather smooth than precisely determined. Initially two input variables were used – temperature of the device and the rate of change of the temperature to determine what kind of delay needs to be introduced.

Figure 6.6-1 shows the fuzzy membership functions and the output (delay) membership function definitions. The rate of change in temperature is divided into seven linguistic terms (***Figure 6.6-2***):

- Negative Large
- Negative
- Negative Small
- Zero
- Positive Small

- Positive
- Positive Large

The temperature of the device is divided into five ranges (***Figure 6.6-3***):

- Cold
- Cool
- Normal
- Warm
- Hot

Delay as the output function of the fuzzy controller is defined in terms of fuzzy rules and this relationship is shown in ***Figure 6.6-4***.

A Simulink block diagram is shown in ***Figure 6.6-5.*** Two identical Fuzzy Logic controllers are used to monitor temperature of their controlled devices. The action of each of the controllers is independent of one another. Yet, the results of the simulation (shown in ***Figure 6.6-6***) indicate that temperatures of each of the devices gradually converge to a nearly common for both devices temperature level.

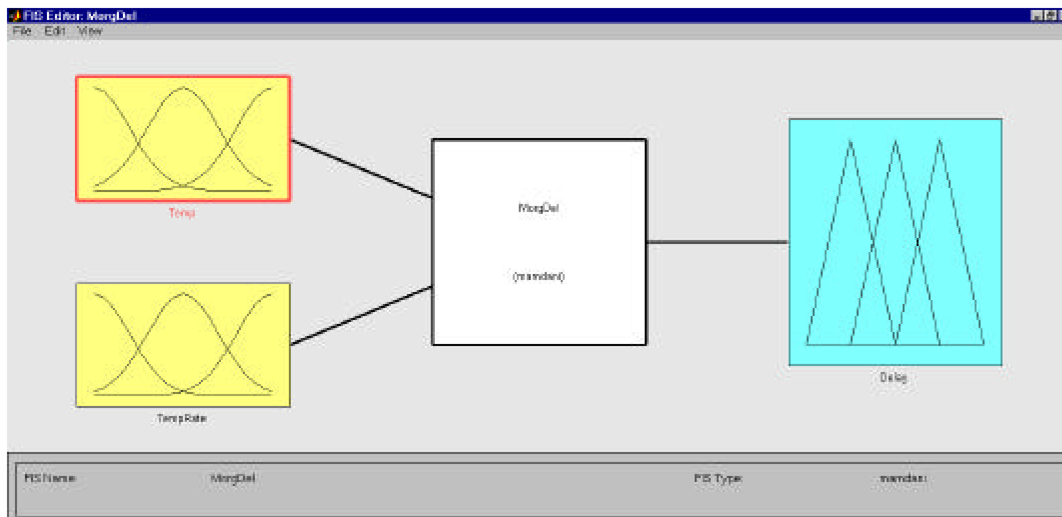


Figure 6.6-1. Fuzzy Input/Output Definition

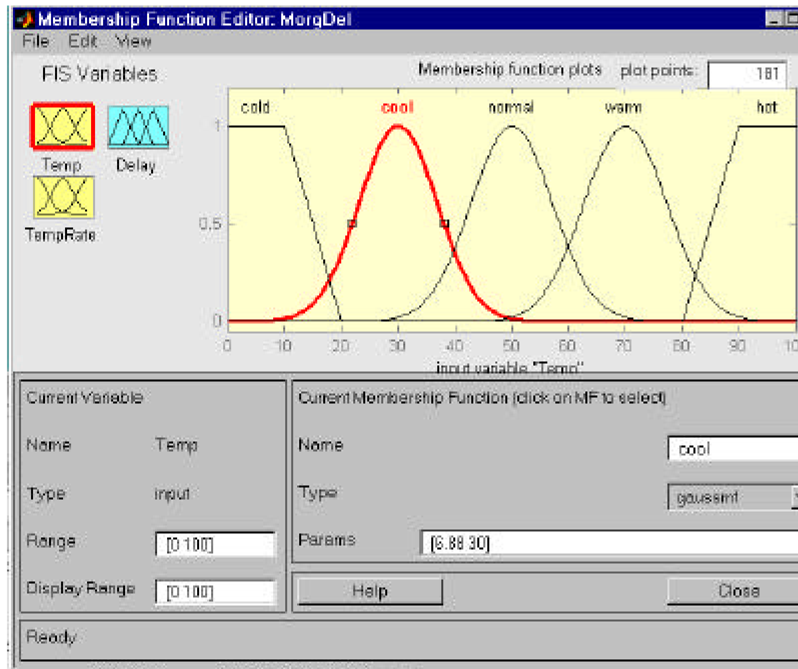


Figure 6.6-2. Rate of Change of Temperature Membership Function

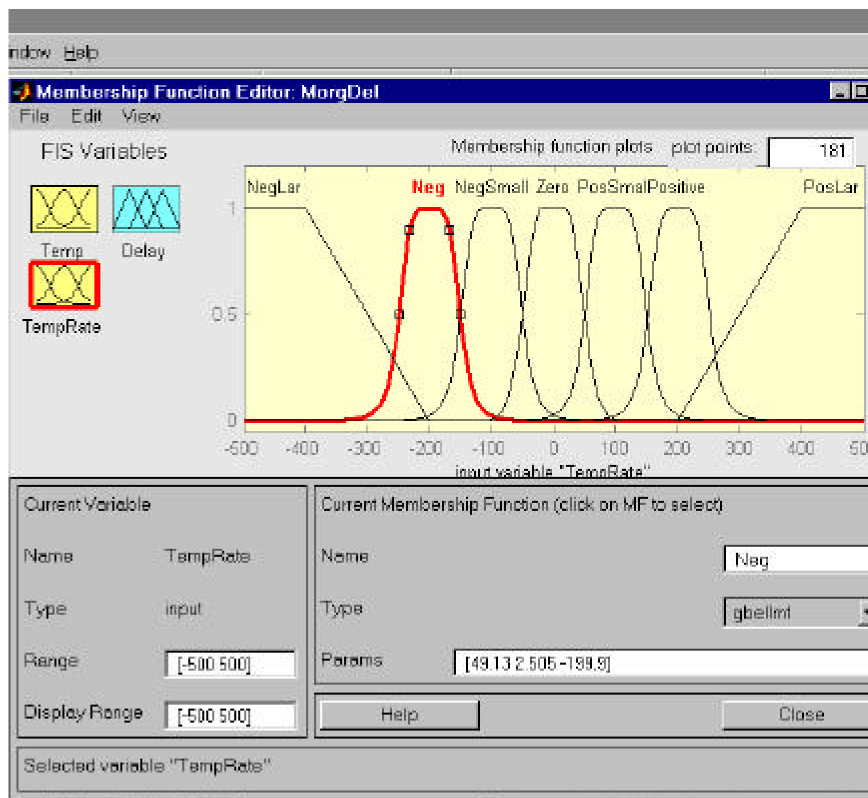


Figure 6.6-3. Temperature Membership Function

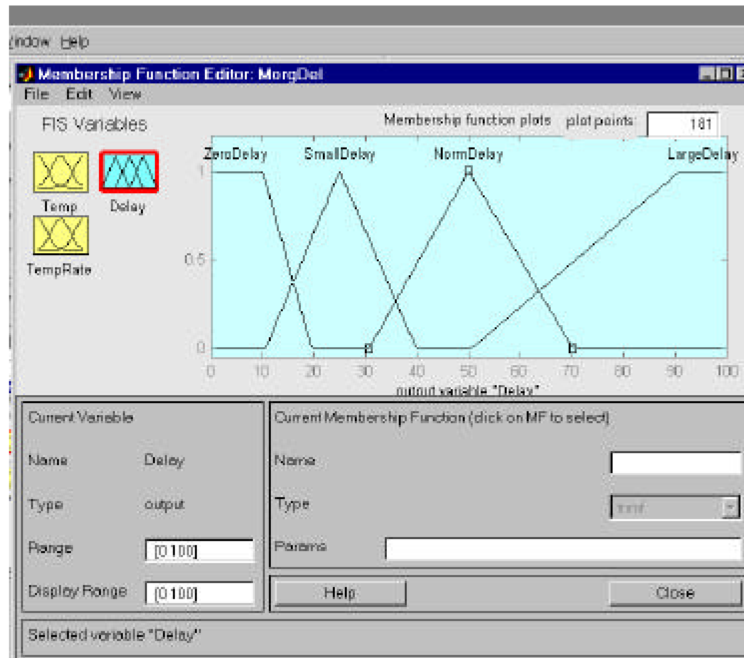


Figure 6.6-4. Fuzzy Rules For the Delay

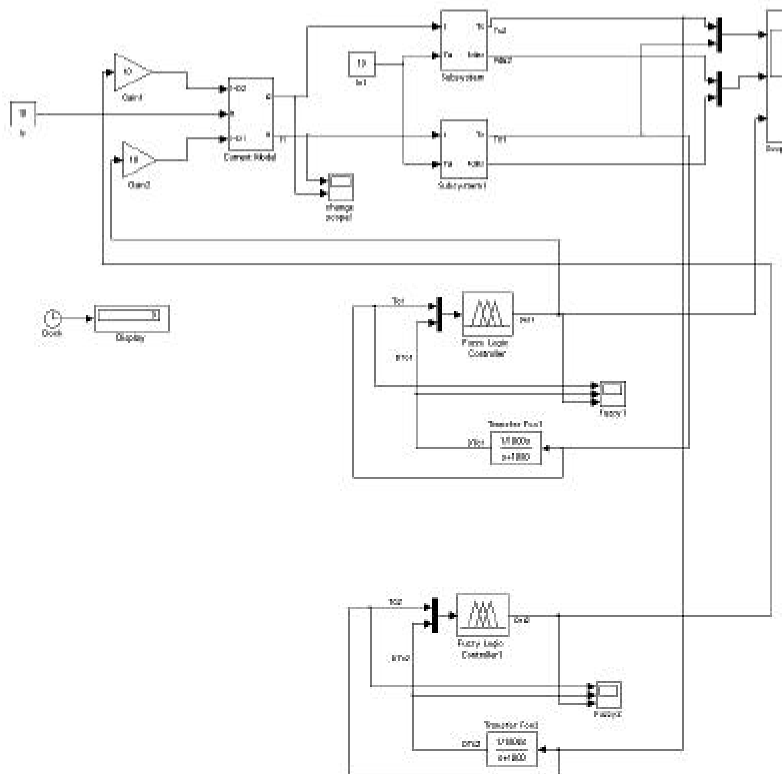


Figure 6.6-5. Simulation Block Diagram

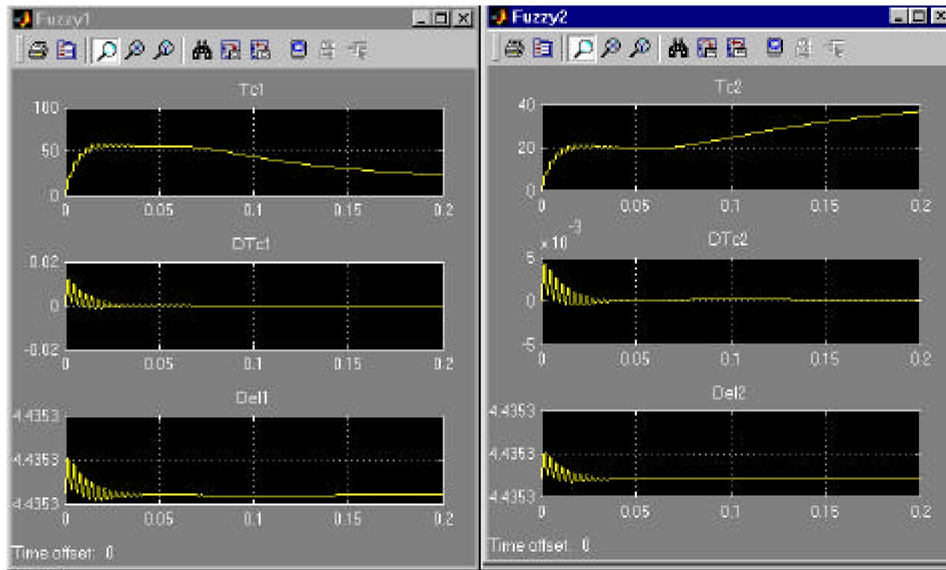


Figure 6.6-6. Simulation Results of Temperature Control with Fuzzy Logic

The initial simulation demonstrated a validity of the approach. When two or more devices are paralleled, their temperatures can be controlled independently. It is sufficient that each device/module temperature is monitored and controlled. In this case a fuzzy controller was utilized to quickly validate the approach. The fuzzy controller realization does not precisely quantify and define the output parameter (delay) in terms of input parameters (temperature and a rate of change in device temperature). A more rigorous and formal approach was later used in further development of the balancing current technique. The next section presents a simulation and realization of this method.

6.7. Simulation and Realization of Smart Gate Drivers

The following schematics were created in PSIM to represent two, Paralleled H-Bridges.

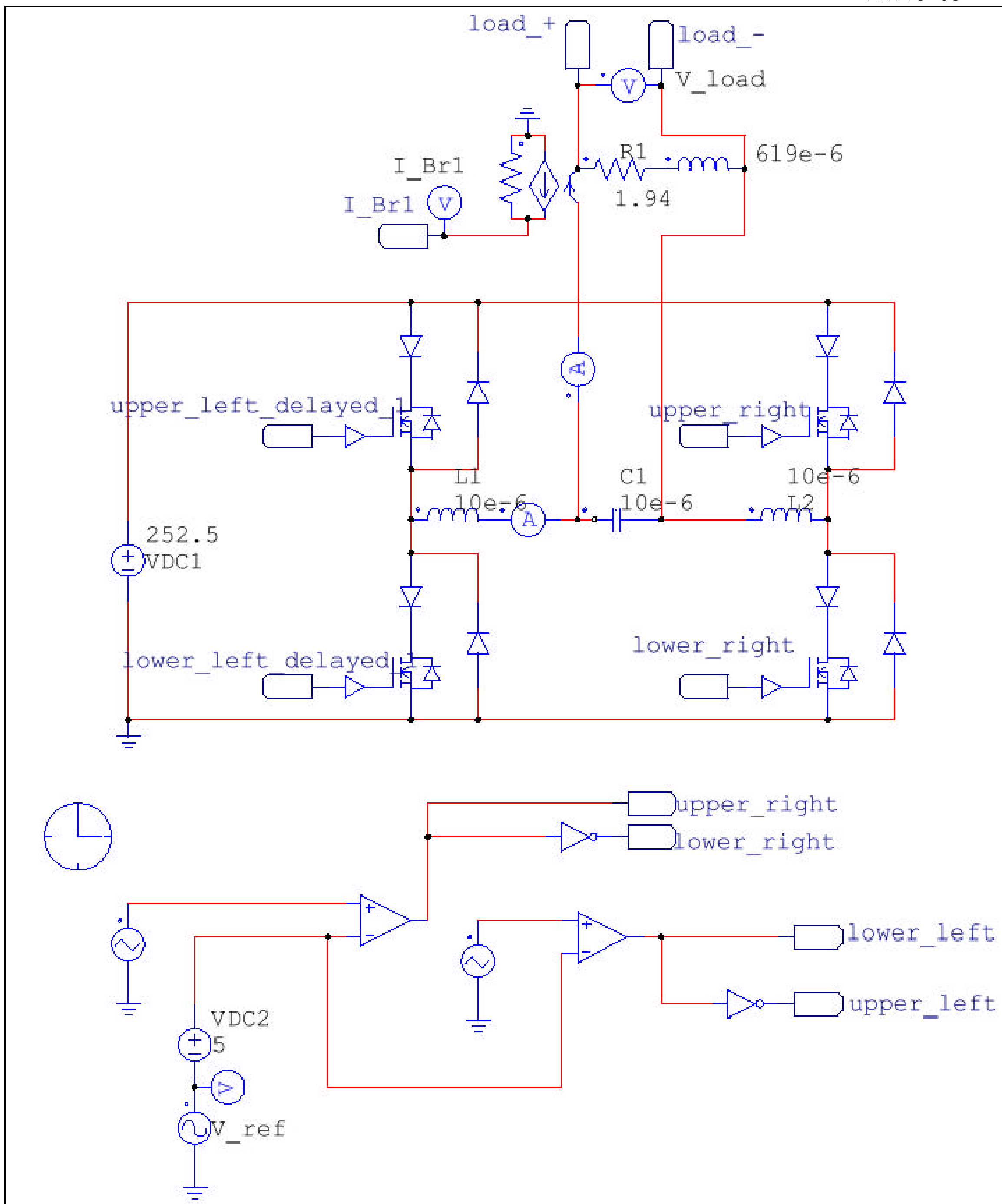


Figure 6.7-1: PSIM, 1st H-Bridge and linear part of load

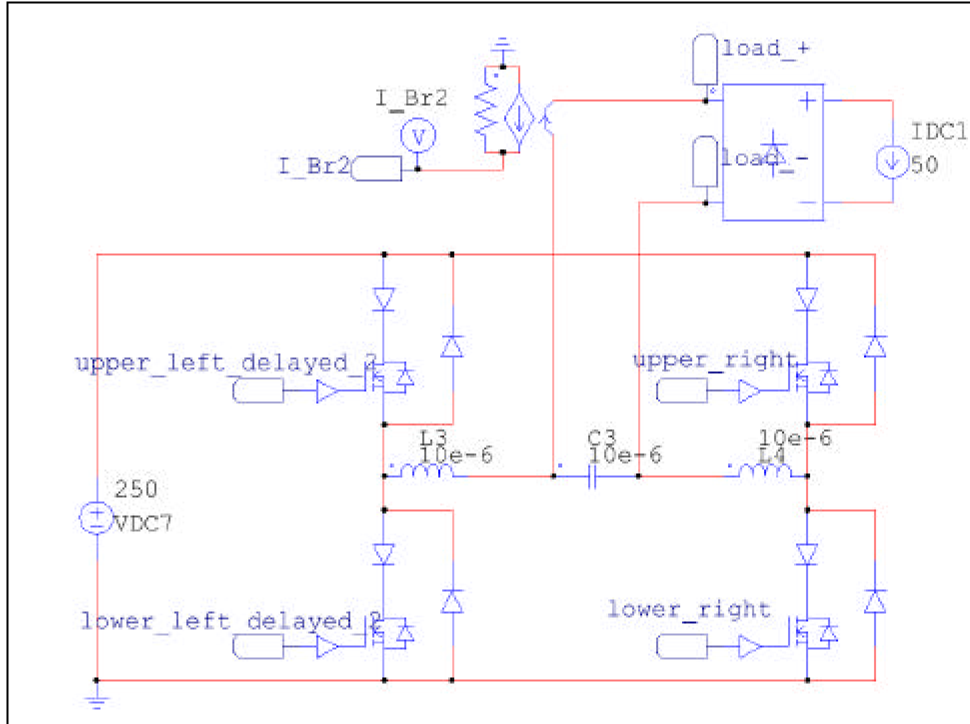


Figure 6.7-2: PSIM 2nd H-Bridge and non-linear part of load

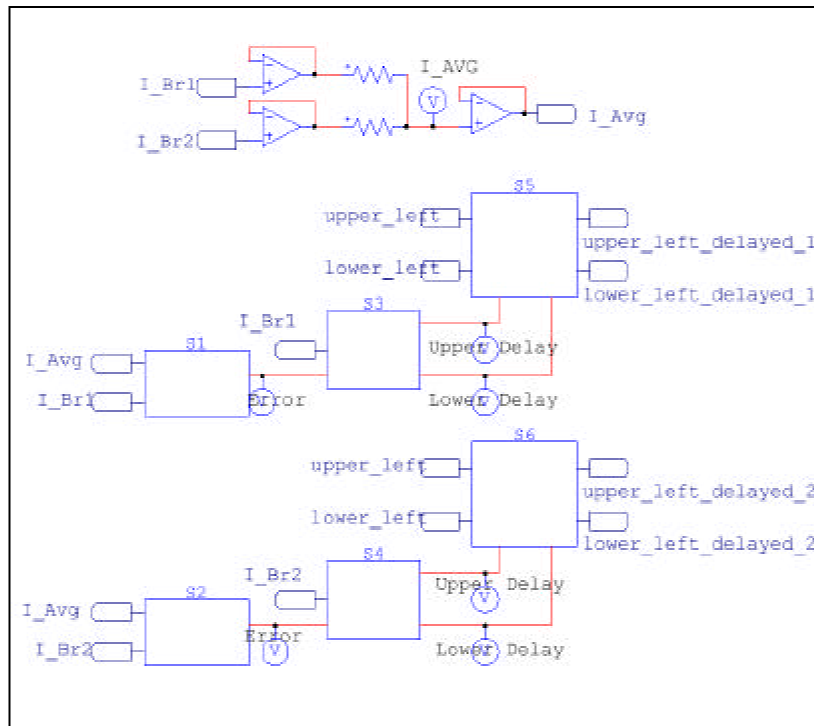


Figure 6.7-3: PSIM, Overview of Delay Control

Figure 6.7-4: PSIM, Blocks S1 and S2, Error

Figure 6.7-5: PSIM, Blocks S3 and S4, Delay Selection

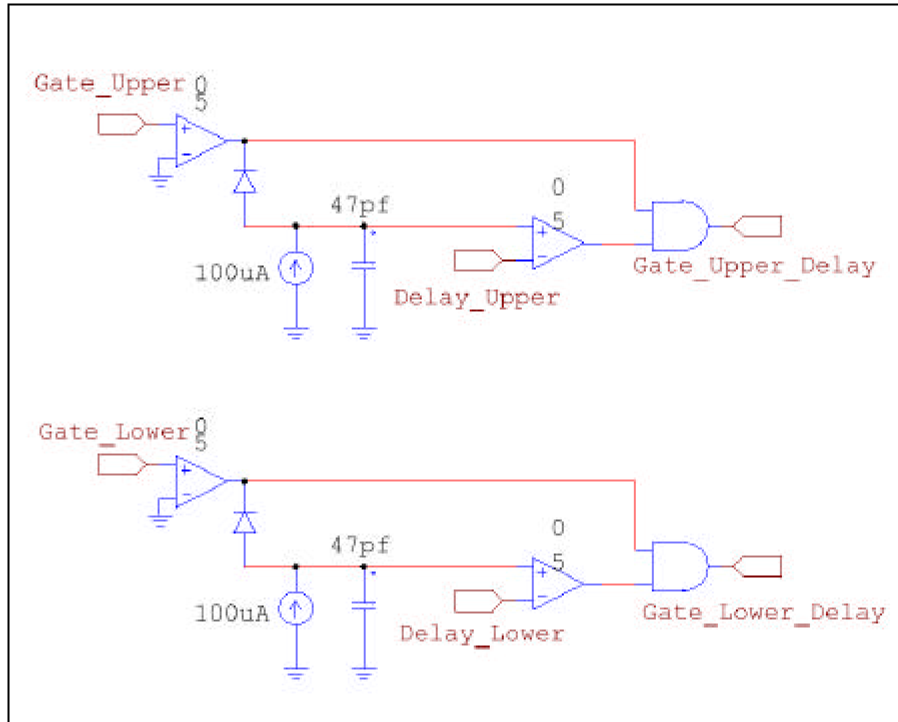


Figure 6.7-6: PSIM, Blocks S5 and S6, Delay Implementation

Using PSIM, the a DC imbalance of 2.5 V results in the following:

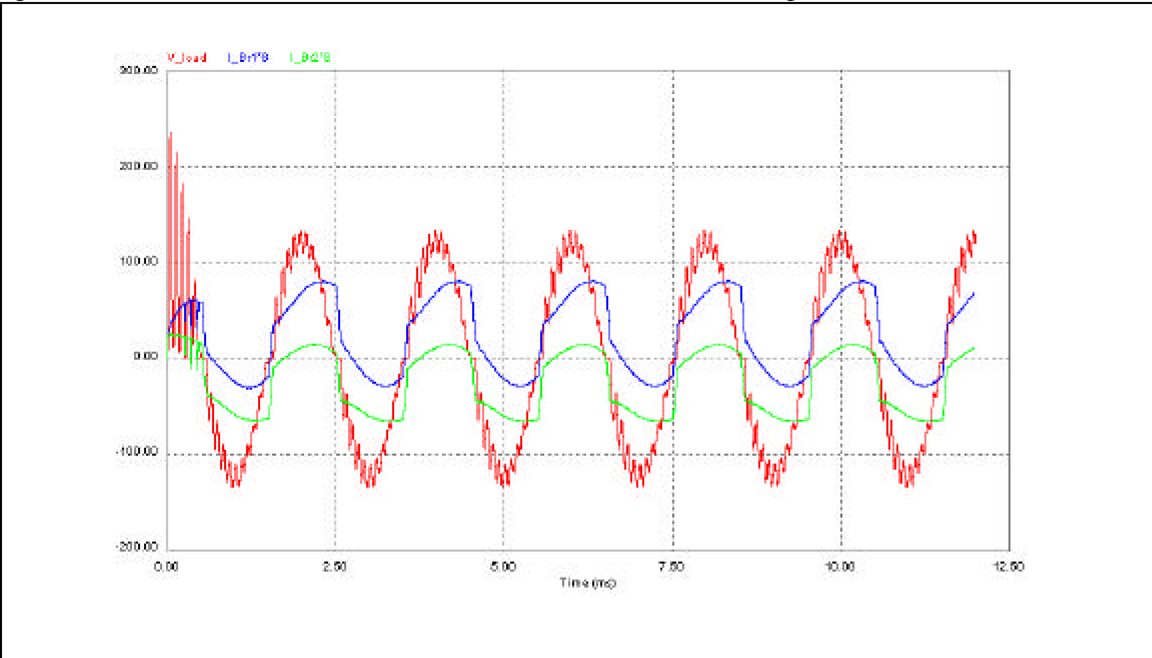


Figure 6.7-7: PSIM, Uncontrolled Response

Adding PI based delay control:

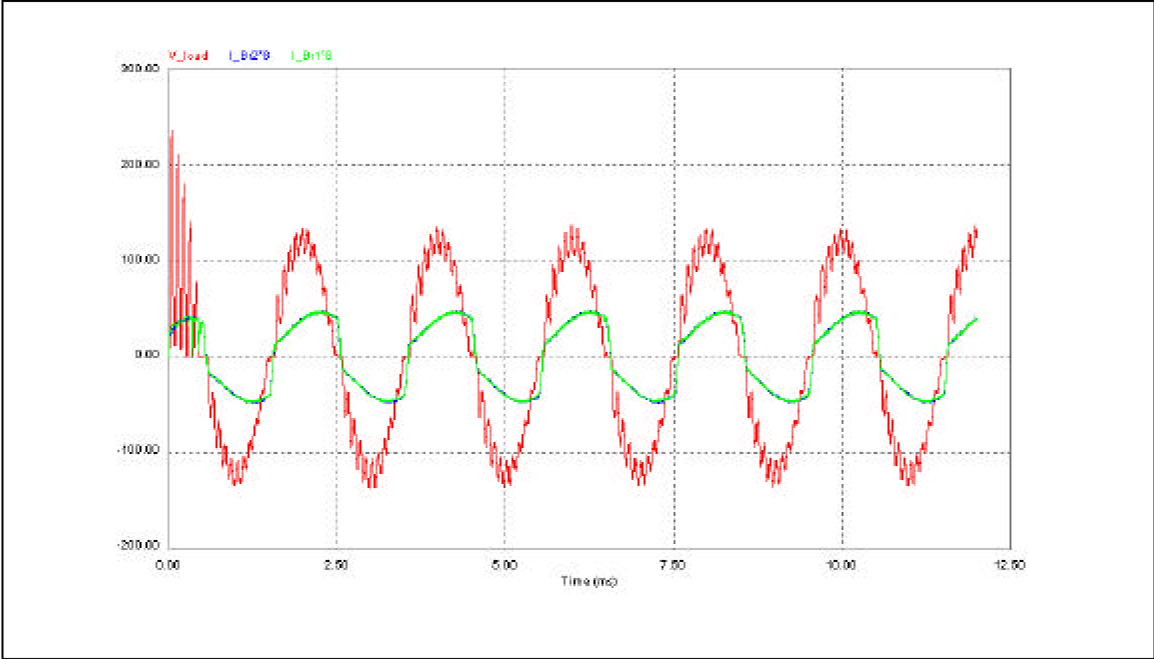


Figure 6.7-8: PSIM Controlled Response

The following OrCad schematic documents a physical design. These can be found here for HI-RES:

Orcad\Delay_control_final.PDF

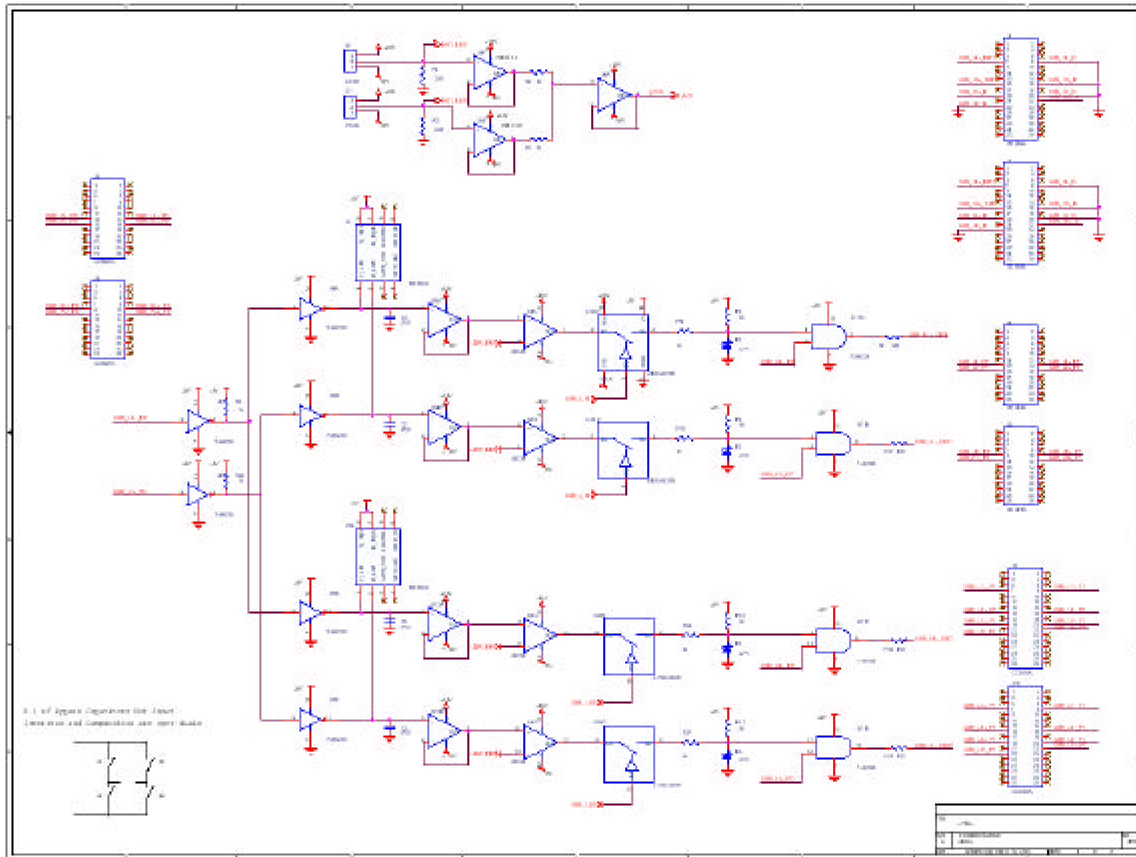


Figure 6.7-9: OrCad Page 1

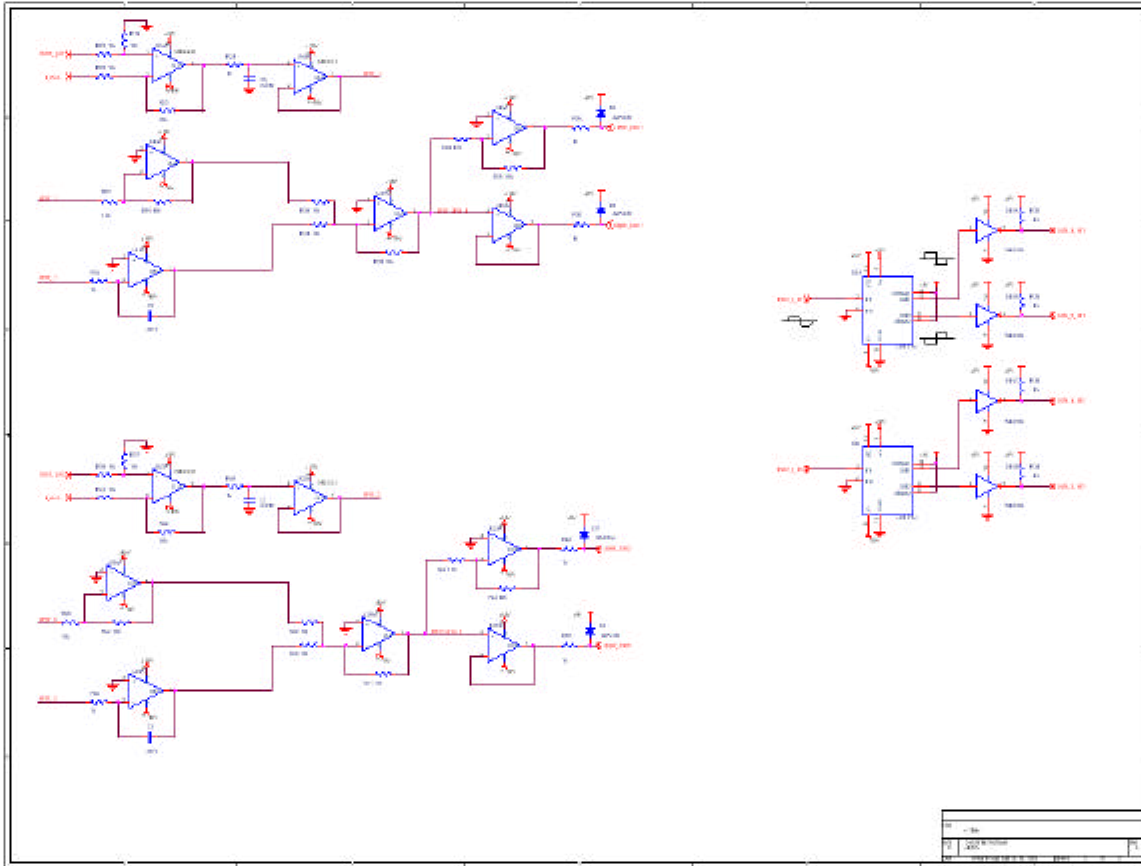


Figure 6.7-10: OrCad, Page 2

The following breadboard was built using the OrCad schematics.

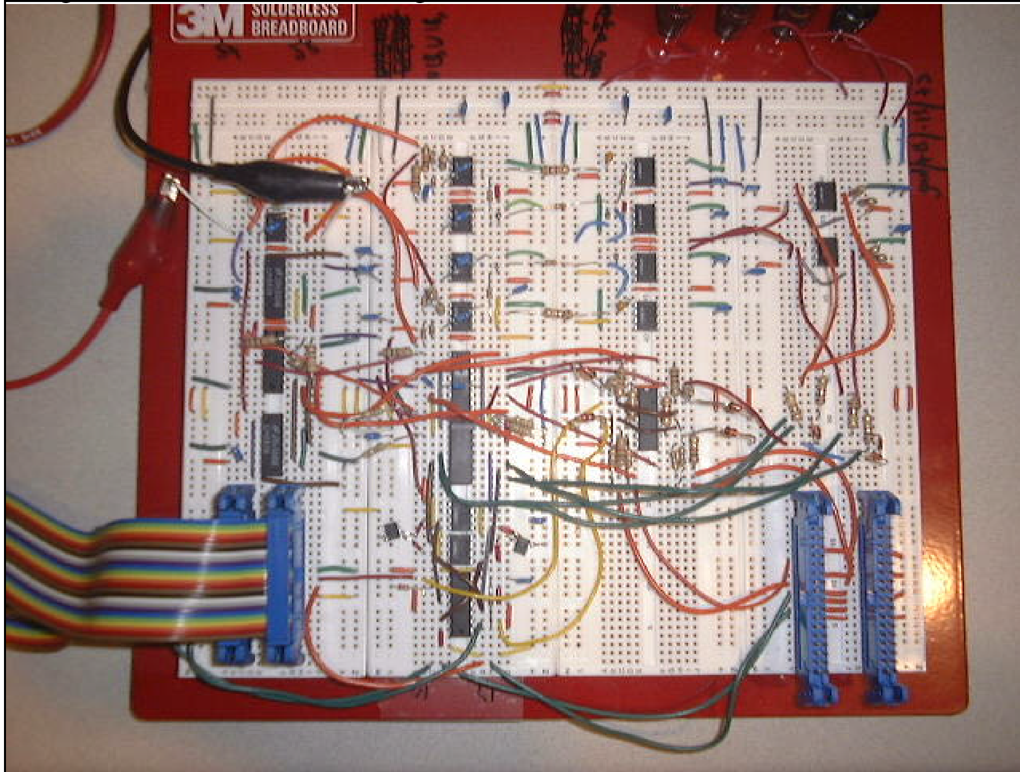


Figure 6.7-11: Breadboard Controller

Next we used the HEV board to generate a PWM gating signal and a variable DC power supply to simulate current sense inputs. Because the controller is a PI type, the DC error compounds quickly to the maximum value due to lack of feedback in the test setup. This results in the maximum delay of 3us. The following show both delayed and non-delayed gating input and outputs.

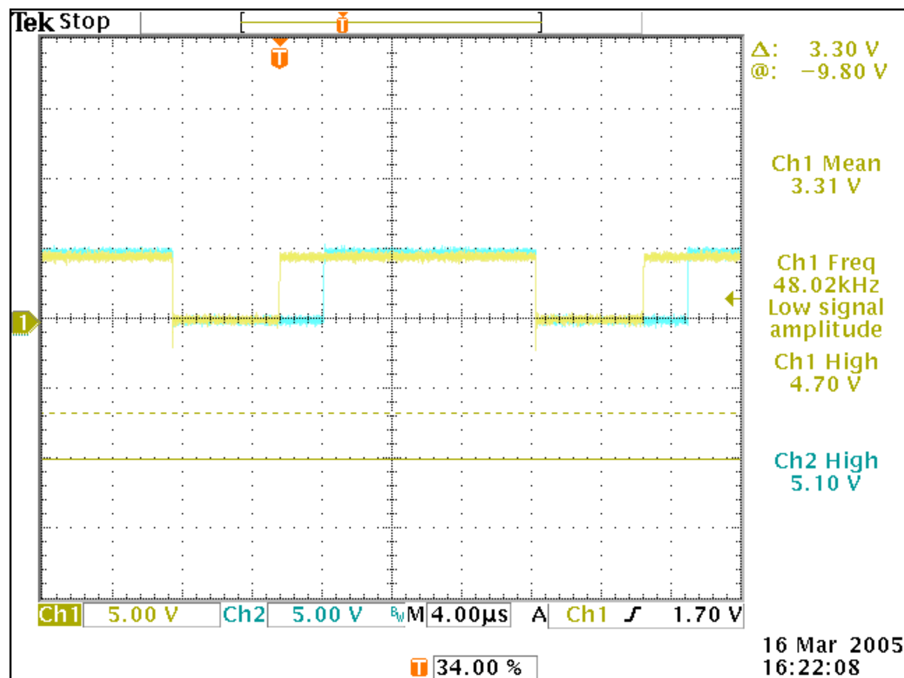


Figure 6.7-12: Blue is delayed output with 3us turn on delay, Yellow is input

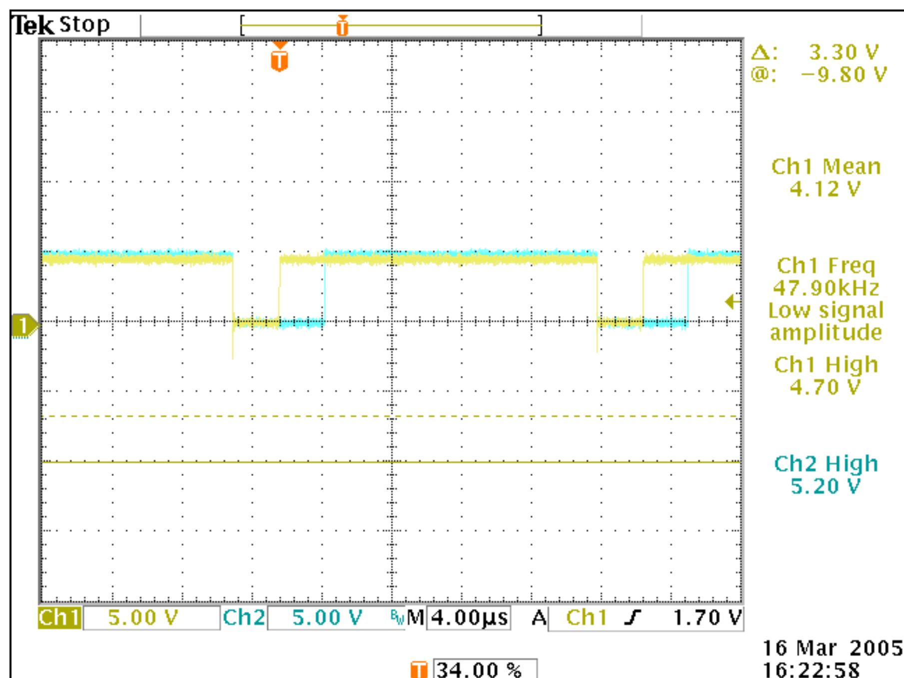


Figure 6.7-13: Blue is delayed output with 3us turn on delay, Yellow is input

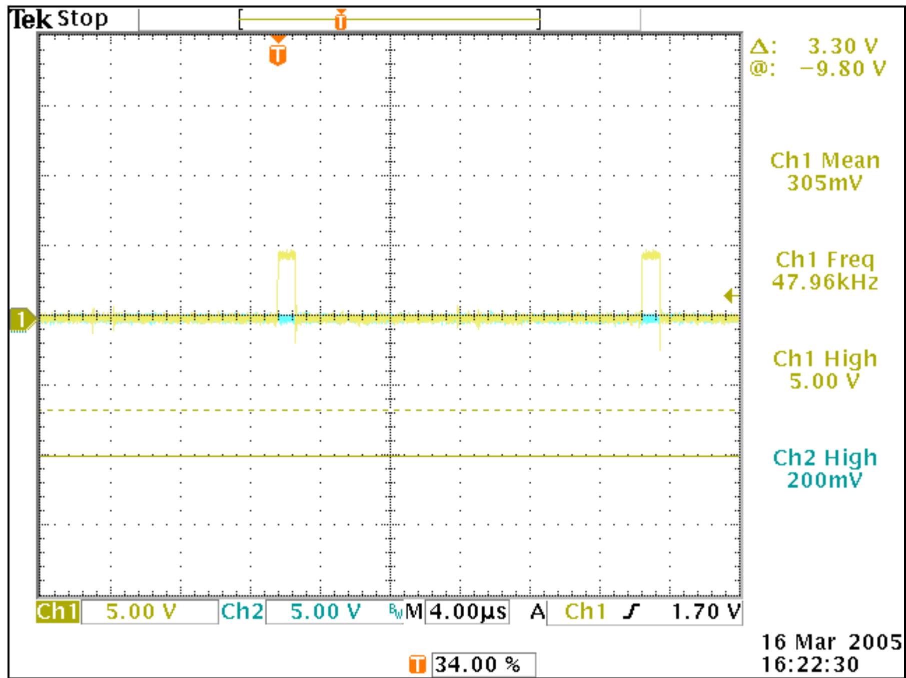


Figure 6.7-14: Blue is delayed output with 3us turn on delay, Yellow is input

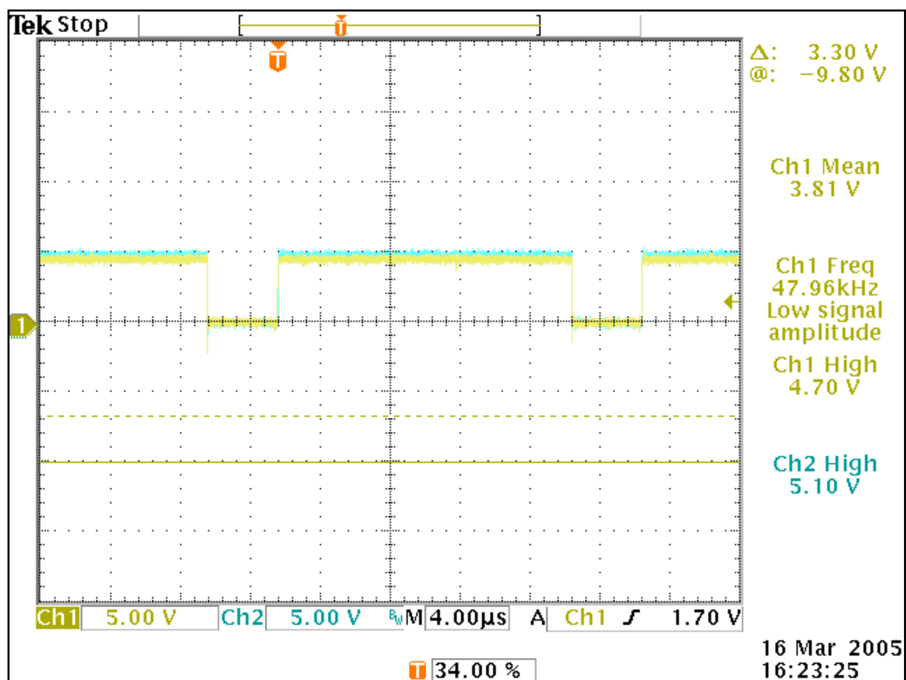


Figure 6.7-15: Blue is output with no delay, Yellow is input

Scale for Currents is 1/8 Volt per Amp

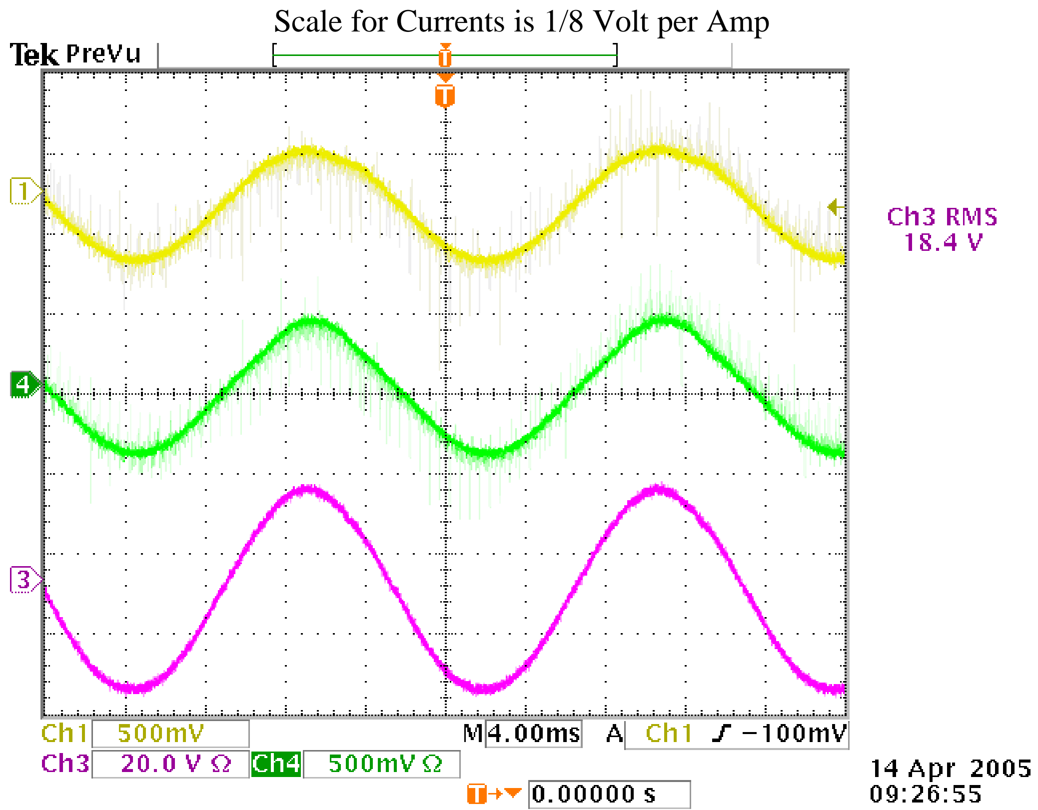


Figure 6.7-16: PM10s with no imbalance

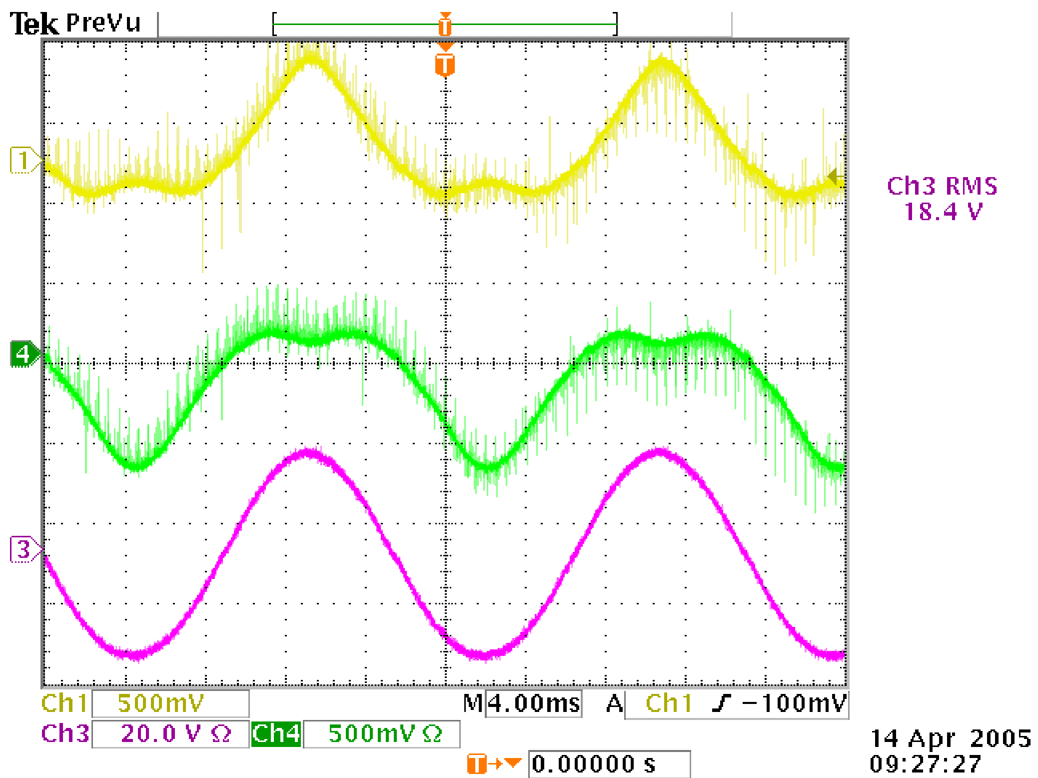


Figure 6.7-17: 0.3 Ohm resistor placed in line with Bridge 1

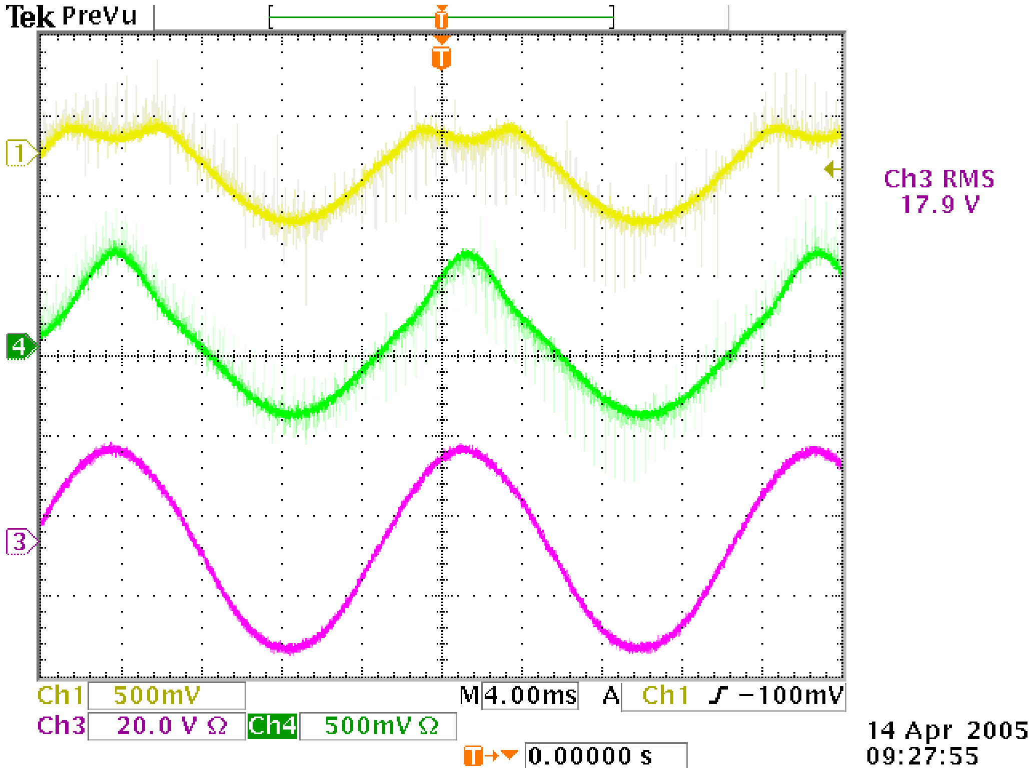


Figure 6.7-18: Applying neg DC error to Br1

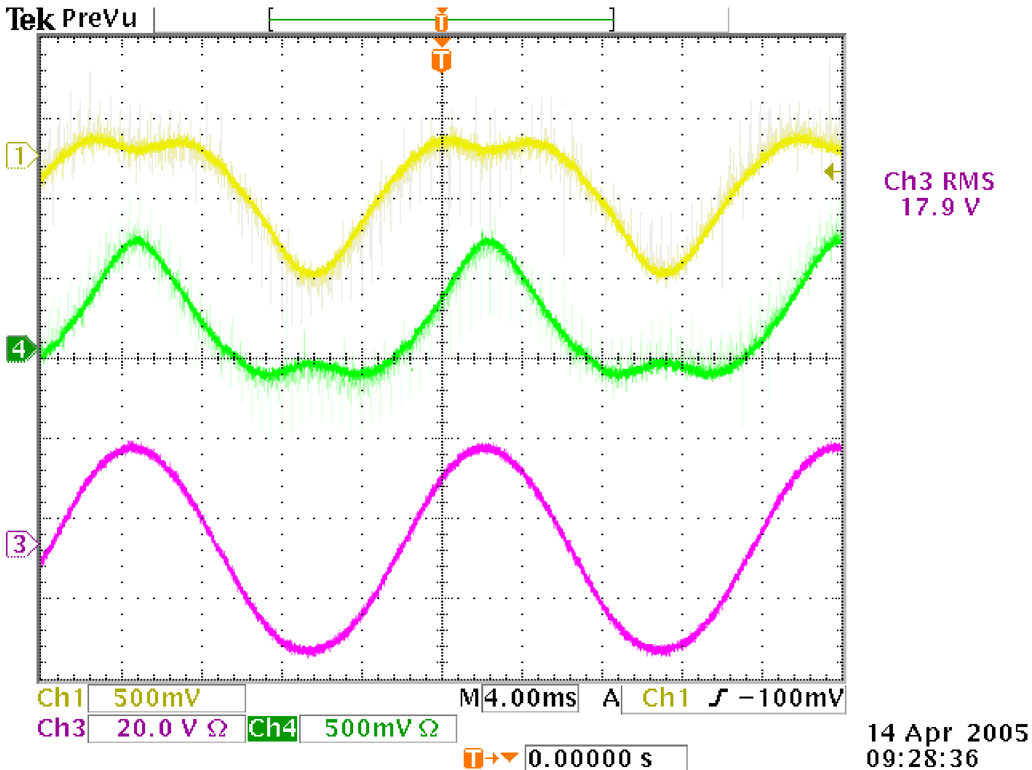


Figure 6.7-19: Applying pos DC error to Br1

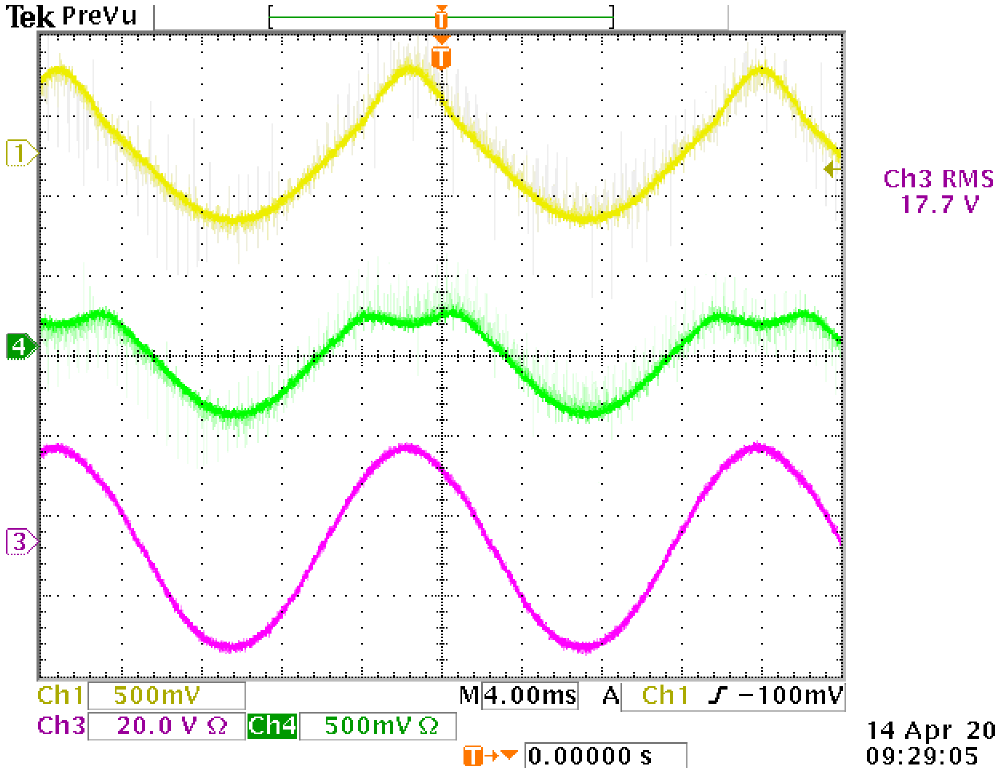


Figure 6.7-20: Applying neg DC error to Br2

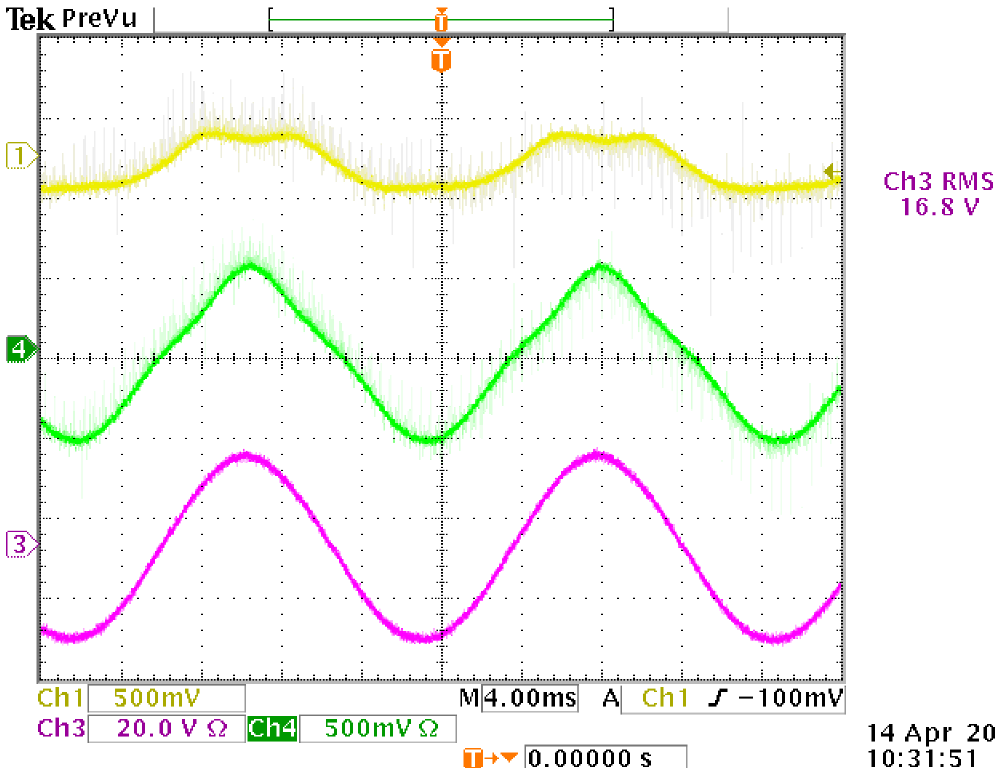


Figure 6.7-21: Applying pos DC error to Br2

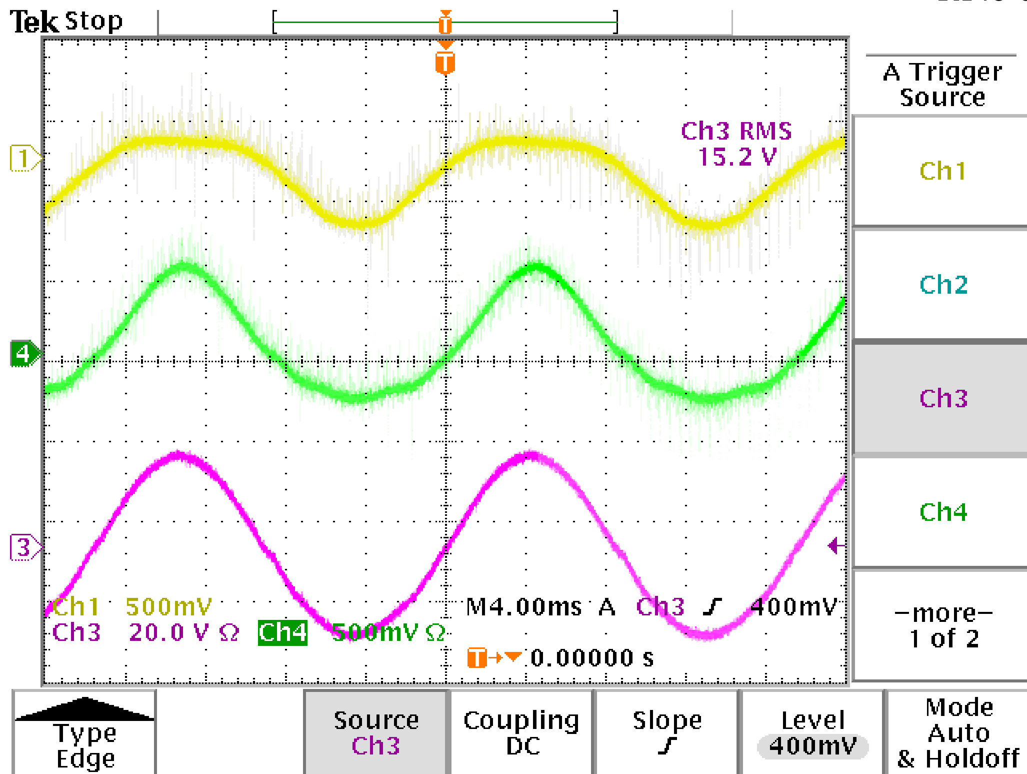


Figure 6.7-22: Trying to compensate using both error adjustments (DC)

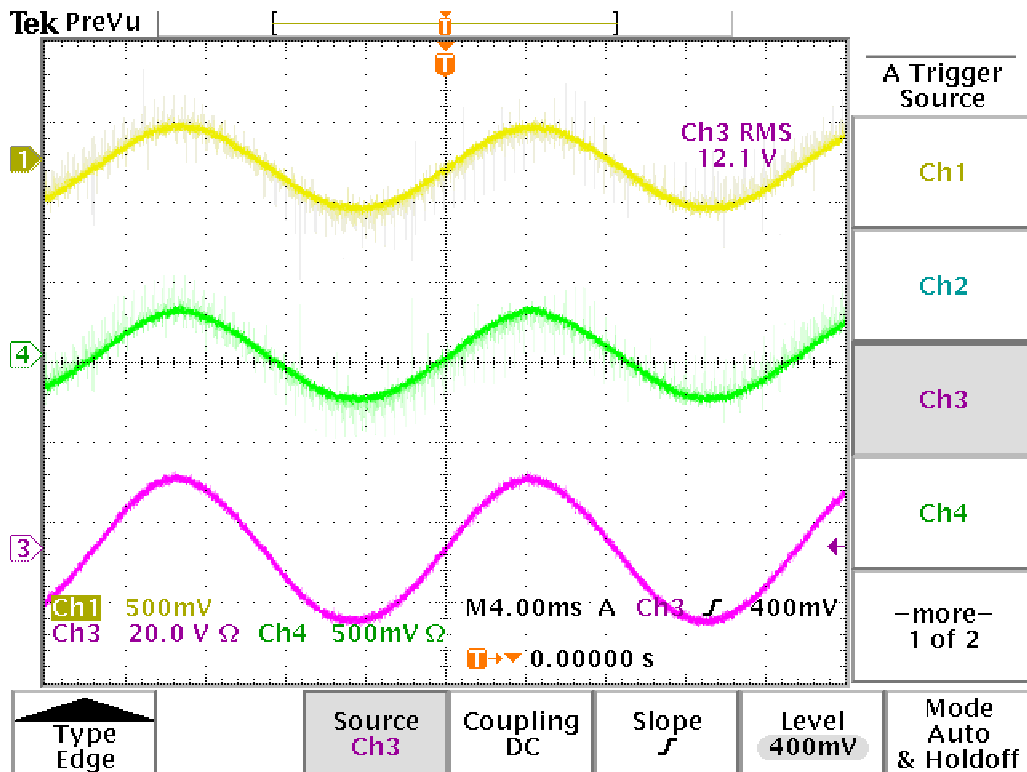


Figure 6.7-23: Using P error based controller.

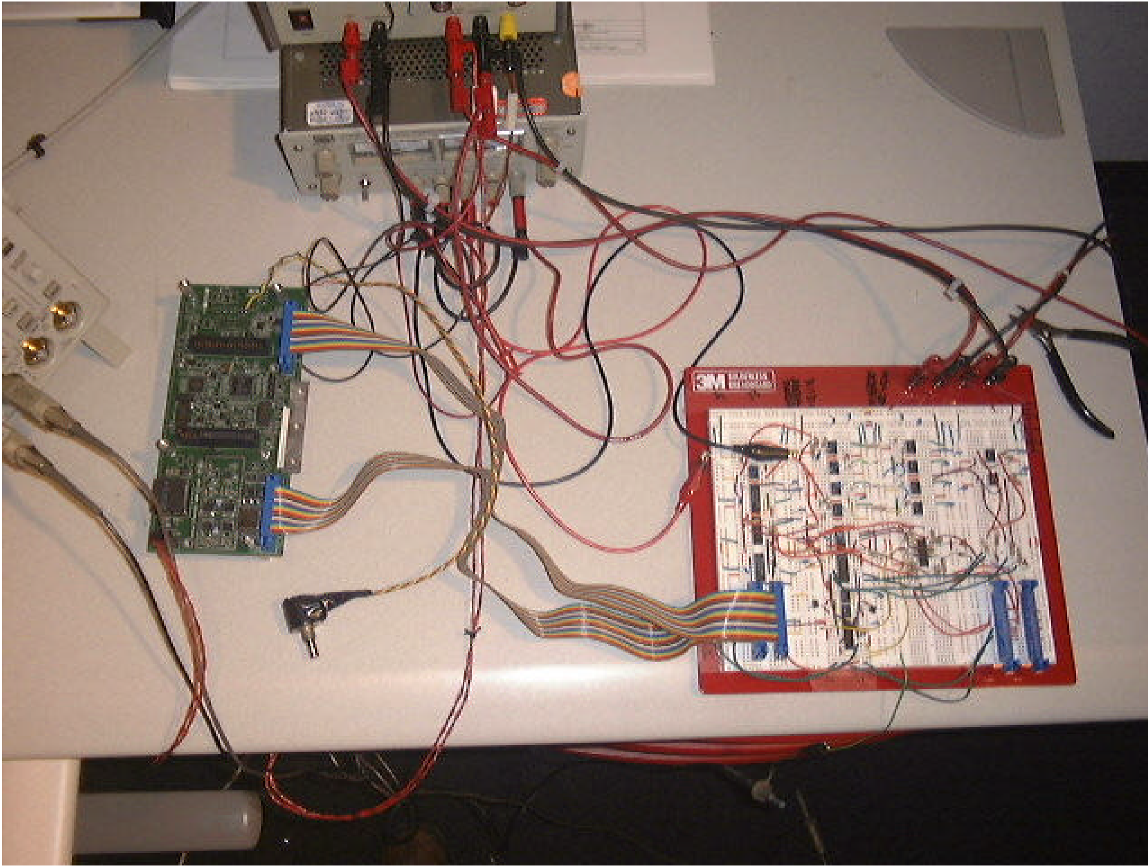


Figure 6.7-24: HEV controller and Delay Circuit Board (Open loop)

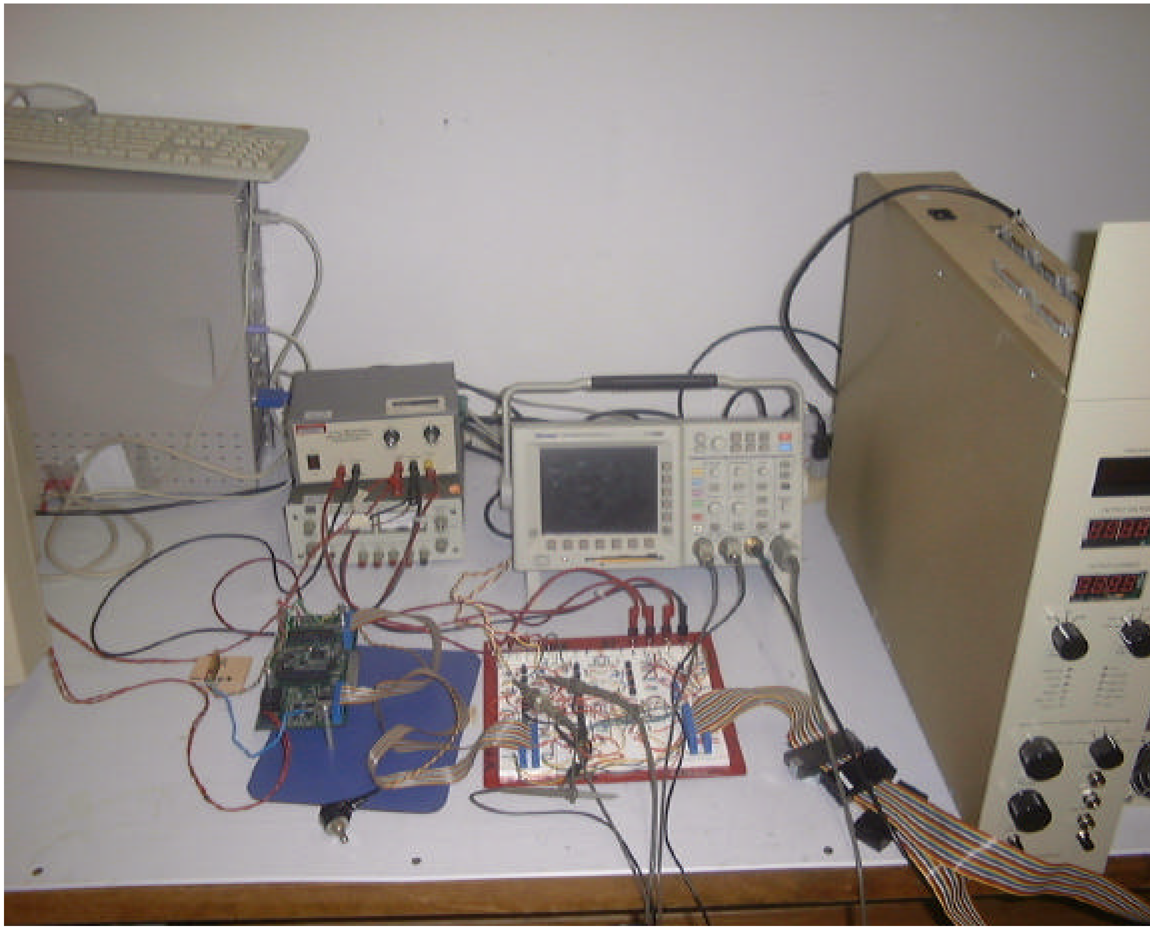


Figure 6.7-25: Control Circuitry

Figure 6.7-26: Parallel PM10s, DC power supply, and Small Load

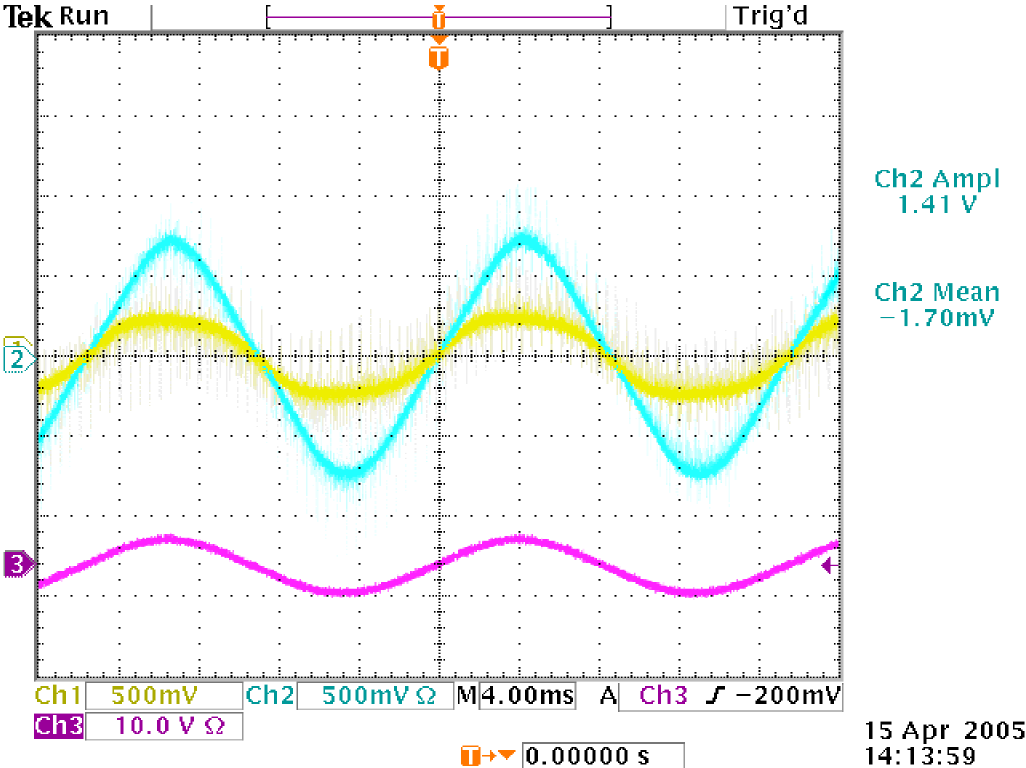


Figure 6.7-27: 50V, 2.8A with no delay control

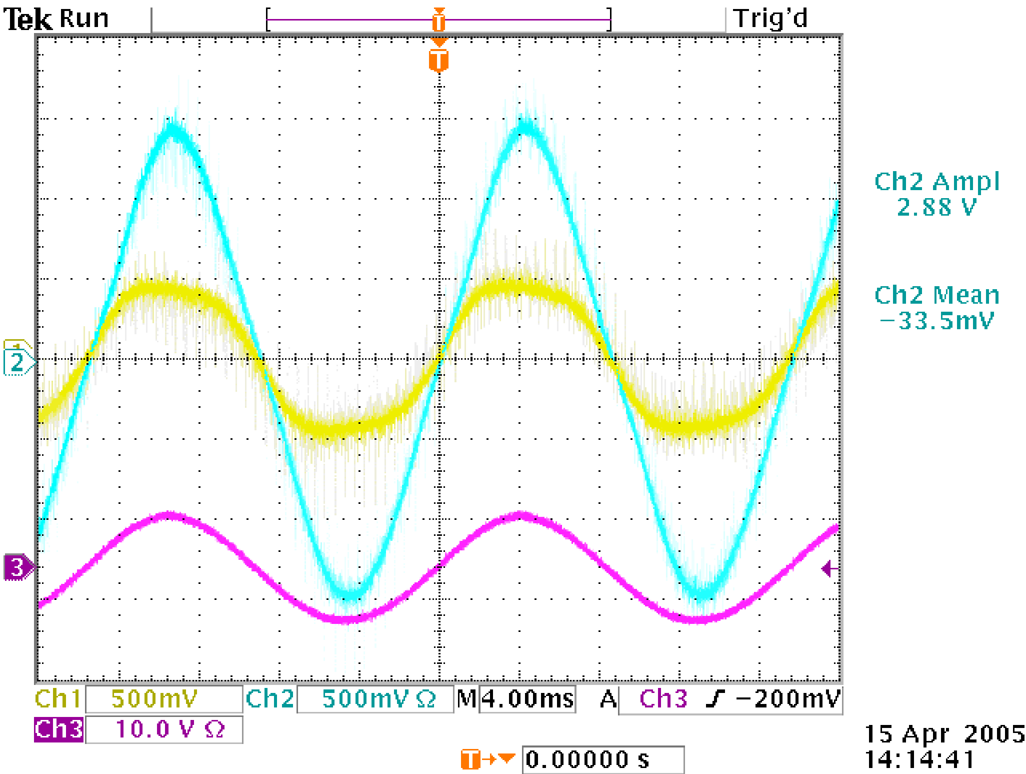


Figure 6.7-28: 100V 5.5A, with no delay control

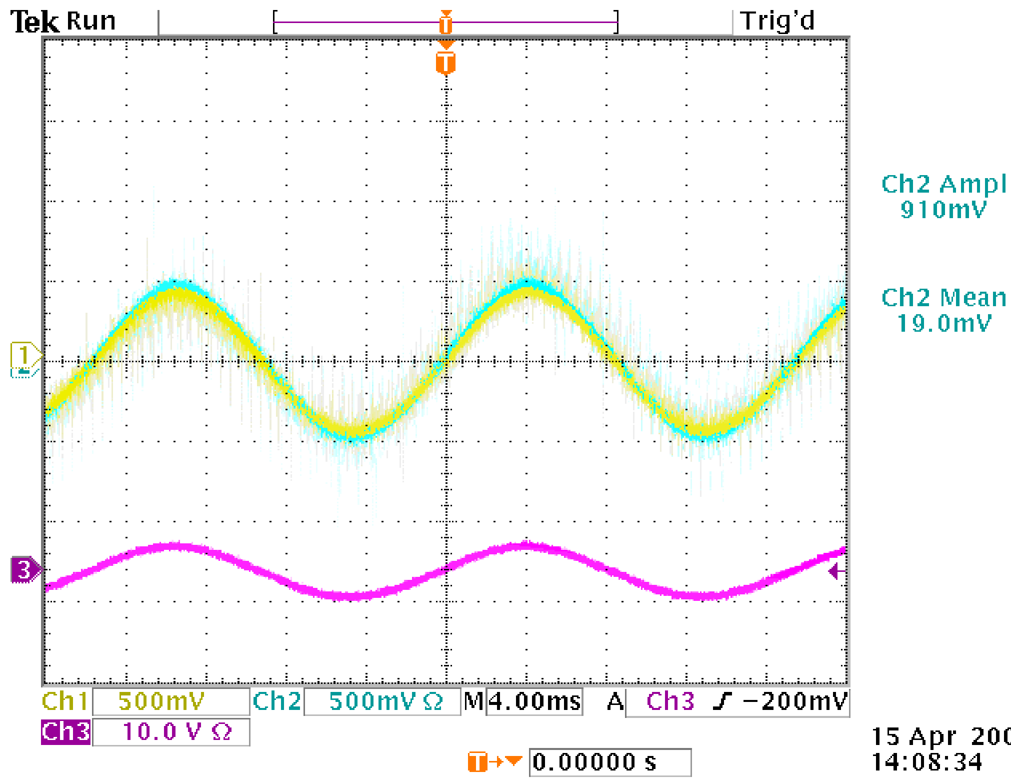


Figure 6.7-29: 50V, 2.8A, P Control

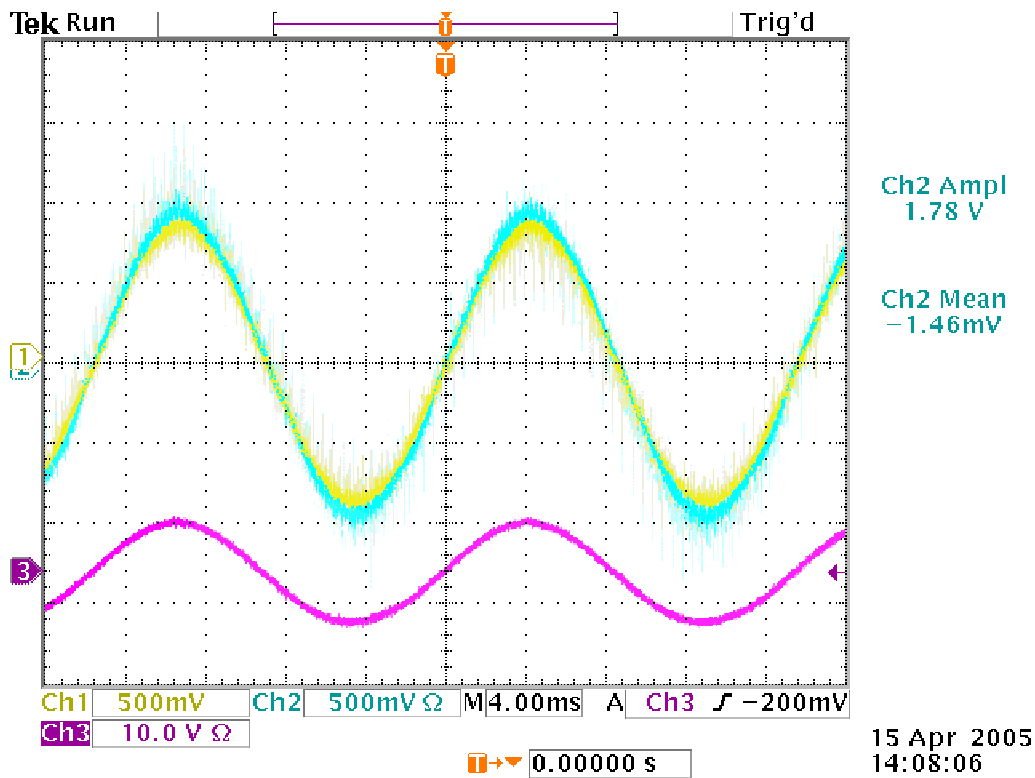


Figure 6.7-30: 100V, 5.5A, P Control

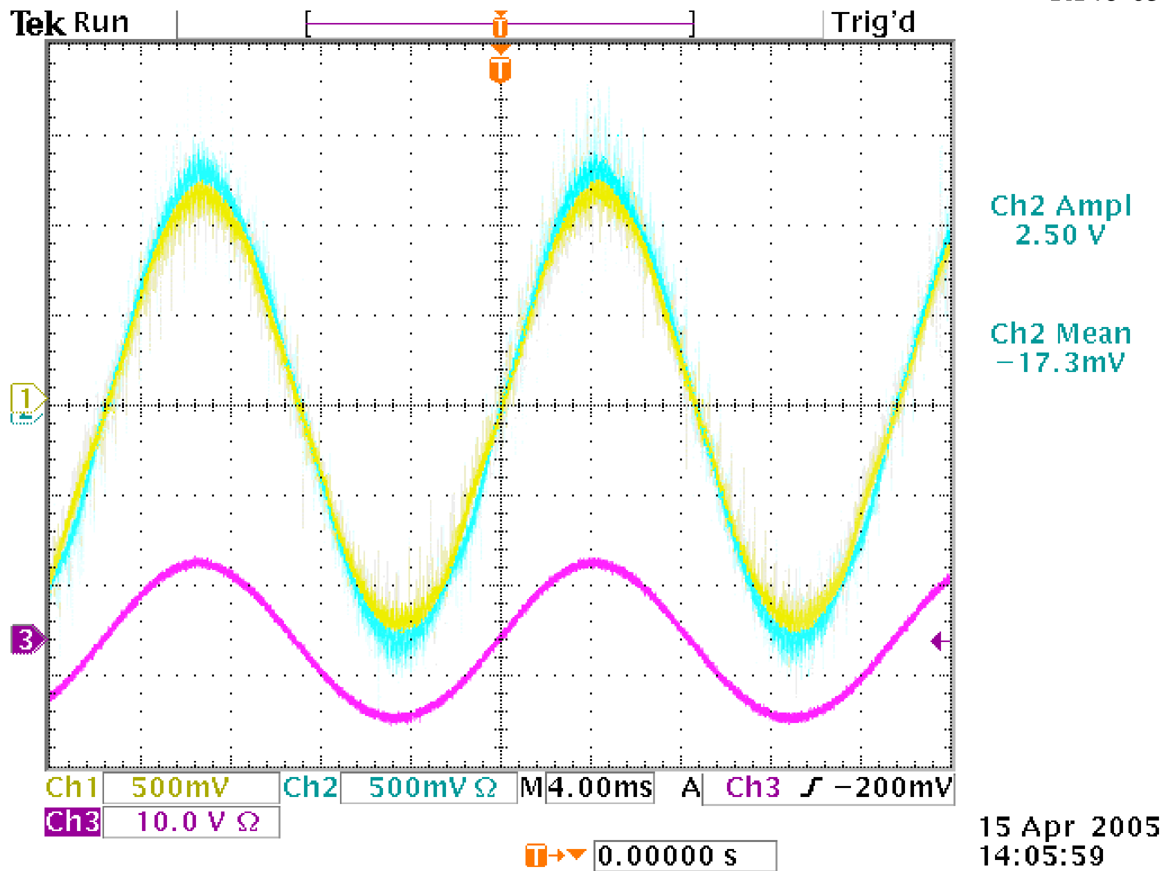


Figure 6.7-31: 140V, 7.5A, P Control

6.8. Summary:

The goal of this project is to advance key technologies to reduce size, weight and cost while enhancing performance and reliability of Modular Inverter Product for Distributed Energy Resources (DER). Efforts address technology development to meet technical needs of DER market protection, isolation, reliability, and quality.

Program activities build on SatCon Technology Corporation inverter experience (e.g., AIPM, Starsine, PowerGate) for Photovoltaic, Fuel Cell, Energy Storage applications. Efforts were divided in to the following four technical areas:

1) Capacitors
2) Cooling
3) Voltage Sensing
4) Control of Parallel Inverters

Capacitors

As originally envisioned, this task involved the manufacturing and testing of a modified electrolytic capacitor by increasing terminals from 2 to 4 to provide DC Bus capacitance, with improved performance and without increasing cost. Capacitor OEM suppliers saw no immediate market for 4-terminal cap and our analysis work has shown that the planned modifications will not result in sufficient improvements in parasitic equivalent series inductance (ESL) and

resistance (ESR) to meet performance objectives; mixes of electrolytic and inherently low loss capacitor types are necessary. As a result, this objective was modified, substituting a redesign of the module bus work to provide for the configuration of low loss capacitors. This change met the top-level objectives of the task and resulted in the demonstration, by fabrication and testing, of a significantly improved inverter. The proposed change did not change the project amount or period of performance. An AIPM unit hybrid bus capacitor configuration was design, built and tested yielding a 2+ % *h (efficiency)* improvement (5+ % *h* at peak power) and switching transient reduction from130 V to 80V , HF reduction in device stress (should permit another 1+% *h*).

Cooling

The objective of the air-cooling area is to eliminate the need for liquid cooling and to demonstrate the resulting performance using our AIPM module. This was implemented using an Augmented Surface, Bonded, Fin heat sink in our AIPM, as a direct substitute to our liquid cooled, internally finned, rectangular cross-section copper tube cold plate. This design eliminates the need for a radiator, pump, coolant and associated plumbing, thereby resulting in an overall cost, weight, and space savings at the higher assembly level. An optimized "augmented surface bonded fin heat-sink" was found for the AIPM application. Based on the optimized geometry and commercially viable heat sinks, a COTS heat sink as close to the optimal as possible was identified, purchased, integrated and thermally tested, verifying the predicted performance was conservative.

The *goal* of maintaining a peak power output of at least 35 to 40 kW and without increasing the module footprint with air-cooling, was not reached due to lower efficiency and corresponding higher than proposed losses in the AIPM. A steady state operating limit of 20 kW at low voltage and 25 kW at high voltage is recommended, based on thermal constraints. Heat sink and cooling fans increased the height of the AIPM by 2.8 inches, resulting in a change in over all height from 5.44 to 8.25 inches. The weight increased from 16 ½ to 19 ½ Lbs, of which 1.8 Lbs are due to the fans. However, the total system weight impact must also consider the elimination of the radiator, pump, fluid and hose weights.

Voltage Sensing

The voltage sensing efforts enabled adaptation of HEV-size power conversion devices to DG applications with an upgrade to the architecture of the voltage sensing system. Standalone HEV-style inverters do not include galvanic isolation of the voltage sensors. Also, phase measurements can be made from the simple DC link voltage reference. SatCon developed and demonstrated modifications to HEV-style modules that enable voltage and phase sensing systems suitable for DG application providing:

- Better handling of asymmetric loads
- Improved noise immunity
- Better power-to-control isolation

A single sensor board, with multiple configurations was designed to meet application specific needs. Three specific board configurations were tested and all three boards showed:

- Comparable DC offsets over operating ranges (within 100mV).
- Voltage and current measurements were accurate (within 200 mV).

- Testing showed measurements were within 5% of each other at tested power levels

Therefore, the new voltage sensor boards are drop-in-compatible with the previous boards, yielding improved functionality in same volume/cost and enabling UL1741 (IEEE 1547, NEC) DER applications by providing power-control isolation

Control of Parallel Inverters

The main reasons for paralleling of modules and switching devices are reliability and cost. The goal of the control area was to establish a reliable and realizable technique to control individual inverters without a need for existence of a communication link. There are numerous communication-less techniques described in literature treating problem of paralleling that we considered in this program. All of these techniques share a common approach: they emulate the synchronous machine. The control, therefore, is based on voltage and frequency droop, reactive and active power deviation, or current feed forwarding. The major deficiency of these methods is poor performance at transient conditions, inadequate sharing of nonlinear loads, and quite substantial output voltage deviations with the load levels. Additionally, the discrepancy between the individual switches/modules in terms of their characteristics as well as cooling conditions may necessitate their intentional operation below current normal ratings. The objective of this area was to provide a mechanism enforcing the current to be balanced (or intentionally unbalanced) between the modules. SatCon Applied Technology developed a proprietary "smart driver" technique in a course of this program. It provides a mean to balance the current in the paralleled modules or devices by conditioning the gate signals. The technique is universal and could be extended to use in conjunction with equalization of individual devices/modules temperature balance. Both static and dynamic current sharing was achieved by introducing a delay to the individual PWM gate pulses. The load currents were shared with a high level of accuracy for any type of load: from linear resistive through linear inductive to nonlinear. It is a simple yet powerful method for paralleling both individual devices and modules that can be built into conventional gate drivers without a need of integration with existing individual controllers. This technique dramatically improves reliability and fault tolerance of power systems built of paralleled inverters. A patent application has been made based on this technology.

5.9 Conclusions:

- Powerful new approach
- Robust correction for imbalance
- Matches modules operating as voltage sources without droop
- Relatively simple, needs to be integrated into gate drive circuitry

Appendix A consists of a number of slides of a Power Point Presentation that was presented as a summary of this report

7. Program Achievements

The achievements of the activities performed under this contract are summarized as follows:

•Capacitors

–Hybrid 2+ % *h (efficiency)* improvement (5+ % *h* at peak power)

–HF, reduction in device stress (should permit another 1+% *h)*

•Cooling

–Successful operation with forced air convection cooling using integrated finned heat sink

–20kW Operation with 59°C Ambient Air

•Sensing

–Improved Functionality in same volume/cost

–Enables UL1741 (IEEE 1547, NEC) DER applications

•Control/Paralleling

–New powerful Technique

–Robust correction for imbalance

–Matches modules operating as voltage sources without droop

–Relatively simple, needs to be integrated into gate drive circuitry

8. Future

• Capacitors

–Hybrid Optimization for Applications, analytic tools for tradeoffs

–Integrated Packaging:

- •Co-fire ceramic into Bus work
- •Package hf cap inside IGBT package
- •Package snubber (true snubber) with IGBT
- •Evaluate negative inductance from filter configuration to cancel capacitor ESL
- •Structural capacitors

• Cooling

–Heat Sinks Optimized for Higher Operating Temperature

–Packaging for larger Delta T and higher T

- •MMC
- •Graphite Copper

•Sensing

–Board Modifications for Improved Manufacturability

–Investigate further purely optical techniques

•Control/Paralleling

–Further refinement, verification, expansion, full-system studies

–I.C. implementation for low-cost

–Apply to PM10 (and other) modular building block amplifiers

Appendix A

Final Presentation

SatCon Technology Corporation

Breaking Barriers to Low-Cost Modular Inverter Production & Use

DE-FC26-04NT41979

SatCon Technology Corporation
27 Drydock Ave.
Boston, Massachusetts 02210

Agenda

10:30	Video Conference Setup	L. Alvarez & J. Foshage
10:50	Program Overview	J. Foshage & L. Casey
11:00	Air Cooling	J. Foshage
11:30	Voltage Sensing	J. Parkinson
11:45	Advanced Controls	B. Borowy
12:15	Capacitor	L. Casey
12:30	Smart Gate Drive	L. Casey
1:00	Wrap Up Discussions	A. Yocum & J. Foshage

SatCon Technology Corporation

Air Cooling

Jerry Foshage

Air Cooling

Objective:

To replace liquid cooling in AIPM DC to DC Converter with Forced Air, Convection Cooling

Tasks include:

- Requirement Definition
- Heat Sink Optimization
- Thermal Analysis
- COTS Hardware Identification
- Performance Test

Air Cooling

Requirement Derivation From Proposal Graph and Assumed Heat Sink Vendor Data Sheet

Air Cooling

Thermal Lumped Parameter Analysis of Sink Thermal Resistance

1

Air Cooling

Air Cooling

Air Cooling

Air Cooling

AAVID COTS HEAT SINK

Air Cooling

AAVID COTS HEAT SINK

Air Cooling

COTS AUGMENTED, IMPINGMENT FLOW, BONDED HEAT SINKS vs OPTIMIZED HEAT SINK

o

Air Cooling

Steady State Junction Temperature vs. Heat Sink Thermal Resistance

Air Cooling

AAVID P/N 27441 COTS AUGMENTED, BONDED FIN HEAT SINK vs LIQUID COOLING COLD PLATE

Air Cooling

Fan Selection & Ratings

2 Fans in a Impingement Flow Configuration, each with:

- 201 cfm Air Flow
- 24 V – 36 Watt
- 5100 RPM
- 119 mm Square x 38.4 mm
- 0.9 Lbs
- Brushless DC with Ball Bearings
- Plastic Impeller - Aluminum Venturi

Air Cooling

HEAT SINK INTERFACE COMPARISON

APM IGBTs

Air Cooled Heat Sink

Water Cooled Heat Sink

Air Cooling

APM LIQUID AND AIR COOLING CONFIGURATION TESTING

Air Cooling

Thermal Test History

Power Levels:

Air Cooling

Thermal Testing Results Summary

[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
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						[illegible]	[illegible]

Air Cooling

Summary:

- AIPM DC to DC Converter Liquid cooling was successfully replaced with Forced Air, Convection Cooling
- COTS Heat Sink Identified that is quite close to optimum
- Air Heat Sink Performed Better Than Analyses Predicted
- Recommend 20 KW Operation Over Full Voltage Range to Stay within Thermal Limit
- Higher operating temperature of SiC technology would enable use of 0.5" folded fin, but will require ducting.

SatCon Technology Corporation

Isolated Voltage Sensing

Jim Perkinson

Isolated Voltage Sensing

Strategic Goal: Low cost power inverter for a broad market

To adapt SatCon's AIPM inverter module, designed for HEV's, to DG applications.

- Provide 1.5kV Galvanic Isolation between controller and power
- Provide for Zero Sequence Measurements

Design Considerations:

- Maintain high temperature rated parts and design.
- Maintain low cost

Isolated Voltage Sensing

Investigation into **Galvanic Isolation**:

Methods of Galvanic Isolation: Magnetic, Capacitive, Optical

Cost was the driving factor, as adding any isolated component that was rated for Automotive temperatures was prohibitively expensive.

Solution: redesign the Sensor Interface Board, a sub-assembly of the AIPM. The new design will have dual use functionality.

In one configuration, the SIB will have high temperature and no galvanic isolation

In a second configuration, the SIB will have commercial temperature and galvanic isolation

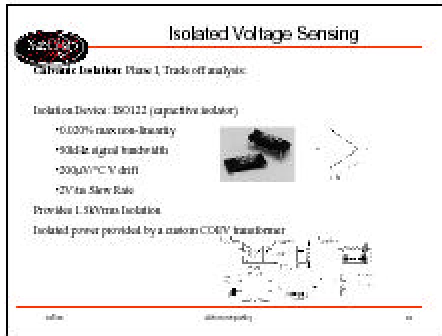
Isolated Voltage Sensing

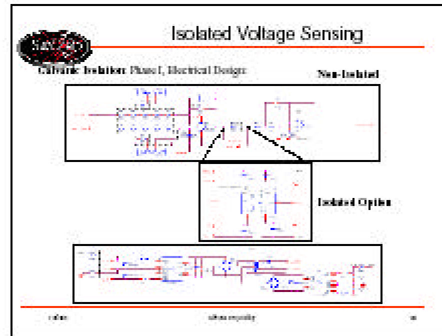
Galvanic Isolation Phase I, Trade off analysis:

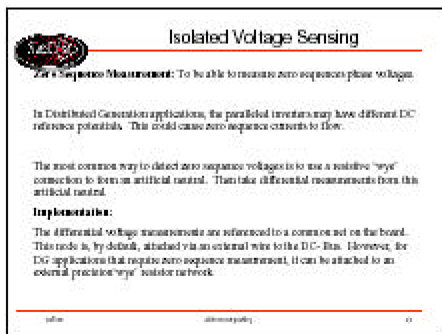
Sensor Interface Board Functionality Overview:

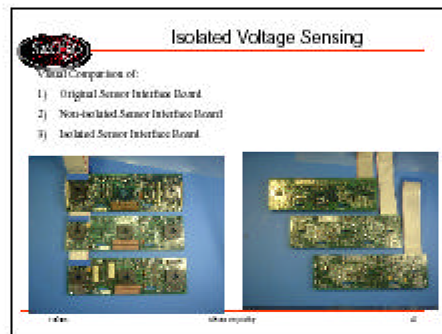
- 3 AC phase voltage measurements (Referenced to DC GND), High Impedance
- 1 DC Voltage measurement (Referenced to DC GND), High Impedance
- 3 AC Current voltage measurements (LEM- Magnetically Isolated)
- DC Voltage Discharge (Optically isolated)

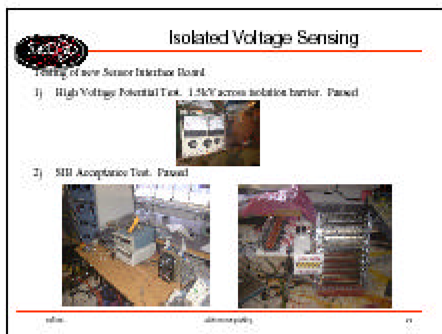
Wish to add isolation to 4 voltage measurements

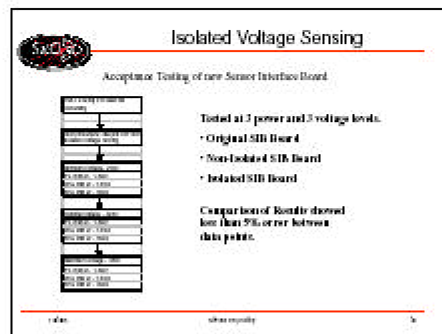

Isolated Voltage Sensing
Galvanic Isolation: Phase I, Trade off analysis:
Isolation Device: ISO122 (capacitive isolator)
•0.020% max non-linearity
•50kHz signal bandwidth
•200μV/°C V drift
•2V/us Slew Rate
Provides 1.5kVrms Isolation
Isolated power provided by a custom COTV transformer


Isolated Voltage Sensing
Galvanic Isolation: Phase I, Electrical Design:
Non-Isolated
Isolated Option


Isolated Voltage Sensing
Zero Sequence Measurement: To be able to measure zero sequence phase voltages.
In Distributed Generation applications, the paralleled inverters may have different DC reference potentials. This could cause zero sequence currents to flow.
The most common way to detect zero sequence voltages is to use a resistive "wye" connection to form an artificial neutral. Then take differential measurements from this artificial neutral.
Implementation:
The differential voltage measurements are referenced to a common net on the board. This node is, by default, attached via an external wire to the DC- Bus. However, for DG applications that require zero sequence measurement, it can be attached to an external precision "wye" resistor network.


Isolated Voltage Sensing
Visual Comparison of:
1) Original Sensor Interface Board
2) Non-Isolated Sensor Interface Board
3) Isolated Sensor Interface Board


Isolated Voltage Sensing
Testing of new Sensor Interface Board
1) High Voltage Potential Test. 1.5kV across isolation barrier. Passed
2) SIB Acceptance Test. Passed


Isolated Voltage Sensing
Acceptance Testing of new Sensor Interface Board
Tested at 3 power and 3 voltage levels.
• Original SIB Board
• Non-Isolated SIB Board
• Isolated SIB Board
Comparison of Results showed less than 5% error between data points.

Isolated Voltage Sensing

Summary:

- Selected a cost effective method for providing Galvanic isolation
- Selected a means for zero sequence measurement
- Implemented both in a 'drop in replacement board for the AIPM
- Verified the design through acceptance testing

DC Bus Capacitance

- Three Distinct Functions
  - Energy Storage
  - Ripple Current
  - Switching Transient Bypass
- Three Distinct Time Scales
  - DC – Fundamental (or harmonic of for imbalance)
  - Switching Period
  - Transition Time
- Three distinct Manufacturing, Packaging Technologies, and three distinct Costs ($/uF)

Electrolytic Life Compromise System Cost

Electrolytics cheap but

- Short lived
- Poor Parasitics

Good BUS Capacitor is Hybrid, and is Distributed

Migrate some of the high frequency capacitor to the switch

Rule of Thumb

Typically 100:1 ratio between T and t_{sw}

Parasitic Inductance – Current Commutation

$V_{CE} = L_s \, di/dt$

Commutation between IGBT1 and D2 (IGBT2 ↔ D1)

L_s is the Loop Inductance (20nH of which is in present Eupec package)

$L_s I^2$ lost every switching cycle, turn-on and turn-off

Typical Loop Inductance -- L_s

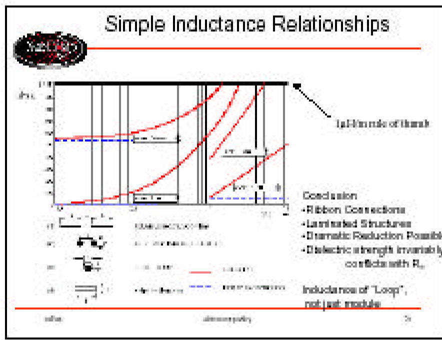
I 400 A/div (green)

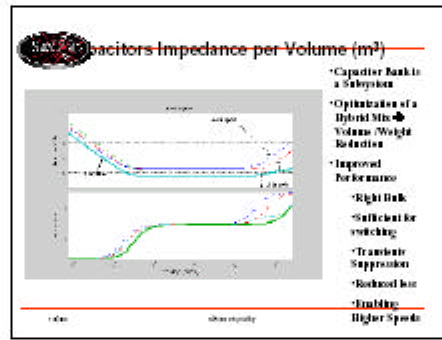
V 200 V/div (black)

At zero crossing have ? V = 230V

di/dt = 3200A/800nS

➔ L_s = 58nH (typically 1/3 module, 1/3 interconnect, 1/3 capacitor)





Capacitor Bank Requirements

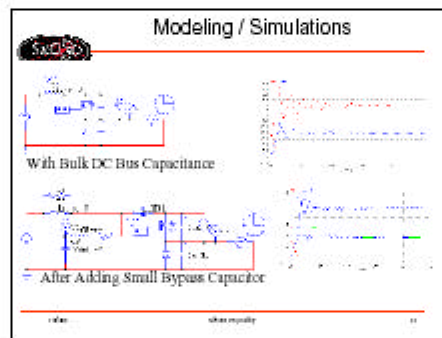
2010 Typical Capacitor Bank Requirements	
Capacitance, µF	2800+/-10%
Voltage rating, VDC	440
Peak transient voltage for 50 ms	600
Leakage current at rated voltage, mA	1
Dissipation factor, %	<1
ESR, mohm	<3
ESL, nH	<20
Ripple current, amp rms	250
Temperature range of ambient air, °C	-40 to +140
Weight requirement, kg	10.8
Volume requirement, l	0.4
Cost	$90
Failure mode	Benign
Life @80% rated voltage	>10,000 hr, 20 amps rms, +85°C

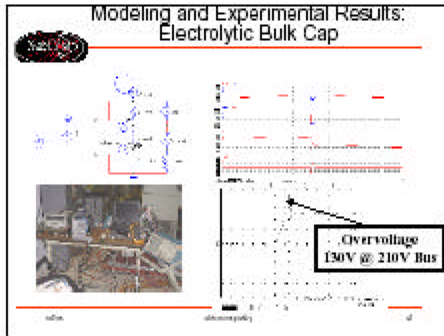
Qualitative Comparison

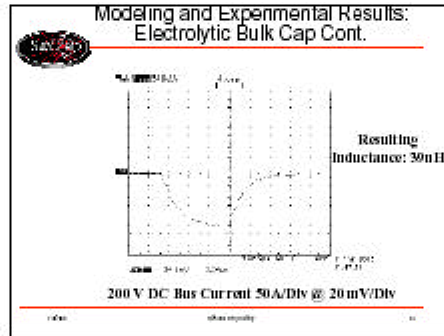
	Electrolytic	Polymer Film	Ceramic
Size, Weight	Poor	Good	Excellent
ESR	Marginal	Excellent	Excellent
Temp. Stability	Marginal	Good	Excellent
Reliability	Marginal	Excellent	Excellent
Ripple Current	Marginal	Good	Excellent
Failure Mode	Poor	Excellent	To be demonstrated
Cost	Excellent	Good	Poor

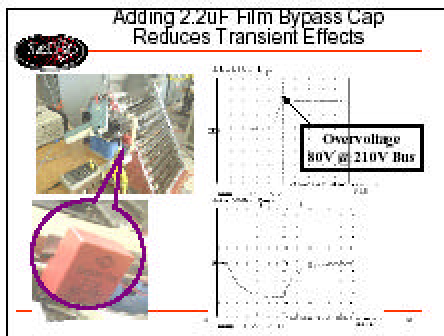
If Ceramics Are So Great, why They're Not Commonly Used?

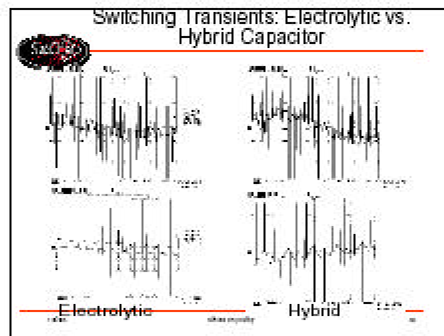
- Mechanical Challenges
  - Brittle
  - Not Easily Fabricated as Large Storage Elements
- Current Effort to Overcome these Issues Lies in Material Selection:
  - ferroelectric materials
  - antiferroelectric/ferroelectric phase-switch ceramics
  - glass ceramics











Advanced Controls -- Paralleling

- Flexibility
- Total Power Availability
- Reliability
- Expandability
- Modularity

} System Cost

Ideally – One Standard Building Block for All Systems

Desired Features of Paralleling

- No communication between units
- Load shared according to:
  - Module ratings
  - Module temperature
  - Module functionality
- Voltage @ Point of Interconnection is the only common source of information

Types of Paralleled Systems: Grid Tied

- Current Controlled Utility Interconnected Inverter
- VSI Operating with Utility Line

Stand Alone Systems

- Approaches
  - Emulation of parallel synchronous machines
    - Limited frequency variations due to inertia
    - Presence of synchronizing torque keeps them in synch
    - ΔP ~ Δf: Change in power ⇔ Change in frequency
    - ΔQ ~ΔV: Change in React. Power ⇔ Change in Voltage
- Techniques
  - Voltage and Frequency Droop
  - Power Deviation Control
  - Current Feedforward

Stand Alone Systems -- Control Overview

Voltage and Frequency Droop

Power Deviation

Current FeedForward

Ideally – Would Parallel Identical Voltage Sources

Ideally
- Same gain (A)
- No offset, linear
- No Impedance
  - No loss
  - Not required

But, Nothing is Ideal or Identical

Ideally
- Same gain, A
- No offset
- No Impedance
  - No loss
  - Not required

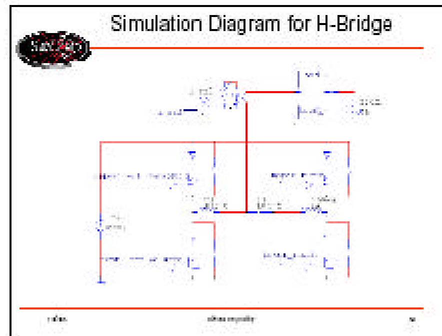
Gain, Offset, Nonlinearities, ...

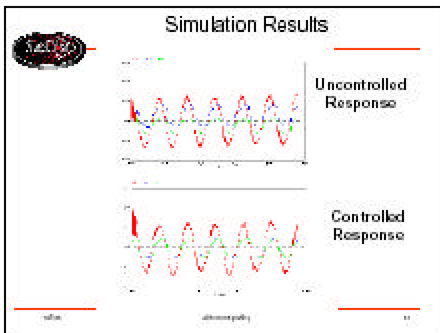
Reality
- Mismatches

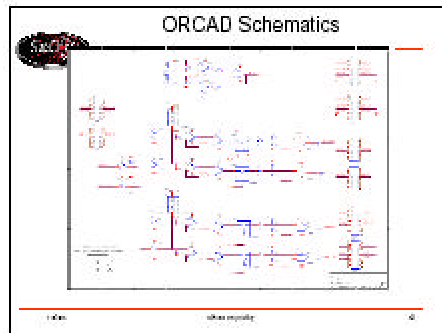
Consequence
- Imbalance
- Oscillation

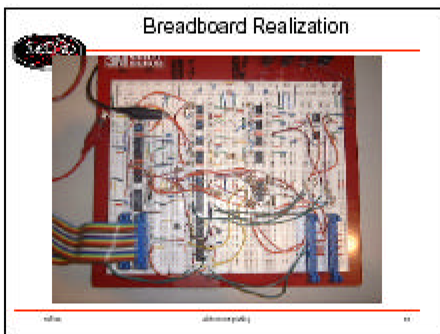
Switch Balancing Paradigm

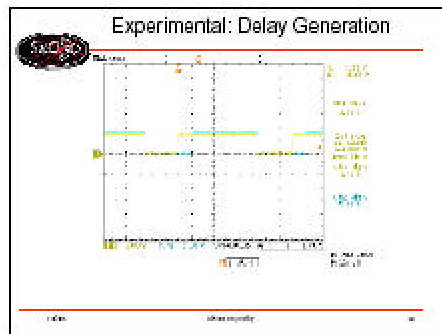
- Fundamental Principle:
  - Balance or intentional imbalance among switches
  - Control is done on a Pulse-by-Pulse basis (deadbeat)
- Incremental Delays Control Local (Micro) and Global (Macroscopic) Imbalances

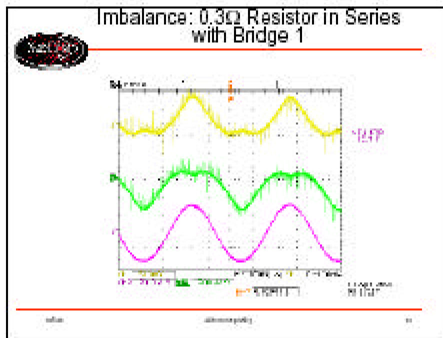


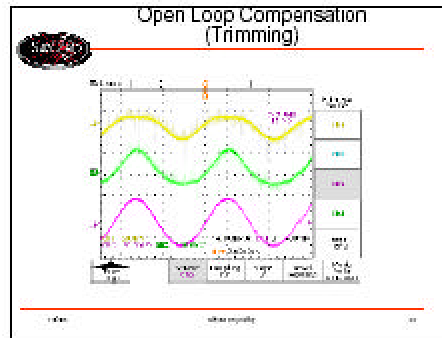


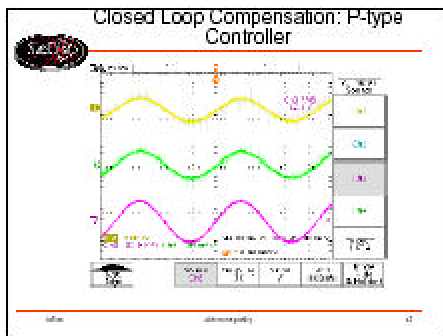


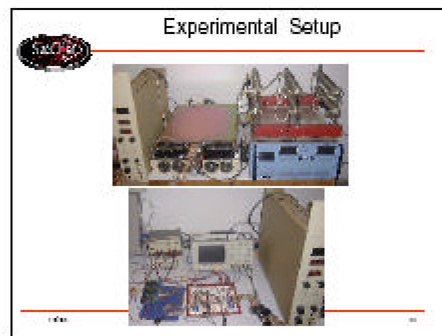


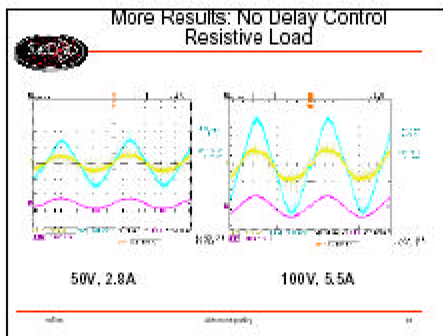


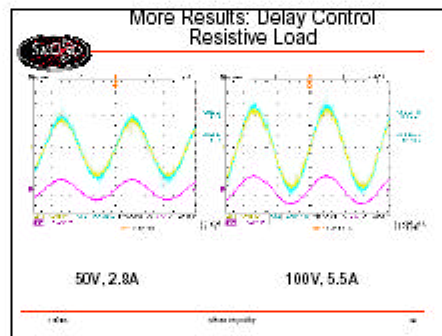

Imbalance: 0.3Ω Resistor in Series
with Bridge 1


Open Loop Compensation
(Trimming)


Closed Loop Compensation: P-type
Controller


Experimental Setup


More Results: No Delay Control
Resistive Load
50V, 2.8A
100V, 5.5A


More Results: Delay Control
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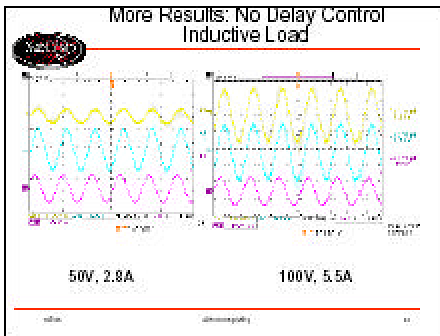
50V, 2.8A
100V, 5.5A



Switch Balancing → New Approach in Paralleling

- Use of Pulse-by-Pulse Control
- Non-Linear Control – Fast Transient Response
- The Load Characteristics (Inductive, Resistive, Linear, Non-Linear) – nearly outside of interest
- Exceptionally effective at achieving Balance

Conclusion

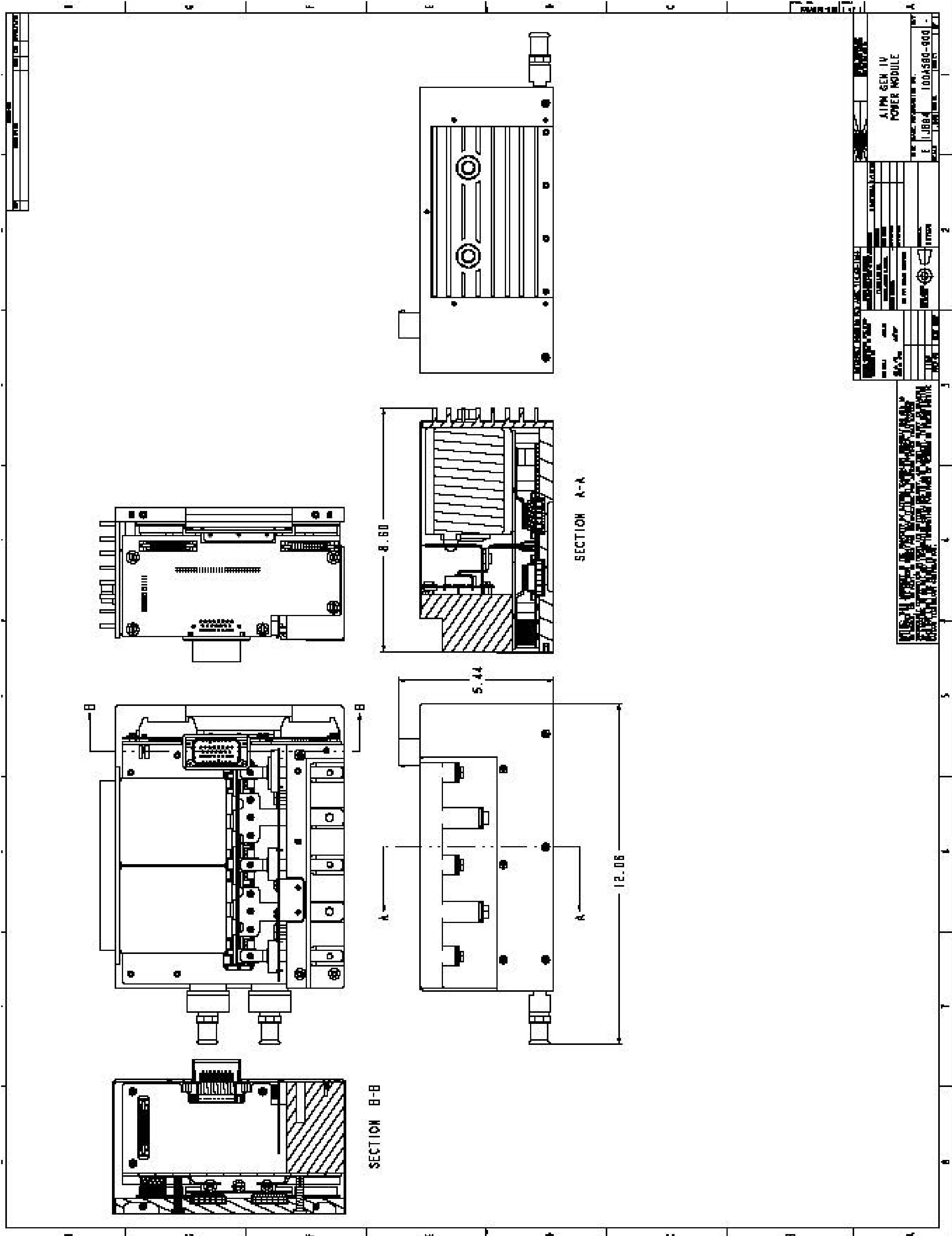
- Powerful new approach
- Robust correction for imbalance
- Matches modules operating as voltage sources without droop
- Relatively simple, needs to be integrated into gate drive circuitry

Program Achievements

- Cooling
  - 20kW Operation with 59°C Ambient Air
- Sensing
  - Improved Functionality in same volume/cost
  - Enables UL1741 (IEEE 1547, NEC) DER applications
- Capacitors
  - Hybrid, requires tradeoff and distribution
- Control/Paralleling
  - New Technique

Appendix B

Baseline AIPM Liquid Cooled Cold Plate and Modified AIPM Air Cooled Heat Sink Layout Drawings


AIPM GEN IV
POWER MODULE
SECTION A-A
SECTION B-B
8.60
5.44
12.08

ASSEMBLY, AIR COOLED