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# Soft-Core Processor Study for Node-Based Architectures

Daniel E. Gallegos, Benjamin J. Welch, Jason J. Jarosz, Jonathan R. Van Houten, and Mark W. Learn

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## ABSTRACT

Node-based architecture (NBA) designs for future satellite projects hold the promise of decreasing system development time and costs, size, weight, and power and positioning the laboratory to address other emerging mission opportunities quickly. Reconfigurable Field Programmable Gate Array (FPGA) based modules will comprise the core of several of the NBA nodes. Microprocessing capabilities will be necessary with varying degrees of mission-specific performance requirements on these nodes. To enable the flexibility of these reconfigurable nodes, it is advantageous to incorporate the microprocessor into the FPGA itself, either as a hard-core processor built into the FPGA or as a soft-core processor built out of FPGA elements. This document describes the evaluation of three reconfigurable FPGA based processors for use in future NBA systems – two soft cores (MicroBlaze and non-fault-tolerant LEON) and one hard core (PowerPC 405). Two standard performance benchmark applications were developed for each processor. The first, Dhrystone, is a fixed-point operation metric. The second, Whetstone, is a floating-point operation metric. Several trials were run at varying code locations, loop counts, processor speeds, and cache configurations. FPGA resource utilization was recorded for each configuration. Cache configurations impacted the results greatly; for optimal processor efficiency it is necessary to enable caches on the processors. Processor caches carry a penalty; cache error mitigation is necessary when operating in a radiation environment.

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# ACRONYMS

| | |
|---|---|
| ASIC | application-specific integrated circuit |
| BRAM | Block RAM |
| COTS | commercial off-the-shelf |
| CPU | central processing unit |
| DCM | Digital Clock Manager |
| DSP | digital signal processing |
| EDAC | error detection and correction |
| EDK | Embedded Development Kit |
| FPGA | Field Programmable Gate Array |
| FPU | floating-point unit |
| GUI | graphical user interface |
| HDL | hardware description language |
| IP | intellectual property |
| JTAG | Joint Test Action Group |
| LMB | Local Memory Bus |
| LUT | lookup table |
| MHS | Microprocessor Hardware Specification |
| MMU | memory management unit |
| MSS | Microprocessor Software Specification |
| OCM | on-chip memory controller |
| OPB | on-chip peripheral bus |
| NBA | node-based architecture |
| PPC | PowerPC |
| RAM | random access memory |
| ROM | read-only memory |
| SDRAM | synchronous dynamic random access memory |
| SEE | single-event effect |
| SEFI | single-event functional interrupt |

| | |
|---|---|
| SEU | single-event upset |
| SIRF | SEU Immune Reconfigurable FPGA |
| SNL | Sandia National Laboratories |
| SRAM | Static Random Access Memory |
| | |
| TMR | triple mode redundancy |
| | |
| UART | Universal Asynchronous Receiver/Transmitter |
| | |
| XPS | Xilinx Platform Studio |
| XRTC | Xilinx Radiation Test Consortium |

# EXECUTIVE SUMMARY


Node-based architecture (NBA) designs for future satellite projects hold the promise of decreasing system development time and costs, size, weight, and power, and, through its reconfigurable nature, being able to position the laboratory to address other emerging mission opportunities quickly.

Reconfigurable Field Programmable Gate Array (FPGA) based modules will comprise the core of several of the NBA nodes identified in the “Future NDS Architecture Description” document. Microprocessing capabilities will be necessary with varying degrees of mission-specific performance requirements on these nodes. To enable the flexibility of these reconfigurable nodes, it is advantageous to incorporate the microprocessor into the FPGA itself, either as a hard-core processor built into the FPGA or as a soft-core processor built out of FPGA elements.

The reconfigurable FPGA targeted for the NBA is the Xilinx SEU Immune Reconfigurable FPGA (SIRF) device, a radiation-hardened by design Static Random Access Memory (SRAM) device based on the commercial off-the-shelf (COTS) Xilinx Virtex-5 FX130T. The SIRF device is still currently under development but is expected to be available in the first quarter of 2010. NBA developers can begin designing now with the COTS equivalent and then incorporate the SIRF device into their designs when it becomes available.

Currently the SIRF development effort is targeted to eliminate the device configuration errors that upset Xilinx SRAM-based FPGAs when operated in radiation environments. **The characterization of SIRF device internal building blocks such as Memory Resources (Block RAMs), Logic Resources (Slices, Logic Cells, CLB Flip-Flops), Clock Resources (DCM, PLL), and Embedded Hard Intellectual Property Resources (DSP48E slices, PowerPC (PPC) 440 processor, RocketIO Transceivers) in radiation environments will provide designers with the information needed to develop a mitigation strategy at the device level based on the target mission (orbit).**

Three different FPGA-based processors (two soft core and one hard core) were evaluated on the Xilinx Virtex-4FX FPGA because Virtex-5 FXT devices were not available at the onset of the study. Two processors “native” to the Xilinx FPGAs were evaluated, the soft-core MicroBlaze processor and the hard-core PPC405. Processors native to the Xilinx FPGAs are attractive for NBA because of the amount of testing and mitigation that Xilinx and the Xilinx Radiation Test Consortium develop for these processors. In addition, the soft-core LEON3 (non-fault-tolerant) processor was included because of the popularity of the LEON cores in the space processing community and the potential for code and tool reuse if the rad-hard application-specific integrated circuits (ASICs) such as the Atmel AT697E (LEON2 Fault-Tolerant) or the AeroFlex UT699 (LEON3 Fault-Tolerant) devices are used in other NBA modules.

Two standard performance benchmark applications were developed for each processor. The first, Dhrystone, is a fixed-point operation metric. The second, Whetstone, is a floating-point operation metric. Several trials were run at varying code location, loop counts, processor speeds, and cache configurations. FPGA resource utilization was recorded for each configuration.

The MicroBlaze and PPC processors have wider operating ranges than the LEON processor. Surprisingly, more FPGA resources were consumed by the LEON processor than by either of the other two processors. Cache configurations impacted the results greatly – for optimal processor efficiency it is necessary to enable caches on the processors. Processor caches carry a penalty – cache error mitigation is necessary when operating in a radiation environment. The Virtex-4 PPC instruction cache contains an error that does not allow for the graceful mitigation of this resource.

Similar characterizations (with possible optimizations) should be conducted on the COTS Xilinx Virtex-5 FX130T device when it becomes available.

# 1. INTRODUCTION

This document describes the evaluation of three reconfigurable Field Programmable Gate Array (FPGA) based processors for use in future node-based architecture (NBA) systems – two soft cores (MicroBlaze and non-fault-tolerant LEON) and one hard core (PowerPC [PPC] 405).

The Xilinx SIRF (Virtex-5 FX130T) reconfigurable FPGA device that is targeted for NBA is not yet available; Xilinx Virtex-4 FPGAs were used exclusively in this study. MicroBlaze and PPC405 evaluations were conducted on an ML-405 board that contains a Virtex-4 FX20 device. LEON evaluations required the use of a different development board, the ML-410 with a larger Virtex-4 FX60 device because resources consumed by the LEON core. Lessons learned in this study will be directly applicable to developing Virtex-5 processor based systems.

In general: LEON would be good for low-intensity applications; PowerPC and MicroBlaze have wider operating ranges and are better suited for more computationally intensive applications.

LEON processors can be found in radiation-hardened application-specific integrated circuits (ASICs) such as the Atmel AT697E (LEON2 Fault-Tolerant) or the AeroFlex UT699 (LEON3 Fault-Tolerant). It is not yet known whether a fault-tolerant LEON soft core would be fault tolerant in a Xilinx SEU Immune Reconfigurable FPGA (SIRF) device.

Operating systems and how they interact with mitigation schemes were not evaluated as part of this study – they should be included in follow on efforts along with:

- Optimizing the processor hardware designs to minimize FPGA resource utilization. One particular point to investigate is why the LEON processor required so much more FPGA resources than the other two processors; in particular, why did the LEON soft-core processor consume significantly more resources than the soft-core MicroBlaze?
- Exploring low-power modes of the processors.
- Evaluating the PPC440 hard core resident in the Virtex-5 FX devices. (The PPC440 is expected to have higher performance numbers than the PPC405 tested.)
- Measuring the power consumed by the FPGA when configured with an internal hard/ soft core processor.

Xilinx and the Xilinx Radiation Testing Consortium (XRTC) are performing a great deal of mitigation and testing on the Virtex-4QV space-grade device and will continue to do so for the SIRF device. The processors that Xilinx supports are the MicroBlaze (Virtex-4 and SIRF), the PPC405 (Virtex-4) and the PPC440 (SIRF). Sandia National Laboratories (SNL) is currently positioned to help develop mitigation strategies for the SIRF device through its involvement in the XRTC. ***It is highly recommended that SNL continue to place a high priority on its involvement in XRTC activities.***

# 2. FPGA-BASED PROCESSOR DOWN-SELECTION

The long list of processor intellectual property (IP) suitable for NBAs and its wide variety of applications was whittled down using the following criteria:

- Only 32-bit processors were considered. It was desirable to eliminate memory space addressing and paging problems associated with 8- and 16-bit devices.
- Only processors that could be outfitted with a floating-point unit (FPU) were considered.
- The search was limited to popular architectures to take advantage of economies of scale.
- Support for radiation effects testing and mitigation was desired.

Processor cores “native” to the Xilinx Virtex-5 (MicroBlaze and PPC) are attractive for use in NBAs for several reasons:

- They are inexpensive. Dual PPC440 cores are built into the FX130T device and are essentially “free” with the purchase of the FPGA itself – Xilinx has paid for the PPC440 IP and built that into the sale price of the FPGA. The MicroBlaze processor is IP that is available with the purchase of the Xilinx Embedded Development Kit (EDK) software at a very affordable price of $500. Software development tools for both processors are available as part of the EDK.
- Mitigation strategies are developed and tested by Xilinx and the XRTC. SNL is a member and contributor to the XRTC. Xilinx and the XRTC are going to great effort to characterize their FPGAs and to develop mitigation strategies for all of the FPGA building blocks, including these processors. This type of development effort would be left to the individual with non-native processors targeted to the Xilinx platform.

Xilinx native processors and the Xilinx processor design flow are not without their drawbacks, including:

- Soft-core processor and support IP can change from one release of Xilinx tools to the next, impacting the number of resources used for both system definition and mitigation. One could be “stuck” with using older Xilinx toolsets just to support a known processor and processor IP version.
- Newer versions of Xilinx tools tend to drop off support for older FPGA devices. This could be a concern several years down the NBA development path.

The risk mitigation scheme for these issues would be to include a tool archival process into the project.

A couple of popular processor IP cores that are traditionally used in System on Chip (SoC) designs and can also be targeted to FPGA platforms were initially considered but then eliminated because of IP licensing issues.

***ARC International*** provides several configurable central processing unit (CPU) and digital signal processing (DSP) IP cores. However, the licensing fees for these cores were outside of the budget of this study.

***ARM Ltd*** is the provider of the most widely used microprocessor cores. The newest cores in the ARM product line come from the ARM Cortex family. ARM has licensing fees on par with ARC. An attempt was made to obtain an evaluation license and non-disclosure agreement for characterizing ARM Cortex performance after Xilinx TMRTool mitigation. However, an agreement could not be negotiated and this effort was abandoned. Currently Actel has a license agreement with ARM to provide Cortex processors in FLASH-based FPGA devices. Unfortunately, the license agreement does not extend to anti-fuse FPGA devices. It is not expected that Actel will support anti-fuse devices with the Cortex processor in the near future.

# 3. PERFORMANCE METRICS

Dhrystone v2.1 processing metric applications (fixed-point performance) were developed for three processor types (PPC405, MicroBlaze Version 6.00.b, and LEON3) and executed on the Xilinx ML-405 and Xilinx ML-410 development boards. The main objective of this Dhrystone benchmark experiment was not only to compare the processors to each other with respect to their suitability for use in any NBA scenario, but to also see how each processor behaves when operational design parameters of the processor system are modified and how these processor designs impact FPGA resource utilization. The benchmark results shown may not match those published by manufacturers – the benchmarks included in this report are for ***unoptimized*** hardware and software designs.

For the PPC405 processor, configurations that were tested for multiple trials included:

- Processor speed (100 MHz to 300 MHz)
- Application location in memory (internal BlockRAM [BRAM] or external synchronous dynamic random access memory [SDRAM])
- Cache configuration (enabled or disabled)

Configurations in the MicroBlaze trials included:

- Processor speed (50 MHz to 100 MHz)
- Application location in memory (internal BRAM or external SDRAM)
- Cache configuration (enabled or disabled)

Variables in the LEON trials included:

- Processor speed (40 MHz to 75 MHz)
- Application location in external SDRAM
- Cache configuration (enabled or disabled)

For all processors, performance increased by enabling the caches. For the PPC405, the location of the application in memory was a surprising factor – the processor was most efficient when running out of external SDRAM as opposed to the internal BRAMs of the Virtex-4. The processing efficiency of the PPC also decreased with increasing clock rates. This points to some non-optimal design of the PPC system – the peripheral bus frequency being held at a constant 100 MHz is the likely cause.

Normalized plots of the processor benchmarks show that the LEON3 is more efficient than either the MicroBlaze or PPC405 in DMIPS/MHz, but because it cannot operate at the higher frequencies that the others can it is not suitable for computationally intensive algorithms.

Whetstone v1.2 processing performance metric applications (floating-point performance) were also created for the three processors. Tests were conducted with both floating-point emulation and with floating-point units.  All three processors utilized soft-core floating-point unit (FPU) to enhance the floating-point performance of the standard core.

For the PPC405 processor, configurations that were tested with floating-point emulation were:

- Processor speed (100 MHz to 300 MHz)
- Application location in memory (internal BRAM or external SDRAM)
- Cache configuration (enabled or disabled)

IP restrictions for the PPC405 FPU used (evaluation version) limited the processor speed to a single frequency (200 MHz) when the FPU was enabled.  Otherwise, the following parameters were varied:

- Application location in memory (internal BRAM or external SDRAM)
- Cache configuration (enabled or disabled)

MicroBlaze Whetstone tests included varying:

- Processor speed (50 MHz to 100 MHz)
- Application location in memory (internal BRAM or external SDRAM)
- Cache configuration (enabled or disabled)
- FPU configuration (enabled or disabled)

LEON processor Whetstone test results with the FPU enabled were a bit inconclusive and unresolved after several iterations.  With the LEON processor FPU enabled and running at 20 MHz, the performance of the LEON was 8x greater than the PPC running at 200 MHz.  These results are unbelievable, even though the LEON core passed all of the core validation metrics.

Independent Whetstone performance numbers for each of the three processor types were unavailable to corroborate the results that were obtained.

## 3.1 Virtex-4 Dhrystone

The normalized Dhrystone plot in Figure 1 shows that the LEON3 soft-core processor is more efficient than the MicroBlaze and PPC processors – especially when the cache is enabled. Computationally intensive applications are not well suited for the LEON3, however, because the maximum operational frequency of the soft core is only around 75 MHz due to FPGA timing limitations.  The upper frequency tested on the soft-core MicroBlaze was 100 MHz (again, FPGA timing restrictions) and the upper frequency tested for the PowerPC405 was 300 MHz.

The on-chip memory controller (OCM) for the PPC405 shows a decline in efficiency for increasing processor frequencies.

Figure 2 shows that the PPC405 processor hard core has better raw performance than both the LEON3 and the MicroBlaze soft cores, and therefore is considered a better target for computationally intensive applications.

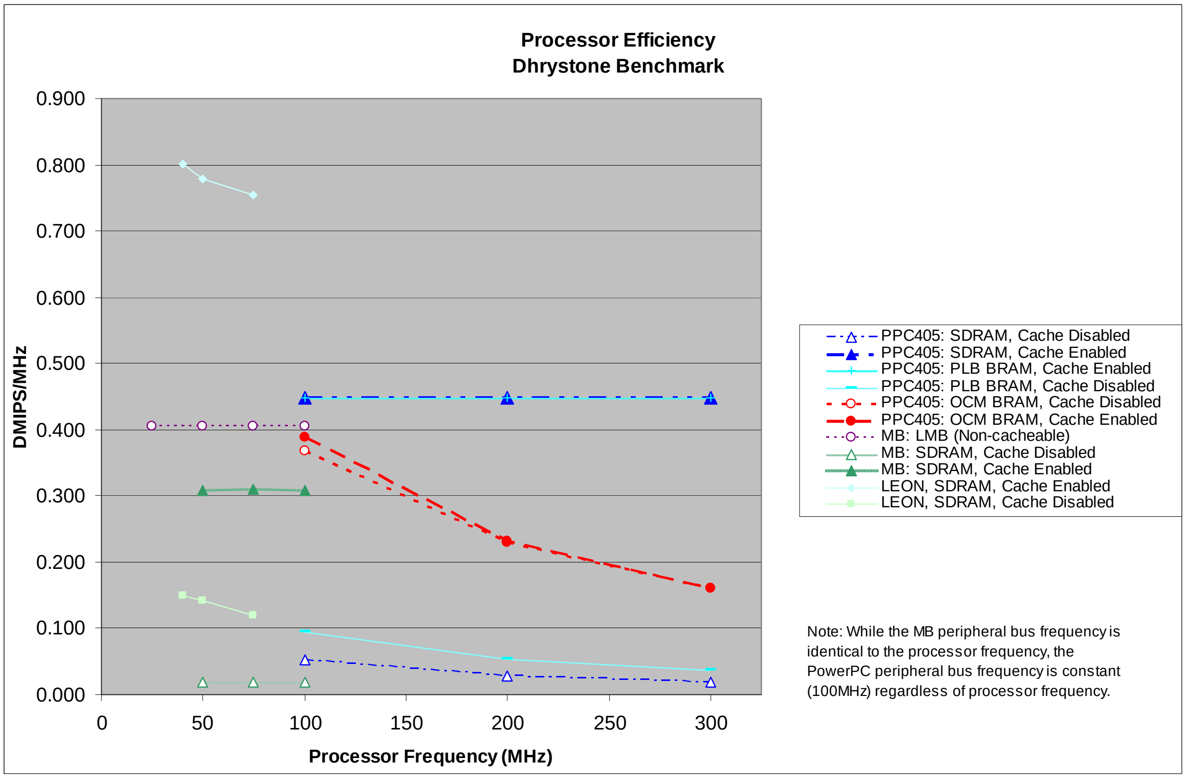



*Figure 1. Processor speed normalized Dhrystone benchmark results: all processors.*

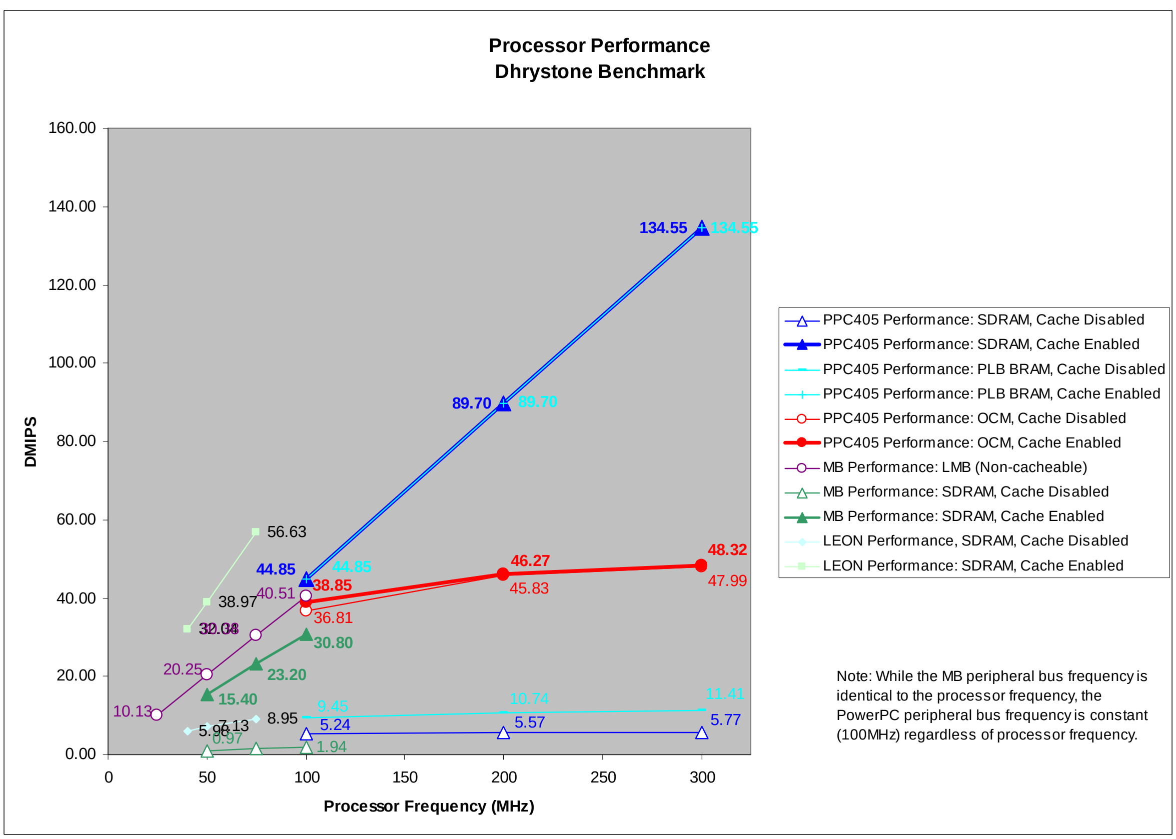



*Figure 2. Non-normalized Dhrystone benchmark results: all processors.*

### *3.1.1 Virtex-4 PPC405*

This section contains a summary of the PPC405 configuration used in the Dhrystone benchmark.

Processor core frequency is listed in the second column of Table 1. The on-chip peripheral bus (OPB) frequency is 100 MHz for PPC405. It is possible to modify the OPB frequency, but it was held constant during these tests for the sake of reducing configurations.

The Virtex-4 PPC405 has a ***fixed*** cache size: 16 Kbytes for data and 16 Kbytes for instruction. Unlike the soft core MicroBlaze and LEON3 processors, the cache size for the V4 PPC405 cannot be changed.

Local memory (BRAM) used in these tests was 32 KBytes for data and 32 Kbytes for instructions.

The size of the executable listed in Table 1 is the size of an executable created for loading via the Joint Test Action Group (JTAG) cable and not the Flash read-only memory (ROM) binary size.

Note: The Virtex-4 speed grade –10 does not allow for 400 MHz PPC405 operation (DS302, p13, CPMC405CLOCK AC switching limitations). 300 MHz was the highest PPC405 frequency tested on the ML-405 board.

The V4 PPC405 FPU can only be used up to 233 MHz in a –10 speed grade Virtex-4, an IP limitation. The highest frequency tested was 200 MHz.

Figure 3 shows the Virtex-4 PPC405 Dhrystone efficiency vs. frequency for the different configurations.

*Table 1. Virtex-4 PPC405 Dhrystone Application Configuration and Memory Utilization.*

| Processor Setup | | | | | Dhrystone Scores | | | | | | Application Size | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Processor | Processor Frequency (MHz) | FPU | Cache | Code Location | # of Runs | Duration (sec) | Microseconds for one run through Dhrystone | Dhrystones per Second | DMIPS | DMIPS/ MHz | .text | .data | .bss | Total Size of Executable |
| PPC405 | 100 | Disabled | Disabled | PLB | 100000 | 6.02 | 60.2 | 16611.3 | **9.45** | **0.095** | 24058 | 1360 | 12936 | 38354 |
| PPC405 | 200 | Disabled | Disabled | PLB | 100000 | 5.30 | 53.0 | 18875.0 | **10.74** | **0.054** | 24058 | 1360 | 12936 | 38354 |
| PPC405 | 300 | Disabled | Disabled | PLB | 100000 | 4.99 | 49.9 | 20040.1 | **11.41** | **0.038** | 24058 | 1360 | 12936 | 38354 |
| PPC405 | 100 | Disabled | Enabled | PLB | 100000 | 1.27 | 12.7 | 78801.7 | **44.85** | **0.449** | 24058 | 1364 | 12932 | 38354 |
| PPC405 | 200 | Disabled | Enabled | PLB | 100000 | 0.63 | 6.3 | 157602.3 | **89.70** | **0.448** | 24058 | 1364 | 12932 | 38354 |
| PPC405 | 300 | Disabled | Enabled | PLB | 100000 | 0.42 | 4.2 | 236401.8 | **134.55** | **0.448** | 24058 | 1364 | 12932 | 38354 |
| PPC405 | 100 | Disabled | Disabled | OCM | 100000 | 1.55 | 15.5 | 64683.1 | **36.81** | **0.368** | 24058 | 1360 | 18828 | 44246 |
| PPC405 | 200 | Disabled | Disabled | OCM | 100000 | 1.24 | 12.4 | 80515.3 | **45.83** | **0.229** | 24058 | 1360 | 12940 | 38358 |
| PPC405 | 300 | Disabled | Disabled | OCM | 100000 | 1.19 | 11.9 | 84317.0 | **47.99** | **0.160** | 24058 | 1360 | 12940 | 38358 |
| PPC405 | 100 | Disabled | Enabled | OCM | 100000 | 1.47 | 14.7 | 68259.4 | **38.85** | **0.388** | 24058 | 1364 | 18824 | 44246 |
| PPC405 | 200 | Disabled | Enabled | OCM | 100000 | 1.23 | 12.3 | 81300.8 | **46.27** | **0.231** | 24058 | 1364 | 12936 | 38358 |
| PPC405 | 300 | Disabled | Enabled | OCM | 100000 | 1.18 | 11.8 | 84889.6 | **48.32** | **0.161** | 24058 | 1364 | 12936 | 38358 |
| PPC405 | 200 | Disabled | Disabled | OPBRAM | 100000 | 10.69 | 106.9 | 9351.9 | **5.32** | **0.027** | 24058 | 1360 | 12948 | 38366 |
| PPC405 | 200 | Disabled | Enabled | OPBRAM | 100000 | 0.63 | 6.3 | 157599.8 | **89.70** | **0.448** | 24058 | 1364 | 12940 | 38362 |
| PPC405 | 100 | Disabled | Disabled | SDRAM | 100000 | 10.86 | 108.6 | 9205.9 | **5.24** | **0.052** | 24058 | 1360 | 18824 | 44242 |
| PPC405 | 200 | Disabled | Disabled | SDRAM | 100000 | 10.22 | 102.2 | 9784.7 | **5.57** | **0.028** | 24058 | 1360 | 12936 | 38354 |
| PPC405 | 300 | Disabled | Disabled | SDRAM | 100000 | 9.87 | 98.7 | 10133.5 | **5.77** | **0.019** | 24058 | 1360 | 12936 | 38354 |
| PPC405 | 100 | Disabled | Enabled | SDRAM | 100000 | 1.27 | 12.7 | 78801.2 | **44.85** | **0.448** | 24058 | 1364 | 18820 | 44242 |
| PPC405 | 200 | Disabled | Enabled | SDRAM | 100000 | 0.63 | 6.3 | 157600.2 | **89.70** | **0.448** | 24058 | 1364 | 12932 | 38354 |
| PPC405 | 300 | Disabled | Enabled | SDRAM | 100000 | 0.42 | 4.2 | 236397.2 | **134.55** | **0.448** | 24058 | 1364 | 12932 | 38354 |

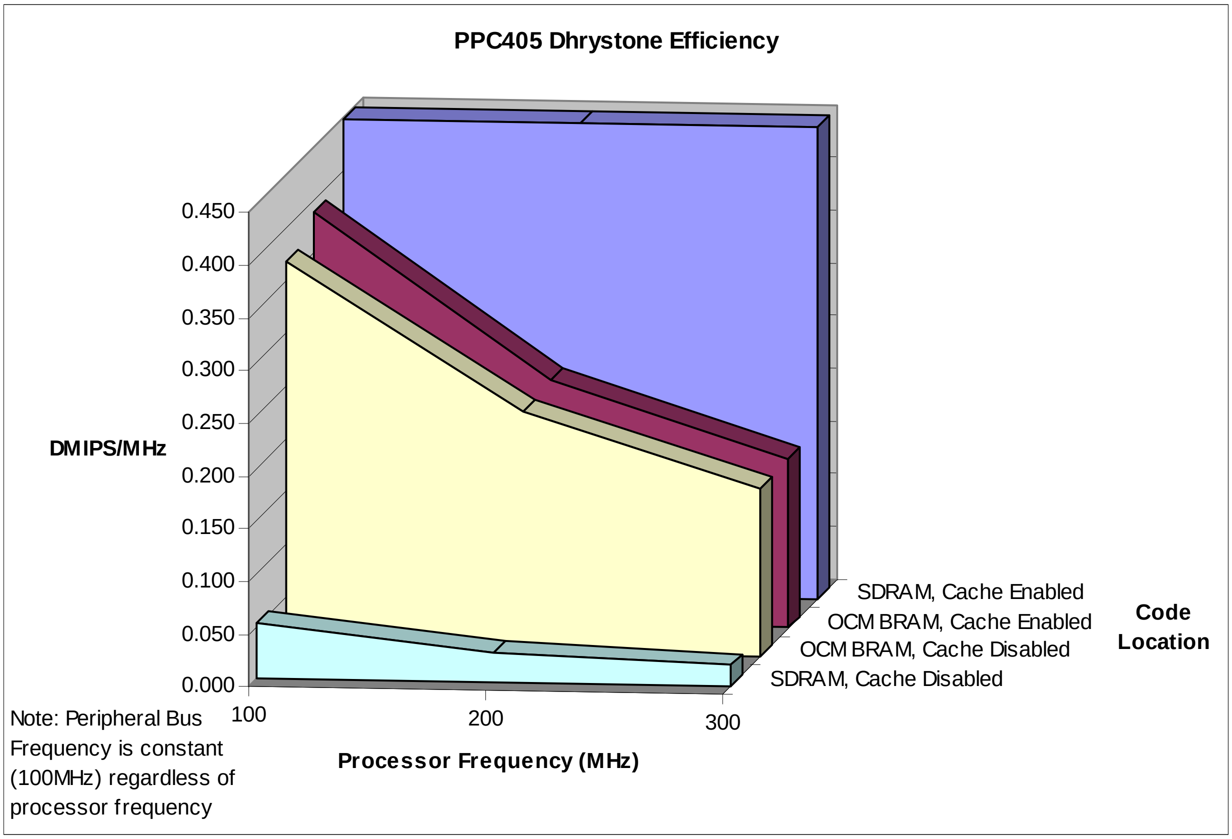



*Figure 3. Normalized Dhrystone benchmark details: Virtex-4 PPC405.*

### *3.1.2 MicroBlaze*

This section contains a summary of the MicroBlaze configuration used in the Dhrystone benchmark.

Processor core frequency is listed in the second column of Table 2. The OPB frequency was equal to the processor frequency for the MicroBlaze.

The MicroBlaze has a ***programmable*** cache size. For this test 16 Kbytes for data and 16 Kbytes for instruction cache were defined. The cache is comprised of BRAM blocks.

The size of the executable listed in Table 1 is the size of an executable created for loading via the JTAG cable and is not the Flash ROM binary size.

The MicroBlaze is capable of utilizing internal Virtex-4 BRAM as program/data space with the Local Memory Bus (LMB) IP.

Figure 4 shows the MicroBlaze Dhrystone efficiency vs. frequency for the different configurations.

*Table 2. Virtex-4 MicroBlaze Dhrystone Application Configuration and Memory Utilization.*

| Processor Setup | | | | | Dhrystone Scores | | | | | | Application Size | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Processor | Processor Frequency (MHz) | FPU | Cache | Code Location | # of Runs | Duration (sec) | Microseconds for one run through Dhrystone | Dhrystones per Second | DMIPS | DMIPS/ MHz | .text | .data | .bss | Total Size of Executable |
| MB | 25 | Disabled | Disabled | LMB | 100000 | 5.62 | 56.2 | 17793.6 | **10.13** | **0.405** | 13052 | 3146 | 12896 | 29094 |
| MB | 50 | Disabled | Disabled | LMB | 100000 | 2.81 | 28.1 | 35587.2 | **20.25** | **0.405** | 13052 | 3146 | 12896 | 29094 |
| MB | 75 | Disabled | Disabled | LMB | 100000 | 1.87 | 18.7 | 53380.8 | **30.38** | **0.405** | 13040 | 3146 | 12900 | 29086 |
| MB | 100 | Disabled | Disabled | LMB | 100000 | 1.41 | 14.1 | 71174.4 | **40.51** | **0.405** | 13048 | 3146 | 12900 | 29094 |
| MB | 25 | Disabled | Disabled | SDRAM | 100000 | would not run | #VALUE! | #VALUE! | **######** | **######** | 14108 | 3146 | 12896 | 30150 |
| MB | 50 | Disabled | Disabled | SDRAM | 100000 | 58.82 | 588.2 | 1700.2 | **0.97** | **0.019** | 14108 | 3146 | 12896 | 30150 |
| MB | 75 | Disabled | Disabled | SDRAM | 100000 | 39.34 | 393.4 | 2541.9 | **1.45** | **0.019** | 14096 | 3146 | 12900 | 30142 |
| MB | 100 | Disabled | Disabled | SDRAM | 100000 | 29.41 | 294.1 | 3400.5 | **1.94** | **0.019** | 14104 | 3146 | 12900 | 30150 |
| MB | 25 | Disabled | Enabled | SDRAM | 100000 | would not run | #VALUE! | #VALUE! | **######** | **######** | 14108 | 3150 | 12892 | 30150 |
| MB | 50 | Disabled | Enabled | SDRAM | 100000 | 3.70 | 37.0 | 27057.1 | **15.40** | **0.308** | 14108 | 3150 | 12892 | 30150 |
| MB | 75 | Disabled | Enabled | SDRAM | 100000 | 2.45 | 24.5 | 40766.7 | **23.20** | **0.309** | 14096 | 3150 | 12888 | 30134 |
| MB | 100 | Disabled | Enabled | SDRAM | 100000 | 1.85 | 18.5 | 54114.3 | **30.80** | **0.308** | 14104 | 3150 | 12888 | 30142 |

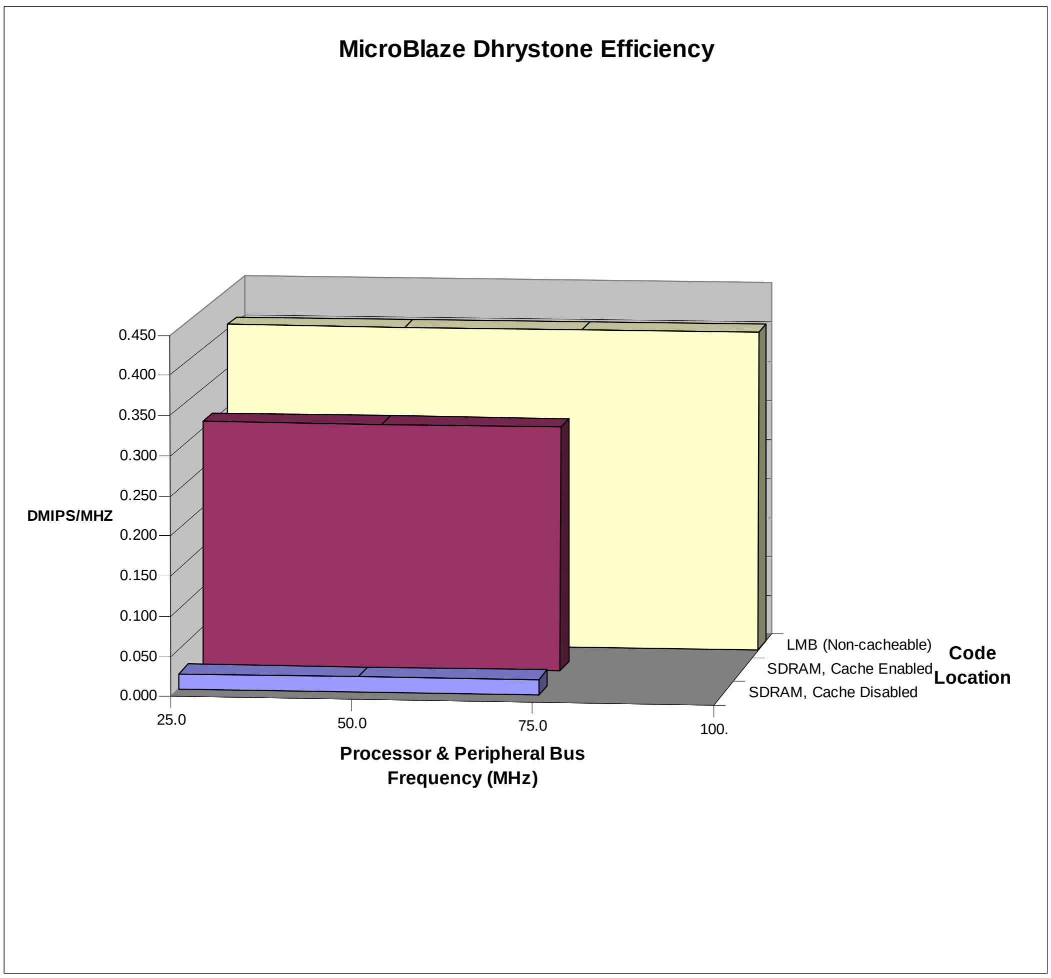



*Figure 4. Virtex-4 MicroBlaze normalized Dhrystone benchmark details.*

### *3.1.3 LEON3*

This section contains a summary of the LEON3 configuration used in the Dhrystone benchmark.

The processor frequency is equal to the core frequency listed in Table 3.

*Table 3. Virtex-4 LEON3 Dhrystone Application Configuration and Memory Utilization.*

| Processor Setup | | | | | | Dhrystone Scores | | | | | | Application Size | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Processor | Processor Frequency (MHz) | mv8 Compile Switch | FPU | Cache | Code Location | # of Runs | Duration (sec) | Microseconds for one run through Dhrystone | Dhrystones per Second | DMIPS | DMIPS/MHz | .text | .data | .bss | Total Size of Executable | Notes |
| LEON | 25 | Disabled | Disabled | Disabled | SDRAM | 200000 | | | Would not synthesize | | | | | | | |
| LEON | 40 | Disabled | Disabled | Disabled | SDRAM | 200000 | 20.958 | 104.79 | 9542.9 | **5.43** | **0.136** | 50432 | 2464 | 10772 | 52896 | |
| LEON | 50 | Disabled | Disabled | Disabled | SDRAM | 200000 | 17.657 | 88.29 | 11327.0 | **6.45** | **0.129** | 50432 | 2464 | 10772 | 52896 | |
| LEON | 75 | Disabled | Disabled | Disabled | SDRAM | 200000 | 14.022 | 70.11 | 14263.3 | **8.12** | **0.108** | 50432 | 2464 | 10772 | 52896 | |
| LEON | 25 | Disabled | Disabled | Enabled | SDRAM | 200000 | | | Would not synthesize | | | | | | | |
| LEON | 40 | Disabled | Disabled | Enabled | SDRAM | 200000 | 3.828 | 19.14 | 52246.6 | **29.74** | **0.743** | 50432 | 2464 | 10772 | 52896 | |
| LEON | 50 | Disabled | Disabled | Enabled | SDRAM | 200000 | 3.138 | 15.69 | 63734.9 | **36.27** | **0.725** | 50432 | 2464 | 10772 | 52896 | |
| LEON | 75 | Disabled | Disabled | Enabled | SDRAM | 200000 | 2.157 | 10.79 | 92721.4 | **52.77** | **0.704** | 50432 | 2464 | 10772 | 52896 | |
| LEON | 25 | Enabled | Disabled | Disabled | SDRAM | 200000 | | | Would not synthesize | | | | | | | |
| LEON | 40 | Enabled | Disabled | Disabled | SDRAM | 200000 | 19.042 | 95.21 | 10503.1 | **5.98** | **0.149** | 50416 | 2464 | 10772 | 52880 | |
| LEON | 50 | Enabled | Disabled | Disabled | SDRAM | 200000 | 15.969 | 79.85 | 12524.3 | **7.13** | **0.143** | 50416 | 2464 | 10772 | 52880 | |
| LEON | 75 | Enabled | Disabled | Disabled | SDRAM | 200000 | 12.713 | 63.57 | 15731.9 | **8.95** | **0.119** | 50416 | 2464 | 10772 | 52880 | |
| LEON | 25 | Enabled | Disabled | Enabled | SDRAM | 200000 | | | Would not synthesize | | | | | | | |
| LEON | 40 | Enabled | Disabled | Enabled | SDRAM | 200000 | 3.553 | 17.77 | 56290.5 | **32.04** | **0.801** | 50416 | 2464 | 10772 | 52880 | |
| LEON | 50 | Enabled | Disabled | Enabled | SDRAM | 200000 | 2.921 | 14.61 | 68469.7 | **38.97** | **0.779** | 50416 | 2464 | 10772 | 52880 | |
| LEON | 75 | Enabled | Disabled | Enabled | SDRAM | 200000 | 2.010 | 10.05 | 99502.5 | **56.63** | **0.755** | 50416 | 2464 | 10772 | 52880 | |

The LEON3 has an ***extremely programmable*** cache size. For this test 16 Kbytes for data and 16 Kbytes for instruction cache were defined.

There are fewer memory configuration options for LEON3 than for MicroBlaze and Virtex-4 PPC405 processors for the ML-405 and ML-410 platforms; all LEON code was located in SDRAM for these tests. The LEON3 configuration utility is FPGA platform independent and does not know how to construct a processor memory block from the internal Virtex-4 BRAMs.

Figure 5 shows the MicroBlaze Dhrystone efficiency vs. frequency for the different configurations.

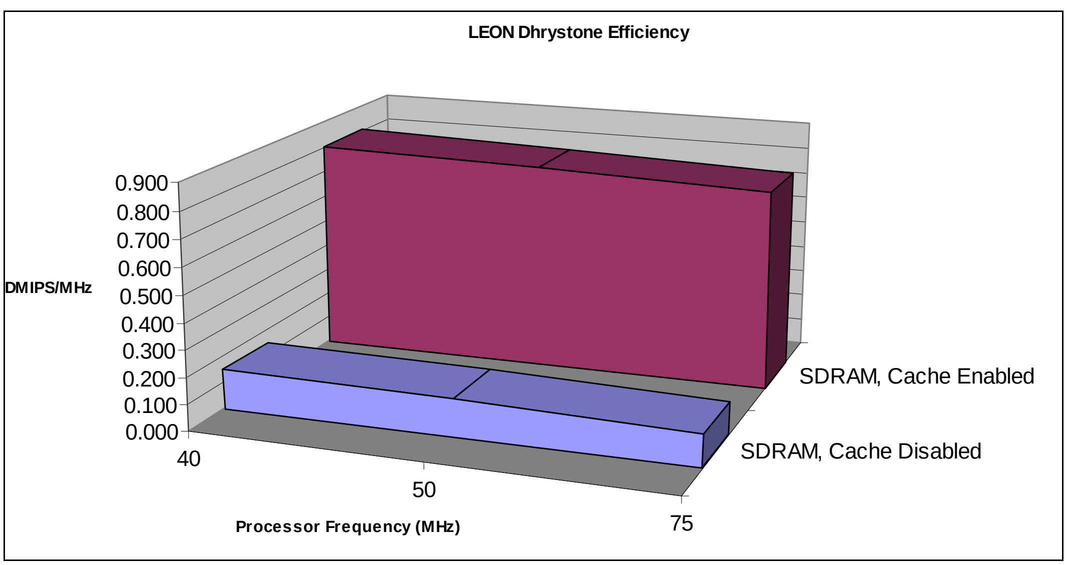



*Figure 5. Virtex-4 LEON3 normalized Dhrystone benchmark details.*

## 3.2 Virtex-4 Whetstone

The normalized Whetstone plot in Figure 6 shows that the LEON3 soft-core processor is more efficient than the MicroBlaze and PPC processors – especially when the cache is enabled. Computationally intensive applications are not well suited for the LEON3, however, because its raw performance is limited by the maximum synthesizable core frequency (75 MHz on the Virtex-4 –10 speed-grade). The PPC FPU was compiled into the hardware design for the Whetstone tests discussed in this section.

The OCM for the PPC405 again shows a decline in efficiency for increasing processor frequencies.

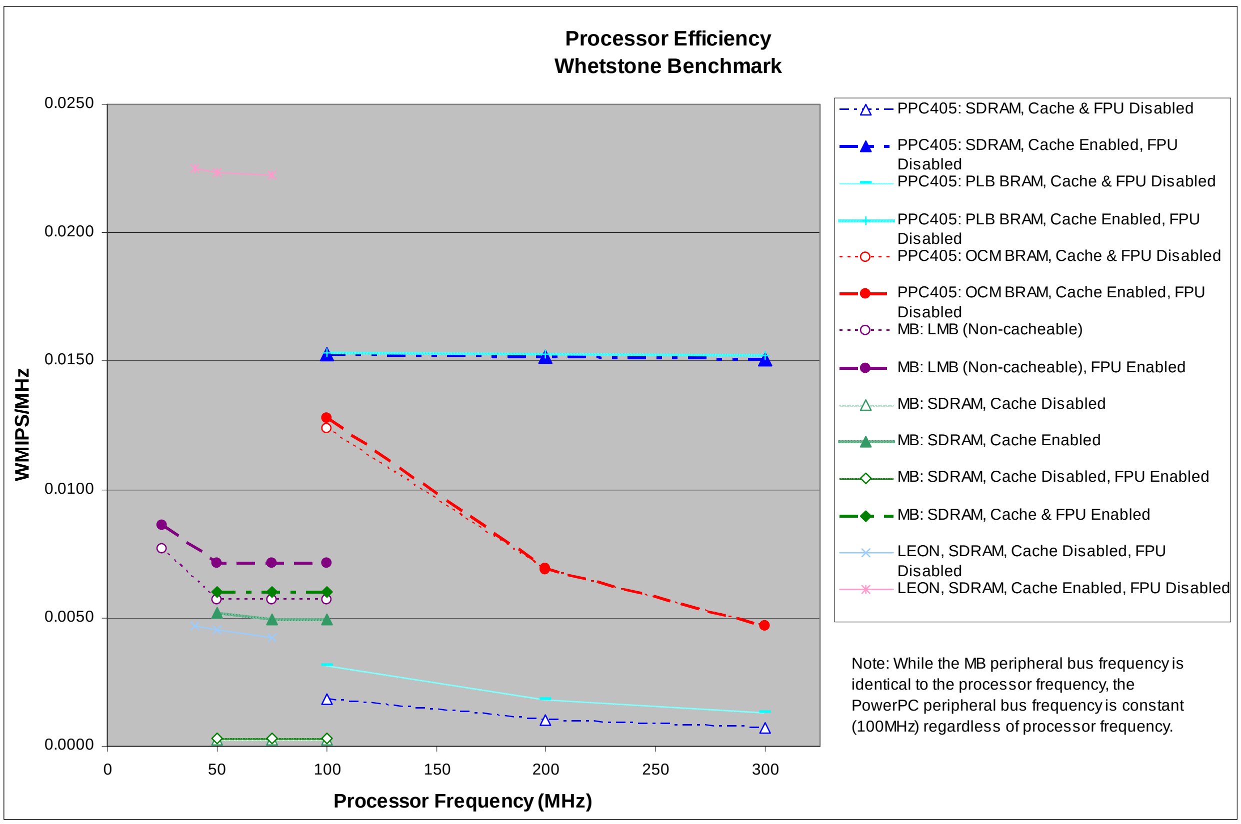



*Figure 6. Processor speed normalized Whetstone benchmark results: all processors.*

Figure 7 shows that the PPC405 processor hard core outperforms both the LEON3 and the MicroBlaze soft cores, and therefore is considered a better target for computationally intensive applications.

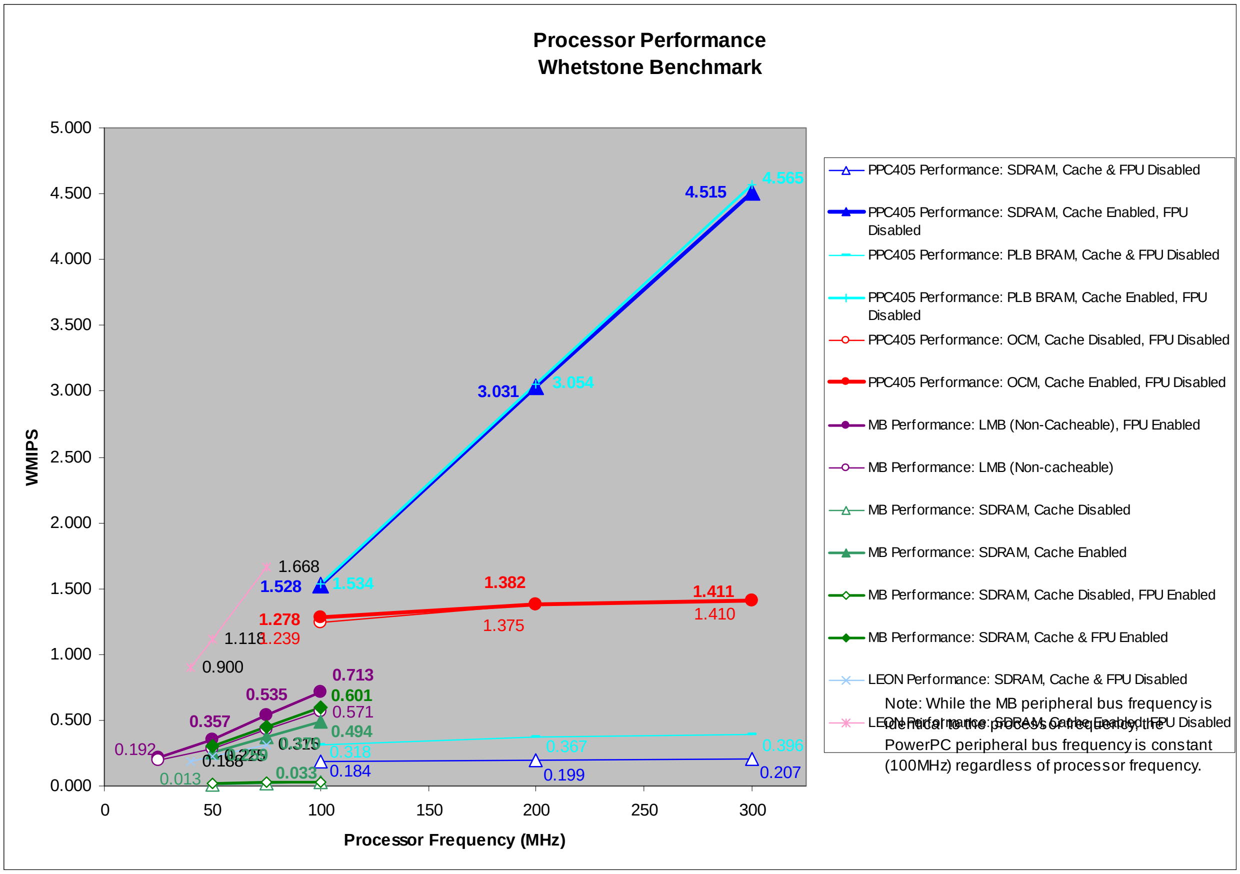



*Figure 7.  Non-normalized Whetstone benchmark results: all processors.*

### *3.2.1    Virtex-4 PPC405*

This section contains a summary of the PPC405 configuration used in the Whetstone benchmark.

Processor core frequency is listed in the second column of Table 4.  The OPB frequency is 100 MHz for PPC405.  It is possible to modify the OPB frequency, but it was held constant during these tests for the sake of reducing configurations.

Note: The PPC405 FPU can only be used when the peripheral frequency is exactly 1/2 the processor frequency.

The Virtex-4 PPC405 has a ***fixed*** cache size:  16 Kbytes for data and 16 Kbytes for instruction. Unlike the soft core MicroBlaze and LEON3 processors, the cache size for the Virtex-4 PPC405 cannot be changed.

*Table 4. Virtex-4 PPC405 Whetstone Application Configuration and Memory Utilization.*

| Processor setup | | | | | Single Precision FP Whetstone Scores | | | | | Application Size | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Processor** | **Processor Frequency (MHz)** | **FPU** | **Cache** | **Code Location** | **# of loops** | **# of Iterations** | **Duration (sec)** | **Whetstones (MIPS)** | **WMIPS/MHz** | **.text** | **.data** | **.bss** | **Total Size of Executable** | **Speed-Up Due to FPU** |
| **PPC405** | 100 | **Disabled** | **Disabled** | PLB | 30 | 1 | 9.442 | **0.318** | **0.0032** | 42613 | 324 | 2676 | 45613 | |
| **PPC405** | 200 | **Disabled** | **Disabled** | PLB | 30 | 1 | 8.168 | **0.367** | **0.0018** | 42613 | 324 | 2676 | 45613 | |
| **PPC405** | 300 | **Disabled** | **Disabled** | PLB | 30 | 1 | 7.571 | **0.396** | **0.0013** | 42613 | 324 | 2676 | 45613 | |
| **PPC405** | 200 | **Enabled** | **Disabled** | PLB | 30 | 1 | 6.279 | **0.478** | **0.0024** | 40257 | 324 | 2684 | 43265 | 23% |
| **PPC405** | 100 | **Disabled** | **Enabled** | PLB | 30 | 1 | 1.956 | **1.534** | **0.0153** | 42613 | 328 | 2672 | 45613 | |
| **PPC405** | 200 | **Disabled** | **Enabled** | PLB | 30 | 1 | 0.982 | **3.054** | **0.0153** | 42613 | 328 | 2672 | 45613 | |
| **PPC405** | 300 | **Disabled** | **Enabled** | PLB | 30 | 1 | 0.657 | **4.565** | **0.0152** | 42613 | 328 | 2672 | 45613 | |
| **PPC405** | 200 | **Enabled** | **Enabled** | PLB | 30 | 1 | 0.789 | **3.803** | **0.0190** | 40257 | 328 | 2680 | 43265 | 20% |
| **PPC405** | 100 | **Disabled** | **Disabled** | **OCM** | 30 | 1 | 2.421 | **1.239** | **0.0124** | 42613 | 324 | 2676 | 45613 | |
| **PPC405** | 200 | **Disabled** | **Disabled** | **OCM** | 30 | 1 | 2.182 | **1.375** | **0.0069** | 42613 | 324 | 2676 | 45613 | |
| **PPC405** | 300 | **Disabled** | **Disabled** | **OCM** | 30 | 1 | 2.128 | **1.410** | **0.0047** | 42613 | 324 | 2676 | 45613 | |
| **PPC405** | 200 | **Enabled** | **Disabled** | **OCM** | 30 | 1 | 1.714 | **1.750** | **0.0088** | 40257 | 324 | 2676 | 43257 | 21% |
| **PPC405** | 100 | **Disabled** | **Enabled** | **OCM** | 30 | 1 | 2.347 | **1.278** | **0.0128** | 42613 | 328 | 2672 | 45613 | |
| **PPC405** | 200 | **Disabled** | **Enabled** | **OCM** | 30 | 1 | 2.171 | **1.382** | **0.0069** | 42613 | 328 | 2672 | 45613 | |
| **PPC405** | 300 | **Disabled** | **Enabled** | **OCM** | 30 | 1 | 2.126 | **1.411** | **0.0047** | 42613 | 328 | 2672 | 45613 | |
| **PPC405** | 200 | **Enabled** | **Enabled** | **OCM** | 30 | 1 | 1.700 | **1.765** | **0.0088** | 40257 | 328 | 2672 | 43257 | 22% |
| **PPC405** | 100 | **Disabled** | **Disabled** | **SDRAM** | 30 | 1 | 16.346 | **0.184** | **0.0018** | 42613 | 324 | 2676 | 45613 | |
| **PPC405** | 200 | **Disabled** | **Disabled** | **SDRAM** | 30 | 1 | 15.047 | **0.199** | **0.0010** | 42613 | 324 | 2676 | 45613 | |
| **PPC405** | 300 | **Disabled** | **Disabled** | **SDRAM** | 30 | 1 | 14.461 | **0.207** | **0.0007** | 42613 | 324 | 2676 | 45613 | |
| **PPC405** | 200 | **Enabled** | **Disabled** | **SDRAM** | 30 | 1 | 11.489 | **0.261** | **0.0013** | 40257 | 324 | 2684 | 43265 | 24% |
| **PPC405** | 100 | **Disabled** | **Enabled** | **SDRAM** | 30 | 1 | 1.963 | **1.528** | **0.0153** | 42613 | 328 | 2672 | 45613 | |
| **PPC405** | 200 | **Disabled** | **Enabled** | **SDRAM** | 30 | 1 | 0.990 | **3.031** | **0.0152** | 42613 | 328 | 2672 | 45613 | |
| **PPC405** | 300 | **Disabled** | **Enabled** | **SDRAM** | 30 | 1 | 0.664 | **4.515** | **0.0150** | 42613 | 328 | 2672 | 45613 | |
| **PPC405** | 200 | **Enabled** | **Enabled** | **SDRAM** | 30 | 1 | 0.796 | **3.770** | **0.0189** | 40257 | 328 | 2680 | 43265 | 20% |
| **PPC405** | 200 | **Disabled** | **Disabled** | **OPBRAM** | 30 | 1 | 16.040 | **0.187** | **0.0009** | 42613 | 324 | 2676 | 45613 | |
| **PPC405** | 200 | **Disabled** | **Enabled** | **OPBRAM** | 30 | 1 | 0.992 | **3.025** | **0.0151** | 42613 | 328 | 2672 | 45613 | |

Figures 8 and 9 show graphically the Whetstone performance of the PPC405 processor for different memory configurations.

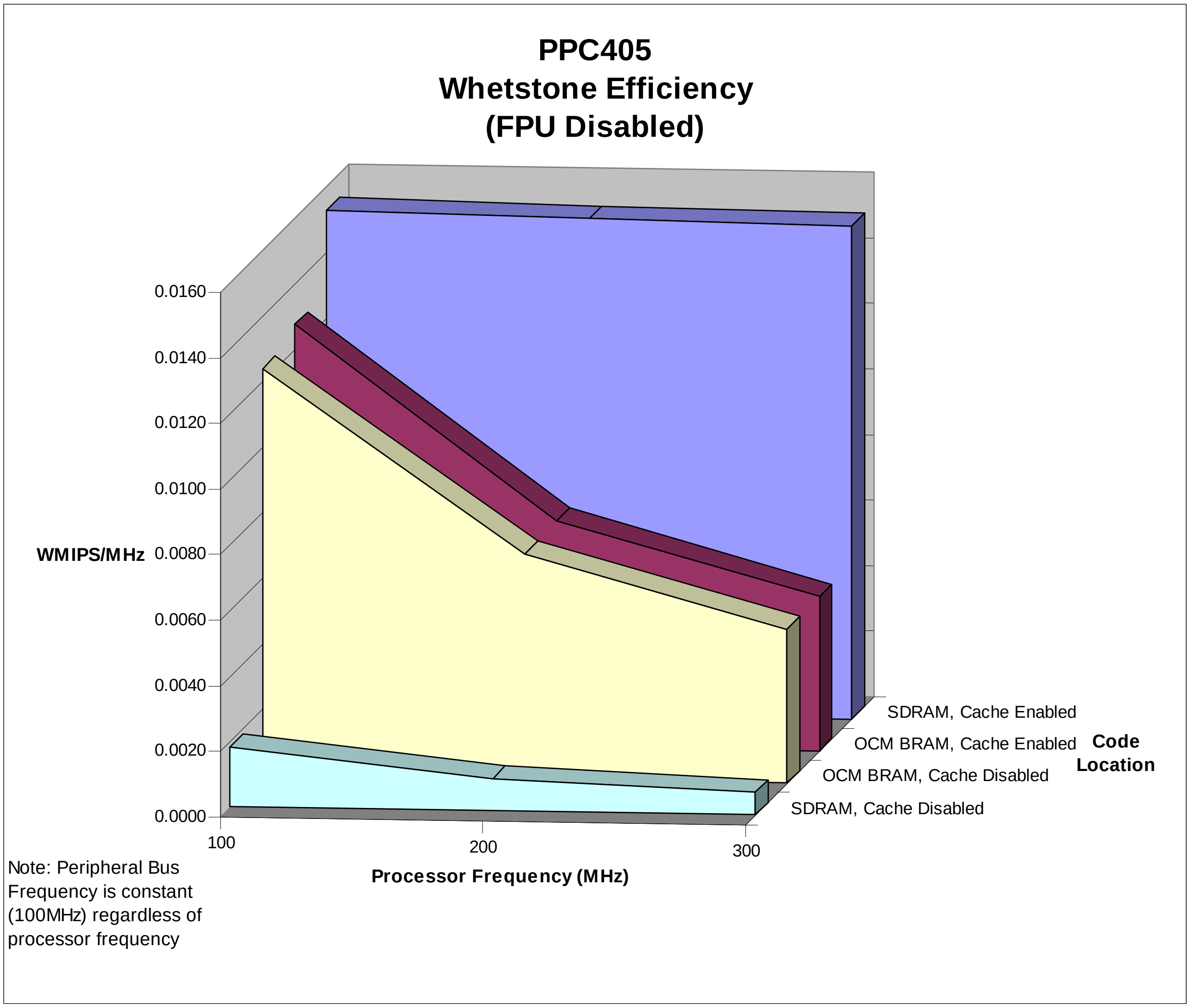



*Figure 8. Virtex-4 PPC405 normalized Whetstone benchmark details, FPU disabled.*

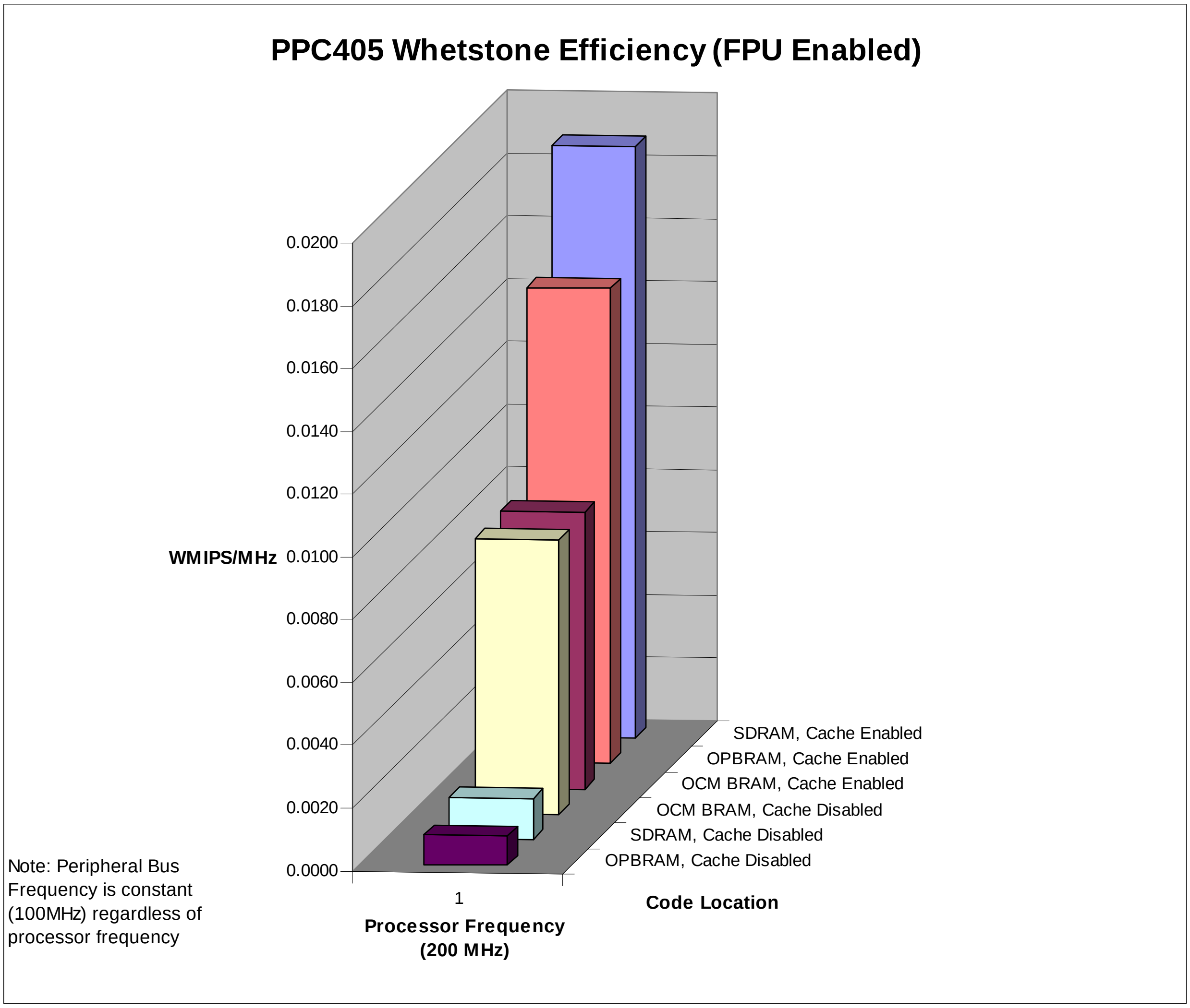



*Figure 9. Virtex-4 PPC405 normalized Whetstone benchmark details, FPU enabled.*

### *3.2.2 MicroBlaze*

This section contains a summary of the MicroBlaze configuration used in the Whetstone benchmark.

Processor core frequency is listed in the second column of Table 5. The OPB frequency was equal to the processor frequency for the MicroBlaze.

The MicroBlaze has a ***programmable*** cache size. For this test 16 Kbytes for data and 16 Kbytes for instruction cache were defined. The cache is comprised of BRAM blocks.

The size of the executable listed in Table 5 is the size of an executable created for loading via the JTAG cable and is not the Flash ROM binary size.

*Table 5. Virtex-4 MicroBlaze Whetstone Application Configuration and Memory Utilization.*

| Processor setup | | | | | Single Precision FP Whetstone Scores | | | | | Application Size | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Processor | Processor Frequency (MHz) | FPU | Cache | Code Location | # of loops | # of Iterations | Duration (sec) | Whetstones (MIPS) | WMIPS/MHz | .text | .data | .bss | Total Size of Executable | Speed-Up Due to FPU |
| MB | 25 | Disabled | Disabled | LMB | 10 | 1 | 5.203 | 0.192 | 0.0077 | 42328 | 2626 | 2632 | 47586 | |
| MB | 50 | Disabled | Disabled | LMB | 10 | 1 | 3.504 | 0.285 | 0.0057 | 42328 | 2626 | 2632 | 47586 | |
| MB | 75 | Disabled | Disabled | LMB | 10 | 1 | 2.336 | 0.428 | 0.0057 | 42328 | 2626 | 2632 | 47586 | |
| MB | 100 | Disabled | Disabled | LMB | 10 | 1 | 1.752 | 0.571 | 0.0057 | 42324 | 2626 | 2636 | 47586 | |
| MB | 25 | Enabled | Disabled | LMB | 10 | 1 | 4.644 | 0.215 | 0.0086 | 39236 | 2610 | 2636 | 44482 | 11% |
| MB | 50 | Enabled | Disabled | LMB | 10 | 1 | 2.805 | 0.357 | 0.0071 | 39232 | 2610 | 2636 | 44478 | 20% |
| MB | 75 | Enabled | Disabled | LMB | 10 | 1 | 1.870 | 0.535 | 0.0071 | 39232 | 2610 | 2636 | 44478 | 20% |
| MB | 100 | Enabled | Disabled | LMB | 10 | 1 | 1.402 | 0.713 | 0.0071 | 39232 | 2610 | 2636 | 44478 | 20% |
| MB | 25 | Disabled | Disabled | SDRAM | 10 | 1 | would not run | #VALUE! | #VALUE! | 42360 | 2626 | 2632 | 47618 | |
| MB | 50 | Disabled | Disabled | SDRAM | 10 | 1 | 75.907 | 0.013 | 0.0003 | 42360 | 2626 | 2632 | 47618 | |
| MB | 75 | Disabled | Disabled | SDRAM | 10 | 1 | 51.027 | 0.020 | 0.0003 | 42360 | 2626 | 2632 | 47618 | |
| MB | 100 | Disabled | Disabled | SDRAM | 10 | 1 | 37.998 | 0.026 | 0.0003 | 42356 | 2626 | 2636 | 47618 | |
| MB | 25 | Enabled | Disabled | SDRAM | 10 | 1 | would not run | #VALUE! | #VALUE! | 39268 | 2610 | 2628 | 44506 | |
| MB | 50 | Enabled | Disabled | SDRAM | 10 | 1 | 60.756 | 0.016 | 0.0003 | 39264 | 2614 | 2624 | 44502 | 20% |
| MB | 75 | Enabled | Disabled | SDRAM | 10 | 1 | 40.880 | 0.024 | 0.0003 | 39256 | 2610 | 2636 | 44502 | 20% |
| MB | 100 | Enabled | Disabled | SDRAM | 10 | 1 | 30.430 | 0.033 | 0.0003 | 39256 | 2610 | 2636 | 44502 | 20% |
| MB | 25 | Disabled | Enabled | SDRAM | 10 | 1 | would not run | #VALUE! | #VALUE! | 42356 | 2630 | 2624 | 47610 | |
| MB | 50 | Disabled | Enabled | SDRAM | 10 | 1 | 3.867 | 0.259 | 0.0052 | 42356 | 2630 | 2624 | 47610 | |
| MB | 75 | Disabled | Enabled | SDRAM | 10 | 1 | 2.703 | 0.370 | 0.0049 | 42356 | 2630 | 2624 | 47610 | |
| MB | 100 | Disabled | Enabled | SDRAM | 10 | 1 | 2.026 | 0.494 | 0.0049 | 42356 | 2630 | 2624 | 47610 | |
| MB | 25 | Enabled | Enabled | SDRAM | 10 | 1 | would not run | #VALUE! | #VALUE! | 39268 | 2614 | 2628 | 44510 | |
| MB | 50 | Enabled | Enabled | SDRAM | 10 | 1 | 3.333 | 0.300 | 0.0060 | 39264 | 2614 | 2624 | 44502 | 14% |
| MB | 75 | Enabled | Enabled | SDRAM | 10 | 1 | 2.225 | 0.449 | 0.0060 | 39256 | 2614 | 2624 | 44494 | 18% |
| MB | 100 | Enabled | Enabled | SDRAM | 10 | 1 | 1.665 | 0.601 | 0.0060 | 39256 | 2614 | 2624 | 44494 | 18% |

Figures 10 and 11 show graphically the Whetstone efficiency of the MicroBlaze processor for different memory, code, and FPU configurations. There is approximately a 20% increase in Whetstone efficiency when using a hardware-based FPU over an emulated FPU.

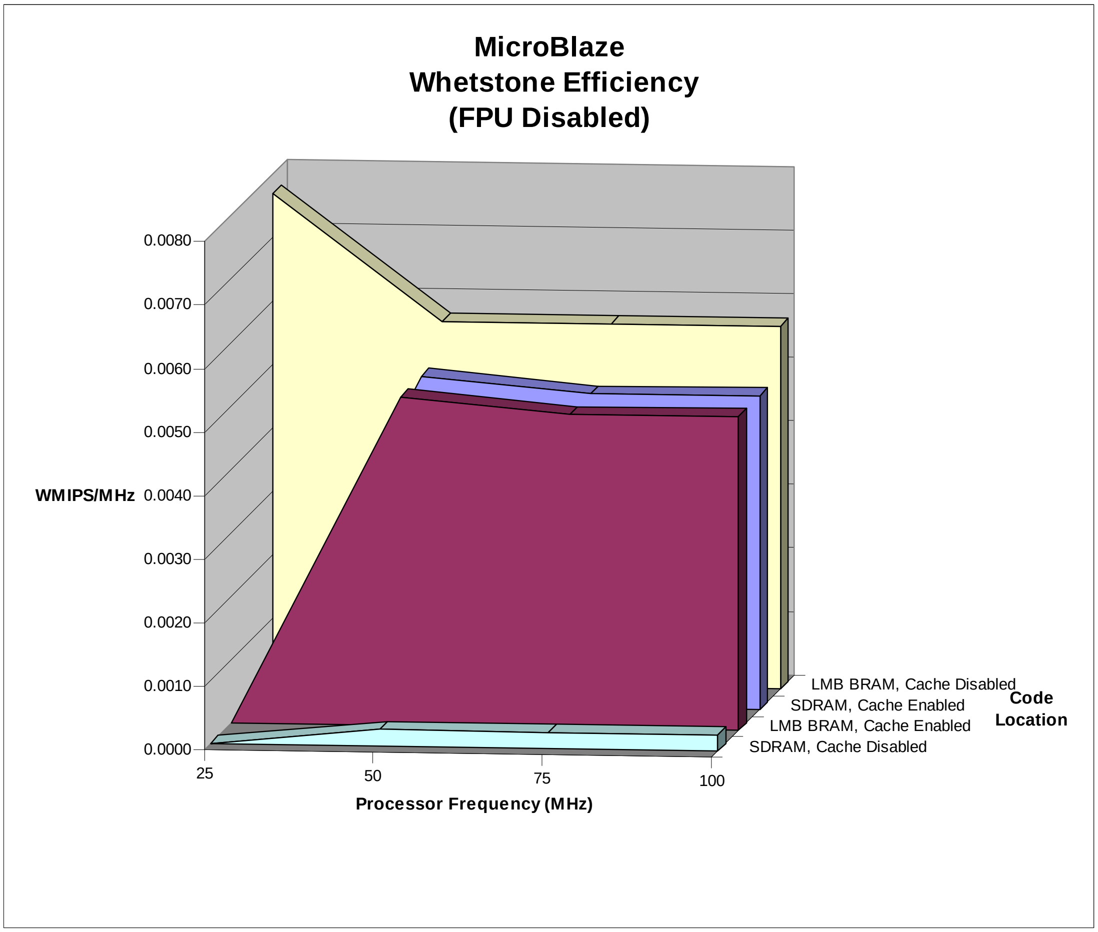



*Figure 10.  Virtex-4 MicroBlaze normalized Whetstone benchmark details, FPU disabled.*

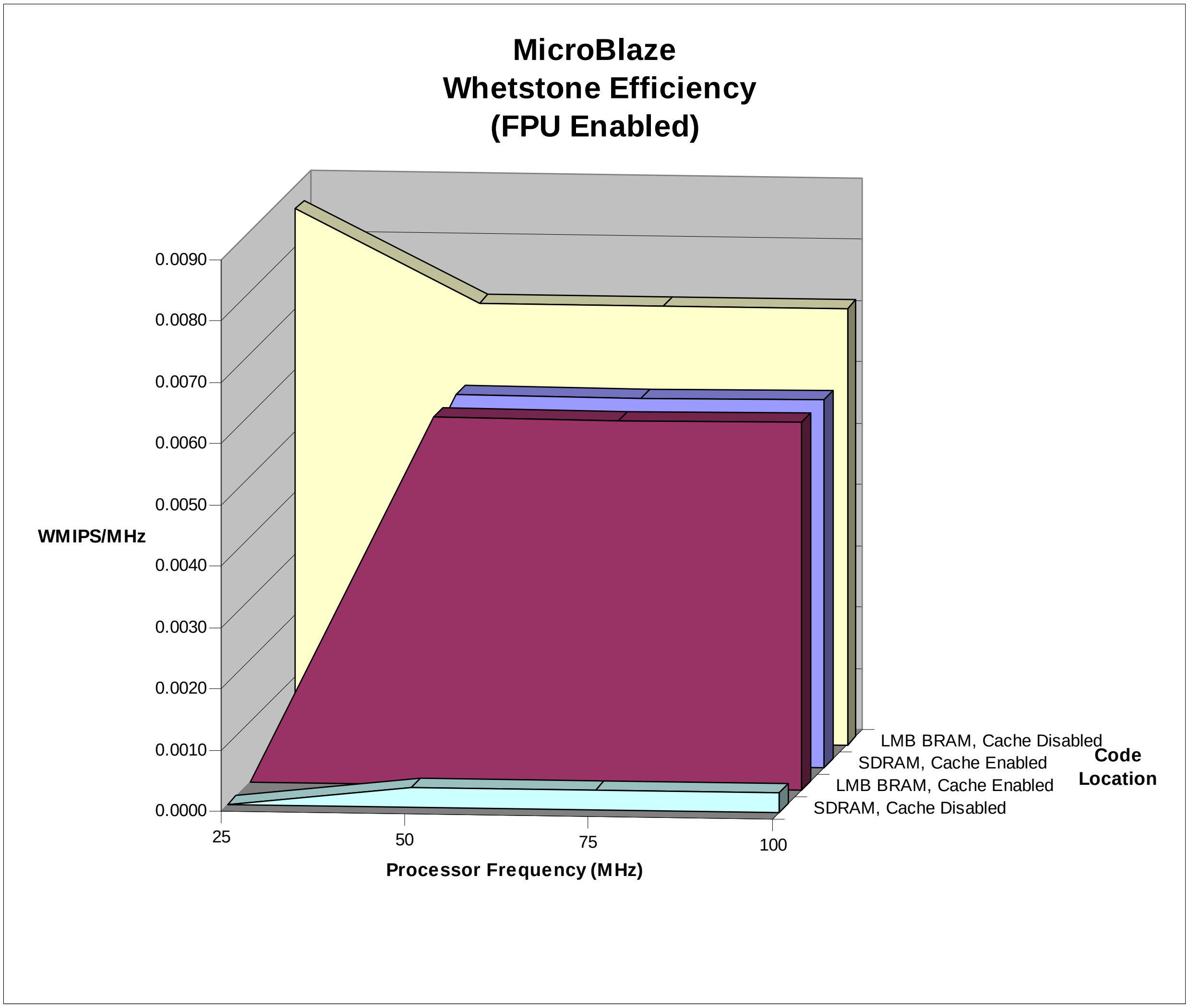



*Figure 11. Virtex-4 MicroBlaze normalized Whetstone benchmark details, FPU enabled.*

### *3.2.3 LEON3*

The Whetstone efficiency of the Leon processor was much higher than that of the MicroBlaze and the PPC. This anomaly was not fully investigated due to time constraints but should be investigated further. Some possible explanations: (1) the MicroBlaze C compiler may not have been generating machine code to take advantage of the hardware FPU, and (2) the timer on the LEON3 may not have been calibrated correctly, skewing the overall run times.

This section contains a summary of the LEON3 configuration used in the Whetstone benchmark.

The processor frequency is equal to the core frequency listed in Table 6.

The LEON3 has an ***extremely programmable*** cache size. For this test 16 Kbytes for data and 16 Kbytes for instruction cache were defined.

There are fewer memory configuration options for LEON3 than for MicroBlaze and Virtex-4 PPC405 processors for the ML-405 and ML-410 platforms; all LEON code was located in SDRAM for these tests. The LEON3 configuration utility is FPGA platform independent and does not know how to construct a processor memory block from the internal Virtex-4 BRAMs.

The "mv8"compiler switch allows the issuing of hardware multiply and divide instructions – this compiler switch was required for proper LEON FPU operation.

*Table 6. Virtex-4 LEON3 Whetstone Application Configuration and Memory Utilization.*

| Processor setup | | | | | | Single Precision FP Whetstone Scores | | | | | Application Size | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Processor** | **Processor Frequency (MHz)** | **mv8 Compile Switch** | **FPU** | **Cache** | **Code Location** | **# of loops** | **# of Iterations** | **Duration (sec)** | **Whetstones (MIPS)** | **WMIPS/MHz** | **.text** | **.data** | **.bss** | **Total Size of Executable** | **Speed-Up Due to FPU** | **Notes** |
| LEON | 25 | Disabled | Disabled | Disabled | SDRAM | 100 | 1 | | | | | | | | | Would not synthesize |
| LEON | 40 | Disabled | Disabled | Disabled | SDRAM | 100 | 1 | 61.157 | **0.164** | **0.0041** | 55104 | 2480 | 596 | 57584 | | |
| LEON | 50 | Disabled | Disabled | Disabled | SDRAM | 100 | 1 | 51.038 | **0.196** | **0.0039** | 55104 | 2480 | 596 | 57584 | | |
| LEON | 75 | Disabled | Disabled | Disabled | SDRAM | 100 | 1 | 39.999 | **0.250** | **0.0033** | 55104 | 2480 | 596 | 57584 | | |
| LEON | 25 | Disabled | Disabled | Enabled | SDRAM | 100 | 1 | | | | | | | | | Would not synthesize |
| LEON | 40 | Disabled | Disabled | Enabled | SDRAM | 100 | 1 | 14.232 | **0.703** | **0.0176** | 55104 | 2480 | 596 | 57584 | | |
| LEON | 50 | Disabled | Disabled | Enabled | SDRAM | 100 | 1 | 11.433 | **0.875** | **0.0175** | 55104 | 2480 | 596 | 57584 | | |
| LEON | 75 | Disabled | Disabled | Enabled | SDRAM | 100 | 1 | 7.658 | **1.306** | **0.0174** | 55104 | 2480 | 596 | 57584 | | |
| LEON | 25 | Disabled | Enabled | Enabled | SDRAM | 500 | 1 | | | | | | | | | Would not synthesize |
| LEON | 40 | Disabled | Enabled | Enabled | SDRAM | 500 | 1 | 2.452 | **20.392** | **0.5098** | 45648 | 2480 | 596 | 48128 | | # of loops increased to 500 |
| LEON | 50 | Disabled | Enabled | Enabled | SDRAM | 500 | 1 | 3.923 | **12.745** | **0.2549** | 45648 | 2480 | 596 | 48128 | | # of loops increased to 500 |
| LEON | 75 | Disabled | Enabled | Enabled | SDRAM | 500 | 1 | | | | | | | | | Would not meet timing |
| LEON | 25 | Enabled | Disabled | Disabled | SDRAM | 100 | 1 | | | | | | | | | Would not synthesize |
| LEON | 40 | Enabled | Disabled | Disabled | SDRAM | 100 | 1 | 53.085 | **0.188** | **0.0047** | 55056 | 2480 | 596 | 57536 | | |
| LEON | 50 | Enabled | Disabled | Disabled | SDRAM | 100 | 1 | 44.368 | **0.225** | **0.0045** | 55056 | 2480 | 596 | 57536 | | |
| LEON | 75 | Enabled | Disabled | Disabled | SDRAM | 100 | 1 | 31.719 | **0.315** | **0.0042** | 55056 | 2480 | 596 | 57536 | | |
| LEON | 25 | Enabled | Disabled | Enabled | SDRAM | 100 | 1 | | | | | | | | | Would not synthesize |
| LEON | 40 | Enabled | Disabled | Enabled | SDRAM | 100 | 1 | 11.117 | **0.900** | **0.0225** | 55056 | 2480 | 596 | 57536 | | |
| LEON | 50 | Enabled | Disabled | Enabled | SDRAM | 100 | 1 | 8.942 | **1.118** | **0.0224** | 55056 | 2480 | 596 | 57536 | | |
| LEON | 75 | Enabled | Disabled | Enabled | SDRAM | 100 | 1 | 5.997 | **1.668** | **0.0222** | 55056 | 2480 | 596 | 57536 | | |
| LEON | 25 | Enabled | Enabled | Enabled | SDRAM | 500 | 1 | | | | | | | | | Would not synthesize |
| LEON | 40 | Enabled | Enabled | Enabled | SDRAM | 500 | 1 | 2.066 | **24.201** | **0.6050** | 45536 | 2480 | 596 | 48016 | | # of loops increased to 500 |
| LEON | 50 | Enabled | Enabled | Enabled | SDRAM | 500 | 1 | 3.306 | **15.124** | **0.3025** | 45536 | 2480 | 596 | 48016 | | # of loops increased to 500 |
| LEON | 75 | Enabled | Enabled | Enabled | SDRAM | 500 | 1 | | | | | | | | | Would not meet timing |

## 3.3 Virtex-4 Resources

Figures 12 through 18 summarize the Virtex-4 FPGA resources consumed by the three different processors tested for the hardware configuration extremes (Cache and FPU enabled/disabled). These numbers are dependent on the processor configuration (peripherals) – the processors tested consisted of "default" configurations and may not be representative of a fully optimized hardware design.

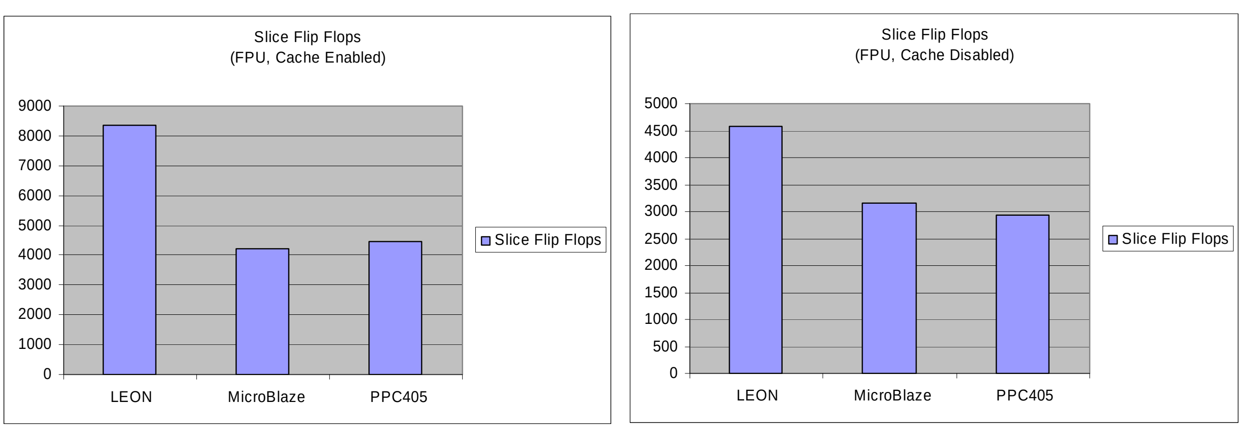



*Figure 12. Virtex-4 FPGA Resources: Slice Flip-Flops.*

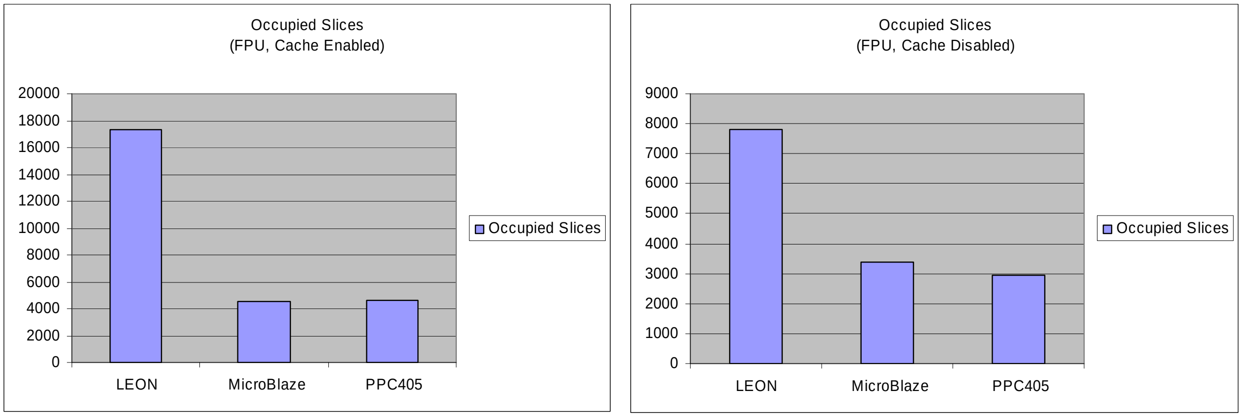



*Figure 13. Virtex-4 FPGA Resources: Occupied Slices.*

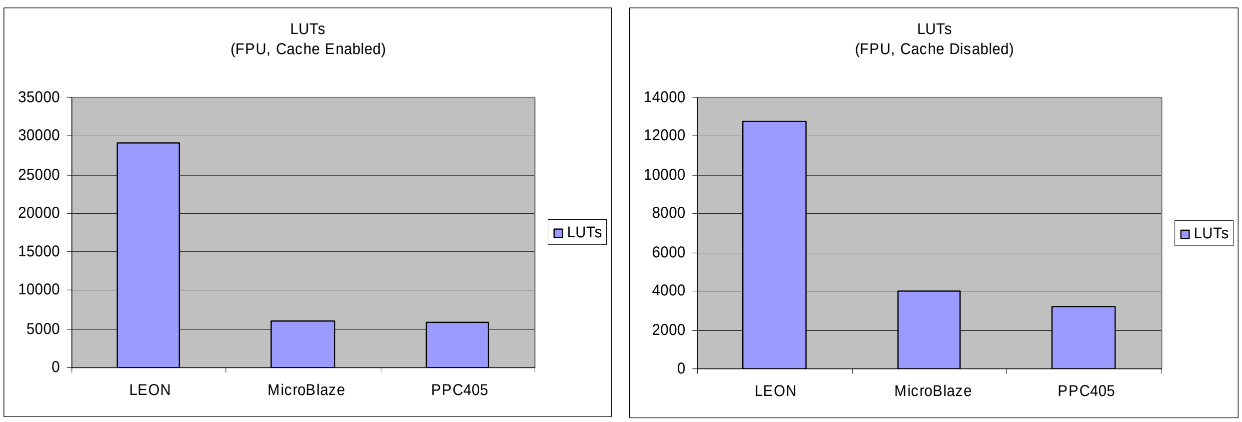



*Figure 14. Virtex-4 FPGA Resources: Lookup Tables.*

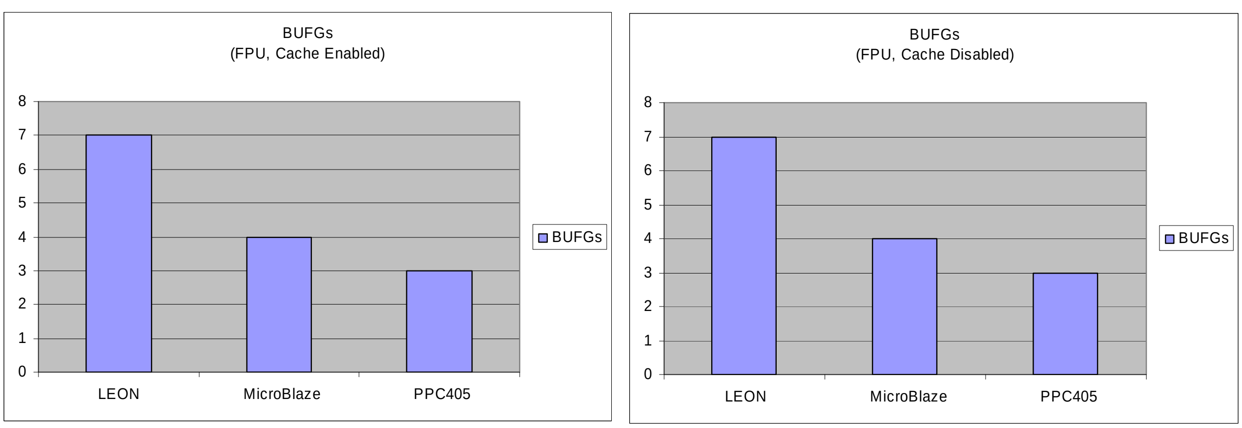



*Figure 15. Virtex-4 FPGA Resources: Clock Buffers.*

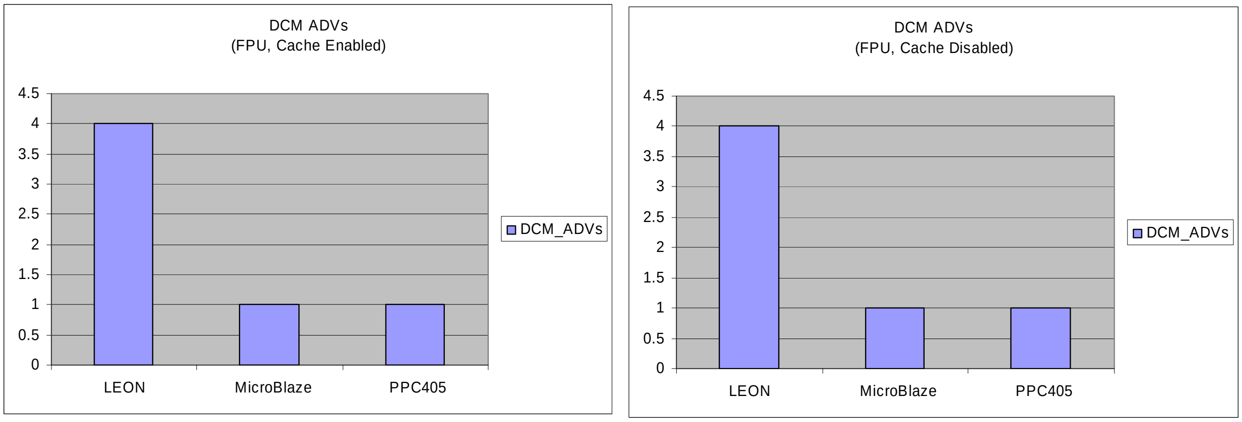



*Figure 16. Virtex-4 FPGA Resources: Digital Clock Managers.*

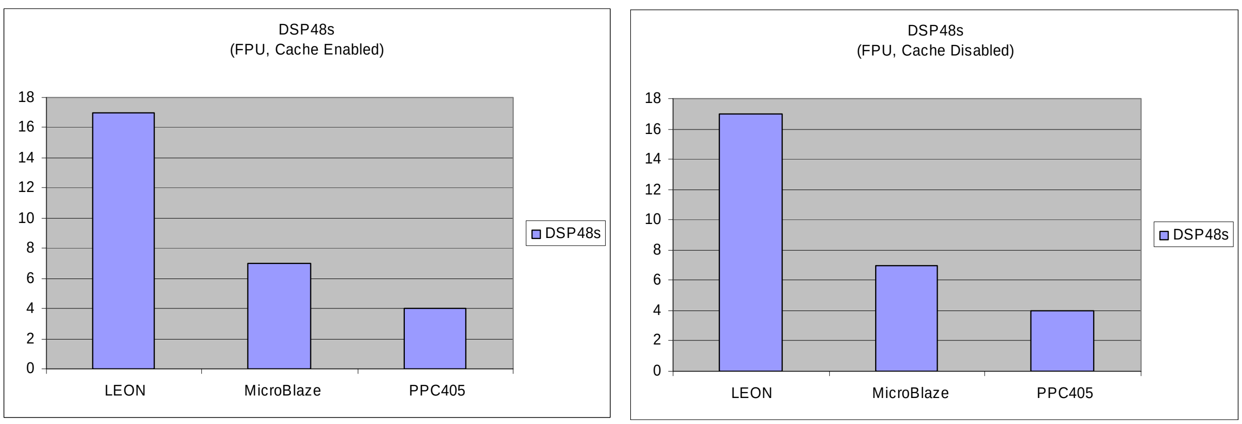



*Figure 17. Virtex-4 FPGA Resources: DSP Blocks.*

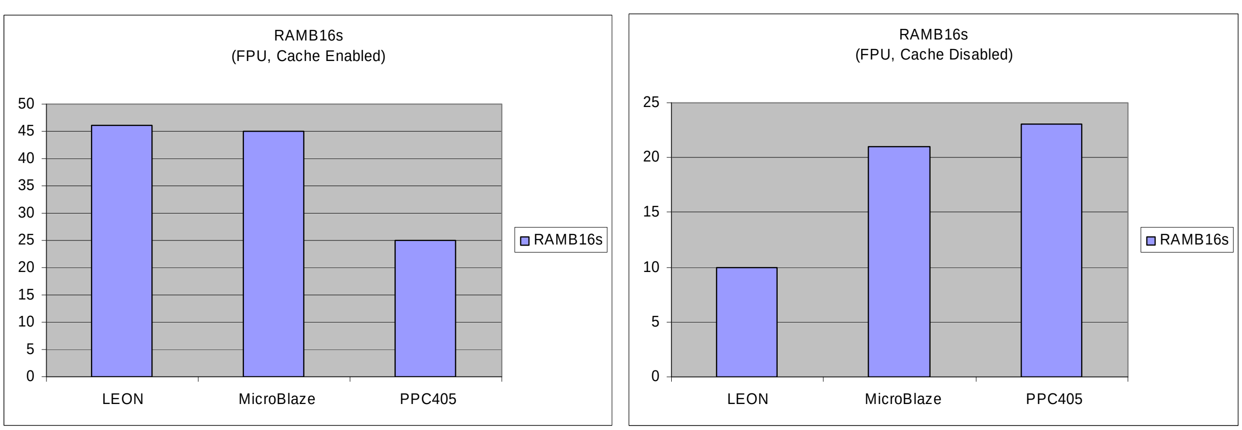



*Figure 18. Virtex-4 FPGA Resources: BRAMs.*

### *3.3.1 Virtex-4 PPC405*

This section and Table 7 contains a summary of the Virtex-4 FPGA resources consumed by the PPC405 configuration used in the Dhrystone and Whetstone benchmarks. Since the processor itself is a hard-core processor, FPGA resources are only needed to realize external "glue-logic" building blocks such as memory controllers and for peripherals such as Universal Asynchronous Receiver/Transmitters (UARTs). The FPU for the PPC405 was realized using FPGA resources – it is not part of the hard core itself.

The instruction and data caches for the PPC405 are internal to the hard core itself – no BRAM blocks are used in the cache structure. The PPC405 requires the use of internal BRAM to boot initially but is quite flexible in the number of internal and external memory configurations that are possible.

Several PPC405 design requirements drive how the processor memory map can be optimally defined and ultimately how to best use internal BRAM:

- The processor must boot from address 0xFFFFFFFC.
- The interrupt vector table must be aligned on a 64 Kbyte address boundary.
- The interrupt vector table length is 0x20C4 bytes long (8K + 196 bytes) and does not fit well within the address spaces definable through EDK Platform Studio (multiples of 4K, 8K, and 16K bytes).

One possible PPC405 memory architecture defines in BRAM the last 64 Kbyte memory space that includes the boot vector (0xFFFF0000 to 0xFFFFFFFF). This block could contain the interrupt vector table, the boot vector, and has some space left over for code or data. This configuration is problematic when considering the recommended BRAM single-event upset (SEU) mitigation scheme (see XAPP962), as this scheme requires a three-fold increase in BRAM resources for triple-mode redundancy. For an optimally configured PPC405 (interrupt vectors located in BRAM), the TMR requirements for the BRAMs will consume a large number of FPGA resources.

### *3.3.2 MicroBlaze*

This section and Table 8 contains a summary of the Virtex-4 FPGA resources consumed by the MicroBlaze configuration used in the Dhrystone and Whetstone benchmarks. Since the processor itself is a soft-core processor, FPGA resources are needed to realize the entire processor, caches, memory controllers, FPU, and peripherals.

*Table 7. Virtex-4 PPC405 System FPGA Resource Utilization.*

| Processor setup | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Processor | Processor Frequency (MHz) | FPU | Cache | Code Location | Slice Flip Flops | Occupied Slices | LUTs | BUFGs | DCM_ADVs | DSP48s | RAMB16s |
| PPC405 | 100 | Disabled | Disabled | PLB | | | | | | | |
| PPC405 | 200 | Disabled | Disabled | PLB | 710 | 786 | 728 | 2 | 1 | 0 | 32 |
| PPC405 | 300 | Disabled | Disabled | PLB | | | | | | | |
| PPC405 | 200 | Enabled | Disabled | PLB | 2236 | 2592 | 3464 | 2 | 1 | 4 | 34 |
| PPC405 | 100 | Disabled | Enabled | PLB | | | | | | | |
| PPC405 | 200 | Disabled | Enabled | PLB | 710 | 786 | 717 | 2 | 1 | 0 | 32 |
| PPC405 | 300 | Disabled | Enabled | PLB | | | | | | | |
| PPC405 | 200 | Enabled | Enabled | PLB | 2236 | 2592 | 3464 | 2 | 1 | 4 | 34 |
| PPC405 | 100 | Disabled | Disabled | OCM | 710 | 726 | 741 | 1 | 1 | 0 | 36 |
| PPC405 | 200 | Disabled | Disabled | OCM | | | | | | | |
| PPC405 | 300 | Disabled | Disabled | OCM | | | | | | | |
| PPC405 | 200 | Enabled | Disabled | OCM | 2234 | 2467 | 3488 | 2 | 1 | 4 | 38 |
| PPC405 | 100 | Disabled | Enabled | OCM | 708 | 726 | 741 | 3 | 1 | 0 | 36 |
| PPC405 | 200 | Disabled | Enabled | OCM | | | | | | | |
| PPC405 | 300 | Disabled | Enabled | OCM | | | | | | | |
| PPC405 | 200 | Enabled | Enabled | OCM | 2234 | 2467 | 3488 | 2 | 1 | 4 | 38 |
| PPC405 | 100 | Disabled | Disabled | SDRAM | 2925 | 2945 | 3188 | 3 | 1 | 0 | 23 |
| PPC405 | 200 | Disabled | Disabled | SDRAM | 2925 | 2945 | 3188 | 3 | 1 | 0 | 23 |
| PPC405 | 300 | Disabled | Disabled | SDRAM | | | | | | | |
| PPC405 | 200 | Enabled | Disabled | SDRAM | 4451 | 4637 | 5935 | 3 | 1 | 4 | 25 |
| PPC405 | 100 | Disabled | Enabled | SDRAM | 2925 | 2945 | 3188 | 3 | 1 | 0 | 23 |
| PPC405 | 200 | Disabled | Enabled | SDRAM | | | | | | | |
| PPC405 | 300 | Disabled | Enabled | SDRAM | | | | | | | |
| PPC405 | 200 | Enabled | Enabled | SDRAM | 4451 | 4637 | 5935 | 3 | 1 | 4 | 25 |
| PPC405 | 200 | Disabled | Disabled | OPBRAM | | | | | | | |
| PPC405 | 200 | Disabled | Enabled | OPBRAM | | | | | | | |

*Table 8. Virtex-4 MicroBlaze System FPGA Resource Utilization.*

| Processor setup | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Processor | Processor Frequency (MHz) | FPU | Cache | Code Location | Slice Flip Flops | Occupied Slices | LUTs | BUFGs | DCM_ADVs | DSP48s | RAMB16s |
| MB | 75 | Enabled | Disabled | LMB | 1901 | 2604 | 3203 | 3 | 1 | 7 | 48 |
| MB | 100 | Enabled | Disabled | LMB | 1902 | 2607 | 2497 | 2 | 1 | 7 | 48 |
| MB | 25 | Disabled | Disabled | SDRAM | | | | | | | |
| MB | 50 | Disabled | Disabled | SDRAM | | | | | | | |
| MB | 75 | Disabled | Disabled | SDRAM | | | | | | | |
| MB | 100 | Disabled | Disabled | SDRAM | 3153 | 3382 | 4036 | 4 | 1 | 3 | 21 |
| MB | 25 | Enabled | Disabled | SDRAM | | | | | | | |
| MB | 50 | Enabled | Disabled | SDRAM | | | | | | | |
| MB | 75 | Enabled | Disabled | SDRAM | | | | | | | |
| MB | 100 | Enabled | Disabled | SDRAM | 3590 | 3872 | 4972 | 4 | 1 | 7 | 21 |
| MB | 25 | Disabled | Enabled | SDRAM | | | | | | | |
| MB | 50 | Disabled | Enabled | SDRAM | | | | | | | |
| MB | 75 | Disabled | Enabled | SDRAM | | | | | | | |
| MB | 100 | Disabled | Enabled | SDRAM | 3890 | 4130 | 5161 | 4 | 1 | 3 | 45 |
| MB | 25 | Enabled | Enabled | SDRAM | | | | | | | |
| MB | 50 | Enabled | Enabled | SDRAM | | | | | | | |
| MB | 75 | Enabled | Enabled | SDRAM | | | | | | | |
| MB | 100 | Enabled | Enabled | SDRAM | 4238 | 4571 | 6068 | 4 | 1 | 7 | 45 |

### *3.3.3 LEON3*

This section and Table 9 contains a summary of the Virtex-4 FPGA resources consumed by the LEON configuration used in the Dhrystone and Whetstone benchmarks. Since the processor itself is a soft-core processor, FPGA resources are needed to realize the entire processor, caches, memory controllers, FPU, and peripherals.

The LEON processor was the last evaluated. The LEON design with an FPU was too large to fit into the ML-405 (containing an FX20 device) development board used for the PPC and MicroBlaze evaluations. A larger device, the FX60, was necessary to fit the LEON-based design – the ML-410 board was used for all subsequent LEON tests.

These utilization statistics were taken from the leon3mp.mrp document.

Note: *75 MHz designs did not meet all timing constraints but executed the Dhrystone benchmarks correctly.

*Table 9. Virtex-4 LEON3 System FPGA Resource Utilization.*

| Processor setup | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Processor** | **Processor Frequency (MHz)** | **FPU** | **Cache** | **Code Location** | **Slice Flip Flops** | **Occupied Slices** | **LUTs** | **BUFGs** | **DCM_ADVs** | **DSP48s** | **RAMB16s** |
| LEON | 40 | Enabled | Enabled | SDRAM | 8357 | 17300 | 29129 | 7 | 4 | 17 | 46 |
| LEON | 50 | Enabled | Enabled | SDRAM | 8355 | 17292 | 29119 | 7 | 4 | 17 | 46 |
| LEON | *75 | Enabled | Enabled | SDRAM | | | | | | | |
| LEON | 40 | Disabled | Enabled | SDRAM | 5270 | 8542 | 14880 | 7 | 4 | 1 | 30 |
| LEON | 50 | Disabled | Enabled | SDRAM | 5268 | 8542 | 14889 | 7 | 4 | 1 | 30 |
| LEON | *75 | Disabled | Enabled | SDRAM | 5270 | 8542 | 14878 | 7 | 4 | 1 | 30 |
| LEON | 40 | Disabled | Disabled | SDRAM | 4569 | 7817 | 12744 | 7 | 4 | 1 | 10 |
| LEON | 50 | Disabled | Disabled | SDRAM | 4567 | 7889 | 12820 | 7 | 4 | 1 | 10 |
| LEON | *75 | Disabled | Disabled | SDRAM | 4569 | 7814 | 12741 | 7 | 4 | 1 | 10 |

## 3.4 Virtex-5 FX130T Resources

Since the target FPGA architecture for node-based design is the Xilinx Virtex-5 FX130T (SIRF) device, ***rough*** estimates for FPGA resources consumed by single-string soft-core processors (LEON and MicroBlaze in Tables 10 and 11, respectively) are included below for this device:

*Table 10. Device Utilization Estimates for LEON3 System on Virtex-5 FX130T, Cache and FPU Enabled.*

| | | |
|---|---|---|
| Digital Clock Managers | 4 out of 12 | 33% |
| Block RAMs | 48 out of 596 | 8% |
| Flip-Flops | 8357 out of 81920 | 10% |
| 6-input Lookup Tables | 29129 out of 81920 | 36% |

*Table 11. Device Utilization Estimates for MicroBlaze System on Virtex-5 FX130T, Cache and FPU Enabled.*

| | | |
|---|---|---|
| Digital Clock Managers | 1 out of 12 | 8% |
| Block RAMs | 45 out of 596 | 7% |
| Flip-Flops | 4238 out of 81920 | 5% |
| 6-input Lookup Tables | 6068 out of 81920 | 7% |

The PPC440 processor is an embedded hard core within the Virtex-5 FX130T FPGA. Since the external fabric of the PPC440 processor is so much different than that of the PPC405, it is expected that Virtex-4 PPC405 resource utilization estimates do not map nicely to Virtex-5 PPC440 designs.

# 4. RADIATION EFFECTS MITIGATION

Radiation effects mitigation is applied at the ***system*** level through:

- Shielding
- Subsystem redundancy (A/B or M-of-N)
- Fault-tolerant hardware and software architectures.

At the ***circuit*** level, mitigation is applied through:

- Error detection and correction (EDAC)
- Triple mode redundancy (TMR)

***Device***-level mitigation can include some of the same system and circuit techniques (on a smaller scale) but emerging systems will also include

- Radiation-hardened-by-design components

A robust system typically requires the use of multiple mitigation strategies at more than one level and is based upon several system-level characteristics:

- The orbit of the system (radiation environment)
- The required availability of the system
- The criticality of data processed by the system

The tolerable upset rate of the ***system*** will drive what mitigation strategies should be applied. This section discusses how each of the three processors evaluated could be mitigated at the ***device*** level.

The reprogrammable FPGA targeted for the NBA is the Xilinx SIRF device, a radiation-hardened-by-design Static Random Access Memory (SRAM) device based on the commercial off-the-shelf (COTS) Xilinx Virtex-5 FX130T. The SIRF device is still under development but is currently expected to be available in the first quarter of 2010. NBA developers can begin designing now with the COTS equivalent and then incorporate the SIRF device into their designs when it becomes available.

Currently the SIRF development effort (Phase 3, FX-1 single-event effect (SEE) Hardening) is targeted to eliminate the device configuration errors (and therefore device scrubbing as mitigation) that upset SRAM-based FPGAs when operated in radiation environments – this includes the Virtex-4QV Space-Grade FPGA. Comprehensive testing of the device under static and dynamic operating environments will follow. Once the device configuration hardening has been validated, Phase 4, FX-2 of the development cycle will commence. Phase 4 will include characterizing the performance of and developing mitigation strategies for the internal FPGA fabric elements. At the end of Phase 4, feasible enhancements to the fabric elements (DSP, BRAM, CMT, PPC, and MGT) will be applied, leading to the commercial production of the SIRF device.

SNL is currently positioned to help develop mitigation strategies for the SIRF device through its involvement in the XRTC. ***It is highly recommended that SNL continue to place a high priority on its involvement in XRTC activities***.

The Virtex-4QV Space-Grade FPGA is not a radiation-hardened-by-design device. It suffers from configuration error upsets and must be mitigated through configuration readback and scrubbing, unlike the SIRF device. Xilinx application note XAPP988 details how to mitigate the Virtex-4 configuration memory.

There are two main steps to mitigating a Virtex-4-based processor design:

- Mitigating the configuration of the Virtex-4 itself through readback and scrubbing.
    - The scrub rate should be 10x the expected (calculated) upset rate.
    - The SEU rate should be at or below the single-event functional interrupt (SEFI) rate.
    - There are four Virtex-4 configuration interfaces:
        - SelectMAP: One must continually clock the TCK line and hold TMS to ‘1’ to keep JTAG in the test logic reset state. The SelectMap 32-bit data interface has 4x the SEFI cross section of the 8-bit SelectMap interface but is obviously faster.
        - Serial (do not use if scrubbing is needed as there is no readback support).
        - JTAG is the most robust mode but alignment is more complex.
        - ICAP (avoid ICAP if you need the most robust design).

- Mitigating the FPGA fabric involving and surrounding the processor using TMR.
    - TMR mitigates against errors between configuration scrub cycles.
    - TMR also mitigates against logic upsets.

Device readback is required to determine if there are problems in the V4 Configuration Status Register (see p. 6-20 of the ***TMRTool Beta*** book). If the GTS_CFG_B bit (5) is cleared all outputs have been tri-stated; it is necessary to pulse the PROG pin to recover. In fact, if any bits inside of the configuration status register toggle after the original device configuration, a SEFI has occurred – pulsing the PROG pin will restore the device.

The following sections discuss processor-specific applications and notes of interest.

## 4.1 Virtex-4 PPC405

Xilinx is currently beam testing the Virtex-4 PPC405 processor and will publish a device cross section at a later time. Xilinx application note XAPP1004 describes how to mitigate a PPC405-based design *with the exception of the processor cache.*

Earlier sections of this document have shown that the performance of the PPC405 processor increases dramatically with usage of cache. It is therefore desirable to have it cache available and enabled for operationally intensive applications. The PPC405 processor cache (16 kB each of instruction and data) is implemented as part of the PPC405 core itself and is not part of the FPGA fabric and has been described by Gary Swift (Xilinx radiation effects expert) as possibly the part of the Virtex-4 device most susceptible to radiation-induced upsets.

In developing a mitigation scheme for the Virtex-4 PPC405 cache, Xilinx encountered some issues with the instruction cache that were then given to SNL to investigate. This mitigation scheme included the use of hardware-generated parity error detection (no correction) within the PPC405 core to trigger software-based flushing of instruction and data caches before corrupted information could be used by the processor. This mitigation scheme works well for the PPC405 data cache but fails when applied to the instruction cache. Results from the SNL investigation indicate a possible PPC405 core defect in that the parity calculation for the instruction cache deterministically generates incorrect parity values. At the time of this writing, an alternate mitigation scheme has not yet been identified.

Below is a short description of how the mitigation scheme was designed to operate:

- The memory management unit (MMU) and Transition Look-Aside Buffer are disabled. It is unclear (but doubtful) whether this mitigation scheme will work with an operating system that requires an MMU.
- The following system elements should reside in uncached memory space. This will cause a degradation in performance but is necessary to ensure proper operation.
    - System stack.
    - System heap.
    - Exception vector table.
- A parity error in either the instruction or data caches of the PPC405 will trigger a machine check exception.
- The machine exception service routine determines whether a data parity fault or instruction parity fault has occurred.
    - If a data parity fault has occurred: invalidate the entire data cache using the ***dcbf*** or ***dcbi*** instructions.
    - If an instruction parity fault has occurred: invalidate the entire instruction cache using ***iccci*** instruction.

## 4.2 Virtex-4 MicroBlaze

Xilinx is currently developing a fault-injector application to simulate configuration errors in the Virtex-4 FPGA fabric that includes the elements that comprise the MicroBlaze soft core processor. Xilinx is also developing a TMRed version of the MicroBlaze processor and is validating the operation of the TMR logic by using the configuration fault injector. The Xilinx TMRTool is being used to convert a single-string MicroBlaze design into a triplicated version.

As of the end of July 2008, there are still some design issues to resolve as the triplicated MicroBlaze processor design still experiences some problems when subjected to the fault injector.

Once the TMRed version of the MicroBlaze has been validated using the fault injector, it will be subjected to beam testing and a device cross section will be published.

## 4.3 Virtex-4 LEON3

The fault tolerant version of the LEON core is only fault-tolerant on FPGA devices that are radiation hardened by design, e.g., Actel RTAX, RHAX. The fault-tolerant core essentially only adds error correction codes on the SRAM elements of an Actel FPGA. Since the other logic elements of an Actel FPGA are mitigated by design within the FPGA itself, there is no mitigation to any other logic elements of the core. Therefore, the fault-tolerant version of the LEON core is not necessarily fault-tolerant when implemented in the Xilinx Virtex-4 FPGA.

For use in the Virtex-4 device, the non-fault-tolerant core used in this evaluation would have to be mitigated using TMRTool or the like. Since this core is not associated in any way with Xilinx, this exercise would be left entirely up to the individual developers.

## 4.4 Virtex-5 (SIRF) PPC440

Only the Xilinx-controlled IP of the SIRF device will be made radiation hardened by design – this excludes the PPC440 cores (which are IBM IP). The PPC440 processors will be available for use in the SIRF device, but just how vulnerable they will be to radiation-induced upsets is unknown. Xilinx expects to begin beam testing and characterizing the SIRF device at the end of 2008. Greg Miller and Gary Swift from Xilinx are the points of contact for the XRTC that handle CPU mitigation and testing.

Commercial-grade Virtex-5 FX boards are just now becoming available (July 2008), too late to be included in this evaluation effort. While Greg Miller from Xilinx has been assured by the microprocessor development group at Xilinx that the cache parity error detection logic functions correctly on theVirtex-5 PPC440 processor, this has yet to be independently confirmed.

## 4.5 Virtex-5 (SIRF) MicroBlaze

It is expected that once the TMRed version of the MicroBlaze is available and tested for Virtex-4 that the same techniques can be used for a Virtex-5 deployment. The radiation tolerance of SIRF internals such as flip-flops and look-up tables is ***expected*** to be better than that of the Virtex-4QV space-grade devices, but that has yet to be proven; internal mitigation such as TMR may still be required.

## 4.6 Virtex-5 (SIRF) LEON3

Since the SEE performance of SIRF fabric elements (DSP, PBRAM, CMT, MGT, etc.) has yet to be determined, it is unknown whether or not the fault-tolerant version of the LEON processor will indeed be fault-tolerant on the SIRF device. Like the Virtex-5 (SIRF) MicroBlaze, TMR may still be required to mitigate radiation effects.

# 5. SIZE, WEIGHT, AND POWER

NBA design holds the promise of reducing ***system*** size and weight through M-of-N redundancy as opposed to A/B redundancy. At the board level, FPGA-hosted processors can help reduce size and weight because they can be combined with peripherals and glue logic that are typically realized in separate devices.

Mitigation strategies (configuration scrubbing and TMR) for reconfigurable FPGA-hosted processors of course add back in some size, weight, and power. Using the Xilinx TMR tool incurs approximately a 3.2x resource overhead. SRL16 replacements are recommended for Virtex-4 designs, which will add some additional overhead. Page 3-31 of TMRTool Beta states "in V4, SRL16 does not necessarily have to be replaced" if data is constantly moving through the register – a design-dependent condition.

The development boards (ML-405, ML-410) used in these evaluations were not configured with power monitors on the FPGA supply pins, making it impossible to separate out the power consumed by the processor portion of the design from all of the other circuitry on the board. DS302 from Xilinx lists the typical power dissipation of the PPC405 processor block as 0.45 mW/MHz.

It is highly recommended that future processor evaluation efforts using the Virtex-5 device make an effort to isolate the FPGA power supplies for processor power measurements.

# 6. DEVELOPMENT TOOLS

For this evaluation, all tools were hosted on Windows XP Professional, Service Pack 2. All of the tools used to define, synthesize, and debug the hardware and develop and debug the software can also be hosted on Linux systems.

It is recommended by Xilinx developers that a 64-bit operating system (currently only 64-bit Linux OS is supported by Xilinx development tools) be used for Virtex-5 development.

## 6.1 Tool Pricing

Pricing for Xilinx tools Version 10.1 as of press time is included in this section even though Version 9.2 was used in this effort. Version 10.1 was released at the end of this effort. Development for Virtex-5 PPC440 processors will require Version 10.1, service pack 2. MicroBlaze development on Virtex-5 is possible with ISE/EDK Version 9.2.

The LEON processor used in these evaluations was the non-fault-tolerant open-source version that is available for evaluation off of the Gaisler web site. A Spartan3 LEON development board from Gaisler (GR-XC3S-1500, price EUR 750) was the initial starting point for the LEON evaluations.

Xilinx ISE Foundation Edition 10.1 – $2,500
Or
Xilinx ISE Foundation Edition with ISE Simulator 10.1 – $3,500

ISE Foundation Edition ships with ISE Simulator Lite, limited to 50,000 lines of source hardware description language (HDL). The full-featured version of ISE Simulator supports any HDL design density.

Xilinx ChipScope Pro 10.1 – $700
Or
Xilinx ChipScope Pro Tool with USB Cable 10.1 – $850

Xilinx Platform Studio and the Embedded Development Kit 10.1 – $500

In addition, the LEON processor requires several additional expenditures:

| | |
|---|---|
| GRMON | - ~$9,000 + maintenance |
| GRFPU | - ~$30,000 (fault-tolerant) or<br>- ~$16,000 (single-string) |
| GRLIB | - ~$63,000 (fault-tolerant) or<br>- ~$32,000 (single-string) |

## 6.2 Processor/System Definition

### *6.2.1 PPC405 and MicroBlaze*

#### 6.2.1.1 Core Configuration

Both the Virtex-4 PPC405 and Microblaze processor-based systems are defined by the Xilinx Platform Studio (XPS) tools that are included with the Xilinx EDK. EDK Version 9.2 was used for the evaluation of PPC405 and MicroBlaze processors on the Virtex-4 FPGA.

XPS contains a "Base System Builder" wizard and the name is accurate – the tool can be used to define just a basic system. Systems that contain hardware and software definitions that differ from a very basic configuration will require manual editing of the Microprocessor Hardware Specification (MHS) and Microprocessor Software Specification (MSS) files. This is perhaps the trickiest step in defining a PPC or MicroBlaze based system.

#### 6.2.1.2 Core Implementation

The XPS graphical user interface is used to generate the HDL files (in netlist format) and libraries that define the PPC and MicroBlaze processor systems. XPS will "stitch" together all of the IP based upon connections described in the MHS file. This is a rather trivial (but still time-consuming) step once the MHS file is defined correctly.

### *6.2.2 LEON3*

#### 6.2.2.1 Core Configuration

The LEON processor core is configured using a script-based graphical tool, *xconfig*. This tool allows the user to customize all configurable aspects of the LEON processor.

Main configurable parameters include:

- Processor and co-processors (FPU)
- Instruction and Data Caches
    - Associativity (sets)
    - Set size
    - Line size
    - Replacement algorithm type
- Memory Controllers
    - External asynchronous
    - SDRAM
- Peripheral Controllers
    - Interrupt Controller
    - Watchdog
    - Ethernet controller
    - PCI controller
- Debug Support Unit
- PCI Interface

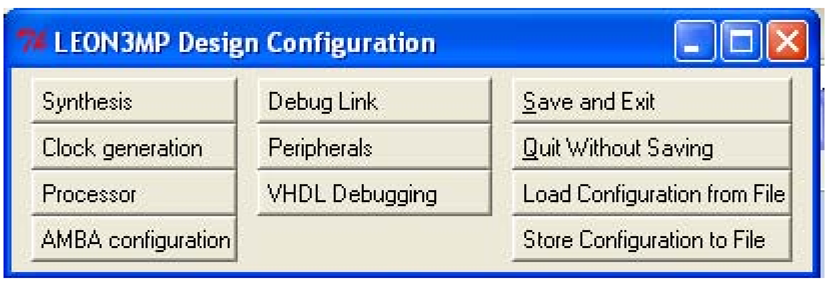
- Fault Tolerance
- Boot Options
    - Memory read/write wait states
    - UART Baud rate
    - Processor clock frequency

A portion of the following steps were taken from the GR-XC3S-1500 Development Board User Manual. NOTE: The VHDL file, leon3mp.vhd, may need modification when migrating to custom board designs. (This file was modified to target both the ML-405 and ML-410 boards.) This file is a wrapper for the LEON microprocessor design and also contains customizations needed on a per board basis. These steps are discussed in a later section.

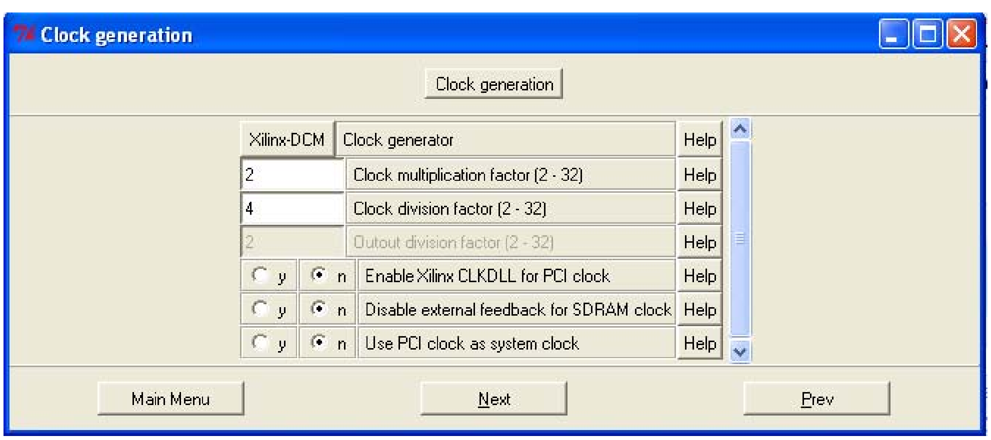
1. In the console window, change to the directory where the model has been unzipped and change to the subdirectory *designs/leon3-gr-xc3s-1500.*

2. Type the "*make xgrlib*" command to run a script that automatically runs a simple graphical interface.

3. Click the "*xconfig*" button. This will launch a graphical tool showing various subsystems for the model as shown below.




4. Selecting any of the subsystems brings up another window with detailed configuration options. For example, shown below is the clock-generation graphical user interface (GUI).



After any configuration changes, click "*Save and Exit*" in the Design Configuration window to finalize the modifications. The core is now ready for implementation.

#### 6.2.2.2 Core Implementation

Download and extract the LEON3 and GRLIB IP. The version being used during the creation of this document is 1.0.17-b2710 along with the GR-XC2S-1500 development board.

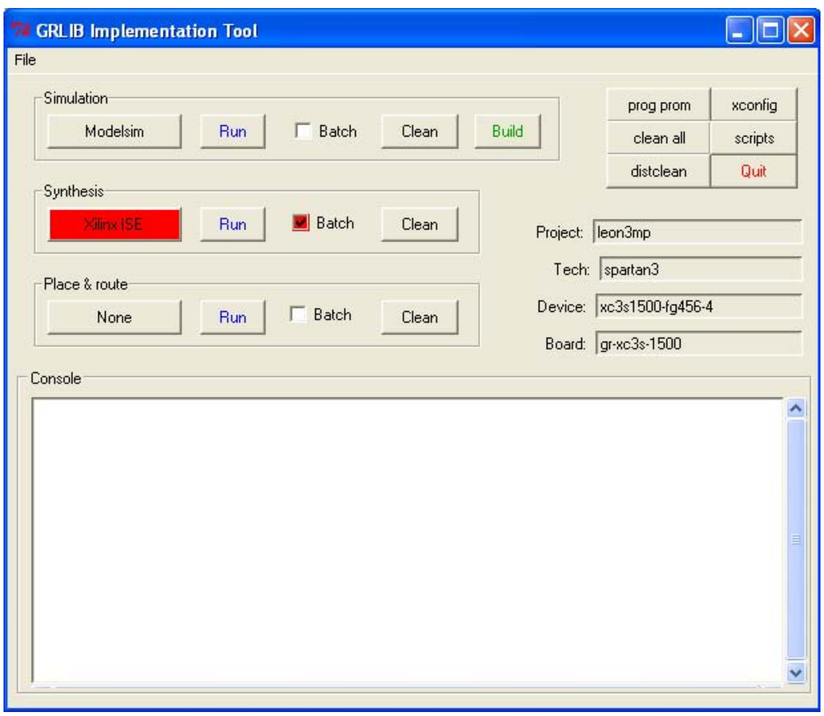
Steps taken from GR-XC3S-1500 Development Board User Manual:

1. Unzip the GRLIB VHDL model to the directory you wish to use.

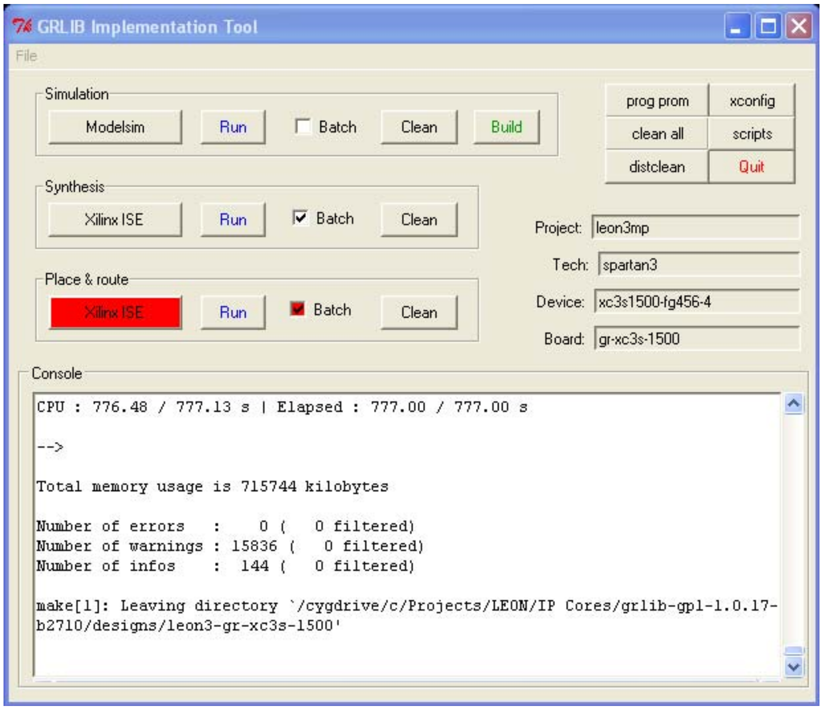
2. In the console window, change to the directory where the model has been unzipped and change to the subdirectory *designs/leon3-gr-xc3s-1500*

3. Type the "*make xgrlib*" command to run a script that automatically runs a simple graphical interface.

4. Select "*Xilinx ISE*" from the synthesis menu. **NOTE**: It is also useful to select the "*Batch*" checkbox. Click "*Run*" to perform the synthesis. This is shown below.



5. Select "*Xilinx ISE*" from the Place & Route menu. **NOTE**: It is also useful to select the "*Batch*" checkbox. Click "*Run*" to perform the place and route. This is shown below.




6. Press "*prog prom*" on the Implementation Tool GUI to program the on-board PROM device. This step will program the device if the board is powered and the programmer is attached.

## 6.3 Synthesis

### *6.3.1 PPC405 and MicroBlaze*

The Xilinx development tools were used exclusively to synthesize the PPC405 and MicroBlaze processor systems – other design flows are supported by third-party tools such as Synplicity Synplify but were not evaluated as part of this effort.

### *6.3.2 LEON3*

The LEON system can be synthesized using a number of tools depending upon the target platform. For the Virtex-4 target, Synplicity Synplify and Xilinx ISE can be used for synthesis. However, Gaisler Research does not guarantee correct operation of their FPU if Synplify is not used.[1] Place and route is accomplished using Xilinx ISE. These tools are widely available and easy to operate. Hardware debugging can be easily accomplished on the Virtex-4 devices using the Xilinx ChipScope tool.

[1] Gaisler Research FAQ, http://www.gaisler.com/cms/index.php?option=com_content&task=view&id=85&Itemid=63

## 6.4 Software Development

### *6.4.1 PPC405 and MicroBlaze*

The PPC 405 processor is supported by many software development tool vendors. Because the MicroBlaze is Xilinx IP, not many software development options are available besides the Xilinx Embedded Development Kit. This effort utilized the EDK tools exclusively for developing software for the PPC405 and MicroBlaze processors.

The Xilinx EDK contains PPC and MicroBlaze software development tools based on GNU compiler tools and two different debugging environments. An Eclipse - based IDE is the basis of the Software Development Kit and a Xilinx also includes the Xilinx Microprocessor Debugger interface, which contains some nice “backdoor” access points to these processors that were used extensively.

The hardware and software development tools are closely coupled from within EDK and are accessed from menu items within the XPS interface.

### *6.4.2 LEON3*

Software development is accomplished using an Eclipse IDE plug-in (GRTools) or using command line tools. This section describes the use of the LEON3 command line toolset. However, the underlying tools are the same regardless of whether the Eclipse IDE or the command line is being used. The compiler used is bcc (Bare C Compiler). Bcc is a cross-compiler for LEON processors based upon the GNU compiler tools and the Newlib standalone C-library. The debug monitor used is GRMON. GRMON supports two operating modes: command-line mode and GDB mode. This allows GRMON to accept commands manually through a terminal window or act as a GDB gateway. The Eclipse plug-in streamlines the debugging interface, allowing easy control for operations such as setting breakpoints, inspecting the stack, etc.

The hardware and software environments are completely decoupled, with no interaction between the tool chains.

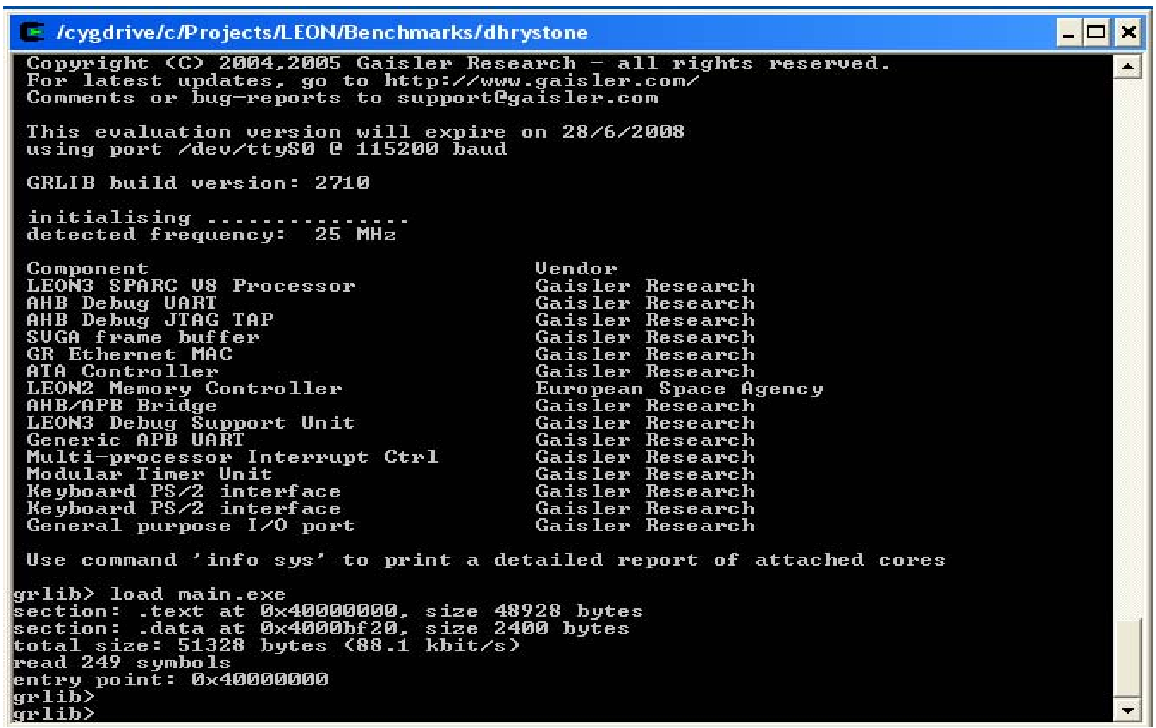
#### 6.4.2.1 Executing Benchmark Applications

This section lists the steps to download an application via the UART debug interface and execute from SRAM. This example is executed from the application directory. The Whetstone and Dhrystone benchmarks are stored in the Benchmarks/whetstone and Benchmarks/dhrystone directories respectively. The source files and makefile for each benchmark is stored in its respective directory.

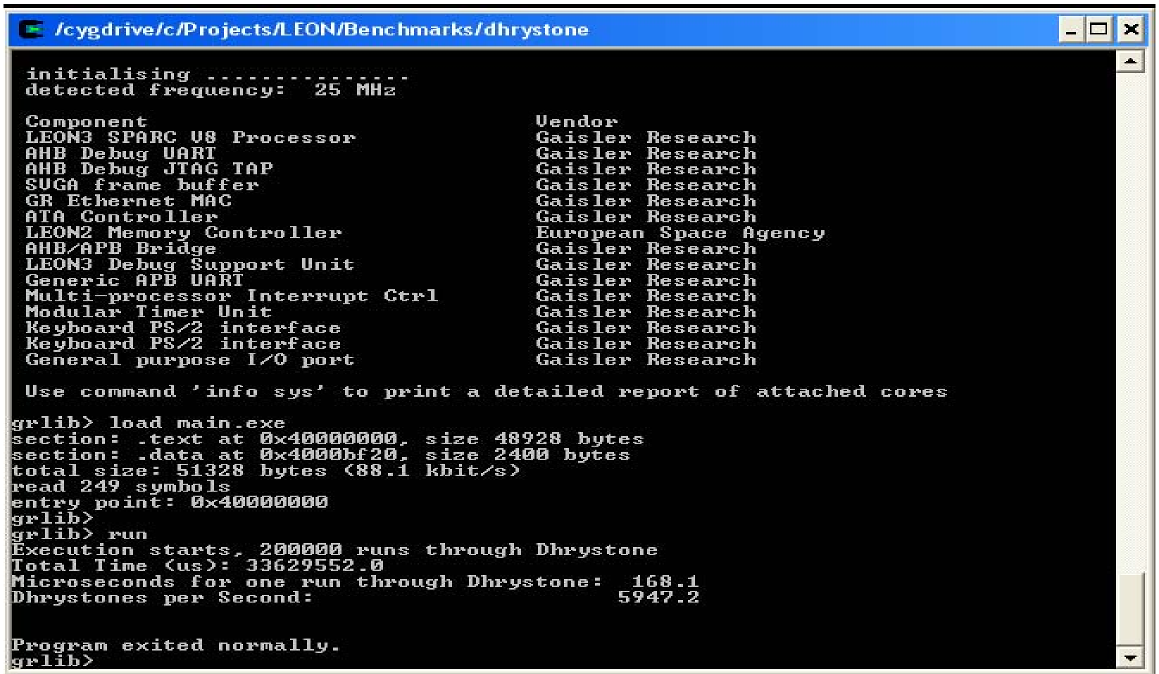
1. Connect to the system using the GRMON application.  The following options are used:
    a. –grlib                      because this a LEON3 processor
    b. –uart /dev/ttyS0     using COM1
    c. –baud 115200           select the baud rate
    d. –i                           initialize the target
    e. –u                          loopback UART so printf goes to GRMON console

   **NOTE:** The –nb option should be used if your application installs an exception handler. This will instruct GRMON to avoid going into break mode on a page fault or data exception.

2. The debugger is now connected.  In this example, the desired application is main.exe. Type "load main.exe" to load the application into system memory.  This is shown below.



3. Execute the application by typing “run.”




## 6.5 Debugging Tools

All three processors utilized JTAG debugger cables for FPGA configuration, code download, and code debugging.

The parallel port JTAG debugger cable from Digilentinc.com that ships with the Gaisler Research GR-XC3S-1500 development kit was used for the LEON processor.

The Xilinx Platform USB Cable (P/N: HW-USB-G) was utilized for both the MicroBlaze and PPC processors.

## 6.6 Operating Systems

All benchmark applications were developed as standalone applications (bare processor executables); no operating systems were used by the benchmarks nor were they evaluated as part of this effort.

### *6.6.1 PPC405*

Many operating systems used in typical application development are compatible with the PPC405 hard-core processor. Some of the more popular include:

- Linux
- VxWorks
- Integrity
- ThreadX

This is not an exhaustive list; other operating systems ***are*** available.

### *6.6.2 MicroBlaze*

Operating systems that are compatible with the MicroBlaze processor include:

- Nucleus
- Xilinx MicroKernel (XMK)
- uClinux
- Linux
- ThreadX

This is not an exhaustive list; other operating systems may also be available.

### *6.6.3 LEON3*

Operating systems listed on the Gaisler web site that are compatible with the LEON3 include:

- RTEMS 4.6.5 (requires the RCC cross-compiler)
- Nucleus
- VxWorks 5.4 and 6.3
- ThreadX

This is not an exhaustive list; other operating systems may also be available.

# 7. CONCLUSIONS AND RECOMMENDATIONS

Tolerable upset rates and processing requirements will be determined by projects at the system level. These requirements will in turn define the processors that can be applied to the problem and also the mitigation schemes that must accompany them.

The radiation-hardened-by-design SIRF device from Xilinx is targeted towards the NBA for future space missions but is still in development – its exact single-event effects have yet to be characterized. The XRTC offers Xilinx device users the opportunity to collaborate in developing radiation tests and also radiation mitigation strategies. Because SNL has programmatic interest in the use of radiation-hardened FPGAs for deployment in radiation environments, it is important that SNL continues to support the XRTC in its efforts to develop and test SIRF device mitigation schemes while the device is still in development and can be modified with design enhancements to make it more robust. Such involvement is mutually beneficial to both SNL and the XRTC.

The dual hard-core processors within the SIRF device, the PPC440, will not have radiation-hardened-by-design improvements made to them but will be available for use if suitable external mitigation schemes can be applied (such as TMR to logic outside of the processor or running the hard-core processors in lockstep with an external monitor). Because these hard-core processors have higher performance benchmarks and lower FPGA resource utilization metrics than soft-core processors, they should be seriously considered for use in the NBA paradigm.

The LEON soft-core processor promises the possibility of code reuse because of the availability of two radiation-hardened ASIC devices. The soft-core LEON processor may be the most difficult to mitigate in a non-radiation-hardened-by-design FPGA because of the lack of mitigation support for this device from the FPGA vendor. It is unknown whether the fault-tolerant LEON core will actually be fault-tolerant when targeted to the SIRF device.

Future processor evaluation efforts should include the measurement of power consumed by the basic FPGA host platform and then the increment added by the processor design. If a suitable COTS Virtex-5 FX130T board with power measurement capabilities is not available, a custom board design with power probes is recommended.

Device drivers and application software can contribute greatly to power consumed unnecessarily by the CPUs. Special care must be taken to architect a software system that seamlessly utilizes hardware low-power modes and abstracts all of the complex power mode behavior into a generic application interface.

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# APPENDIX A

## A.1 LEON ML-405 Modifications

The modifications began with the design files for the ML-401 board located in the following directories: (1) grlib…/designs/leon3-avnet-ml401 and (2) grlib…/boards/avnet-ml401-xc4vlx25. The files in these directories were moved into two new directories: (1) grlib…/designs/leon3-avnet-ml405 and grlib…/boards/avnet-ml405-xc4vfx20.

*Useful links:*
http://tech.groups.yahoo.com/group/leon_sparc/message/12490

The following files needed modification:

IP Cores\grlib-gpl-1.0.17-b2710\boards\avnet-ml405-xc4vfx20\leon3mp.ucf
IP Cores\grlib-gpl-1.0.17-b2710\boards\avnet-ml405-xc4vfx20\Makefile.inc
IP Cores\grlib-gpl-1.0.17-b2710\boards\avnet-ml405-xc4vfx20\prom.cmd
IP Cores\grlib-gpl-1.0.17-b2710\boards\avnet-ml405-xc4vfx20\system.ucf

It does not appear that the ucf files in this directory are used when compiling the core in the manner detailed above. The Makefile.inc file needed modification to update the part and package information. The prom.cmd file needed modification to update the filename of the .mcs file used when programming the prom.

IP Cores\grlib-gpl-1.0.17-b2710\designs\leon3-avnet-ml405\leon3mp.ucf
IP Cores\grlib-gpl-1.0.17-b2710\designs\leon3-avnet-ml405\leon3mp.vhd
IP Cores\grlib-gpl-1.0.17-b2710\designs\leon3-avnet-ml405\leon3mp.xcf
IP Cores\grlib-gpl-1.0.17-b2710\designs\leon3-avnet-ml405\Makefile

The leon3mp.ucf file in this directory is used by the ISE toolset when synthesizing and mapping the design. There were numerous changes in this file to incorporate device pinout changes between the ML-401 and ML-405 boards. Eventually most pin constraints were commented out and left only the critical pin constraints. It should be noted that some of the features of the board are unavailable due to the use of an FX20 device. One bank (Bank 9) of various signals is inaccessible.

The leon3mp.vhd file is the top level VHDL design file. Changes were needed in this file to reduce the number of Digital Clock Managers (DCMs) used by the design and to enable the debug uart without using a GPIO pin. The lines modified in the original file are: lines 249 – 254, line 259, line 297, line 314, and line 317.

The leon3mp.xcf file was modified to comment out timing constraints that were no longer valid due to pins being unconstrained in the leon3mp.ucf file.

The Makefile was modified to change the BOARD variable to represent the ML-405 board.

Another important change was to set the DDR266 SDRAM controller's memory frequency variable to 100 MHz. This change also reduced the number of DCMs required by one. The Chip select bank size was also changed to 128 MB. The design will not synthesize for a clock speed less than 32 MHz. This is due to a minimum frequency constraint for the DCMs in the Virtex-4 devices.

The approach outlined above for programming the LEON core can be applied to the ML-405 board. However, there is one configuration item that must be set on the board to allow successful programming of the Virtex-4 device. The Field Programmable Gate Array (FPGA) configuration must be set to *MAS Ser* mode and SW2 must be set to *Plat Flash*. The Master Serial configuration was not obvious when reading through any of the documentation; this detail was stumbled upon.

## LEON ML-410 Modifications

The ML-410 is used to evaluate performance of the LEON core with a floating point unit (FPU). This was only feasible on the ML-410 board since it has a Virtex-4 FX60 device with sufficient resources to support the FPU.

The procedure was started with the design files for the ML-405 board. Similar modifications to those performed when migrating from the ML-401 to ML-405 board were used when migrating from the ML-405 to ML-410 board. As a sanity check, a system was synthesized with a 40-MHz system clock, cache enabled, and no FPU. The Dhrystone and Whetstone benchmarks were run on this system to verify that the results were close to those of the same configuration on the ML-405 board. The results were identical.

The ML-410 board only contains a System ACE for configuration of the FPGA. Because the purpose of this exercise was only to evaluate the FPU, the .bit files from the synthesized designs were downloaded directly to the FPGA using the Xilinx IMPACT tool. Benchmarks were executed as documented above using COM0 on the ML-410 board.

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