SANDIA REPORT

SAND2008-6142
Unlimited Release
Printed September 2008

Design of a 7-MV Linear Transformer Driver (LTD) for Down-Hole Flash X-Ray Radiography

Joshua J. Leckbee, Bryan V. Oliver, Nichelle Bruner, David V. Rose, Dale R. Welch, David L. Johnson and Steve R. Cordova

Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94-AL85000.

Issued by Sandia National Laboratories, operated for the United States Department of Energy by Sandia Corporation.

Available to DOE and DOE contractors from
U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831

Telephone: (865) 576-8401
Facsimile: (865) 576-5728
E-Mail: reports@adonis.osti.gov
Online ordering: http://www.osti.gov/bridge

Available to the public from
U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Rd
Springfield, VA 22161

Telephone: (800) 553-6847
Facsimile: (703) 605-6900
E-Mail: orders@ntis.fedworld.gov
Online ordering: http://www.ntis.gov/help/ordermethods.asp?loc=7-4-0#online

SAND2008-6142
Unlimited Release
Printed September 2008

Design of a 7-MV Linear Transformer Driver (LTD) for Down-Hole Flash X-Ray Radiography

Joshua J. Leckbee [*], Bryan V. Oliver, Nichelle Bruner [†], David V. Rose [†],
Dale R. Welch [†], David L. Johnson [‡], and Steve R. Cordova
Advanced Radiographic Technologies Department
Sandia National Laboratories
P.O. Box 5800
Albuquerque, NM 87185

Abstract

Pulsed power driven flash x-ray radiography is a valuable diagnostic for subcritical experiments at the Nevada Test Site. The existing dual-axis Cygnus system produces images using a 2.25 MV electron beam diode to produce intense x-rays from a small source. Future hydrodynamic experiments will likely use objects with higher areal mass, requiring increased x-ray dose and higher voltages while maintaining small source spot size. A linear transformer driver (LTD) is a compact pulsed power technology with applications ranging from pulsed power flash x-ray radiography to high current Z-pinch accelerators. This report describes the design of a 7-MV dual-axis system that occupies the same lab space as the Cygnus accelerators. The work builds on a design proposed in a previous report [1]. This new design provides increased diode voltage from a lower impedance accelerator to improve coupling to low impedance diodes such as the self magnetic pinch (SMP) diode. The design also improves the predicted reliability by operating at a lower charge voltage and removing components that have proven vulnerable to failure. Simulations of the new design and experimental results of the 1-MV prototype are presented.

[*]E-mail: jjleckb@sandia.gov
[†]Permanent Address: Voss Scientific, Albuquerque, NM
[‡]Permanent Address: L-3 Communications - Pulse Sciences, San Leandro, CA

Acknowledgment

The authors acknowledge Boris Kovalchuk and Alexander Kim at the High Current Electronics Institute (HCEI) in Tomsk, Russia for their experimental work in developing the 1-MV prototype LTD. We also acknowledge the efforts of Dillion McDaniel and John Maenchen in advancing LTD research and collaborations with the HCEI. We also acknowledge the work of Bill Bui in maintaining and fielding experiments on the 1-MV LTD adder.

Contents

Figures

Tables

1 Introduction

Pulsed power accelerators designed to drive flash radiography diodes are typically quite large. Older machines at the Atomic Weapons Establishment (AWE) in England are based on marx generator capacitive energy storage and Blumlein pulse compression. Modern radiography accelerators such as RITS [2], Mercury [3], and Hydrus [4, 5] use inductive voltage adder (IVA) technology [6]. Inductive voltage adders consist of multiple series IVA cells coupled to a single stalk forming a magnetically insulated transmission line (MITL) which is coupled at the high voltage end to an electron beam diode. The primary energy storage for an IVA system is typically a marx generator capacitor bank. The output pulse of the marx generator is much too slow to produce the desired 50-ns radiation pulse. The output pulse of the marx generator must be compressed in time by charging pulse forming lines (PFL) which narrow the pulse before driving the IVA cells. Including the energy storage and pulse compression stages, the total accelerator footprint becomes quite large. The six stage RITS-6 accelerator is approximately 12 m by 8 m and the design of the ten stage Hydrus accelerator is 25 m by 11 m.

A linear transformer driver (LTD) is a type of IVA where the primary energy storage is packed inside the IVA cells. Inside each cell, or cavity, the energy storage capacitors are arranged as parallel single-stage marx generators. Each single-stage generator contains two capacitors discharged through a spark gap switch in a low inductance geometry commonly referred to as an LTD brick, shown in Figure 1. The primary energy storage discharge circuit inductance is sufficiently low to provide the desired 50-100-ns electrical output pulse without the use of pulse compression stages. The pulse shape is determined primarily by the inductance and capacitance of the individual bricks in a cavity. The impedance of the cavity is determined by the number of parallel bricks.

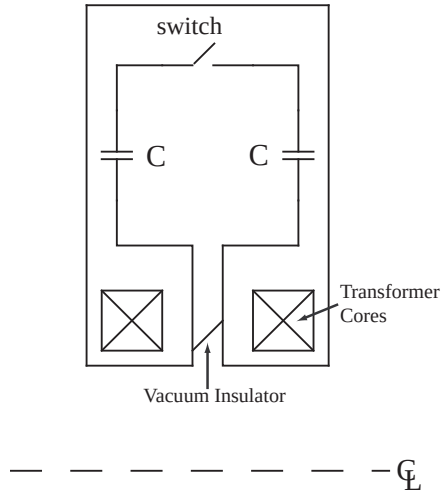

Figure 1. The LTD brick contains two capacitors separated by a spark gap switch. When the switch closes, a voltage is seen across the vacuum insulator and the transformer cores isolate the pulse from the ground return along the cavity housing during the pulse.

The LTD architecture discussed in this report was developed at the Institute of High Current Electronics (HCEI) in Tomsk, Russia. Individual LTD cavities have been tested with 10 [7, 8], 16 [9, 10], 20 [11], and 40 [12, 13] parallel bricks. Repetitive testing of a single, high current, 20-brick cavity has been performed at Sandia to investigate lifetime of the LTD components. The system proved to be very reliable during the 13,500 shots. A LTD adder for radiography has also been tested at Sandia into an electron beam diode load. The LTD adder consists of seven series cavities containing 10 parallel bricks each [14, 15, 8]. A high current adder was recently tested at HCEI with five series cavities with 40 parallel bricks each [13]. This high current system is being upgraded to 10 series cavities and will be tested at Sandia beginning next year.

Pulsed power flash x-ray radiography is an important diagnostic for down-hole sub-critical experiments at the Nevada Test Site (NTS). The Cygnus accelerators [16] have provided dual-axis x-ray imaging for recent experiments by using a 2.25 MV electron beam diode. It is expected that future experiments will require higher voltage accelerators which will not fit in the existing tunnel space if based on the existing IVA technology. The LTD architecture is uniquely suited to solving this challenge. The natural shape of a LTD accelerator for radiography applications is long and narrow. Accelerators based on the existing LTD technology are compact enough to provide dual-axis imaging up to about 7 MV in the same space as the dual-axis 2.25 MV Cygnus system.

This report details the conceptual design of a 7-MV dual-axis pulsed power radiography system based on LTD technology. The accelerator design is part of an effort to anticipate future requirements for increased radiographic capability at NTS. In the absence of programmatic requirements, we have analyzed the largest LTD based accelerator that could be installed in the U1a facility where Cygnus is currently fielded. The design in this report assumes no significant improvements in pulsed power or radiographic diode technology. As these technologies advance, the design could be revised to provide higher voltage and improved radiographic capability.

A previous report described the design of a 6.5-MV, 50-Ω LTD consisting of 48 series LTD cavities with 12 bricks in each cavity [1]. This previous design presented the smallest LTD that could be used to produce a 6.5-MV output pulse with existing LTD technology. The new design presented here is physically larger, has reduced electrical stresses, and should have improved reliability. The Cygnus accelerator was required to have less than one failure in 200 shots including prefires, no-fires, and breakdowns [16]. We do not have sufficient experimental data to perform a detailed statistical analysis of the reliability of the LTD system. However, two modifications have been made to the new design that should improve reliability. This previous design relied on the use of peaking capacitors connected across the output of each cavity to increase the peak output voltage and narrow the radiation pulse. The peaking capacitors are subjected to any voltage reversal or oscillations in the cavity voltage that might arise from impedance mismatches or circuit faults. Peaking capacitors are not included in the new design discussed in this report to reduce the number of fault modes. The new design also assumes a lower charge voltage of 90 kV opposed to 100 kV to improve reliability of the components and of the accelerator as a whole. If future testing shows the reliability to be sufficient, these features could be added to the new design to increase the output voltage capability. Simulations of the accelerator are presented. Experimental results of the 1-MV prototype LTD accelerator will also be discussed.

2 Physical Description

A 7-MV LTD accelerator has been designed that is suitable for a dual-axis down-hole radiography facility. The two accelerators would occupy approximately the same footprint as the existing Cygnus accelerators shown in Figure 2. The U1a facility that houses the Cygnus accelerators is a 6.7 m wide tunnel with an arched ceiling that is 5.18 m at its peak. A minimum 1.2 m clearance must be maintained on one side for access to the experiment room. The machines must also leave room to walk around and between the two. Given these constraints, the LTD cavities can be no more than 1.75 m diameter each.

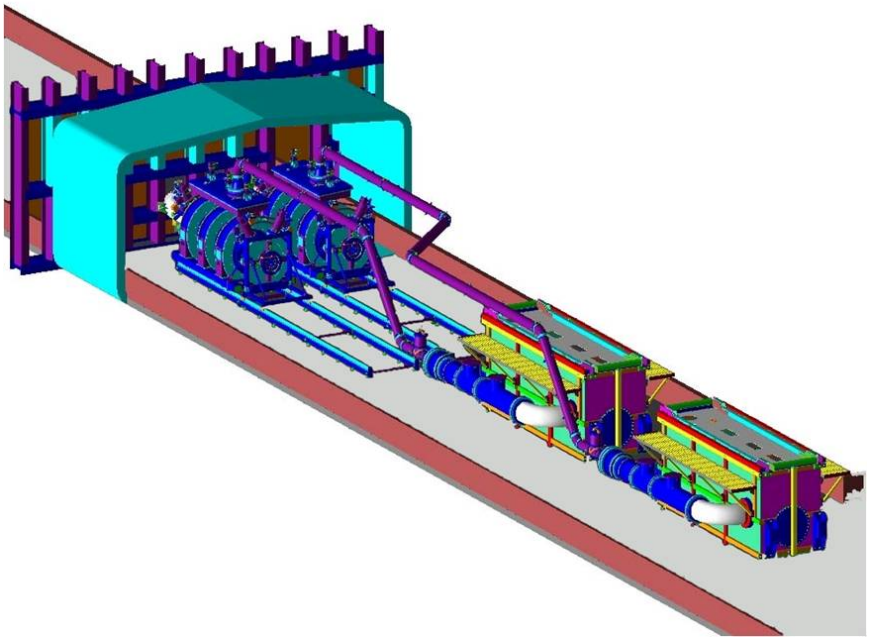

Figure 2. This drawing shows the dual-axis Cygnus radiography system as fielded in the U1a tunnels at the Nevada Test Site.

Experiments on the RITS-6 accelerator with a high impedance, 80-Ω, MITL and a low impedance, 40-Ω, MITL have shown that low impedance diodes such as the Self-Magnetic-Pinch (SMP) perform best when coupled to a low impedance MITL [17]. For this reason, The 7-MV LTD accelerator has been designed with a 40-Ω MITL compared to the 50-Ω MITL in the previous 6.5-MV LTD design [1]. The limitation of the cavity diameter discussed above sets the lower limit on the single cavity impedance by limiting the number of parallel bricks in a cavity. The LTD cavities must be matched to the MITL impedance to produce the desired output pulse shape. The accelerator is designed with a 40-Ω MITL to couple well with low impedance diodes. These impedance matching requirements provide an upper limit on the number of series cavities, and thus the peak attainable voltage. If the design were modified to couple to a higher impedance MITL, then more cavities could be added, increasing the peak diode voltage.

The existing LTD cavity design developed at HCEI is used as a baseline for this design [18, 7]. The cavities in this design have a 1.75 m outer diameter, a 0.56 m bore diameter, and are 0.22 m thick, see Table 1. When stacked in series, the cavities are compressed in groups of eight or 16 to provide a vacuum seal for the MITL. Numbering the cavities starting with the furthest from the diode, additional space is left after cavities 8, 24, 40, and 56 to accommodate the compression mechanism and to leave space for additional vacuum pumps as needed, see Figure 3. After the last cavity, number 72, the MITL extends an additional 2-3 m and is bent toward the center line between the machines. The machines sit parallel to one another, but the x-ray sources both point toward the object to be imaged, similar to the bent vacuum output lines on the Cygnus accelerators. The bent output line on the Cygnus accelerators are design to operate with no electron sheath current. Bent coaxial MITLs have been used successfully in the past, such as in the Aurora accelerator [19]. The total length of the LTD accelerators including these additional spaces is 23 m.

Table 1. LTD System Description

Number of series Cavities	72
Number of parallel Bricks per Cavity	18
Cavity Diameter	1.75 m
Cavity Length	0.22 m
Total Accelerator length	23m

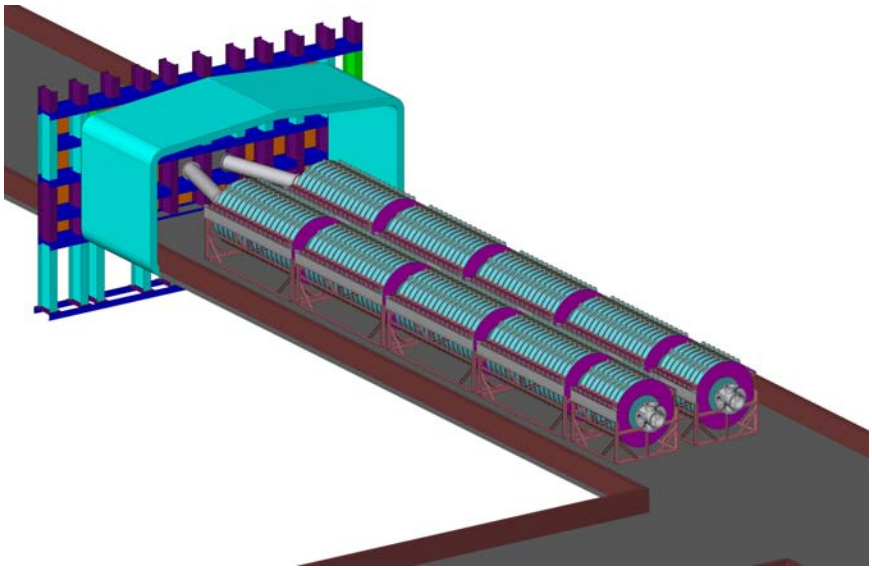

Figure 3. This drawing shows the dual-axis 7-MV LTD as it would look in the U1a facility in place of the Cygnus accelerators.

The MITL is designed to approximately match the impedance of the LTD cavities along its length. An ideal MITL would have stepped diameter transitions at each cavity so that the operating impedance of the MITL would match the impedance of the sum of the cavities up to that point

in the accelerator. A MITL with 72 different impedance steps or a continuous taper would be very complicated and expensive to manufacture. LSP simulations discussed in section 4 are being used to design the MITL and investigate its performance with impedance transitions in 8-cavity intervals, or in 4.4-Ω increments as shown in Table 2. A mechanical design of this particular MITL has not been done at this time. A mechanical stress analysis was performed for the 48-cavity design reported previously [1]. In addition, the MITL is about the same length as the MITL designed for the Hydrus accelerators but will be larger in diameter than the 80-Ω Hydrus MITL. Based on these two designs, an acceptable mechanical design should be achievable and will be completed in future work on this system.

Table 2. MITL Dimensions and Impedances

Cavities	Length (m)	Diameter (m)	Vacuum Impedance (Ω)	Operating Impedance (Ω)
1 - 8	2.25	0.245	8.0	4.4
9 - 16	2.25	0.222	13.8	8.9
17 - 24	2.25	0.203	19.2	13.3
25 - 32	2.25	0.186	24.4	17.8
33 - 40	2.25	0.171	29.5	22.2
41 - 48	2.25	0.157	34.6	26.7
49 - 56	2.25	0.144	39.6	31.1
57 - 64	2.25	0.133	44.6	35.6
65 - 72	2.25	0.122	49.5	40
After 72	3	0.122	49.5	40

3 Circuit Simulations

Circuit simulations have been carried out using the Bertha transmission line circuit code [20]. The circuit model of the 7-MV LTD is an extension of a model developed to describe the seven cavity 1-MV LTD [14]. The model approximates each cavity as a single brick element whose values are equal to the parallel combination of the 18 bricks in the cavity as shown in Figure 4. This greatly reduces the number of circuit elements in the simulation and thus reduces the simulation run time. This lumped circuit method of modeling an LTD cavity has proven to produce very accurate results when compared to single cavity and seven cavity experimental results [14].

Each cavity is modeled separately. This allows us to investigate the effect of cavity timing as well as the effect of driving different MITL impedances. This is important since the MITL is designed with impedance transitions in approximately 1-MV increments. Ideally the MITL center stalk diameter would decrease after each cavity to maintain an ideal impedance matching of the LTD cavities to the MITL.

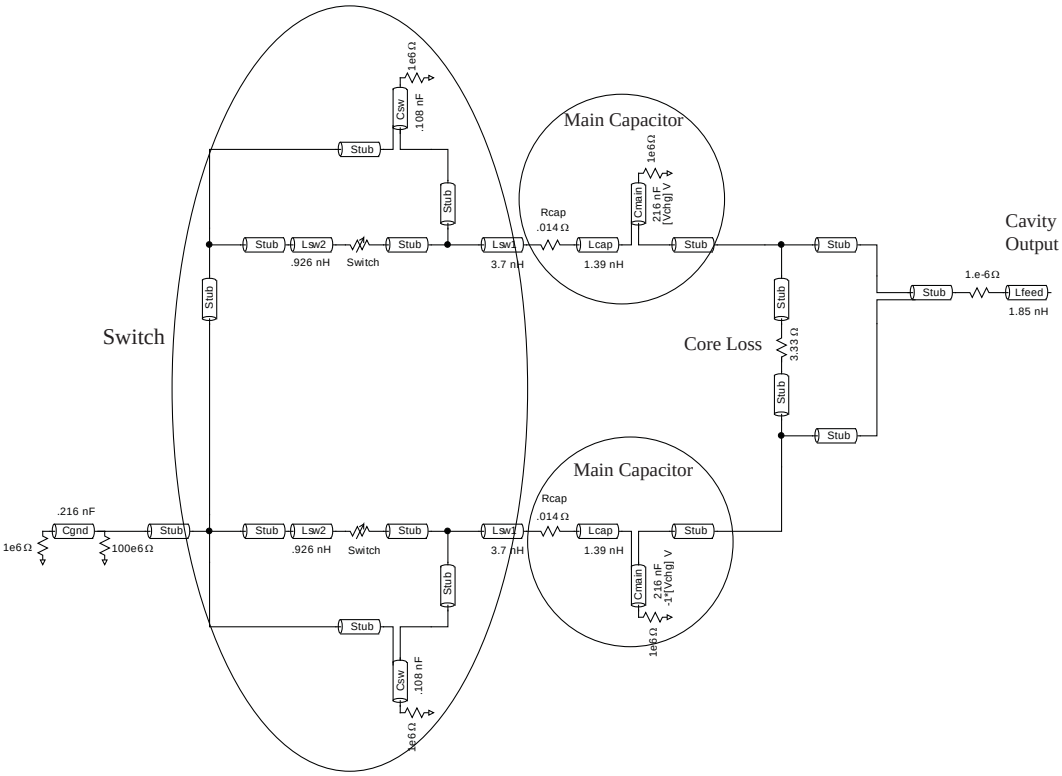

Figure 4. Circuit diagram of a single cavity. "Stub" elements in the circuit diagram are used to facilitate connection of various circuit elements and do not effect the simulation.

The circuit model approximates each section of the MITL as an ideal transmission line with impedance equal to the predicted operating impedance of the MITL after electron sheath flow is

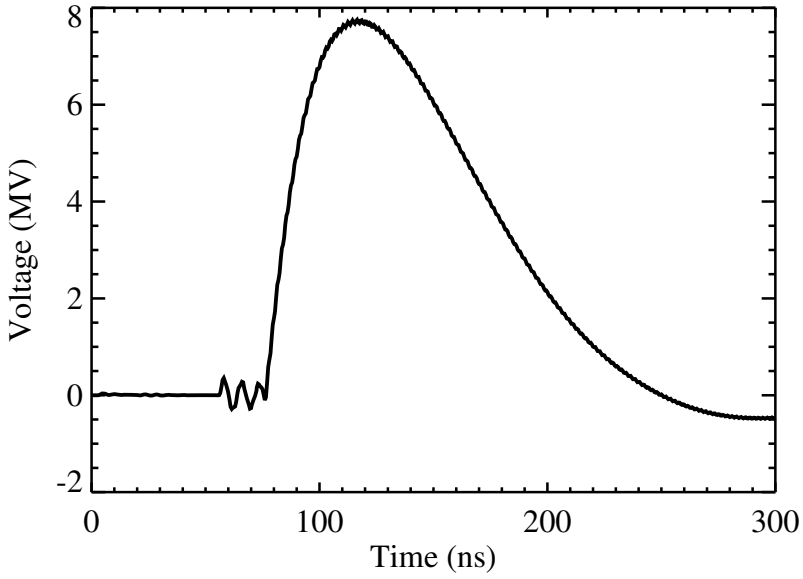

Figure 5. Circuit simulations predict a peak forward going voltage of about 7.7 MV into a 40-Ω MITL.

established. The exact behavior of the electron flow and the MITL impedance is too complex to capture in a simple 1-D circuit element. The circuit simulations using the MITL flow impedance are adequate for determining the forward going voltage pulse into a matched load. Electron sheath flow is established early in the pulse and so the operating impedance of the line is a reasonable approximation for determining the forward going voltage. This model predicts that the LTD circuit will produce a peak forward going voltage on the MITL of 7.7 MV, as shown in Figure 5. A small amplitude, short duration pre-pulse will occur before electron sheath flow is established on the MITL and thus the MITL will run at approximately the vacuum impedance. The simulations using the operating impedance of the MITL will somewhat underestimate the amplitude of this pre-pulse. However, simulations of the pre-pulse using the vacuum impedance of the line show only a few percent increase in the pre-pulse amplitude.

When coupled to a low impedance diode, such as the SMP or negative polarity rod-pinch (NPRP), the diode pulls significantly more current than the bound current in the cathode stalk of the MITL. As a result, much of the sheath current must be retrapped at the penalty of decreasing the diode voltage [21, 22]. Both the amplitude and velocity of the retrapping wave depend on the severity of the impedance mismatch between the MITL and the diode. The 1-D circuit model with ideal transmission line representation of the MITL cannot accurately predict the effect of the retrapping wave generated by coupling the MITL to a low impedance diode. As discussed in Section 7 of this report, future studies will use 2-D particle-in-cell (PIC) simulations using the LSP suite [23] to determine the diode voltage for the given MITL geometry when coupled to a low impedance load. The diode voltage can also be predicted analytically as described in the 6.5-MV LTD design paper [1].

One significant change from the previous 6.5-MV LTD design is the removal of peaking capacitors. The peaking capacitors are subjected to extreme voltage reversal when faults such as a vacuum insulator flashover occur. This was seen as a significant limitation on the reliability of the system that could be eliminated. The peaking capacitors produce an oscillation on the output pulse with a frequency designed to produce a peak that coincides with the natural peak of the pulse. The resulting pulse has a higher voltage peak and a narrower radiation pulse. To achieve the narrower radiation pulse without peaking capacitors, the circuit must either have lower inductance or use lower capacitance per brick. Lower inductance switches are being developed using Lab Directed Research and Development (LDRD) funds at Sandia [24]. However, for this design, we have chosen to use existing switch technology. Thus we have reduced the capacitance from 20 nF per capacitor to 12 nF as listed in Table 3. This results in a radiation pulse that is approximately 50 ns, see Figure 12 and Table 3.

Table 3. Electrical characteristics and circuit simulation results

Capacitors	12 nF
Total inductance of one brick	250 nH
Forward going voltage	7.7 MV
Diode Impedance (bound current)	40 Ω
Diode Voltage	6.7 MV
Estimated Radiation Pulse Width (FWHM)	53 ns

Another significant change from the previous 6.5-MV LTD is the decision to assume that the system will be charged to only 90 kV instead of 100 kV. The distances between components and material thicknesses have not changed, but by reducing the expected charge voltage, the system reliability should increase significantly. If reliability is found to be adequate, then the charge voltage could be increased as high as 100 kV, increasing the load voltage by about 11 %. The new forward going voltage wave would be approximately 8.6 MV with approximately the same MITL operating impedance.

4 Particle-in-Cell Simulations

The proposed transmission line geometry with 72 cavities was modeled using the fully-relativistic particle-in-cell code LSP[25]. The purpose of these studies is first to develop a timing scheme for firing the individual cavities in order to achieve a 50-ns pulse width and second to predict power flow along the transmission line. For the first goal, simulations were run using either the Bertha [26] transmission line algorithms that have been imported into LSP or the Bertha-generated single-circuit waveform as the injected pulse from each cavity. For the second goal, space-charge-limited electron emission is modeled along the entire length of the cathode.

Details of the simulation geometry are shown in Figure 6. Simulations were performed in 2D (r,z) with resolution of 0.5–1 mm in r and 1 mm in z. The spacing between each cavity is 22 cm with a 1-m spacing between 16-cavity groupings. This results in a total length of the voltage-addition section of approximately 20 m. The impedance transitions listed in Table 2 occur in 20-cm long tapered sections positioned just before the subsequent set of 8 cavities. The simulation geometry was limited to just the voltage-addition section with an open boundary replacing the load.

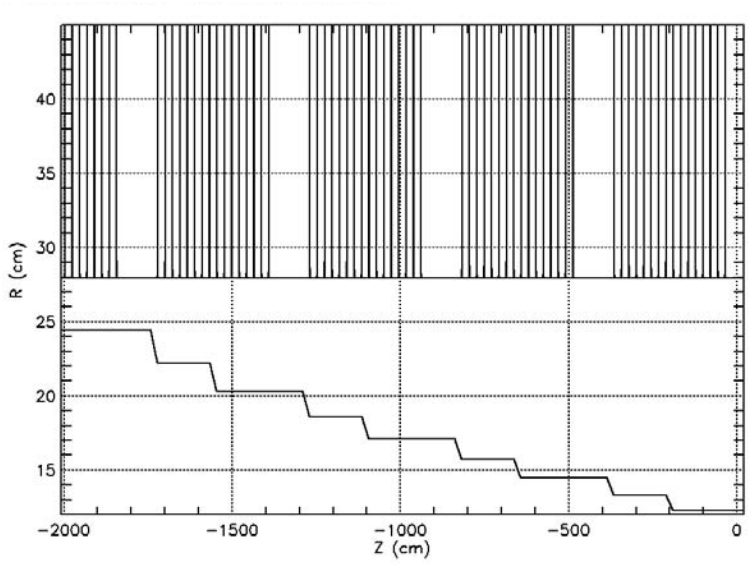

Figure 6. Simulation geometry of the 72-cavity LTD transmission line from LSP.

The cavity inlets were reduced from 2.2 cm to 4 mm for each cavity in the 72-cavity simulation to produce the desired cavity impedance. This reduced the simulation run-time at the expense of identifying when and where free electrons which have crossed the anode-cathode gap may penetrate the cavities.

The voltage output from a single-cavity simulation using the Bertha circuit algorithms in LSP

is shown in Figure 7. The cavity voltage is recorded at both the Bertha circuit connection to the LSP grid and across the cavity inlet port in the grid. These voltages show very slight impedance differences between the circuit and grid, but compare well to the waveform generated by a stand-alone Bertha circuit simulation.

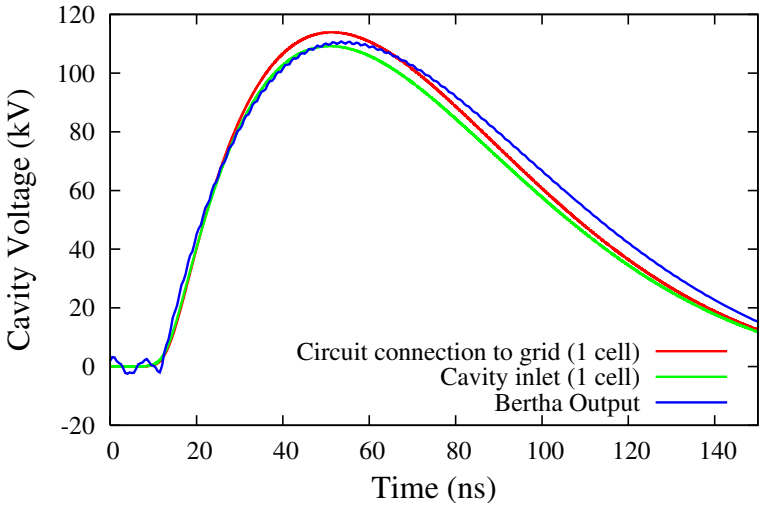

Figure 7. The cavity voltages from a Bertha/LSP simulation recorded at both the output of the Bertha circuit and the inlet port of the cavity on the LSP grid. The waveform from a stand-alone Bertha circuit simulation is shown in blue for comparison.

The waveform from the stand-alone Bertha circuit simulation replaces the full circuit in the 72-cavity simulations. The waveform is injected as a time-varying potential across the inlet boundary which defines each cavity in Figure 6. The timings of the injection of this wave in the cavities were varied in order that the voltages may add more ideally in the transmission line. To achieve this, the voltage injection in the downstream cavities is delayed to coincide with the arrival of the forward-going wave delivered by the upstream cavities. To simplify the timing arrangement, the same timing is applied to every cavity in the 16-cavity groupings shown in Figure 6, and timing is only changed between the groupings.

The two sets of cavity-timings listed in Table 4 were simulated for comparison. Voltage results for the "6.6-ns delay" are shown in Figure 8. The voltage across the cavity vacuum insulators, recorded at $r = 33$ cm in the simulations, show that the upstream cavities are seeing the transmission line vacuum impedance instead of the operating impedance. The forward-going wave in Figure 8b has a peak voltage of 7.5 MV and FWHM of approximately 80 ns and a 10-90% risetime of about 40 ns.

Voltage results for the "13.2-ns delay" are shown in Figure 9. The timing is closer to the ideal set and the voltage across various cavity inlets show that the upstream cavities are seeing the operating impedance. The forward-going wave in Figure 9b has a peak voltage of 7.8 MV and

Cavity	"6.6-ns delay" firing time [ns]	"13.2-ns delay" firing time [ns]
1–8	0.0	0.0
9–24	6.6	13.2
25–40	13.2	26.4
41–56	19.8	39.6
57–72	26.4	52.8

Table 4. The timing delay applied to each cavity grouping.

FWHM of approximately 75 ns and a 10-90% risetime of about 30 ns.

The electron power flow changes dramatically as the delay between cavity firings is increased. For delays shorter than 6.6 ns, the flow is magnetically insulated upon emission. For the "6.6-ns delay", most of the 115-kA sheath is insulated, however an almost continuous 5-kA current crosses the anode-cathode gap between cavities 9–24. The "13.2-ns delay" has 118 kA in the sheath after the last cavity, with roughly 10 kA of sheath current continuously crossing the anode-cathode gap. The particle snapshots in Figure 10 illustrate the particle loss in this region. The snapshots are from 50 ns into the simulations for both timings. The "13.2-ns delay" simulation still has evolving flow at this time and the apparent gap closures at $z = -8$ and -13 m last approximately 10 ns.

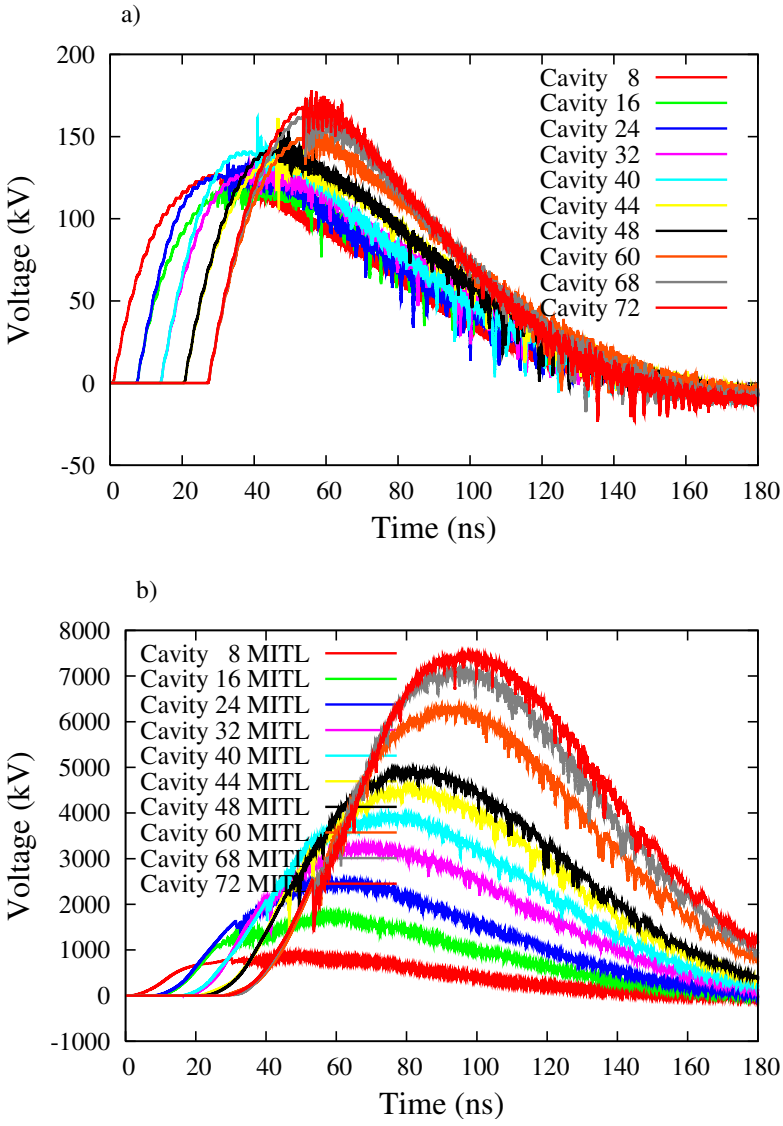

Figure 8. Cavity and line voltages for the "6.6-ns delay" cavity firing timings listed in Table 4. Plot a) shows the voltage drop across several of the cavity inlets recorded at $r = 33$ cm in Figure 6. Plot b) shows the magnetically insulated transmission line (MITL) voltages downstream from various cavities.

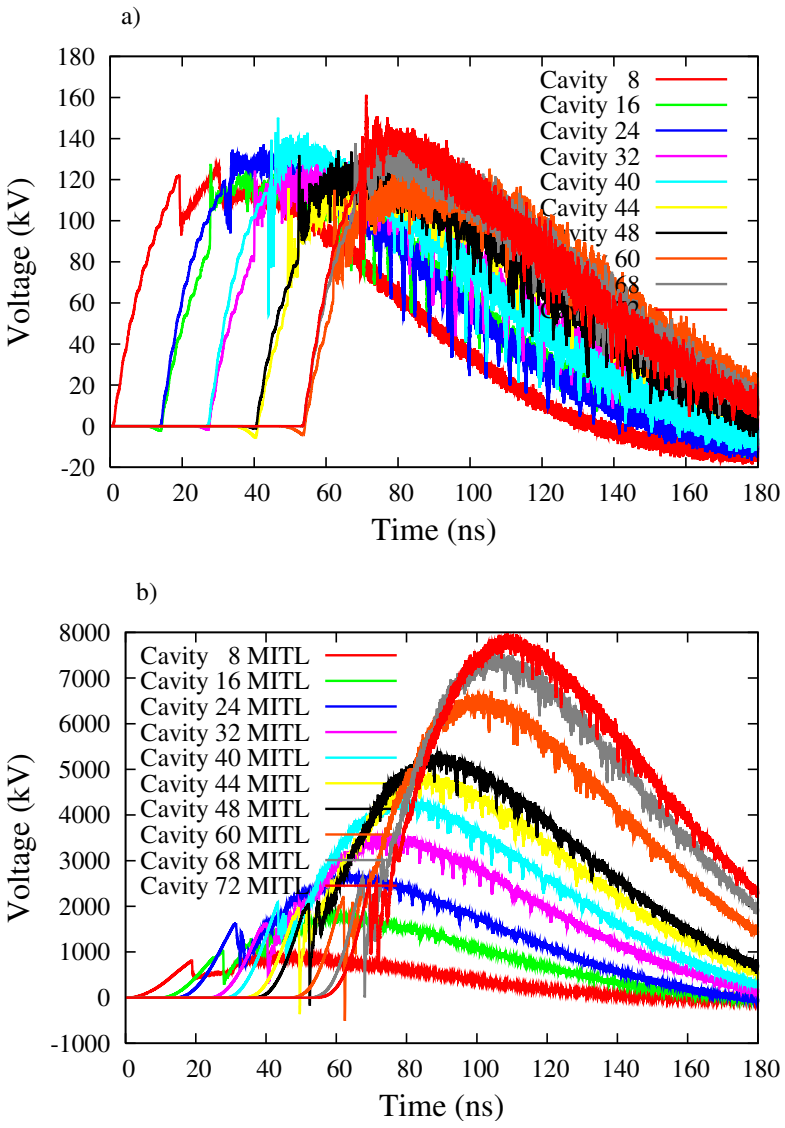

Figure 9. Cavity and line voltages for the "13.2-ns delay" cavity firing timings listed in Table 4. Plot a) shows the voltage drop across several of the cavity inlets recorded at $r = 33$ cm in Figure 6. Plot b) shows the magnetically insulated transmission line (MITL) voltages downstream from various cavities.

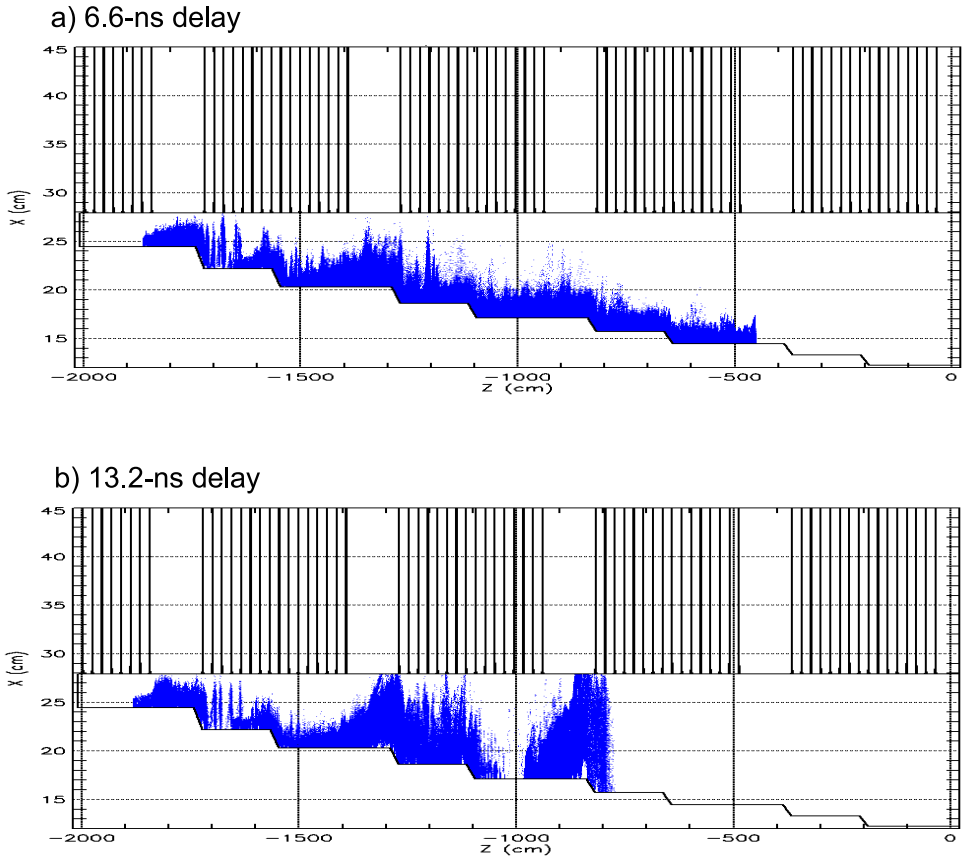

Figure 10. Particle snapshot at 50 ns into the 72-cavity simulations. Electron macroparticles are shown in blue. Plot a) is for the "6.6-ns delay" cavity timings and b) is for the "13.2-ns delay" timings.

5 Predicted Radiographic Capability

The radiographic capability of the LTD system depends on which diode is selected as the load. A radiographic source figure of merit (FOM) has been developed to facilitate comparison of the various radiographic sources. The FOM of a diode is defined as the x-ray dose in Rads measured 1 m from the source divided by the square of the source spot size in mm

$$\text{FOM} = \frac{\text{dose}}{\text{spot}^2} \quad \left(\frac{\text{rad}}{\text{mm}^2}\right). \tag{1}$$

Diodes with a higher figure of merit are considered to be brighter x-ray sources and have superior resolving power.

The "Low Impedance" configuration of the RITS-6 accelerator produces a 7–8-MV drive pulse on a 40-Ω MITL, which is very close to the design parameters of the LTD in this report, as shown in Figure 11. The SMP diode has produced the highest figure of merit in experiments on the RITS-6 accelerator. The total measured x-ray dose from these experiments is greater than 350 Rads@1m with a source spot size of 2.5-3 mm when the Marx generator is charged to 78 kV. This gives a FOM of about 50 Rads@1m/mm^2 [17]. The peak voltage of the LTD is very similar to the peak voltage on RITS-6. As a result, the radiographic capability of the LTD system is expected to be similar to that demonstrated on RITS-6. As discussed in section 3, the LTD cavities were originally designed for operation at 100 kV charge, but for increased reliability, all voltage in this design report assume a charge voltage of 90 kV. If reliability at 100 kV operation is acceptable, the LTD would generate 11% higher voltage and 25-30% higher x-ray dose.

The x-ray dose production of radiographic diodes can be approximated using the radiographers equation for a given diode. The radiographers equations are approximations of the x-ray dose rate based on experimental data and radiation transport simulations. The x-ray dose rate for the SMP diode is given by

$$\frac{dD}{dt} = I_e\left(-2.952V + 2.349V^2 - 0.06934V^3\right), \tag{2}$$

where I_e is the electron current and V is the diode voltage in MV. Figure 12 shows the normalized dose rate calculated using the LTD forward going voltage wave in the MITL and the above SMP diode radiographers equation. The FWHM of the x-ray pulse is 53 ns, see Table 3. The x-ray dose rate will depend on the diode voltage and not the MITL voltage. Future PIC simulations will be used to predict the diode voltage when coupled to a SMP diode.

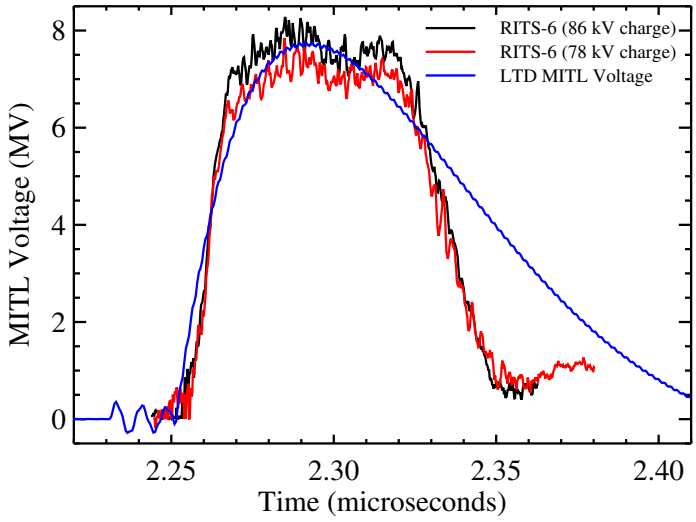

Figure 11. Comparison of the MITL voltage on RITS-6 and simulated voltage of the LTD.

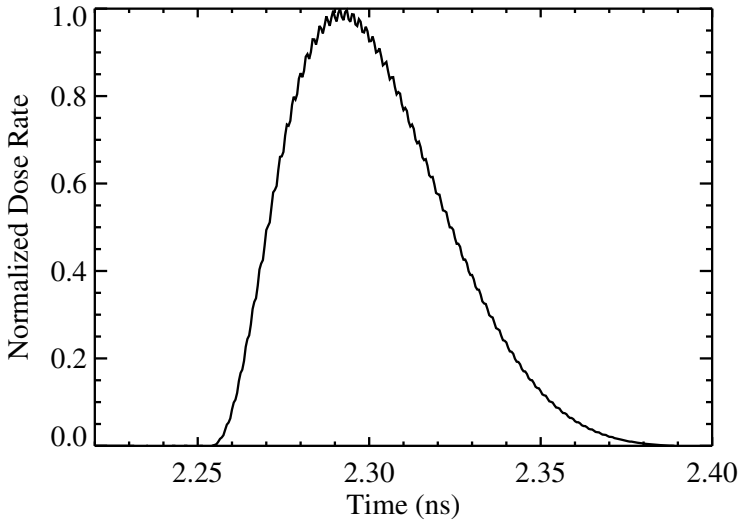

Figure 12. This plot shows the predicted x-ray dose rate calculated using the SMP diode radiographers equation. The x-ray pulse has a FWHM of 53 ns.

6 Testing of a 1-MV Prototype

A 1-MV LTD voltage adder was built at the High Current Electronics Institute in Tomsk, Russia and tested at Sandia National Laboratories [7, 15, 8]. The LTD adder is composed of seven LTD cavities stacked in series. Each LTD cavity contains 10 parallel bricks, as shown in Figure 13. Each brick has 2 capacitors, each 20 nF, connected in series through a multigap spark gap switch. A single cathode stalk is threaded through the centers of the seven series cavities forming a coaxial vacuum insulated transmission line. The LTD adder is designed to supply 125 kA in a 100-ns FWHM voltage pulse without the optional peaking capacitors. The vacuum line is terminated with a large area electron beam diode. Electrons are emitted from the surface of the aluminum cathode, accelerated across a vacuum gap (referred to as the anode-cathode or AK gap), and strike the carbon anode producing an approximately 75-ns FWHM x-ray pulse. The impedance of the electron beam diode is determined by the voltage, length of the AK gap, and the area of electron emission.

6.1 Single Cavity Tests

Individual cavities are tested with a resistive load installed in the center of the cavity. Tests of individual cavities are used to verify that all of the components are functioning properly and also to evaluate the performance of a cavity with different load impedances. The resistor can be filled with different liquid solutions to vary the load resistance. A total of over 1000 shots have been fired with single cavities into a resistive load.

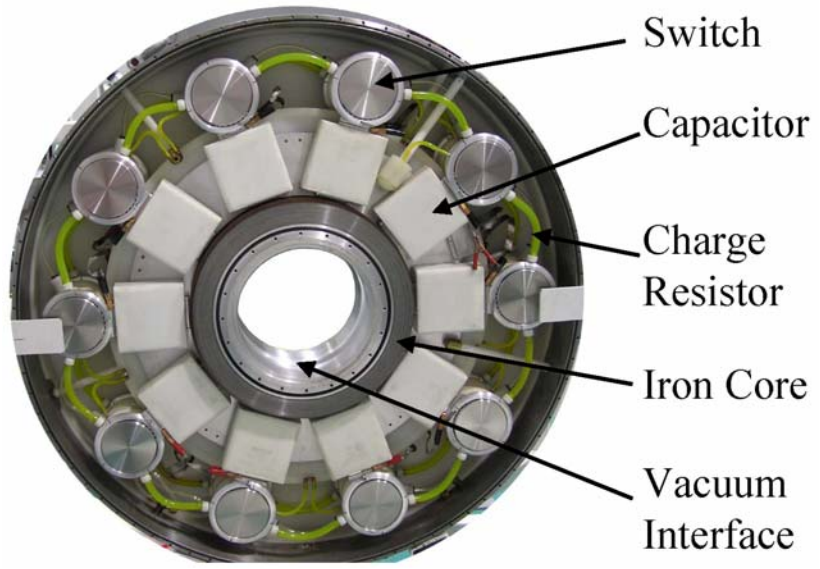

Figure 13. Photograph of a single LTD cavity with the side cover removed to show the layout of internal components.

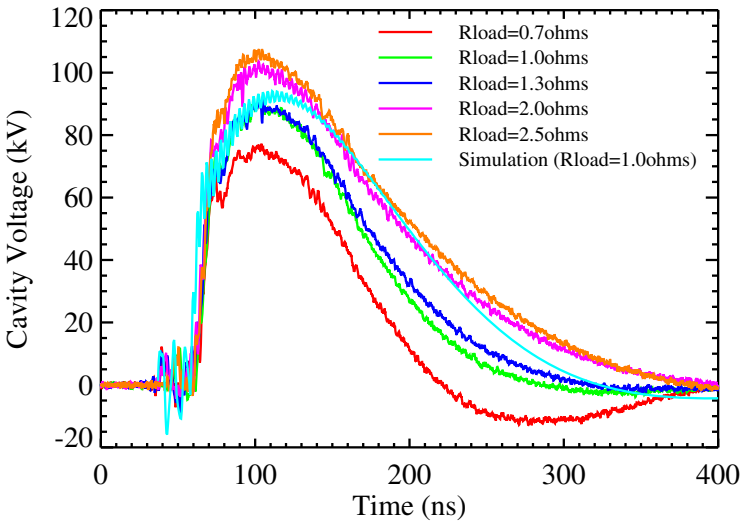

Figure 14. This plot shows the output voltage of a single LTD cavity when tested with different load resistance values. A circuit simulation with a 1-Ω load approximately matches the peak voltage from the experimental results.

A single cavity was tested with different load impedances ranging from 0.7 Ω to 2.5 Ω as shown if Figure 14. The LTD cavity was charged to ±80 kV for this series of shots. A matched RLC circuit should produce a peak voltage of about one half of the total charge voltage, or 80 kV for this experiment. Figure 14 shows that the circuit is approximately matched when the load resistance is in the range 0.7-1.0 Ω.

Circuit simulations of a single cavity were performed using the Bertha circuit code. The circuit model for the individual cavity tests is similar to the model of the 18-brick cavity shown in Figure 4. An example of the circuit simulation results with a 1-Ω load is shown in Figure 14. The circuit simulation predicts a 5% higher peak voltage than the experimental measurement with the same load. The voltage pulse width from the simulation is closer to the experimental pulse width with a 2-Ω load. Future experiments with the seven cavity LTD will include careful calibrations and the addition of a current measurement at the load. This will improve the understanding of the experimental results and help improve the circuit model.

6.2 Full System Tests with Large Area Diode

The seven cavities are stacked in series to form a voltage adder and compressed to form a vacuum seal. A constant diameter cylindrical metal stalk is threaded through the centers of the cavities to form a coaxial vacuum line. The outer conductor diameter is 29 cm and the center stalk diameter

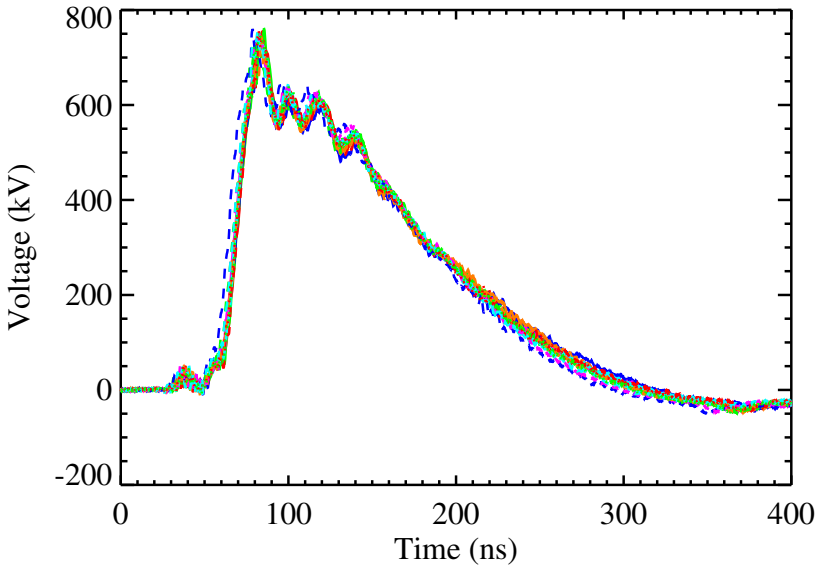

Figure 15. Load voltage vs. time for the LTD adder for 15 consecutive shots into a LAD load. The output pulse of the LTD is very repeatable.

is 21.5 cm, giving a vacuum line impedance of 18 Ω. The coaxial line is terminated with a large area electron beam diode (LAD). The anode is a 1.3-cm thick carbon target mounted to a 1.9-cm thick aluminum plate.

Over 400 full system shots have been fired into electron beam loads with different AK gaps. The individual cavity one-sigma jitters during these tests range from 1.4-2.7 ns. The jitter of the series cavities adds in quadrature, so the total load jitter is similar to the average individual cavity jitter. Over the series of 15 consecutive shots plotted in Figure 15, the one-sigma load jitter is 1.9 ns. The jitter is reported here from a small series of shots because we typically only fire about 15 consecutive shots in any one configuration before changing the charge voltage or the diode AK gap. Over a series of 75 shots with varying voltage and diode configurations the one-sigma load jitter is 7.7 ns. As shown in Figure 15, the timing, peak voltage, and pulse shape are very repeatable.

Large area electron beam diodes have relatively constant impedance through the duration of the pulse compared to a radiographic diode load. However, at the start of the pulse, the electric fields in the diode must exceed the electron emission threshold before current is established. This results in a high impedance phase at the start of the pulse. After current is established, the impedance drops to a relatively constant steady state impedance. The diode impedance remains constant through the pulse as long as the current density on the target is not sufficient to heat the target beyond the threshold for ion emission. If ions are emitted from the anode, the diode impedance will decrease and the beam will begin to pinch. As the beam pinches, the current density increases, which can increase ion production. In extreme cases, the ion production is sufficient to short circuit the AK

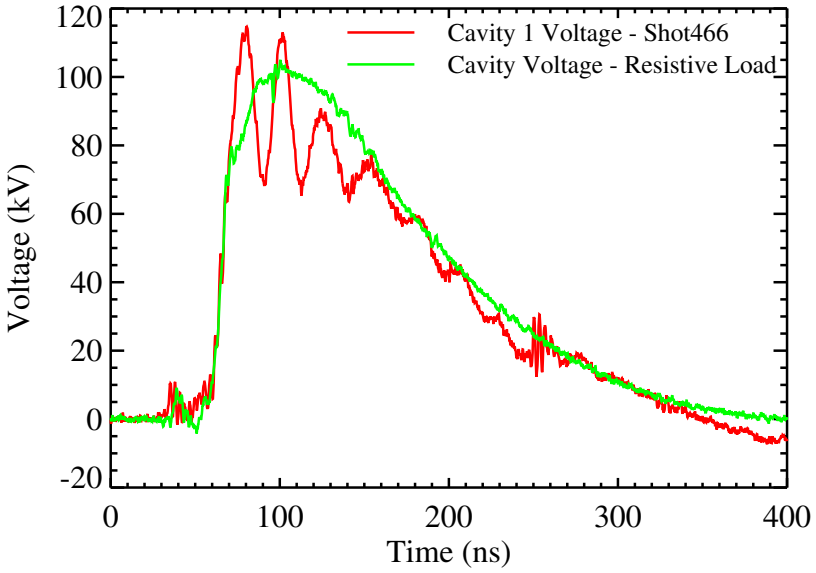

Figure 16. Voltage vs. time comparison of the output voltage of a single cavity when tested as part of the seven cavity adder into a dynamic LAD load and when tested with a constant impedance resistive load.

gap. The diode used in the testing of the seven cavity LTD is designed to deposit the electron current over a sufficiently large area to prevent significant ion production.

Testing a multi-cavity system with a dynamic impedance load is essential for predicting how a large accelerator will perform. The LTD output pulse when tested with a resistor load, has the shape of a simple RLC circuit, as shown in Figure 16. When tested with a dynamic impedance which is a near open circuit for the first few nanoseconds, the load voltage briefly spikes up higher than when tested with a constant load impedance. The spike at the beginning of the pulse is very noticeable in the load voltage shown in Figure 15. After the diode impedance reaches a steady state value, the load voltage more closely resembles the simple RLC pulse shape. The output voltages of the individual cavities also have a spike at the beginning of the pulse, followed by an oscillation that is slowly damped as the pulse continues. The difference between a cavity tested with a load resistor and when tested in the voltage adder configuration with a LAD load is shown in Figure 14. The cavity output voltage oscillations are different for each cavity and are determined by the cavity position in the adder, as shown in Figure 17. The large cavity oscillations vary in amplitude and shape and so the superposition of these voltages results in only a small voltage oscillation at the load, as shown in Figure 15.

A previous paper analyzed the effects of various faults on the components in an LTD cavity [1]. The cavity oscillations do not pose a significant problem for the components in the cavity. Even the largest oscillations seen in this system, do not cause the cavity voltage to reverse, which could increase the probability of insulator flashover. Based on circuit simulations, these oscillations have

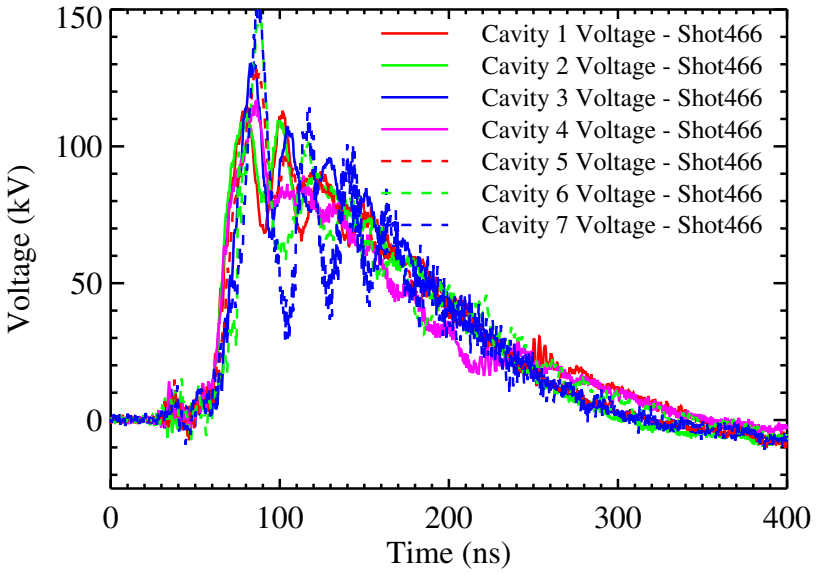

Figure 17. This plot shows the differences in cavity output voltages when tested as a full system into a LAD load. The sum of these seven voltages produces a plot similar to Figure 15.

very little effect on the voltage across the capacitors. A large capacitor voltage reversal could reduce the capacitor life. The peak voltage on the oscillations briefly raises the electric field stress on the vacuum insulators and results in a marginal increase in the probability of insulator flashover.

7 Future Research

Research in the coming years will continue to advance the state of the art LTD systems for radiographic applications. Reliability tests have been carried out as part of the high current LTD experiments. Lifetime testing of a single LTD brick with one multigap spark gap switch has operated for 37,000 shots at the HCEI. In a separate experiment at Sandia, a single cavity with 20 parallel bricks has operated reliably for 13,500 shots. Testing of the 1-MV radiography LTD will continue to gather reliability data in a voltage adder configuration. A second voltage adder will be assembled and tested at Sandia over the next year with 10 series cavities to produce 1-MV, 1-MA pulses into a resistive load. The continued collaboration of these parallel programs will improve the overall reliability of future LTD systems.

A single 10-brick cavity has been designed which incorporates several improvements based on lessons learned through LTD testing at Sandia. When built, this will be the first cavity manufactured entirely in the U.S.A. The cavity will mate to the seven radiography LTD cavities and give an increase in the peak voltage.

Technical risks of building a 7-MV LTD could be greatly reduced by building additional cavities and by expanding and upgrading the existing 1-MV prototype radiography LTD. An accelerator operating at 2-3 MV would produce fully developed MITL electron flow current. The system could then be used to evaluate the effect of MITL flow on the vacuum insulators in the LTD. The vacuum insulators are much closer to the outer conductor of the MITL than in a typical IVA system like RITS-6. A 2-3-MV accelerator could be used to conduct radiographic diode research and better evaluate the LTD when coupled to a high voltage MITL and loads very similar to the full 7-MV system. Changes to the radiography prototype could also be used to closer match the design presented in this report. Changing the capacitors from 20 nF to 12 nF would narrow the output pulse to match this design. This could be done within the existing 10-brick cavity or in a new 18-brick cavity.

PIC simulations were used in section 4 to evaluate the performance of a MITL with 72 cavities and only 9 impedance transition steps. The input voltage for each cavity in the PIC simulation was modeled as a voltage source and an impedance approximately equal to the cavity impedance. The voltage waveform was provided by circuit simulations. Additional PIC simulations will be used to couple a cavity circuit model directly to the MITL to study the effect of the dynamic impedance of the MITL on the cavity circuit. PIC simulations will also be used to estimate the electron current deposition on the vacuum insulators. Simulations could help with a redesign of the insulator if required. Simulations with a dynamic diode impedance will more accurately predict the diode voltage.

Tests of a single high current LTD cavity indicate that the current state of the art is very reliable. Circuit simulations of possible faults indicate that most faults would have little effect on the lifetime of the accelerator as a whole or on the shape and amplitude of the output pulse. Lifetime degradation is predicted to be confined to the cavity where the original fault occurs. Simulated fault experiments will be conducted in the next year on a single radiography cavity with additional voltage and current diagnostics. Faults will be simulated by manually shorting components

and disconnecting charge or trigger cables. Resulting voltage and current measurements will be compared to circuit simulations.

Reducing the inductance of the LTD circuit opens the door to several possible design improvements. Sandia LDRD funds are being used to investigate several low inductance switch geometries that could replace the existing switches [24]. A new lower inductance LTD geometry has been developed at HCEI with a single capacitor in each brick and a switch made of several series and parallel spherical electrodes. Reduced circuit inductance reduces the circuit impedance and allows for several design modifications. The existing design with 18 bricks per cavity could be expanded by adding additional cavities while maintaining the same load impedance and thus launching a higher forward going voltage into the same diode impedance. Another design option would be to reduce the number of bricks in each cavity to reduce the accelerator diameter and keep the same number of cavities.

Two different schemes have been proposed for producing two pulses separated by 100s of nanoseconds to several microseconds. We plan to test both schemes with a single LTD cavity to verify the feasibility. If a single LTD adder can be used to produce two pulses, then two x-ray images could be generated on the same axis. The LTD system in this report could then provide four images from the dual-axis system. Or project costs could be reduced by fielding only one accelerator to obtain two images.

References

[1] J. J. Leckbee, J. E. Maenchen, D. L. Johnson, S. Portillo, D. M. VanDeValde, D. V. Rose, and B. V. Oliver, "Design, simulation, and fault analysis of a 6.5-MV LTD for flash x-ray radiography," *IEEE Trans. Plasma Sci.*, vol. 34, no. 5, pp. 1888–1899, 2006.

[2] D. Johnson, V. Bailey, R. Altes, P. Corcoran, I. Smith, S. Cordova, K. Hahn, J. Maenchen, I. Molina, S. Portillo, E. Puetz, M. Sceiford, D. V. D. Valde, D. Rose, B. Oliver, D. Welch, and D. Droemer, "Status of the 10 MV 120 kA RITS-6 inductive voltage adder," in *Proc. 15th IEEE Int. Pulsed Power Conf.*, Monterey, CA, 2005, pp. 314–317.

[3] R. J. Allen, C. L. Berry, R. J. Commisso, G. Cooperstein, R. C. Fisher, D. D. Hinshelwood, T. A. Holt, A. T. Miller, D. P. Murphy, J. M. Neri, P. F. Ottinger, D. G. Phipps, J. W. Schumer, S. J. Stephanakis, S. B. Swanekamp, and F. C. Y. title =.

[4] I. Crotch, K. Thomas, K. Barry, P. F. Beech, M. Bockle, J. Bonnell, S. G. Clough, G. M. Cooper, M. Copping, S. J. Croxon, P. Evans, C. Goes, R. A. Hamlett, K. Johnston, A. Jones, P. Juniper, N. Kersley, P. Lockyer, P. N. Martin, J. Mclean, M. Myall, J. O'Malley, A. G. Pearce, C. Pearce, M. J. Phillips, S. C. Pope, K. P. Pullinger, D. J. Short, M. A. Sinclair, I. D. Smith, A. Stevens, A. L. Stevens, D. Swatton, N. Graneau, D. Honey, M. Swierkosz, M. J. Tyldesley, J. Wain, K. Webb, T. J. Williams, M. C. Williamson, R. Davitt, G. Jeffries, A. Parlour, N. Webb, R. Alban, and K. Stuart, "Pulsed power driven flash x-ray sources for the Hydrus project at AWE," in *Proc. 16th IEEE Int. Pulsed Power Conf.*, Albuquerque, NM, 2007, pp. 1085–1088.

[5] P. Corcoran, V. Carboni, I. Smith, V. Bailey, R. Altes, H. Kishi, J. Pearce, T. da Silva, D. Spelts, R. Stevens, B. Whitney, J. Douglas, J. DeRosa, T. Tatman, K. da Silva, K. Thomas, T. Bryant, M. Bockle, I. Smith, A. Summers, M. Swierkosz, and S. Fishlock, "Design of an inductive voltage adder based on gas-switched pulse forming lines," in *Proc. 15th IEEE Int. Pulsed Power Conf.*, Monterey, CA, 2005, pp. 308–313.

[6] I. D. Smith, "Induction voltage adders and the induction accelerator family," *Phys. Rev. ST-AB*, vol. 7, 2004.

[7] A. A. Kim, A. N. Bastrikov, S. N. Volkov, V. G. Durakov, B. M. Kovalchuk, and V. A. Sinebryukhov, "1 MV ultra-fast LTD generator," in *Proc. 14th IEEE Int. Pulsed Power Conf.*, Dallas, TX, 2003, pp. 853–854.

[8] J. Leckbee, S. Cordova, B. Oliver, D. L. Johnson, M. Toury, R. Rosol, and B. Bui, "Load line evaluation of a 1-MV linear transformer driver (LTD)," in *Proc. IEEE Int. Power Modulator Conf.*, Las Vegas, NV, 2008.

[9] A. A. Kim, V. Sinebryukhov, B. Kovalchuk, A. Bastrikov, V. D. S. Volkov, S. Frolov, and V. Alexeenko, "Super fast 75 ns LTD stage," in *Proc. 16th IEEE Int. Pulsed Power Conf.*, Albuquerque, NM, 2007, pp. 148–151.

[10] M. Toury, C. Vermare, B. Etchessahar, L. Veron, M. Mouillet, F. Bayol, G. Avrillaud, and A. A. Kim, "IDERIX: An 8 mv flash x-rays machine using a LTD design," in *Proc. 16th IEEE Int. Pulsed Power Conf.*, Albuquerque, NM, 2007, pp. 599–602.

[11] S. T. Rogowski, W. E. Fowler, M. Mazarakis, C. L. Olson, D. McDaniel, K. W. Struve, and R. A. Sharpe, "Operation and performance of the first high current LTD at Sandia National Laboratories," in *Proc. 15th IEEE Int. Pulsed Power Conf.*, Monterey, CA, 2005, pp. 155–157.

[12] A. A. Kim, A. N. Bastrikov, S. N. Volkov, V. G. Durakov, B. M. Kovalchuk, and V. A. Sinebryukhov, "100 GW fast LTD stage," in *Proc. 13th Int. Symposium on High Current Electronics IHCE*, Tomsk, Russia, 2004, pp. 141–144.

[13] M. G. Mazarakis, W. E. Fowler, D. H. McDaniel, C. L. Olson, S. T. Rogowski, R. A. Sharpe, K. W. Struve, W. A. Stygar, A. A. Kim, V. A. Sinebryukhov, R. M. Gilgenbach, and M. R. Gomez, "High current linear transformer driver (ltd) experiments," in *Proc. 16th IEEE Int. Pulsed Power Conf.*, Albuquerque, NM, 2007, pp. 222–225.

[14] D. V. Rose, D. R. Welch, B. V. Oliver, J. J. Leckbee, J. E. Maenchen, D. L. Johnson, A. A. Kim, B. M. Kovalchuk, and V. A. Sinebryukhov, "Numerical analysis of a pulsed compact LTD system for electron beam-driven radiography," *IEEE Trans. Plasma Sci.*, no. 34, pp. 1879–1887, 2006.

[15] J. Leckbee, J. Maenchen, S. Portillo, S. Cordova, I. Molina, D. L. Johnson, A. A. Kim, R. Chavez, and D. Ziska, "Reliability assessment of a 1 MV LTD," in *Proc. 15th IEEE Int. Pulsed Power Conf.*, Monterey, CA, 2005, pp. 132–134.

[16] D. Weidenheimer, P. Corcoran, R. Altes, J. Douglas, H. Nishimoto, I. Smith, R. Stevens, D. L. Johnson, R. White, J. Gustwiller, J. E. Maenchen, P. Menge, R. Carlson, R. D. Fulton, G. Cooperstein, D. Droemer, and E. Hunt, "Design of a driver for the Cygnus x-ray source," in *Proc. 13th IEEE Int. Pulsed Power Conf.*, 2001, pp. 591–595.

[17] S. Portillo, B. V. Oliver, S. R. Cordova, N. Bruner, D. Ziska, and D. Rovang, "Demonstration of the self-magnetic pinch diode as an x-ray source for flash core-punch radiography," Sandia National Laboratories, SAND SAND2007-6324, 2007.

[18] A. A. Kim, A. N. Bastrikov, S. N. Volkov, V. G. Durakov, B. M. Kovalchuk, and V. A. Sinebryukhov, "Development of the ultra-fast LTD stage," in *Proc. 14th IEEE Int. Conf. High-Power Particle Beams*, Albuquerque, NM, 2002, pp. 81–84.

[19] B. Bernstein and I. Smith, "Aurora, an electron accelerator," *IEEE Trans. Nucl. Sci.*, vol. 20, pp. 294–300, 1973.

[20] D. D. Hinshelwood, "Bertha: A versatile transmission line and circuit code," Naval Research Laboratory, Washington, D.C., Memorandum Report 5158, 1983.

[21] J. M. Creedon, "Relativistic brillouin flow in the high ν/γ diode," *J. Appl. Phys.*, vol. 46, no. 7, pp. 2946–2955, 1975.

[22] V. L. Bailey, P. A. Corcoran, D. L. Johnson, I. D. Smith, J. E. Maenchen, K. D. Hahn, I. Molina, D. C. Rovang, S. Portillo, E. A. Puetz, B. V. Oliver, D. V. Rose, D. R. Welch, D. W. Droemer, and T. L. Guy, "Re-trapping of vacuum electron current in magnetically insulated transmission lines," in *Proc. 15th Int. Conf. High-Power Particle Beams*, Saint-Petersburg, Russia, 2004, pp. 247–250.

[23] LSP is a software product of ATK-Mission Research, Albuquerque, NM.

[24] J. R. Woodworth, J. A. Alexander, S. F. Glover, W. A. Stygar, G. J. Denison, J. R. Blickem, F. E. White, L. M. Lucero, H. D. Anderson, M. J. Harden, and F. R. Gruner, "Low-inductance gas switches for linear transformer drivers," in *Proc. IEEE Power Modulator Conf.*, 2008.

[25] T. Hughes, S. Yu, and R. Clark, p. 110401, 1999.

[26] D. D. Hinshelwood, "Bertha: A versatile transmission line and circuit code," Naval Research Laboratory, Washington, D.C., Memorandum Report 5158, 1983.

DISTRIBUTION:

3 Voss Scientific
Attn: D. Welch, D. Rose, N. Bruner
418 Washington SE
Albuquerque, NM 87108

3 Naval Research Laboratory
Attn: G. Cooperstein
Code 6770
4555 Overlook Ave. SW
Washington, DC 20375-5346

1	MS 0139	John Maenchen, 1601
1	MS 1152	Steve Glover, 1654
1	MS 1181	Dillon McDaniel, 1650
1	MS 1181	Larry Schneider, 1650
1	MS 1189	Tom Mehlhorn, 1640
1	MS 1194	Bill Fowler, 1671
1	MS 1194	Keith LeChien, 1671
1	MS 1194	Mark Savage, 1671
1	MS 1194	Joe Woodworth, 1671
1	MS 1195	Steve Cordova, 1645
1	MS 1195	Kelly Hahn, 1645
1	MS 1195	David L. Johnson, 1645
1	MS 1195	Mark Johnston, 1645
5	MS 1195	Josh Leckbee, 1645
1	MS 1195	Isidro Molina, 1645
3	MS 1195	Bryan Oliver, 1645
1	MS 1195	Tim Webb, 1645
1	MS 1195	Derek Ziska, 1645
1	MS 1196	Michael Mazarakis, 1671
1	MS 1196	Bill Stygar, 1671
1	MS 0899	Technical Library, 9536 (electronic)

Sandia National Laboratories