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Final Report

Harsh-Environment Packaging for Downhole Gas and Oil Exploration

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Final Report:
Harsh-Environment Packaging for Down-hole Gas and Oil Exploration

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Executive Summary

This research into new packaging materials and methods for elevated temperatures and harsh environment electronics focused on gaining a basic understanding of current state-of-the-art in electronics packaging used in industry today, formulating the thermal-mechanical models of the material interactions and developing test structures to confirm these models. Discussions were initiated with the major General Electric (GE) businesses that currently sell into markets requiring high temperature electronics and packaging. They related the major modes of failure they encounter routinely and the hurdles needed to be overcome in order to improve the temperature specifications of these products. We consulted with our GE business partners about the reliability specifications and investigated specifications and guidelines that from IPC and the SAE body that is currently developing guidelines for electronics package reliability. Following this, a risk analysis was conducted for the program to identify the critical risks which need to be mitigated in order to demonstrate a flex-based packaging approach under these conditions. This process identified metal/polyimide adhesion, via reliability for flex substrates and high temperature interconnect as important technical areas for reliability improvement.

First, the adhesion of the Copper (Cu) trace to the polyimide was examined through modeling and experimentation. The key parameters for adhesion of Copper to the polyimide substrate are the adhesion material and thickness. Through modeling, a variety of materials were evaluated for stresses generated when the temperature becomes elevated. Chromium (Cr) and Titanium (Ti) were of particular interest due to their widespread use in industry while Tantalum and Nickel appear to have properties favorable in reducing the stress in the metal trace. In order to compare the performance of the each of the materials, test coupons with each of the adhesion layer materials were fabricated. In addition, a sample of commercial material from 3M with their Cr tiecoat process was included. A small design of experiments was conducted where pull-tests were used to characterize the adhesion of each metal to the polyimide when exposed to temperatures between 200°C and 250°C in a nitrogen and air environment for hundreds of hours. These experiments showed that GE's Cr process outperformed other adhesion materials such as Ti and 3M Cr. It was also discovered that an air ambient severely degraded the tiecoat adhesion due to oxidation. Another set experiments were performed to determine the effect of adhesion layer thickness (Cr) on the reliability of the metal traces. These experiments showed that the peel strength of the Cr adhesion layers were reliable for over 1000 hrs at 250ºC. While peel strength for each of the Cr thicknesses was maintained, the conclusion of these experiments was that a 500 A thickness provides adequate coverage while not causing metal cracking.

Another important risk to electronics packaging for high temperature applications is the reliability and design of thru vias necessary for multilayer or two-side board processes. Basic modeling of the via was performed to determine the geometry, materials, and layer thicknesses which minimize stress. These qualitative results showed a large dependence on the geometric variables. The lowest stress conditions were those with large diameter thru-hole vias with thick copper pads. Additionally, the stress was found to decrease with decreasing pad diameter and substrate thickness. It was also determined that changing

geometric processing variables such as increasing the substrate fillet radius dramatically reduced the magnitude of the stress while via taper had a negligible impact on via reliability. A test structure based on a daisy chain of vias was designed and tested by thermal cycling in nitrogen ambient from 30ºC to 250ºC. This test structure examined the role of geometric variables such as Cu thickness, and via diameter on the reliability of the via. Of the over 600 vias tested, no vias experienced a significant rise in resistance indicating a crack or failure over the 1200 cycles performed.

For high temperature interconnect of passive devices, five high temperature solders were selected for examination based on their melting point temperatures and strengths. These included some standard solders that are currently used in industry. The microstructure of each solder was examined both in wire and paste forms in order to understand the relationship between the microstructure and the material properties of the solder. Mechanical properties of the solder were evaluated using tensile testing and nanoindentation. Nanoindentation was used to determine the elastic modulus, hardness, and creep. Tensile testing was used to determine ultimate tensile stress, elastic modulus, and creep. The tensile testing was performed at a range of temperatures from room temperature up to 200ºC. These tests showed differences between room temperature material properties and those at elevated temperatures. As operating temperature approaches the melting temperature of the solder, elastic modulus and ultimate tensile strength degrade appreciably for each solder. In addition, some of the solders examined undergo a phase change between room temperature and 200ºC that can significantly affect the properties of solder. A finite element model of a typical solder joint was developed to predict plastic stain in the solder which is used as part of a fatigue life model. The material properties, determined by material characterization as a function of temperature, were used in this model in order to more accurately predict the plastic strain in the solder joint. These predictions were limited by the lack of integration of the creep properties in the fatigue life model and the lack of fatigue life models for these solders.

In order to substantiate the basic material analysis of the solder, test coupons were developed to experimentally determine the solder joint fatigue life. One set of tests focused on the relationship of pad metallurgy on the shear strength of the solder when exposed high temperature storage at 250ºC. These tests showed that a NiPdAu pad layer outperformed NiAu pad layers in terms of shear strength. In order to compare the results of the fatigue life model to experimental results, a set of daisy chained solder joint coupons were fabricated on a polyimide substrate using both 0804 and 2512 size resistors. These coupons were tested by thermal cycling in nitrogen ambient from 30ºC to 250ºC. These experimental results indicated that the 92.5Pb-5Sn-2.5Ag solder outperformed the other solders in terms of least number of failures after 277 cycles. This is in contrast with the predictions made by the FEA. The primary reasons for the differences between the experimental and analytic analyses are the possible non-planar stresses not accounted for by the model and the fact that the fatigue life model used is not particularly suited to the solders that were examined.

For active devices, multiple approaches for interconnect were evaluated including stud bumping, wire bonding, and ribbon bonding. Modeling of stud bump geometry was performed to determine how stress varies with geometry and where failure between the die

and substrate will occur. These results indicate that tall standoff heights provide more compliance. A process for stud bumping polyimide flex was developed and tested using silicon test die. These test coupons were thermally cycled in nitrogen ambient from 30ºC to 250ºC for over 500 cycles. From these tests, it was determined that higher substrate temperatures lead to more reliable stud bump joints. The test coupons were analyzed and failures were found to occur at the corner pads as predicted by finite element modeling. In order to develop wire and ribbon bond test coupons, a high temperature die attach material is needed to adhere the test die to the polyimide flex. A set of possible die attach materials were analyzed by high temperature storage testing and evaluated through shear strength and warpage measurements. Using the downselected die attach material, test coupons were assembled using both ribbon and wire bonding. These test coupons were thermally cycled in nitrogen ambient from 30ºC to 250ºC for over 277 cycles. The results of these tests were contrasted with the results from the stud bump testing in order to determine from these limited tests, the more reliable assembly method. This ranking showed that stud bumping was more reliable than wire bonding which was more reliable than ribbon bonding. However these results should be confirmed by more extensive and statistical tests.

Ultimately, an entire electronics assembly needs to be evaluated in order to show improved reliability in a high temperature environment. In order to assemble such a unit, a few areas need to be researched further. These areas includes local rigidization of flex for increased reliability and practical implementation in a high vibration environment, multilayer laminations for more complex systems, failure models with creep properties for more accurate failure life predictions, and study of the manufacturability of the different solder systems.

List of Acronyms

AFM	Atomic Force Microscopy
Ag	Silver
ASME	American Society of Mechanical Engineers
Au	Gold
BCC	Body Centered Cubic
CALCE	Center for Advanced Life Cycle Engineering
Co	Cobalt
COTS	Commercial Off the Shelf
CPB	Copper Pillar Bumping
Cr	Chromium
CTE	Coefficient of Thermal Expansion
Cu	Copper
EDS	Electron Dispersive Spectroscopy
FCC	Face Centered Cubic
FEM	Finite Element Modeling
FMEA	Failure Modes & Effects Analysis
Ge	Germanium
GE	General Electric
GEGR	General Electric Global Research
HTS	High Temperature Storage
IMC	Intermetallic Compounds
IMECE	International Mechanical Engineering Congress & Exposition
In	Indium
LCP	Liquid Crystal Polymer
LVDT	Linear Variable Displacement Transducer
MPDB	Multi-Parameter Database
MPT	Multi-Purpose Testware
Ni	Nickel
NIST	National Institute of Standards and Technology
N2	Nitrogen
Pb	Lead
Pd	Palladium
PI	Polyimide
SAE	Society of Automotive Engineers
Sb	Antimony
SEM	Scanning Electron Microscopy
Si	Silicon
SiC	Silicon Carbide
Sn	Tin
SOI	Silicon on Insulator
SUNY	State University of New York
Ta	Tantalum

T_g	Glass Transition Temperature
$T_{liquidus}$	Liquidus Temperature
T_m	Melting Temperature
$T_{solidus}$	Solidus Temperature
Ti	Titanium
W	Tungsten
XPS	X-ray Photoelectron Spectroscopy

Summary of Technology Transfer

The General Electric Global Research team and SUNY Binghamton have been active in disseminating results through the publication of papers and participation in panel discussions at important packaging conferences. To date, two conference papers have been accepted and presented. Other papers for both journal and conference proceedings are planned after the submittal of this final report.

- In November 2006, Dr. Aaron Knobloch attended the ASME (American Society of Mechanical Engineers) IMECE (International Mechanical Engineering Congress and Exposition) in Chicago, IL to give an overview of this program. The Electronic and Photonic Packaging division gave the invitation for Dr. Knobloch to speak as part of a panel discussion on MEMS and electronics packaging. This discussion was limited to an overview of the proposed work on this program and did not extend into any results from this program.

- In July 2007, a paper was presented by Harry Schoeller on the flex adhesion portion of this research entitled "Adhesive Tiecoat / Polyimide Interactions in High Temperature Flex Packaging" at the InterPACK '07 conference in Vancouver, British Columbia, Canada. This paper can be found as part of the proceedings of this conference.

- In November 2007, Harry Schoeller presented a paper based on portions of the solder characterization work entitled "Constitutive Relations of High Temperature Solders" to the 2007 ASME IMECE conference in Seattle, WA. This paper can be found as part of the proceedings of this conference.

- In November 2007, two abstracts were submitted to the HiTEC 2008 conference. The first abstract gives a summary of the results and outcomes of this research program. The second paper will give a more detailed overview of the solder mechanical and structural analysis performed by SUNY Binghamton.

- Other journal articles are planned for publications in the areas of flex adhesion, thru via modeling and testing, solder microstructural and mechanical testing. As these papers are finalized, the Department of Energy will receive copies for their approval.

List of Significant Accomplishments

1. Failure mode and effects analysis of technology approaches
2. Completion of polyimide adhesion models predicting materials and geometry suitable for reliability testing
3. Scanning Design of Experiments identifying potential tiecoat layers suitable for polyimide adhesion at temperatures > 200°C
4. Completed high temperature storage testing (250°C) of adhesion layers
5. Analysis and downselection of primary adhesion layer (Chromium)
6. Completion of via modeling predicting geometry for layout of test structures
7. Fabrication of test coupons for thru via reliability
8. Demonstrated reliability of 23 via coupons (30 vias per coupon) to thermal cycling from 35°C to 250°C (>1200 cycles)
9. Design and fabrication of test coupons for stud bump reliability
10. Process development for stud bumping of polyimide flex and bonding of silicon test die to polyimide flex
11. Demonstrated reliability of 5 stud bump coupons by thermal cycling from 35°C to 250°C (>500 cycles)
12. Failure analysis of thermally cycled stud bump test coupons
13. Microstructural analysis of high temperature solder paste and wire
14. Characterization of high melting point solder properties (modulus, hardness, and creep) with nano-indentation
15. Characterized the mechanical properties of five high temperature solders thru tensile testing at room temperature, 0.7Tm and 200ºC
16. Formulated a finite element model of a solder joined resistor in order to determine plastic strain generated in the joint
17. Using an analytical model, estimated the fatigue life for each solder joint based on the finite element model and material property measurements
18. Characterization of creep of high temperature solders using tensile test equipment
19. Process development for solder reflow of high temperature solders
20. Measurement of shear strength of solder joints as a function of storage time at 250ºC
21. Measurement of shear strength of solder joints as a function of metal pad composition
22. Fabrication of solder test coupons composed of a string of resistors with two resistor sizes for four high temperature solders
23. Completion of thermal cycling testing of solder test coupons from 35°C to 250°C (>277cycles)
24. Selection of four die attach materials for testing and performed preliminary high temperature storage tests examining shear strength degradation
25. Fabrication of wire and ribbon bond test coupons populated with test die using downselected high temperature die attach material
26. Completion of thermal cycling of wire and ribbon bond test coupons from 35°C to 250°C (>277 cycles)

Chapter 1 Technology Status Assessment

1.1 Assessment of Current Package Technology for Downhole Drilling
1.2 Establish System Reliability Test Methodology and Failure Criteria

1.1 Assessment of Current Package Technology for Downhole Drilling

In order to better familiarize ourselves with current technology in electronics packaging, we surveyed two GE businesses which serve as component suppliers for the Oil and Gas industry. GE-Sensing provides sensor solutions that are used for subsea wellhead pressure monitoring and also supply high temperature sensors used in aviation applications. The upper end of the temperature rating for electronics components marketed to these segments is 175°C. While higher temperature sensor elements are possible, this temperature limits the temperature of the electronics that could be used to amplify or temperature compensate the sensor. This can lead to a sensor signal with more noise and a millivolt output which is undesirable to the customer. Like most people in high temperature electronics, GE-Sensing uses test and screening procedures to understand the reliability of Commercial off the shelf (COTS) components that are not rated to the temperatures of service required for their applications. Since many of their applications in the Oil and Gas and Aviation markets require operation over many years, they identified a couple of key stumbling blocks to the development of sensors and electronics for temperatures greater than 400°F. First, component life and reliability is of specific concern especially operational amplifiers. Many of the commercially available op-amps made with Silicon on Insulator (SOI) processes do not possess the required stability over time (such as drift of the zero voltage). Also, the packaging and interconnect methods are expensive and may not translate to temperatures greater than 400°F. We identified a few key components that would necessary to package (actives and passives) for current sensor circuit layouts in order demonstrate the translation of flex packaging technology to an actual sensor and electronics that they would like to market.

GE-Energy's Optimization and Control business (formerly Reuter Stokes) sells sensors such as magnetometers and orientation modules for use in downhole oil and gas exploration. Similar to GE-Sensing, these sensors and their electronics are rated to 175°C and electronics are chosen from COTS components using test and screening procedures. Their typical electronics board is a rigid polyimide board (85N type such as those made by Arlon) which conforms to IPC4101/01 standards. This standard calls for low bromine (used as flame retardant) board materials because the high temperature causes corrosion of metals from the bromine leaking out of the board. GE-Energy uses board manufacturing vendors who specialize in board and assembly processes for high temperature, harsh environments such as downhole oil and gas exploration.

Discussion with Reuter Stokes identified a number of key package failures that should become more important as temperature increases. First, an overarching concern in the use of solder is the ionic cleanliness of board materials. Ultrasonic methods are generally used but this forces solvent in plastic SO8 packages that are typically used and causes subsequent failures when these components are brought up to elevated temperatures. As temperatures approach 400°F, plastic packages become less reliable and will need replacement with die-scale chip attach or ceramic packages which lean more heavily on solder interconnects. If ultrasonic methods are not used for cleaning, contaminants on the

board can form deposits such as carbon which can increase parasitics and ruin the performance of the electronics. Contaminants on the board can be a result of halides from flux used when reworking boards after sustaining component manufacturing defects. Use of a water based flux can resolve some of these issues but can lead to corrosion caused by humidity if not sufficiently cleaned.

GE-Energy supplied us with typical test and failure criteria they use to qualify current products and new board designs. These tests included high temperature storage and mixed vibration and temperature environments. The test specifications given were in line with those guidelines under consideration of the SAE Subcommittee AE-7B and the goals and objectives laid out by this program.

1.2 Establish System Reliability Test Methodology and Failure Criteria

Table 1.1 shows the ultimate specifications desired for electronic packaging for this program. In addition, consideration of the SAE Subcommittee AE-7B High Temperature Electronics Panel guidelines that are under development is being given. In order to demonstrate the reliability of different packaging technologies, we must abate the particular identified risks of each particular method, process or material. Table 1.2 details those risks and the appropriate testing and failure considerations for each risk mitigation.

Table 1.1. Specifications for packaging reliability for this program

Board Specifications		Minimum	Desired
Temperature			
	Storage	–40—440 °F	–40—440 °F
	Operating	400 °F	460 °F
	Maximum	440 °F	480 °F
Vibration		20G RMS	30G RMS
	Frequency	50Hz-2kHz	50Hz-2kHz
	Duration	4 hrs / axis	4 hrs / axis
Shock		1000 G 0.5 ms half sine	3000-4000 G 0.5 ms half sine
Lifetime		1200 hrs	3600 hrs
Enclosure Specifications		**Minimum**	**Desired**
	Pressure	15,000 psi	20,000 psi
	Hermetic Seal	10^{-8} cc/s	10^{-8} cc/s

Table 1.2. List of Tests and Failure Criteria

Technology	Risk	Test Method	Failure
Polyimide Substrate	Metal Line Delamination	High Temperature Storage	Pull Test strength below 4 lbs/in
Polyimide Substrate	Thru board via reliability	High Temperature Via Daisy Chain in Vibration & Thermal Cycling	Loss of Electrical Continuity
Interconnect	Stud bump failure	High Temperature Storage and Vibration, Die Shear	Loss of Electrical Continuity
Interconnect	Solder joint failure due to fatigue	Thermal Cycling and Vibration, Intermetallic growth study	Loss of Electrical Continuity, unstable intermetallics
Interconnect	Wire bond failure	High Temperature Storage & Vibration, Pull and Shear strength tests	Bond strength below 2-3 grams-force
Interconnect	Microvia	High Temperature Storage & Vibration	Loss of Electrical Continuity

Note: Loss of electrical continuity includes both open circuit condition or significant increase in resistance (>300 ohm).

Evaluate capabilities of different packaging technologies

A failure mode effects analysis (FMEA) was performed in order to better evaluate the risks of each particular technology and is shown in Figure 1.1. Appendix A shows a detailed compilation of the results.

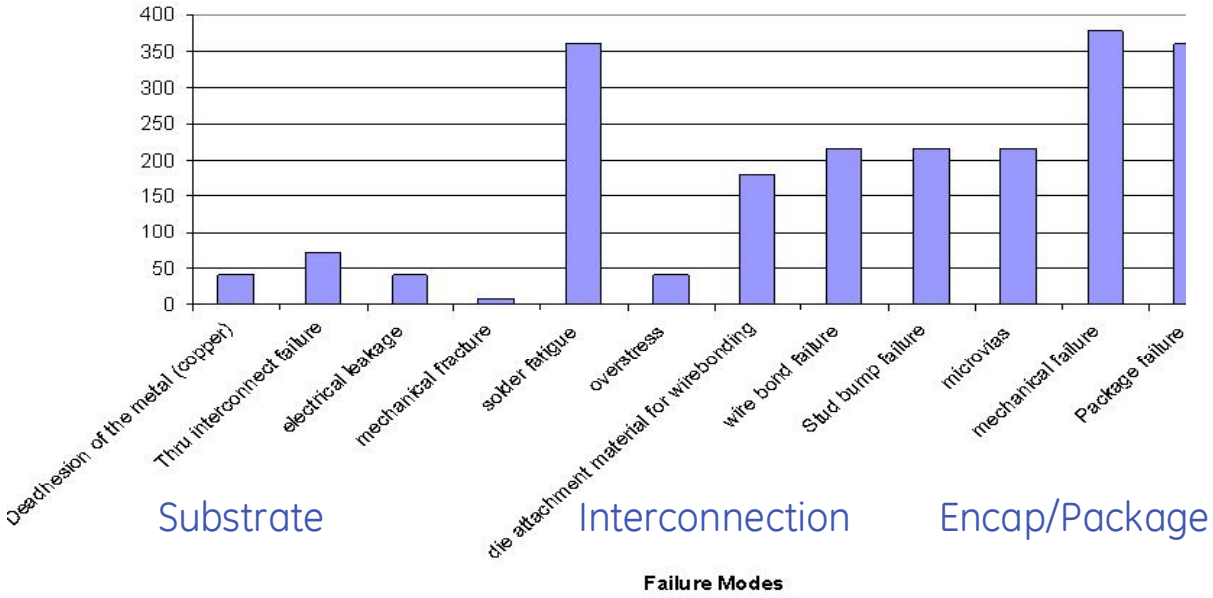

Figure 1.1. Results of FMEA analysis on interconnect and substrate technology. Increasing y-axis score denotes an increase in a combination of failure rate, impact of failure and difficulty of detection.

Chapter 2 Flex Adhesion Modeling and Characterization

2.1 Overview of Flex for High Temperatures

When examining the feasibility of using Flex-based packaging for temperatures greater than 400°F, there are two key areas of concern in regards to the board material. The first key metric is identifying a flex material with the performance and properties required for reliability as temperature is increased. An evaluation of the potential board materials (i.e. flex) was done through a survey of possible materials and their fundamental properties such as the glass transition temperature (Tg), the lateral and out of plate coefficient of thermal expansion (CTE), elastic modulus and yield strength. This application necessitates Tg greater than operation temperature, high strength, and closely matched CTE to Cu. Table 2.1 shows material properties for the flex materials considered for use in these environments. These materials span the breadth of polyimide films to liquid crystal polymers (LCPs).

Table 2.1. List of known flex substrate materials and their important electrical and mechanical properties.

Material	**Source**	**Dielelectic Const**	**Dissipation**	**CTExy**	**CTEz**	**Modulus**	**Tg**	**Tm**	**Tservice**
Type	*units*			*ppm/C*	*ppm/C*	*MPa*	*C*	*C*	*C*
LCP	Rogers R/Flex 3600	2.9	0.0025	17	150	2450		290	190
LCP	Rogers R/Flex 3850	2.9	0.0025	17	150	2450		315	190
Polyimide	Kapton H	3.5	0.009	25-30	81	2500	>400		300
Polyimide	Kapton E	3.2	0.0015	14-17	120	4900	>400		300
Kapton/FEP	Kapton® 150FWR019				135-234		350	270	
PIBO	Toyobo America	3.8	0.014	5	90	6000-8000	>600	NA	> 400
Polyimide glass	Arlon	4.7	0.015	15	55	12000	250		260
Cyanate Ester		3.8		12	55		250		
Polyimide/Quartz	Arlon 35NQ	3.5	0.009	9-10	50	12000	>250		
LCP	Xydar G930	3.9		3-7	40-80	15800			220
LCP	Xydar G430	4.2		-1	55	15900			
LCP	Xydar MG-350	3.9		7	60	16100			
LCP	Xydar M-345								
Upilex	Upilex-25S	3.5	0.0013	12	110	9120	>500	None	
Polyimide	Ultem			55	55	2850	245		
Polyimide/Glass	Arlon 85N	3.6	0.014	9	55	22063	250		

The second key area is the adhesion of the copper traces for the purposes of interconnecting the components and via reliability. Adhesion can be adversely affected by the choice of tiecoat layer used to bind the copper to the polyimide and the preparation of the substrate prior to the deposition of the tiecoat layer. Via reliability brings together the adhesion of the copper traces with the selection of the flex material. Conceptually, a flex material with higher CTE in the out of plane direction will generate higher stresses on the via. As a preliminary analysis, FEM of a via was run to examine the role of the material properties of the flex on the reliability of the via. This simple Finite Element Model (FEM) was performed using software available from Center for Advanced Life Cycle Engineering (CALCE) at University of Maryland. The inputs to this program mirrored the properties in Table 2.1 and used a temperature cycle consisting of 25 to 200°C. Figure 2.1 shows the results of this analysis. Another key input into the choice of substrate material are aspects related to the manufacture and commercialization of the technology. At General Electric Global Research (GEGR), our experience in flex material is mainly tied to Kapton E, Kapton H, some LCPs and Upilex.

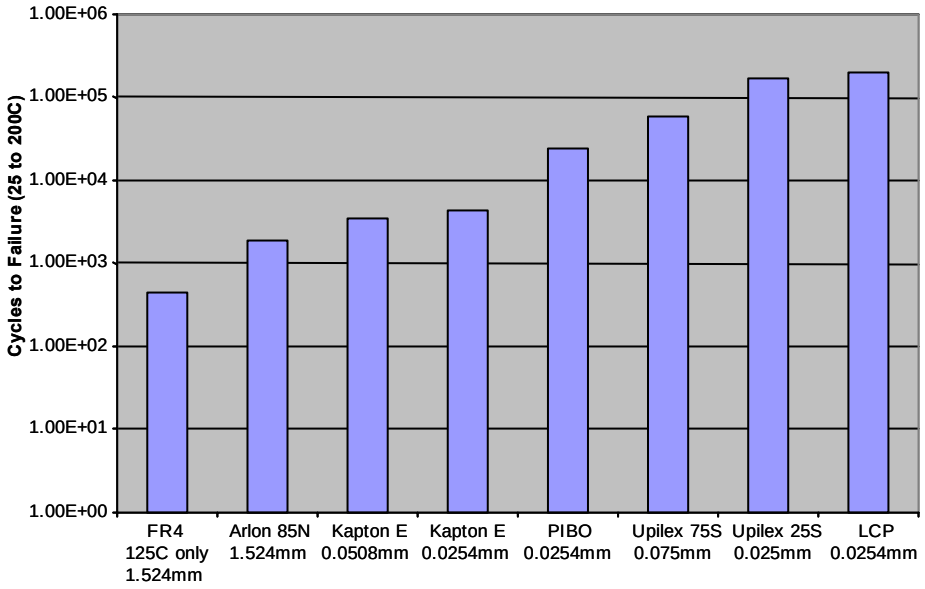

Figure 2.1. A comparison of the via reliability of several possible flex material substrates. It is important to note that common currently used substrates (such as FR4 or Arlon 85N) are much poorer performers than the flex substrate materials.

From these analyses, we decided to focus on Kapton E with a secondary interest in Upilex. Kapton E is the best CTE matched material in the x-direction and also has a low CTE in the z-direction. Use of Kapton E also leverages fabrication expertise and processes at the center and is widely used in industry outside GE. As a secondary choice, Upilex is attractive for many of the same reasons as Kapton E.

2.2 Modeling of Flex Adhesion at High Temperatures

Geometry, Boundary Conditions and Loading

A 2-D plane stress elastic-plastic finite element model consisting of a 1 mil polyimide substrate, 100 nm tiecoat, and 0.5 mil copper layer was generated using ANSYS 10.0. The geometry was mapped meshed using Plane 183 quadrilaterals as shown in Figure 2.2. Only half of the geometry was modeled due to symmetry and the elements were refined at the interface because of the stress concentration in this region. A fixed constraint was placed on the bottom left keypoint and a symmetry boundary condition was placed on the left hand side to constrain motion in the x-direction. In order to perform nonlinear elastic-plastic analysis, true stress-strain curves were used to document the material's constitutive response. Additional temperature dependent mechanical properties were obtained from the MPDB software and Dupont [1-2]. A uniform temperature load was applied to the system assuming no thermal gradients and perfect heat conduction throughout the package. The temperature was slowly ramped at 14°K/min from 298°K to 500°K.

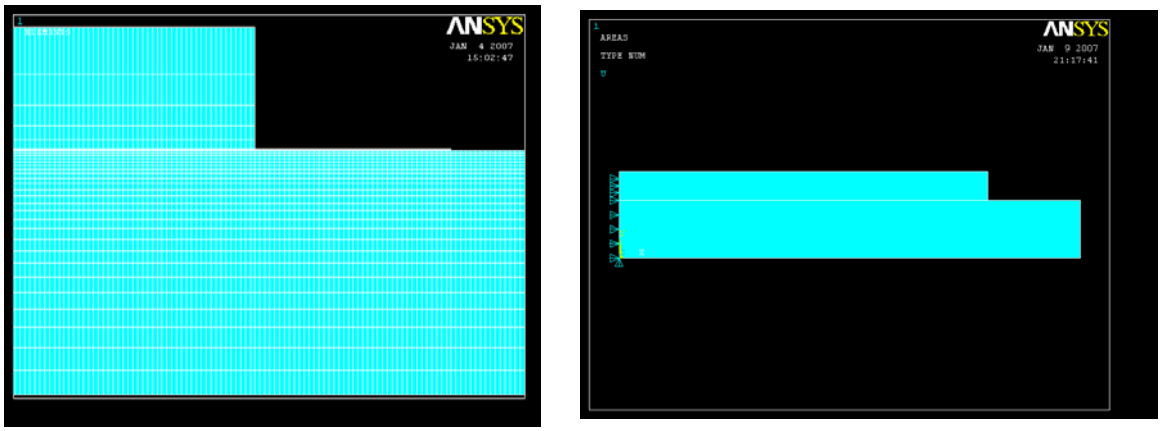

Figure 2.2. Left, shows a zoom view of the mesh at the interface. A large number of elements were used to preserve Ansys aspect ratio requirements for quadrilaterals. Right, an overview of boundary conditions placed on the 2-D plane stress model.

Adhesion Materials

Electronic packaging components with mismatched CTE generate stress which can affect the reliability of the package. These thermally induced stresses have been shown to cause delamination of thin films from the substrate and cracking in the films/substrate. The stress in a thin film due to CTE mismatch is given by:

$$\sigma = E \cdot \Delta\alpha \cdot \Delta T \qquad (1)$$

where σ is stess, E is elastic modulus, $\Delta\alpha$ is the change in coefficient of thermal expansion, and ΔT is the change in temperature [3]. Therefore the material properties of interest in the model are the temperature dependent coefficient of thermal expansion (α) and elastic modulus (E). Since polyimide (PI) and copper (Cu) have similar values of in-plane CTE, minimal amount of stress is generated at the Cu/PI interface. However, when an adhesion layer, with a different CTE, is introduced in-between the substrate and copper trace, large thermal-mechanical stresses develop. Since the CTE of both the substrate and copper trace are higher than most adhesion metals, the adhesion metal is placed under tension, while the substrate and copper trace are under compression at the bottom corners. The stress distribution at the interface causes slight concave bending in the package, so the top surface of the copper is in tension as shown in Figure 2.3. As expected in bending the tensile force is greatest in the center of the copper and gradually decreases approaching the edge. A contour y-displacement plot shown in Figure 2.3 verifies slight concave bending. Given that adhesion metals are high modulus materials, they are able to resist deformation and high stresses develop. Polyimide on the other hand accommodates the stress through larger elastic strains. Furthermore, the elastic strains in PI can be recovered at high temperatures due to stress relaxation, a characteristic of viscoelastic materials. A nodal contour image of the in-plane stress-distribution for a Cu/Ti/PI system is shown in Figure 2.4. The image verifies our earlier predictions showing both the copper trace and substrate under compression while the adhesion layer is under tension. In the zoom image we can see the highest stress occurs in the region where both the copper trace and polyimide are placing the adhesion metal in tension. The stress diminishes to the right where only the polyimide is pulling on adhesion layer. Also as expected, the magnitude of the stress is greater at the copper/adhesion layer interface than the adhesion layer/polyimide interface because of

the higher elastic modulus of the copper. Since the copper trace is under compression, the stress concentration is located on the outer edge of the interface.

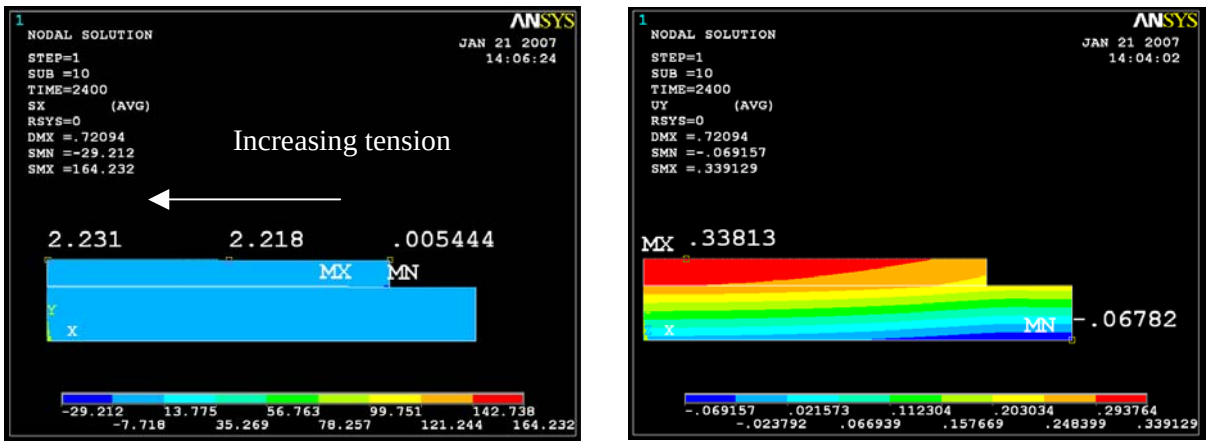

Figure 2.3. Left, contour image showing increasing tension on copper surface from the edge toward the center of the copper/Ti/polyimide system. Right, y-direction displacement plot showing concave bending in the model.

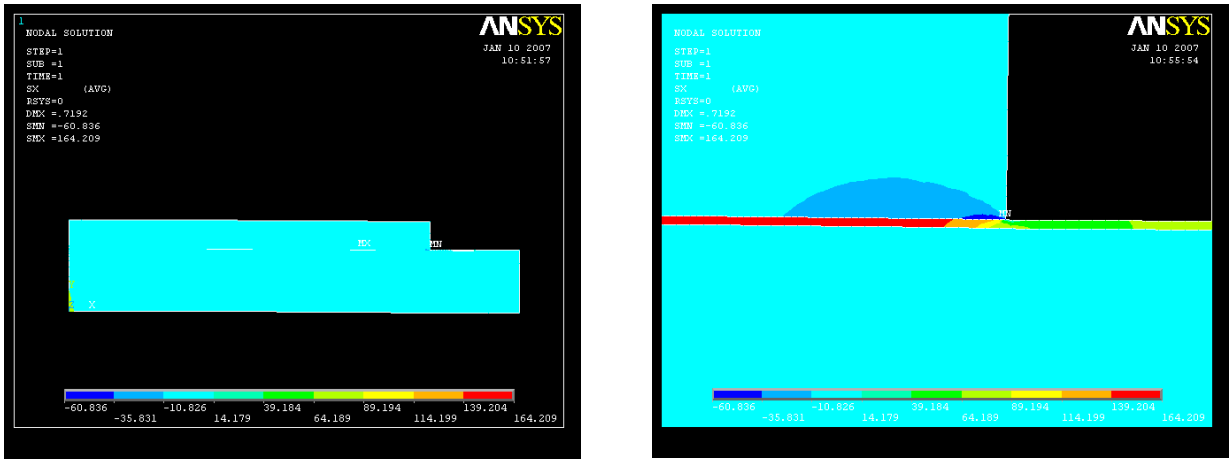

Figure 2.4. Nodal contour Image of σ_x in the copper/Ti/polyimide system. A zoomed in view on the right shows the adhesion layer under tension and the copper and polyimide under compression

A chart comparing the thermal-mechanical stresses generated for common adhesion metals is shown in Figure 2.5. Tungsten generates the largest stresses because of its particularly high elastic modulus (400 GPa) and low CTE (4 ppm/°C) [4]. Chromium also shows high stresses in the X direction, which exceed its yield strength. Since chromium has a body centered cubic crystal structure and has shown to be quite brittle in literature, there exists the possibility of cracking in the adhesion layer upon heating. Both copper and cobalt showed the lowest stress values because of their fairly low elastic modulus and matched expansion coefficients. However they are unsuitable as adhesion layers because of poor chemical bonding to polyimide [5]. The short and long-range diffusion of copper into polyimide due to the lack of a stable interface is well documented in literature [6]. It's interesting to note that both nickel and tantalum show similar stress values

despite having different material properties. This occurs because the elastic modulus of copper (126 GPa) is closer to tantalum (182 GPa) than nickel (204 GPa), conversely the CTE of copper (16.7 ppm/°C) is closer to nickel (12.6 ppm/°C) than tantalum (6.6 ppm/°C) [7-8].

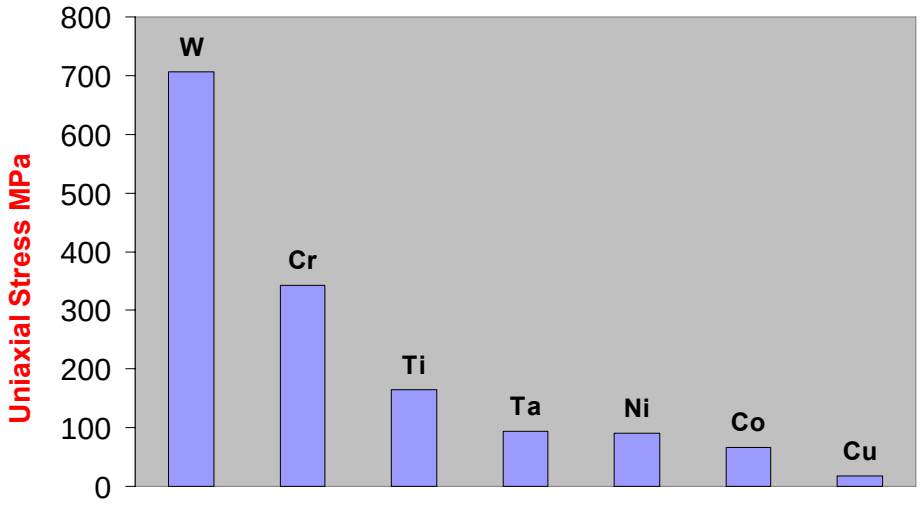

Figure 2.5. Plot comparing the maximum uniaxial σ_x stress for several common adhesion materials.

To compare which mechanical property has the most influence on stress generation, both CTE and modulus were varied while keeping all other material properties constant. Figure 2.6 shows the effect of varying the adhesion layer modulus from 2 GPa to 400 GPa. This resulted in a 15800% increase in the uniaxial x-direction stress in the adhesion layer from the low stress state of matched modulus to the grossly mismatched W/PI combination. Likewise, the CTE was varied from 17 ppm/°C to 3 ppm/°C, which resulted in a 2598% increase in the uniaxial stress (Figure 2.6). So it can be concluded that when the modulus of the tiecoat is well matched to Cu less stress develops than with favorably CTE matched tiecoat/PI combinations.

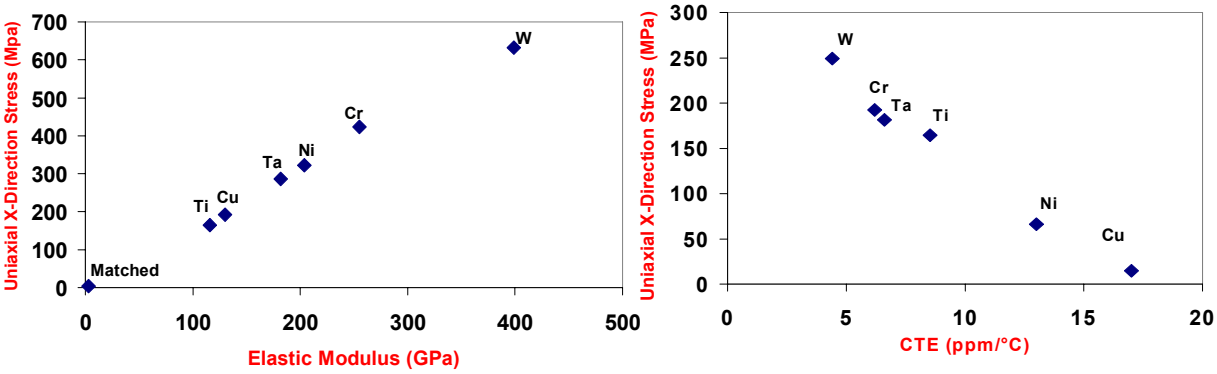

Figure 2.6. Plots showing the effect of changes in CTE and tiecoat modulus on the unixial stress generated in the tiecoat layer. The effect of varying the CTE or tiecoat modulus was performed while the other properties in the model were assumed to be that of Titanium.

Lastly, for the adhesion layer modeling, we examined the effect of changing geometry within the Cu/Ti/PI system. Figure 2.7 shows the effect of varying the thickness of the tiecoat material. By increasing the tiecoat thickness from 400 A to 2000 A, there was only a 3% decrease in stress. This is most likely a result of the thicker layer being able to accommodate higher stresses. The copper trace thickness was also varied to determine its contribution to the stress profile. Figure 2.7 shows a small increase in stress with increasing copper trace thickness. Finally, the thickness of the polyimide substrate was varied from 25 microns to 100 microns as seen in Figure 2.8. Only a negligible 1% increase in stress was found with increasing substrate thickness.

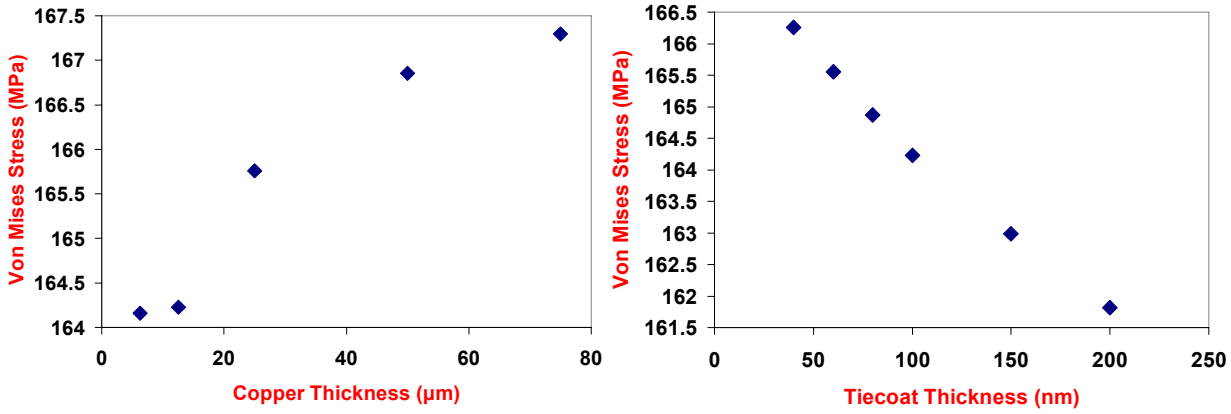

Figure 2.7. Left, plot showing the effect of copper trace thickness on stress generated in the adhesion layer. Right, this plot shows the effect of increasing the thickness of the adhesion layer on the stress generated in the adhesion layer.

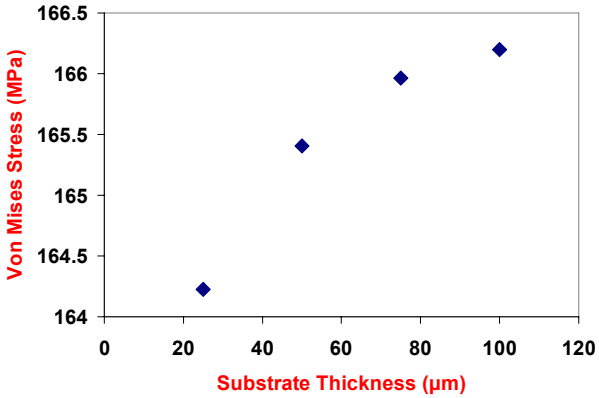

Figure 2.8. Plot illustrating the effect of substrate thickness on stress developed in the adhesion layer.

2.3 Adhesion Validation Testing

In order to confirm and validate the preceding analysis, test coupons for determining the adhesion strength and reliability were fabricated. Our initial screening of tiecoat layer materials consisted of the GE standard process of 1000 A Ti, 500 A Cr, 500 A Ni and a commercially available ~200 A Cr seeded Cu from 3M. Each of these adhesion layers was deposited using sputtering (thin copper seed) and covered with an electroplated Cu 1 mil thick. A GE proprietary preparation process was used on the substrate to facilitate

adhesion of the tiecoat layer. New etching processes were developed for Ni and Cr for the GE samples since these are not typical tiecoats used at GEGR. The 3M sample was copper clad polyimide and patterned to form the test lines for the peel test. In order to process the thin polyimide (1 mil), a GE proprietary process for stretching the polyimide (Kapton E in this case) over a 4 inch diameter metal hoop was used. This process allows for the samples to be handled more easily and for the process to be done in batch. At 3M, their more industrial process involves a roll-to-roll machine that streamlines the deposition and patterning of the thin polyimide. Each hoop of Kapton contains 7 peel test samples. After the Cu is plated on the patterned lines of tiecoat, the Kapton E is laser cut into 2 inch squares and separated from the hoop. A small number of hoops were processed in order to assess basic reliability of the different tiecoat layers.

Figure 2.9 shows the test setup used to measure the adhesion strength of various tiecoat-substrate combinations. Prior to any peel tests being performed on the samples, a lamination process is performed. The polyimide sample is attached to a 2 inch by 2 inch alumina substrate with a Dupont pyralux adhesive attach at 200°C. As seen in Figure 2.9, the laminated sample is held to a flat steel plate (stage) with two clamps. The operator starts the peel manually and attaches the metal strip to the jaws of the tester. The head of the machine is comprised of a force gage which measures the force exerted on the part in order to peel the metal. The stage is spring loaded such that the head of the peel tester maintains a 90 degree angle with the sample. The peel strength is calculated by dividing the force measured by the width of the line. Each coupon of Kapton contains 4-5 metal peel strips. The accuracy of the peel test is approximately 0.5 lb/in.

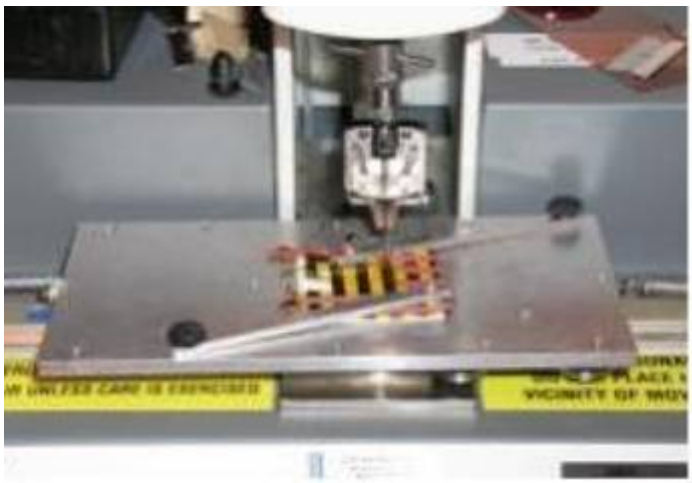

Figure 2.9. Photograph of peel test apparatus at GEGR for measuring adhesion properties of Cu lines to polyimide substrates. A sample coupon is shown under test.

In order to study the effect of ambient conditions and high temperature storage on this series of tiecoat layers, a set of tests were performed on the test coupons. Results of these tests can be found in Table 2.2. Initially, we characterized the adhesion strength of the tiecoat layers prior to any storage conditions to get a baseline. In the flex industry, a peel test result greater than 3 lbs/in denotes good adhesion. Our process typically yields 6-8 lbs/in for Ti tiecoats on Kapton E. After this baseline, coupons were subjected to either 200°C or 250°C in either air or N_2 atmosphere for up to 100 hrs. The data shows that the air ambient samples were outperformed by the inert samples. This is due to the

oxidation of the tiecoat layer degrading the bond between the polyimide and the tiecoat. This oxidation causes the metal – carbon bonds to become metal – oxygen bonds which are not as strong. After 100 hr, adhesion layer peel strength drops to an unacceptable level. The data for the air ambient testing shows a slight trend between the effectiveness of the different tiecoat layers. The 3M Cr samples appear in 3 of the 4 tests to significantly under perform as compared to the GE Ti or GE Cr. This may be due to the thinner tiecoat layer which is estimated in Table 2.2 as 200 A but may be much thinner. An adhesion layer of this thickness may not uniformly cover the polyimide, forming island-like structures. If the tiecoat is not uniform across the polyimide, it may allow Cu to diffuse into the polyimide resulting in catalyzed thermal oxidative degradation of the polyimide, and ultimately poor adhesion. Another reason for the poor performance in air could be that the degradation of PI is accelerated due to oxidation as has been shown by Tsukiji et al. [9].

Table 2.2. Final results of a Design of Experiments on different adhesion layers at various temperatures and under various ambient conditions using pull testing. All pull test data is in lbs/in and is averaged from multiple samples. Testing error is considered to be ±0.5 lbs/in.

Adhesion layer	0hr/RT	10hr/200C	100hr/200C	500Hr/200C	10hr/250C	100hr/250C	500hr/250C	10hr/250C	100hr/250C
	Air	Air	Air	Air	Air	Air	Air	N2	N2
GE Ti	6.8	3.5	0.96		2.5	1.3		4.1	6.9
3M Cr (~200A)	6.8	2.5	1.8		1	0.65		5.1	
GE Cr (500A)	6.2	3.6	1.8		2.2	1.3		6.9	5.79
GE Ni (500A)	8	0.1	0.9		0.75	0.05		6.6	6.6
GE Ta (500A)	6.7		2.7	0.95	3.58	2.45	1.12	7.1	6.35

Testing on samples annealed in nitrogen ambient shows much more positive results for the peel strength. After 10 hrs at 250°C, all of the tiecoat layers maintained significantly higher peel strength than the air samples. X-ray Photoelectron Spectroscopy (XPS) scans of the peeled interfaces showed failure occurring in the bulk polyimide for the Cr nitrogen annealed samples, and at the TiO_2/PI interface for the air annealed Ti sample. This indicates that the strength of the polyimide is the limiting factor when annealed in inert environments. In addition, the GE Cr sample showed no degradation in peel strength over this short period of time. The samples of Ti and 3M Cr still showed some degradation which may be due to the smaller thickness of the Cr on the 3M sample which is also supported by the FEA results. The source of the Ti failure is still under investigation. The Nickel samples also looked promising in maintaining their adhesion to the polyimide and is garnering further consideration.

Tantalum is an interesting tiecoat material due to its high resistance to oxidation as compared to Ni, Cr or Ti which could enable non-hermetic applications. The data in Table 2.2 shows that Ta generally outperformed other tiecoats in an air ambient but did not provide an adequate solution to prevent oxidative degradation of polyimide. Figure 2.11 shows a comparison of Ta peel strength to that of Ni.

Figure 2.10. A microscope image of stress cracking on a 2000 A thick Cr sample.

High temperature storage testing of Cr adhesion layers was performed in order to characterize the reliability of the adhesion layer in relation to thickness. More than 30 test samples were fabricated with varying thicknesses of Cr from 125 A up to 2000 A. It was found in the particular process used here that for Cr thicknesses above 1000 A tend to forms cracks (Figure 2.10) which could have a negative impact on our results. Our set of samples focuses on thicknesses up to 1000 A with a couple of samples of 1500 A and 2000 A thickness. Intermediate samples were taken out at times up to 1000 hrs and systematically pulled in order to understand and predict life of these interfaces. Figure 2.12 shows a summary of these results at 250°C in nitrogen ambient. All of the Cr adhesion layers irrespective of thickness performed well up to 1000 hrs at 250°C. For each adhesion thickness, multiple frames were fabricated and the samples for each high temperature storage time were selected such that frame variation did not impact the results. It is interesting to note that the slight dip in the results for peel strength at 100 hrs. It is believed this is a result of some brittleness in the polyimide for these samples that was not present in other samples at other storage times. This brittleness of the polyimide may have adversely affected the pull test data to represent a slightly lower value. However, the values at 100 hrs are still higher than the minimum necessary peel strength of 3 lbs/in. It appears from the data that thinner adhesion layer thicknesses such as 125 A and 500 A appear to outperform their thicker counterparts. Also, it is important to remember that there appeared to be some cracking in the thicker adhesion layer thicknesses such as 2000 A which could degrade the performance in longer testing. There is some risk with 125 A thick Cr that there may be incomplete coverage of the polyimide which could possibly degrade the adhesion due to copper's poor adhesion to polyimide. From these results, it was determined for future polyimide testing (such as via reliability and high temperature interconnect) that 500 A Cr is an appropriate adhesion layer thickness which will maintain reliable adhesion to the polyimide.

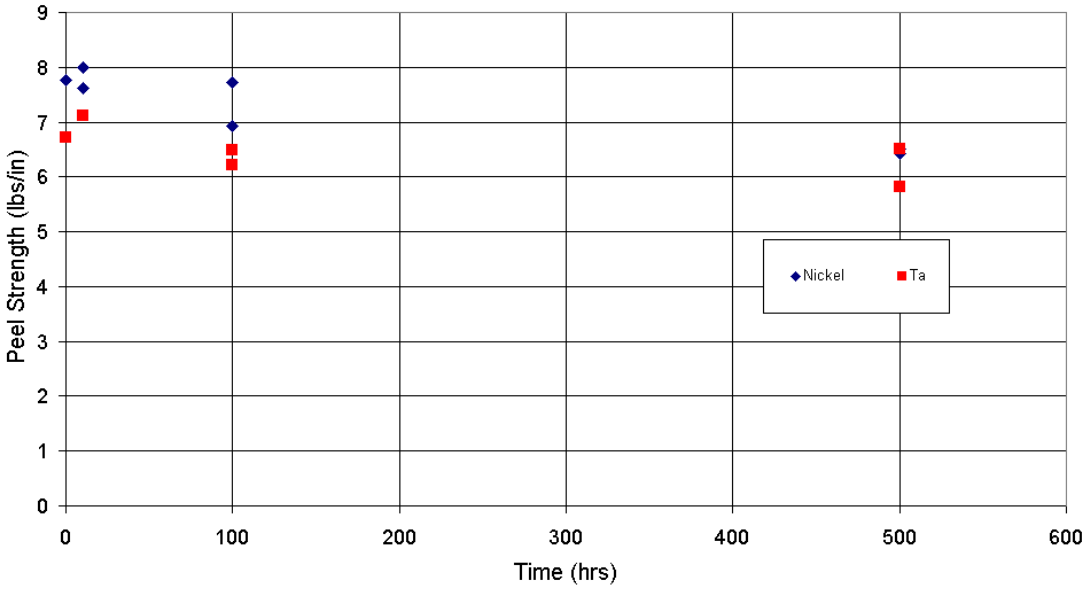

Figure 2.11. Comparison of Ni and Ta tiecoat layers at 250°C in nitrogen ambient.

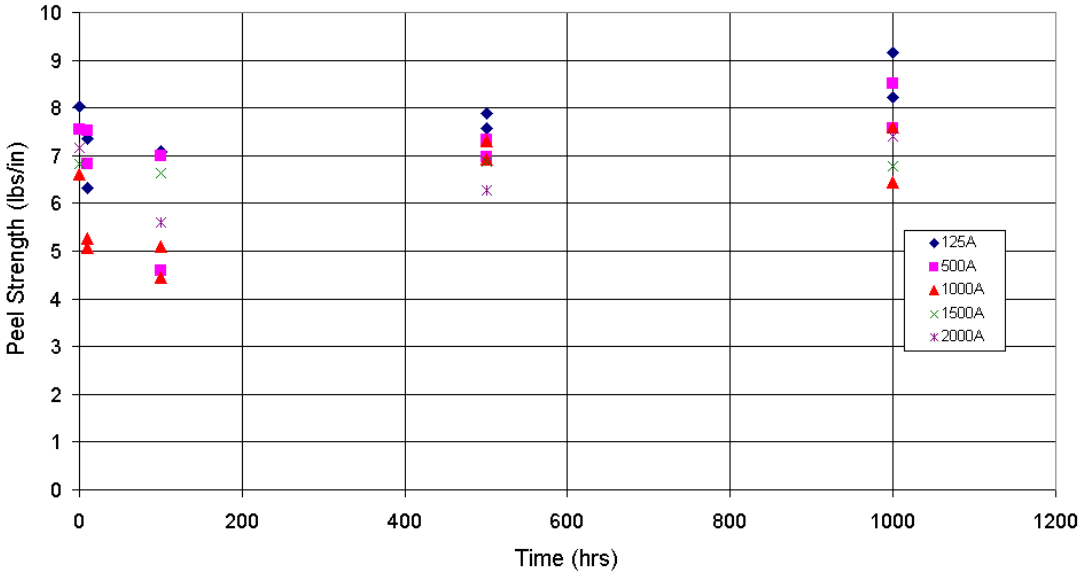

Figure 2.12. Peel strength variation of Cr tiecoat layers at 250°C in nitrogen ambient.

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Chapter 3 Thru Via Modeling and Characterization

3.1 Via Design and Modeling
3.2 Validation of Thru Via Reliability

3.1 Via Design and Modeling

Reliability of copper thru-hole vias in flex packaging is a function of both material selection and geometry of the via. An appropriate adhesion layer material binding the copper trace to the polyimide should have matching mechanical properties as was discussed in the prior section. The geometry of the via should be designed in such a way to minimize stress concentrations to enhance the overall reliability of the structure.

Two important material design parameters are the choice of adhesion layer material and substrate. In addition to being matched in CTE and modulus the adhesion layer material should be fairly ductile to accommodate high stresses without cracking. Due to its geometry and the inherently large out-of-plane CTE of polyimide, vias generate larger stresses than the flat regions of the flex package. For this reason, more ductile metals such as Face Centered Cubic (FCC) nickel may be able to withstand higher temperatures and more cycles without cracking than brittle metals such as Body Centered Cubic (BCC) chromium. Additionally, it was shown in the previous section that FCC adhesion layer metals generate less stress because they are more closely matched to the copper trace in modulus and CTE.

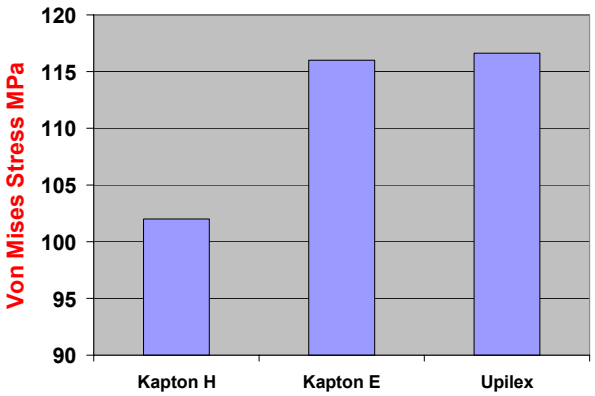


Figure 3.1. Chart comparing the maximum von Mises stress in copper with different types of polyimide substrates.

Selection of a suitable substrate material is crucial in via reliability. Since most of the common polyimides have similar in-plane CTE and modulus, out-of-plane CTE becomes an important parameter in the selection of a substrate material. As will be discussed later, larger out of plane thermal expansion increases the bending force on the copper trace of the via, thereby limiting the reliability of the package. A comparison of stresses generated in Kapton E, Kapton H and Upilex is shown in Figure 3.1. From the chart it can be seen that Kapton H generates lower stresses because of its smaller out-of plane CTE and lower elastic modulus.

The via should be designed in such a way as to minimize stresses arising from CTE mismatch. Parameters such as substrate thickness, substrate fillet, via diameter, via fill percentage, pad thickness, pad diameter, and via taper were all varied to determine their relative contribution to stress generation in the package. To study these parameters, a FEM was generated of an individual via using Ansys. A modeling Design of Experiments

was created to compare the effect of each parameter and to determine which combination of features leads to the lowest stress state.

Figure 3.2 shows the Design of Experiments results of the stress developed in the linear-elastic 3-D model. The results were separated by parameter to understand their relative contribution. In the side-by-side comparison copper thickness and via diameter are the most influential parameters of the Design of Experiments. To a lesser effect, Kapton H and Kapton E depicted as 0 and 1 respectively, and the substrate thickness influenced the outcome of the Design of Experiments. The magnitude of the stress was consistently lower with a 25 micron Kapton H substrate.

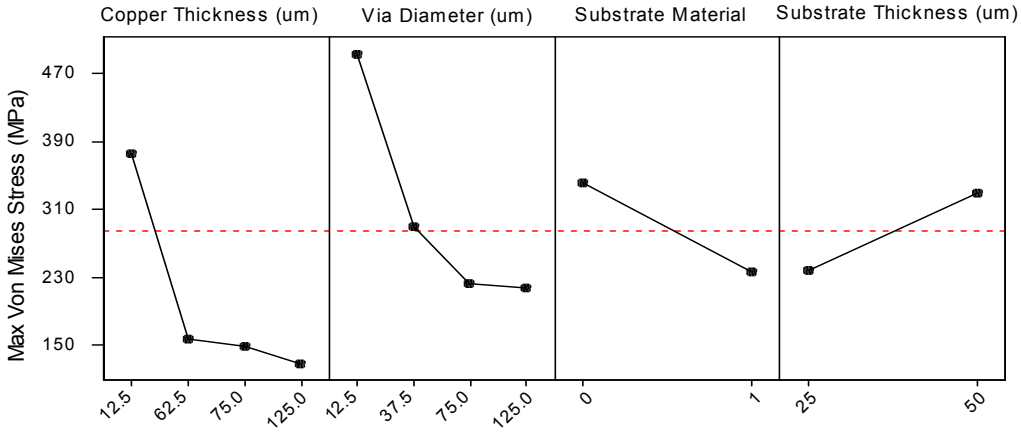


Figure 3.2. Results from Design of Experiments for optimizing via geometry using Ansys 3-D linear elastic models.

To further understand the role of individual geometric variables, each parameter was plotted against stress through its range of values. Figure 3.3 shows the variation in stress in the copper pad as via diameter is increased from 10 mils to 60 mils. With increasing via diameter, the maximum von Mises stress in the copper decreases. This is understandable since larger diameter vias are more effective in distributing stress around their circumference. Via fill was also examined to see its effect on stress in the copper pad as shown in Figure 3.4. The magnitude of the stress varies very little when increasing the via fill from 10% to 100%. However, an important observation here is that the location of the largest stresses changes with via fill percentage. These results show that after roughly 25% via fill, large stresses are no longer located on the inner diameter of the via. It is important that the inner diameter remain free of residual stress that negatively affects package reliability.

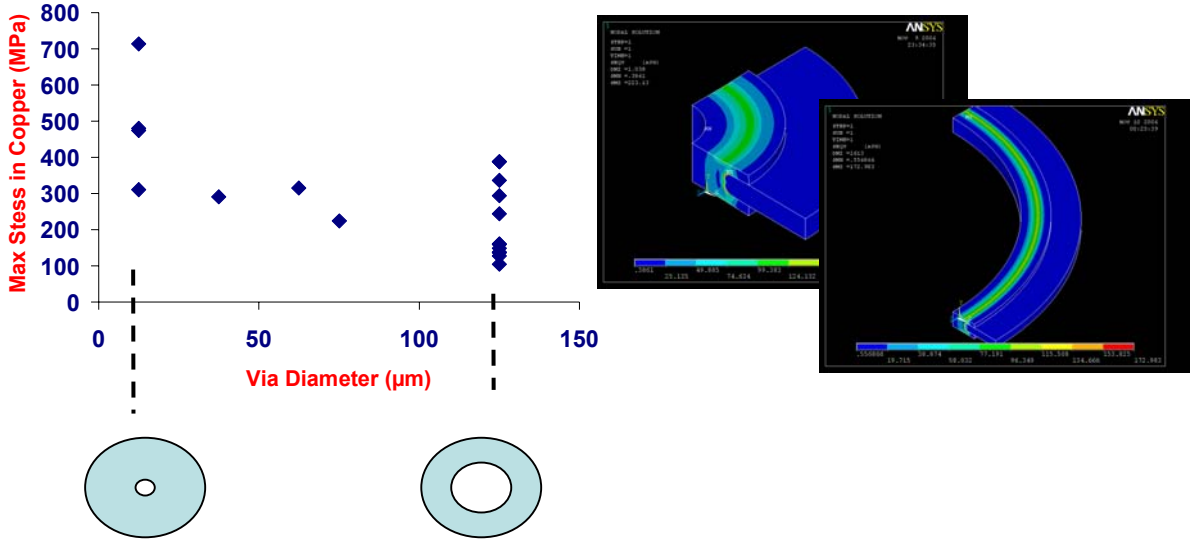


Figure 3.3. Results of a Design of Experiments showing stress as a function of via diameter. Image to the right is a nodal contour image of the models showing the geometrical extremes.

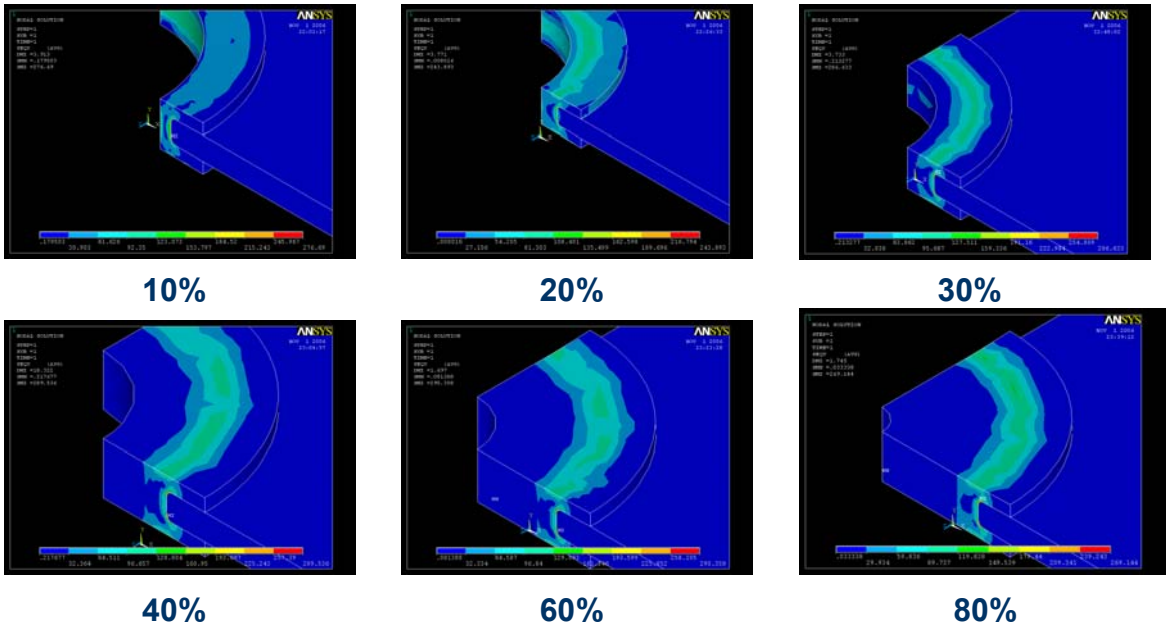


Figure 3.4. Nodal contour image of stress propagation with increasing via fill.

Based on this model, the parameter that has the largest influence on the magnitude of the von Mises stress is the fillet radius of the polyimide substrate. Figure 3.5 shows that increasing the fillet radius from 0.1 micron to 10 micron results in a 300% decrease in the maximum von Mises stress. High stress concentrations can lead to crack formation at the polyimide/adhesion layer interface, which will most likely propagate through the copper. If the fillet on the polyimide cannot be rounded because of processing issues, a ductile adhesion layer metal with a larger plasticity should be used. Via hole taper is another processing related geometry that was investigated through our model. In Figure 3.6, an exaggerated via with a 50% taper was compared to a straight via. The tapered via showed both a shift in the location of the stress concentration and an increase in the

magnitude of the stress. This is thought to be a consequence of increasing the length of the moment arm of the bottom copper trace.

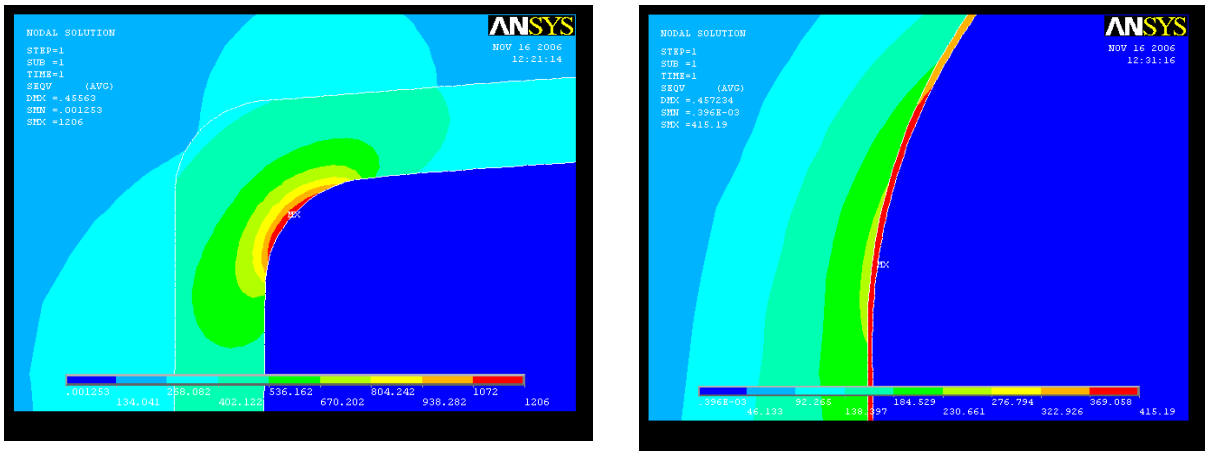


Figure 3.5. Nodal contour image of stress in the substrate fillet of the via.

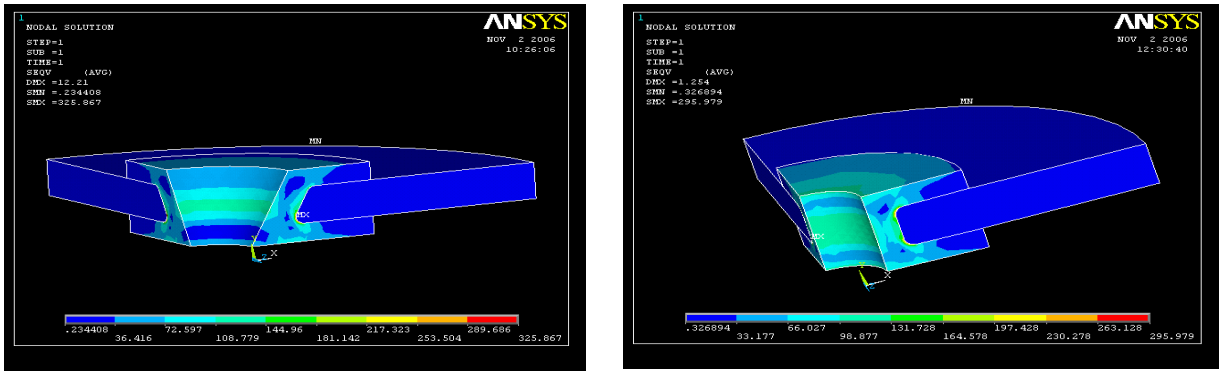


Figure 3.6. Nodal contour image of stress in tapered vias. Image to the left shows a 50% taper, image on right is a straight via.

The thickness and length of the copper pad also influenced the stress distribution in the via. Figure 3.7 is a chart from the Design of Experiments plotting the maximum stress in copper as a function of pad thickness. The trend of these results shows decreasing von Mises stress as the copper thickness is increased from 0.5 mils to 6 mils. Physically, this makes sense since a thicker pad should be able to absorb larger stresses. In a similar run, pad diameter was varied to examine its effect on the stress generation in the via. Like the taper results, the magnitude of the stress concentration at the copper/polyimide interface increased 30% as the pad diameter was varied from 0.5 mils to 6 mils as measured from the end of the substrate. Again the increasing length of the moment arm of the copper trace can explain the result found in Figure 3.8.

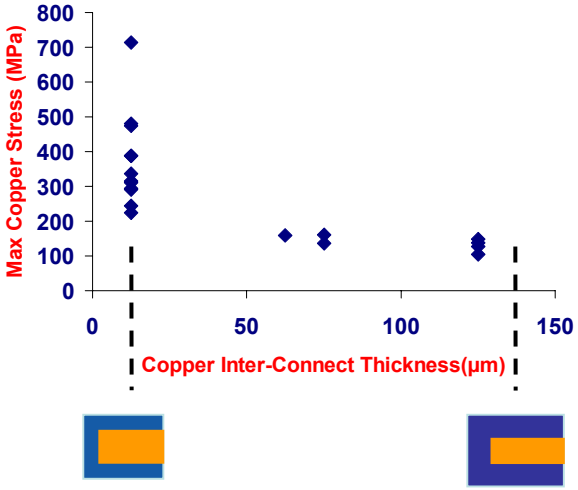


Figure 3.7. Results of Design of Experiments showing stress as a function of pad thickness.

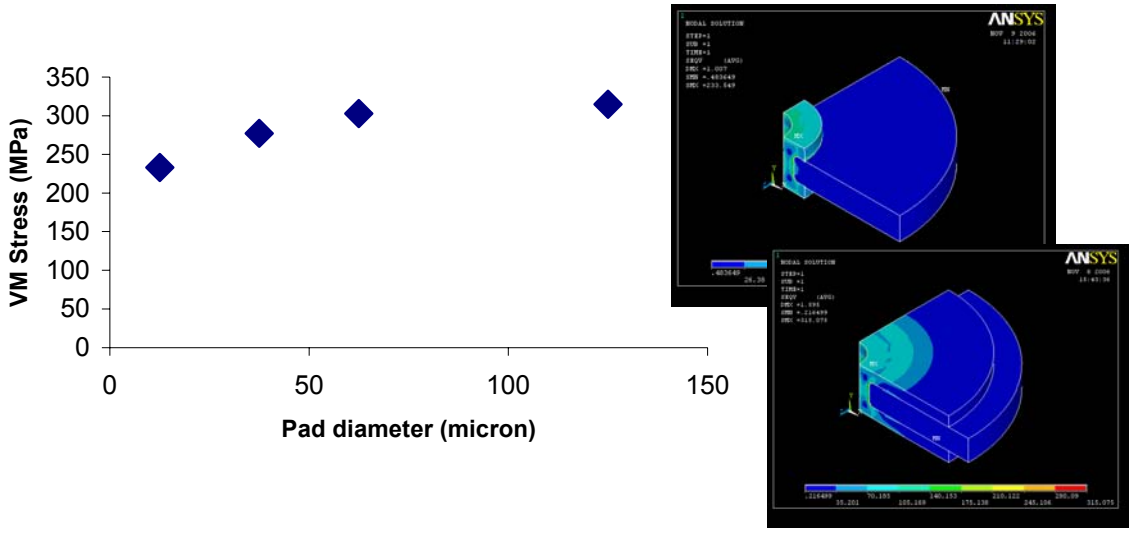


Figure 3.8. Result of FEM showing stress as a function of pad diameter. Image to right shows complimenting 3-D models used in the simulation.

The last geometric parameter varied in the Design of Experiments was the thickness of the polyimide substrate. Two common polyimide thicknesses 25.4 micron and 50.8 micron were compared in the Design of Experiments. The thinner substrate thickness was found to generate less stress as seen in Figure 3.9. This is in part due to the increasing length of the vertical moment arm in the via, which in turn increases the magnitude of the stress at the copper/polyimide interface stress concentration.

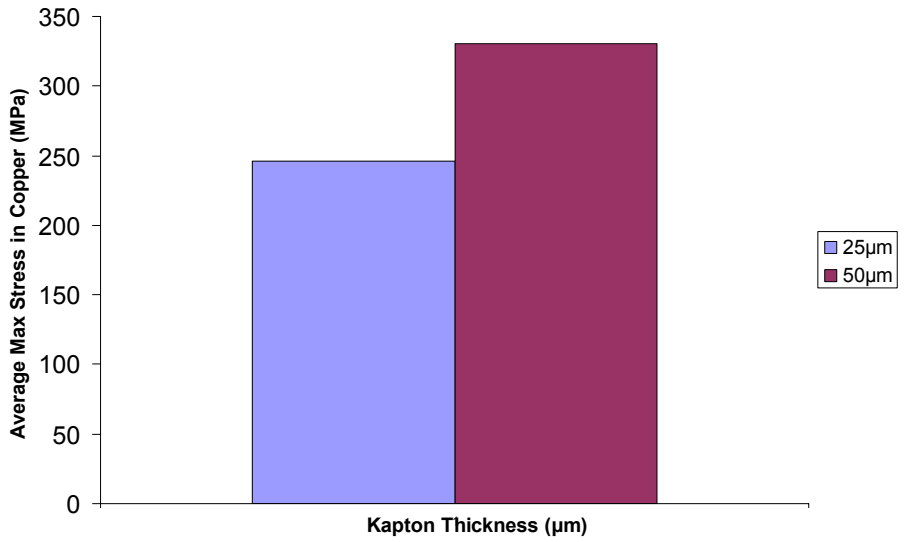


Figure 3.9. Results of the FEM comparing different polyimide substrate thicknesses.

In this section, we looked at the basic mechanics of copper/tiecoat/polyimide interactions at high temperatures for thru-hole vias. Via modeling showed a large dependence on the via geometric variables. Results from several modeling Design of Experiments showed that large diameter thru-hole vias with thick copper pads exhibited the lowest stress state. Additionally, the stress was found to decrease with decreasing pad diameter and substrate thickness. Changing geometric processing variables such as increasing the substrate fillet radius dramatically reduced the magnitude of the stress while via taper had a negligible impact on via reliability leading to corner cracks.

3.2 Validation of Thru Via Reliability

Reliability of via connections in printed circuit substrates is critical in practical applications to route conductors between components in a circuit. The thermal expansion of the substrate is typically greater through its thickness due to constrain structure of the laminate in its plane. Finite Element modeling indicates that via diameter and plating thickness are significant factors in stress in the via and Kapton E had lower stress than Kapton H. A test plan was formulated to validate the modeling results. Copper thickness and via diameter were selected as principle factors to vary in the experiment.

Daisy chained vias (30 per chain) were designed in 1 mil Kapton E with four different via diameters and four different plating thicknesses. An adhesion layer of 500 A Cr and a finish layer of 1 um Ni/1500 A Au were used on all test samples. Figure 3.10 shows a top view of the coupon that was designed for this test. The resistance of via chains is measured after cycle intervals. A profile of 7 cycles is shown in Figure 3.11. A Blue-M Ultra Temp Inert oven is used for temperature cycling between 35 and 250°C with a dwell time of 15 minutes at each extreme and a nitrogen ambient atmosphere.

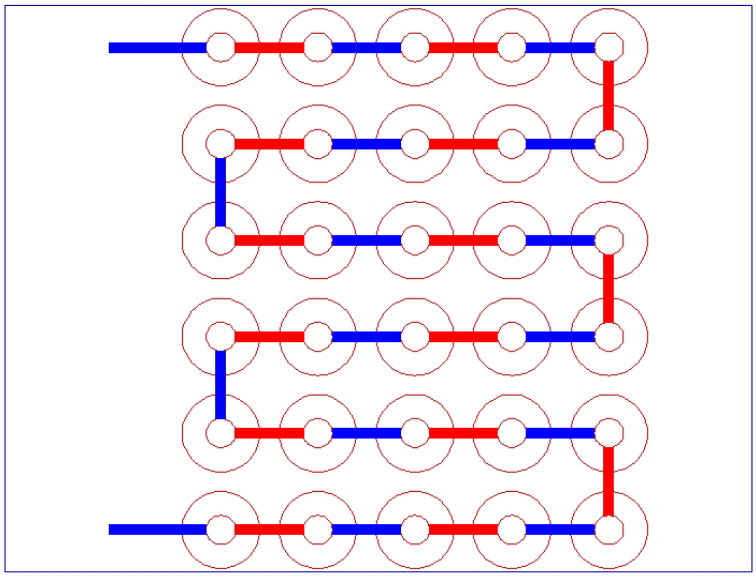


Figure 3.10. A top view representation of the via test structure. The round holes represent individual vias with the red lines showing metal on topside of the polyimide and the blue lines showing metal on the backside of the polyimide.

	Peak	Min	Max Rising	Max Falling	Rising Time 130.0	Time Between 130.0/160	Rising Time 160.0	Time Between 160.0/183	Total Time 183.0	Pointer 44.1	Pointer 78.4	Pointer 205.7	Pointer 225.3
1	251.1	53.0	0.11	-0.07	11134.73	2645.92	8488.81	1782.00	14385.54	53.0	249.0	53.8	261.0
2	18.9	18.1	0.00	-0.00	0.00	0.00	0.00	0.00	0.00	18.2	18.6	18.5	18.7
3			0.00	0.00	0.00	0.00	0.00	0.00	0.00				
4			0.00	0.00	0.00	0.00	0.00	0.00	0.00				
5			0.00	0.00	0.00	0.00	0.00	0.00	0.00				
6			0.00	0.00	0.00	0.00	0.00	0.00	0.00				

Figure 3.11. Temperature cycling profile (35 to 250°C).

The test samples completed 1200 cycles without significant change in resistance resulting in failure. The average resistance for the 30 via nets is plotted in Figure 3.12 by via diameter and Figure 3.13 by copper thickness. The resistance increases with small via and copper thickness geometries, as expected. It should be noted that the data presented is for a resistance of 30 vias in series. An average value of a single via is calculated by dividing the resistances reported by 30.

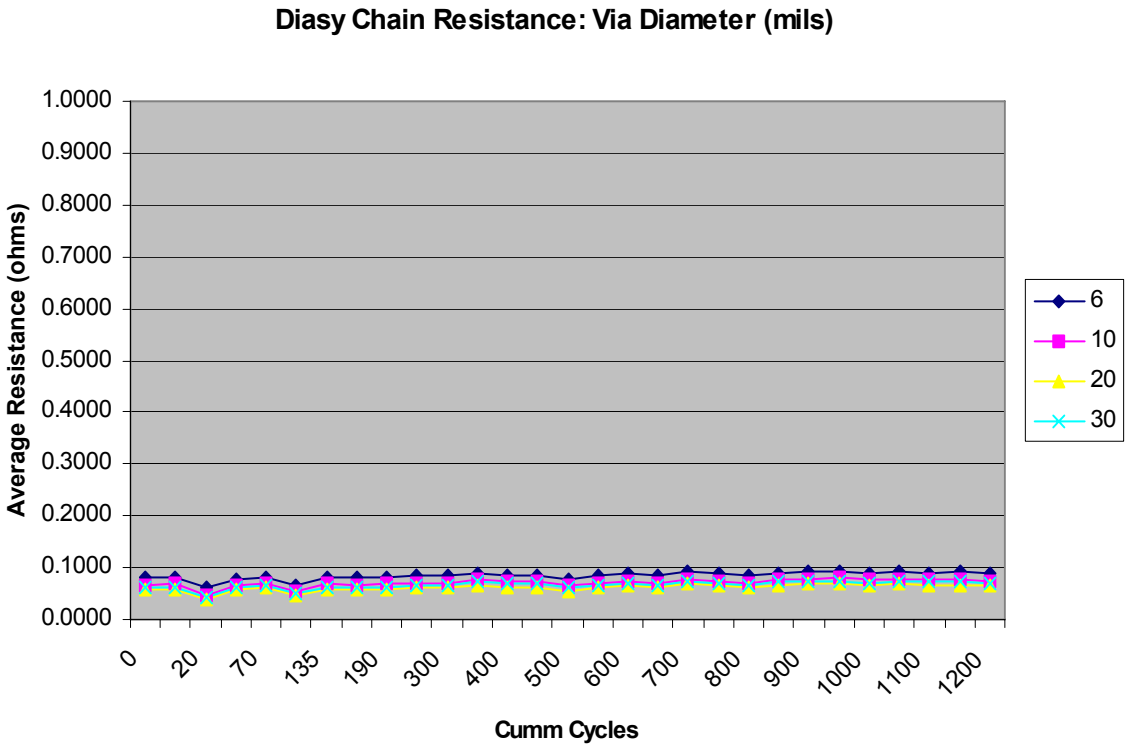


Figure 3.12. Average Daisy Chain Resistance by Via Diameter (shown in mils).

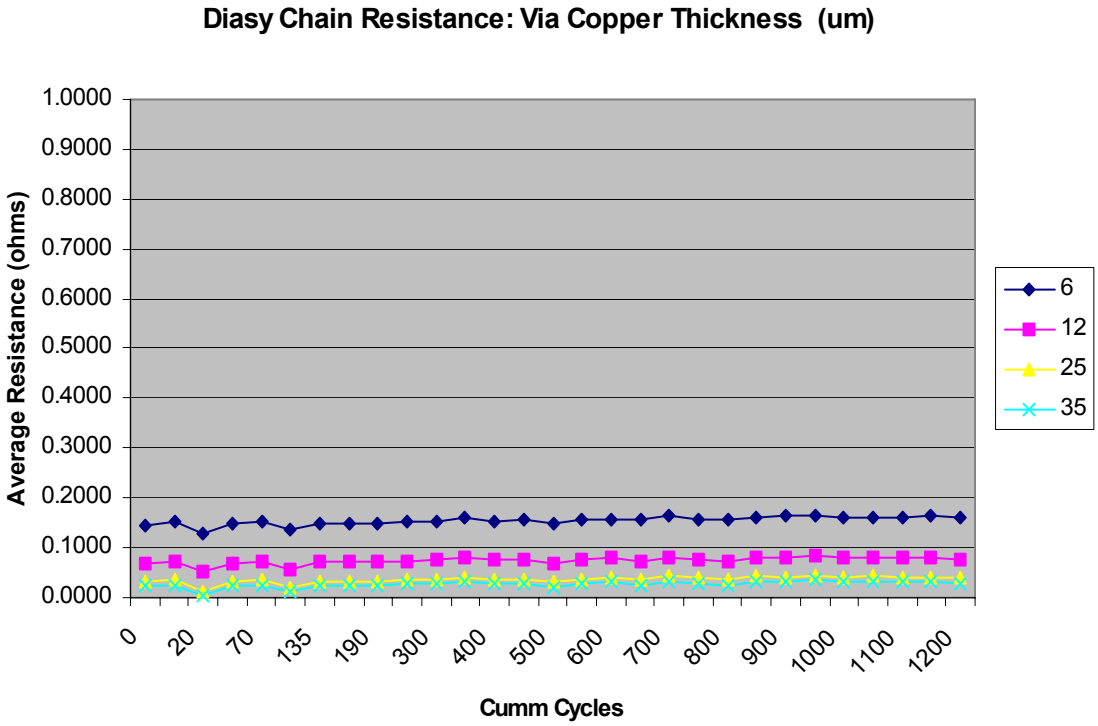


Figure 3.13. Average Daisy Chain Resistance by Copper Thickness (thickness shown in microns).

Although no hard failures were detected in any via, an average increase in resistance was found for the entire population. Figure 3.14 indicates this linear trend in the data. An effects plot of the average change in resistance by design factor, Figure 3.15, shows little effect of diameter and a strong effect on thickness. The thinnest copper thickness shows the most increase in resistance and a smaller change with thicker copper that decreases with thicker copper. A regression analysis of the diameter and thickness confirmed a strong correlation to the thickness and a weak correlation to diameter. This could indicate diffusion into the copper that is more pronounced with a thin copper trace since the diffusion layer would be a larger percentage of the bulk as indicated by a square root of cycle relationship with resistance change. A reliability analysis by percent degradation would indicate a reverse trend since the resistance of thinner copper is higher than for thicker copper. An increase in resistance with a lower resistance via would have a larger percent increase. It is common to define a failure criterion using a percent degradation, which would give misleading results in this case.

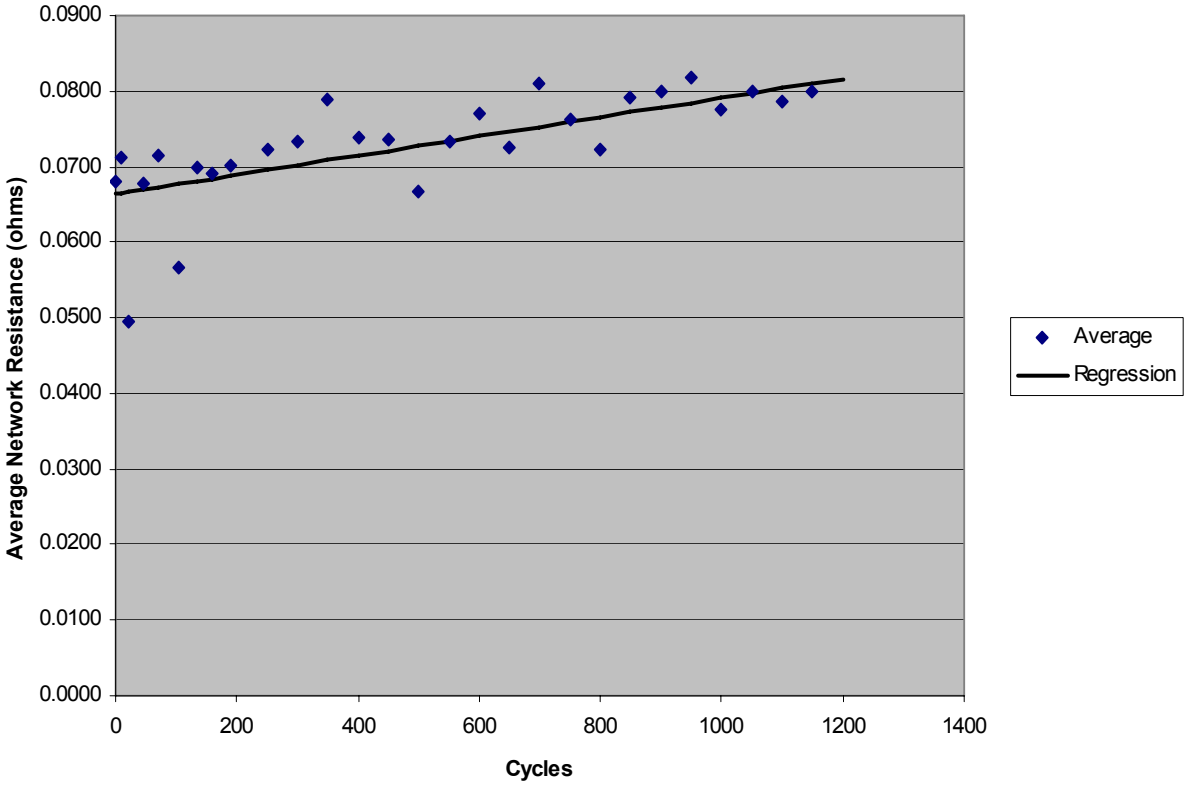


Figure 3.14. Average resistance of all resistive nets.

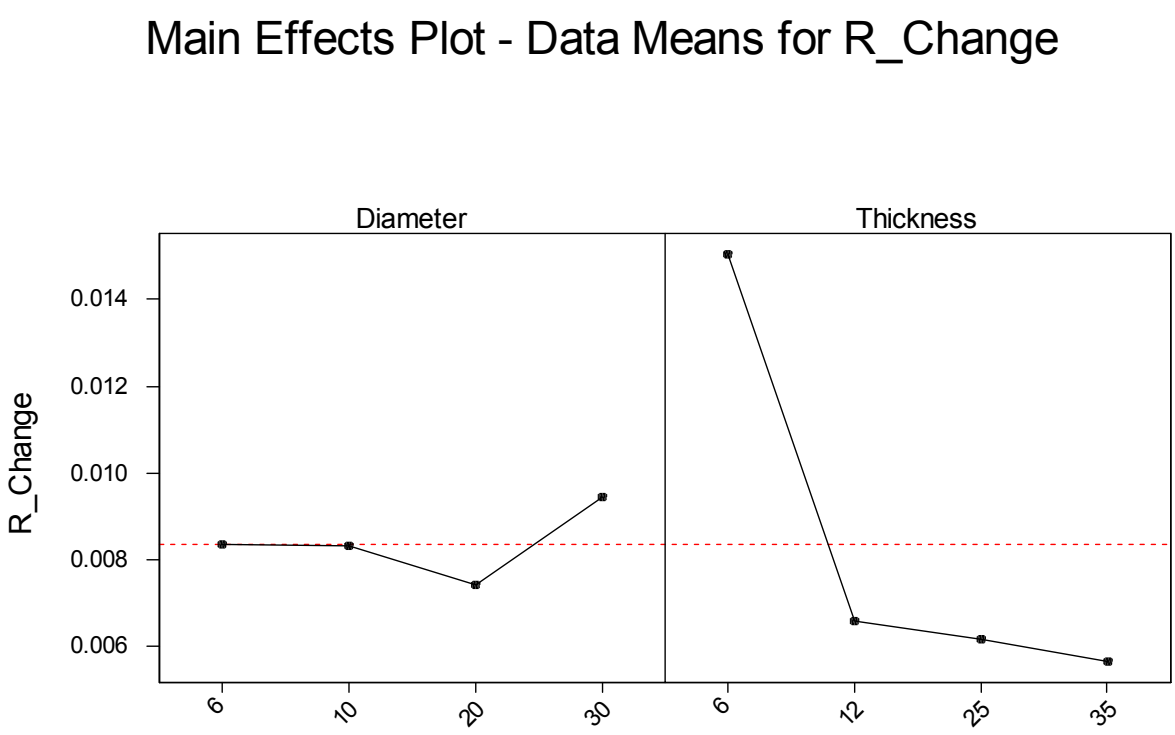


Figure 3.15. Mean of Resistance Change by Via Design Factor: Cu Thickness (microns) and Via Diameter (mils).

A reliability degradation analysis is used to estimate via life using a failure criteria defined as an increase of 1 micro-ohm per via (0.03 ohms per net). This avoids the concern regarding a percent degradation criterion. The degradation analysis performs a life regression fit of the degradation data and calculates the failure time of each net. The data for the 6 micron thick copper was removed from the population since it had a significantly different resistance change than the rest of the population. The degradation analysis was performed using Weibull++ 7. The distribution analysis found that a two-parameter Weibull distribution represented the life data best with a mean of 3823 cycles and beta of 15.1369. A distribution plot is shown in Figure 3.16.

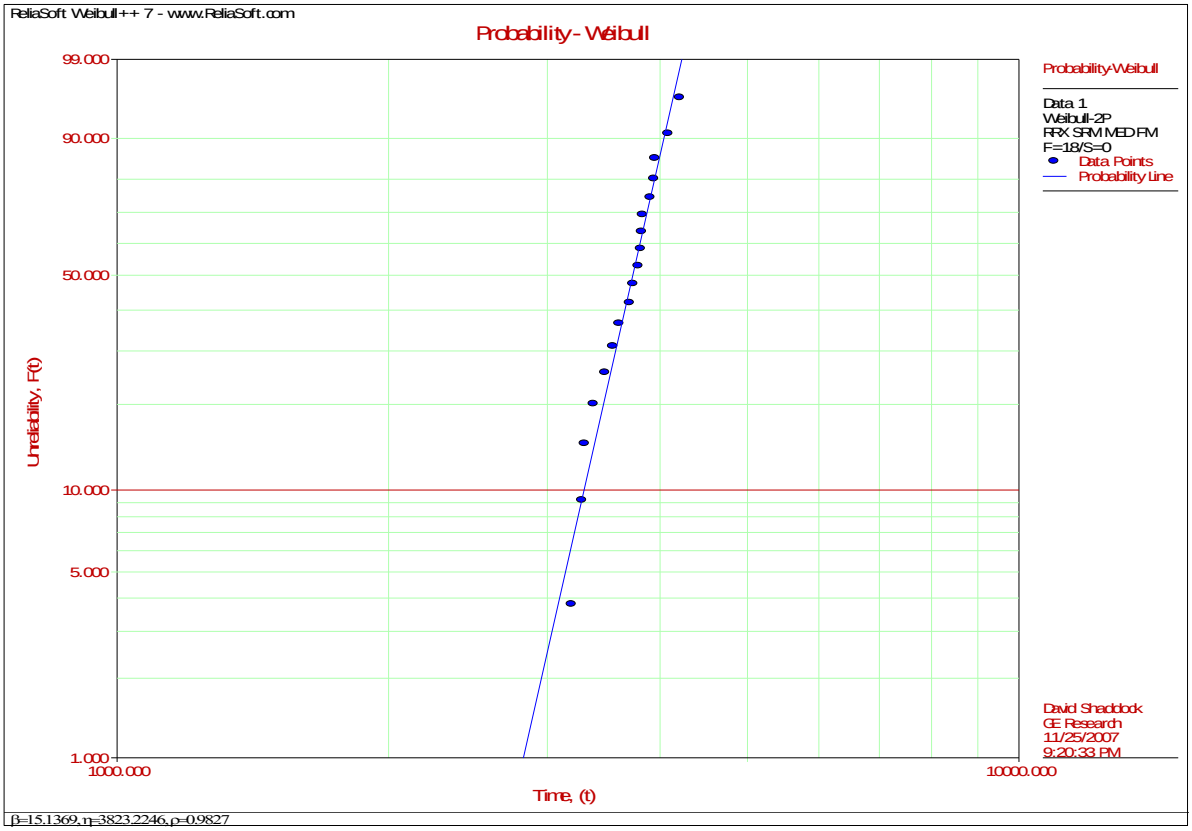


Figure 3.16. Via life degradation model.

Chapter 4. Solder Characterization

4.1 Solder Overview

A solder alloy with a melting point comfortably above that of the peak application temperature must be selected. For this application, an alloy with melting point of at least 250°C would be an appropriate choice. Table 4.1 lists the solder alloys evaluated in this study, ordered according to their liquidus temperature.

Table 4.1. High temperature solder alloys to be tested and their properties.

Solder Alloy	$T_{solidus}$ (°C)	$T_{liquidus}$ (°C)	Strength (MPa)
90Pb-10Sn	268	301	30
95Pb-5In	300	313	29.8
93Pb-3Sn-2In-2Ag	-	304	38.4
92.5Pb-5Sn-2.5Ag	287	296	29
95Sn-5Sb	235	240	40

Reflow soldering, generally used by industry as a batch process for surface mounted components, is the most cost effective and high throughput process. However, this soldering process applies maximum stress on the assembly as the entire assembly is heated to a temperature of at least 25°C above the liquidus temperature of the solder alloy. However, the Kapton E material chosen as part of the analysis in prior sections has a Tg significantly higher than the liquidus temperature of each of these solder alloys.

0805 and 2512 resistors will be used for the purpose of testing: thermal cycle and high temperature storage (HTS). Surface finish of the passive components is also an important variable in the process and will be evaluated in the test. The kinetics of formation and growth of intermetallics will be studied for the combinations of solder and surface finish. For example, Ni_3Sn_4 (Au) has been observed to form after reflow of PbSn5 solder on Ni/Au surface finish [10]. Study of intermetallic composition and adhesion strength of solder to the surface finish will help in solder selection. Since the properties of high temperature solders are relatively unexplored in literature, stress-strain properties of above-mentioned solder materials will be obtained at different temperatures to further help in the solder down selection. These temperature dependent properties were used to evaluate the reliability under thermal cycling using a FEM. These solder alloys would also be tested for creep and fatigue behavior in the temperature range of application.

4.2 Microstructural Characterization

To ensure meaningful results from our low cycle fatigue life models of solder interconnects, accurate material properties are needed. Uniaxial tensile tests and nanoindentation will be used to measure the mechanical properties (elastic modulus, yield stress, etc.) of the solders. Uniaxial tensile tests will be used to measure the constitutive relationship to be entered into the ANSYS finite element simulation software, as well as elastic modulus, yield strength, tensile strength, strain hardening exponent, and total elongation. The temperature dependence of these properties will be measured by insitu tensile testing in a furnace. To determine the strain rate dependence of the mechanical properties, samples will be pulled at several different rates.

Nanoindentation is a convenient tool for this application because it permits testing of microscopic specimens. It is impractical to measure the mechanical properties of reflowed solder paste using a standard tensile test because of the amount of paste needed to make a dog bone sample. Instead, tensile tests will be performed on the same composition solder wire, which can be related to solder paste via nanoindentation and microstructural characterization. Since the wire and paste forms have the same compositions, both will have the same phases present; provided they are both at the same temperature. The primary difference between the two forms is the size of the grains generated from different processing methods. For instance, during processing, solder wire undergoes a cold rolling process which distorts the size of the grains, leading to strain hardening [1]. Grain size is an important material property because it is directly related to the strength of the metal. From the Hall-Petch equation it can be seen that grain size is related to yield strength by:

$$\sigma_y = \sigma_o + Kd^{-\frac{1}{2}} \qquad (1)$$

where σ_y is the yield stress, σ_o and K are material constants, and d is the average grain diameter [1]. It's evident from Hall-Petch equation that strength is inversely proportional to grain size. For the same composition metal, the strength will generally increase with decreasing grain size. However, this increase in strength usually comes at the price of reduced ductility [2].

The microstructure of the wire and paste were examined by embedding the solder in an epoxy resin and polishing the cross section. Both mechanical polishing and chemical etching techniques were used to expose grain boundaries and examine the different phases of the solders. Since four of the solders contain 90%+ Pb, a very soft metal, special polishing techniques were developed to reduce the number of polishing particles embedded in the solder surface. It is important to avoid embedded particles because they act as artifacts and hide important features of the microstructure.

4.2.1 Solder Wire Microstructure

Figure 4.1 is an optical microscope image of the 90Pb-10Sn microstructure from as received solder wire. A light colored oval phase can be seen dispersed throughout the matrix of the solder. The Pb-Sn phase diagram reveals this phase to be tin (Sn) rich β phase. Tin has limited solubility in lead. At room temperature, 2% tin dissolves into lead to form the α phase, the matrix of the solder, the rest of the tin precipitates out to form the Sn-rich β phase. A high resolution Atomic Force Microscopy (AFM) image of the 90Pb-10Sn microstructure can be seen in Figure 4.2. It's important to note that the microstructure of 90Pb-10Sn will change as the solder is cycled from 298K to 523K. Above 423K, 10% Sn is fully soluble in Pb and only the α phase is present.

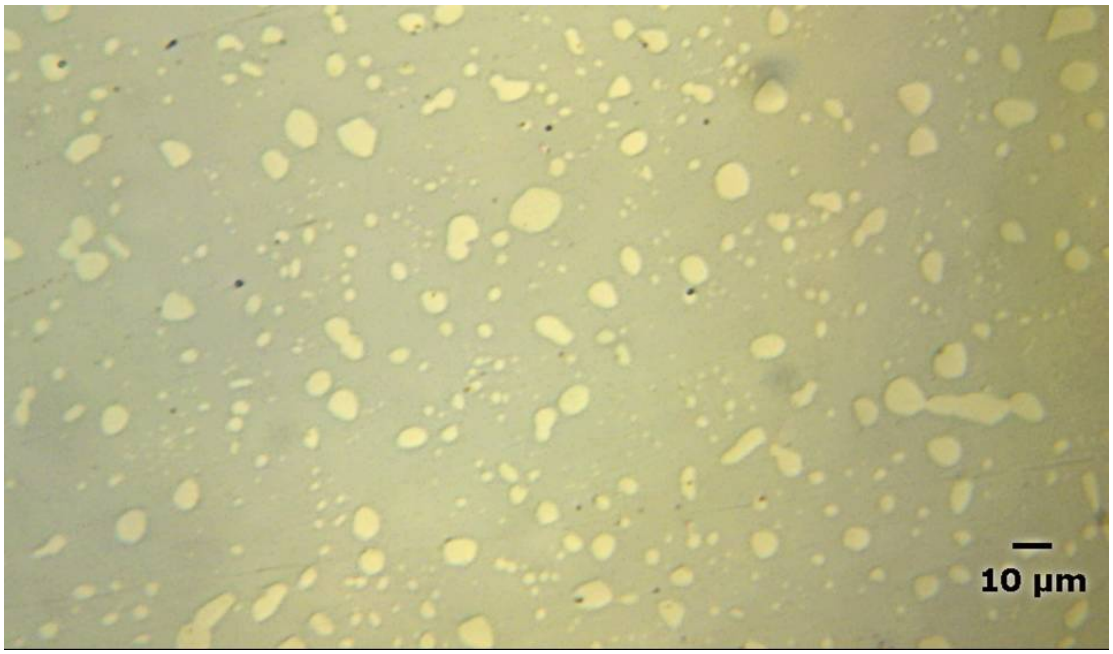


Figure 4.1. Optical image of the 90Pb-10Sn wire microstructure at 1000X. The light colored regions are the Sn-rich β phase.

A chemical etchant was used to reveal the grain boundaries of 90Pb-10Sn. The solution consisted of a 1:1 ratio of hydrogen peroxide 30% and glacial acetic acid [3]. 90Pb-10Sn was immersed in the solution for less than one second and immediately rinsed to halt the etching process. An image of the etched 90Pb-10Sn surface is shown in Figure 4.3. Initial grain size estimation places the grain diameter between 5-7 microns.

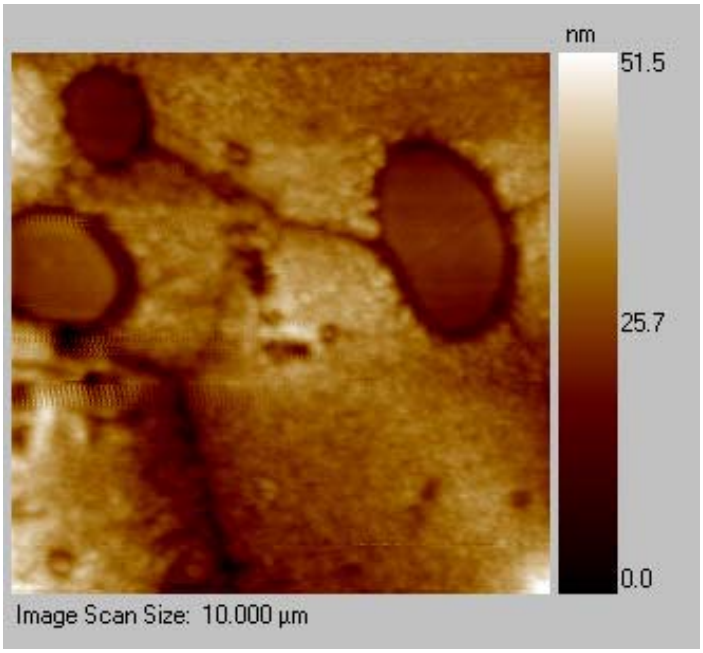


Figure 4.2. 10 µm AFM scan of Pb-10Sn wire surface. The Sn-rich β phase is shown as a depression relative to the matrix of the solder.

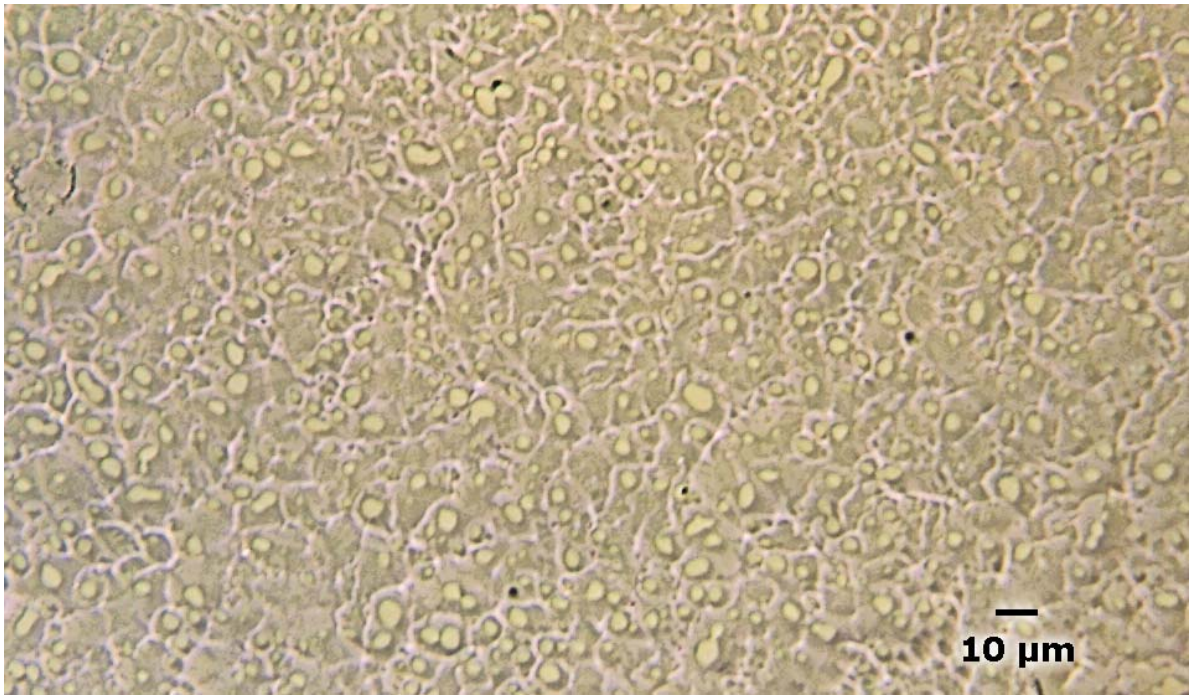


Figure 4.3. Optical image of 90Pb-10Sn wire microstructure at 400X. The light colored blotches are the Sn-rich β phase. Most grains measured between 5-7 microns.

A similar preparation technique was used to reveal the microstructure of 95Pb-5In. The sample was first mechanically polished with 0.02 micron colloidal silica, and then chemically etched with an acetic acid/hydrogen mixture for 10 seconds. From Figure 4.4, it can be seen the grains are considerably larger than in the 90Pb-10Sn structure. While the grains on the outer rim measure approximately 20 microns, the grains toward the center of the wire are considerably larger measuring anywhere from 20-60 microns in diameter. According to the Pb-In binary phase diagram only one phase in present at the 95Pb-5In composition. This is confirmed in the optical images where one phase is visible. Unlike the 90Pb-10Sn solder, there is no phase change during heat treatment of 95Pb-5In.

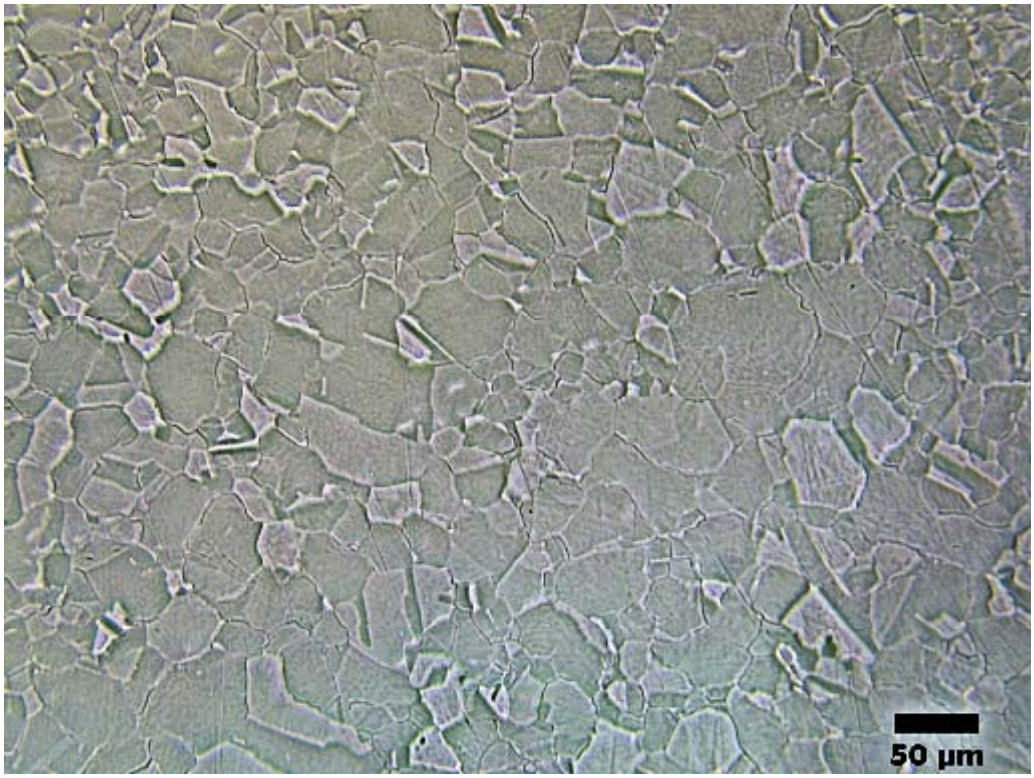


Figure 4.4. Optical image of center of 95Pb-5In wire microstructure at 200X with clearly defined grain boundaries.

95Sn-5Sb was the hardest of all the solders and therefore, the easiest to polish. A standard polishing technique was employed incrementing from 600 grit SiC, to 800 SiC, to 1200 SiC and so on. Unlike the two previous solders, no separate chemical etching step was necessary. Only a ten-minute hand polish with acidic (PH 9) 0.02 micron silica slurry was needed to expose the grain boundaries. Figure 4.5 shows an optical image of the 95Sn-5Sb microstructure. Although there is a large range in the grain sizes, most grains measured between 5-10 microns. Also noticeable in this image are the white precipitates dispersed throughout the microstructure. From the peritectic binary Sn-Sb phase diagram, antimony has limited solubility in tin. Therefore like 90Pb-10Sn, two phases exist at room temperature, the Sn-Sb matrix α, and antimony rich phase β. The β phase strengthens the alloy and dissolves into the matrix of the solder with increasing temperature [3].

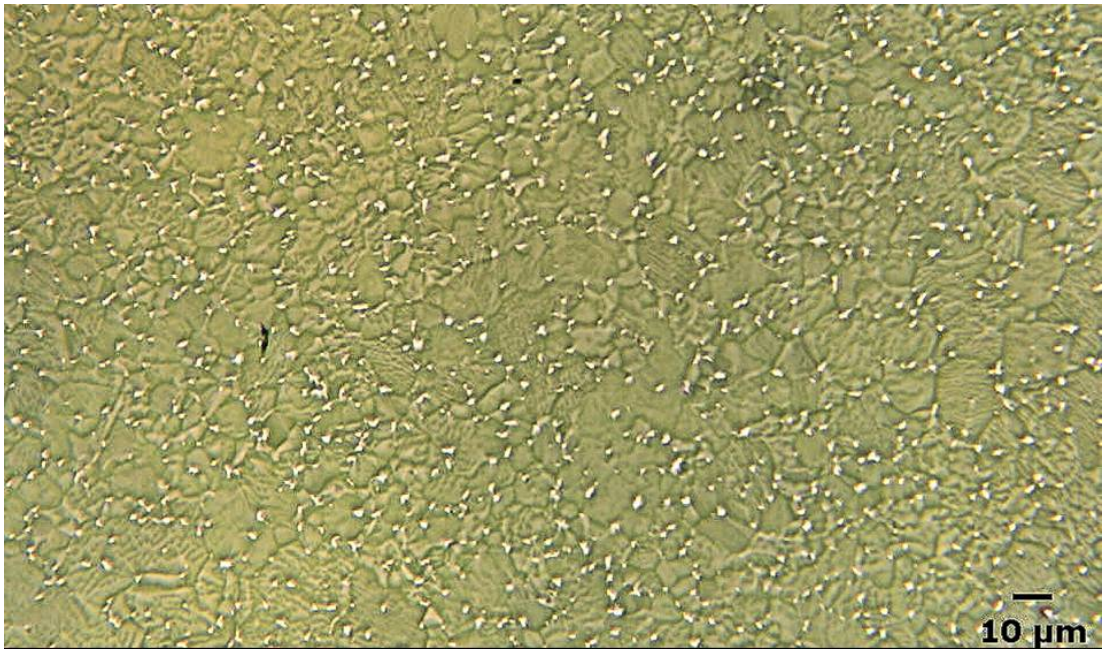


Figure 4.5. Optical image of 95Sn-5Sb wire microstructure at 400X. The white colored precipitates are the Sb-rich β phase.

Optical images of 93Pb-3Sn-2Ag-2In and 92.5Pb-5Sn-2.5Ag are shown in Figures 4.6 and 4.7 respectively. Like the other lead solders, special care was taken not to embed polishing particles in the surface. However, unlike 90Pb-10Sn, and 95Pb-5In, no separate chemical etching process was used. Figure 4.6 clearly shows the grain boundaries of 93Pb-3Sn-2Ag-2In with an average grain diameter of 4 microns. Also visible from the image are white precipitates indicating the presence of at least two phases. A quaternary phase diagram for this alloy does not exist, however it is suspected this phase is Ag_3Sn.

The microstructure of 92.5Pb-5Sn-2.5Ag as seen in Figure 4.7 is very similar to that of 93Pb-3Sn-2Ag-2In. The average grain size was measured to be between 3 and 4 micron. 92.5Pb-5Sn-2.5Ag shows a much more prominent second phase scattered throughout the microstructure. From the ternary phase diagram shown in Figure 4.8 the second phase appears to be Ag_3Sn, a very hard, high modulus intermetallic compound which provides dispersion strengthening to the matrix of the solder.

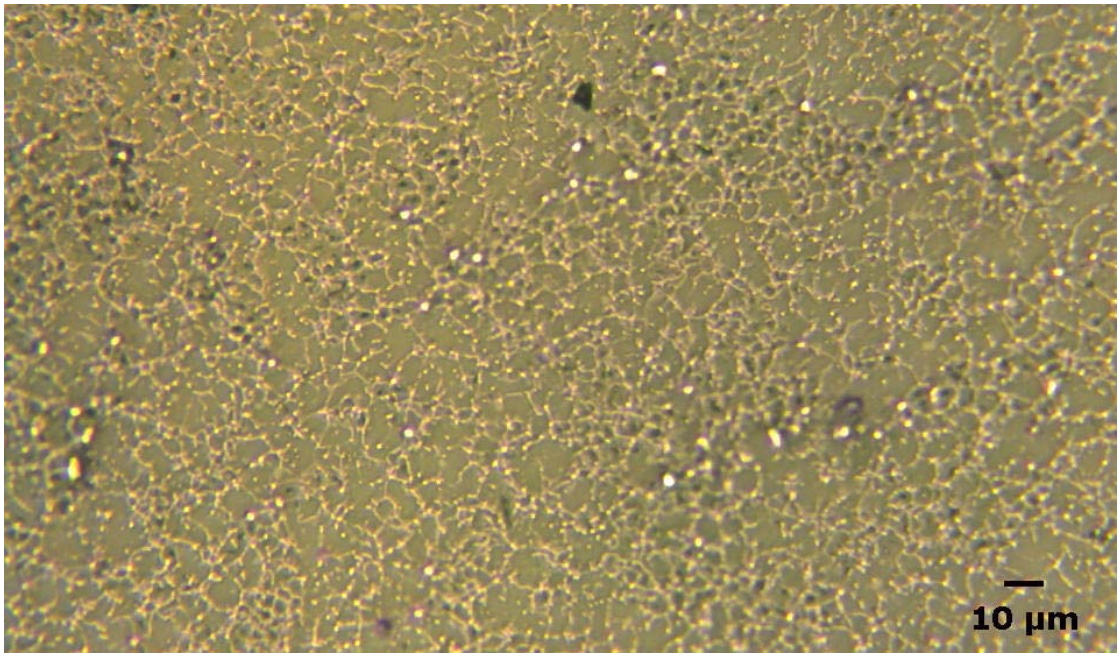
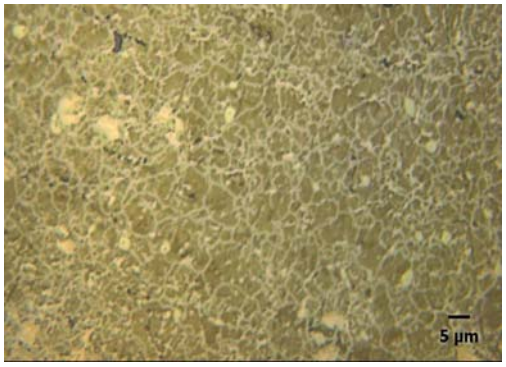


Figure 4.6. Optical image of 93Pb-3Sn-2Ag-2In wire microstructure at 400X. A second precipitate appears as light colored particles.



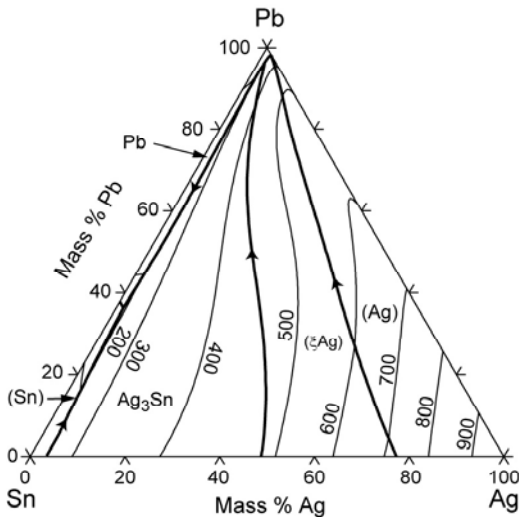


Figure 4.7. Left, optical image of 92.5Pb-5Sn-2.5Ag wire microstructure at 1000X. The light colored phase is Ag_3Sn. Right, ternary phase diagram of Pb-Sn-Ag [4].

4.2.2 Solder Paste Microstructure

Microstructural characterization of the reflowed high temperature solders was completed to contrast with that of the solder wire discussed in the prior section. Environmental Scanning Electron Microscopy (SEM), Energy Dispersive Spectroscopy (EDS), and optical microscopy were used identify the morphology and elemental composition of each phase of the solder. Each of the reflowed solder pastes were potted in an epoxy resin and polished with a 0.02 micron silica slurry to reveal the microstructure. The pad metallurgy consisted of 4.3µm of copper, 1.3µm of nickel and

0.15μm of gold. Figure 4.8 shows an optical image of Pb92.5-Sn5-Ag2.5 reflowed solder paste.

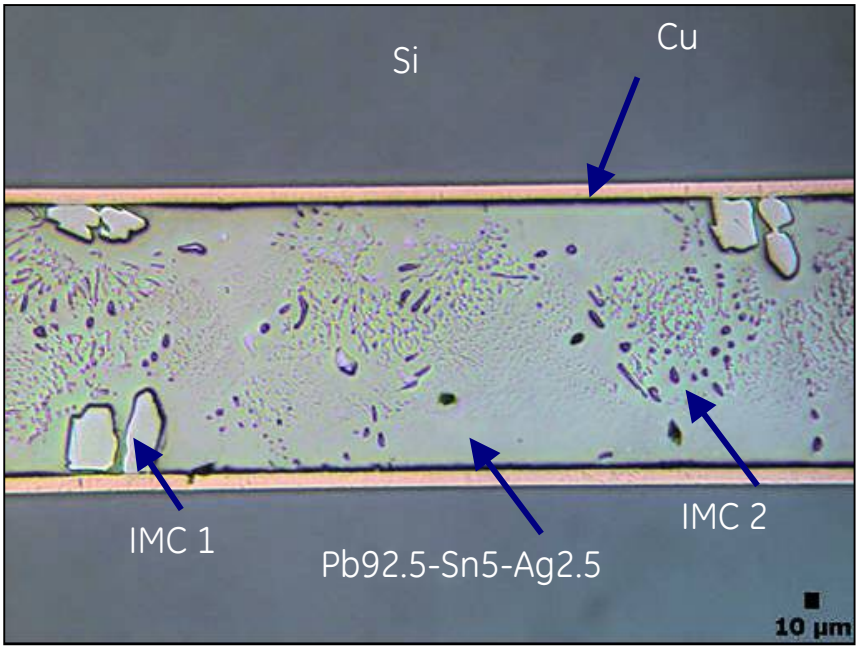


Figure 4.8. Optical image of reflowed 92.5Pb-5Sn-2.5Ag paste.

Two distinct intermetallic compounds (IMC) are visible in the matrix of this solder. The large plate-like IMC labeled IMC 1 is Ag_3Sn possibly with Cu or Au impurities. The EDS spectrum for IMC 1 is shown in Figure 4.9. Ag and Sn show the largest intensities and their ratio indicates the presence of Ag_3Sn. The relatively large presence of copper in this spectrum may explain the unusual shape and size of this compound. The EDS spectrum of IMC 2 is also shown in Figure 4.9. It shows a similar ratio of Ag to Sn, again indicating the presence of Ag_3Sn.

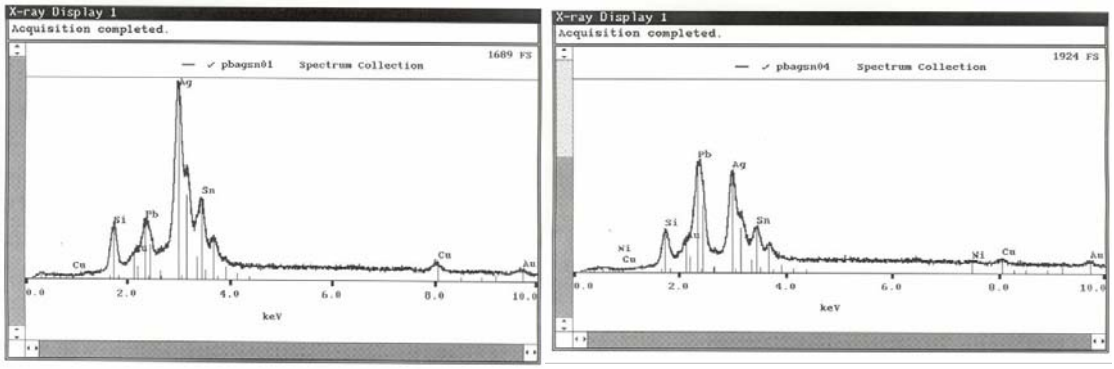


Figure 4.9. Left, EDS spectrum of IMC 1. Right, EDS spectrum of IMC 2. Both spectrums indicate the presence of Ag_3Sn.

Figure 4.10 shows an optical image of the Pb90-Sn10 microstructure. Three phases are visible in the image, the matrix of the solder, β-Sn, and an intermetallic compound. The EDS spectrum of the intermetallic compound is shown in Figure 4.11. The ratio of Au to Sn in the spectrum suggests the IMC is $AuSn_4$.

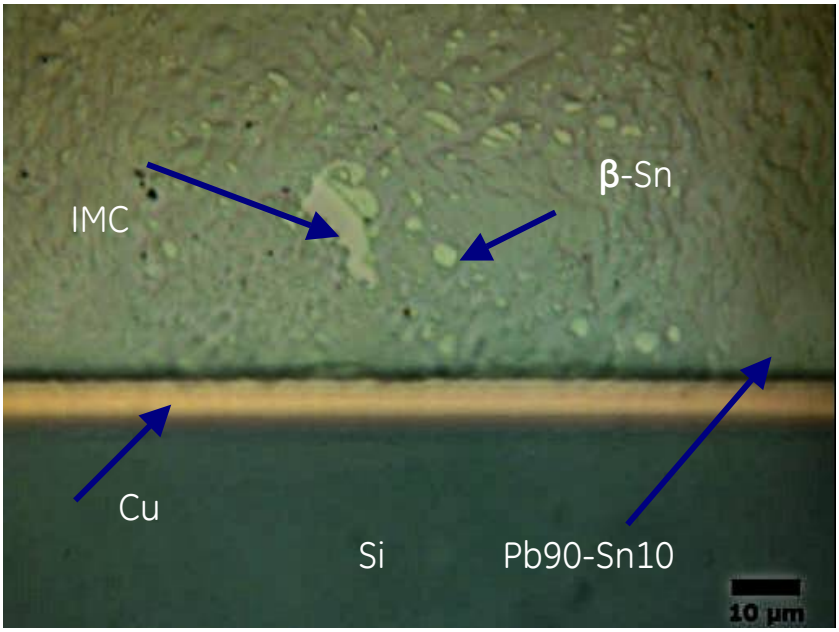


Figure 4.10. Optical image of reflowed Pb90-Sn10 solder paste.

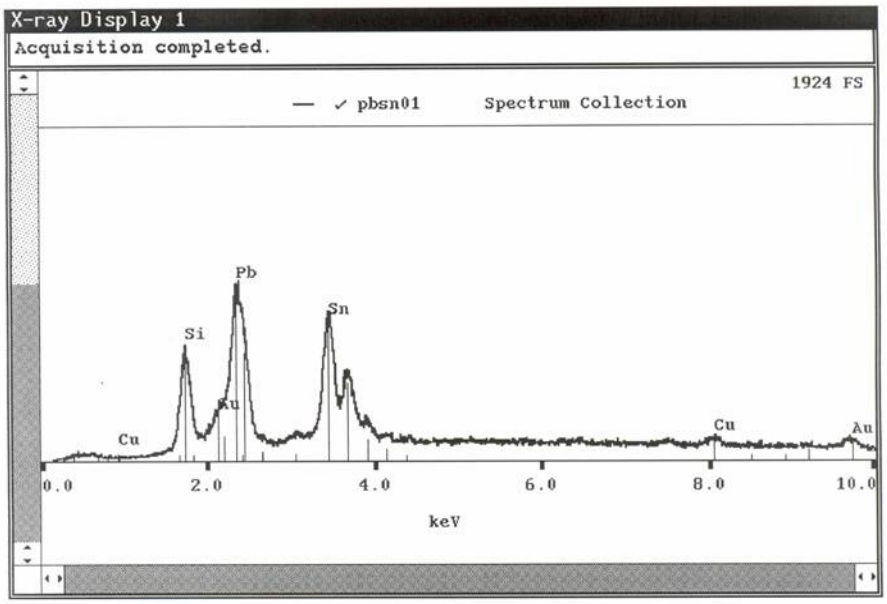


Figure 4.11. EDS spectrum of AuSn4 in the Pb90-Sn10 solder matrix.

The cross-sectional optical image of reflowed Sn95-Sb5 is shown in Figure 4.12. Two distinct intermetallic compounds are seen in this image, one scattered throughout the matrix of the solder, and the other at the pad/solder interface. EDS analysis of each location reveals the interface intermetallic to be Ni_3Sn_4 and the matrix intermetallic to be $AuSn_4$.

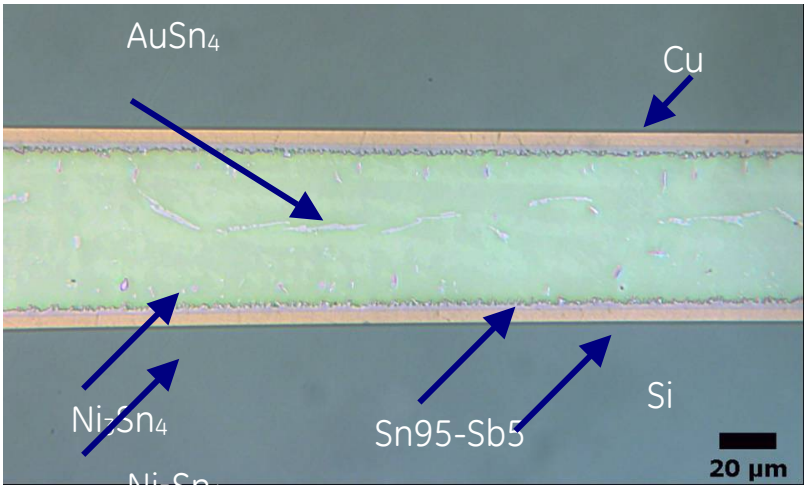


Figure 4.12. Optical image of reflowed Sn95-Sb5 solder paste.

The cross-sectional optical image of reflowed Pb95-In5 is shown in Figure 4.13. Two distinct intermetallic compounds are seen in this image, one scattered throughout the matrix of the solder, and the other at the pad/solder interface. These intermetallics are most likely the result of a reaction between Au and In, Au and Pb, or Ni and In. It was also observed the grains in the paste form are much smaller than the grains in wire form.

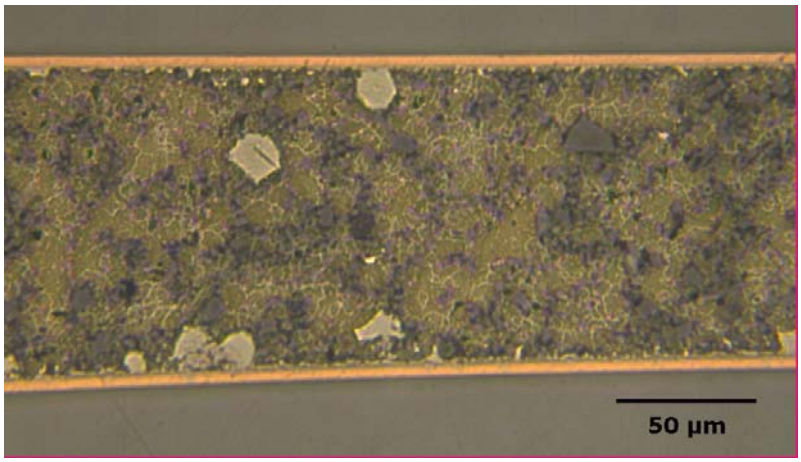


Figure 4.13. Optical image of reflowed Pb95-In5 solder paste.

Microstructural characterization of the solder pastes complements characterization of the solder wire completed discussed in the previous section. However, the microstructure of the reflowed solder pastes on Cu/Ni/Au pads is a better representation of the actual solder joint. During reflow, diffusion of the pad metals into the solder forms intermetallics not seen in the wire form. Location, composition, and morphology of these IMCs contribute greatly to the mechanical strength and reliability of the solder joint.

In addition to the microstructural characterization of solders reflowed Cu/Ni/Au pads, the microstucture of two of the most promising solders, Pb93-Sn3-Ag2-In2 and Pb92.5-Sn5-Ag2.5 was investigated on Cu/Ni/Pd/Au pads. Both solders were cross-sectioned after reflow and after aging for 500 hours at 250˚C to track microstructural changes with aging. Figure 4.14 shows the cross-section of Pb92.5-Sn5-Ag2.5 reflowed on a Cu/Ni/Pd/Au pad.

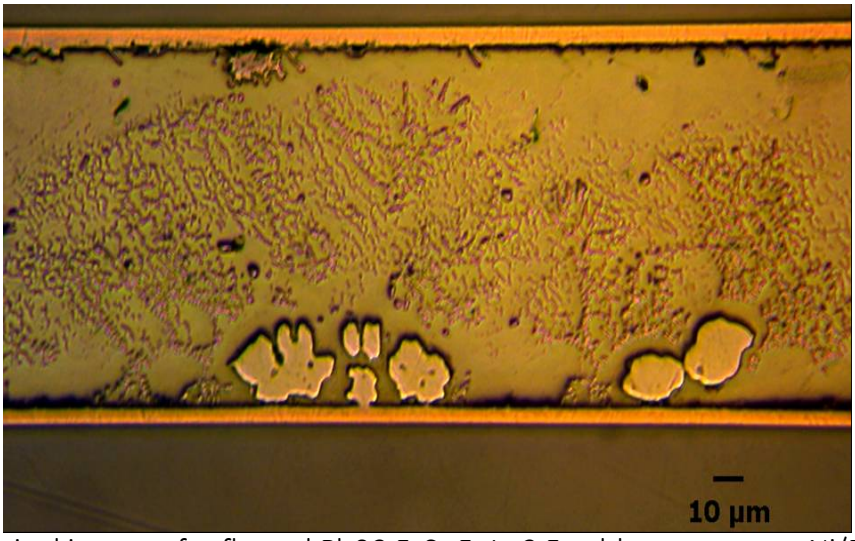


Figure 4.14. Optical image of reflowed Pb92.5-Sn5-Ag2.5 solder paste on a Ni/Pd/Au pad.

Many intermetallic compounds and second phase precipitates are visible in the solder matrix. The large plate-like phase toward the bottom interface is Ag_3Sn with Au impurity. Also a interfacial intermetallic compound is visible on the top interface. This compound was identified as Ni_3Sn_4. Under 1000X (Figure 4.15) the morphology of the small network of precipitates can be seen more clearly. These precipitates were previously identified as Ag_3Sn and Sn precipitates.

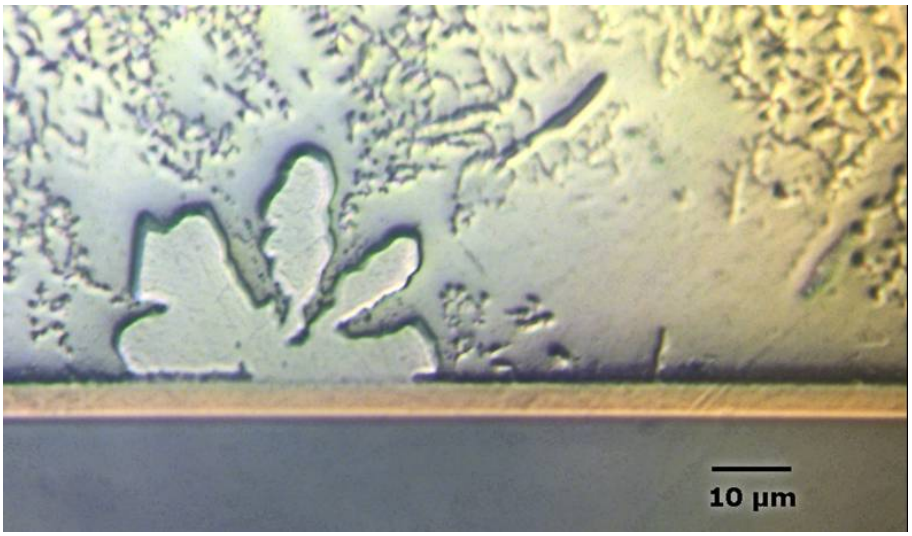


Figure 4.15. Optical image of reflowed Pb92.5-Sn5-Ag2.5 solder paste 1000X.

After aging for 500hrs at 250ºC little change was found in the microstructural features. Figure 4.16 is an optical image of Pb92.5-Sn5-Ag2.5 after aging. Just as in the sample with no aging, Ag_3Sn with Au plates, Ag_3Sn needles, and Sn precipitates can be seen in the matrix. However under higher magnification (Figure 4.17), a thicker interfacial intermetallic layer Ni_3Sn_4 is visible.

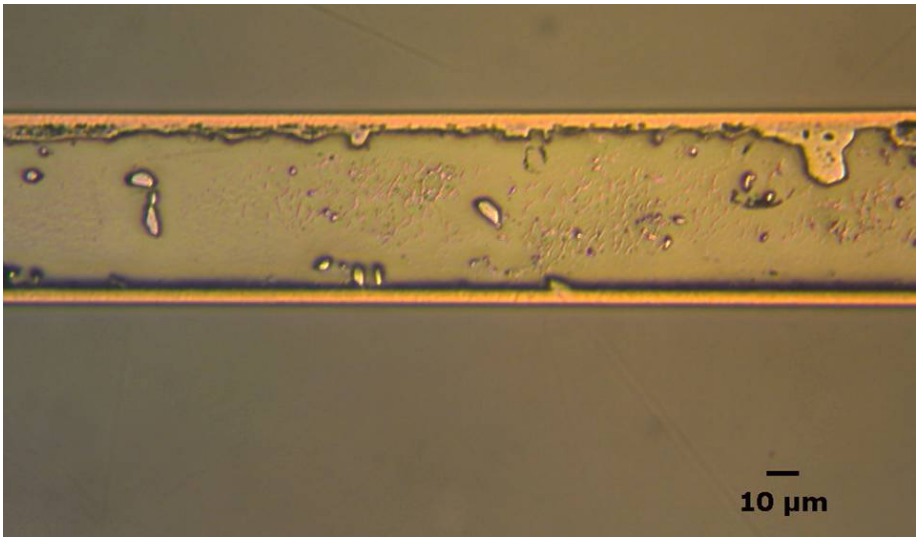


Figure 4.16. Optical image of reflowed Pb92.5-Sn5-Ag2.5 solder paste on a Ni/Pd/Au pad aged for 500hrs at 250ºC.

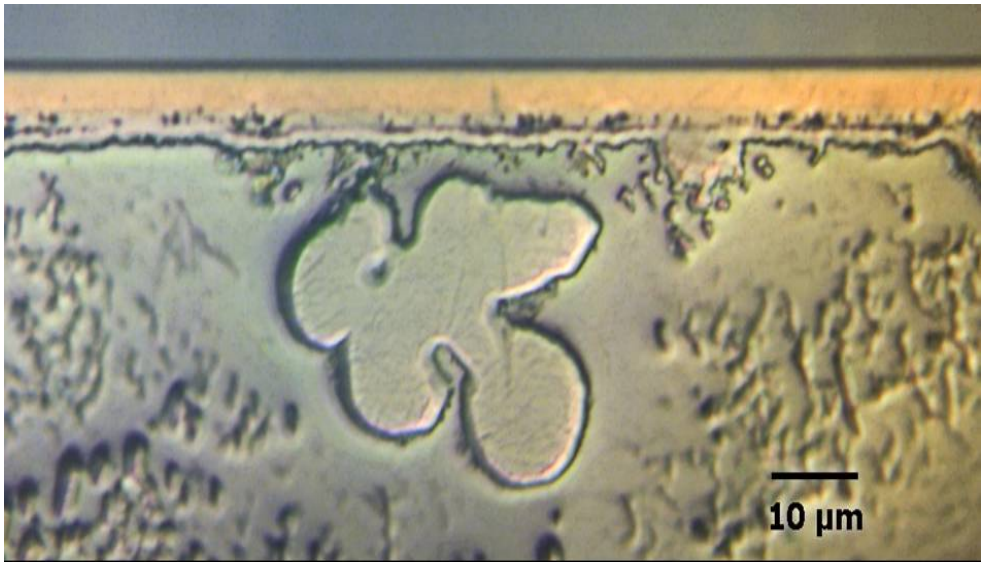


Figure 4.17. Optical image of reflowed Pb92.5-Sn5-Ag2.5 solder paste aged for 500 hrs at 250ºC at 1000X.

Pb93-Sn3-Ag2-In2 on Cu/Ni/Pd/Au was also cross-section after reflow and reflow/aging for 500 hrs at 250ºC. Figure 4.18 shows an optical image of the cross-sectioned solder after reflow. Little difference can be found between Pb93-Sn3-Ag2-In2 and Pb92.5-Sn5-Ag2.5. It seems the In in Pb93-Sn3-Ag2-In2 either remains in solid solution or is absorbed by the intermetallic compounds.

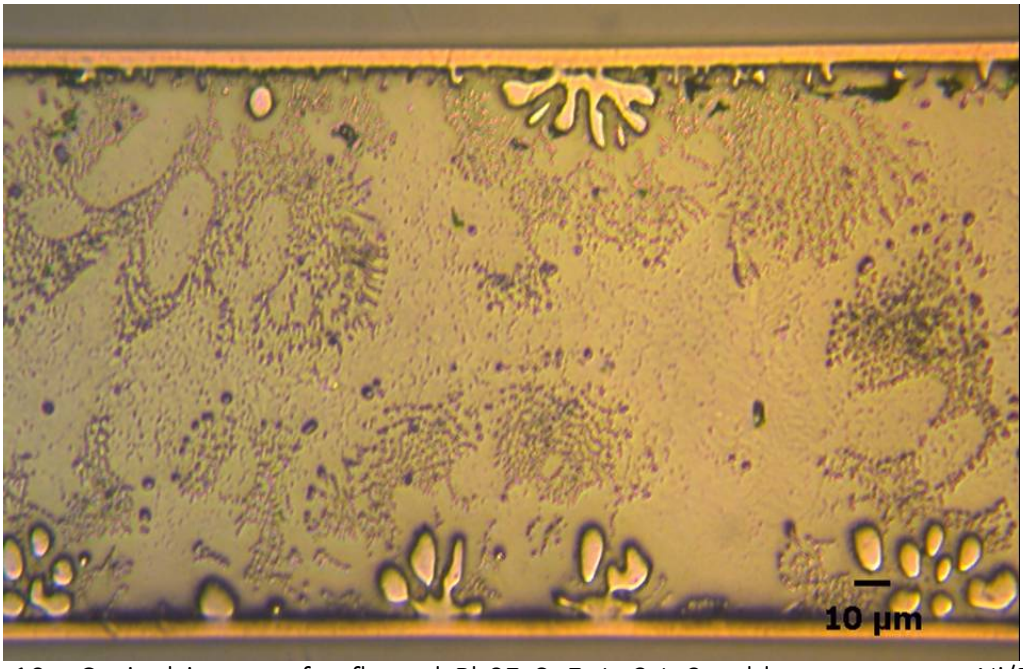


Figure 4.18. Optical image of reflowed Pb93-Sn3-Ag2-In2 solder paste on a Ni/Pd/Au pad.

The microstructure of Pb93-Sn3-Ag2-In2 after aging for 500 hrs at 250ºC again shows little difference from the reflowed only case. Figure 4.19 shows an optical image of the cross-sectioned solder after reflow and aging. One notable difference however is the development of voids between the pad and the interfacial intermetallic structure. Under stress these voids may grow and lead to possible sites for delamination and failure.

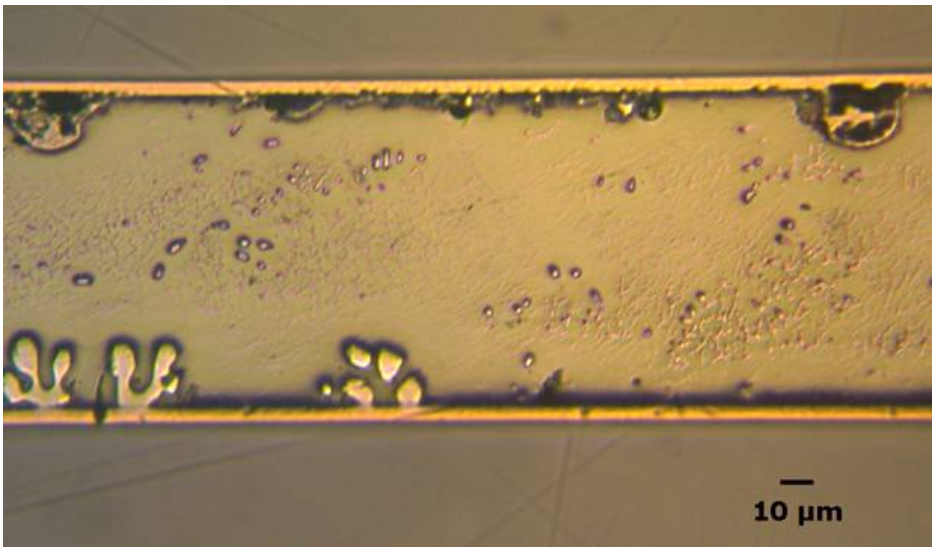


Figure 4.19. Optical image of reflowed Pb93-Sn3-Ag2-In2 solder paste aged for 500 hrs at 250C.

To track diffusion of the constituents, x-ray mapping was performed on Pb93-Sn3-Ag2-In2 after reflow and aging for 500 hrs at 250ºC. X-ray mapping shows the location and relative concentration of elements in the microstructure. Mapping results are shown in Figure 4.20.

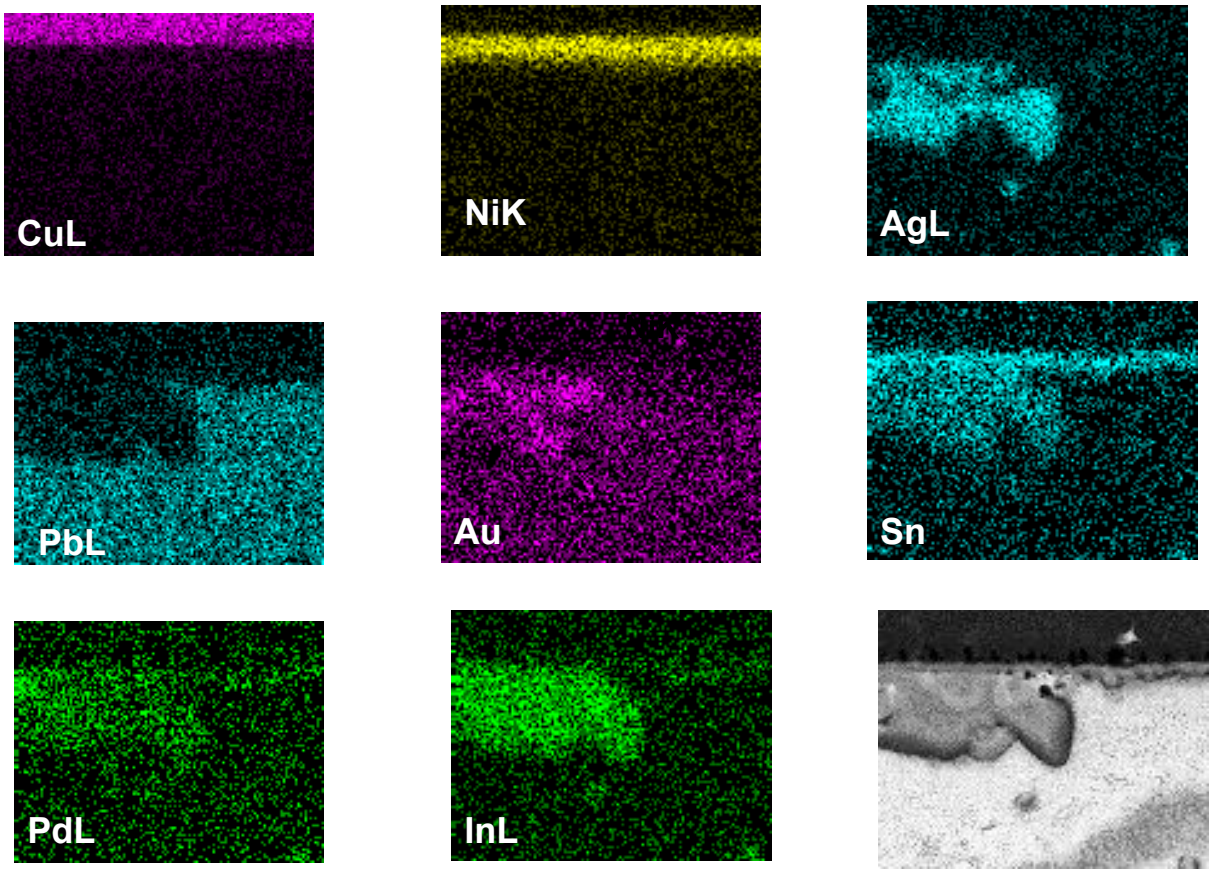


Figure 4.20. X-ray mapping of reflowed Pb93-Sn3-Ag2-In2 solder paste aged for 500 hrs at 250°C.

Several conclusions can be drawn from the mapping results. First the matrix of the solder seems to be primarily Pb, as was expected. The solder constituents and pad metals form intermetallic compounds and second phase precipitates rather than enter into solid solution with Pb. Secondly, the overlapping concentrations of Ni and Sn indicate the presence of a Ni_3Sn_4 interfacial intermetallic layer. The other plate-like intermetallic growing off the interface is Ag_3Sn. Mapping results indicate Ag_3Sn absorbs In, Pd, and some Au. It is also evident that Ni is an adequate diffuse barrier for the Cu pad. Ni prevents the nucleation and growth of detrimental Cu-Sn intermetallics.

4.3 Nanoindentation Overview

Nanoindentation like other hardness tests involves the penetration of the sample with an indenter. However, in nanoindentation, a new depth sensing parameter, contact depth (h_c), is introduced. Contact depth, the depth in which the sample is in contact with the indenter, is measured by extending the slope of the upper portion of the unloading curve to the x-intercept as in Figure 4.21:

$$h_c = h_{\max} - \varepsilon \frac{P_{\max}}{S} \qquad (2)$$

where ε is the geometric constant, P_{max} is the maximum load, S is the contact stiffness, and h_{max} is the maximum load [5].

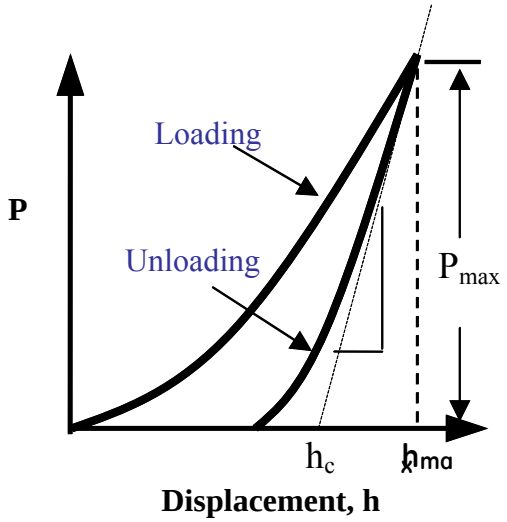


Figure 4.21. Load (P) vs. displacement (h) plot for a typical nanoindentation loading and unloading cycle.

The area function then uses the contact depth to estimate the projected contact area. Contact area can be used to determine the hardness, *H* and reduced modulus, E_r of a sample from the following equations:

$$H = \frac{P_{max}}{A} \tag{3}$$

where P is load and A is the projected contact area, and:

$$E_r = \frac{\sqrt{\pi}}{2\beta}\frac{S}{\sqrt{A}} \tag{4}$$

where S is contact stiffness and β is an indenter constant [5]. To obtain Young's modulus from the reduced modulus, the following equation can be used:

$$\frac{1}{E_r} = \frac{1-\upsilon^2}{E} + \frac{1-\upsilon_i^2}{E_i} \tag{5}$$

where *i* is the subscript for diamond indenter, and ν is Poisson's ratio [5]. In this model, it is assumed that both the film and substrate are flat surfaces. However, on a rough surface the contact depth h_c can be over or underestimated depending where the

indenter is positioned on the surface. This highlights the importance of surface preparation as was discussed in the previous section.

Quasi-static nanoindentation has certain limitations in the characterization of materials that exhibit time dependent plasticity [6]. For such applications, a continuous stiffness indentation method was developed to remove the effect of creep on the measured contact stiffness [6]. Dynamic nanoindentation superimposes a sinusoidal load on top of a quasi-static load to obtain contact stiffness measurements continuously as a function of displacement. Figure 4.22 shows the typical loading curve for a dynamic nanoindentation test. From the contact stiffness, elastic modulus and hardness can be calculated as a function of depth.

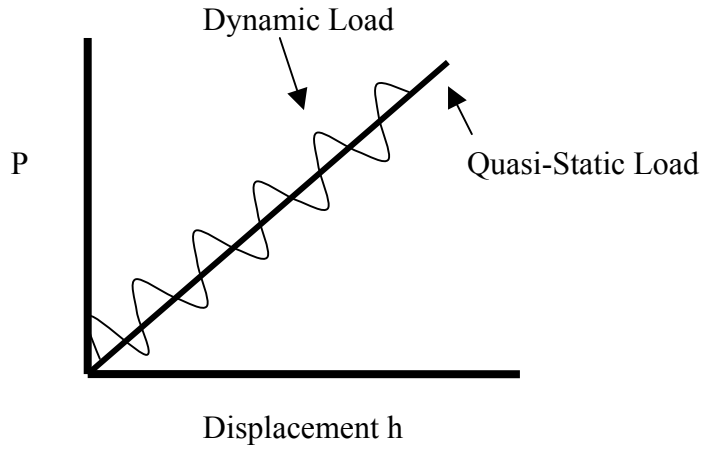


Figure 4.22. Load (P) vs. displacement (h) plot for a dynamic nanoindentation test. The dynamic load is superimposed on the quasi-static load to measure the contact stiffness as a function of depth.

Elastic modulus and hardness are two important material properties which give insight into the fatigue life of solders. The elastic modulus is a direct measurement of the stiffness of a material. When thermally cycled, stiffer (higher modulus) solders will generate larger mechanical stresses, which results in larger strains. Over the lifetime of a solder joint, this may lead to premature failure depending on the elastic limit and total elongation of the solder. It should also be noted, however, that stiffer solders generally have a greater resistance to time dependent plasticity. Given this is a high temperature application, and plasticity due to creep is significant above $0.5T_m$, high temperature creep experiments are needed to more fully characterize the solders. Hardness can be related to joint strength since it is proportional to the ultimate tensile strength of a material [7]. Ideally, the solder should have a low elastic modulus, and high hardness (high yield/tensile strength) for a longer fatigue life.

4.3.1 Nanoindentation Results

Figure 4.23 shows a continuous stiffness measurement of elastic modulus versus displacement for 95Sn-5Sb. An AFM scan was performed on the surface prior to indentation to ensure measurement on the matrix of the solder, not the precipitate

phase. Several testing parameters must be optimized to ensure meaningful accurate dynamic indentation results. These include quasi-static load, dynamic load, frequency, and loading rate.

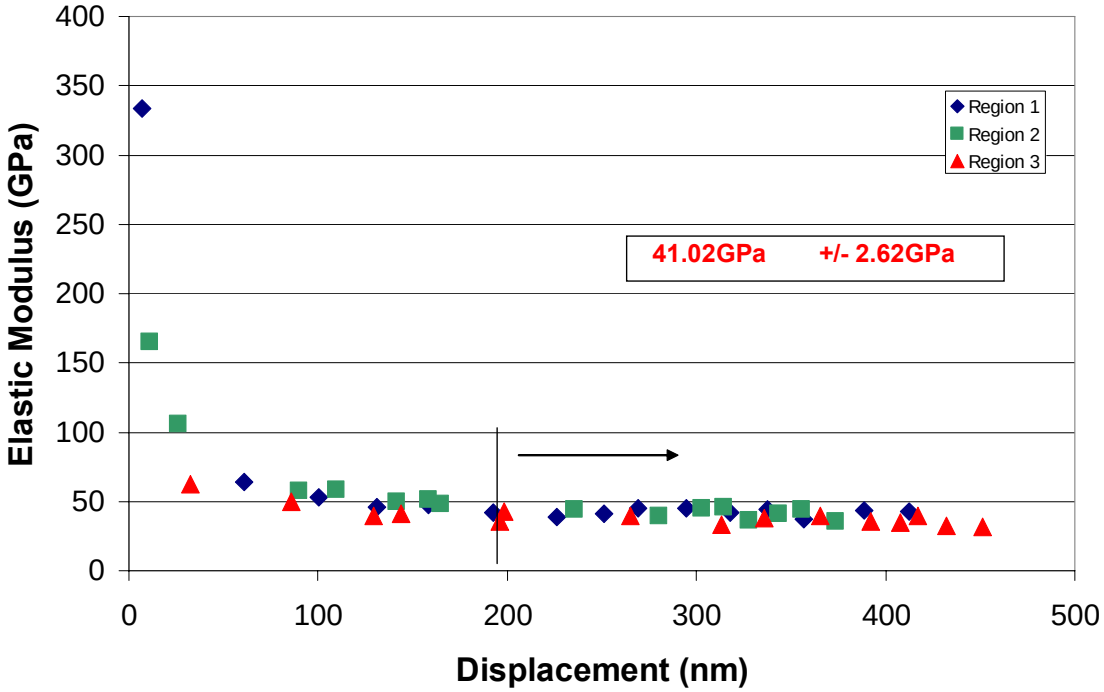


Figure 4.23. Plot of results from a dynamic nanoindentation test. Elastic modulus plotted as a function of depth for 95Sn-5Sb.

The first 200 nm of this measurement is removed because of shallow depth surface effects which overestimate contact stiffness values. Averaged from 200 nm to 450 nm, the elastic modulus was measured to be 41.02 GPa which is in good agreement with the NIST uniaxial tensile test measurement of 44.5 GPa [8]. Care was taken during the indentation test to avoid the Sb-rich phase and only indent on the matrix of the solder. Figure 4.24 shows a plot of hardness verses displacement calculated from the same contact stiffness used to compute elastic modulus. The hardness of 95Sn-5Sb was calculated to be 228 MPa. A similar procedure was used to measure modulus and hardness for the other four high temperature solders.

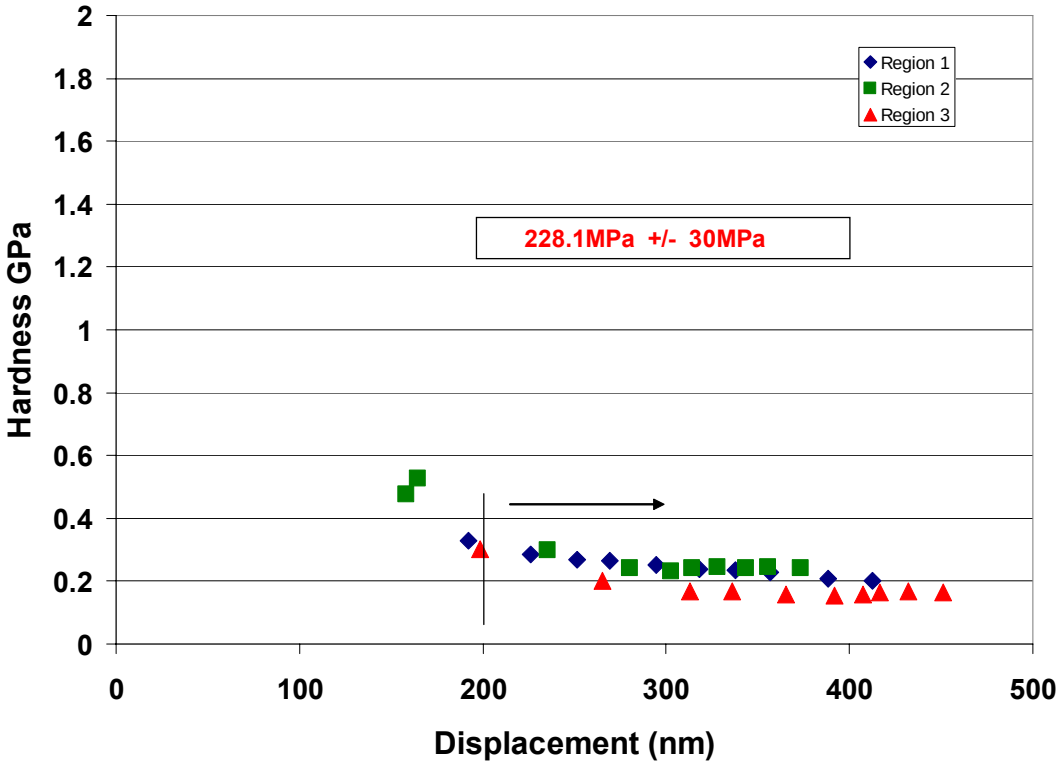


Figure 4.24. Plot of results from a dynamic nanoindentation test. Hardness as a function of depth for 95Sn-5Sb.

A chart comparing the measured elastic modulus of the solders is shown in Figure 4.25. As expected the stiffest solder is the tin based 95Sn-5Sb. Of the lead-based solders, 95Pb-5In had the largest modulus at 27 GPa while the other three lead-based solders measured between 16 and 19 GPa with overlapping margins of error. In addition, the modulus values for the wires were compared to the pastes. Figure 4.26 is a plot comparing the elastic modulus of the wire and paste forms of 90Pb-10Sn and 92.5Pb-5Sn-2.5Ag. Both solders are in very good agreement with overlapping margins of error. This is as expected since elastic modulus is not predicted to change significantly with grain size.

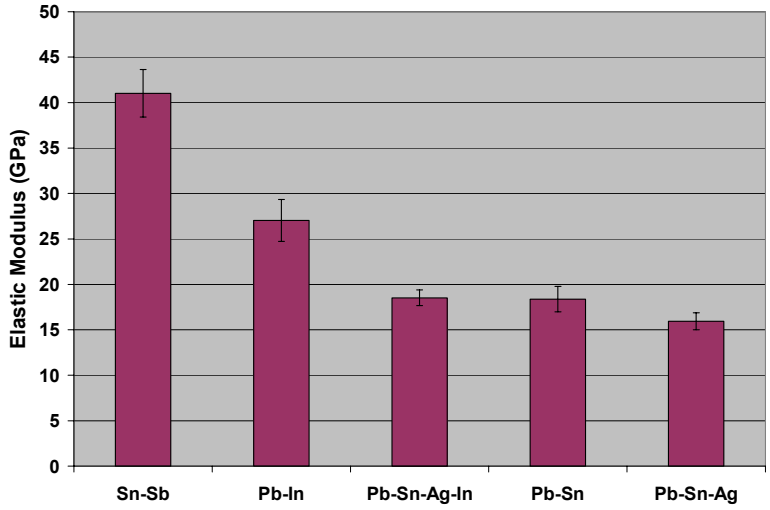


Figure 4.25. Plot comparing the elastic modulus of five high temperature solders measured via dynamic nanoindentation.

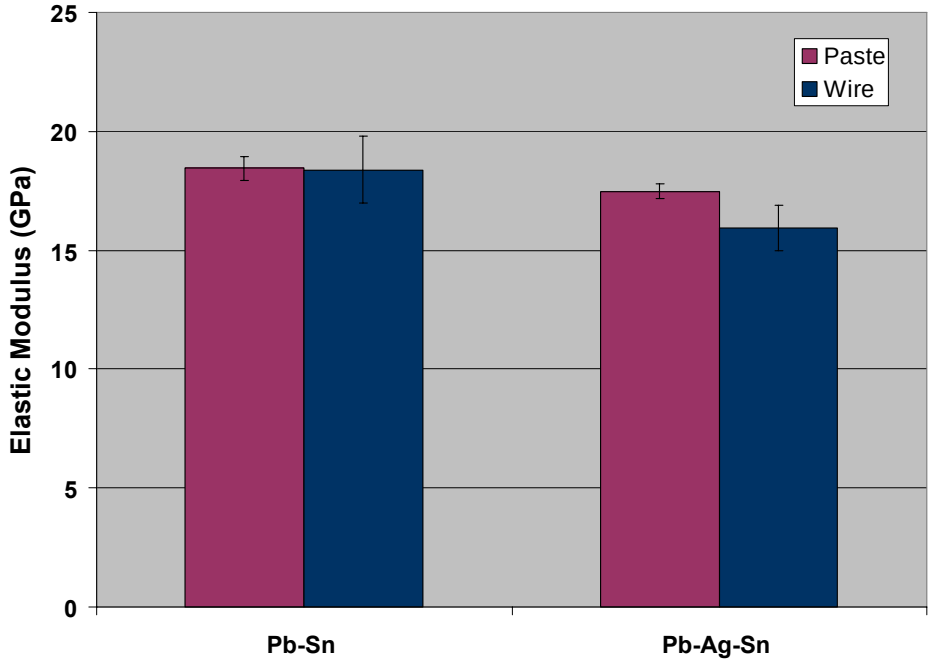


Figure 4.26. Plot comparing the elastic modulus of the wire and paste forms of 90Pb-10Sn and 92.5Pb-5Sn-2.5Ag.

4.3.2 Nanoindentation Creep

Nanoindentation was also used to characterize the creep behavior of the five high temperature solders in this study. Even though nanoindentation creep is a fairly new technique, it offers advantages over standard creep testing in that testing requires significantly less material and tests are completed in a fraction of the time [9]. The stress exponent, which gives the mechanism of creep, is determined from slope of the log strain/log stress plot. Figure 4.27 shows an example calculation of the stress exponent for Sn95-Sb5. The creep resistance of each solder was compared by determining the

strain rate under constant stress. As seen in Figure 4.28, Sn95-Sb5 shows the greatest creep resistance at room temperature.

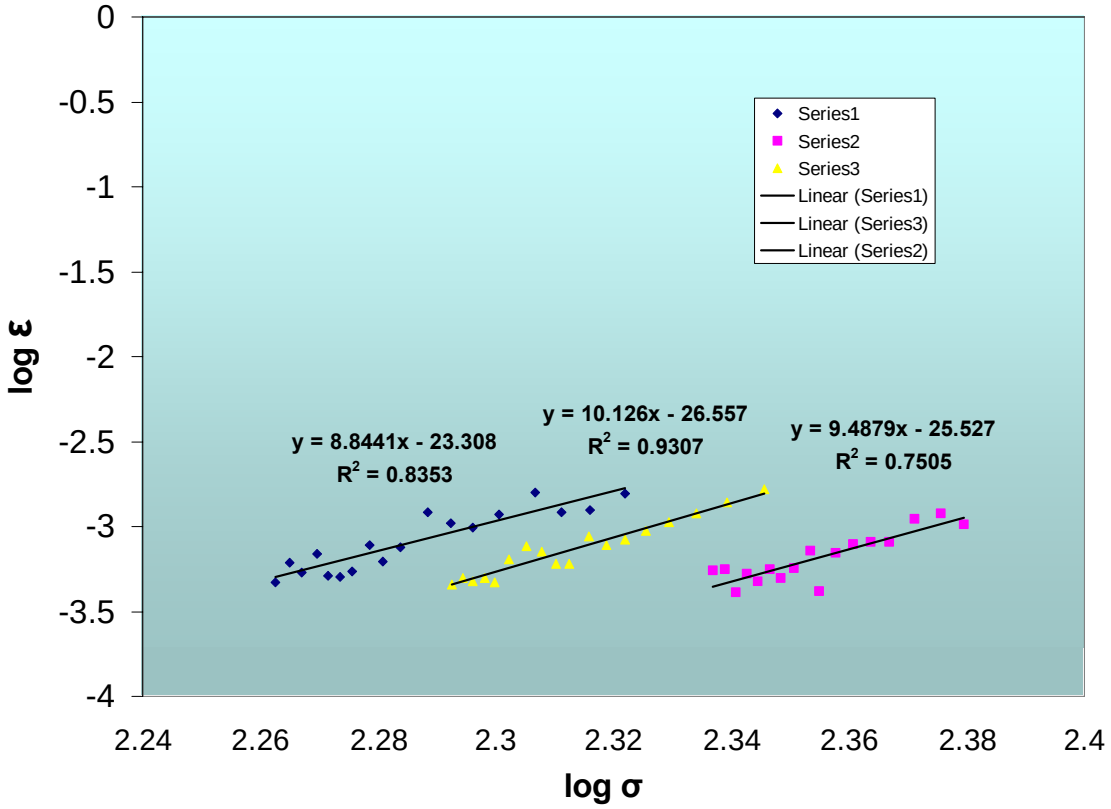


Figure 4.27. Estimation of the stress exponent for Sn95-Sn5 using quasi-static nanoindentation.

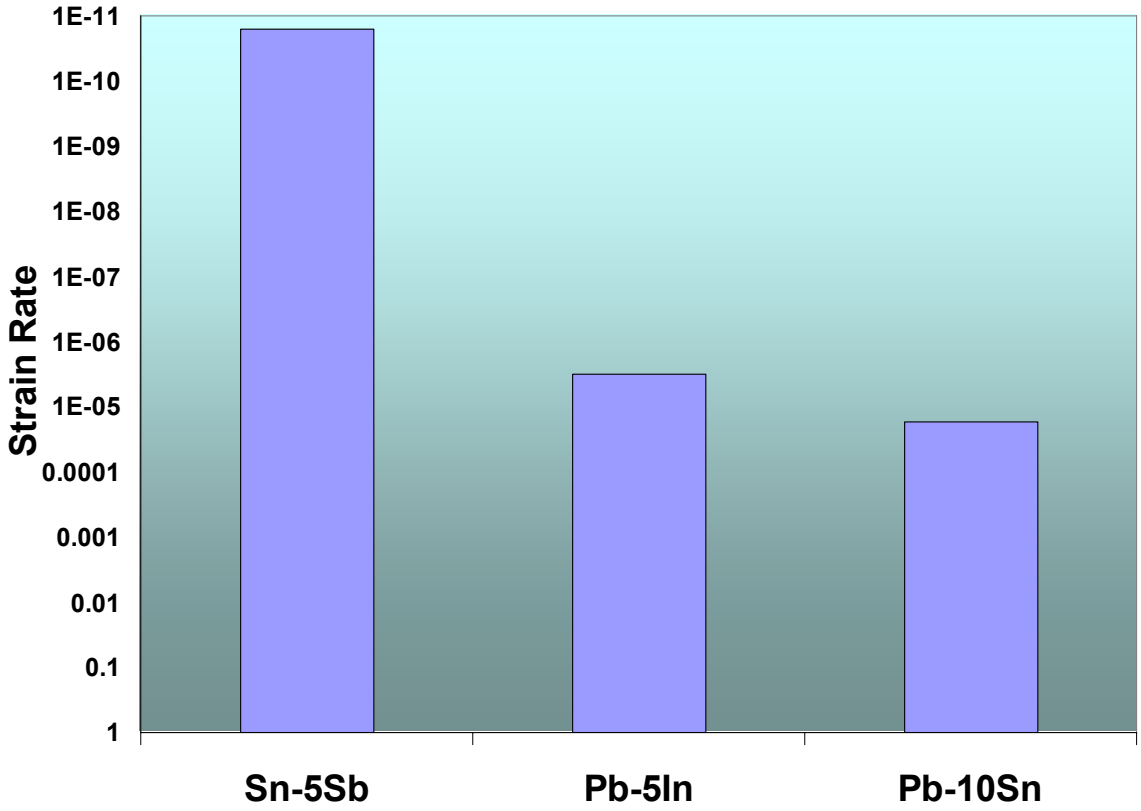


Figure 4.28. Comparison of the creep resistance of Sn95-Sb5, Pb95-In5, and Pb90-Sn10 determined through nanoindentation.

4.4 Solder Tensile Testing

Tensile testing of the five high melting temperature solders was performed to determine their mechanical properties. The solders were chosen such that their melting temperature was greater than the fatigue test temperature cycle (250°C) but less than the glass transition temperature of polyimide (400°C). The five solders are 90Pb-10Sn, 95Sn-5Sb, 92.5Pb-5Sn-2.5Ag, 95Pb-5In, and 93Pb-3Sn-2Ag-2In. All experiments were preformed on 3.175 mm diameter solder wire obtained from the Indium Corporation.

4.4.1 Tensile Testing Procedure

Mechanical tensile tests were performed using a MTS servohydraulic machine with a 5kN load cell and self-tightening wedge grips. In accordance with ASTM Standard E8-04, a 12.7 mm gage length extensometer was used to measure strain and accurately determine elastic modulus and yield stress. A high temperature furnace around the test specimen was used to determine the stress-strain relation as a function of temperature. Each solder was tested at 23°C, 0.7Tm and 200°C. Inside the furnace, the sample was loaded into the grips and the extensometer attached at room temperature. Once the desired temperature was reached and held for 30 minutes, the extensometer was zeroed and the test was conducted. Elongation of each solder was measured in a separate test without the extensometer. The MTS system LVDT was used to measure percent elongation due to the large strains encountered.

4.4.2 Strain Rate Study

The effect of strain rate on the mechanical properties obtained from tensile testing is well documented [10]. To eliminate time-dependent plasticity from the results 90Pb-10Sn, 95Sn-5Sb, and 92.5Pb-5Sn-2.5Ag were pulled at 0.5%/sec, 1%/sec, and 5%/sec. Results from the strain rate experiment are shown in Figures 4.29 and 4.30. In Figure 4.29, the measured elastic modulus is shown to steadily increase with increasing strain rate. For example, the modulus for 95Sn-5Sb was shown to increase from 38 GPa at 0.5%/sec to 43.9GPa at 5%/sec which is in close agreement with the National Institute of Standards and Technology (NIST) reported value of 44.5GPa [8]. At slower strain rates, deformation from creep is added to elastic deformation from the applied stress lowering the value of elastic modulus. The effect of strain rate had a similar effect on the ultimate tensile strength of the tested solders. As shown in Figure 4.30, the tensile strength of each solder decreases with decreasing strain rate. Again the added creep deformation of slower strain rates leads to premature necking, limiting the magnitude of the ultimate tensile strength.

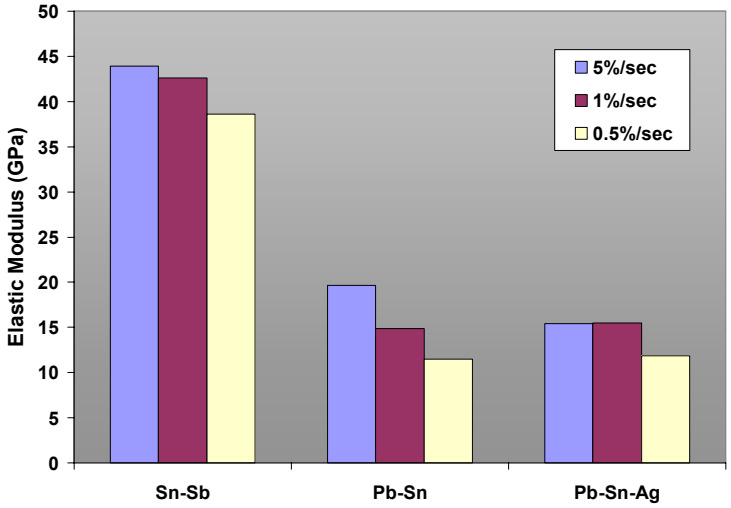


Figure 4.29. Bar graph relating the effect of strain rate on average elastic modulus of 95Sn-5Sb, 90Pb-10Sn, and 92.5Pb-5Sn-2.5Ag.

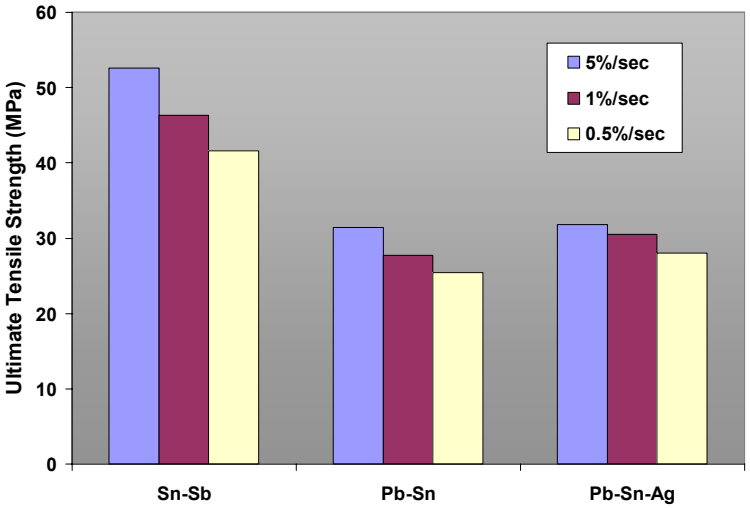


Figure 4.30. Bar graph relating the effect of strain rate on average ultimate tensile strength for 95Sn-5Sb, 90Pb-10Sn, and 92.5Pb-5Sn-2.5Ag.

In addition to the observed effects on elastic modulus and yield strength, the effect of strain rate can be quantified through the strain rate sensitivity exponent. This phenomenon is expressed by power law relation:

$$\sigma_f = C\dot{\varepsilon}^{m} \tag{6}$$

where σ is the flow stress, C is the strength coefficient, and m is the strain rate sensitivity exponent [7]. The strain rate sensitivity exponent was extracted from the tensile test data from the slope of the plastic portion of the log stress/log strain rate curve. An example plot for Sn95-Sb5 at room temperature is shown in Figure 4.31. Physically, the strain rate sensitivity exponent is a measure of the materials resistance to further deformation after the onset of necking. In this sense, strain rate sensitivity exponent along with the strain hardening coefficient, gives some indication as to the total elongation possible for a given material. Assuming the strain hardening exponent of two materials are equal, a material with a larger strain rate sensitivity exponent will have greater elongation. A chart comparing the strain rate sensitivity of Pb90-Sn10, Pb92.5-Sn5-Ag2.5, and Sn95-Sb5 is shown in Figure 4.32. At room temperature, Sn95-Sb5 showed the highest strain rate sensitivity meaning it shows greater resistance to further necking after the onset of necking. It should be noted, however, that the strain rate sensitivity is quite low for all three solders, well below the super-plasticity zone where m falls between $0.3 < m < 0.7$.

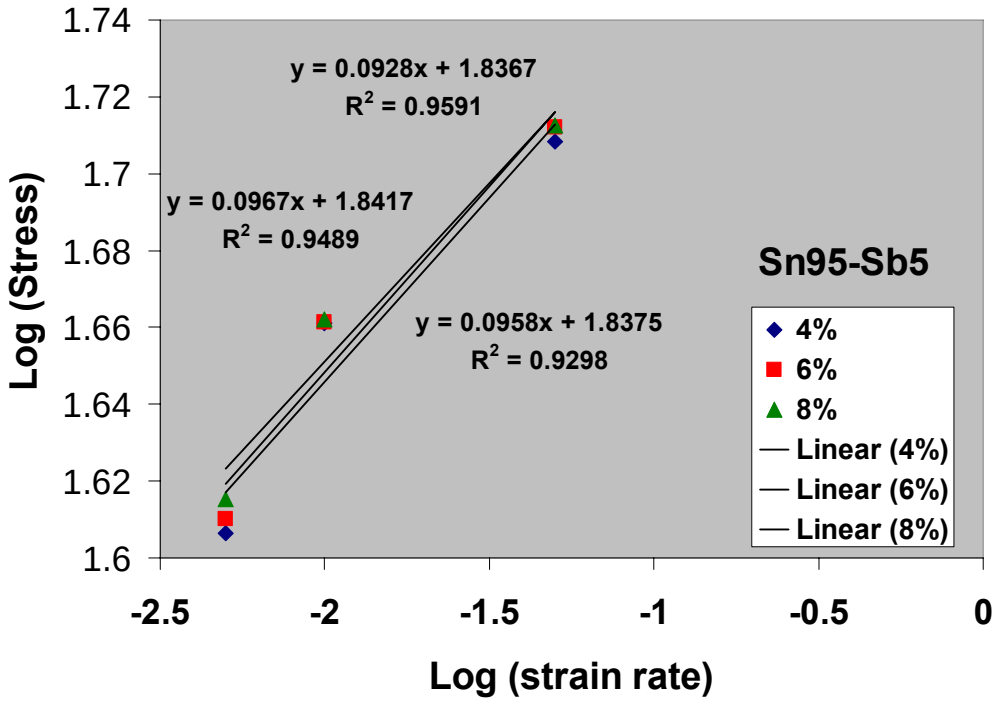


Figure 4.31. Room temperature plot of log (stress) vs. Log (strain rate) for Sn95-Sb5. The strain-rate sensitivity exponent is extracted from the slope of the curve.

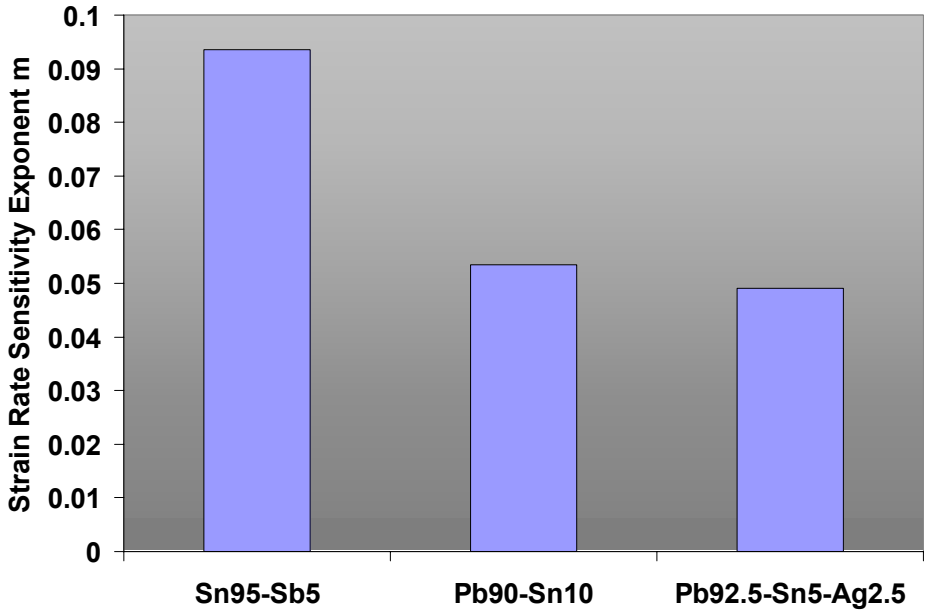


Figure 4.32. Chart comparing the average strain rate sensitivity exponent for Sn95-Sb5, Pb90-Sn10, and Pb92.5-Sn5-Ag2.5.

4.4.3 Room Temperature Results

Following this study, a strain rate of 5%/sec was chosen for the remaining tests because it eliminates creep deformation and it produces results consistent with published values for 95Sn-5Sb, and 90Pb-10Sn [10]. Similar studies have shown that increasing the strain rate further has little affect on the constitutive response [10].

Figure 4.33 shows a comparison of the stress-strain curves for all five solders pulled at a strain rate of 5%/sec in the 0-10% stain range. 95Sn-5Sb showed the strongest mechanical performance of the five primarily because it is a tin based solder while the other four contain >90% lead. Additionally, the SnSb second phase precipitate discussed earlier enhances the solders strength through dispersion strengthening.

Of all the lead based solders, 93Pb-3Sn-2Ag-2In performed the best. While its measured elastic modulus was found to be similar to the other lead based solders in this study, its ultimate tensile strength was significantly higher. In Figure 4.34, the ultimate tensile strengths of the five solders are compared. As expected, 95Sn-5Sb showed the largest ultimate tensile strength followed by 93Pb-3Sn-2Ag-2In which outperformed the other lead solders by roughly 25%. Surprisingly, this solder is quite close in composition to 92.5Pb-5Sn-2.5Ag which arguably showed the weakest performance.

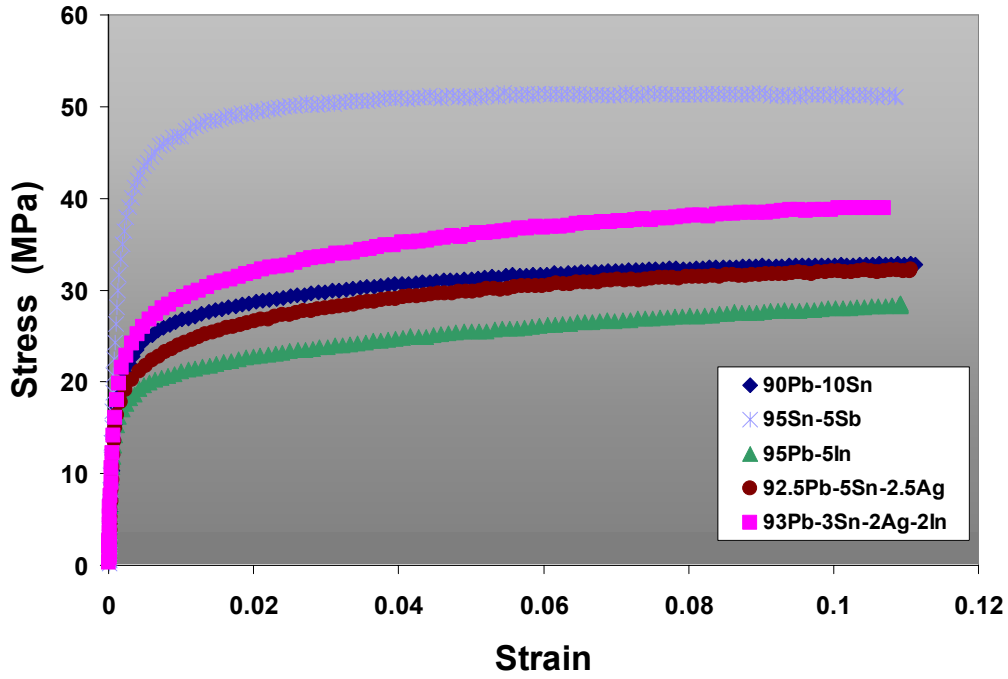


Figure 4.33. Representative stress-strain curves for all five solders pulled at a strain rate of 5%/sec in the 0-10% stain range.

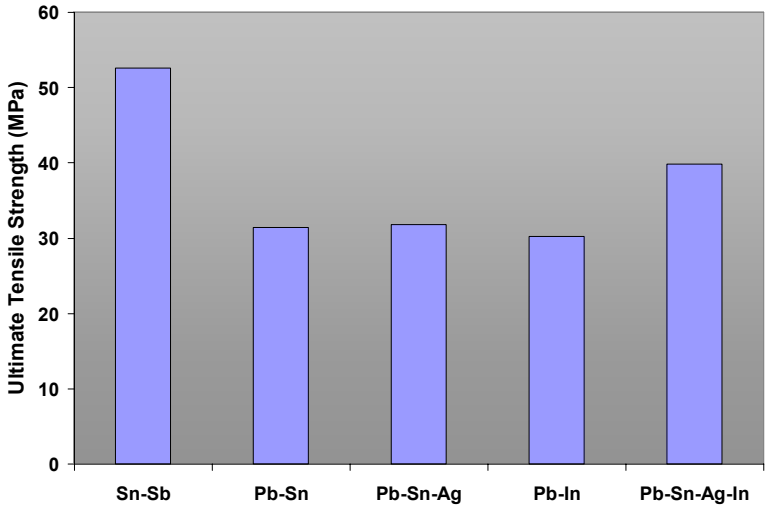


Figure 4.34. Bar graph comparing the average ultimate tensile strength of 95Sn-5Sb, 90Pb-10Sn, 92.5Pb-5Sn-2.5Ag, 95Pb-5In, and 93Pb-3Sn-2Ag-2In.

Figure 4.35 shows a comparison of the stress-strain curves for all five solders pulled at a strain rate of 5%/sec in the 0-1% strain range. This plot illustrates the highly plastic nature of these solders. The elastic limit of the solders is reached well before the conventional 0.2% strain typically used to compute yield strength. Similar studies have used deviation from linearity to calculate elastic modulus and yield strength, but such methods are highly arbitrary. To standardize the process, this study used a 0.02% offset method to determine the yield strength of the solders.

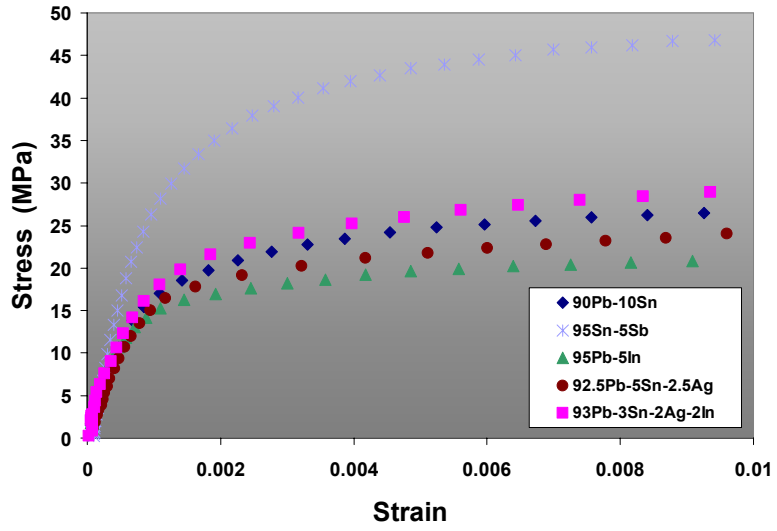


Figure 4.35. Representative stress-strain curves for all five solders pulled at a strain rate of 5%/sec in the 0-1% stain range.

A comparison of the elastic modulus for the solders can be seen in Figure 4.36. All of the Pb-based solders measured between 15-20 GPa. This was expected since EDS revealed the matrix of these solders to be mostly Pb. As is often the case, the secondary and tertiary elements combine to form additional phases at the expense of the matrix of the solder. The yield strengths of the solders are compared in Figure 4.37. Similar to the

ultimate tensile strength measurements, 95Sn-5Sb and 93Pb-3Sn-2Ag-2In showed the highest strength. Again 92.5Pb-5Sn-2.5Ag underperformed the other solders studied.

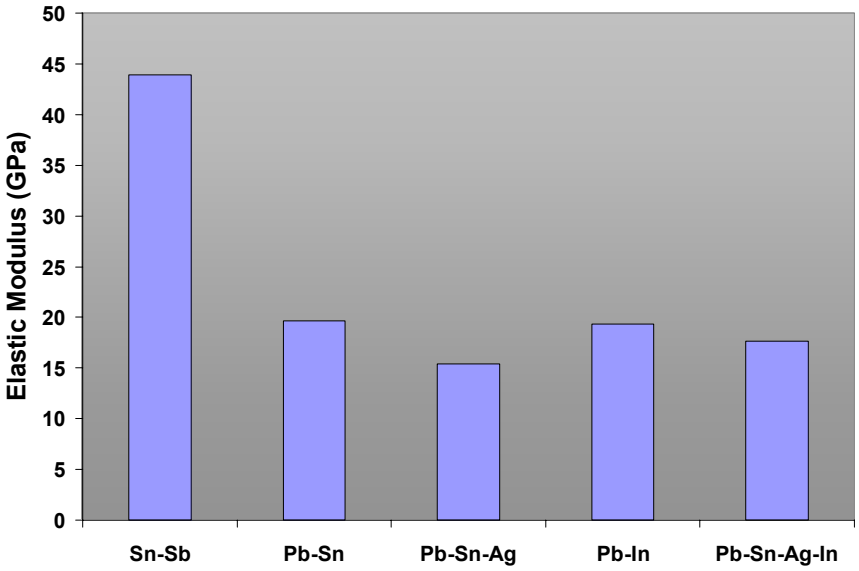


Figure 4.36. Bar graph comparing the average elastic modulus of 95Sn-5Sb, 90Pb-10Sn, 92.5Pb-5Sn-2.5Ag, 95Pb-5In, and 93Pb-3Sn-2Ag-2In at room temperature.

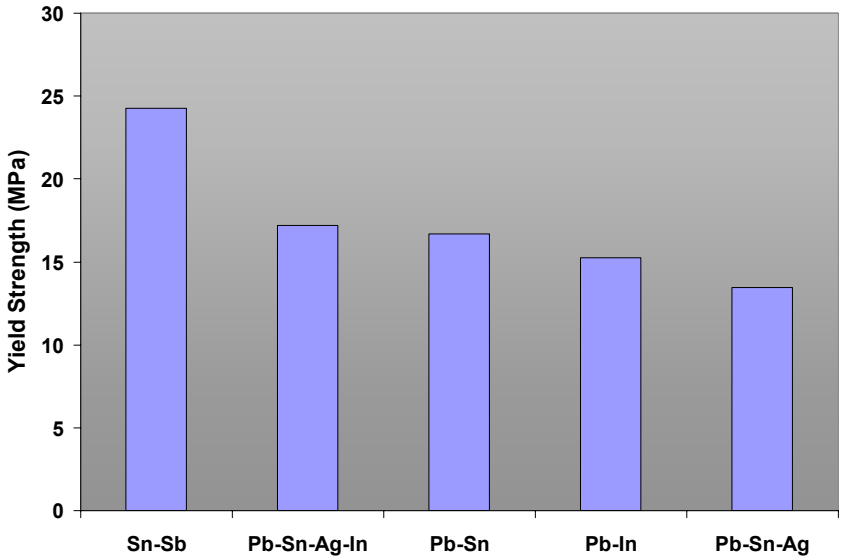


Figure 4.37. Bar graph comparing the average yield strength of 95Sn-5Sb, 90Pb-10Sn, 92.5Pb-5Sn-2.5Ag, 95Pb-5In, and 93Pb-3Sn-2Ag-2In at room temperature.

4.4.4 High Temperature Results

Following the procedure outlined earlier, each solder was tested at 0.7Tm and 200˚C. The homologous temperature, 0.7Tm, was chosen rather then a fixed median temperature to isolate the true compositional mechanical strength from the temperature effect. The homologous temperature 0.7Tm for each solder Sn95-Sb5 (87°C), Pb90-Sn10 (129°C), Pb92.5-Sn5-Ag2.5 (125°C), Pb95-In5 (137°C), Pb93-Sn3-Ag2-In2 (131°C) is calculated by multiplying the melting temperature in Kelvin by 0.7. Figure 4.38 shows the

resulting stress-strain curves for each solder tested at 0.7Tm. The results at 0.7Tm show a very similar trend to the room temperature results with Sn95-Sb5 outperforming the Pb-based solders. Of the Pb-based solders, Pb93-Sn3-Ag2-In2, again showed the greatest strength and Pb95-In5 showed the lowest strength just as in the room temperature test. The similar trend between room temperature and 0.7Tm results are not surprising since there are no phase changes in the solders and all of the Pb-based solders have similar melting temperatures. Charts comparing the elastic modulus and ultimate tensile strength of the solders are shown in Figures 4.39 and 4.40 respectively. All of the solders experience a drop in modulus as would be expected at 0.7Tm, however, the three solders with high temperature intermetallic phases (Sn95-Sb5, Pb92.5-Sn5-Ag2.5, and Pb93-Sn3-Ag2-In2) show much smaller decreases.

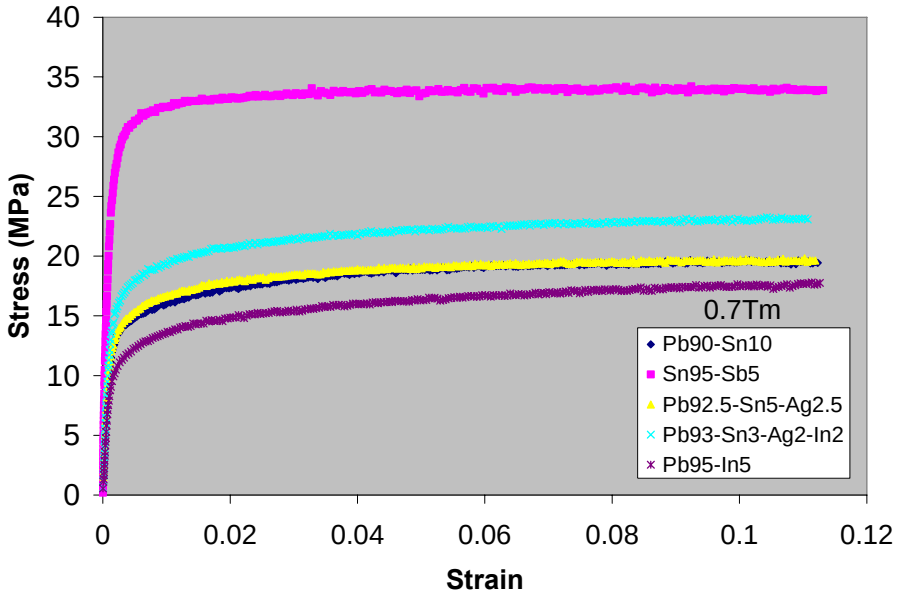


Figure 4.38. Representative stress-strain curves for all five solders tensile tested at 0.7Tm in the 0-10% strain range.

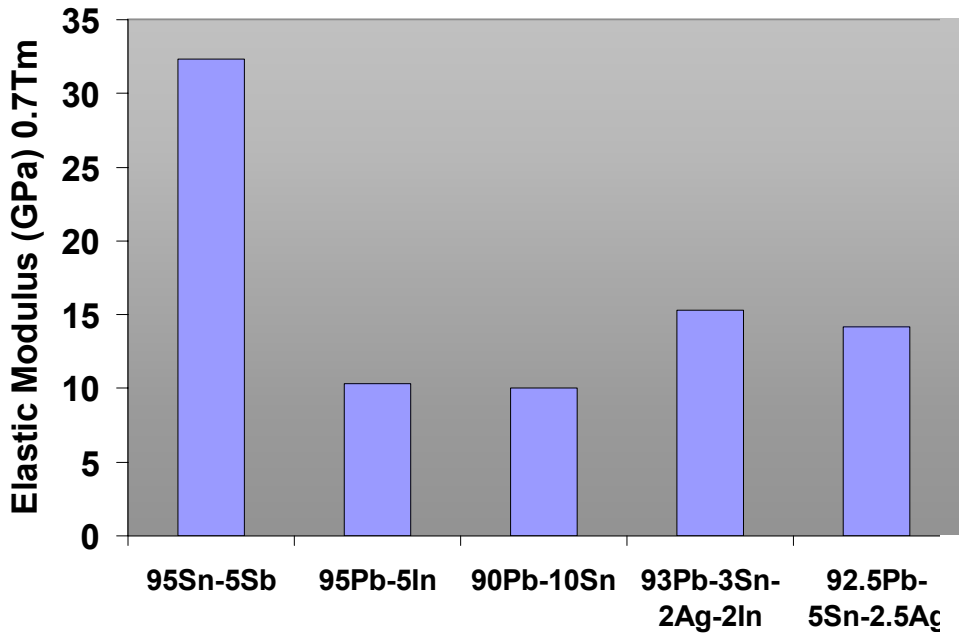


Figure 4.39. Bar graph comparing the average elastic modulus of 95Sn-5Sb, 90Pb-10Sn, 92.5Pb-5Sn-2.5Ag, 95Pb-5In, and 93Pb-3Sn-2Ag-2In at 0.7Tm.

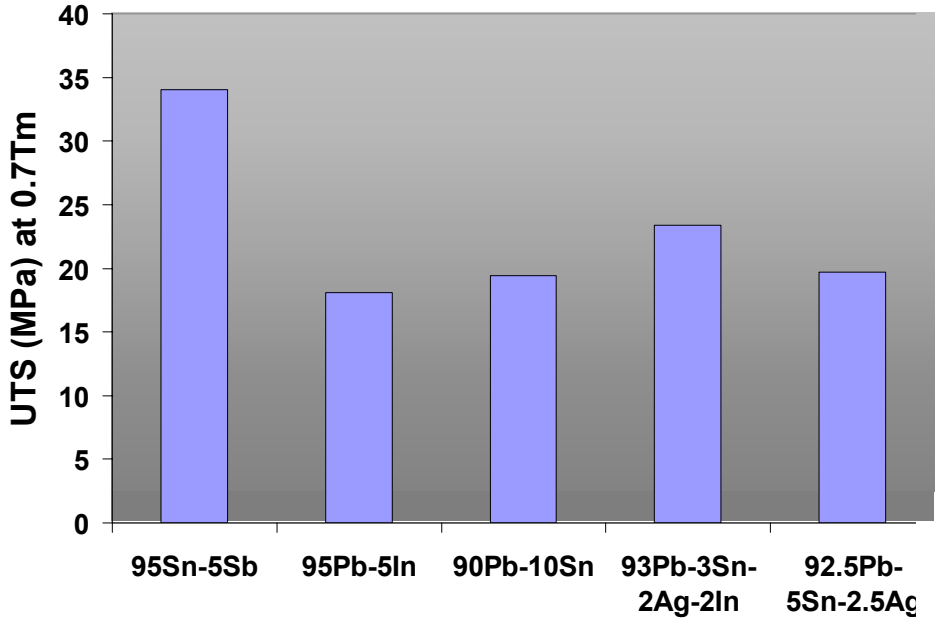


Figure 4.40. Bar graph comparing the average UTS of 95Sn-5Sb, 90Pb-10Sn, 92.5Pb-5Sn-2.5Ag, 95Pb-5In, and 93Pb-3Sn-2Ag-2In at 0.7Tm.

The preceding trends change rather dramatically at 200°C. As can be seen in Figure 4.41, Pb90-Sn10 now slightly outperforms the other solders and Pb92.5-Sn5-Ag2.5 shows the lowest strength. Sn95-Sb5 no longer shows the highest strength because of its high homologous temperature (.93Tm) at 200°C. A chart comparing the strength and modulus of each solder at 23°C, 0.7Tm, and 200°C is shown in Figures 4.42 and 4.43 respectively.

As mentioned earlier, the trend in ultimate tensile strength after 23°C and 0.7Tm are very similar, however these trends change significantly at 200°C.

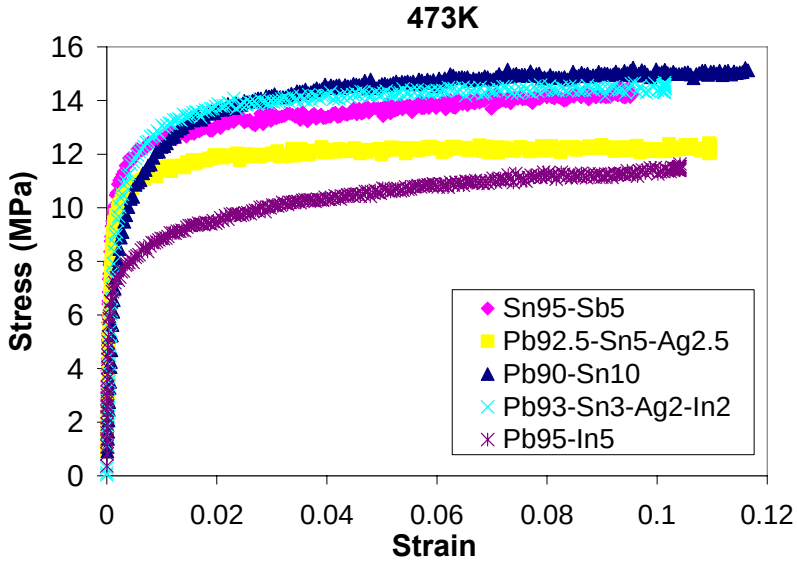


Figure 4.41. Representative stress-strain curves for 95Sn-5Sb, 90Pb-10Sn, 92.5Pb-5Sn-2.5Ag, and 93Pb-3Sn-2Ag-2In pulled at 200°C in the 0-10% strain range.

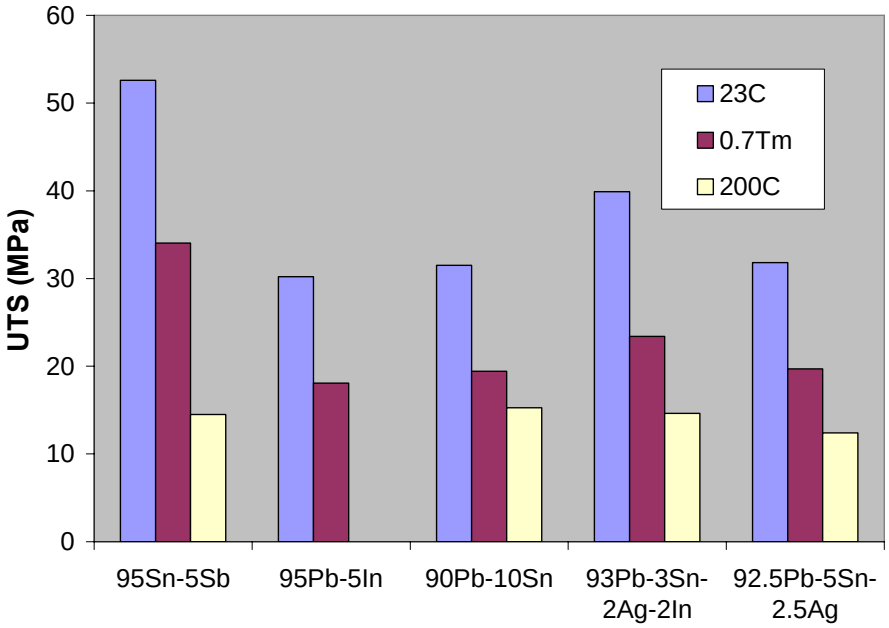


Figure 4.42. Bar graph comparing the average UTS of 95Sn-5Sb, 90Pb-10Sn, 92.5Pb-5Sn-2.5Ag, and 93Pb-3Sn-2Ag-2In at 23°C, 0.7Tm, and 200°C.

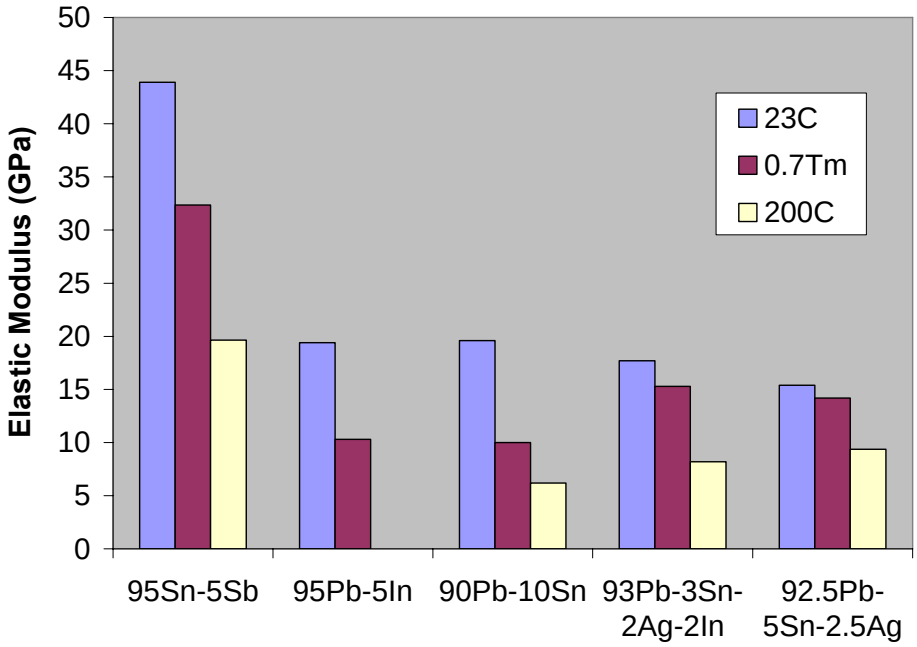


Figure 4.43. Bar graph comparing the average elastic modulus of 95Sn-5Sb, 90Pb-10Sn, 92.5Pb-5Sn-2.5Ag, and 93Pb-3Sn-2Ag-2In at 23°C, 0.7Tm, and 200°C.

Deviation from the previous trend can be attributed to phase transformation and different homologous temperatures of each of the solders. For instance, in addition to its high homologous temperature, Sn95-Sb5 undergoes a phase change at 200°C. Figure 4.5 shows an optical image of the Sn95-Sb5 microstructure. Two distinct phases can be identified from this image, the Sn-rich matrix of the solder, and the SnSb intermetallic phase distributed throughout the matrix. The Sn-Sb phase diagram shown in Figure 4.44 shows at approximately 180°C the intermetallic compound SnSb dissolves into the tin rich matrix forming a single phase alloy. Previously at 23°C and 87°C the intermetallic phase SnSb reinforces the matrix because of its small size and regular dispersion impedes dislocation motion. However at 200°C, this phase disappears further reducing the tensile strength of the solder.

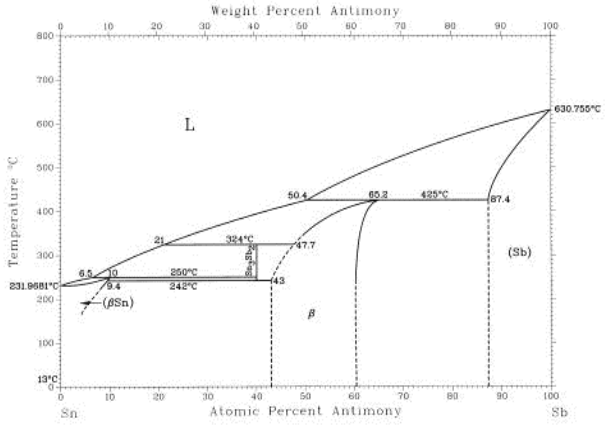


Figure 4.44. Sn-Sb phase diagram [11].

Pb90-Sn10 experiences a similar transformation resulting in microstructural changes when the solder is heated from 129°C to 200°C. Like Sn95-Sb5, Pb90-Sn10 shows two distinct phases at room temperature, a Pb-rich matrix and Sn-rich second phase as seen in the Figure 4.3. Figure 4.45 below shows the Pb-Sn phase diagram. Following the Pb90-Sn10 compositional line, the Sn-rich dissolves back into the Pb-rich matrix at temperatures greater than 150°C. However, Pb90-Sn10 shows only a small reduction in tensile strength between 129°C and 200°C because solid solution hardening of the Pb FCC structure with the larger tin atoms at interstitial sites.

Pb92.5-Sn5-Ag2.5 and Pb93-Sn3-Ag2-In2 on the other hand, do not undergo phase change up to 200°C. The high temperature intermetallic phases in each of the solders do not dissolve back into the Pb-rich matrix. In fact these compounds often coarsen with high temperature aging at the expense of the matrix. So the reduction in the mechanical strength in this case is primarily a function of temperature, rather than temperature and phase change.

These results highlight the importance of understanding the relationship between microstructure and mechanical strength. Under temperature and stress, materials can undergo phase transformations which affect the mechanical response of the material. For example Pb90-Sn10 and Pb92.5-Sn5-Ag2.5 have similar melting temperatures and showed nearly identical mechanical strength at room temperature and 0.7Tm. However at 200°C, there is a large disparity in mechanical strength between the two because of the phase change of Pb90-Sn10.

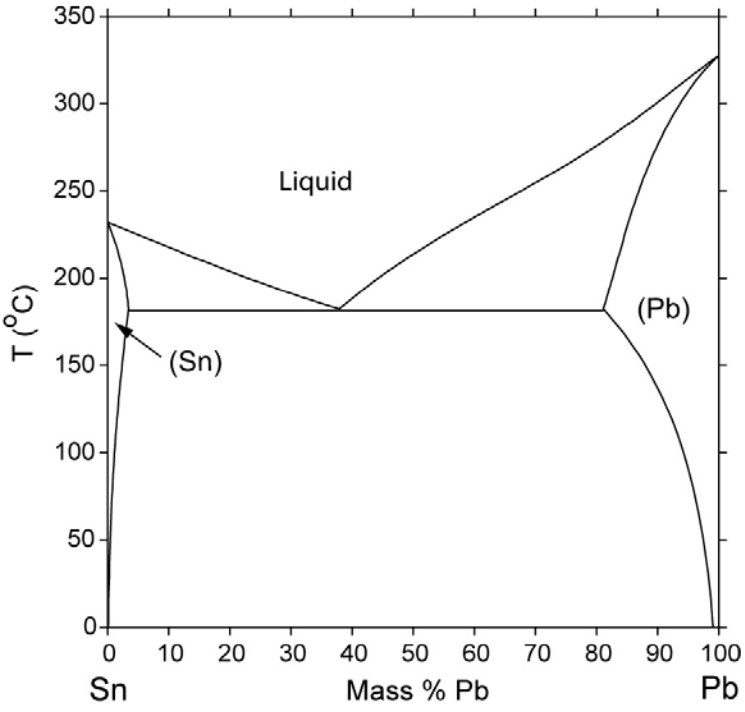


Figure 4.45. Pb-Sn phase diagram [11].

4.4.5 Strain Hardening Results

A key parameter of solder joint fatigue resistance is the total elongation possible before fracture. The strain hardening exponent is a measure of a materials resistance to the

onset of necking. In this sense, strain hardening can give a preliminary estimation of the elongation behavior of the material. As a material is plastically deformed, dislocations pile up, increasing the strength of the material. This phenomenon is described by Holloman's equation:

$$\sigma = K\varepsilon_p^{\ n} \tag{7}$$

where σ is the flow stress, K is a stress coefficient, ε is the plastic strain, and n is the strain hardening coefficient [7]. The strain hardening exponent can be extracted from the slope of plastic region of the true stress/true strain curve. An example plot for Pb90-Sn10 at room temperature is shown in Figure 4.46. Figure 4.47 shows the strain hardening behavior of each of the solders as a function of temperature. At room temperature Pb95-In5 shows the greatest strain hardening followed by Pb93-Sn3-Ag2-In2, Pb92.5-Sn5-Ag2.5, Pb90-Sn10, and Sn95-Sb5.

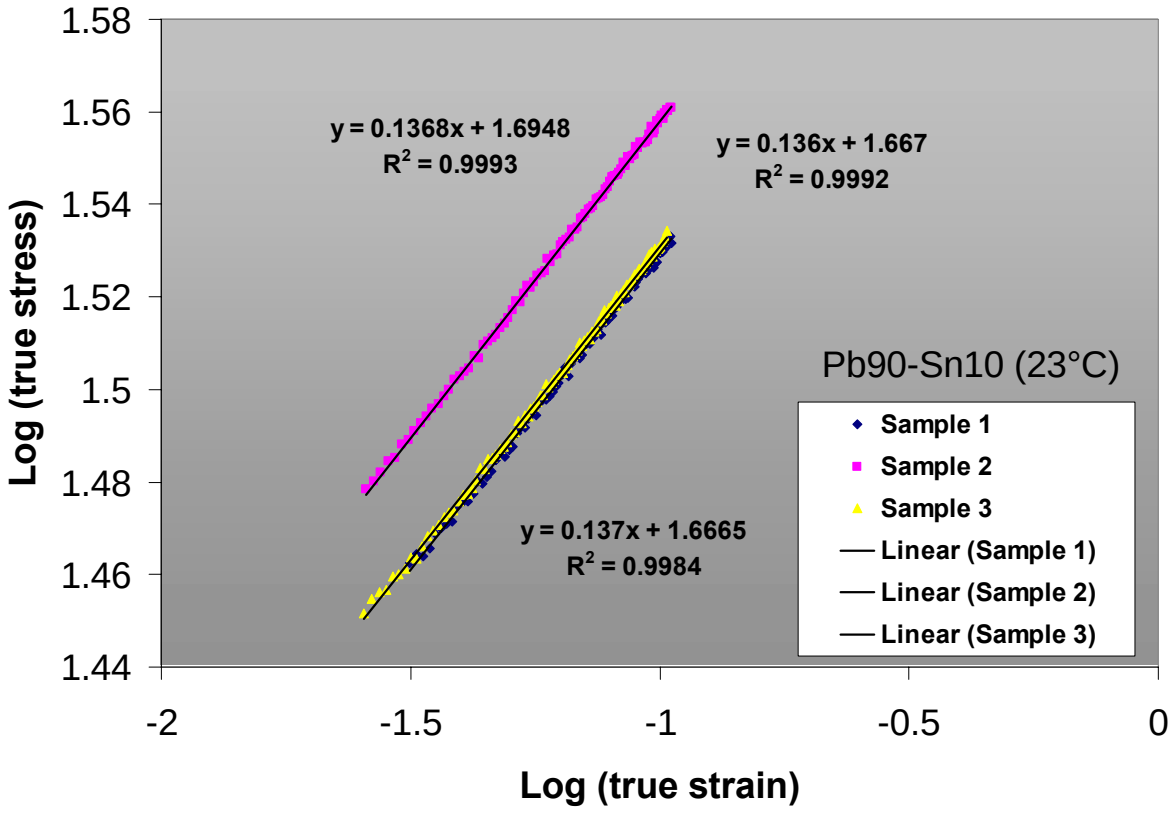


Figure 4.46. Plot of log (true stress)/log (true strain) to determine the strain hardening coefficient of Pb90-Sn10 at 23°C

The three solders that do not undergo a phase transformation, Pb93-Sn3-Ag2-In2, Pb92.5-Sn5-Ag2.5, and Pb95-In5 show similar decreases in strain hardening dn/dT indicating the decrease in strain hardening is primarily a function of temperature. The change in strain hardening with respect to temperature for Pb90-Sn10, and Sn95-Sb5, on the other hand, shows a different behavior indicating dn/dT is a function of both

temperature and phase change for these solders. The complete results of the tensile testing for each solder are summarized in Table 4.2.

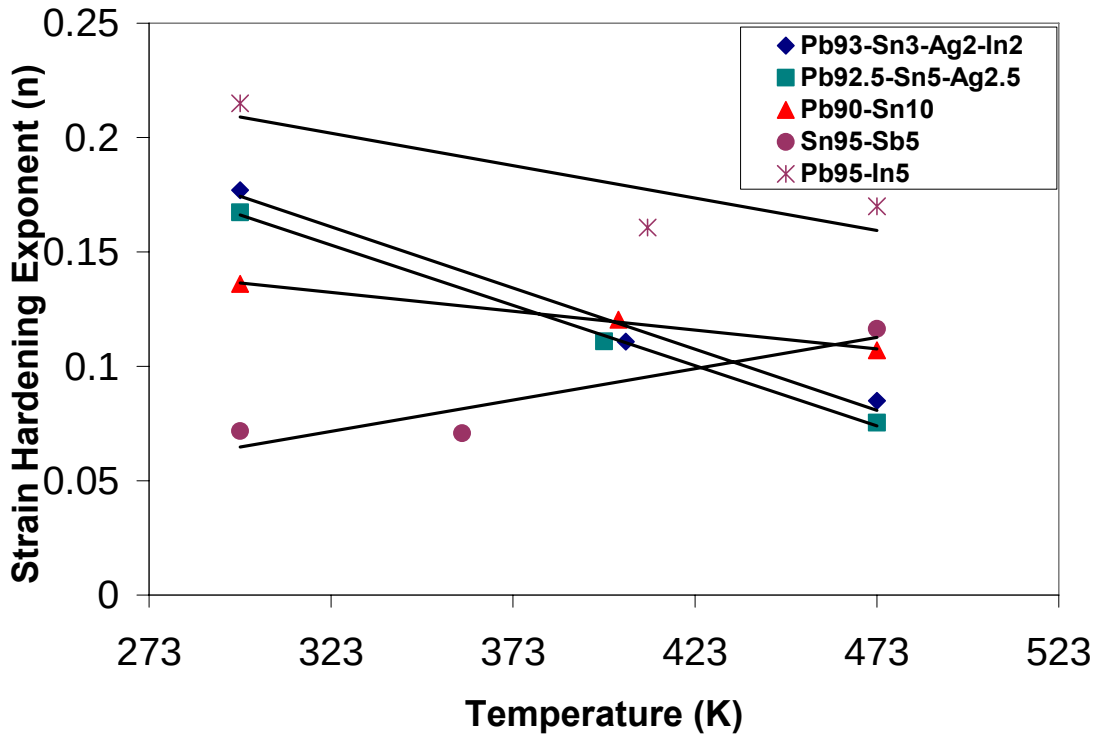


Figure 4.47. Plot of average strain hardening coefficient verses temperature for 95Sn-5Sb, 90Pb-10Sn, 92.5Pb-5Sn-2.5Ag, 95Pb-5In, and 93Pb-3Sn-2Ag-2In.

Table 4.2 Time-independent mechanical properties

SOLDER	E (Modulus) Tensile (GPa)	E (Modulus) Tensile @ .7Tm (GPa)	E (Modulus) Tensile @ 200C (GPa)	Ultimate Tensile Strength (MPa)	Ultimate Tensile Strength @ .7Tm (MPa)	Ultimate Tensile Strength @ 200C (MPa)	Strain Hardening Exponent n @ 23C	Strain Hardening Exponent n @ .7Tm	Strain Hardening Exponent n @ 200C	Strain Rate Sensitivity Exponent m @ 23C	E Dynamic Nanoindentation (GPa)	Nanoindentation Hardness (MPa)
95Sn-5Sb	43.9	32.4	19.6	52.6	34.0	14.5	0.072	0.076	0.116	0.094	41.0	228.1
95Pb-5In	19.4	10.3	9.9	30.2	18.1	11.6	0.215	0.161	0.170		18.7	191.8
90Pb-10Sn	19.6	10.0	6.2	31.5	19.4	15.3	0.136	0.120	0.107	0.053	18.4	190.0
93Pb-3Sn-2Ag-2In	17.7	15.3	8.2	39.9	23.4	14.6	0.177	0.111	0.085		18.5	151.6
92.5Pb-5Sn-2.5Ag	15.7	14.2	9.4	31.8	19.7	12.4	0.167	0.111	0.075	0.049	15.9	110.8

4.5 Passive Device Solder Model

A passive device solder model was constructed in ANSYS to simulate the equivalent plastic strain generated from thermal expansion mismatches. These plastic strain results were then used in conjunction with other mechanical properties determined from testing in preceding sections to estimate the fatigue life of the solder joint. A 2-D plane-strain elastic/plastic ANSYS model with ½ symmetry is shown in Figure 4.48. Table 4.3a shows the constitutive relations assumed for each component of the model. Table 4.3b shows the dimensions used for each component of the model. Note that the wetting angle between the pad and solder is 45 degrees and the solder reaches 50% the resistor height. For the initial run only, room temperature time-independent stress-strain data was used for the solder. Thermo-mechanical stresses generated in the joint were simulated by cycling the model from 35°C to 250°C.

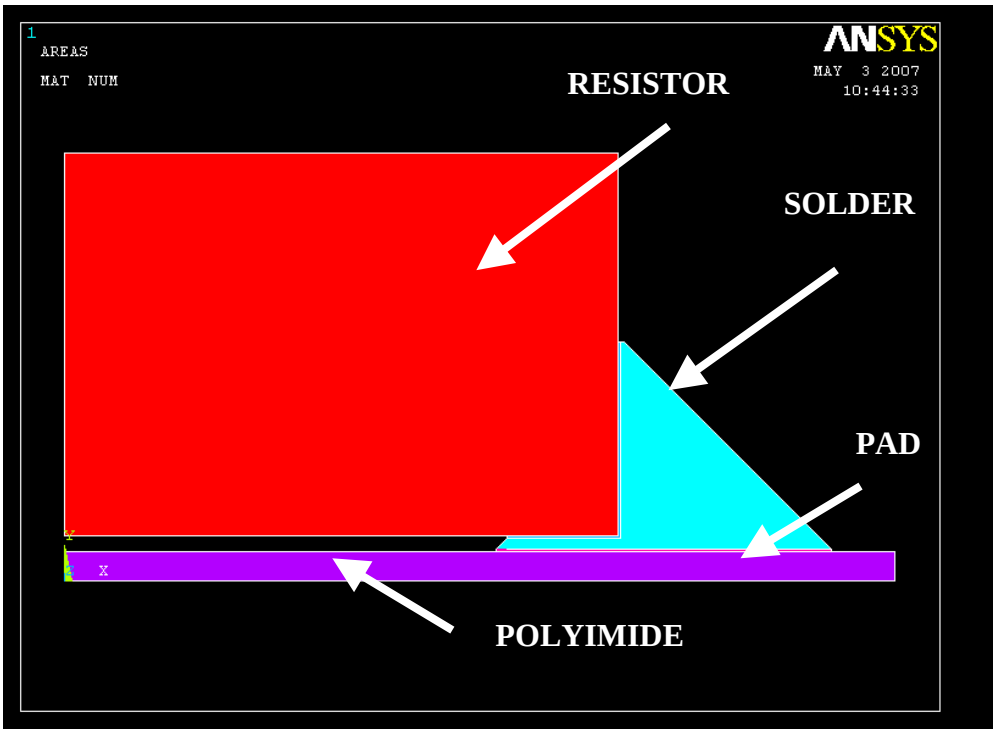


Figure 4.48. Passive device solder model formulated in ANSYS.

Table 4.3a. Constitutive Relations used in ANSYS model.

Component/Material	Constitutive Relation
Substrate/Polyimide (Kapton E)	Temperature dependent elastic-plastic
Pad/Cu/Ni/Au	Temperature dependent elastic-plastic
Solder/Pb90+/Sn95-Sb5	Elastic-plastic
Resistor/Alumina	Elastic

Table 4.3b. Dimensions used in ANSYS model.

Component/Material	Dimensions (L= length)(t=thickness)
Substrate/Polyimide (Kapton E)	L= 3mm, t= 50.8μm
Pad/Cu/Ni/Au	L= 0.6mm, t = 5.75μm composite layer
Solder/Pb90+/Sn95-Sb5	L = 0.6mm, t =20μm (between pad-resist)
Resistor/Alumina	L = 2mm, t = 0.5mm (0805)

Figure 4.49 shows the resulting shear stress distribution after one thermal cycle (35°C - 250°C, 250°C -35°C) for Pb93-Sn3-Ag2-In2. The largest stresses develop at the resistor/solder corner interface highlighted below. This region develops positive shear because the alumina resistor has a smaller CTE (3 ppm/C) than the solder (30 ppm/C). When these stresses exceed the yield strength of the particular solder, plastic strain is generated. After a certain amount of plastic deformation, voids will nucleate leading to crack generation. Cracks will most likely occur in high stress concentration regions such as the resistor/solder corner interface. To estimate the solder's fatigue life, the equivalent plastic strain generated at the resistor/solder corner interface was entered into a fatigue life model.

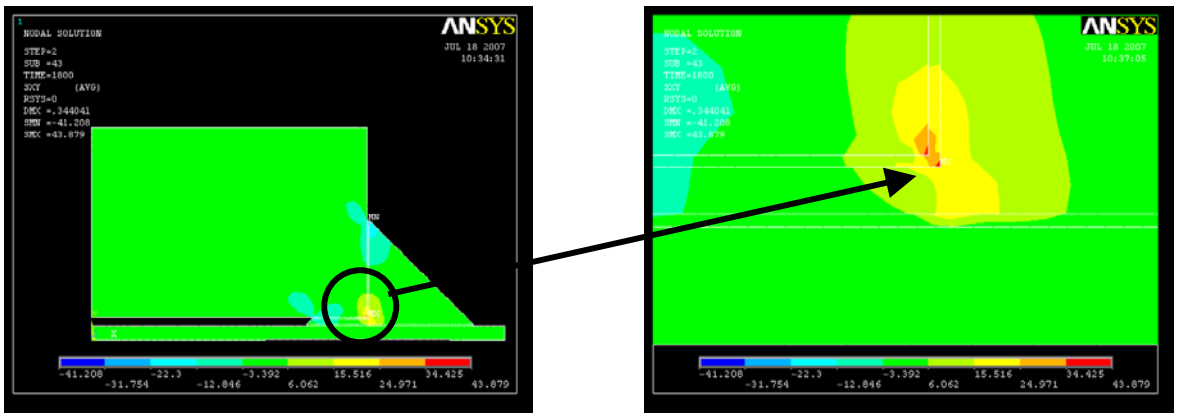


Figure 4.49. Left, ANSYS contour plot of the thermo-mechanical shear stress generated after one thermal cycle for Pb93-Sn3-Ag2-In2. Right, zoom image of stress concentration at the resistor/solder corner interface.

4.5.1 Solder Fatigue Life Model

Fatigue life of the passive device solder joint was estimated using the Engelmaier model for the Pb-based solders and the Kanchanomai model for Sn95-Sb5. The Engelmaier model has been used in several studies to successfully estimate the fatigue life of eutectic Pb-Sn solder [12,13]. Engelmaier's model is a Coffin-Manson based relation that accounts for the mean temperature of the cycle, and the number of cycles per day

$$N_f = \frac{1}{2}\left(\frac{\Delta\varepsilon_p}{2\varepsilon_f}\right)^{1/c} \qquad (8)$$

where ε_p is the equivalent plastic strain per cycle calculated in the ANSYS model, ε_f is the strain at fracture, N_f is the number of cycles to failure, and c is the exponent that accounts for the cyclical frequency and mean temperature of the cycle.

$$c = -0.442-(6\times10^{-4})*Tm+(1.74\times10^{-2})*\ln(1+f) \qquad (9)$$

A median temperature of 125°C and 20 cycles/day were chosen for Tm and f respectively.

Since the composition of Sn95-Sb5 varies from the Pb-based solders substantially, an alternative fatigue model was chosen. Several researchers have reported successful results using the Kanchanomai model for Sn96.5-Ag3.5 which is similar in composition to Sn95-Sb5 [13,14]. Kanchanomai defined the number of cycles to failure by the following relationship:

$$N_f = 27.63\Delta\varepsilon_p^{-1.08} \quad (10)$$

where N_f is the number of cycles to failure and ε_p is the plastic deformation per cycle [12]. Figure 4.50 shows a bar graph ranking the initial estimates of fatigue life for each solder based on room temperature mechanical properties. As expected, Sn95-Sb5 outperforms the Pb-based solders because of its superior mechanical properties at room temperature. Of the Pb-based solders, Pb95-In5 shows the greatest fatigue life primarily because of its significantly higher elongation resulting and greater strain hardening. Pb92.5-Sn5-Ag2.5 showed the least number of cycles to failure in the modeling because of its poor elongation and mechanical strength. Again it must be noted these values are expected to change with the addition of temperature and time-dependent mechanical properties.

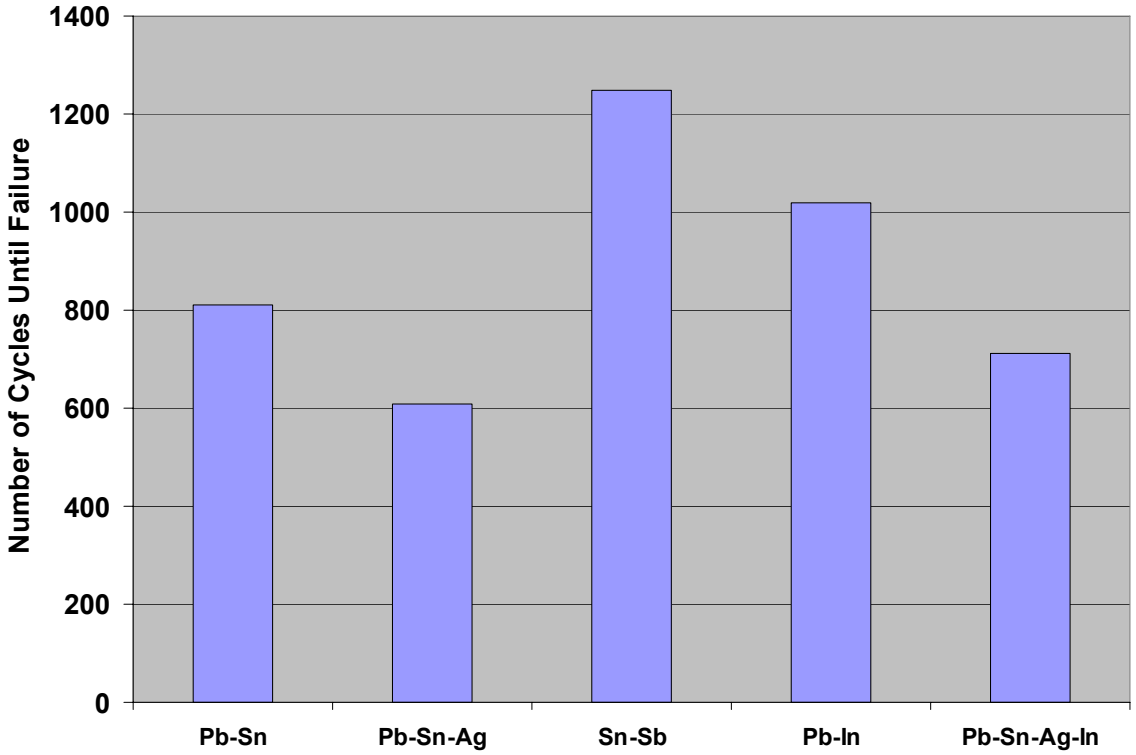


Figure 4.50. Bar chart comparing fatigue life estimations of 95Sn-5Sb, 90Pb-10Sn, 92.5Pb-5Sn-2.5Ag, 95Pb-5In, and 93Pb-3Sn-2Ag-2In using only room temperature mechanical properties.

Next the fatigue models were repeated with elevated temperature stress-strain data. Figure 4.51 shows the results from these models. With the elevated temperature data, Pb95-In5 showed the greatest fatigue life, primarily due to its much higher elongation.

Due to their relatively poor elongation both Pb92.5-Sn5-Ag2.5 and Pb93-Sn3-Ag2-In2 showed poor fatigue life.

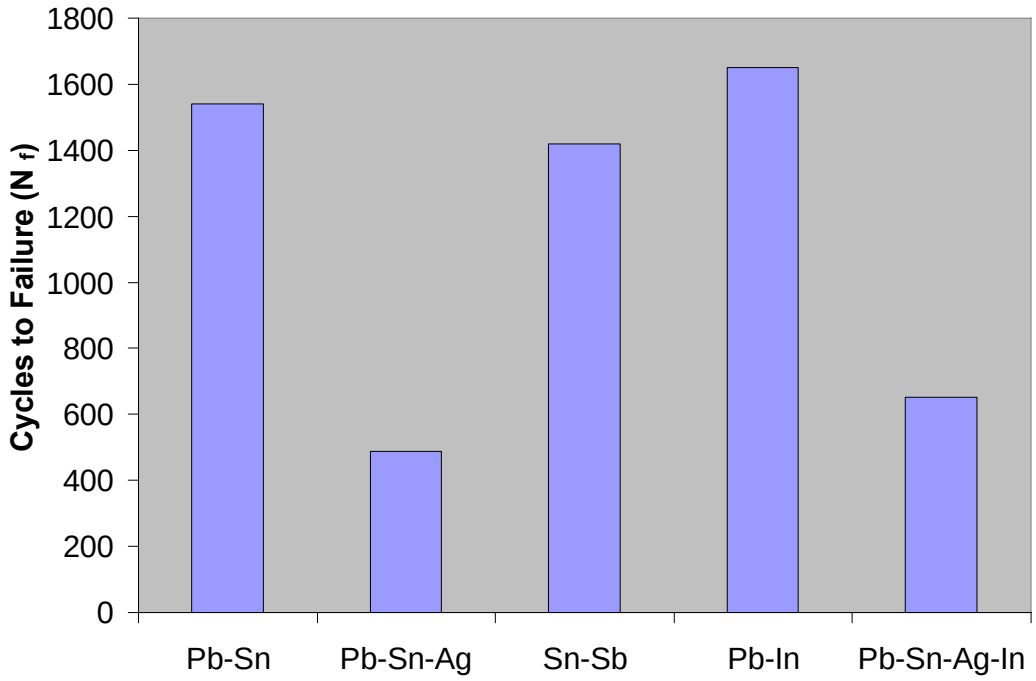


Figure 4.51. Bar chart comparing fatigue life estimations of 95Sn-5Sb, 90Pb-10Sn, 92.5Pb-5Sn-2.5Ag, 95Pb-5In, and 93Pb-3Sn-2Ag-2In using temperature dependent stress-strain data.

Looking back at Engelmaier's equation, total elongation and plastic stain per cycle determine each solder's fatigue life. Total elongation which is proportional to the number of cycles to failure is a material property dependent on composition, microstructure and temperature. Plastic strain calculated from the modeling is a function of each materials constitutive relationship. Since stiffer less compliant materials tend to develop higher stresses during thermal cycling, solders with a lower elastic modulus are desirable. The ideal solder should have a low elastic modulus, and large tensile strength, strain hardening coefficient, and total elongation for the maximum possible fatigue life.

Both Engelmaier's and Kanchanomai's models were implemented to estimate the fatigue life of the passive device solder joints. Inspection of both models revealed total elongation, elastic modulus and tensile strength are the most influential parameters in the fatigue life model. Using only room temperature properties for the initial run, Sn95-Sb5 showed the greatest fatigue life because of its superior mechanical strength at room temperature. Of the Pb-Based solders, Pb95-In5 showed the greatest fatigue resistance because of its large total elongation at room temperature.

4.6 Creep Study

The constitutive relationship for solders is often broken up into three governing equations, describing the elastic behavior, time-independent plastic behavior, and the time-dependent plastic behavior. As result the total strain can be expressed by the following relation:

$$\Delta\varepsilon_{total} = \varepsilon_{elastic} + \varepsilon_{plastic} + \varepsilon_{creep}$$

(11)

where $\varepsilon_{elastic}$ is the elastic strain from Hooke's law, $\varepsilon_{plastic}$ is the time-independent plastic strain defined by Holloman's power law relation, and ε_{creep} is the time-dependent plastic strain often quantified by the power-law or power-law breakdown creep constitutive equations [14]. Thus far we have only considered the first two portions of the constitutive equation namely the elastic behavior and the time-independent plastic behavior. This section will focus on the time-dependent plastic behavior of the five high temperature solders. The specific application of solders exposed to extremely high ambient temperatures for extended periods of time warrants a detailed study of the creep behavior.

Creep is defined as the increase in deformation resulting from a constant applied load. Creep deformation becomes significant when the ambient temperature exceeds 0.5Tm [7]. At high homologous temperatures, the rate of deformation is dominated by competing strain hardening and recovery reactions:

$$\dot{\varepsilon} = \frac{d\sigma / dt}{d\sigma / d\varepsilon} \tag{12}$$

where the numerator is the recovery rate of the material and the denominator is the strain hardening rate [7]. An ideal strain rate results when:

$$d\sigma / dt << d\sigma / d\varepsilon \tag{13}$$

in other words, materials in which the rate of strain hardening is much greater than the rate of recovery have excellent creep resistance.

4.6.1 Parameters Controlling Creep in Visco-Plastic Solders

The rate-controlling mechanism and overall creep behavior of a material is dependent on several material and environmental parameters. A material's crystal structure, grain size, and microstructural constituents all determine how it reacts under constant load. When comparing materials of similar composition, factors like precipitate strengthening and grain size become of greater importance. The morphology, crystal structure, and dispersion of second phase precipitates in the matrix all influence the creep behavior of a material. Likewise, when grain boundary diffusion is significant, grain size becomes an important factor in the overall creep behavior.

In addition to material variables, environment also influences the creep response. As was stated earlier, creep becomes significant as the ambient temperature approaches 0.5Tm. This is because creep is a thermally activated process driven by diffusion. As the diffusion of vacancies increase at higher temperatures, so do the mobility of dislocations throughout the lattice. Creep is also highly dependent on the level of stress. The level of stress determines whether the rate-controlling mechanism is dislocation climb, glide, or grain boundary sliding [7].

4.6.2 Creep Experiment Procedure

All constant-load creep tests were preformed on an MTS 858 tabletop servo-hydraulic tensile testing machine. Figure 4.52a is a picture of the system used in this test. Just as with tensile testing, all creep tests were performed on 3.175 mm diameter solder wire obtained from the Indium Corporation. Strain measurements were acquired via a high temperature 12.7 mm gage length extensometer as seen in Figure 4.52b.

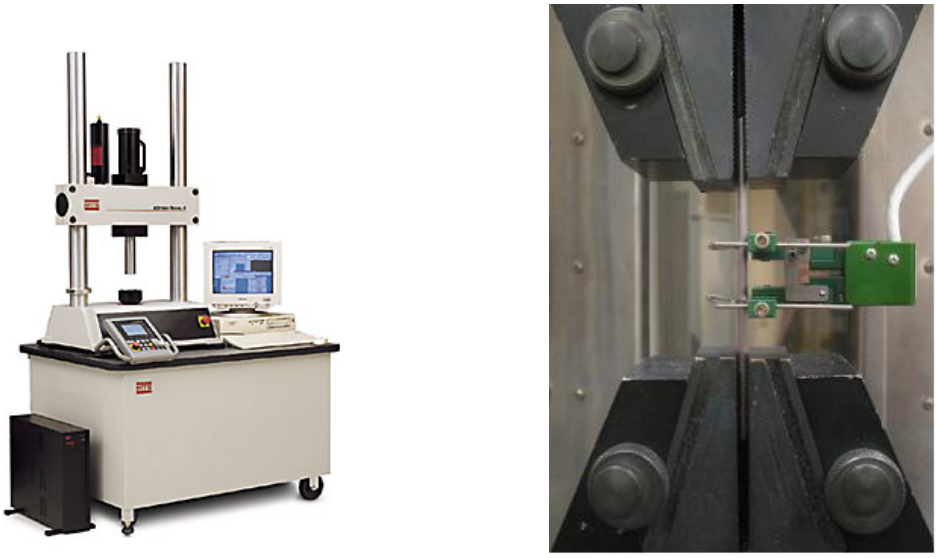


Figure 4.52. (a) Picture of 858 tabletop MTS machine, (b) picture of experimental setup, with wedge grips an extensometer.

Multiple loadings were performed on each sample in order to obtain the stress exponent from a single sample. Samples were loaded from 60N-180N using loading profiles generated using MTS Multi-Purpose Testware (MPT). An example loading profile is shown in Figure 4.53. To minimize creep strains during loading the load was ramped at 20N/sec. Next, the load was held until primary creep effects were eliminated and the steady state creep rate could be calculated. The strain rate is calculated from the time rate derivative of the strain:

$$\frac{d\varepsilon}{dt} = \frac{\varepsilon_2 - \varepsilon_1}{t_2 - t_1} \tag{14}$$

where ε is the strain, and t is time.

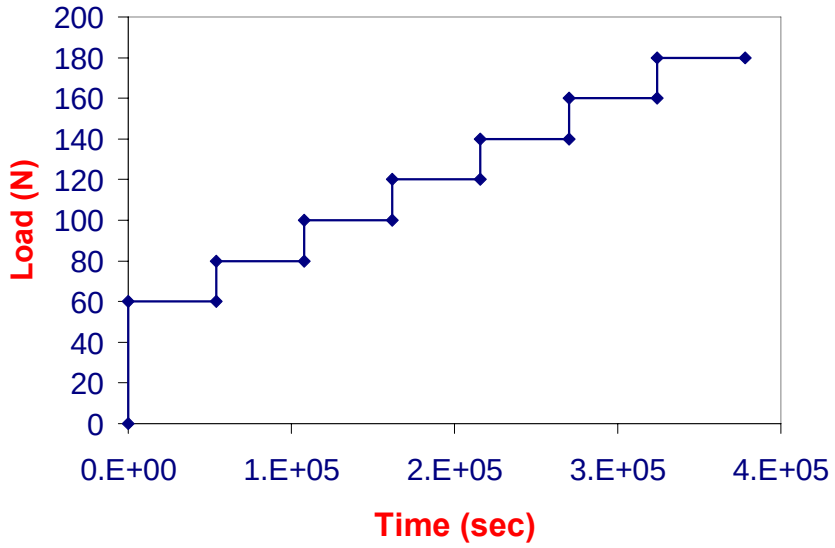


Figure 4.53. Example loading profile for a multiple constant load creep test.

As can be seen in Figure 4.54, the steady-state strain rate is calculated from the strain-rate verses strain diagram. This is the resulting curve of a constant 140N creep test of Pb95-In5. The initial portion of this curve shows the transient creep response of the solder as the creep rate is decreasing with time. Once dε/dt reaches a minimum value or the slope of the curve is approximately zero, steady- state creep has been reached.

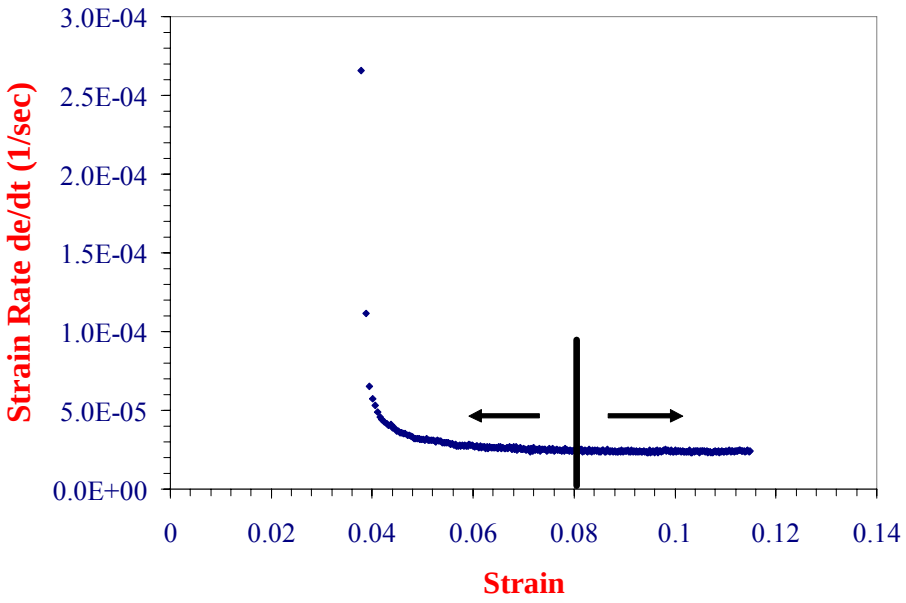


Figure 4.54. Resulting strain rate profile from constant load creep test of Pb95-In5 at 140N.

Figure 4.55 shows the resulting strain rate curves for a multiple constant-load creep test of Pb95-In5. With each loading, Pb95-In5 shows a brief transient period followed by steady state creep. Neglecting slight reductions in cross-sectional area, each step of the test can be considered constant stress. By calculating the steady-state strain rate at each constant stress step, the resulting data can be used to calculate the stress

exponent of the power-law equation. It should be noted that none of these curves show tertiary creep behavior. Tertiary creep is an exponential increase in strain rate after the steady state portion of the curve. Due to micro-void nucleation during tertiary creep, steady-state results of subsequent loadings must be discarded.

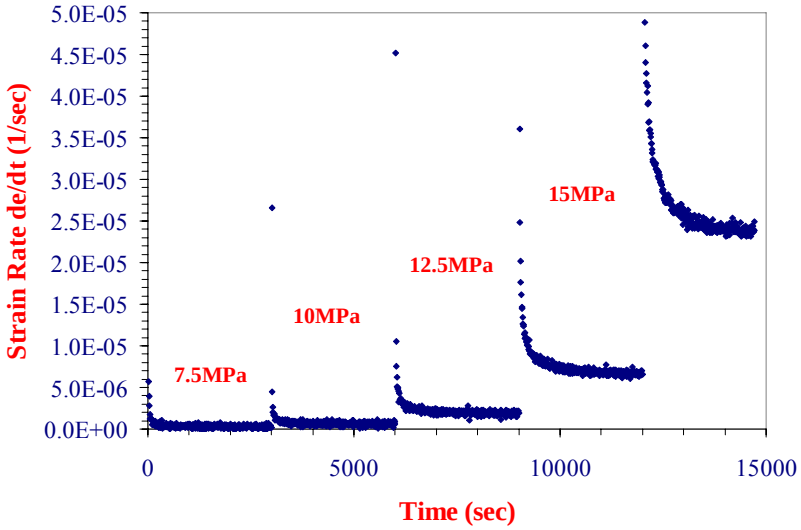


Figure 4.55. Resulting strain rate profile from constant load creep test of Pb95-In5 at 140N.

To validate the use of multiple loading creep tests, the steady-state strain rate was compared to tests in which there was only one loading. Figure 4.56 compares the strain rate of two multiple load creep tests and a single load creep test. Only a negligible difference in the steady state creep rate is observed. This is a significant finding in that multiple loading tests save considerable material and sample preparation costs and allows the calculation of the stress exponent from a single sample rather then a minimum of three samples as with single load creep tests.

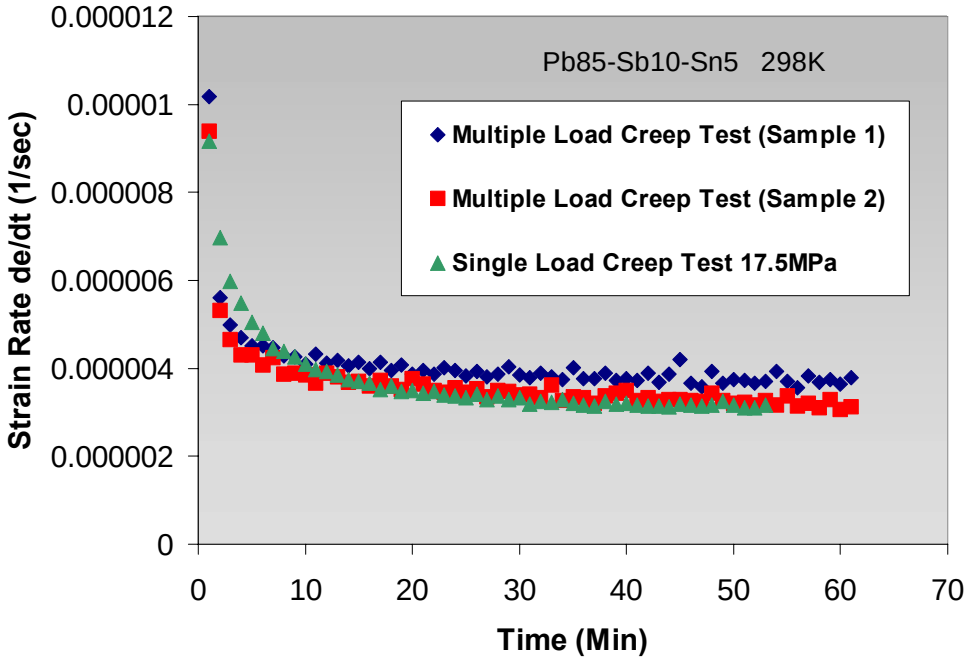


Figure 4.56. Resulting strain rate profile from constant load creep test of Pb95-In5 at 140N.

4.6.3 Room Temperature Creep Results

Time-dependent plasticity contributes greatly to the overall deformation of solder even at room temperature because of its high homologous temperature. Using the techniques outline earlier, each composition was tested from 5MPa to approximately 22.5MPa ranging from low stress application to high stress application such as in the current study. The steady-state strain rate was calculated at each stress, and the stress exponent determined from the log strain rate verses log stress plot. Figure 4.57 shows such a plot for all five compositions at 298K. Each measurement on the plot is the average of three tests. To determine the rate-controlling mechanism, each composition was curve fit to a power-law relation to determine the stress exponent and stress coefficient. The power-law equation combined with an Arrhenius term is shown in equation (5) below:

$$\dot{\varepsilon} = b\sigma^{n} \exp\left(\frac{-Q}{RT}\right) \qquad (15)$$

where b is the stress coefficient, n is the stress exponent, Q is the activation energy, R is the gas constant, and T is temperature in Kelvin [7].

A preliminary estimation of the controlling mechanism is based on the value of the stress exponent. When the stress exponent is 1, creep is controlled exclusively by dislocation climb. Higher stress exponents from 3-8 are thought to be a mix of dislocation climb and dislocation glide. Finally at relatively higher stresses, when the stress exponent is greater than 8, the power-law relationship breaks down and creep is solely controlled by dislocation glide.

According to Figure 4.57, the stress exponent for most compositions falls between 3 and 8, indicating creep is controlled by dislocation glide aided by vacancy diffusion. However both Pb92.5-Sn5-Ag2.5 and Pb93-Sn3-Ag2-In2 show power-law breakdown behavior with stress exponents exceeding 8. Pb93-Sn3-Ag2-In2 in particular shows a lower stress exponent of 4.5 at lower stresses (10-15MPa) however at higher stresses (15-20MPa) the stress exponent increases to 8.8.

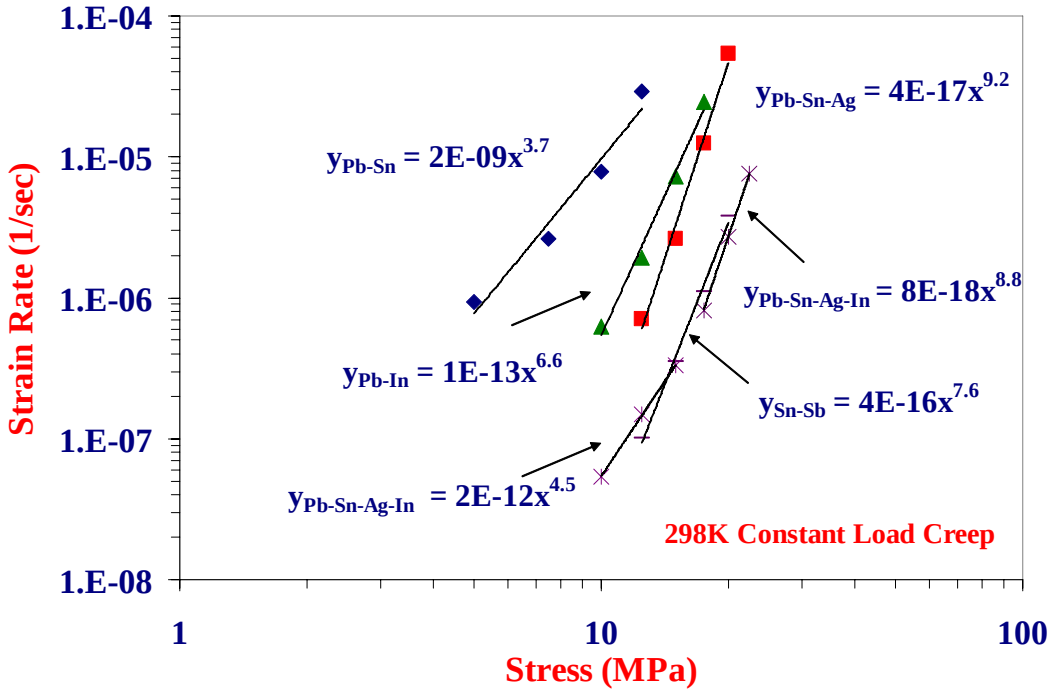


Figure 4.57. Resulting strain rate profile from constant load creep test of Pb95-In5 at 140N.

To make a relative comparison of the creep resistance of different compositions, the steady state strain rate was compared at 12.5MPa. Figure 4.58 shows the steady state strain rate for each composition tested at room temperature. It's obvious from the chart, Pb90-Sn10 shows the poorest creep resistance at room temperature, followed by Pb95-In5. Compositionally these samples are very similar Pb-rich solders however from a microstructure standpoint they are quite different. As has been discussed earlier Pb90-Sn10 is a two phase alloy with a Pb-rich matrix with a Sn-rich oval second phase dispersed throughout the microstructure. Pb95-In5 on the other hand, is a single phase solid solution. Based on these observations one would think Pb90-Sn10 would have a greater creep resistance because of the Sn-rich second phase, however this is not the case. Looking further into the microstructure, there is a large disparity in the grain size of the two alloys. Similar to the other Pb-rich solders, Pb90-Sn10 has rather small grains measuring anywhere from 5-10 um. Pb95-In5 on the other hand has much larger grains measuring from 25-50um. This suggests perhaps grain boundary diffusion is the rate controlling mechanism for theses alloys since creep resistance is proportional to grain size. The remaining three compositions namely Pb92.5-Sn5-Ag2.5, Pb93-Sn3-Ag2-In2, and Sn95-Sb5 all contain hard IMC dispersed throughout the matrix. Precipitates greatly

enhance the creep resistance through precipitate hardening during slip since dislocation glide was found to be the rate-controlling mechanism for these alloys.

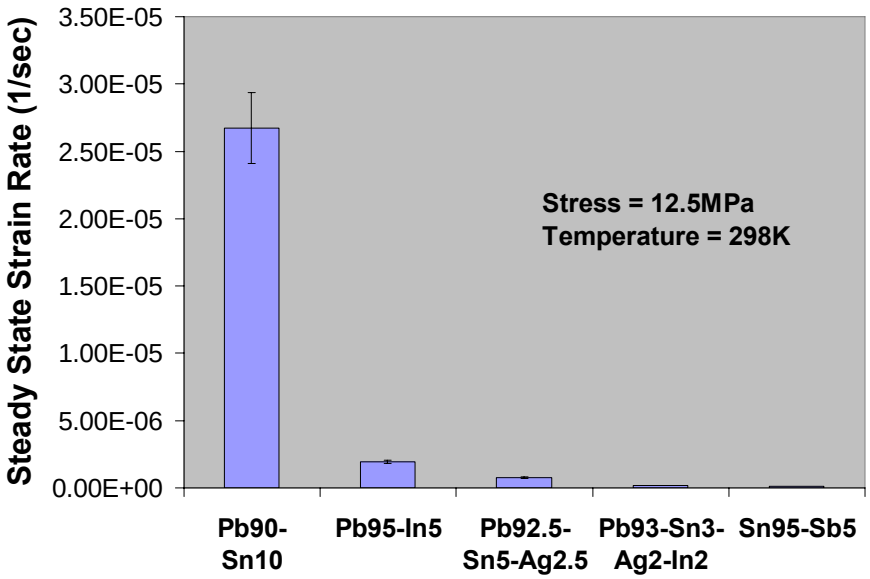


Figure 4.58. Resulting strain rate profile from constant load creep test of Pb95-In5 at 140N.

Conclusions

In this program, the mechanical behavior of five high temperature solders were characterized though tensile testing and nanoindentation. In an effort to reduce the influence of time-dependent deformation on the tensile test results, each solder was pulled at several strain rates. A strain rate of 5%/sec was selected because it eliminated the most time-dependent deformation. Comparison of the strain rate sensitivity exponent for Sn95-Sb5, Pb90-Sn10, and Pb92.5-Sn5-Ag2.5 showed Sn95-Sb5 to have the greatest strain rate sensitivity at room temperature; however the exponent was relatively small for all three solders. Room temperature tensile testing revealed Sn95-Sb5 to have superior mechanical strength compared to the Pb-based solders. Of the Pb-based solders Pb93-Sn3-Ag2-In2 had the largest tensile strength, and Pb95-In5 showed the weakest. At 200°C there was a drastic change in the mechanical strength of the solders. Sn95-Sb5 no longer showed the greatest strength because of its phase change at 180°C and higher homologous temperature. Pb90-Sn10, on the other hand, showed the greatest strength of all the solders tested at 200°C.

Both Engelmaier's and Kanchanomai's model were implemented to estimate the fatigue life of the passive device solder joints. Inspection of both models revealed total elongation, elastic modulus and tensile strength are the most influential parameters in the fatigue life model. Using only room temperature properties for the initial run, Sn95-Sb5 showed the greatest fatigue life because of its superior mechanical strength at room temperature. Of the Pb-Based solders, Pb95-In5 showed the greatest fatigue resistance because of its large total elongation at room temperature.

The fourth quarter's effort concentrated on measuring the time-dependent plasticity of each solder. Room temperature results of the stress exponents showed dislocation climb

to be the rate controlling creep mechanism for most of the solder, however Pb92.5-Sn5-Ag2.5 and Pb93-Sn3-Ag2-In2 did show breakdown in the power-law behavior where creep is controlled by dislocation glide. A comparison of the steady state strain rate at 12.5 MPa showed Pb93-Sn3-Ag2-In2 and Sn95-Sb5 to have the greatest creep resistance at room temperature.

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Chapter 5 Solder Validation

5.1 Process Development for Solder Reflow

Five solders ranging from high Sn to high Pb content were selected based on the melting points, such that $T_{solidus}$ > 250°C. Two different surface finishes, Ni/Au and Ni/Pd/Au, are being used to evaluate reliability of each of the solder alloys. Au thickness of < 0.5 μm has been used to prevent Au embrittlement due to formation of $AuSn_4$ [1]. Pd has a lower dissolution rate than Au in Sn and also Pb based alloys. Therefore, Pd in NiPdAu surface finish is known to retard kinetics of intermetallic formation, making it a good surface finish for high temperature applications [2]. Solder pastes were time dispensed on 5 mm X 5 mm squares of wafers with Ni/Au and Ni/Pd/Au stack up and reflowed in N_2 atmosphere in a BTU oven. The oven consists of eight zones wherein temperature was initially profiled using a KIC temperature profiler. The effect of belt speed on temperature profile was studied for 90Pb-10Sn solder (Indalloy 159) as shown in Figure 5.1. Based on this, belt speed of 15 inch/min was chosen for all the solder pastes. The reflow profiles for all five solder pastes are shown in Figure 5.2. 90Pb-10Sn (Indalloy 159) and 92.5Pb-5Sn-2.5Ag (Indalloy 151) have melting points of 302°C and 296°C; therefore same profile was used to reflow both solders. 95Sn-5Sb (Indalloy 133) was reflowed with a peak reflow temperature of 298°C. 95Pb-5In (Indalloy 11) and 93Pb-3In-2Sn-2Ag (Indalloy 237) were reflowed using the same profiles, as their melting points are 313°C and 304°C respectively.

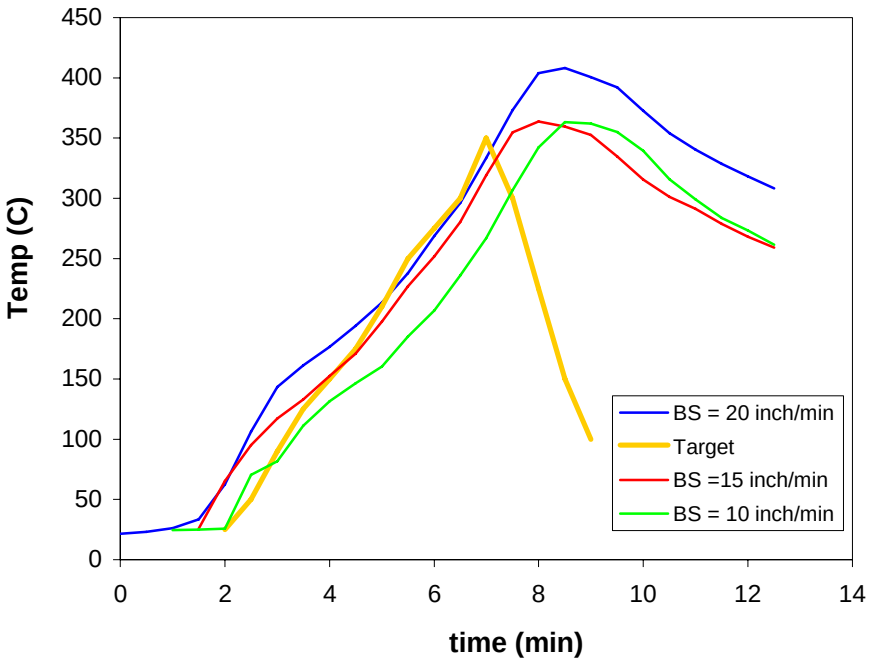


Figure 5.1. Effect of belt speed on reflow profile.

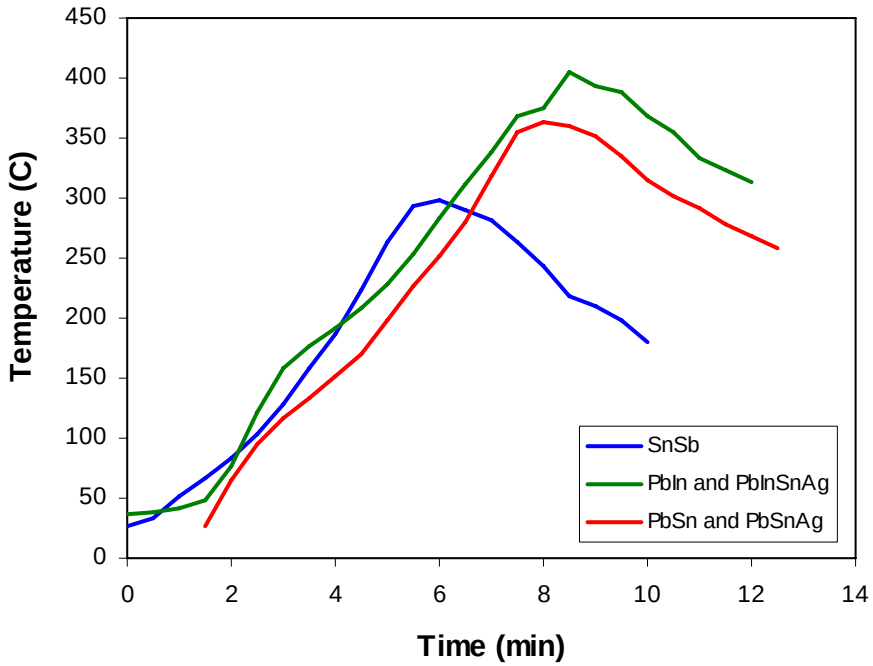


Figure 5.2. Reflow profiles for all five solder pastes.

Four samples of each type were tested and the average shear strength values are shown in Figure 5.3. After reflow, the shear strength of solders was tested using the Dage shear tester with a 20 kg load cell. All failures under as reflowed conditions were in the bulk of the solder indicating high interfacial strength between the solder and surface finish on the substrate. 95Sn-5Sb and 95Pb-5In show highest shear strength values while 90Pb-10Sn shows lowest strength. It is very well known [3] that Au which is an oxidation barrier, dissolves in solder during reflow and Ni based intermetallics are formed at the solder/surface finish interface to facilitate bonding. High lead solders have lower strength values, therefore 90Pb-10Sn and 92.5Pb-5Sn-2.5Ag solders show low shear load values upon reflow on both surface finishes. However, the addition of In to Pb and Pb-Sn-Ag alloy leads to formation of $AuIn_2$ phase upon reflow with Ni/Au and Ni/Pd/Au surface finish, thereby increasing the strength of those solders.

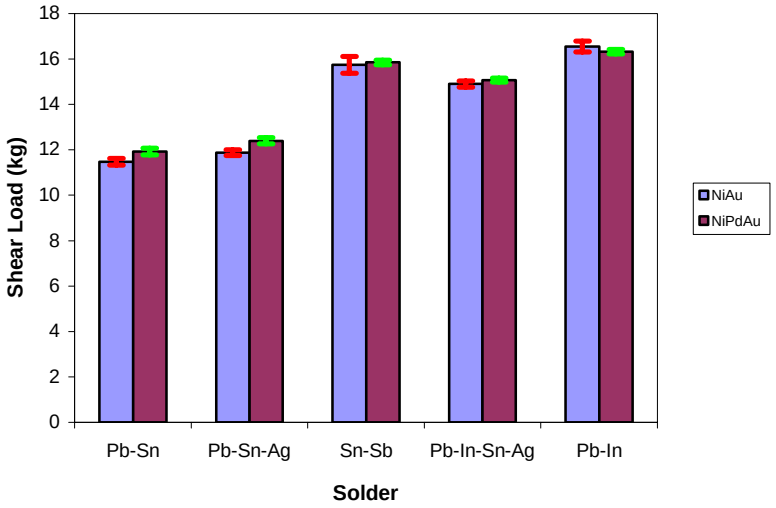


Figure 5.3. Comparison of shear strength of solders under as-reflowed conditions for two different surface finishes.

5.2 Surface Finish Development

High temperature storage tests were conducted on all solders for the two types of surface finishes, NiAu and NiPdAu. The specimens were tested at 250°C for up to 1000 hrs to test the effect of high temperature storage on die shear strength and intermetallics formed over time. Figure 5.4 and Figure 5.5 show the die shear loads for 5 mm X 5 mm samples with NiAu and NiPdAu surface finishes respectively. All solders show higher shear strength on NiPdAu surface finish. 90Pb-10Sn solder shows maximum drop in shear strength on NiAu surface finish. Pb93-Sn3-Ag2-In2 shows minimal decrease in shear strength on both surface finishes.

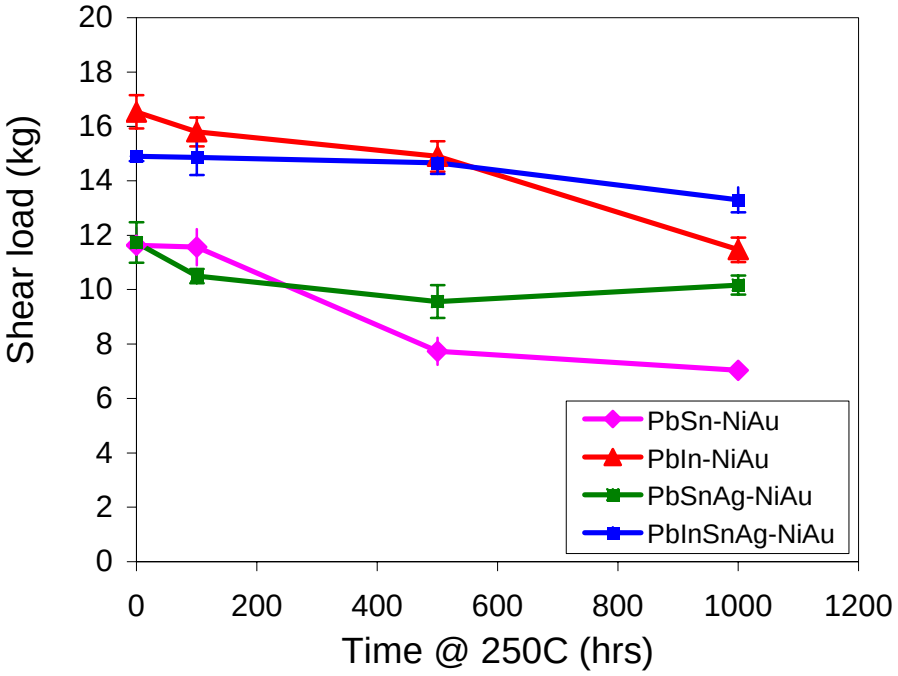


Figure 5.4. Shear strength of four different high temperature solders on a Ni-Au surface finish after high temperature storage at 250°C.

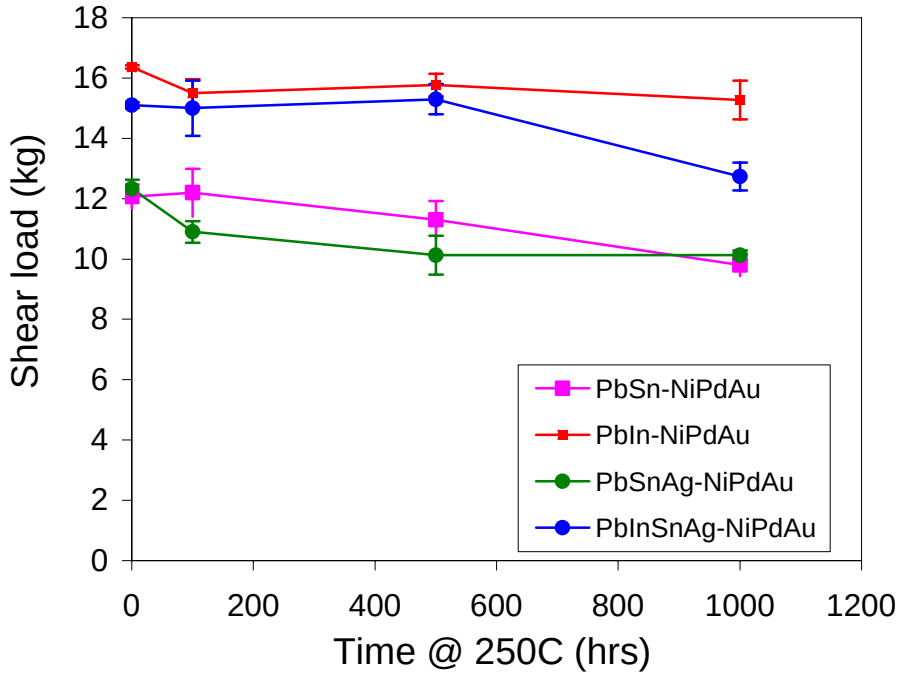


Figure 5.5. Shear strength of four different high temperature solders on a Ni-Pd-Au surface finish after high temperature storage at 250°C.

5.3 Resistor Test Coupon Assembly

In order to test the reliability of each of the high temperature solders, a test coupon of Kapton E, 1 mil flex with 30 daisy chained 0 ohm resistors was designed. For each of the

solders, two different resistor types (0805 and 2512) were assembled in order to determine reliability as a function of component size. Sn95-Sb5 was not a part of this experiment because temperature cycling would go beyond the melting temperature of the solder. Failure of the solder joint is defined as a rise of resistance in the daisy chain or an open circuit.

The assembly of the resistors was performed using paste form of each of the solders (in contrast to the tensile testing which used wire forms of the solders). The solder was auto-dispensed on the flex coupon and the resistors were pick-and-placed onto the solder. A special carrier for the flex coupon was designed in order to provide rigid backing during the assembly process and keep the flex from rolling up during the reflow process. The coupons were then reflowed using the reflow profiles reported in a prior section. Figures 5.6-5.11 show example solder joints formed using this process.

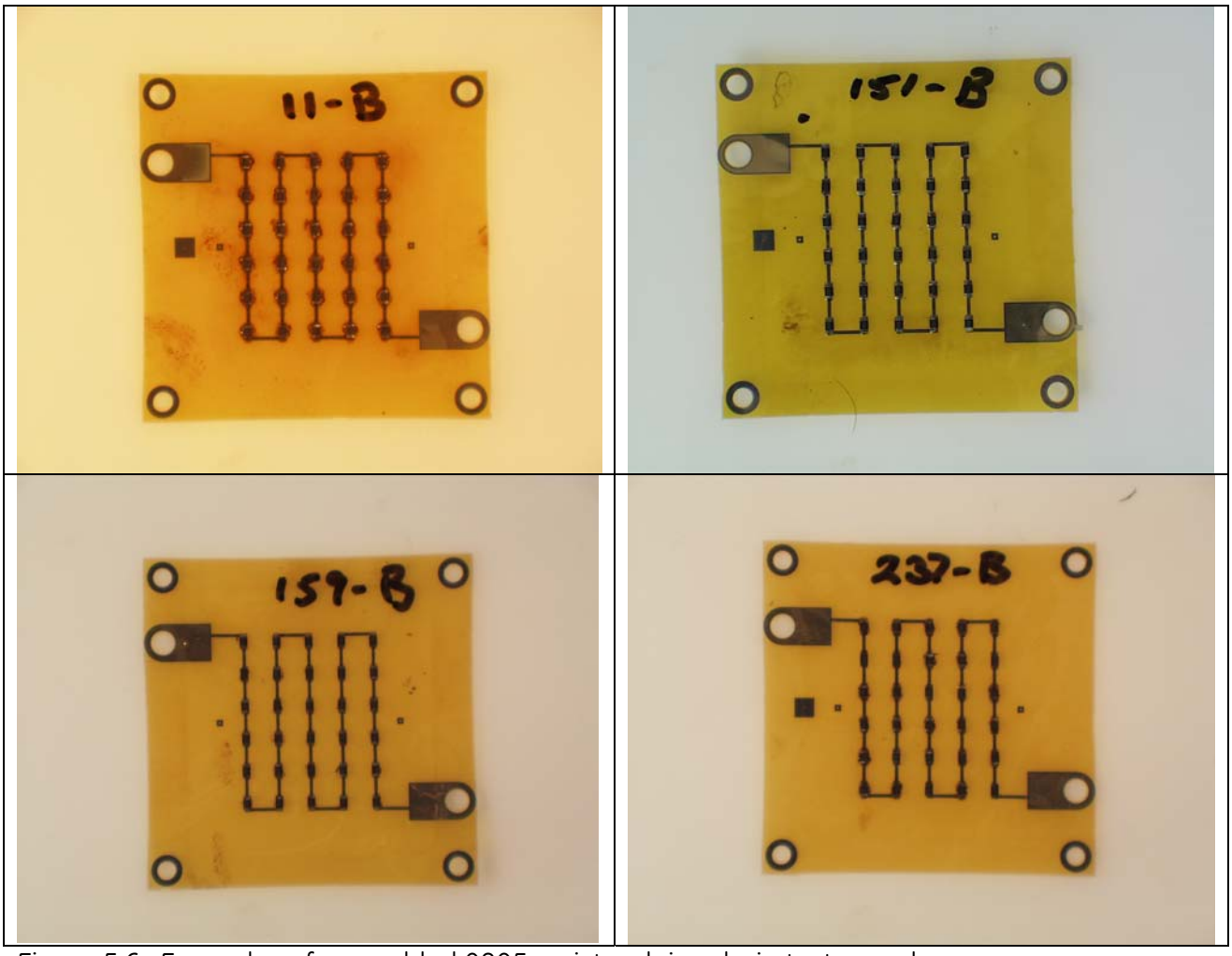


Figure 5.6. Examples of assembled 0805 resistor daisy chain test samples.

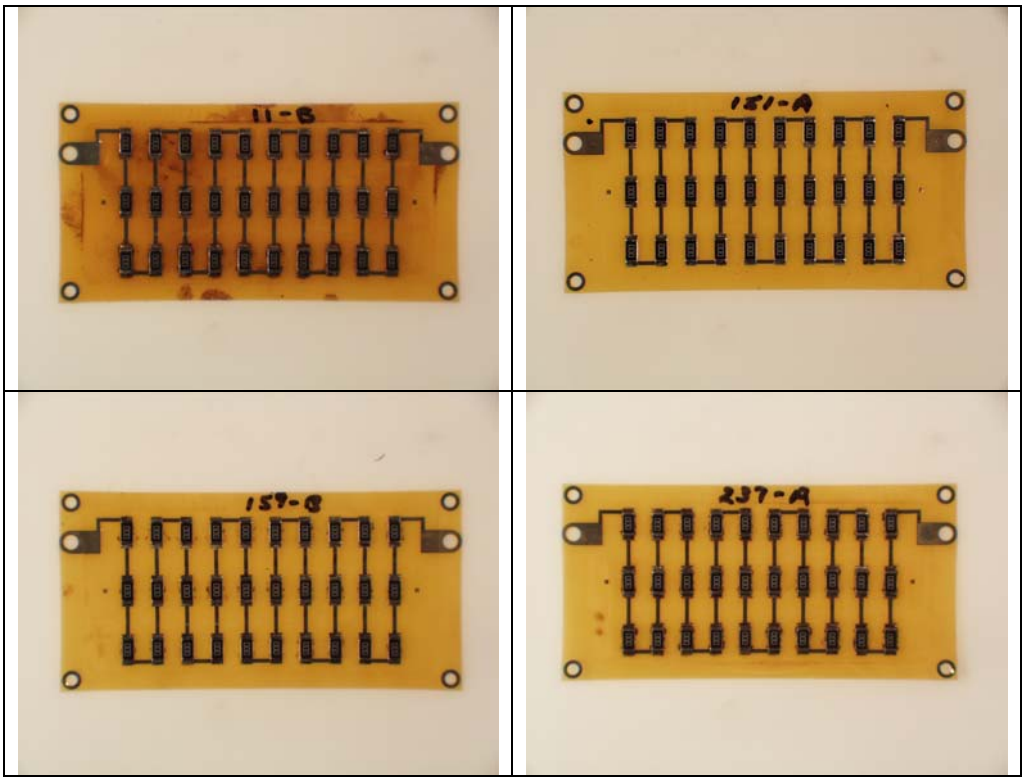


Figure 5.7. Examples of assembled 2512 resistor daisy chain test samples.

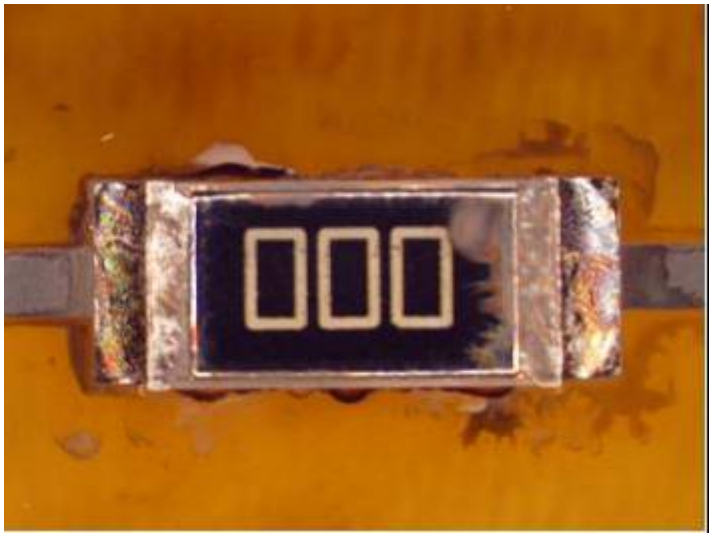


Figure 5.8. 2512 resistor assembled on flex using Pb95-In5 solder paste.

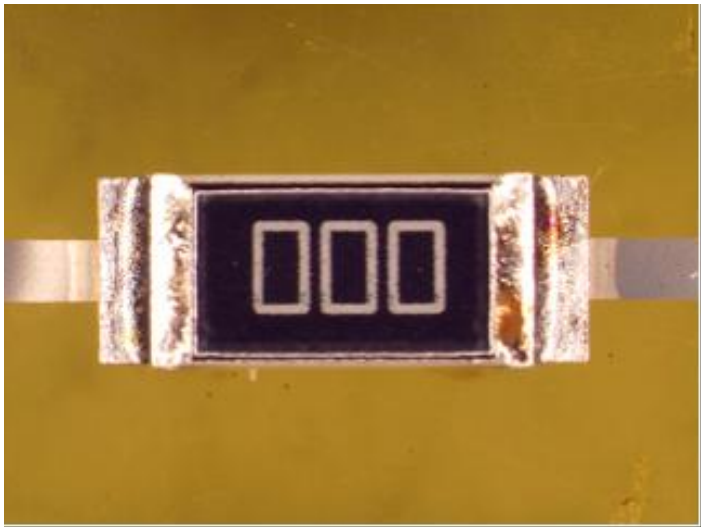


Figure 5.9. 2512 resistor assembled on flex using Pb92.5-Sn5-Ag2.5 solder paste.

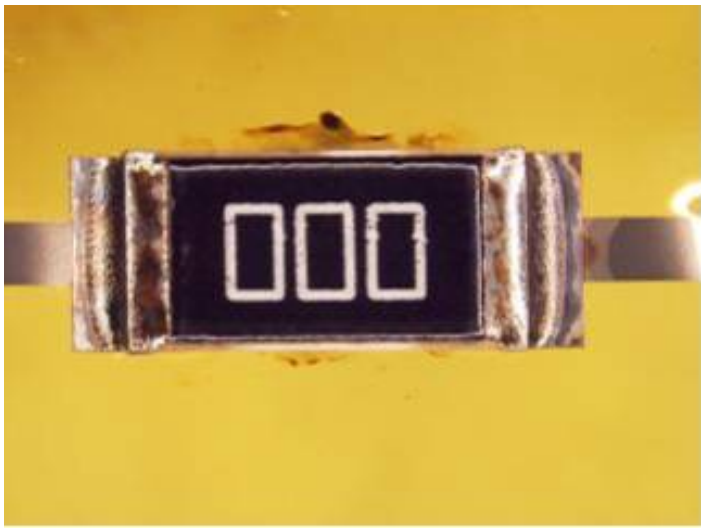


Figure 5.10. 2512 resistor assembled on flex using Pb90-Sn10 solder paste.

Figure 5.11. 2512 resistor assembled on flex using Pb93-Sn3-Ag2-In2 solder paste.

Visual inspection was performed after soldering. The solder surface of all the solders appeared grainy to varied degrees with the Pb90-Sn10 having the smoothest finish.

Solder beads formed on the Pb95-In5 and Pb93-Sn3-Ag2-In2 is an indication of the need for further tuning of the solder reflow profile. These typically are removed during a post solder cleaning process.

5.4 Reliability Testing of Resistor Test Coupons

The daisy chains are continuously monitored consistent with IPC-9701A (Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments). A profile of 7 cycles is shown in Figure 5.12. A Blue-M Ultra Temp Inert oven is used for temperature cycling between 35 and 250°C with a dwell time of 15 minutes at each extreme and a nitrogen ambient atmosphere. The daisy chain resistance is monitored using an Agilent 35970A data acquisition/switch unit with 34901A and 34908A multiplexers. The 35970A is scanned using a Labview application every 60 seconds and logs the oven temperature and daisy chain resistances. The connection between the daisy chains and the data acquisition unit is through glass insulated, 20 AWG nickel wire with AMP Strato-Therm terminals, which make contact to pads on the flex circuits using #4-40 screws and lock washers. The flex are mounted onto PEEK substrates drilled and tapped with #4-40 mounting holes to accommodate the flex test circuits. The solder joints were continuously monitored for resistance and inspected at room temperature after intervals of 50 cycles typically. The failed solder joints were recorded and repaired using the same solder alloy as originally soldered before placing back into the chamber to continue cycling. Reliability distribution analysis was performed using an interval censoring approach.

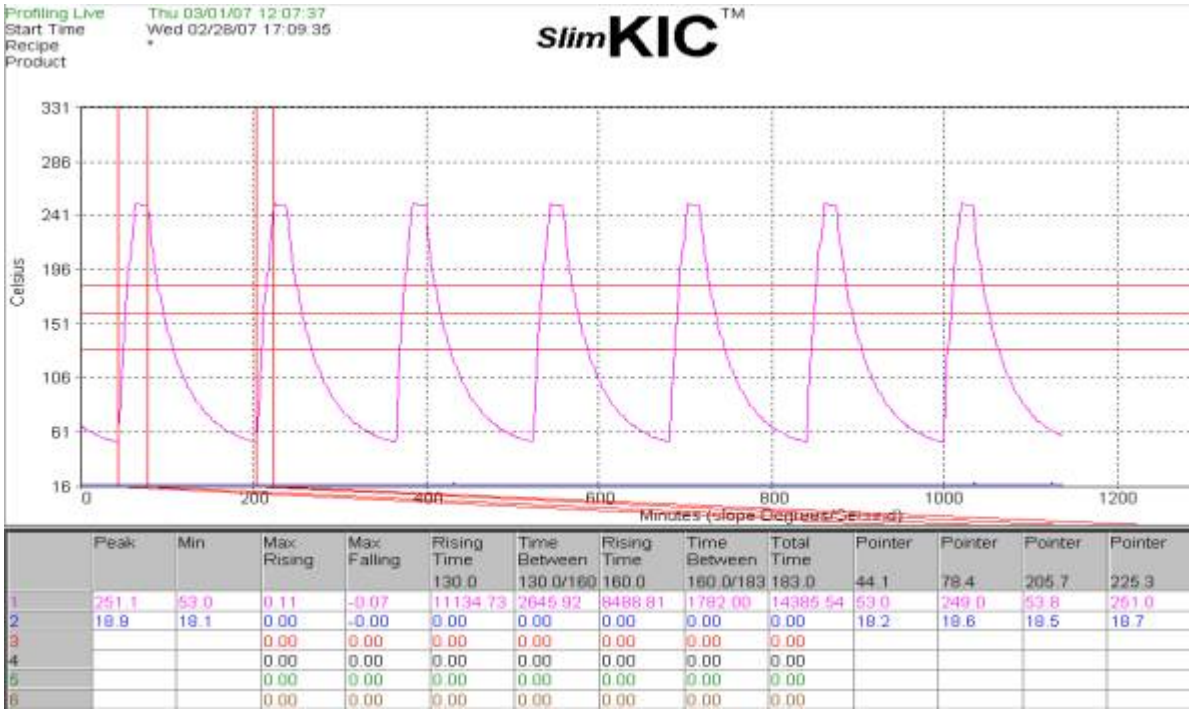


Figure 5.12. Temperature cycling profile (35 to 250°C).

The results of the solder joint failures were analyzed after 277 cycles. The 92.5Pb-5Sn-2.5Ag solder samples had no failures at the time. One failure was detected on a pad that lifted from the laminate but the solder joint remained sound. More failures occurred on 0805 components than the 2512 components. The rank of solders from longest life to

shortest is: 92.5Pb-5Sn-2.5Ag, 93Pb-3Sn-2Ag-2In, 95Pb-5In, and 90Pb-10Sn. The pooled failure results by solder alloy were found to fit a two-parameter Weibull distribution shown in Figure 5.15. The Weibull distribution parameters are listed in Table 5.1. The 92.5Pb-5Sn-2.5Ag data could not be analyzed since it had no solder joint failures. Ranking of the solders by characteristic life is: 92.5Pb-5Sn-2.5Ag, 95Pb-5In, 90Pb-10Sn, and 93Pb-3Sn-2Ag-2In. 93Pb-3Sn-2Ag-2In has a higher beta than the other two alloys and could have a higher failure rate. The distribution analysis was performed on only four samples, more intervals would be needed to make a solid conclusion. What is clear is that the 92.5Pb-5Sn-2.5Ag out performs the other three alloys. A principle cause of solder joint failure occurs where the flex wrinkles due to exposure to soldering temperatures and during temperature cycling. An example of this is shown in Figure 5.16. Laminating the flex to a stiffener with an adhesive, such as Staystik, may reduce this occurrence. The difference between the modeling results and the experimental results are attributed to non-planar stresses that occur during testing.

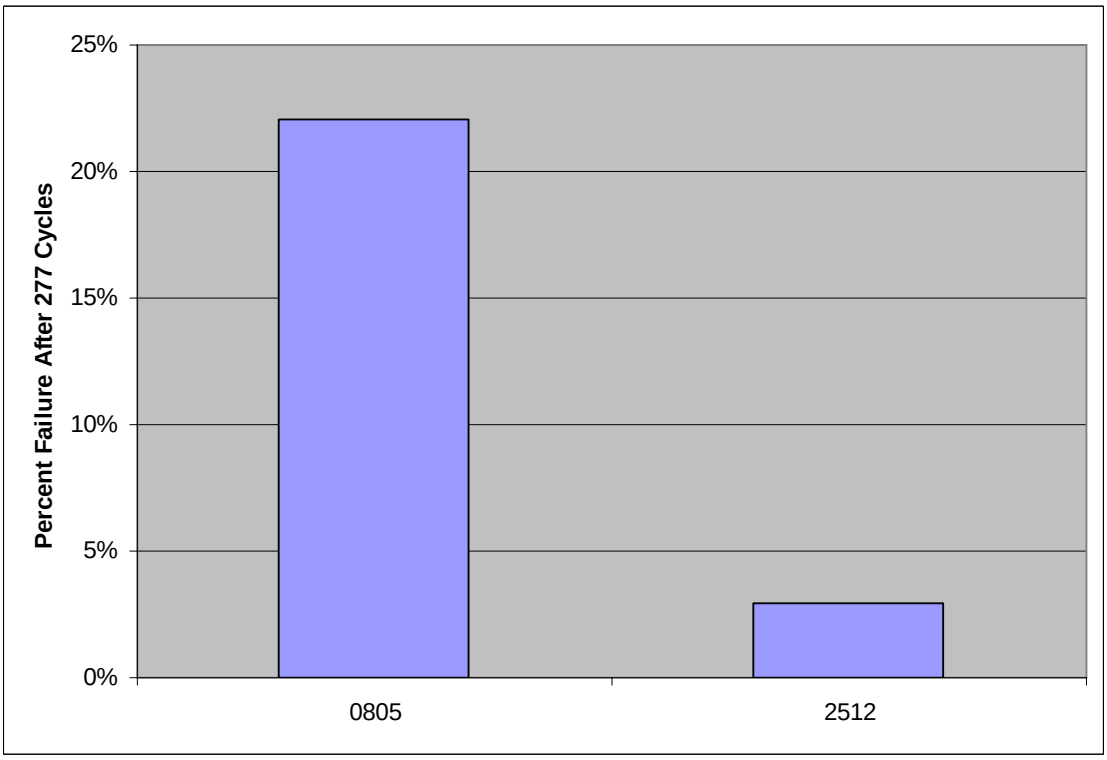


Figure 5.13. Comparison of failures by resistor package size.

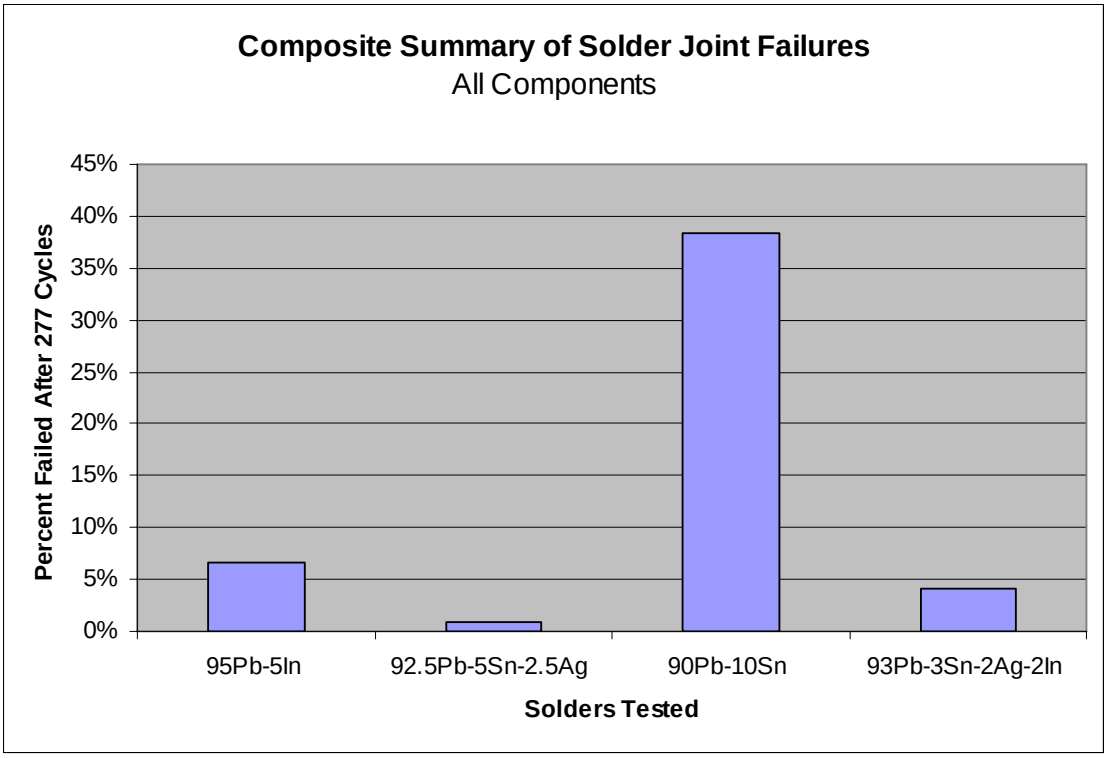


Figure 5.14. Comparison of failures by solder alloy.

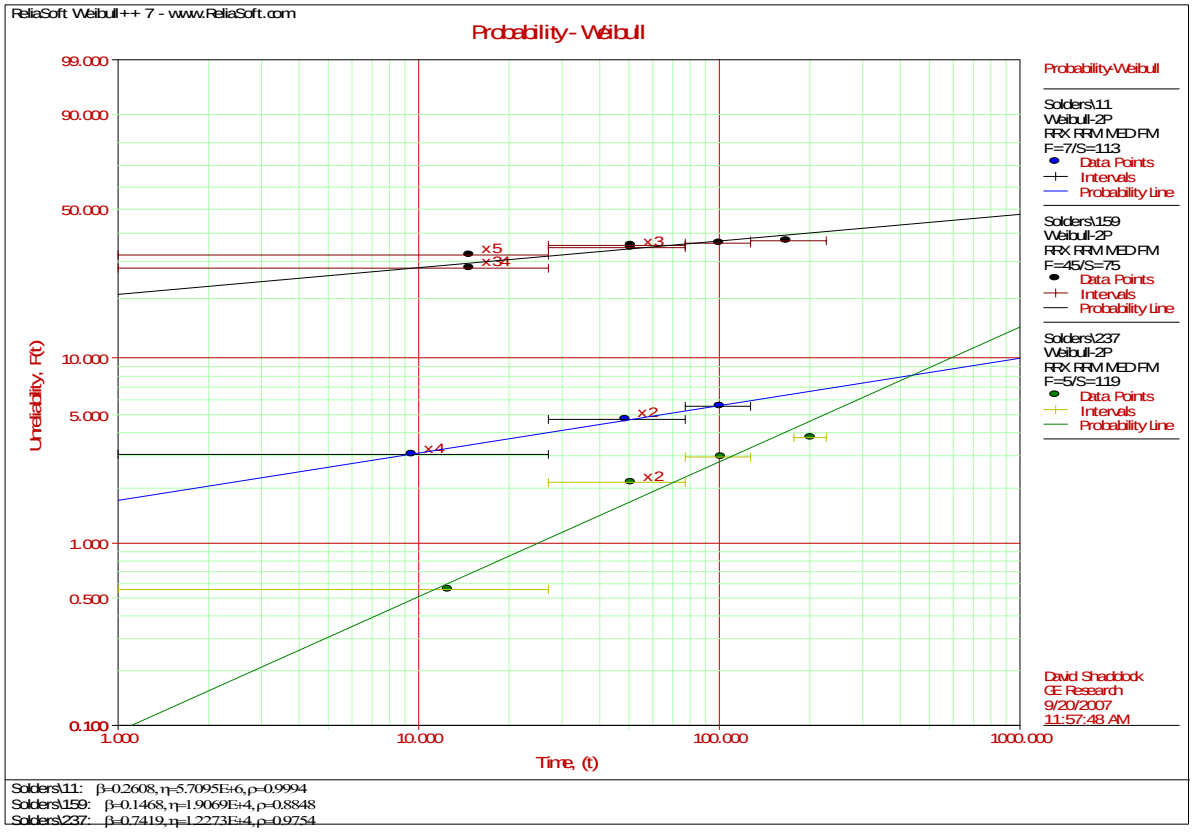


Figure 5.15. Distribution plot of failed solder joints.

Table 5.1 Distribution parameters of failed solder joints.

Solder Alloy	Mean	Beta
95Pb-5In (Indalloy 11)	5709500	0.2608
90Pb-10In (Indalloy 159)	19069	0.1468
93Pb-3Sn-2Ag-2In (Indalloy 237)	12273	0.7419

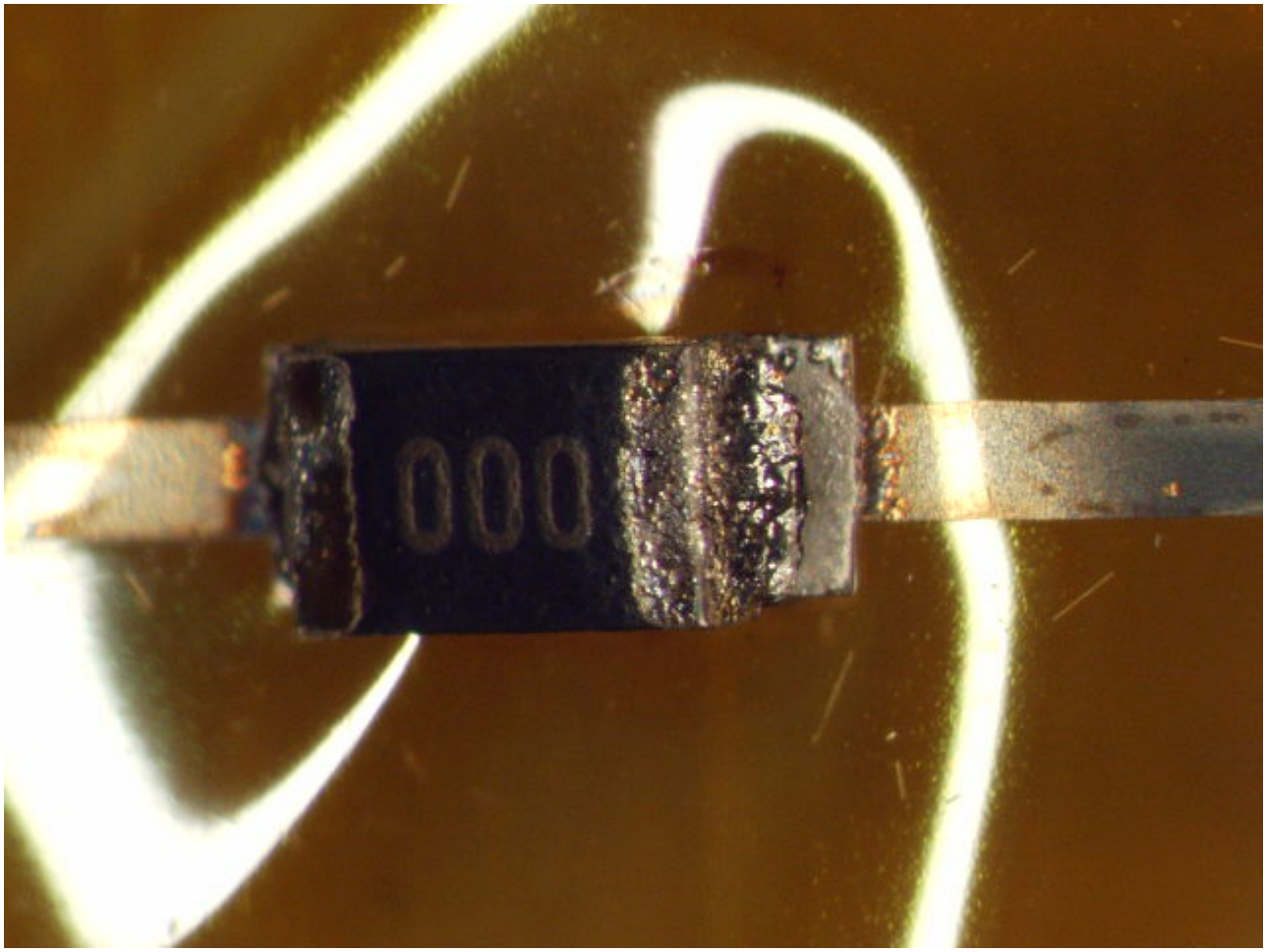


Figure 5.16. Example of failure: 0805, 90Pb10Sn resistor.

References

1. Peng W., et al., "Microstructural and performance implications of gold in Sn-Ag-Cu-Sb interconnections", 2003 ECTC, pp. 809-815.
2. Coyle R. J., et al., "The effect of modifications to the nickel/gold surface finish on the assembly quality and attachment reliability of a PBGA", 2003 IEEE Transactions in CPMT, vol. 26, no. 4, pp. 724-32.
3. Shiau L. C., "Reactions between Sn-Ag-Cu lead-free solders and the Au/Ni surface finish in advanced electronic packages", *Soldering and Surface Mount Tech.*, 2002, vol. 14, no. 3, pp. 25-29.

Chapter 6. Active Interconnect Development

6.1 Active Interconnect Overview

A systematic analysis of the stress in interconnects due to CTE mismatch between die and substrate as a function of aspect ratio of interconnects has been conducted for active component interconnects. Figure 6.1 shows a plot of maximum Von Mises stress in Au stud bump as a function of the height for 150 μm pitch and 2 mm X 2 mm die. These specifications for the die size and pitch are typical of high temperature instrument amplifiers such as those sold by Haric. Figure 6.2 shows some snapshots of stress-distributions in Au interconnect for different aspect ratios (AR) when assembly is cooled from 250°C to RT. As can be seen from these snapshots, the maximum stress concentration is at the pad/die interface. The maximum Von Mises stress in interconnect decreases from 265 MPa for AR = 2/3 (closer to Au stud bump) to 186 MPa for AR = 3/2 (closer to pillar bump).

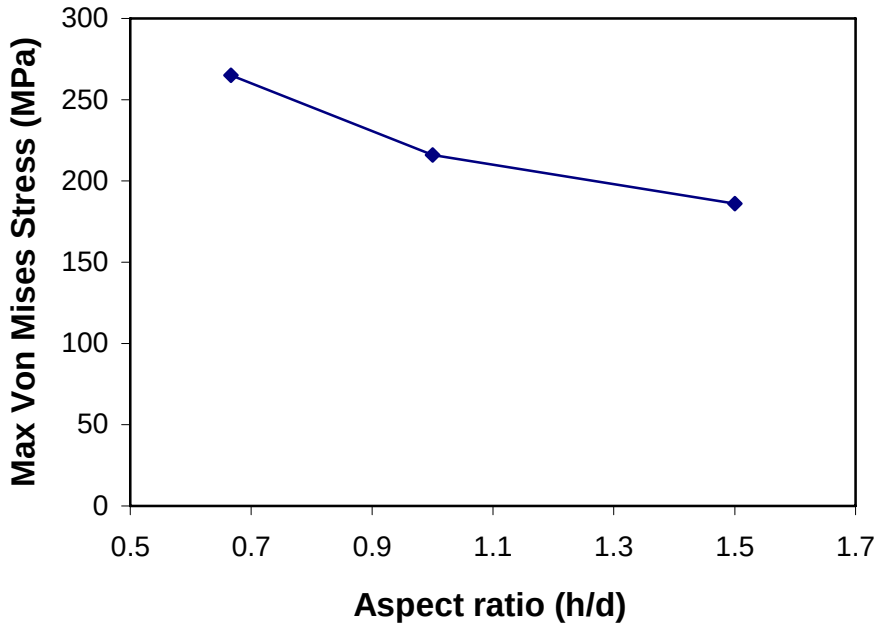
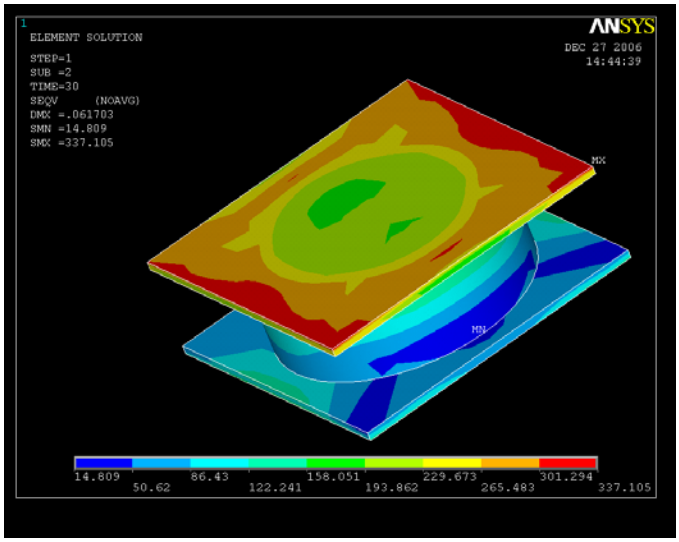
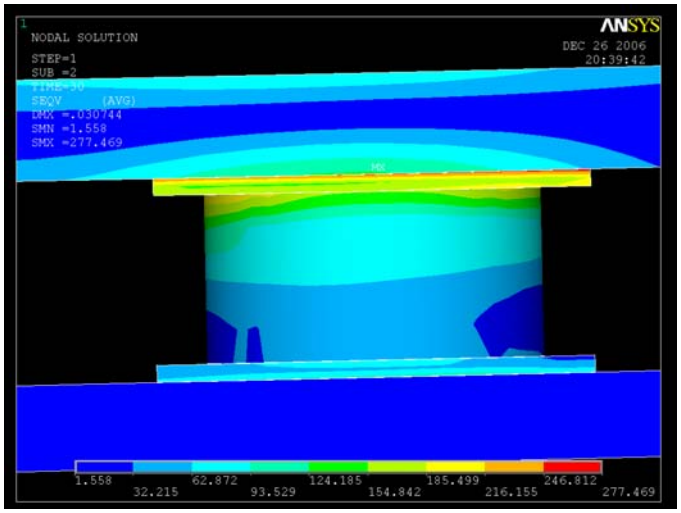


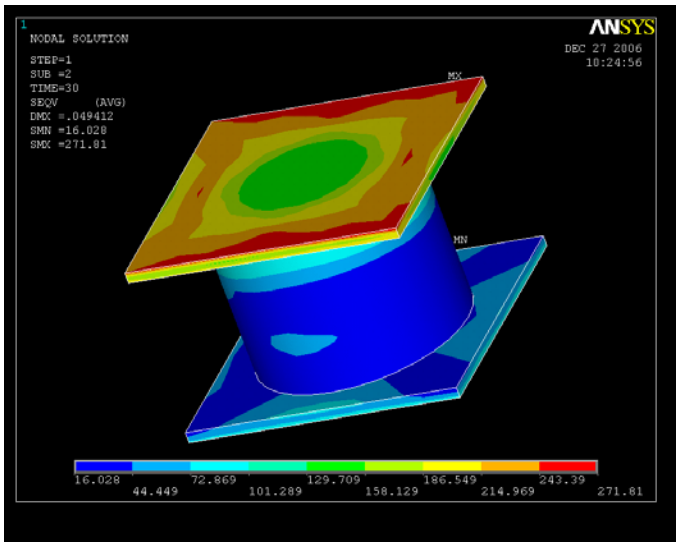
Figure 6.1. Maximum Von Mises stress in Au bump as a function of aspect ratio when assembly is cooled from 250°C to 20°C.



h/d = 2/3



h/d = 1



h/d = 3/2

Figure 6.2. Stress distribution in Au interconnections for different aspect ratios.

It is evident that as standoff height of interconnect is increased, the structure becomes more compliant and reliability without underfill can be ensured. Based on this analysis, different interconnect techniques ranging from Au-stud bump (aspect ratio < 1) to wire

bond (aspect ratio > 1) were chosen to be evaluated as a part of this study. Following techniques are candidates for chip assembly:

1. *Au stud bumping:* Gold bumps are created and coined using a modified wirebonding approach on chip side. The joint between the die and the substrate is created by using thermosonic or thermocompression bonding. For 150 μm pitch and 100 μm pad size, typical height of stud bump would be 70 μm. Maximum assembly temperature is 150°C in case of thermosonic and 250°C for thermocompression bonding. Temperature cycling and vibration will be the two critical tests to assess reliability of Au stud bumps. A standard 2.5 mm X 2.5 mm die with daisy chain will be used for reliability testing. The layout of the die is shown in Figure 6.3. This method can be evaluated using temperature cycling from 35°C to 200°C and failure will be defined per IPC and SAE standards. UBM on die side will be Ti (W)/Au and surface finish on substrate side will be Ni/Au and Ni/Pd/Au.

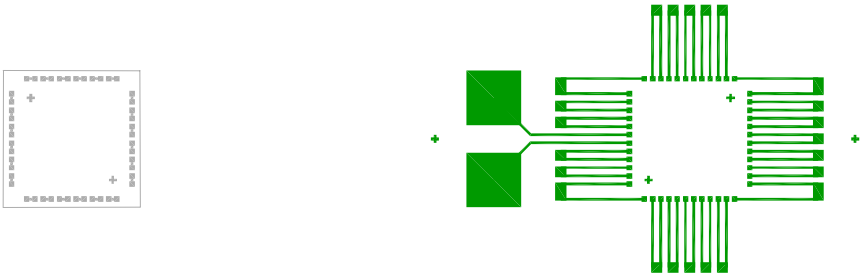


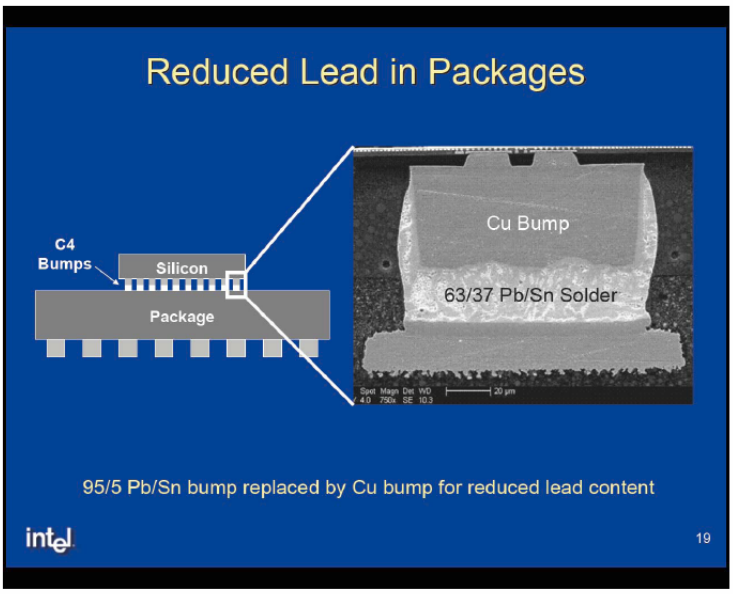
Figure 6.3. Layout for die and substrate designs to be used for testing different interconnection techniques.

2. *Au-In low temperature bond:* Hard solders are usually low melting point Au alloys that have high strengths. The most commonly used hard solders include Au-Sn, Au-Ge, and Au-Si eutectic alloys. They all have high thermal conductivity and free from thermal fatigue because of the high strength, which results in elastic rather than plastic deformation. They are also not as susceptible to fatigue or rupture during thermal cycling as soft solders. A drawback would be that these interconnect will break the active device during operation due to its high strength. In contrast to the rare use of Au-In alloys, indium has been widely used as a soft solder for bonding delicate devices, which need a low process temperature (157°C). Indium has been recognized for its excellent adhesive properties to metals as well as nonmetals. Adhesion at the interface is at least as great as the bulk strength of indium [1]. Use of indium is appropriate when plastic deformation of the bonding layer is required to absorb the induced stress [2]. Indium has also been used to bond gold-coated glass, forming an In-rich Au-In alloy that has good sealing properties. Microsoldering using Au-In-Au layers for the purpose of making electrical contacts has been demonstrated with excellent bond strength [3].

3. *Wire/ Ribbon bond:* Au wire and ribbon bonds is another approach for interconnection to active devices. This will require a high temperature adhesive such as polyimide or LCP for die attach. The compliant structure would accommodate the stresses due to CTE mismatch. Studies have shown that wirebonding is robust to the temperatures of interest in this application [4]. However, the primary disadvantage of this strategy is the use of adhesive for chip attach which may add additional risk [5]. Another

approach would be ribbon bonding which has demonstrated higher reliability and high frequency performance [6].

4. *Au or Ni column with solder:* A new interconnection approach under consideration for active devices is Au pillars capped with solder. Using Ni-pillars is another good approach due to microstructural stability and good high temperature properties of Ni. In a normal 100% solder interconnect, solder serves as the support structure, electrical conductor, and mechanical wetting agent to the substrate and the die. The drawback of this approach would be failure due to creep and thermal fatigue during high temperature application due to CTE mismatch between the substrate and the components. However, using a combination of Au or Ni pillar with solder would provide a high strength interconnect with reasonable compliance resulting in a reliable assembly. Intel Corp. has introduced "Copper Pillar Bumping (CPB) Technology" in their 65 nm dual-core processor [7]. A cross-section view of a copper bump is shown in Figure 6.4. CPB offers high interconnect density, better electrical and heat dissipating performance, greater mechanical strength and increased reliability. This pillar bumping technology is an attractive option for high temperature packaging, where use of an underfill is challenging due to temperature compatibility of underfill material. Since copper might not be suitable due to grain growth at high temperature, Au and Ni could be evaluated for this application.

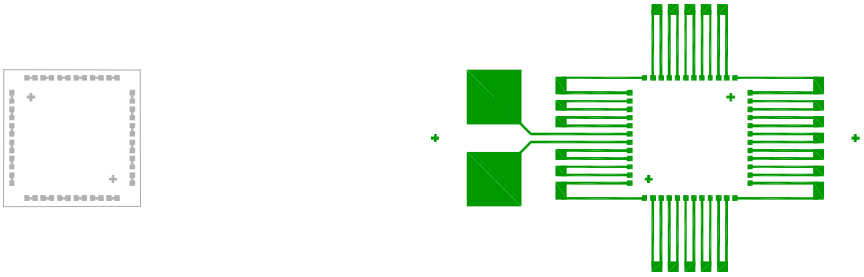


Source: Intel

Figure 6.4. Cross-section view of Intel's Copper Pillar Bump (CPB) Technology [7].

6.2 Stud Bump Development

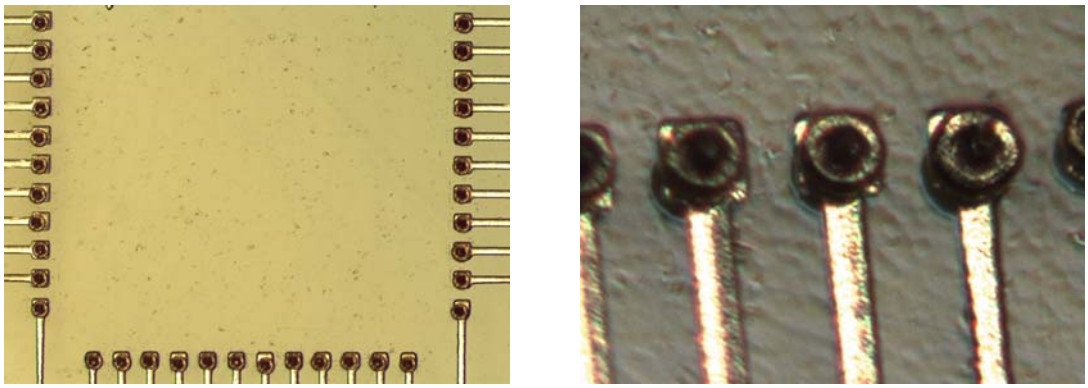
Au stud bumping on flex and die assembly using thermosonic bonding has been demonstrated. The daisy chain coupon for the flex substrate and 2.5 mm by 2.5 mm die with 150 μm pitch and 100 μm pad size is shown in Figure 6.5.



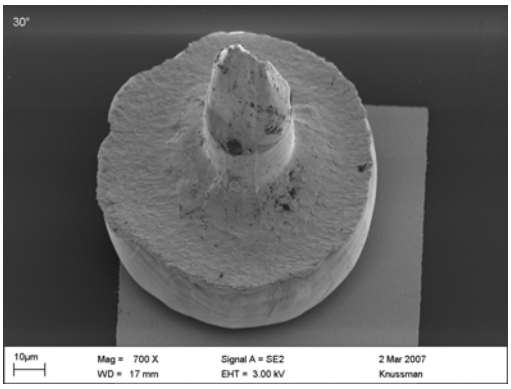
(a) (b)

Figure 6.5. Schematic showing the daisy chain layout for stud bumping (a) die and (b) flex substrate.

Au stud bumps were made using K&S 4522 wire bonder, which has a capability of operating both in wire bonding and stud bumping mode. A 1 mil diameter wire was used and the bump diameter was chosen to be about 4.5 times the wire diameter. Figure 6.6 shows optical and SEM images of the bumped flex substrate.



(a)



(b)

Figure 6.6. (a) Optical and (b) SEM images of bumped flex substrate prior to coining.

Stud bumps were then coined and die was assembled using a FineTech thermosonic bonder. The bonding profile is shown in Figure 6.7. Figure 6.8 shows side and top view of the assembled die on substrate.

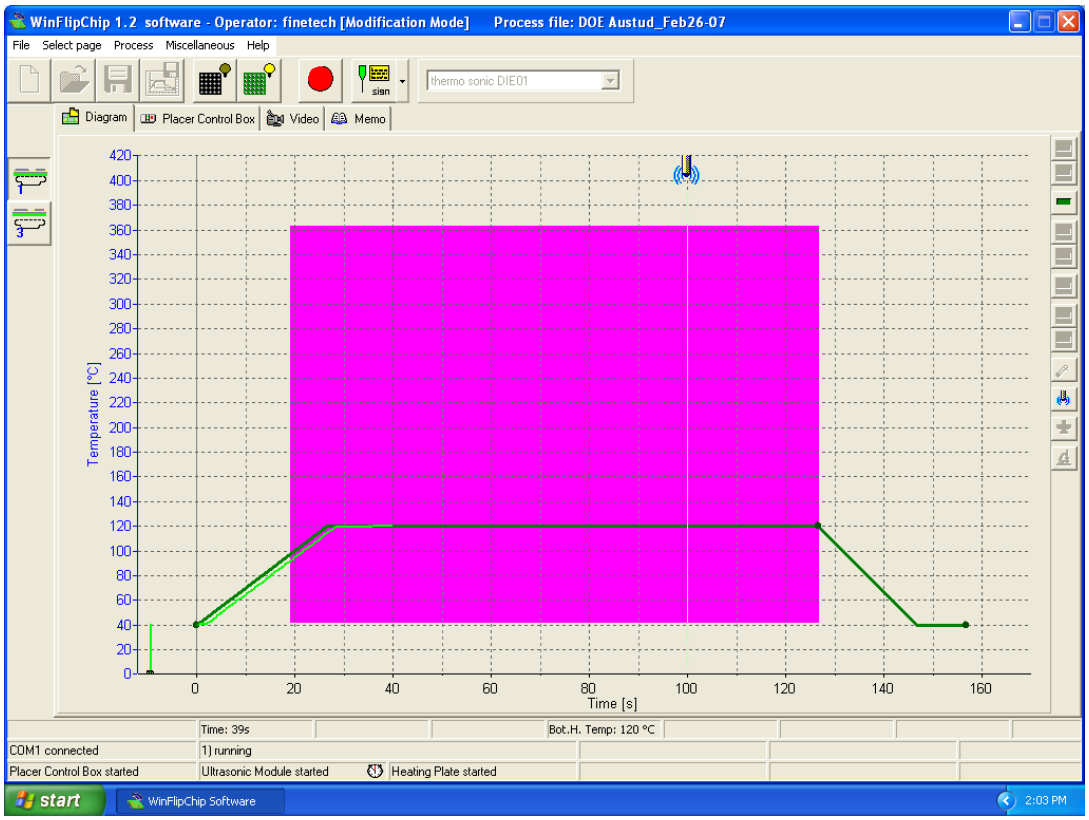
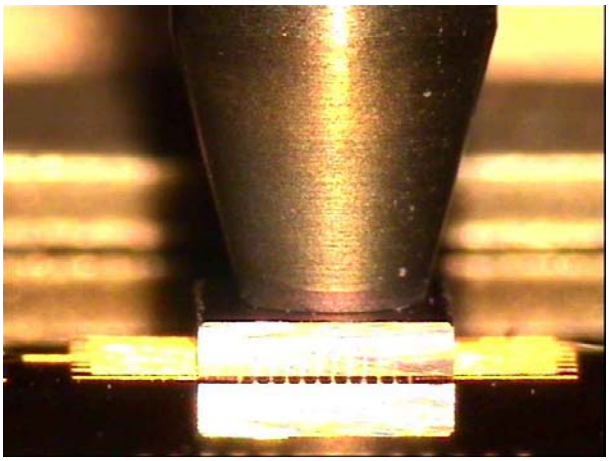
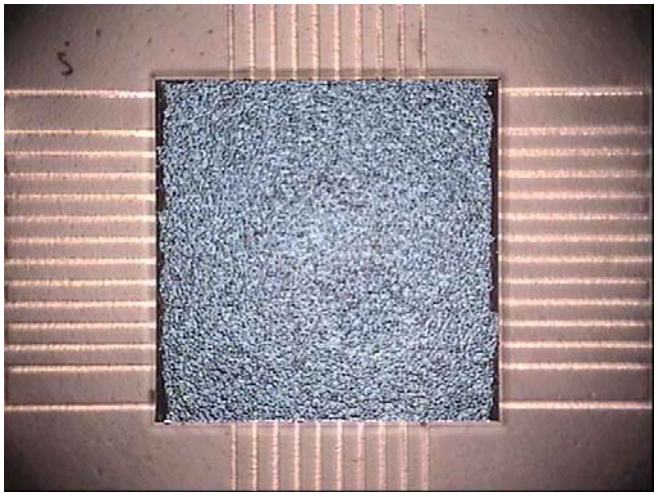


Figure 6.7. Example of a Thermosonic bonding profile for die assembly on bumped flex substrate.



(a)



(b)

Figure 6.8. (a) Side and (b) top view of die assembled on a bumped flex substrate using thermosonic bonding.

During our stud bumping process, the flex substrate is first bumped and then chip is assembled using a thermosonic bonding method. The parameters that have been varied are thermosonic bonding temperature (pick up tool temperature), ultrasound power, ultrasound working time, and heating time. Ultrasound power of 10,000 mW for duration of 2000 ms was used for the bonding. A force of 22 N was used for the thermosonic bonding. For stud bumping the flex, the substrate was temporarily rigidized in a 2 inch X 2 inch frame for handling. The parameters used for stud bumping the flex were power = 1.8, force = 1, ball size = 4.5, temperature 130°C.

Three different bonding temperatures of 100°C, 150°C and 175°C were used for pick-up tool temperature. A critical bonding temperature of 100°C was observed below which no bonding would take place. Below this critical bonding temperature low bond strength is observed indicating weak bonding. Ten coupons were bumped and assembled using the aforementioned procedure and were tested for bond shear strength and electrical continuity during thermal cycling. Five different coupons were thermal cycled and tested periodically (20-30 cycles) for continuity. The results of these continuity tests are shown

in Figure 6.9. Sample 2K that was processed at 100°C showed failure at 290 cycles. Samples 2H and 2M used a bonding tool temperature of 150°C showed failures between 400-500 cycles. Samples 2G and 2L processed at 175°C showed failures between 400-550 cycles. Failure is defined as 20% increase in resistance or loss in continuity of the daisy chain network. Resistance measurements for each die as a function of number of cycles from 30°C to 250°C are shown in Figure 6.9.

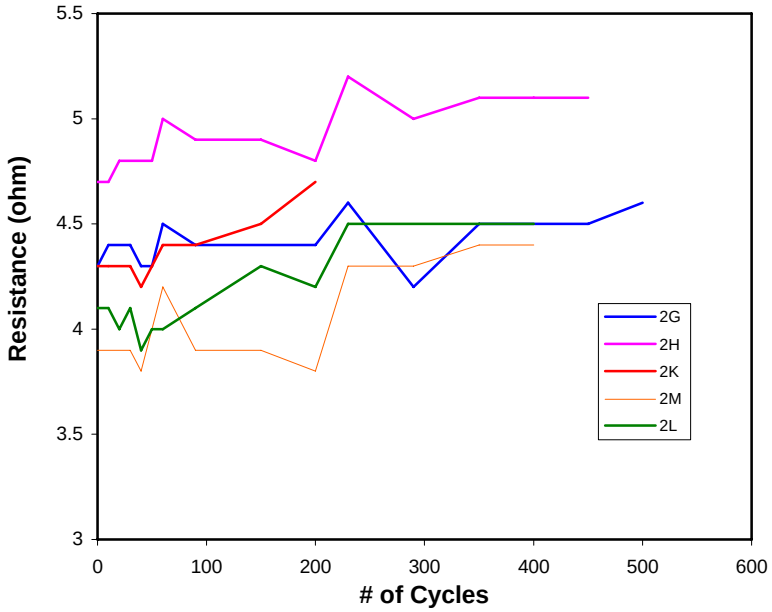


Figure 6.9. Resistance of stud bumped die as a function of number of thermal cycles. Variation in the resistance shown arises partly to variation in the location of the probes during each test.

Sample 2K showed failure at the stud bump die interface as shown in Figure 6.10. Samples bonded at 150°C and 175°C showed failure in the corner bump with largest distance from neutral point (Figures 6.11 and 6.12). This observation is consistent with GE's stud bump reliability model discussed in a preceding section, where high stresses were predicted in the die.

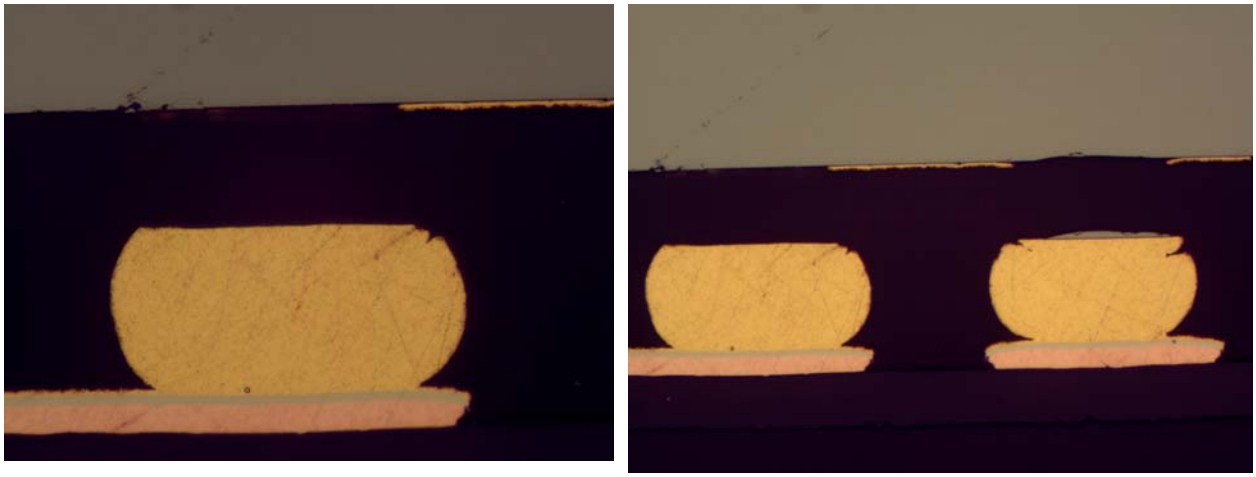


Figure 6.10. Failure at stud bump- die interface in the coupon bonded at 100°C pick-up tool temperature.

Figure 6.11. Failure in the die for coupons bonded at 175°C pick-up tool temperature.

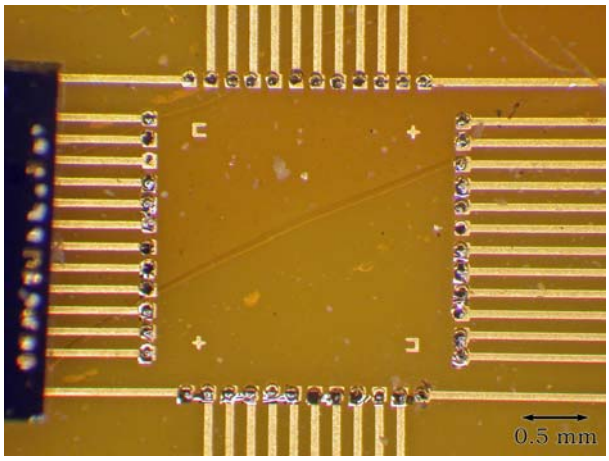


Figure 6.12. Top-down image of failed coupon processed at 150°C. Failure occurred at the stud-bump die interface.

6.3 High Temperature Die Attach Materials

A high temperature die attach is needed for securing the die to the flex for the wire and ribbon bonding samples. Polymer die attach materials that have published operating values of greater or equal to 250ºC were tested for high temperature reliability. Four candidate materials were selected from three suppliers and are listed in Table 6.1 with their rated temperatures.

Table 6.1. High temperature die attach materials.

Material	Mix	Cure	Type	Rated Operating Temperature
EpoTek P1011	NA	80ºC, 10-30 min+150ºC, 1hr	Polyimide	350ºC
EpoTek H74	100:3	150ºC, 5 min	Epoxy	-55 to 250ºC
EpoTek H21D	10:1	150ºC, 5 min	Epoxy	-55 to 250ºC
Ablestik 71-2	NA	150ºC, 30min + 275ºC, 30 min	Polyimide	250ºC

Some of the substrates were found to warp and wrinkle after the specified curing schedule. Generally, the longer and higher temperature cure materials had less warping. A rank comparison of the warp for each material is shown in Figure 6.13.

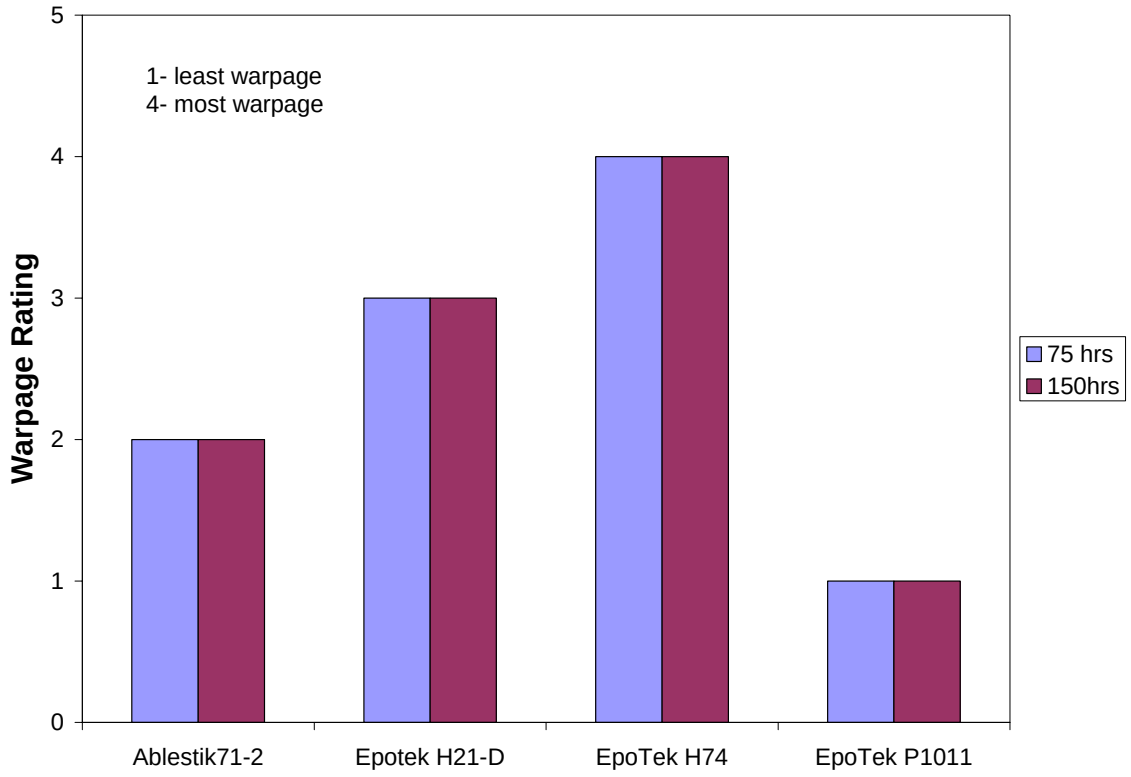


Figure 6.13. Comparison of substrate warp after die attach adhesive cure.

The materials were tested after exposure to high temperature storage at 250ºC in an air ambient atmosphere followed by cycling between 30 and 250ºC in a nitrogen atmosphere. One group of samples was exposed to 250ºC and shear tested after 75 hours and 150 hours (Figure 6.14). While none of the materials showed poor shear strength as evaluated using MIL-STD-883 standards, the Ablestik 71-2, Epotek H21D and H74D maintained a higher shear strength than the Epotek P1011.

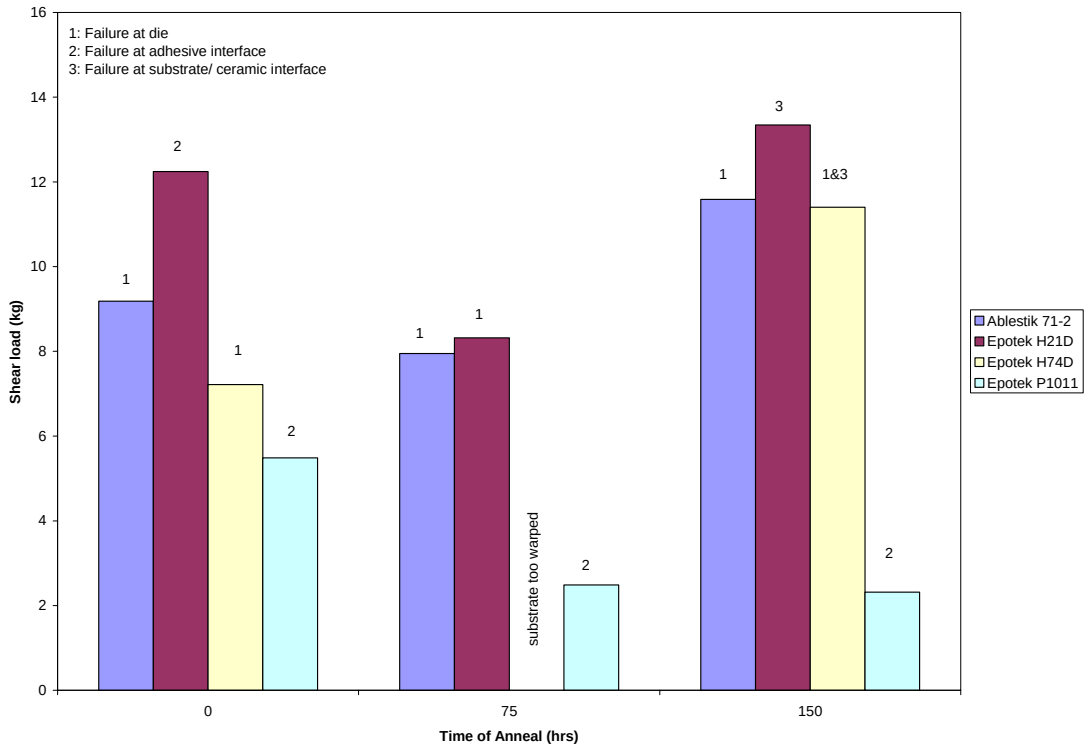


Figure 6.14. Shear testing results after exposure to 250ºC.

A second group of samples were exposed to 75 hours of 250ºC followed by temperature cycling from 30 to 250ºC. Samples were shear tested after cycle intervals. The results to date are shown in Figure 6.15. A slight decrease in the shear strength of the Epotek P1011 was observed while the other materials continue to hold higher shear strength. Temperature cycling is planned to continue sampling after 50 cycle intervals. Based on the performance of the materials tested, Ablestik 71-2 was selected for processing the wire and ribbon bonding test samples. The Ablestik 71-2 has the additional advantages of having a single component and reasonable pot life that is beneficial in manufacturing.

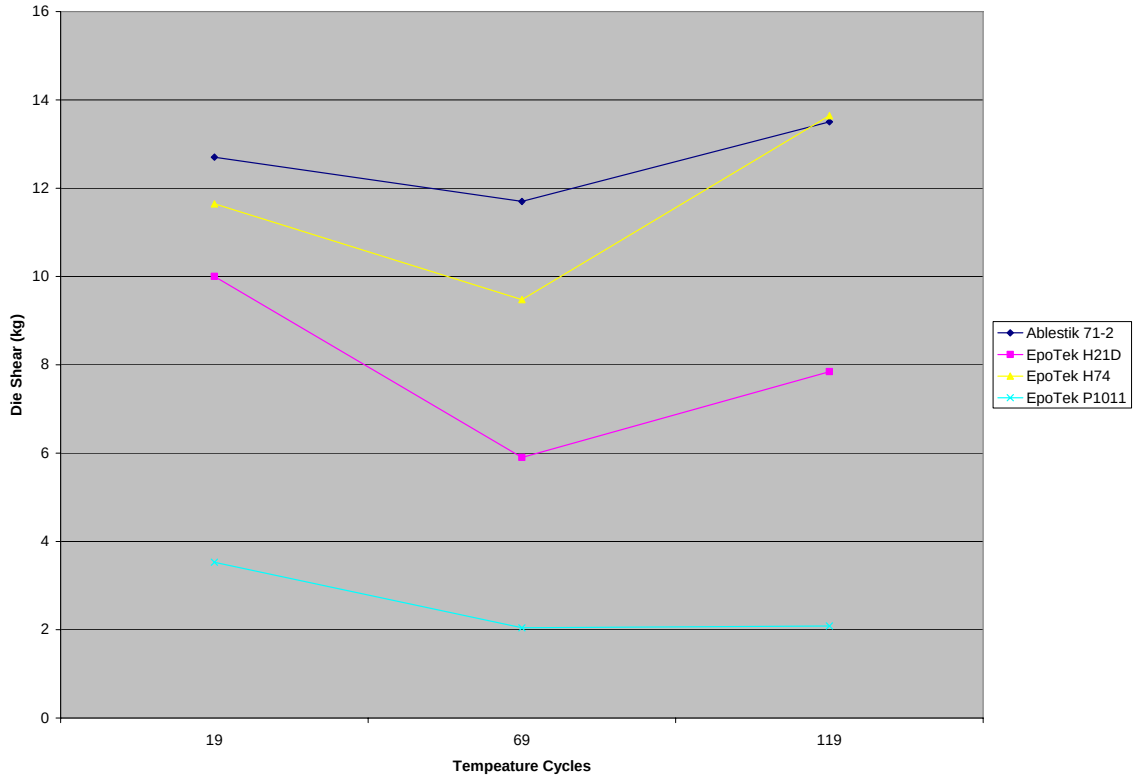


Figure 6.15. Shear strength after temperature cycling 30 to 250°C.

6.4 Reliability Testing of Active Device Interconnect Coupons

A daisy chained test coupon was fabricated with four separate groups of three daisy chained test die. A figure of the test coupon and a ribbon bonded test die are shown in Figure 6.15. Each test die has 40 bond pads. Two coupons were wire bonded with 4 daisy chains of 3 die per coupon. Two coupons were ribbon bonded but due to difficulty in tooling only 2 daisy chains on one coupon and 3 daisy chains on the other coupon yielded for testing.

The daisy chains are continuously monitored consistent with IPC-9701A (Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments). A profile of 7 cycles is shown in Figure 6.15. A Blue-M Ultra Temp Inert oven is used for temperature cycling between 35 and 250°C with a dwell time of 15 minutes at each extreme and a nitrogen ambient atmosphere. The daisy chain resistance is monitored using an Agilent 35970A data acquisition/switch unit with 34901A and 34908A multiplexers. The 35970A is scanned using a Labview application every 60 seconds and logs the oven temperature and daisy chain resistances. The connection between the daisy chains and the data acquisition unit is through glass insulated, 20 AWG nickel wire with AMP Strato-Therm terminals, which make contact to pads on the flex circuits using #4-40 screws and lock washers. The flex are mounted onto PEEK substrates drilled and tapped with #4-40 mounting holes to accommodate the flex test circuits. The daisy chained die were continuously monitored for resistance and failure cycle recorded. Reliability distribution analysis was performed using an interval censoring approach.

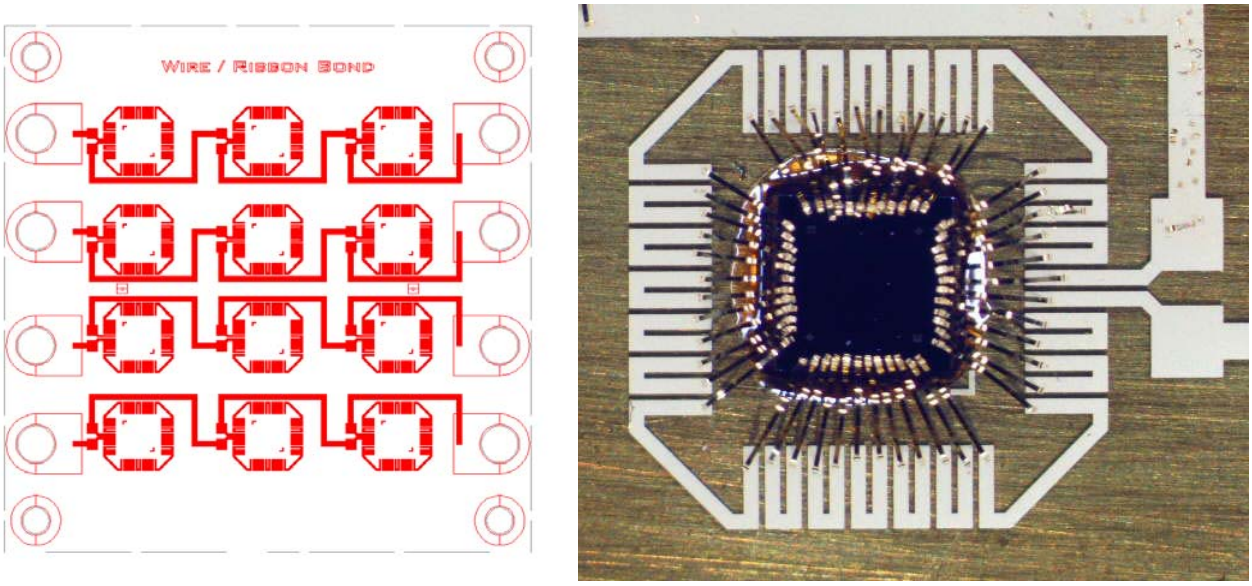


Figure 6.15. Test coupon and sample ribbon bonded test die.

Figure 6.16. Temperature cycling profile (35 to 250°C).

Resistive nets inspected at 50 cycle intervals and failed daisy chain nets were recorded. The samples have completed 277 cycles at the time of this report. The failures were found to fit a two-parameter Weibull distribution. The distribution plots are shown in Figure 6.17 for wire bond, ribbon bond, and stud bump samples. The stud bump failures were reported in Figure 6.8. The Weibull distribution parameters are shown in Table 6.1. A comparison of the means shows the stub bumped samples having the highest mean time to failure, the ribbon bonded samples having the shortest life and the wire bonded samples in the middle. The ribbon bonded sample failure may be attributed to its stiffness in the planar direction that is exacerbated by wrinkling of the flex during cycling. The flex could be laminated to stiffener with a high temperature adhesive, such as

Staystik, to reduce this problem. The stud bumps are less prone to the flexing due to their small size and the orientation of their short leads.

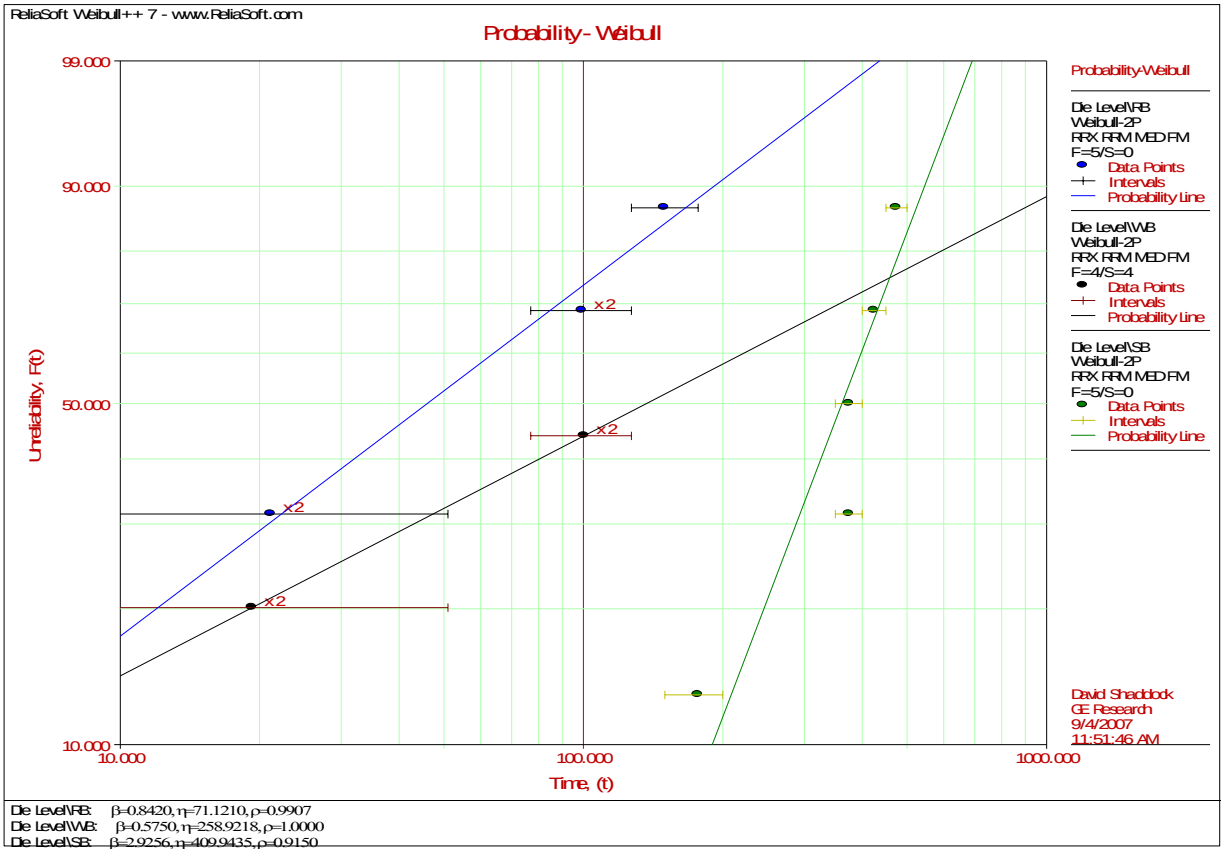


Figure 6.17 Distribution plots of interconnect failures.

Table 6.1 Distribution Parameters of Failed Interconnects

Solder Alloy	Mean	Beta
Ribbon Bond	71.12	0.8420
Wire Bond	258.92	0.5750
Stud Bump	409.94	2.9256

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Conclusions

Ultimately, the results of this program should be demonstrated through a test vehicle which would be tested at high temperature and vibration. In order to manufacture and assemble such a vehicle, a design for such a vehicle must be made using the recommendations for substrate and interconnect methods from this program. The downselection of packaging methods is based on the conclusions of fatigue and reliability testing of the different packaging methods discussed in the preceding sections.

This study has led to some basic conclusions about the design of flex-based packaging methods for high temperature environments. First, Kapton E has been chosen as the primary polyimide material for this application. Kapton E was chosen for its superior CTE match in the x-direction as well as its low CTE in the z-direction which is beneficial for via reliability. In addition, it is a commonly used material within the packaging industry which allows for easier adoption by the oil and gas community.

Two important modes of failure in flex-based packages are adhesion of the copper traces to the flex and fatigue of vias in the flex. From testing in an inert atmosphere (nitrogen), Cr seed layer of approximately 500 A was shown to provide reliable adhesion to the flex for over 1000 hrs at 250ºC. Thermal cycle testing examining via geometries which would enable two-sided board designs and more dense board layouts has shown that for more than 600 vias, no failures have occurred during 1200 thermal cycles. This is significantly more reliable than dictated by recent draft SAE standards on high temperature electronic packaging. Since failures have not occurred, it would be advisable to use the finite element models as a guide to via design. These models indicated that larger diameter vias with thicker Cu lowered the stress in via.

Thermal cycling of active and passive component interconnects has been used to experimentally compare the reliability of different packaging methods. Validation testing of the high temperature solders has shown that the 92.5Pb-5Sn-2.5Ag solder outperforms all other solders in terms of failures during testing. Also this solder was found to be easier to wet to assemble devices than others. For pad materials, NiPdAu metal stack on the polyimide was shown to have higher die shear strength than NiAu pad metallurgy. For active devices, the tests performed by this study indicate that stud bumping of the polyimide substrate is more reliable than wire or ribbon bonding. It should be noted that more tests should be performed to confirm this statistically.

However, there will need to be further work in order to build a test vehicle for validation of these design recommendations. In order to withstand vibration, a design for substrate constraint will need to be modeled in order to minimize vibration stresses at specific components. This analysis may recommend rigidization of the substrate for lower stresses which will require a lamination material that is suitable for high temperature. If the design for the test vehicle requires a complex interconnect pattern, a multilayer board configuration would be necessary. Additional work on the testing of the solders and stud bumping should

be performed in order to gain additional information on the assembly methods and failure modes of these interconnect methods.

Appendix A. Detailed Results of FMEA

Item/Function	Potential Failure Mode(s)	Potential Effect(s) of Failure	Sev	Potential Cause(s)/Mechanism(s) of Failure	Occ	Current Design Controls	Det	RPN	Recommended Action(s)
Substrate	Deadhesion of the metal (copper)	open circuit	8	humidity, temperature, CTE mismatch, embrittlement	5		1	40	High Temperature(250C)/Humidity Storage + Peel Strength , Insitu Peel Measurement
	Thru interconnect failure	open circuit	8	CTE mismatch stress, humidity, low elongation of Cu	9		1	72	Via Chain thermal cycling to test via, Continous Operating/Humidity
	electrical leakage	short, low resistance path	8	humidity, high temperature, contamination, material breakdown	1		5	40	SIR test at Temperature
	mechanical fracture	open circuit, mechanical failure	8	temperature, bending of the substrate	1		1	8	No Action
Interconnect	solder fatigue	open circuit, high resistance connection	8	CTE mismatch, humidity, manufacturing process, material selection	9		5	360	thermal cycling, High Temperature/ Humidity Storage, Intermetallic growth (sections)
	overstress	open circuit	8	vibration, shock, manufacturing defect, material selection	5		1	40	Random vibration @ Temperature, Shock
	die attachment material for wirebonding	accelerate wire bond failure	6	humidity, CTE mismatch, material selection, mfg. Defect	5		6	180	Storage & Cycling
	wire bond failure	open circuit, intermittent	8	metalization, vibration, CTE mismatch, humidity	9		3	216	Storage & Cycling, pull tests
	Stud bump failure	open circuit, high resistance, intermittent	8	metalization, bump height variation, vibration, humidity, CTE	9		3	216	Storage & Cycling, shear testing
	microvias	open circuit, high resistance, intermittent	8	CTE, humidity, metalization ductility, material selection, mfg. Defect	9		3	216	Storage & Cycling
Encapsulation	mechanical failure	corrosion of components, accelerated wire bond failure	7	cracks, penetration of contaminants, wirebond breakage, CTE, humidity	9		6	378	High Temperature/ Humidity on a vehicle with connections

Appendix B. Milestone Plan / Status Report

Critical Path Project Milestone Description	Planned Start Date	Planned End Date	Actual Start Date	Actual End Date	Comments
Coupled Thermal mechanical models of Package designs	9/1/2007	5/7/2007	9/1/2007	6/1/2007	Completed late due to equipment delays at SUNYB, Refinement of the mechanical models of solder interconnect will be completed prior to the end of the program
Downselection of preferred package method(s)	5/21/2007	7/16/2007	5/21/2007	8/31/2007	Experimental work continued to validate models and demonstrate reliability, cycling of stud bump die was finished and results analyzed. Test coupons for solder evaluation were assembled and tested. Test coupons for wire/ribbon bonding were assembled and tested.
Test Vehicle Design for a Prototype Electronics Board	7/16/2007	8/10/2007	8/1/2007	8/31/2007	Evaluation of solder test coupons and active interconnect methods has been complete. Recommendations for materials and interconnect schemes made as part of the final report.

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