PROCEEDINGS OF SCIENCE

3D Circuit Integration for Vertex and Other Detectors

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High Energy Physics continues to push the technical boundaries for electronics. There is no area where this is truer than for vertex detectors. Lower mass and power along with higher resolution and radiation tolerance are driving forces. New technologies such as SOI CMOS detectors and three dimensional (3D) integrated circuits offer new opportunities to meet these challenges. The fundamentals for SOI CMOS detectors and 3D integrated circuits are discussed. Examples of each approach for physics applications are presented. Cost issues and ways to reduce development costs are discussed.

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1. Introduction

The requirements for vertex electronics and detectors continue to push the limits for lower mass and power, and higher resolution. Over the past years significant progress has been made to address these issues by integrating sensors and front end electronics in Monolithic Active Pixel Sensors (MAPS). Although much has been accomplished, MAPS have a number of fundamental limitations. Minimum ionizing particles leave 80 electrons/micron in the MAPS epi layer. Since the epi layers, when they are present in a CMOS process, are only about 2-15 microns thick, the signals are relatively small. Furthermore, to avoid charge loss, most readout circuit designs are limited to strictly NMOS transistors or designs with very few PMOS transistors, thus limiting the complexity of readout circuit. Finally, since charge collection is due to diffusion and not drift, signal rise time is rather slow for many applications.

There are other approaches now being developed that offer advantages over MAPS. SOI CMOS detectors offer larger signals with faster rise times due to depleted diode regions in the high resistivity substrate beneath the buried oxide (BOX). Early work on SOI CMOS detectors was reported by C. Penng [1], followed by J. Marczewski [2]. Recent availability of SOI CMOS in deep submicron processes has spurred new developments [3].

The newest approach being vigorously pursued by industry is three dimensional integrated circuits (3D). Reductions in trace length in 3D circuits results in lower resistance, capacitance and inductance which improves circuit performance. The two main applications currently being developed are stacked memory for speed, and imagers with higher functions built into the pixel. The work being done on imagers is directly applicable to HEP vertex circuits where higher functionality (compared to MAPS and SOI CMOS) can be placed in each pixel. An additional benefit of 3D is the ability to dramatically reduce mass as will be shown later in this paper. The first circuit for HEP using 3D technology has already been designed [4].

2. SOI CMOS Detectors

Wafers for SOI Detectors are obtained from companies such as SOITEC in France. The wafers arrive with a very thin silicon layer on top of an oxide layer called the buried oxide (BOX). Beneath the BOX is a high resistivity substrate which is generally used only for mechanical support. In an SOI detector, diode implants are formed in the substrate beneath the BOX and connected by means of vias to CMOS circuitry built in silicon islands on top of the BOX as shown in Figure 1. The substrate forms the detector volume which can be depleted by applying a bias on the backside of the substrate.

SOI detector have a number of advantages. Pixels can be laid out with 100% fill factor. Since all of the CMOS circuitry is formed in P and N islands above the BOX, both NMOS and PMOS transistors can be used without causing a charge loss problem as found in MAPS. The signal amplitude is proportional to the thickness of the substrate and not limited to the epi thickness as with MAPS. Because the charge from ionizing particles is collected by drift rather than diffusion, signals will have a faster rise time. Since diffusion is less dominant, there will

be less chaarge sharing than in MAPS. In addition to the above advantages, SOI circuits have long been know to use less power and be immune to latchup.

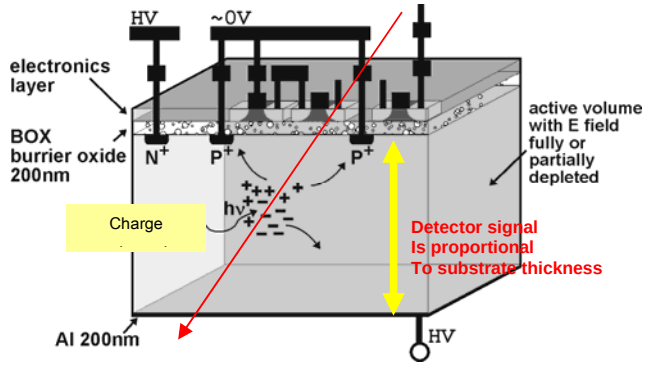

Figure 1 – SOI CMOS detector showing ionizing particle and charge collection principle

2.1 Fermilab SOI CMOS Detector

Yasuo Arai from KEK has brokered two multiproject runs at OKI in Japan to develop SOI CMOS detectors [3]. The second run, which was done in a 0.15 um process, had projects from several organizations including KEK, University of Hawaii, Lawerence Berkeley Laboratory, and Fermi National Accelerator Laboratory.

Fermilab designed a Monolithic Active Pixel Matrix with Binary Output chip, MAMBO, which is an imaging detector to be used in counting applications. The chip is intended for direct detection of soft X-rays and for use in electron microscopy (TEM) [5]. The chip is a 64 x 64 pixel array laid out on a 26 um pitch. There are four parallel sensing diodes spaced 13 um apart in each pixel. Each pixel has a Charge Sensitive Amplifier, CR-RC^2 shaper, discriminator and a 12 bit counter as shown in Figure 2. There are 280 transistors in each pixel.

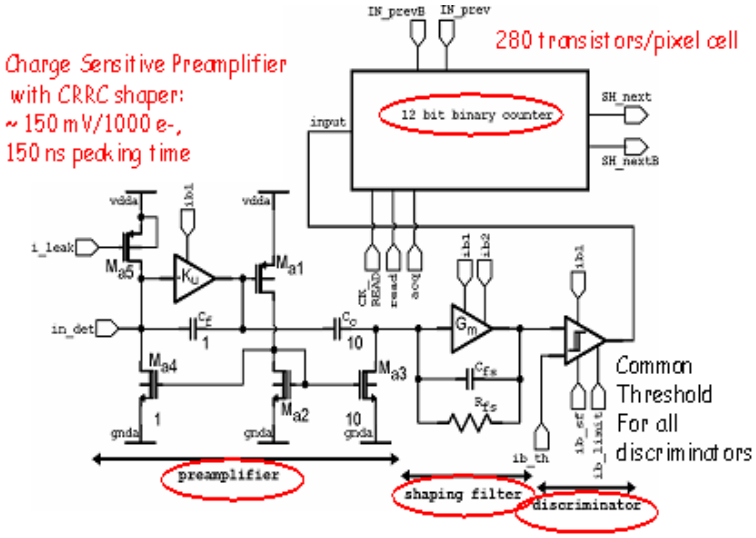

Figure 2 – Schematic diagram of electronics for one pixel cell in MAMBO chip.

Figure 3 shows the layout of one pixel cell including the four equally spaced detector diodes. All of the analog circuits are located at the center of the pixel while the 12 bit counter is wrapped around the outside edge of the cell. The counter is reconfigureable as a shift register for serial readout of all pixel cells.

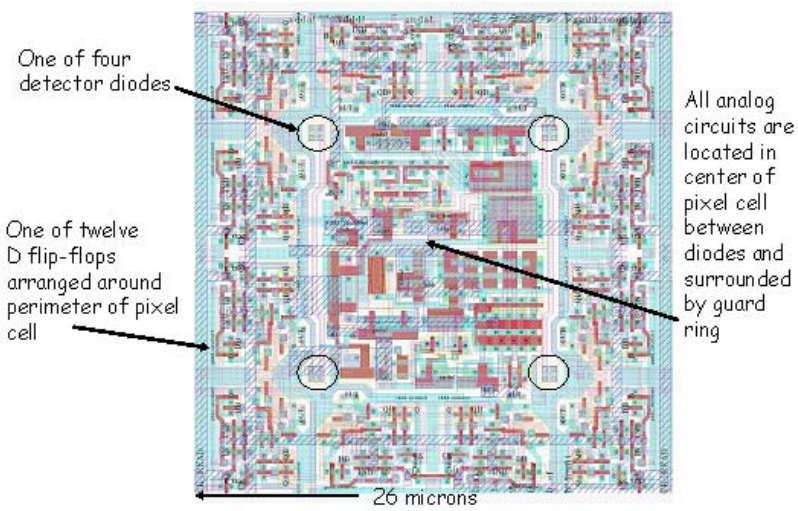

Figure 3 – One pixel cell in the MAMBO chip.

The MAMBO chip was found to be only partially functioning when it was tested. The analog portion of the chip was found to be working although the gain was lower and shaping time faster than expected. This was traced to inaccurate models. The counter circuits had high leakage currents which inhibited proper operation of the flip-flops. These problems will be corrected in the next submission.

2.2 Potential Problems in SOI Detectors

Three potentail problems have been observed in SOI detector circuits. The buried oxide

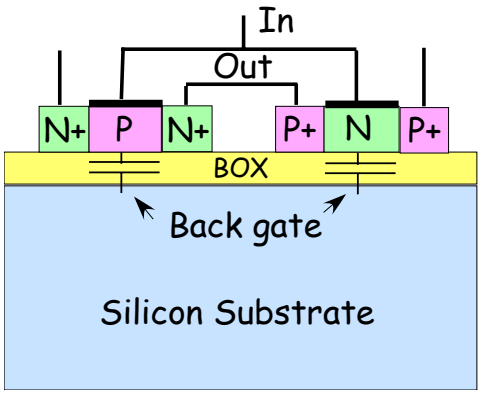

Figure 4 – Back gate effect for transistors.

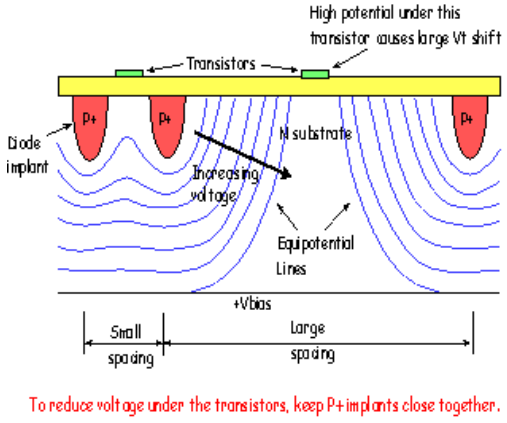

Figure 5- Effect of diode implants on $V_{backgate}$.

acts as a back gate for the NMOS and PMOS transistors as shown in Figure 4. The BOX is thick enough (200 nm) to trap charge and cause threshold shifts with radiation. It has been shown, however, that the threshold shift can be corrected by adjusting the substrate voltage with a separate bias supply connected to the back of the substrate [6].

When a voltage is applied to the back side of the substrate to deplete the substrate in detector applications, the voltage directly beneath the BOX is dependent on the diode implant spacing as shown in Figure 5. When the implant spacing is small, the voltage directly beneath the BOX is low and has little effect on the transistors above the BOX. If however, the spacing is large enough, the full backside voltage can appear beneath the BOX which is acting as a back side gate for transistors above the BOX. A large enough voltage on the back gate will cause threshold shifts that are large enough to cause circuit failure. Thus for the MAMBO chip, a diode implant spacing of 13 microns was chosen to minimize the back gate effect. A transistor with a separate back gate can eliminate this problem [7].

The BOX is relatively thin (200-400 nm), which permits the active circuitry above the BOX to inject charge through the BOX into the detector substrate as shown in Figure 6.

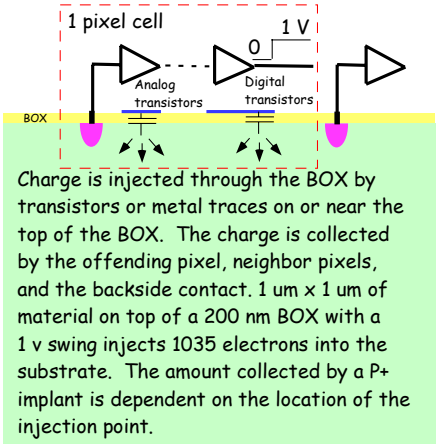

Figure 6 – Charge injection from active CMOS circuitry into the substrate.

This problem can be reduced or eliminated by adding a pinning layer, using differential signals, or having no active circuitry above the BOX during signal acquisition.

3.0 3D Integrated Circuits

A 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded, and interconnected to form a "monolithic" circuit. These layers or tiers can be fabricated in different processes. Industry is moving toward 3D to improve circuit performance. Performance is improved by 1) reducing interconnect resistance, inductance, and capacitance for higher speed, 2) reducing I/O pad count, 3) reducing interconnect power and crosstalk, and 4) reducing the circuit form factor. Several examples of 3D pixel arrays exist [8], [9], [10]. Vertex detectors can take advantage of the 3D work being done in industry.

Three dimensional integrated circuits for pixel arrays offer several advantages over SOI detectors. The 3D circuits can have increased circuit density due to multiple tiers and at the same time be very thin as shown in Figure 7. Different materials can be used for each tier to optimize circuit performance. Thus circuits developed in CCD, DEPFET, and MAPS technologies can be improved by vertically adding additional circuitry.

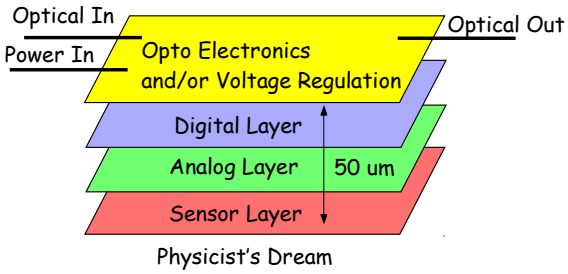

Figure 7 – Ultimate three dimensional integrated circuit for High Energy Physics.

Circuits for HEP can be fabricated using either die to wafer bonding or wafer to wafer bonding as shown in Figure 8. Die to wafer bonding may be more advantageous for HEP circuits since wafers of different sizes can be used and yield can be improved due to the use of known good die (KGD). Wafer to wafer bonding requires less material handling but wafers must be the same size with circuits aligned to permit simultaneous interconnection of all chips.

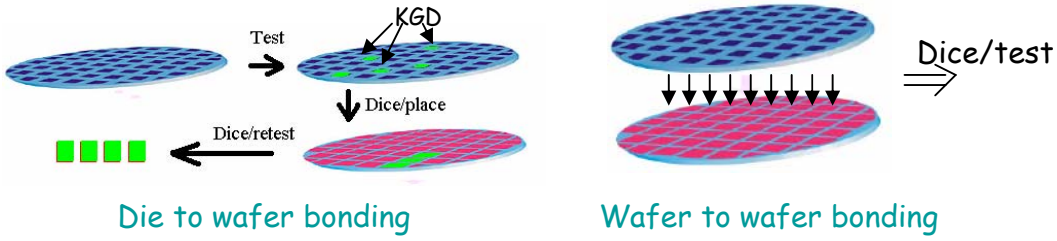

Figure 8 - Die to Wafer and Wafer to Wafer bonding choices.

3.1 Key Technologies for 3D circuits

There are four key technologies for 3D circuit integration: 1) bonding between layers, 2) wafer thinning, 3) through wafer via formation and metallization, and 4) high precision alignment. Many of these technologies are also used in the development of SOI detectors.

3.1.1 Bonding Between layers

Two commonly used bonding processes are shown in Figure 9: adhesive bonding (using BCB) and oxide to oxide bonding. The adhesive bond has temperature limits that may restrict later 3D processing steps. The oxide bond is a strong bond that forms when two specially prepared smooth silicon oxide surfaces are brought together. Both of these bonding techniques are generally used only for wafer to wafer bonding and only provide mechanical bonds.

Electrical interconnects (metal filled vias) must be added at a later time. Although capacitive interconnects are used in some situations, they are not practical for most HEP applications.

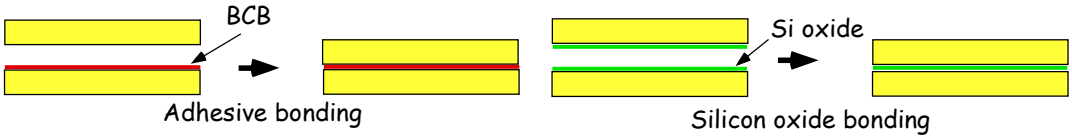

Figure 9 – Adhesive bonding and silicon oxide bonding techniques.

Two other bonding techniques are commonly used to form both electrical and mechanical connections during the bonding process: copper thermo compression bonding, and copper tin eutectic bonding. Since these bonds also provide the mechanical connection between devices, the bonded surface area has typically been around 75%. In order to achieve a large bonding area, extra copper is deposited on the surfaces to be bonded as shown in Figure 10. Typically the copper on each surface is about 5 microns thick.

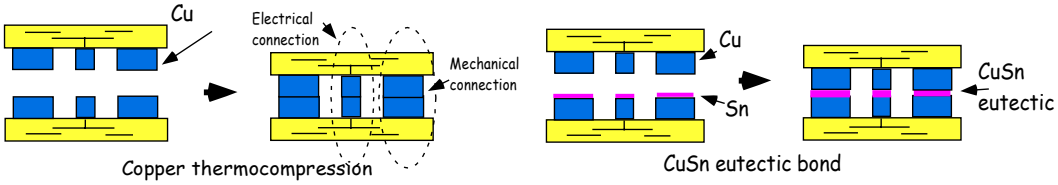

Figure 10 – Copper themocompression and CuSn eutectic bonding.

A 10 micron thick layer of copper between devices represents 0.1% of a radiation length, which would be unacceptable for low mass applications like the vertex detector in the ILC. One advantage of the copper bonding techniques is that they can be used for both die to wafer bonding as well as wafer to wafer bonding.

The Direct Bond Interconnect (DBI) is a bonding technique that also provides electrical and mechanical connections but uses minimal metal (providing very low Z). DBI uses both oxide bonding and thermo compression metal bonding in the bonding process as shown in Figure 11.

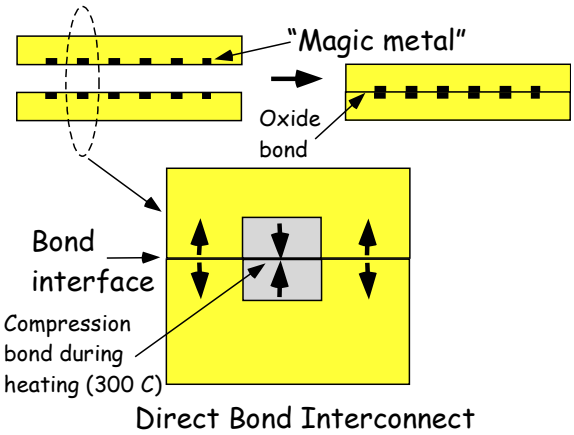

Figure 11- The Direct Bond Interconnect process

The silicon oxide surfaces, with small embedded metal pads, are prepared for oxide bonding. After the parts are brought together and a strong mechanical oxide bond is formed, the parts are heated to about 300 degrees C causing the metal to expand and form the electrical interconnects. Due to the strong mechanical bond across the entire surface area, further 3D processing such as thinning can be done without damaging the bonds. The metal connections are about one micron in diameter and only 1 micron tall. Bonding at a pitch of 3 microns has been successfully demonstrated. The DBI process can be used for die to wafer bonding as well as wafer to wafer bonding. The DBI process could be a replacement for conventional bump bonding, particularly in fine pitch applications. Ziptronix in North Carolina is the only company currently offering the DBI process.

3.1.2 Wafer Thinning

Through wafer vias typically have an 8 to 1 aspect ratio. In order to keep the area of the via as small as possible, the wafers should be thinned as much as possible. Thinning is typically done by a combination of grinding, lapping, and chemical or plasma etching. In SOI processes wafers can be thinned to 6 microns, as shown in Figure 12, by using the BOX as an etch stop. In CMOS processes, wafers can be thinned to about 15-20 micron.

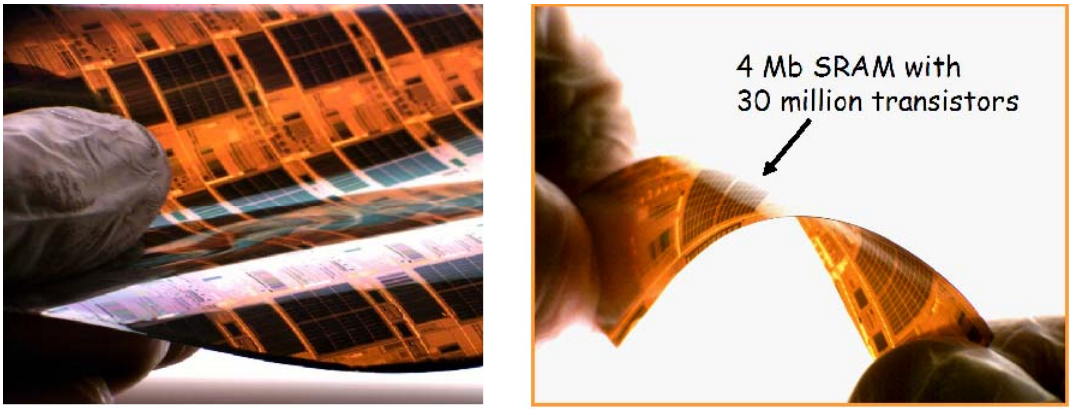

Figure 12 – Six inch wafer thinned to 6 microns and mounted on 3 mil kapton at MIT LL.

3.1.3 Through Wafer Via Formation and Metalization

Via holes and metallization may take place on wafers before bonding or on die and wafers after bonding. This choice is known as “via first” and “via last” in 3D technology and depends on the fabrication process being used.

Vias in CMOS circuits are formed using the Bosch process [11] and must be passivated before filling with metal. Vias in SOI are formed in the insulator areas between transistors using an oxide etch. Since the SOI vias are already in an insulator, the vias no not require passivation. Figure 13 shows vias formed in CMOS and in SOI. The oxide etch vias tend to

have more angled side walls than the Bosch process. The oxide etch via shown is about 1-2 microns in diameter in a SOI process with 3 metal layers.

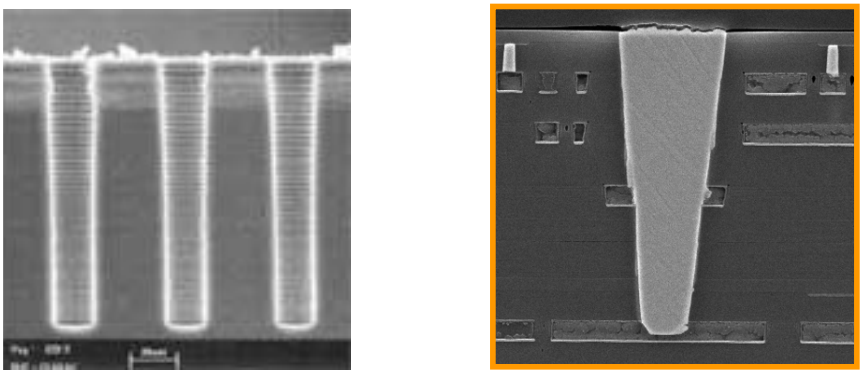

Figure 13 – (Left) SEM of 3 vias in Bosch process, (Right) SEM of oxide etch via from MIT LL

3.1.4 Precision Alignment

Precise alignment is needed for small diameter vias. Die to wafer and wafer to wafer alignment at the 1 micron level has been achieved by MIT, IBM, and Ziptronix. Die to wafer placement will provide the best yield for HEP and is better suited to layouts with different arrangements of die on a wafer. Figure 14 shows die to wafer and wafer to wafer placement.

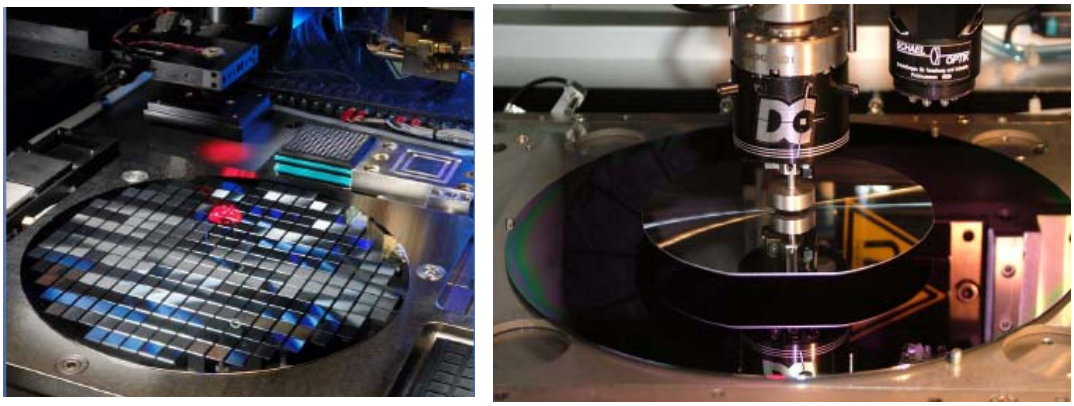

Figure 14 – (Left) 1 Megapixel, 8 um pitch die being mounted on 200 mm ROIC wafer, (Right) wafer to wafer alignment and placement.. Photos by Ziptronix.

3.2 – 3D Pixel Design for ILC Vertex Detector

A 3D chip called VIP1 (Vertically Integrated Pixel) has been designed in the MIT Lincoln Laboratory 0.18 um process. The chip is intended to be a demonstrator of 3D technology for the ILC vertex detector. Key features of the chip include analog pulse height, sparse readout, high resolution time stamps, test inputs for every pixel, 20 um pixels, and readout between bunch trains. Figure 15 shows a block diagram for a 1 Megapixel array. The

design submitted to a MIT LL 3D multi project run is a 64 x 64 array. Since a sensor layer was not available in the multiproject run, a pad in each pixel was included for bonding to a detector. A schematic for a single cell is shown in Figure 16. Sample 1 occurs before the bunch train.

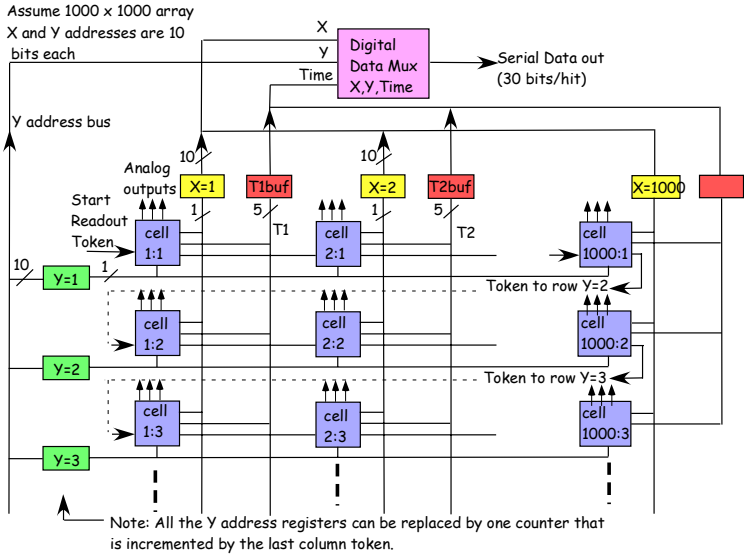

Figure 15 – Block diagram for one Megapixel ILC vertex detector

When a hit occurs, the hit pixel stores sample 2 and the time stamp, and sets the hit latch in the sparse readout circuit. During readout, when the read out token arrives, the time stamp and analog values are read out, and the hit pixel points to the hit address found on the perimeter of the chip. While outputting data from one pixel, the readout token is passed ahead looking for the next pixel that has been hit.

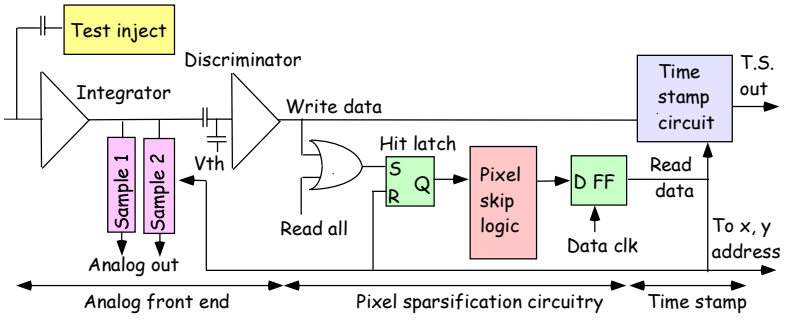

Figure 16 – Schematic of electronics for one pixel cell.

The schematic in Figure 16 is subdivided into three tiers as shown in the right hand side of Figure 17. The left side of Figure 17 shows the layout for each tier and the 3D interconnections between levels. Each pixel cell contains 175 transistors (both NMOS and PMOS) in a 20 x 20 um pixel. Each via is 1.5 um in diameter and is 7.3 um long. Thus the ILC pixel has three layers of transistors, 11 levels of metal in a total vertical height of only 22 microns.

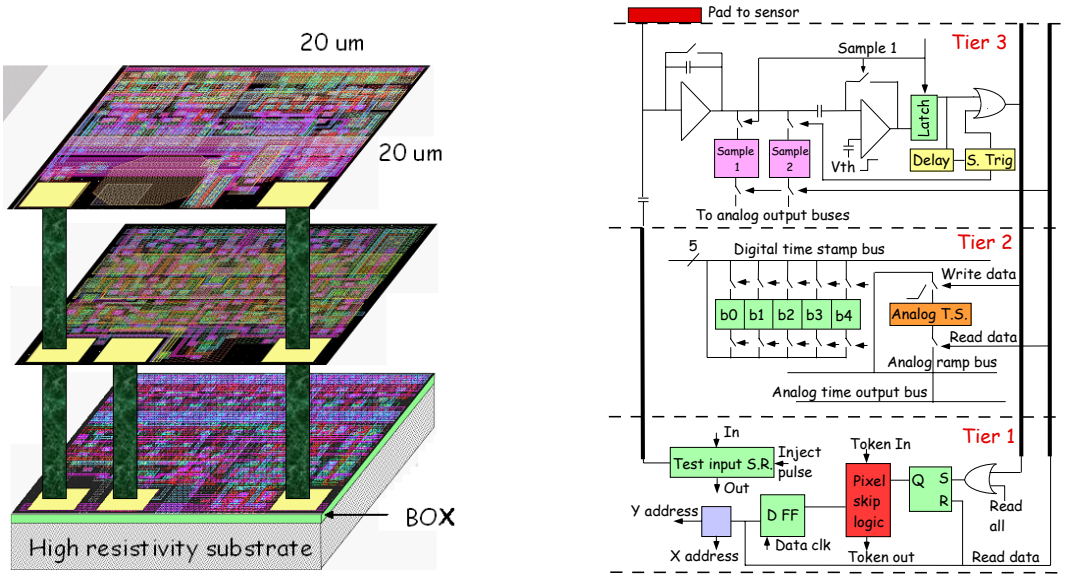

Figure 17 – (Left) Three tier pixel with 3D vias, (Right) three tier schematic.

4.0 Cost Consideration

Three dimensional circuits are expensive to fabricate. Each tier in a 3D circuit generally comes from a separate dedicated run. Thus the cost is roughly proportional to the number of tiers plus bonding between each of the tiers. If wafer to wafer bonding is used, the yield will be lower resulting in a further increase in cost. In HEP the cost needs to be justified based on reduced mass, higher functionality, or by supporting mixed technologies.

Prototyping costs can be reduced by fabricating a detector tier and two electronics tiers from one set of masks and one wafer run as shown in Figure 18. The 3 tiers can be assembled with only one bonding step. Consider a frame that has two A circuits (sense diode and CMOS) and two B circuits (CMOS only). These circuits can be bonded together either face to face or back to face depending on the type of bonding, via formation, and thinning procedures to be used. For the face to face bond, one wafer is flipped horizontally and thinned after bonding. For the face to back bond, one wafer is thinned, rotated 180 degrees and then bonded. Unfortunately, only one half of the silicon results in useful devices.

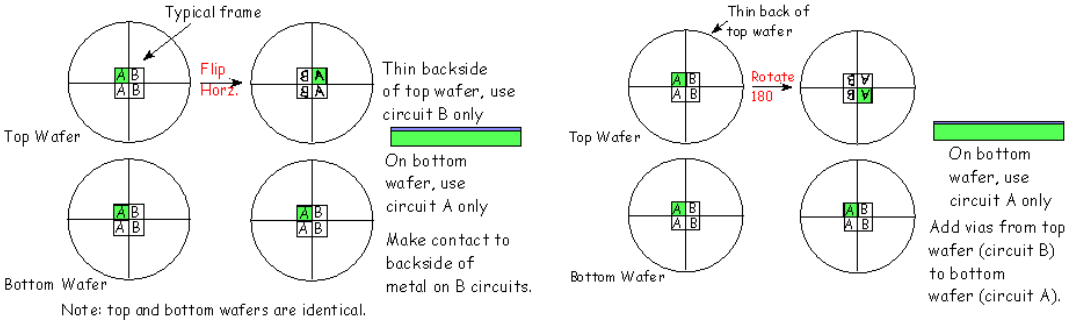

Figure 18 – 3D IC from one mask set. (Left) face to face bond, (Right) face to back bond.

5.0 Conclusion

Industry is pursuing 3D integrated circuit design and developing the key technologies. HEP should continue to follow these developments since they offer new opportunities to meet the stringent requirements of future vertex detectors. The example presented for the ILC vertex detector shows that designs are now possible that meet the ILC mass and functional requirements. Although the development costs are relatively high at this point, sharing runs and creative mask usage can reduce the cost.

6.0 Acknowledgements

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