Small-Scale Readout System Prototype for the STAR PIXEL Detector

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Abstract:
A prototype readout system for the STAR PIXEL detector in the Heavy Flavor Tracker (HFT) vertex detector upgrade is presented. The PIXEL detector is a Monolithic Active Pixel Sensor (MAPS) based silicon pixel vertex detector fabricated in a commercial CMOS process that integrates the detector and front-end electronics layers in one silicon die. Two generations of MAPS prototypes designed specifically for the PIXEL are discussed. We have constructed a prototype telescope system consisting of three small MAPS sensors arranged in three parallel and coaxial planes with a readout system based on the readout architecture for PIXEL. This proposed readout architecture is simple and scales to the size required to readout the final detector. The real-time hit finding algorithm necessary for data rate reduction in the 400 million pixel detector is described, and aspects of the PIXEL system integration into the existing STAR framework are addressed. The complete system has been recently tested and shown to be fully functional.

Index Terms:
Silicon detectors, CMOS detectors, detector readout, cluster finding algorithm.

I. INTRODUCTION

The STAR experiment at the Relativistic Heavy Ion collider (RHIC) at the Brookhaven National Laboratory (BNL) studies hot and dense nuclear matter [1] created in high energy heavy ion collisions. After several years of operation the STAR detector is going through a series of upgrades that will allow for deeper understanding of the observed physics as well as a study of new physics. One of these upgrades, the Heavy Flavor Tracker, will improve tracking capabilities to allow identification of short-lived hadrons containing charm and bottom quarks with decay lengths of hundreds of micrometers [2]. These heavy flavor hadrons are created at very early times in the evolution of the collision and therefore are ideally suited as probes of the early collision dynamics.

The HFT will consist of three detector systems with graded resolution. The outermost detector is an existing double-sided Silicon Strip Detector (SSD) [3] that will be upgraded. The second detector will be a new Inner Silicon Tracker (IST) [4] using single-sided silicon strip sensors. The inner-most and highest precision system will consist of a new PIXEL detector, described below. The PIXEL will allow determination of the position of the secondary vertex with a precision close to 30 μm.

In this work we briefly describe the PIXEL detector which also has been discussed in a previous publication [5]. We present the development of Monolithic Active Pixel Sensors that is ongoing at Institut Pluridisciplinaire Hubert Curien (IPHC), Strasbourg, France, and is dedicated to this new vertex detector. Using the first generation of MAPS prototypes developed for the STAR PIXEL detector, we have constructed a prototype telescope consisting of three sensors with a readout system that includes on-the-fly data sparsification. The readout system is a small-scale prototype that features all functionality required by the final detector system. We have demonstrated the performance of the telescope and the readout system in tests with a 1.2 GeV electron beam at the Advanced Light Source (ALS) at LBNL, and in the STAR detector at RHIC during the 2006-2007 Au-Au run.

II. PIXEL DETECTOR DESIGN

The main requirement for the PIXEL detector is to provide direct topological reconstruction of heavy flavor decays, including those of D0, that are displaced from the main vertex by 100 μm on average [6]. The vertex detector has to provide impact parameter resolution on the order of 30 μm to allow for efficient detection of these secondary vertices. To provide this capability, the vertex detector has to be characterized by very low mass and low Z so that multiple Coulomb scattering is minimized. The design goal is a radiation length of less than 0.5% per layer. This small amount of material can be achieved with sensors thinned down to 50 μm, readout cables with aluminum conductors, and air cooling of the system.

The PIXEL detector, as it is currently envisioned, will consist of 40 sensor ladders with ten 2 cm × 2 cm sensors per ladder. The ladders, supported by a carbon fiber structure, will be organized into two layers at radii of 2.5 and 8 cm with 10 and 30 ladders on the inner and outer layer, respectively. The complete detector will consist of about 400 million pixels. The conceptual design of the PIXEL detector is presented in Figure 1 [6]. The mechanical support structure located at one end is intended to provide capability for quick removal and replacement of the detector while preserving high accuracy positioning.

The sensor pixel pitch chosen for this application is 18.4 μm. This pixel pitch combined with binary readout and the presented geometry of the detector will provide the required impact parameter resolution of $13 \oplus 19$ GeV/p·c μm. It is worth noting that the predicted resolution of the detector is dominated by MCS and is not determined by the individual pixel resolution.

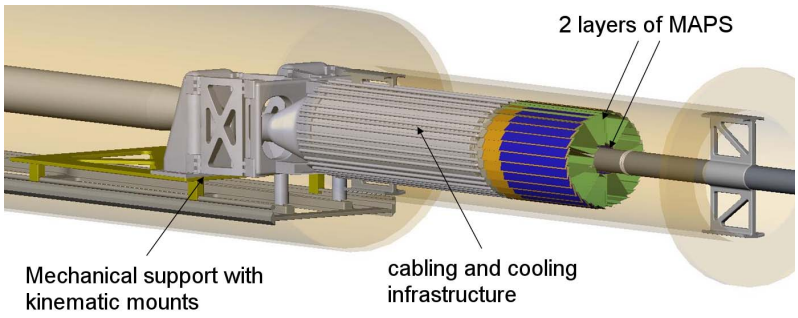


Figure 1. Conceptual design of the PIXEL detector for the Heavy Flavor Tracker. The support structure with kinematic mounts and cabling located in one end of the carbon fiber cone will provide capability for a quick replacement of the detector with a very high accuracy positioning (on the order of 20 μm). A two layer structure of the detector is composed of 30 and 10 ladders in the outer and inner layer, respectively. Each ladder with a length of about 24 cm is equipped with 10 MAPS sensors mounted on Kapton cables.

The initial development path for the PIXEL detector included building a prototype detector with sensors providing 30 μm pixel pitch, analog readout, and integration time of 4 ms. This device would advance the PIXEL development even though it would have the integration time 20 times longer than what is required to operate at the expected RHIC peak luminosity of 8×10^{27} $cm^{-2}s^{-1}$ at the time of installation of the PIXEL detector. This paper describes the results of work done along this initial development path.

An integrated dose of several tens of krad per year of running of STAR was initially expected in the PIXEL inner layer. The most recent expectations range up to 300 krad and close to 10^{13} 1 MeV n_{eq}/cm^2 caused mostly by pions. An extensive study of MAPS resistance against ionizing and non-ionizing radiation has been performed in [7]. The brief discussion of radiation tolerance in this paper is limited only to ionizing radiation damage with respect to the early estimates of the dose.

III. MONOLITHIC ACTIVE PIXEL SENSOR TECHNOLOGY

The sensor technology of choice for the PIXEL detector is Monolithic Active Pixel Sensors (MAPS). MAPS are built using standard commercially available CMOS technologies. They integrate sensor and readout electronics in one silicon device. MAPS operation is based on charge collection from the active volume, which in this case, is epitaxial layer (typically about 10 μm thick) providing a 100% fill-factor. Only a small part of the active volume near the charge collecting n-well/p-epi diode is depleted. The charge collection process from undepleted regions is driven by thermal diffusion and typically gives a collection time on the order of 100 ns [8]. Potential barriers at the substrate and p-well regions limit the spread of the charge. The principle of operation of MAPS is presented in Figure 2.

MAPS offer competitive performance compared to the well established hybrid pixel and CCD technologies. MAPS can be readout faster than CCDs although not as fast as hybrid pixel sensors that take advantage of advanced, dedicated readout electronics. On the other hand, MAPS offer high granularity (with pixel size as small as several square micrometers) and limited sensor thickness that can not be matched by hybrid pixel

devices. Thinning of MAPS wafers and dies to several tens of micrometers is available as standard post-processing [9].

Modern CMOS processes with small feature size and thin oxide layers are, to some extent, inherently radiation tolerant giving MAPS an advantage over classical CCDs. At the same time, MAPS, unlike hybrid pixel devices, will suffer from bulk damage due to the limited speed of charge collection from the undepleted sensitive volume. The presented overall characteristics of MAPS make this technology an attractive solution for the PIXEL detector.

A limitation of the MAPS technology originates from the n-well/p-epi diode being used for charge collection. This imposes a restriction on the use of PMOS transistors in a pixel cell that would have to be implemented in another n-well, which would compete in charge collection with the main diode.

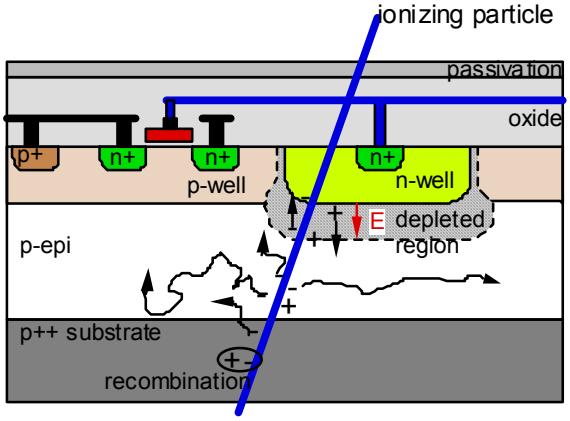


Figure 2. Cross-section through part of a MAPS pixel. Electrons generated in the epitaxial layer diffuse thermally until they are attracted to the n-well by the electric field in the limited depleted region.

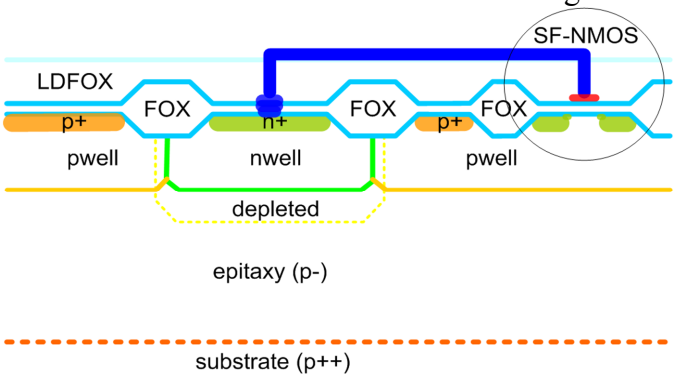
Since 1999 MAPS have been developed extensively at the IPHC [10] and elsewhere (e.g. [11,12,13]). The main application that has been driving the development is tracking of ionizing particles in high-energy physics experiments, with particular interest in application for vertex detectors for STAR, International Linear Collider (ILC) [14], and Compressed Baryonic Matter (CBM) [7]. Advantages of MAPS make them also very attractive devices in other domains, e.g. medical imaging and material science [15,16].

IV. MAPS DEVELOPMENT FOR STAR

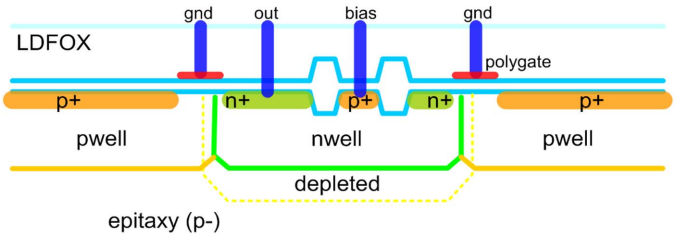
Enhanced radiation tolerance of MAPS

Part of the development of MAPS at IPHC dedicated to vertex detectors has been optimized for the PIXEL detector. The first family of sensors dedicated to the STAR application includes two prototypes: small size MimoSTAR2 with 128 × 128 pixel array, and MimoSTAR3 with 320 × 640 pixels (half of the final sensor). Both feature 30 µm pixel pitch and analog readout through fast (50 MHz) differential current drivers (2 parallel outputs in case of the larger prototype). Pixels are read out serially in a rolling

shutter mode that leads to an integration time of 4 ms for the final-size sensor with two parallel outputs. The sensors have been optimized for integration in a large detector system through implementation of a JTAG control interface that allows for setting internal configuration and internal reference currents and voltages.



a)



b)

Figure 3. Cross-section through a typical MAPS pixel in a 3T configuration, a), and through a charge collecting diode with enhanced radiation tolerance, b). The increased tolerance to ionizing radiation is achieved through a layout technique that eliminates thick oxide or Field OXide (FOX) from the perimeter of the diode. Thick oxide is not present in the areas with high doping and in places where gate oxide is located.

The PIXEL detector is expected to operate at relatively high temperatures due to limited capabilities of cooling based on air flow. Temperatures in the 20 to 30 °C range can be expected even with the moderate power dissipation at the design level of 100 mW/cm^2. In this environment the leakage current in charge collecting diodes will impact the noise performance of the sensors. The radiation environment will add to the increase of the leakage current resulting in degradation of the performance with time.

The typical charge collecting diode in MAPS is not well suited for operation in either high temperature or in a high radiation environment. The radiation tolerance of MAPS against ionizing radiation has been enhanced with a radiation hardened diode layout that is presented as a cross-section through a MAPS pixel in Figure 3 b) in comparison to the standard layout presented in Figure 3 a) [17]. The enhancement is obtained through elimination of field oxide from the periphery of the charge collecting diode. The thick oxide traps positive charges generated by ionizing radiation and the charge buildup near the Si-SiO$_2$ interface can lead to an inversion layer in a p-type substrate. This effect together with the Si-SiO$_2$ interface imperfections acting as

generation-recombination centers can increase surface leakage current. Thermally grown thick oxide in CMOS processes is used for isolation of highly doped transistor regions. Field oxide is absent over the highly doped areas and in places where gate oxide is located. The radiation tolerant diode in MimoSTAR prototypes is designed with gate oxide layer covering the periphery of the diode.

Test devices with both types of pixels were irradiated with Cobalt source. The leakage current change after a dose of 20 krad is shown to illustrate the radiation tolerance improvement. The increase of leakage current in the standard structure is presented in Figure 4 a) as a function of temperature. At 30 °C, and for the integration time of 4 ms, the noise performance is dominated by shot noise. The shot noise amounts to 12 and 39 electrons before and after irradiation with 20 krad, respectively. The measured improvement for a radiation hardened diode design is depicted in Figure 4 b). Significant reduction (by a factor of about 5) in the leakage current increase can be observed.

The electron noise charge performance of the radiation hardened diode is degraded initially by about 30% due to higher capacitance and slightly increased leakage current of this structure. However, at ionizing radiation doses greater than several krad, the performance of the radiation hard design is superior.

Both types of diodes were implemented in MimoSTAR2 for comparison purposes, while the MimoSTAR3 design features only the radiation hardened diode. The charge collecting diode in MimoSTAR prototypes uses the continuously reversed bias technique [17]. The operating point of the diode is continuously set with a forward biased p+/n-well junction created by a p-implant inside the n-well.

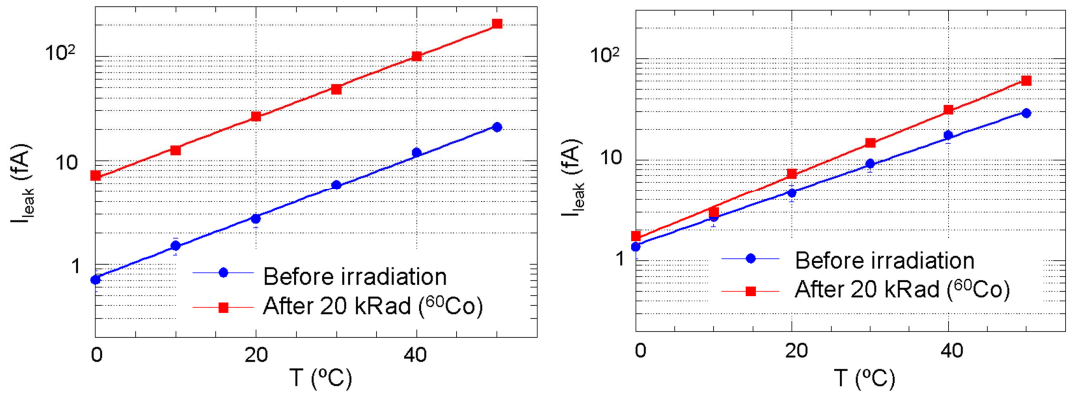


Figure 4. Leakage current measured for a standard, a), and radiation tolerant diode design, b), as a function of temperature. Small increase of leakage current after the ionizing dose of 20 krad presents a significant improvement with respect to the diode with the standard layout.

MimoSTAR2 has been extensively tested in the laboratory and with minimum ionizing particles from various test beams. A non-irradiated chip operated at the temperature of 30 °C and with the integration time of 4 ms, demonstrated electron noise charge, ENC, of 16 electrons and the single pixel S/N ratio for the most probable value of charge generated by a minimum ionizing particle of 14. The hit detection efficiency was

estimated at the level of 99.7 ± 0.06%. This provides sufficient performance for the PIXEL detector that requires detection efficiency above 99%.

Next generation of prototypes for PIXEL detector

The final PIXEL detector, scheduled to be deployed at STAR in 2012, will operate at high luminosities of RHIC II (8×10^{27} $cm^{-2}s^{-1}$). To avoid pile-up of consecutive events, integration times at the level of 200 μs are required. For large pixel arrays, the standard rolling shutter readout can not provide such a short integration/readout time. MAPS used for the PIXEL detector are going to implement column parallel processing with a discriminator at the end of each column and a data stream multiplexer for a fast binary readout.

A suitable structure has already been tested in Mimosa8 and Mimosa16 – small-scale prototypes developed at IPHC in collaboration with DAPNIA, CEA-Saclay, France. These prototypes feature in-pixel correlated double sampling (CDS) that allows subtracting two consecutive voltage samples to extract the signal accumulated within the integration time. CDS is implemented with a clamping capacitor. A detailed description of the operation of this chip can be found in [18]. The single threshold discriminator is located at the bottom of each column. In addition to the signal comparison to a reference voltage, it also minimizes pixel-to-pixel variations, referred to as Fixed Pattern Noise – FPN, by performing second CDS operation. The main part of the FPN is due to the in-pixel source follower mismatches. The suppression of the FPN is necessary for on-chip signal discrimination. The sensor architecture, which is presented in Figure 5, reduces FPN below the temporal noise level [18]. Temporal noise refers to the combined effect of shot noise, thermal noise, and 1/f noise, which are typically independent and add in quadrature.

Mimosa16 is an implementation of the Mimosa8 prototype in a technology with a thicker epitaxial layer (approximately 15 μm) [19]. It also features an improved in-pixel amplifier with a higher gain than the one implemented in Mimosa8 [20]. At 20 °C and with integration time of 50 μs, the detection efficiency for MIPS was close to 100% for a range of discriminator thresholds from 3 to 7 mV. At the same time, the accidental hit rate per pixel dropped from 10^{-3} to 10^{-6}. These numbers meet the performance goals for the PIXEL detector.

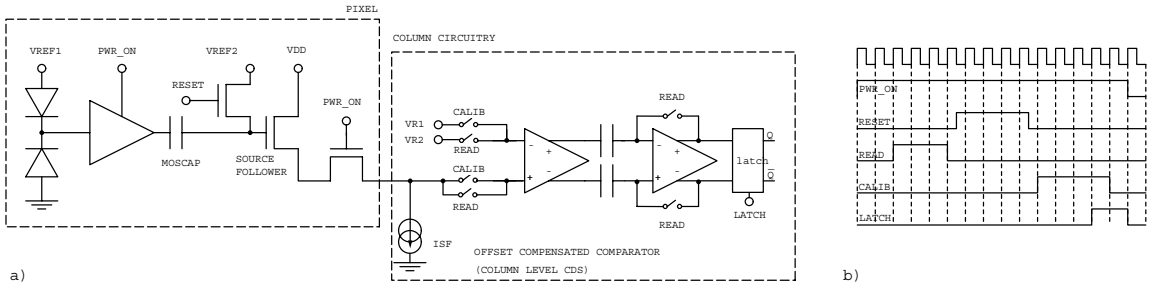


Figure 5. Schematic representation of a pixel and column circuitry in Mimosa8 and Mimosa16 prototypes, (a), and the timing pattern for pixel operation, (b). These prototypes have column parallel readout with a voltage discriminator located at the end of each pixel column. CDS, performed on a clamping capacitor, provides the difference between two consecutive pixel voltage samples, while CDS performed at the column level on the voltage discriminator stage reduces FPN of the sensor below the magnitude of the temporal noise.

V. LADDER STRUCTURE FOR PIXEL DETECTOR

The readout system for the PIXEL detector is designed to be modular with parallel independent ladder readout. The basic unit will be composed of a group of ladders.

An early ladder prototype is presented in Figure 6. The test readout cable was built from a Kapton cable with 4 copper conductor layers and populated with full-reticule size Mimosa5 prototypes. Four outputs per chip were routed to the edge of the ladder structure using only two conductor layers. The other layers formed ground and power supply planes.

Figure 6 Early prototype ladder quipped with MAPS. A Kapton cable with 4 copper conductor layers was used to route signals from/to sensors to the edge of the ladder. Analog buffers are visible at the edge of the ladder.

The next generation ladder will be designed differently. The readout buffers and drivers will be located at its end. Plans include using aluminum conductors to reduce radiation length of the structure. The signals will be sent to the readout system for processing, forming events, and inclusion into the STAR event structure.

VI. TELESCOPE AND PROTOTYPE READOUT SYSTEM

System architecture

A schematic diagram of the prototype readout system for the PIXEL detector is presented in Figure 7. At the time the readout system was designed, only the smaller of the MimoSTAR prototypes was available for testing. The readout system has been coupled to a three sensor telescope head constructed with MimoSTAR2 prototypes. All sensors operate in parallel with synchronized frame readout. The telescope assembly is connected to the motherboard and routed to a daughter card that performs digitization and processing of data. Data processing consists of CDS and an on-the-fly data reduction accomplished with a hit finding algorithm that returns only addresses of cluster central pixels. Resulting addresses are formed into events and buffered in a commercial Altera Stratix field programmable gate array (FPGA) development board. The Stratix board interfaces to a fiber optic readout system and sends data to an acquisition PC. It also provides JTAG communication with the telescope head. A circuit on the motherboard supplies latch-up protected power, clocks and resets to the telescope.

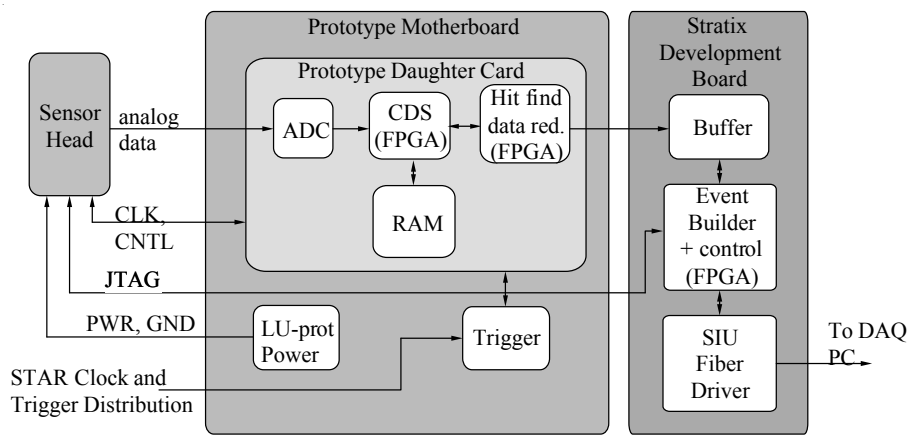


Figure 7. Functional block diagram of the prototype PIXEL readout system.

The system is run continuously with a 50 MHz clock sent to sensors. The motherboard/daughter card assembly accepts external triggers. In response to a trigger, hit data corresponding to one, full-frame sensor readout are transferred to the acquisition PC.

The prototype readout system presented in this paper is a small-size prototype developed for the PIXEL detector. The architecture can be scaled up to provide parallel modules for the full-size detector.

Hardware implementation

MimoSTAR2 sensors are designed to mimic a larger sensor by adding dummy pixels to give an apparent size of 128×640 pixel array. The full die thickness sensors are mounted to two-layer Kapton flex cables with a total thickness of 50 μm. Flex cables are glued to aluminum frames that define the telescope geometry with a planar spacing of 2.7 mm as shown in Figure 8.

The daughter card is a small printed circuit board containing an 8-channel, 12-bit ADC (TI ADS5270), Xilinx XC2V100 FPGA for signal processing, and two 18 Mb GSI GS8162Z72C SRAM modules that store signal samples for CDS.

The motherboard provides regulated power, control, and configuration to the sensors, accepts external triggers, and provides interconnections between the sensor head, the daughter card, and the Stratix development board.

The Stratix development board is the interface to the fiber optic data transmission module that connects the readout system and the acquisition/control PC. It also provides logic for sensor JTAG communication, event building, and buffering. The fiber optic module is a Digital Data Link interface that has been developed at CERN for the ALICE detector [21] and has been chosen as the readout system for most of the current STAR upgrade. It provides data transfer rates from the detector system to a PCI bus in an acquisition PC up to 1.2 Gb/s.

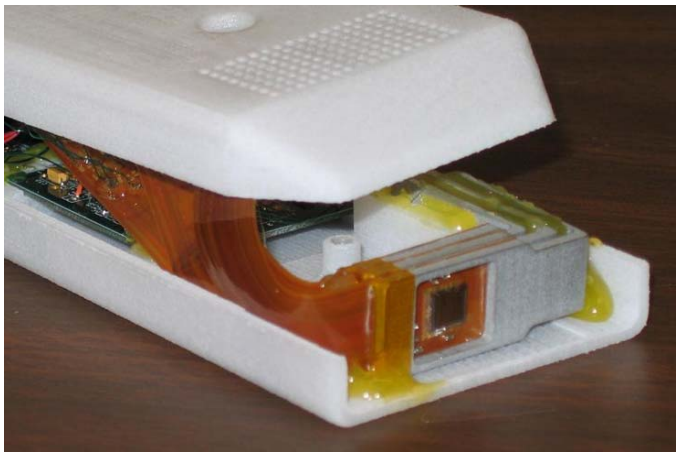


Figure 8. Picture of three sensor telescope constructed with three MimoSTAR2 sensors. Kapton cables provide connection between sensors and control/readout electronics located on a readout PCB. The telescope was enclosed in a plastic housing head.

Data processing in FPGA

Analog differential current signals from the MimoSTAR2 sensor are converted to a voltage and continuously digitized with a 50 MHz clock. Digitized data are synchronously passed to the SRAM modules. The memory is configured as an updating array of 12-bit ADC values, where each entry corresponds to the physical sensor pixel. One sensor frame for each chip is continuously present in memory. The ADC value of a current pixel signal is subtracted from the value registered in the previous frame. The CDS subtraction allows extracting signals generated by passing ionizing particles, and at the same time removes FPN. The subtraction is performed at the main system clock frequency of 50 MHz. The current ADC sample overwrites the previous one. The result of subtraction, reduced to an 8-bit value, is passed to the next stage that performs data reduction through a real-time hit finder.

To prepare the data for hit finding, the multiplexed serial data output stream from the sensor is reordered to reflect the geometrical pixel arrangement. This permits a simple implementation of a 3×3 pixel window scan across the chip that steps at the clock frequency. The implementation of the hit finding algorithm is presented in the diagram in Figure 9.

Two full rows and three additional pixels are input into a shift register. The threshold criteria applied to each cluster require the central pixel to pass a high threshold and one of the eight neighbors to be above a lower threshold. This algorithm has an efficiency and accidental rate comparable to the classical cluster finder that uses a high central pixel cut and a cut on the 9 pixel sum. When the cluster criteria are met, the 18-bit address of the center pixel is sent to an event FIFO.

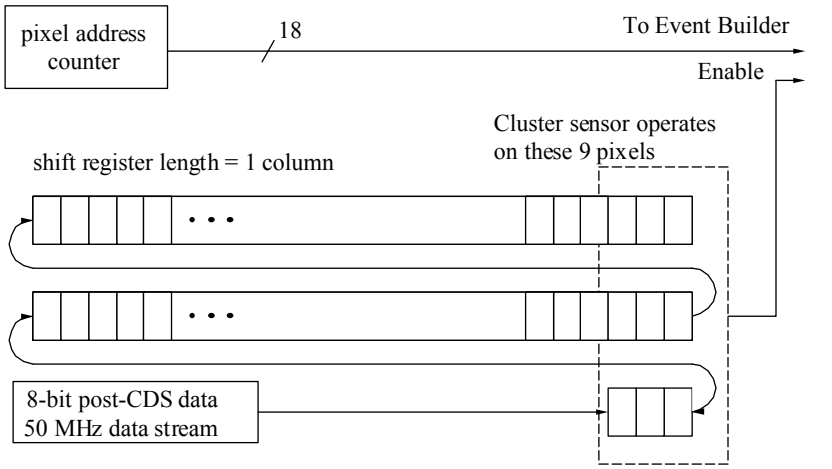


Figure 9. Schematic representation of the hit finder algorithm implemented in the prototype readout system for the PIXEL detector. The algorithm allows performing zero suppression at the FPGA level. 12-bit ADC data from the two full rows and the additional 3 pixels from the next row are sent to a high/low threshold discriminator. The center pixel is compared to a high threshold and the surrounding 8 pixels with a lower threshold. If the center pixel and one of the 8 neighbors exceed their thresholds, then a hit is found. The address of the central pixel is the position of the hit and stored into a readout FIFO.

A trigger from the STAR trigger system enables the event FIFO for a time window equivalent to readout of one sensor frame. In response to the trigger, after closing FIFOs for each sensor, the addresses are bundled with a received trigger ID, built into an event structure, and transferred to a STAR DAQ receiver PC.

To handle triggers that arrive randomly, with a mean frequency of 1 kHz, four FIFOs are implemented for each sensor. When the first trigger arrives, data is transferred to the first FIFO. If another trigger arrives before the readout is finished, then data is also transferred to the next FIFO. Dead time only arises when all the FIFOs are active. This architecture can easily be expanded by increasing the number of FIFOs if system dead time becomes a problem.

The raw data rate from the telescope is 225 MB/s with an average occupancy of 20 hits per sensor per frame. The average readout frequency is 1 kHz. The zero suppression algorithm, which has some event structure overhead, reduces the data rate to about 612 kB/s. For the full PIXEL detector system this would correspond to a reduction from about 51 GB/s down to about 114 MB/s.

VII. TEST RESULTS WITH THE PROTOTYPE TELESCOPE SYSTEM

The assembled telescope and the prototype readout system were calibrated with a ^{55}Fe source. The ENC was estimated at the level of 30 and 35 electrons for the standard and radiation tolerant diode designs, respectively. This noise has a much higher value than measured earlier with another dedicated sensor test board (11 to 15 electrons at ambient temperature of about 28 °C).

The high noise value is attributed to the method used for mounting chips on the flex cable. The MimoSTAR2 prototype features a large number of signal outputs intended only for testing purposes. When the telescope system was designed, the layout of the Kapton flex cables was optimized for minimum size and minimum mass as needed for the final detector architecture. As a result, there were not enough lines and some of

the chip's output pads were left un-bonded. It has been verified that leaving a set of un-terminated DAC outputs prevented proper stabilization of internal reference voltages and was responsible for the measured increase in the noise level.

The system was first tested with a 1.2 GeV electron test beam at the Advanced Light Source (ALS) at LBNL and then in the STAR detector at RHIC during the 2006-2007 Au-Au run. The results presented below focus on the overall performance of the complete system and do not include detailed characterization of the MimoSTAR2 prototype.

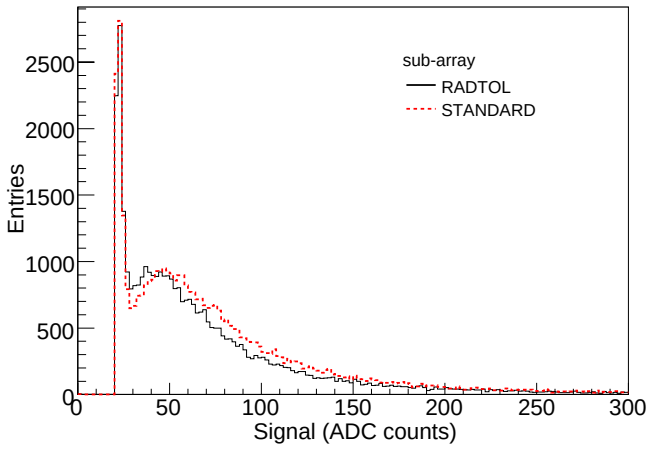


Figure 10. Single pixel signal distributions measured with the telescope in a 1.2 GeV test electron beam at LBNL ALS. The Landau shaped spectrum for the standard and radiation tolerant diodes is presented.

Tests at the ALS revealed that in the enclosed telescope head the performance of sensors degraded moderately, most likely due to higher operating temperature, to about 34 and 38 electrons for the standard and radiation tolerant diode, respectively. The test beam intensity was adjusted to provide only several hits per sensor in 1.7 ms readout time. An example of the measured single pixel distribution for signals from 1.2 GeV electrons is presented in Figure 10. Signals passing the cut of 20 ADC counts, equivalent to approximately three times the mean noise value, in cluster central pixels are plotted. The peak at the left-hand side represents noise. The observed most probable value of signal in the Landau shaped distribution (MPV) is at 49 and 43 ADC counts for standard and radiation tolerant structure, respectively. The standard diode has a smaller input capacitance and, therefore, a higher gain. Using conversion gain known from the ^{55}Fe calibrations (G_{STD} = 4.7 e-/ADC, G_{RAD} = 5.5 e-/ADC), the MPV is measured to be approximately 230 electrons. The cluster size distribution is characterized by the mean value of 1.6 pixels for the cuts of approximately 3.5 and 2 times the mean noise value in the central and neighboring pixel, respectively.

The telescope head was assembled without a very precise control on the alignment of all three sensor layers. The final alignment was performed in software by searching for straight tracks from the electron test beam that passed through all three layers. The correlations between hit locations in all three layers revealed shifts between

sensors. The largest offset was about 340 μm and one sensor plane was rotated with respect to other planes by about 25 milliradians.

The fully tested and calibrated system was mounted inside the STAR detector for the last three weeks of the 2006-2007 run. The sensor head was placed near the beam interaction point with the sensor plane approximately perpendicular to the beam axis. The final location of the telescope head was about 5 cm below the beam pipe and about 145 cm from the center of the interaction region. The electronics box containing the prototype readout system was located inside the STAR magnet pole tip, at approximately the position expected to be used for the final PIXEL detector electronics. The whole assembly operated in the nominal STAR magnetic field at 0.5 T.

The goal of the test was to measure the performance of the telescope system in the STAR environment, check for environmentally induced noise, to measure the charged particle density in STAR, and to do limited tracking. Integration of the system with the STAR control and trigger subsystems was an important milestone. The telescope with the readout system was integrated with STAR DAQ trigger, run control, and slow control. The data stream was delivered to the DAQ standard readout PC but was not collected by the STAR event builder.

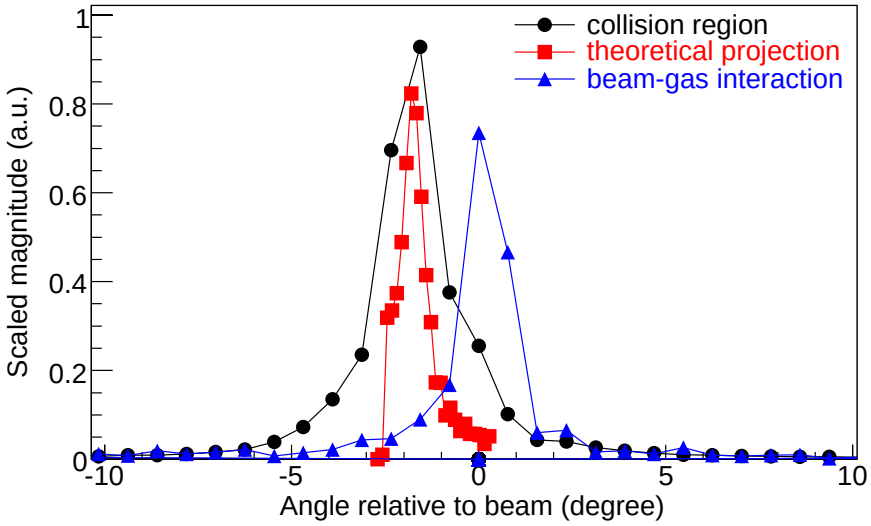


Figure 11. Angular distribution of tracks registered with the telescope in the STAR environment. The angular distribution of tracks measured during normal triggered data acquisition is shown. It is compared with a calculated distribution corresponding to the beam interaction diamond at STAR. The angular distribution of background tracks was obtained in a special run in which RHIC beams were displaced not to collide in the interaction region.

Noise performance measured in the STAR environment was comparable to the results from laboratory and ALS tests. However, it is possible that the overall noise performance of the telescope assembly might have masked some small environmentally induced noise increase. The charged particle density observed with the 1.7 ms integration time was about 3.9 hits per sensor. The average luminosity during the time the telescope was at STAR was 8×10^{26} $cm^{-2}s^{-1}$.

Data taken during the normal STAR operation included background tracks, the majority of which can be expected to originate from the beam-gas type interactions, and charged particle tracks originating at the collision point. The known distribution of collision point locations inside STAR can be geometrically projected into the prototype telescope. The result of this projection, neglecting scattering in the beam pipe material, is shown in Figure 11 and compared with measured data. The angular distribution of registered straight tracks passing through the telescope peaks at approximately two degrees and agrees with the projection. The measured distribution is wider, which we attribute to scattering in the beam pipe. For a short run the RHIC particle beams were displaced and did not collide in the interaction region. The measured angular distribution of the background tracks, which have a significantly lower density, peaks at zero degrees showing tracks parallel to the beam pipe. All curves in the plot are scaled arbitrarily to highlight the angle measurements.

VIII. CONCLUSIONS

A preliminary readout system design for the PIXEL vertex detector at STAR has been presented. This system is a small scale prototype that includes all features necessary for a module of the final detector.

We have successfully tested the prototype readout system together with the 3-sensor telescope assembly at a continuous 50 MHz readout with on-the-fly data sparsification that gives nearly three orders of magnitude data flow reduction from the raw ADC rates.

The system works well providing reasonable detection efficiency and accidental hit rates. Simple tracking has been performed and lead to imaging of the interaction diamond and beam-gas background.

Stable noise level throughout all tests, and in particular at STAR, validates the system's electronics design.

The integration of the system with the STAR control and trigger subsystems has been a major achievement allowing the prototype telescope system to function as a part of the STAR detector.

The presented system will need to be slightly modified when the second generation MAPS prototypes become available. The signal processing will be shifted to the on-chip electronics simplifying the readout system architecture. However, multiple event buffering, event building and possibly on-the-fly cluster reconstruction will still be implemented in the system's FPGAs.

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