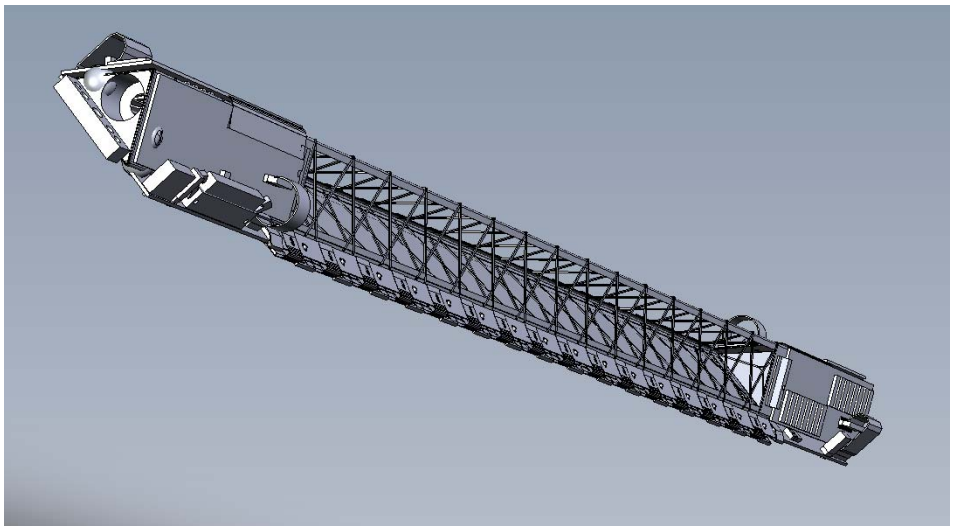
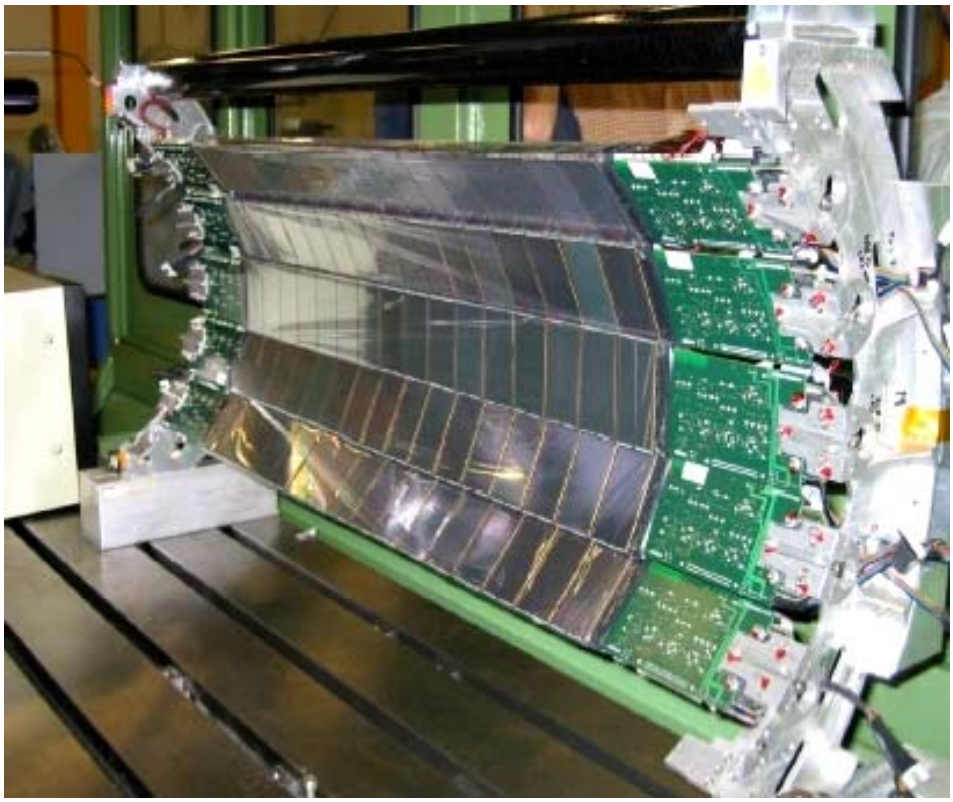
A Proposal to Upgrade the Silicon Strip Detector





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A Proposal to Upgrade the Silicon Strip Detector

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1. Executive Summary

The STAR Silicon Strip Detector (SSD) was built by a collaboration of Nantes, Strasbourg and Warsaw collaborators. It is a beautiful detector; it can provide 500 μm scale pointing resolution at the vertex when working in combination with the TPC. It was first used in Run 4, when half the SSD was installed in an engineering run. The full detector was installed for Run 5 (the Cu-Cu run) and the operation and performance of the detector was very successful. However, in preparation for Run 6, two noisy ladders (out of 20) were replaced and this required that the SSD be removed from the STAR detector. The re-installation of the SSD was not fully successful and so for the next two Runs, 6 and 7, the SSD suffered a cooling system failure that allowed a large fraction of the ladders to overheat and become noisy, or fail. (The cause of the SSD cooling failure was rather trivial but the SSD could not be removed betweens Runs 6 and 7 due to the inability of the STAR detector to roll along its tracks at that time.)

The SSD was removed from STAR in the summer of 2007 along with the Silicon Vertex Tracker (SVT) in preparation for the low mass run to study the effectiveness of identifying non-photonic electrons with the TPC, alone.

We propose to reinstall the SSD in Run 9 (the Au-Au run with TOF), utilize it in Run 10 (the low energy scan), and to upgrade it to DAQ1000 specifications in time for Run 11.

The motivating factors in favor of the upgrade include:

- Improve the reconstructable yield of the strange mesons and baryons; especially the K, Λ, Ξ, and Ω.
- Improve the invariant mass resolution for resonances and spectra measurements
- Improve single track high p_T resolution by approximately a factor of 2
- Preserve the manpower and restore the performance of the SSD because it is essential for the HFT upgrade (~$16 M). The HFT project needs to know as soon as possible that the SSD is a success so that it can move ahead with confidence and keep its costs under control. A new replacement for the SSD would be prohibitively expensive.

The required maintenance and upgrades, which must be in place before each run begins, include the following items:

Run 9
- Redesign and replace the cooling system
- Fix the Level 2 abort problem

Run 10
- Upgrade 3 ladders (one sector) of the SSD readout electronics to 1 kHz

Run 11
- Upgrade all of the SSD readout electronics from 200 Hz to 1 kHz

In addition, there are several smaller tasks such as sending the ladders back to SUBATECH for repair prior to Run 9, modifying the East and West TPC cones, and upgrading the slow controls system in concert with the installation of one sector of the upgraded SSD for Run 10. These activities are discussed more fully in section 4.

This proposal discusses the motivation for reinstalling the SSD, gives a status report on the technical progress towards upgrading the detector, and includes an estimate of the cost and schedule for performing the upgrade. All labor for the upgrade will be contributed by the participating institutions except the US technical effort. In particular, the engineering effort to design and fabricate the boards for the electronics upgrade will be contributed by SUBATECH as long as the money for hardware purchases can be exchanged in a timely manner. Therefore, the majority of the costs reported in this proposal are for hardware items, alone.

2. Introduction and Motivation for the Upgrade

The STAR Silicon Strip Detector (SSD) is a high resolution Si detector which is mounted inside STAR at a radius of 23 cm. It has the same ϕ and rapidity coverage as the TPC meaning that it offers full 2π azimuthal coverage and covers a pseudo rapidity range of |eta| < 1.2. Its radial location puts it midway between the event vertex and the TPC and so it is ideally suited for the purpose of improving the TPCs pointing and momentum resolution; and extending its physics program.

The SSD yields a highly accurate space point with a resolution of 30 μm in the R-ϕ direction and 850 μm in the Z direction[1,2]. This is a considerable improvement over the resolution of the TPC pointing at the SSD (which is greater than 1 mm in both directions) and so enhances the overall pointing resolution at the vertex. The excellent resolution of the SSD is achieved by using double sided Si with crossed strips; (i.e. with strips on both sides of the same piece of Si). Because of this unique double-sided feature, the SSD is a thin detector and is only ~1% radiation length thick. Thus, it can be used to tag non-photonic electrons while generating a minimum amount of background.

The excellent resolution of the SSD, and its ideal location, means that it is suitable to extend and improve the full physics program in which the TPC can participate. For example, the SSD improves the single track DCA resolution at the vertex from a few mm (at 1 GeV) to less than 1 mm in the R-ϕ direction without using a vertex constraint[3]. See Figure 1.

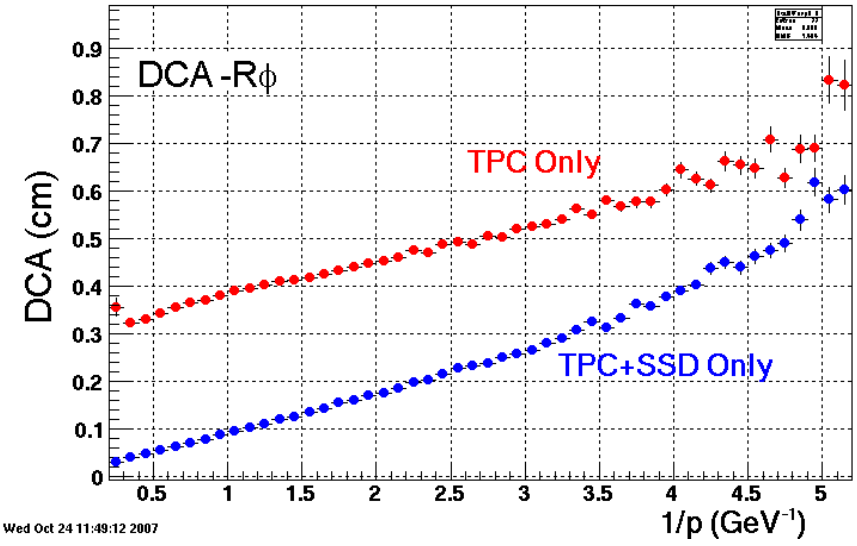

Figure 1: The DCA resolution of the TPC and the SSD versus the inverse momentum of the track. The top line shows the DCA resolution of the TPC, acting alone, for all tracks entering the TPC (i.e. no track cuts) during the high intensity Cu-Cu run at RHIC. The bottom line demonstrates how the pointing resolution of the TPC can be improved by including the SSD hits on tracks. The results are quoted for 200 GeV minBias Cu-Cu collisions with $|Z_{vertex} < 5$ cm| and $|\eta| < 1$. This work is from the thesis of Jonathan Bouchet (SUBATECH, Nantes).

The improved pointing resolution provided by the SSD will yield important improvements in the reconstructable yield of neutral and charged particles that decay within a few cm of the event vertex; in particular the strange mesons and baryons (K, Λ, Ξ, and Ω). Figure 2 shows a sample of K^0 mesons measured in the Cu-Cu beam with and without the use of the SSD. The improved signal to noise ratio (due to the improved background rejection) for the detection of baryons, mesons and resonances, will be important in our upcoming heavy ion runs and especially in the proposed low energy scan, where the integrated luminosity (and thus statistics to tape) will be limited.

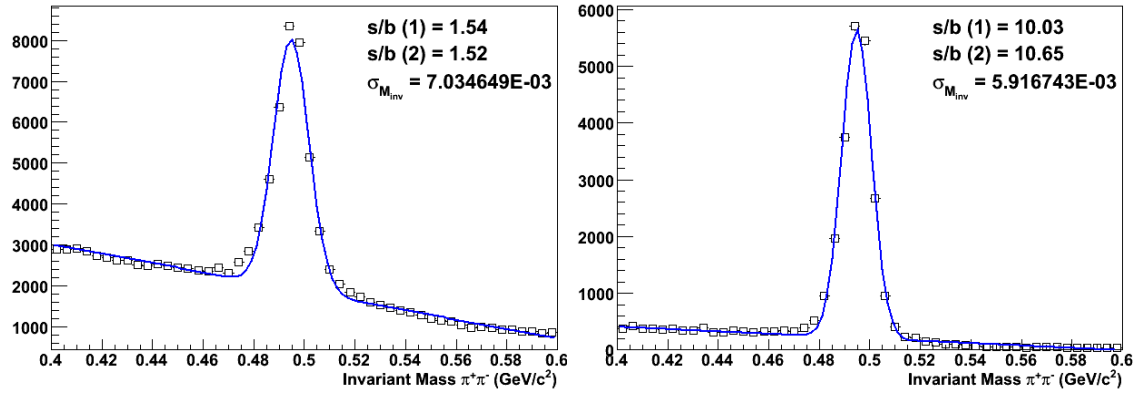

Figure 2: K^0 spectra for the high intensity Cu-Cu run at 200 GeV. The left panel shows the reconstructed K^0s using the TPC alone. The right hand panel shows a factor of six improvement in the signal to noise ratio when the SSD hits are included in the track fit. From the thesis of Jonathan Bouchet.

Figure 3 shows that the SSD is also important to the heavy ion and p-p physics program because it improves the TPC momentum resolution by a factor of 2 at high p_T. As a result, it improves the invariant mass resolution for resonances that decay into multiple charged particles (eg. φ(1020), Λ). The improvement in momentum resolution can be achieved on a track by track basis and does not require a beamline or vertex constraint to achieve these results.

The improved momentum resolution will be useful in a future program of intermediate to high p_T hyperon measurements at STAR. For example (anti-)Λ production whose longitudinal spin transfer is sensitive to the helicity distribution function of strange quarks in the nucleon[4]. Figure 4 shows a Monte Carlo simulation of high p_T Λ spectra that can be observed in polarized p-p collisions at RHIC. There is a cut on the data to ensure that the Λ decays inside the SSD radius. The simulations[5] show that the width of the peak is improved substantially when the SSD is included in the tracking algorithm. It should be noted that an increasing fraction of Λ decay at radii larger than the SSD radius as p_T increases. (The two panels in the figure are different simulations and have a different number of events thrown in each simulation. The reader should focus on the width of the peaks as a measure of the improved quality of the tracking.)

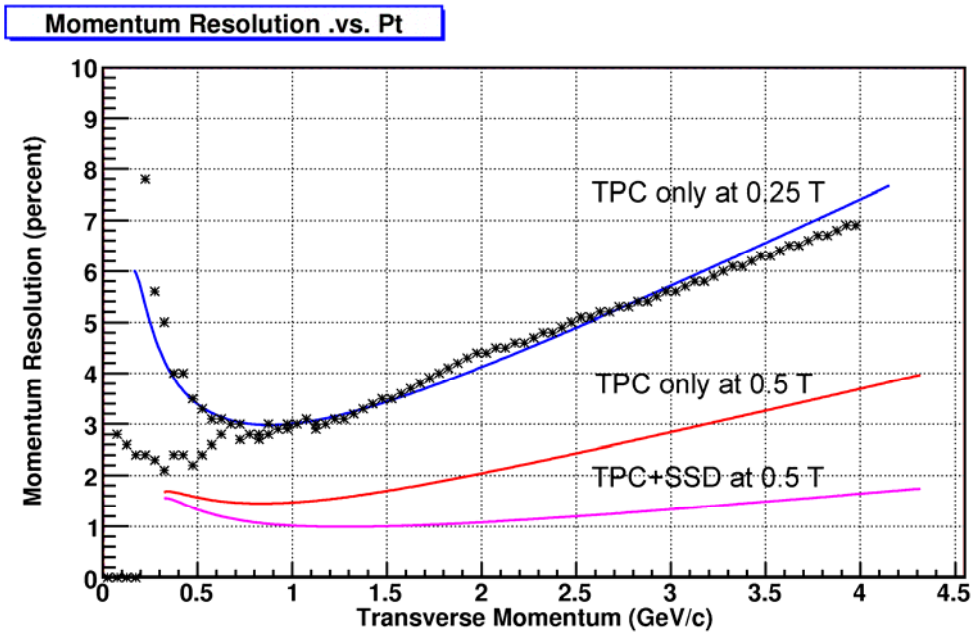

Figure 3: Data compared to simulated momentum resolution of the TPC and SSD detectors in STAR. The data points show a superposition of measured pion and antiproton spectra[6] at 0.25 Tesla in the STAR TPC. The blue line (top) is the simulated 0.25 Tesla p_T spectrum for anti protons, while the red (middle) and pink (bottom) lines show the simulated momentum resolution for the TPC and TPC+SSD at 0.5 T, respectively. The SSD improves the momentum resolution at high p_T.

The SSD is also a relatively fast detector and so it is only sensitive to tracks for 1.5 μs whereas the TPC is sensitive to tracks crossing its fiducial volume for 36 μs. This is important in p-p collisions where multiple events pile-up in the TPC and these piled up events must be distinguished on an event by event and vertex by vertex basis. The SSD can help to resolve the ambiguities due to multiple vertices because there is no appreciable pile-up in a fast Si detector, even for p-p collisions at 500 GeV.

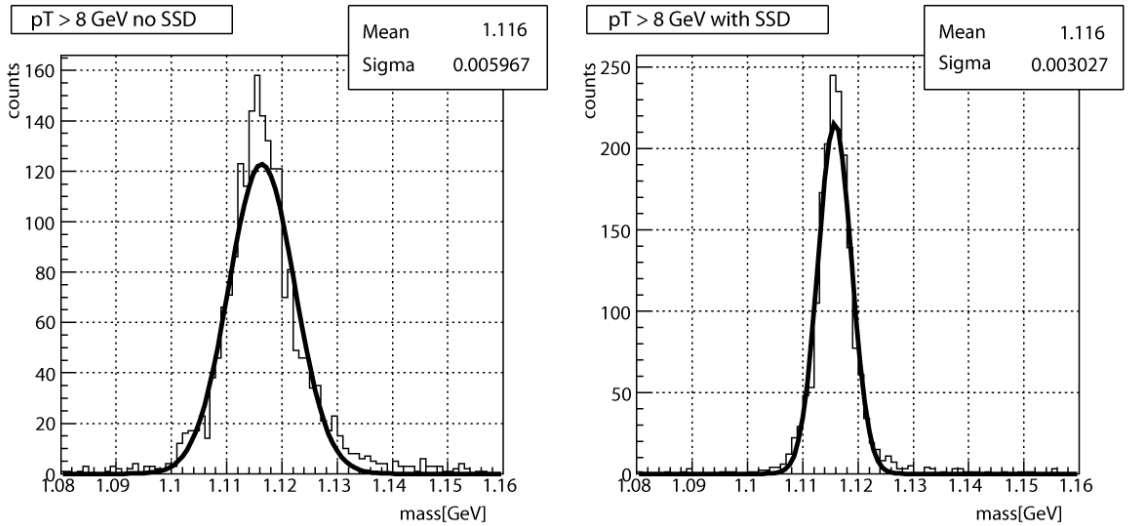

Figure 4: Simulated high p_T Λ spectra using the TPC alone (left panel) or the TPC+SSD (right panel) at 0.5 Tesla. The statistics boxes in each panel document the improved width of the peak when the SSD is included in the tracking algorithm. The simulations were performed by Qinghua Xu.

Finally, the SSD is an integral part of the proposed Heavy Flavor Tracker (HFT) upgrade. The HFT will extend the STAR physics program into the charm (and beauty) sector by enabling the direct topological reconstruction of open charm (and beauty). The critical elements in the HFT are the PIXEL detector layers that will be mounted at 2.5 cm and 8.0 cm radius, respectively. These inner layers are segmented into 30 μm x 30 μm pixels and so yield 9 μm resolution at each layer. However, it is not a simple task to match the projected TPC tracks onto the pixel layers. Matching a track from the TPC with a hit on the pixel layers will require highly efficient intermediate tracking and graded resolution from the outside going in. The SSD sits at an ideal location, with excellent performance characteristics, to be a critical element in the track matching algorithm for the HFT.

Table 1 shows a self consistent simulation of the pointing resolution of the HFT detector sub-system at various points along the path of a kaon as it is tracked from the outside going in towards the event vertex.

Graded Resolution from the Outside - In		Resolution(σ)
TPC pointing at the SSD	(23 cm radius)	~ 1 mm
SSD pointing at IST-2	(17 cm radius)	~ 330 μm
IST-2 pointing at IST-1	(12 cm radius)	~ 225 μm
IST-1 pointing at PIXEL-2	(7 cm radius)	~ 200 μm
PIXEL-2 pointing at PIXEL-1	(2.5 cm radius)	~ 70 μm
PIXEL-1 pointing at the vertex		~ 40 μm

Table 1: A calculation of the pointing resolution of the TPC+SSD+IST+PIXEL detectors at intermediate points along the path of a 750 MeV kaon as it is tracked from the outside – in. Good resolution at the intermediate points is needed to resolve ambiguous hits on the next layer of the tracking system.

A more detailed look at the resolution of the HFT system is described in the HFT proposal[7]; and an important figure from that proposal is shown in Figure 5. The top panel shows the r-ϕ pointing resolution and the bottom panel shows the z pointing resolution at different places in the system. The beam pipe is included in the calculations. Due to the different geometry of the detectors, the r-ϕ and z resolutions are different in different places but, typically, the average pointing resolution improves for layers at smaller radii.

The red line (top) in Figure 5 shows the simulated pointing resolution of the TPC (acting alone) at the vertex, while the black line shows the pointing resolution of the TPC onto the SSD. The pointing resolution onto the SSD is better than at the vertex because the SSD is closer to the TPC.

The remainder of Figure 5 is devoted to showing the pointing resolution of the system at each layer of the system. A detailed examination of the figure shows an alternating pattern of improvement in the resolution of the system of proposed detectors. For

example, the SSD detector has an asymmetric resolution of approximately 30 μm in the r-ϕ direction and 850 μm in the Z direction. The resolution of the TPC+SSD pointing at IST2 is shown by the green line in the figures. The r-ϕ and z resolution are also different for the proposed IST detectors; so for example, IST2 has a resolution of approximately 11,500 μm in the r-ϕ direction and 17 μm in the z direction. The yellow line in the figures shows the resolution that can be achieved by the TPC+SSD+IST2 pointing at IST1 and, because of the underlying characteristics of each detector, the ordering of the yellow and green lines are reversed in the two panels of the figure. The same story plays itself out for IST1 (magenta line), but the figure returns to a simply ordered pattern with the addition of the PIXEL layers because these detectors are symmetric systems with 9 μm resolution in both directions.

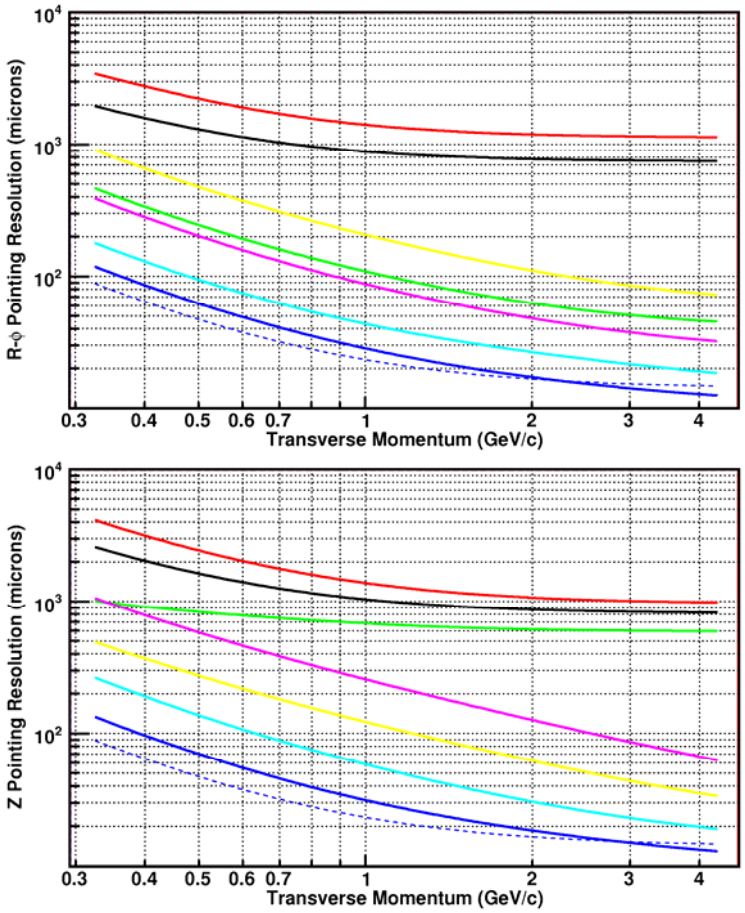

Figure 5: The simulated pointing resolution of the HFT detector system (σ); where the r-ϕ and z pointing resolutions are plotted separately (top and bottom, respectively). The calculations assume a kaon passing through the system. The pointing resolution of the TPC onto the vertex is shown by the red line. The pointing resolution of the TPC onto the SSD is shown by the black line. The TPC+SSD pointing at IST2 is shown in green. The TPC+SSD+IST2 pointing at IST1 is yellow, TPC+SSD+IST2+IST1 pointing at PIXEL2 is magenta, TPC+SSD+IST2+IST1+PIXEL2 pointing at PIXEL1 is cyan, and the full system TPC+SSD+IST2+IST1+PIXEL2+PIXEL1 pointing at the vertex is blue. The blue dashed line is the theoretical limit; it shows the idealized HFT performance without beam pipe or other sources of MCS.

The net effect of the increased pointing resolution that is delivered by the SSD is that it increases the efficiency for reconstructing a D^0 meson by at least factor of 2.

In addition, the SSD is also an important element in the alignment and calibration of the TPC because it has different systematic errors than the TPC (e.g. no distortions due to spacecharge or gridleak). As the SSD has a different spatial symmetry from the TPC, it is very useful for aligning the two halves of the TPC. It provides an independent measurement to assure that the TPC is operating at its expected resolution. Thus the theoretical efficiencies described above could not be achieved in practice without the extra benefit of the SSD as a calibration device.

In conclusion, the SSD is an important element in designing an efficient tracking system for the HFT because the efficiency of reconstructing heavy flavor mesons will increase by more than a factor of 2 and it will insure that the TPC will be performing at its optimum level

3. The SSD – A brief overview of the hardware

The SSD enhances the tracking capabilities of the STAR experiment by measuring accurately the two-dimensional hit position and energy loss of charged particles. It aims specifically at improving the pointing resolution of TPC tracks at the vertex (or at the proposed inner Si layers of the HFT). As a result, STAR's tracking *efficiency* is significantly improved by the SSD. The SSD resides at a distance of 23 cm from the beam axis, it covers a pseudorapidity range of $|\eta| < 1.2$, and it has a total silicon surface of about 1 m^2.

The SSD will be the outermost Si layer in support of the proposed Heavy Flavor Tracker. It is also the only *existing* device proposed for that detector. It will be installed between IST-2 and the TPC. Its relation to the HFT can be viewed in Figure 6.

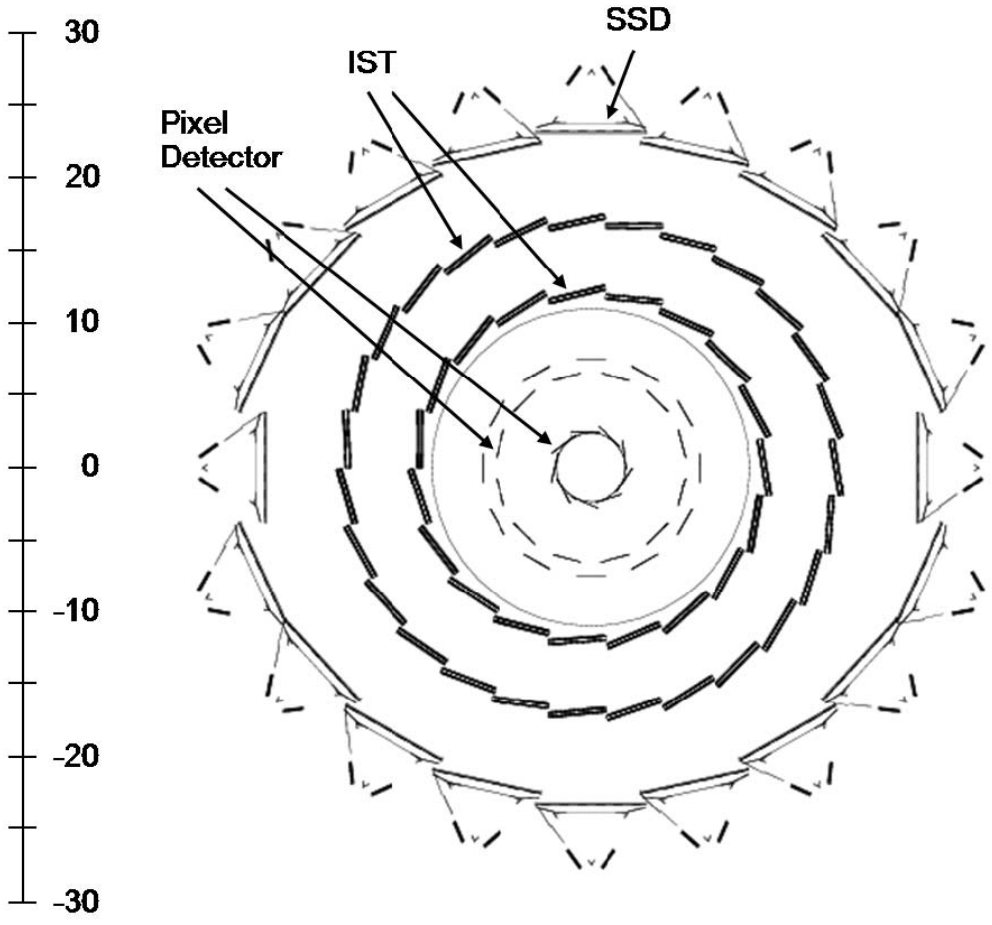

Figure 6: The SSD is shown surrounding the proposed inner silicon tracking layers of the HFT.

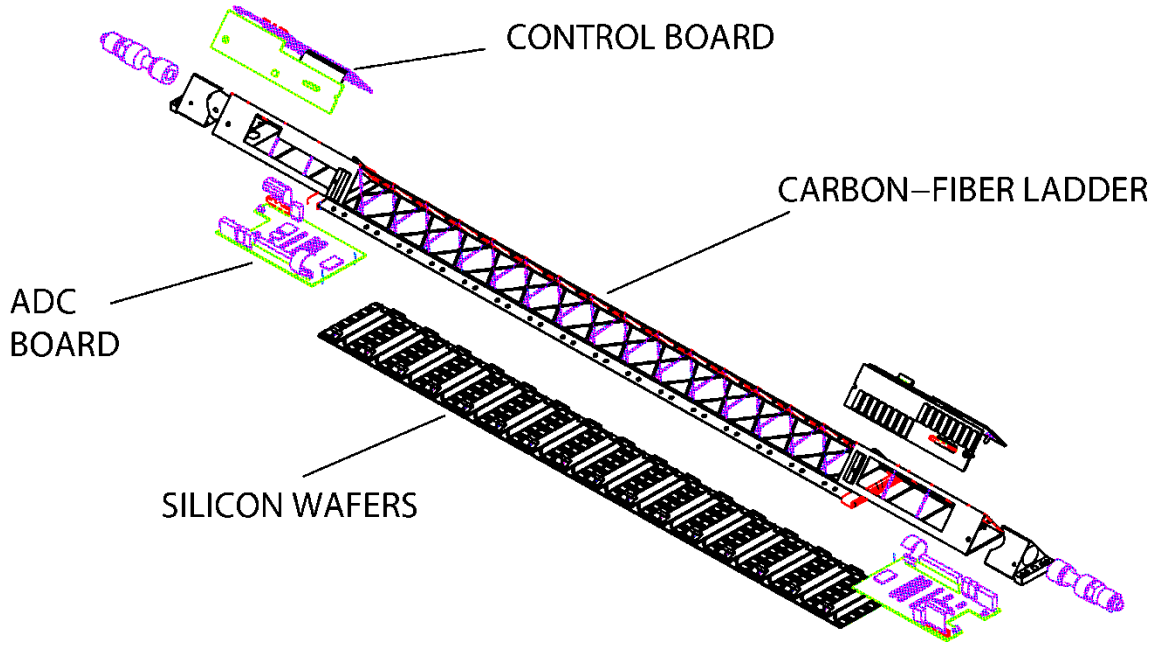

Figure 7: An SSD ladder showing its various components.

The SSD is divided mechanically into four sectors. Two sectors support 3 carbon fiber ladders, each, while the other two sectors support 7 ladders. (The photo on the cover of this proposal shows 5 ladders mounted on a sector, with two still to be installed.) One ladder is shown in Figure 7. Each of the ladders contains 16 wafers using double-sided silicon strip technology (768 strips per side). The total radiation length of each ladder is approximately 1%. The wafers are connected to the front-end electronics (six ALICE 128C chips per side) by means of the Tape Automated Bonded (TAB) technology. These ladders are tilted with respect to their long axis, allowing the overlap of the detectors in the transverse plane for better hermeticity and alignment. Two cable busses, one per side of the Si wafers, transport the analog signals along the ladder to a 10-bit ADC board which are installed at each end. After digitization, the signals are sent to Readout Boards, which are linked to the DAQ system through Giga-link optical fibers.

3.1 Overview of the existing readout electronics

A schematic view of the existing electronics readout chain can be seen in Figure 8. The SSD is capable of running at 200 Hz. The basic unit of electronics is a set of ten ADC boards which are daisy chained to feed one readout board (RDO). Since each of the twenty ladders has two ADCs, a total of four RDO boards are used to digitize the output of the full detector.

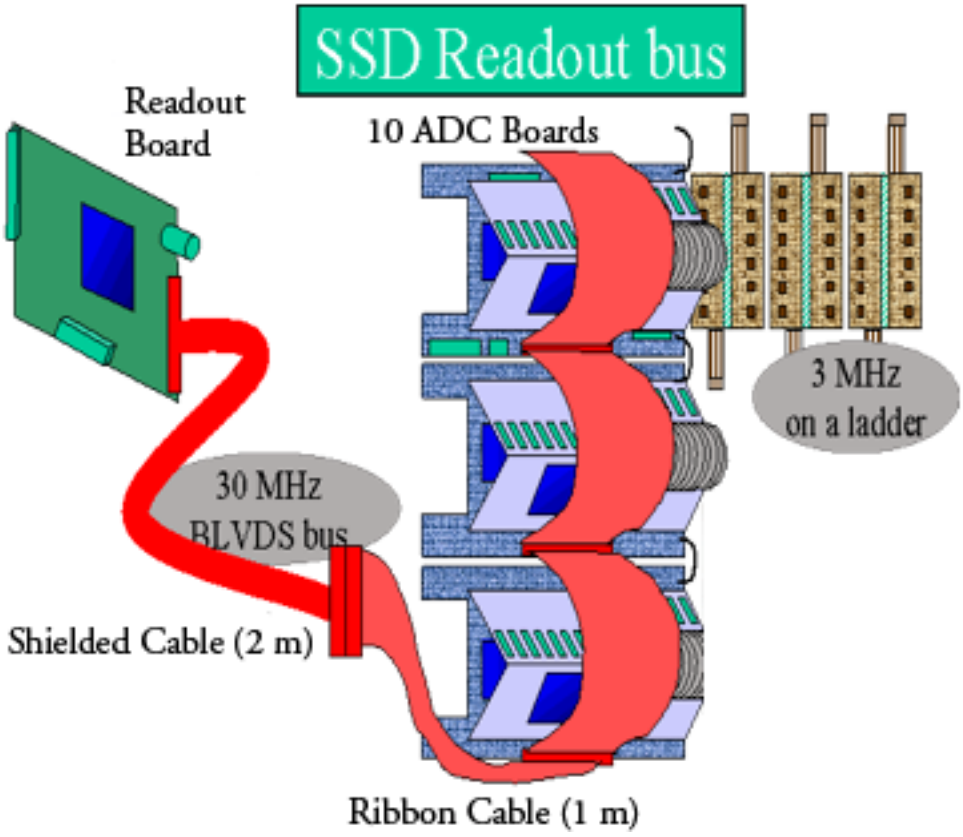

Figure 8: Module layout of the electronics.

The existing FEE electronics runs at a 3 MHz clock rate and, because there are 768 strips per wafer and 16 wafers per ADC Board, it takes 4.1 ms to read a ladder into the ADC Board. Each RDO, which runs at 30 MHz, controls ten ADC boards. Therefore, it takes a similar time, 4.1 ms, to read out each RDO. Due to the desire to match the TPC format and length, there is an extra 3 ms of zeros added to the SSD data stream. Nevertheless, the SSD readout time is less than that of the TPC.

The current speed of the SSD system is too slow to meet the TPC DAQ1000 specifications and so it will be necessary to upgrade the SSD DAQ and RDO system to ensure that it is a viable detector in the future. The silicon wafers can be reused, but the readout electronics on each end of the ladders must be upgraded. The readout electronics upgrade will be discussed, and costed, later in the proposal.

The SSD is remotely controlled using JTAG for the power settings and temperature readings and also to calibrate and tune the front-end electronics. Each ladder dissipates about 20 Watts of power: 8 watts from the Si wafers and 6 watts from the electronics on each end of a ladder. The total heat dissipated by the system is 400 watts.

3.2 The Cooling System

The SSD uses air cooling which greatly reduces the material budget for the detector compared to other cooling methods.

The cooling system is based on a vacuum driven air flow[8]. The air comes from within the inner field cage of the TPC and starts at a temperature of approximately 24°C. A 'Transvector Vortec[9]' (an air driven venturi tube) is used to draw the air over the ladders at a rate of approximately 1 liter per second. Each ladder is wrapped in a Mylar sheet to contain the flow, and then the air is drawn down a 1 cm diameter flexible pipe to the Vortec which is mounted outside of the TPC. Ultimately, the warm air is discharged into the Assembly Hall.

A Transvector is merely a source of vacuum for the cooling system. See Figure 9. It provides a high volume of airflow, which is rated at 475 cubic feet per minute (13400 LPM) at the source. Four Transvector heads are used to cool the SSD and each head is used to cool five ladders. However, the impedance between the ladders and the Transvector is very high due to the 1 cm diameter tubes that connect the two items and so the flow experienced by each ladder is only about 1 liter per second (< 0.5 m/sec). This is inefficient; but is sufficient to cool the ladders and was carefully tested on the bench before installing the SSD in the STAR detector.

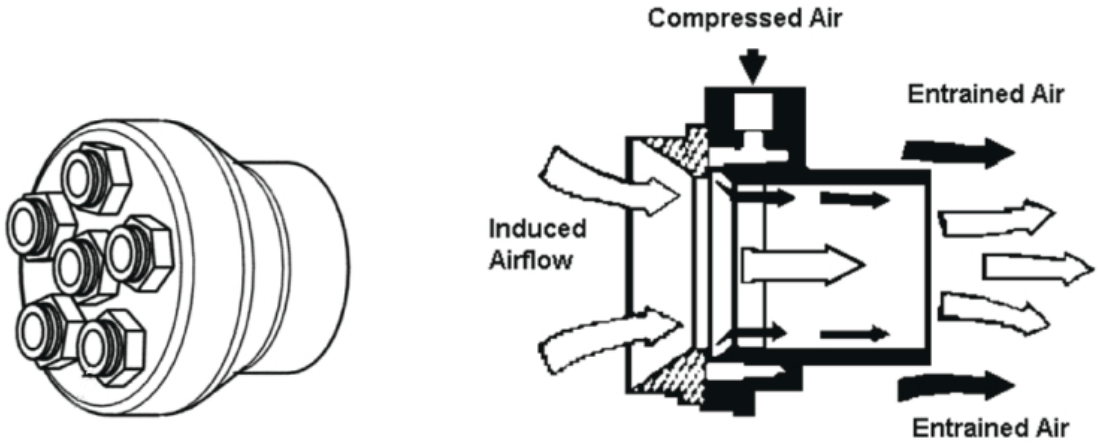

Figure 9: The left panel shows the vacuum distribution head that transfer airflow from the small diameter tubes to the larger Transvector. The right panel shows the Transvector airflow amplifier and its principles of operation.

The measured temperature distribution on the ladders depends on the point of interest, however, the hottest point is usually the ADC board and this board runs as high a 45° C without cooling air (assuming 20° C ambient air) and drops to 30° C when the cooling air is flowing[8]. The corresponding pressure drops are -12 mbar (relative) at the hose end of the ladders and -43 mbar at the Transvectors.

The 1 cm diameter flexible hoses were the probable-cause of the cooling failures seen in Run 7. After re-installing two ladders of the SSD during the shutdown following Run 5, the SSD was re-inserted into STAR. However, sufficient care was not taken with the hoses during installation and several of them were bent out of shape and kinked. The kinked hoses interrupted the airflow to perhaps 10 of the 20 ladders and probably affected all of the ladders to one degree or another. The exact analysis is hard to determine because the kinked hoses are hidden from view during the operation of the detector, however we found direct evidence in several cases that this was problem during the disassembly of the SVT and SSD in the shutdown period following Run 7. See Figure 10.

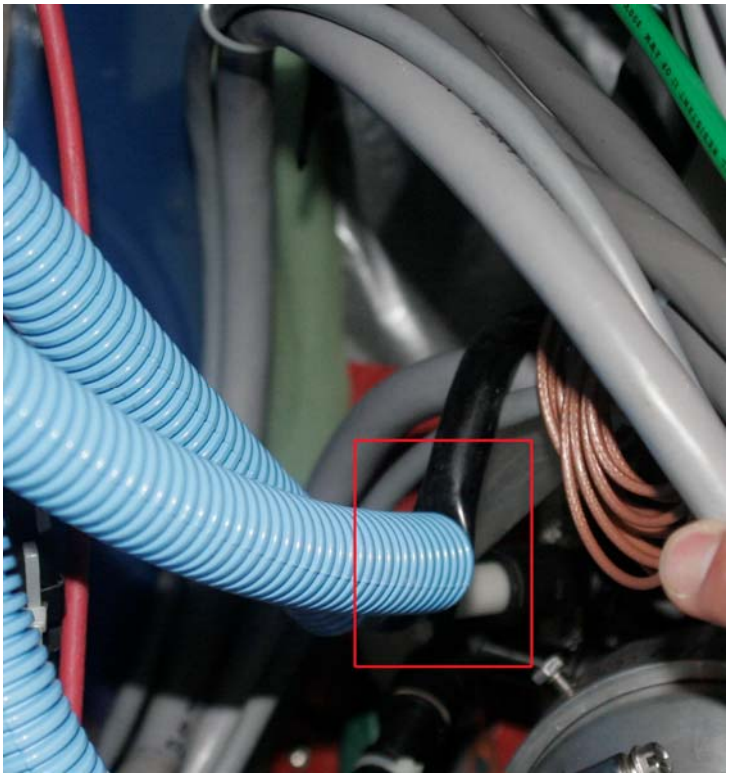

Figure 10: The red box highlights a kinked cooling hose that was discovered during the removal and disassembly of the SSD in August, 2007. Ideally, the blue corrugated hose should have protected the black vacuum line … but didn't in this case.

We believe that these problems can be overcome by hard-plumbing the cooling lines to the SSD ladders and replacing the Transvectors with a more reliable and simpler system.

4. Past Performance of the SSD

The SSD installation started in the summer of 2002, with the installation of 1 prototype ladder in the STAR experiment complex. During the summer of 2003, 9 additional ladders were installed (for a total of 10 ladders) with half of the detector acceptance being covered. During the 2003/2004 data taking (Run 4), 1 ADC board was not operational, and thus only 5 ladders were recording data.

Finally, the complete installation was performed during the summer of 2004, and the 200 GeV Cu-Cu run (Run 5) was the first data taking with a complete SSD detector. In total, there were 46 million minimum bias events recorded and 22 millions high momentum triggered events with the TPC and the SSD recording data. During the low energy run at the end of Run 5, there were 35 million events recorded with the TPC and SSD.

Due to an issue with the level-2 trigger abort, which has not yet been solved, the SSD is not compatible with the STAR level-2 trigger so the SSD was not included in the data acquisition stream for data taking in light systems (e.g. p-p) where the interaction rate is high and requires the level-2 trigger system. Therefore during the p-p running in Runs 5 and 6, the SSD was turned off.

In 2007, the SSD detector was in the acquisition stream during the entire data taking period. A total of 50 million minimum bias events were recorded with the TPC and SSD included.

Thus, the SSD was fully operational during Run 5 in Cu-Cu collisions at 200 GeV and 62 GeV in the center of mass, and during Run 7 in Au-Au collisions at 200 GeV.

4.1 Detailed status at the end of Run 7

At the end of Run 7, the SSD was removed from the STAR detector as part of the SVT decommissioning process. We have already performed a limited test of each ladder in the laboratory at BNL, and a primary conclusion of these tests is that the ladders should be sent back to SUBATECH to be examined by the people who built them and several ladders need to be repaired. The results of the tests at BNL are that thirteen ladders behaved almost normally during the run and seven ladders were not operational due to cooling and hardware failures. Six of the thirteen ladders performed normally and two were nearly perfect (see Figure 11). The absolute efficiency measured in Run 5 for ladders 11 and 12 was greater than 90% and matches the geometric acceptance of the ladders. Thus, the Si was 100% efficient on these ladders. Six of the thirteen good ladders had one bad Si wafer (out of 16) and we assume that these wafers cannot be repaired; we will have to live with these dead-wafers forever. One of the good ladders was noisy and the cause has not yet been identified.

Seven ladders were not operational in Run 7. Four of these bad ladders can be fixed: two of the ladders need a new HV capacitor (due to an assembly error) and two need better cooling. The remaining three bad ladders, ladders 6, 7 and 8, have problems that have not yet been identified. Additional information about the status of the ladders at the end of Run 7 is presented in section 6.3.

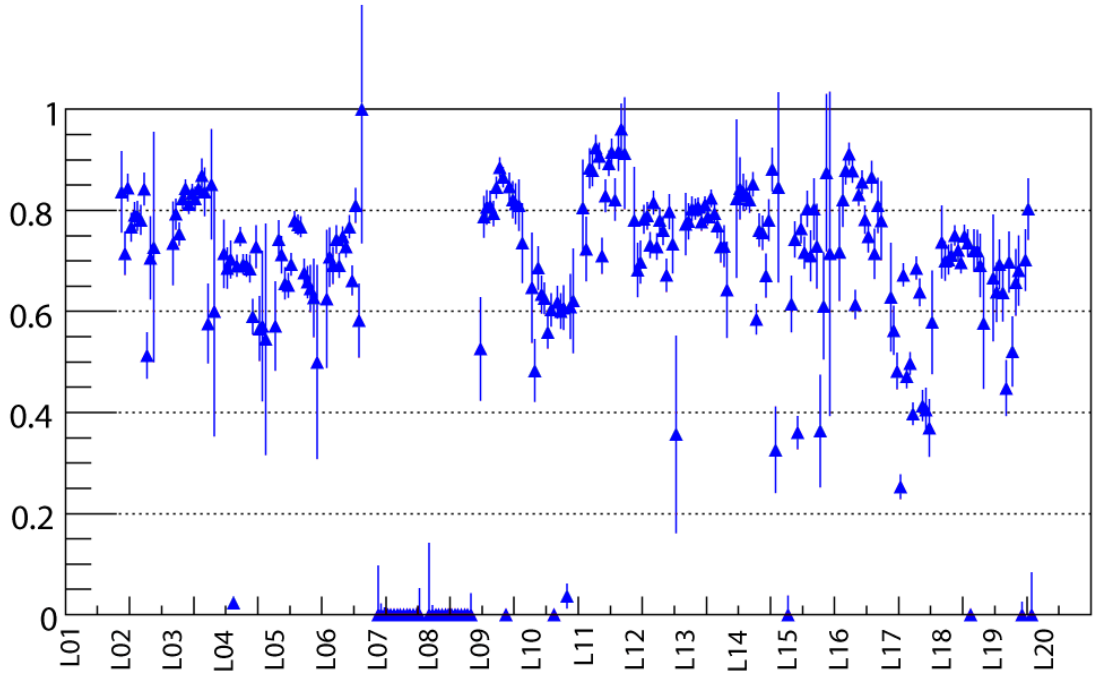

Figure 11: The absolute efficiency of the SSD was measured by asking if there was a hit in the SSD when there was a good track in the TPC and also a good hit in the SVT beneath it. The data were taken during the 200 GeV Cu-Cu run (day 21). In general, the efficiency of a ladder can exceed 90% and match the geometrical acceptance the ladder (e.g. ladders 11 and 12) but some ladders had a lower absolute efficiency and this is understood to be due to noise in the ladders. From the figure, you can see that the efficiency was not measured in ladders 1 and 20 (because the SVT coverage was not good in this area) and ladders 7 and 8 were turned off due to hardware failures on the ladders.

5. Repair of the SSD and Upgrade of the Electronics

There are three major and two minor items of repair or upgrade that must be performed on the SSD in order to ensure that it is a viable detector for the next 10 years.

- Redesign and replace the cooling system
- Fix the Level 2 abort problem, identify the problem and repair the firmware
- Upgrade the SSD readout electronics from 200 Hz to 1 kHz
  - Upgrade one sector of the SSD readout electronics in time for Run 10
  - Upgrade all of the SSD readout electronics in time for Run 11
- Design a new slow controls system to be compatible with the new electronics
- Ensure that all cone modifications proposed for the FGT and HFT are compatible with the re-installation of the SSD

Finally, all of the SSD ladders will have to go back to SUBATECH for repair prior to Run 9. We will also place some constraints on rest of the detector and, for example, we will need the space that was vacated by the SVT RDO boxes in order to have sufficient space for the new SSD readout boxes and electronics.

5.1 The cooling system

Air-cooling has been shown to be a satisfactory method to maintain the SSD within its temperature limits. However, experience has shown that great care must be taken to keep the cooling system working at the specified level of performance or the detector will fail.

We propose to build a new cooling system that will be more robust than the previous design, have additional cooling capacity, and an interlock system to prevent the operation of the detector should the cooling system fail. Also, the upgraded ADC boards that are located on the ends of the existing ladders will increase the power dissipation, and so additional cooling capacity may be required.

The cooling system for the SSD is a conventional system and does not present any extraordinary engineering design challenges. Therefore, we merely propose to re-engineer the system and to hard-plumb the pipes (i.e. use hard walled tubing) which run between the SSD ladders and the Transvector heads.

We also propose to replace the Transvectors with a conventional cooling system that uses a heavy duty 230 Volt motor (no brushes) that is designed for continuous operation[10].

The SSD cooling problem is an intellectual problem that requires a solution that employs the best engineering practices. Therefore, we envision that the cost of performing this repair is the salary for the people employed and not so much in the materials required to make the repair. These costs are included in the final chapter of the proposal, but the engineering effort is expected to be a BNL contribution. Therefore, the labor does not represent a new expense for STAR, but requires a redirection of effort.

5.2 The L2 problem

Currently the SSD receiver board software is crashing when L2 aborts are present and, in future runs, the SSD will be excluded from most of the interesting triggers until the source of this problem can be tracked down and fixed. This is not an acceptable situation since we plan to run the existing readout system, including the existing DAQ receiver boards, during Runs 9 and 10. In Run 11, the new DAQ receiver boards will be available and they will talk to the new STAR DAQ 100 system which, we hope, will not have this problem.

We believe the L2 abort problem is purely an intellectual problem (i.e. it can be solved with software) and so we must allocate human resources to solving the problem but it will not cost much in terms of hardware expenses.

5.2.1 What is the problem?

The manifestation of the problem is in the readout board (RB) software running on the mezzanine CPUs. These CPUs crash in the presence of L2 aborts. That does not mean that the RB software is the cause of the problem. A number of hypotheses are being followed: one is that the SSD readout board (RDO) firmware misbehaves in the presence of L2 aborts. However, the RDO was tested at SUBATECH with L2 aborts without such a problem in evidence. Another possibility is that the L2 aborts are only introduced when there is a high rate of L0 accepts; much higher than the 100 Hz to which the SSD readout is exposed in the absence of L2 aborts. This could arise from a crack in the busy logic specific to the SSD. Note that the SSD RDO contains no busy logic; this logic is in the RB and in the TRG system.

5.2.2 What is the solution?

Currently the SSD ladders have been removed from STAR. However, the SSD RDOs are still present and capable of responding to triggers (with nonsensical data). This abbreviated system has been used to try to characterize the behavior, and will be utilized in continuing efforts to instrument the mezzanine software to generate more specific diagnostics. We also have hardware logic analyzers we can use once we have more specific hypotheses to verify. We expect that the DAQ crew (Landgraf, Ljubicic) will be helpful in these efforts. Christophe Renard (SUBATECH) can also generate diagnostic firmware to run on the RDOs. The tests utilizing DAQ will be run at every opportunity when there is no physics running taking place.

5.3 The upgrade for the readout electronics

The present SSD readout is limited to slightly more than 200 Hz trigger rate due to a number of factors. The ADCs which digitize the signals from the modules are limited in sampling rate. The fiber link to the DAQ receiver board is limited to 1 Gb/s (120 MB/s),

and the data are required to be formatted in a somewhat inefficient way in order to be compatible with the existing DAQ TPC receiver boards.

The aim of the new electronics architecture is to read the modules in parallel. New, high speed ADCs will be employed in the upgraded electronic and the ADC outputs from several ladders will be brought to a readout box (RDO) located on the TPC wheel. A single RDO board will collect the data from 5 ladders in parallel, sending the data to a DAQ SSD PC via a DDL fiber link (160 MB/s). A total of 8 RDOs and 8 DDL fiber links will be required. The DDL links, together with their source interface to the SSD RDO and the PCI card residing in the SSD PC, are available through the ALICE collaboration.

The upgraded readout requires redesign of

- the ADC boards (one per ladder, containing 4 ADCs), which send 4 streams in parallel via each of five 5m-long cables to the RDO at the TPC wheel,
- the connection board at the end of each ladder which merges the data from the modules to the ADC boards,
- the RDO boards which perform the buffering and/or zero-suppression and deliver the data to the DDL link. We propose to house the 4 RDOs at each end of the TPC in a VME-like crate in the space that was previously used by the SVT RDOs.

Two approaches to managing dead time are being considered. The first takes advantage of the fact that a full event fragment (1/8 SSD event) occupies the DDL fiber for a significant period of time, which dominates the behavior of dead time as a function of trigger rate. The dead time behavior can be modified at lower trigger rates by employing randomizing buffers on the RDO. As a result, the dead time can be kept to an acceptable value at trigger rates up to ~600 Hz. In this approach, it is neither necessary to pedestal subtract the data, nor to suppress empty strips.

A second, complementary, approach to be implemented at the RDO consists of zero-suppressing the pedestal-subtracted strips whose signal falls below a threshold placed just above the average noise value. This approach can be extremely effective if the occupancy of the strips is small (<3%). In fact, the dead time calculated suggests that for these small occupancies, the multiple randomizing buffers may not be necessary.

Figure 12 and Figure 13 illustrate the dead time behavior as a function of trigger rate for both scenarios.

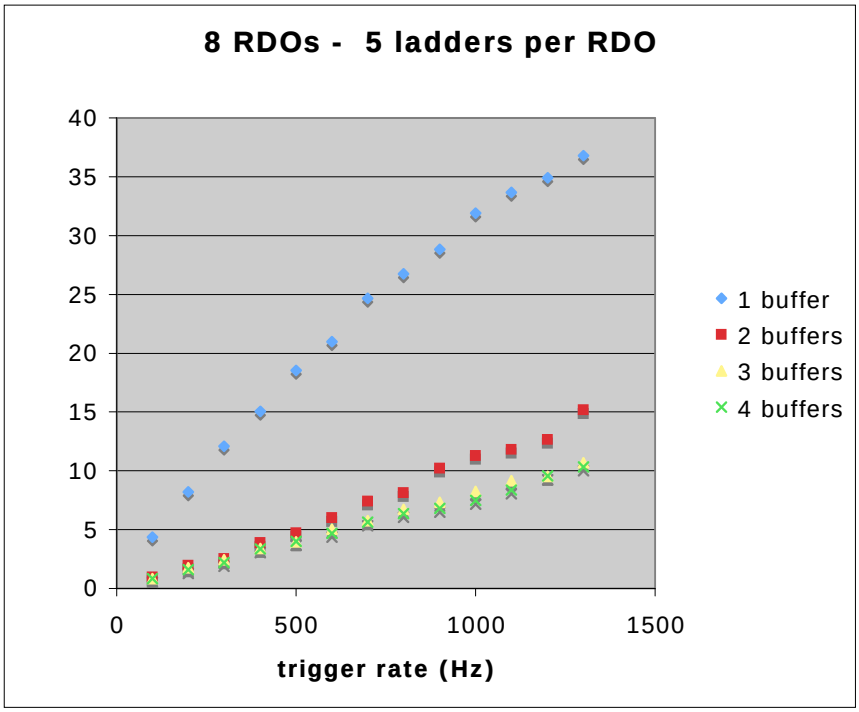

Figure 12: Dead time as a function of random trigger rate for one or several de-randomizing buffers at the RDO. No zero suppression is performed.

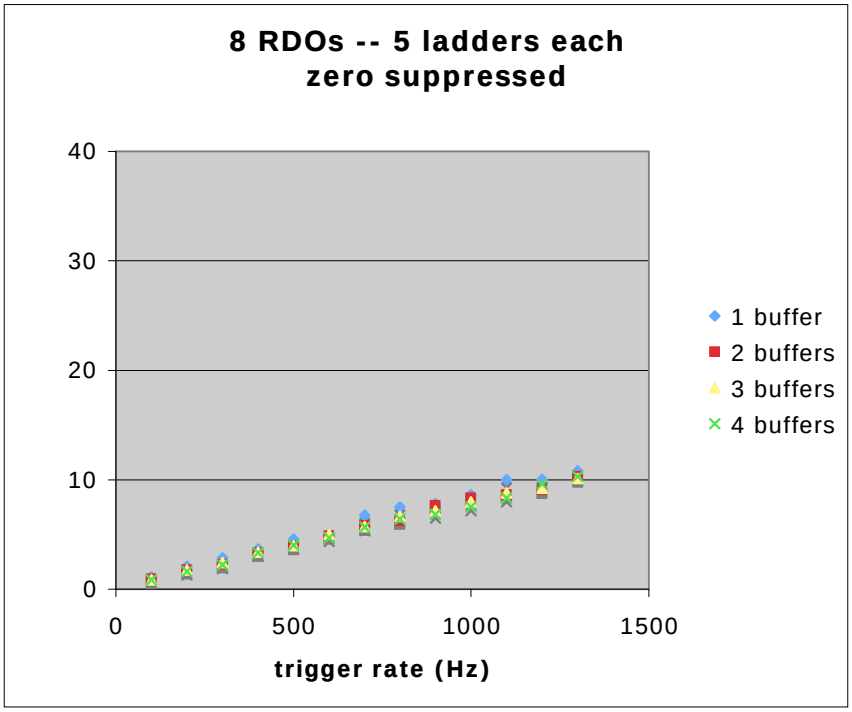

Figure 13: Dead time as a function of random trigger rates, for one or several de-randomizing buffers in the RDO. Empty strips are suppressed in the RDO; 3 per cent occupancy is assumed. Under these conditions, it is clear that multiple buffers offer no advantage.

It is worth noting that delivering the unsuppressed data to the PC can result in a heavy computing and memory-access load on the PC, which may limit the number of DDL fibers which it can host, since the ADC value for each strip has to be extracted from the word in which it has been stored along with 2 other ADC values, pedestal subtracted, and possibly written back to memory. These steps become unnecessary if the data are zero suppressed at the RDO.

The two approaches are being studied by a collaboration of scientists and engineers from SUBATECH and BNL. The experience of both groups is required because a cost effective solution to the problem will require all of the experience gained in designing the STAR and ALICE silicon strip detectors. We will also take advantage of the ALICE electronics designs whenever possible.

5.4 Slow Controls and Low Voltage Power Supplies

The new readout boards for the SSD will require a freshly programmed set of screens for the slow controls interface to the system. In particular, the Slow Controls interface should incorporate features that will prevent high voltage actuation and operation without adequate cooling.

This is an intellectual challenge that can be solved with contributed labor; although the level of effort will be substantial because the SSD places a fairly complex set of demands upon the slow controls system to set voltages on each Si wafer, to read the temperature on each ladder, etc. The primary goal is to keep the user interface simple because we only have a small team of experts working on the SSD and therefore we must rely upon the control room shift crews to accurately and reliably maintain the detector during the RHIC running periods.

So we anticipate that the labor costs will be low but there will be some modest hardware costs associated with the Slow Controls upgrade. For example, the STAR slow controls group is moving away from the old Sun workstation / VME / VxWorks environment that predominate in the STAR control room today and instead they are proposing to use a PC and Ethernet based system. We will use whatever system they deem to be best but we will have to purchase the hardware to match the new system. Purchases will include PCs and Ethernet switches. We will also have to purchase a pair of new low voltage power supplies of to replace the existing CAEN power supplies which have become unreliable and are the source of substantial down-time for the detector.

6. Integration with STAR and the STAR Run Plan

The SSD operated successfully in Run 7 but it was removed from STAR at the end of the run as part of the decommissioning of the SVT. As there was not enough time, the detector was not reinstalled for Run 8.

We would like to reinstall the SSD in time for Run 9 and include it in the STAR run plan, thereafter, as a standalone scientific instrument and to eventually become part of the proposed Heavy Flavor Tracker. However, there are some logistical hurdles that need to be resolved in order to keep the SSD in the run plan. For example, we will need to use the space that was vacated by the SVT RDO boxes in order to have sufficient space for the new SSD readout boxes and electronics. However, the most important issue is that new detectors will be coming, and going, and the addition of these detectors will require changes to the East and West TPC support cones upon which the SSD is installed

6.1 Modifications to the existing cones

We propose to install the SSD during the summer of 2008 using the original cones, and in later years when the new cones are ready, the SSD will be moved to and installed on the new cones. A summary of the schedule of activities is shown in the following list, and again in more detail in Table 2.

Run 8 – SSD is not installed

Run 9 – Installation during summer 2008

- Install SSD with conventional electronics on the existing cones

Run 10 – Installation during summer 2009

- Remove SSD
- Remove and replace the West cone to make space for the FGT.
- Reinstall SSD with three ladders (one sector) of upgraded electronics

Run 11 – Installation during summer 2010

- Remove SSD
- Remove and replace East cone to make space for PXL patch prototype
- Reinstall SSD with a full set of upgraded electronics

Run 12 – Installation during summer 2011

- Install and run the SSD as part of the HFT detector

For the purpose of this document, we propose to rely upon the HFT and FGT projects to design the new cones and to ensure that they will be compatible with the SSD. No funds are included in this proposal for that work. However, some engineering and technical effort will have to be expended on behalf of the SSD in order to verify that the proposed changes to the cones are compatible with the SSD. Figure 14 illustrates one such issue – the mount points for the SSD are fairly simple but they must be available, and must meet spec for each new design of the East and West cones.

Time	Beam(s)	Detectors		Others
Run 8	dAu,pp			
Summer 08		SSD install	SSD: reinstall SSD	DAQ 1000 TOF 50%
Run 9	AuAu, pp	SSD		
Summer 09		Install FGT SSD -	Remove Cone. Cutoff West- Add New East (FGT) Reinstall Cone	Finish TOF - reaction plane detectors.
Run 10	Low-E auau, pp 500	SSD, FGT	move west cone to LBNL Modify for installation SSD 1sector new electronic	FTPC(E) FTPC(W) ??
Summer 10		New Beampipe; Refurbished Cone. Install two patches	Phase-1 pixel	Remove FTPC(s)
Run 11	(AA,pp) (UU?)	PIXEL Patch, SSD,FGT,	SSD: new electronics	EBIS operational (?)
Summer 11		Complete Pixel Cooling. Install IST	ultimate installed	
Run12		Pixel complete, SSD,FGT,IST,		
Summer 12				

Table 2: A strawman schedule[11] for the installation of the SSD, HFT and FGT detectors in STAR. Column 4 contains comments about the cones and how they will change with time.

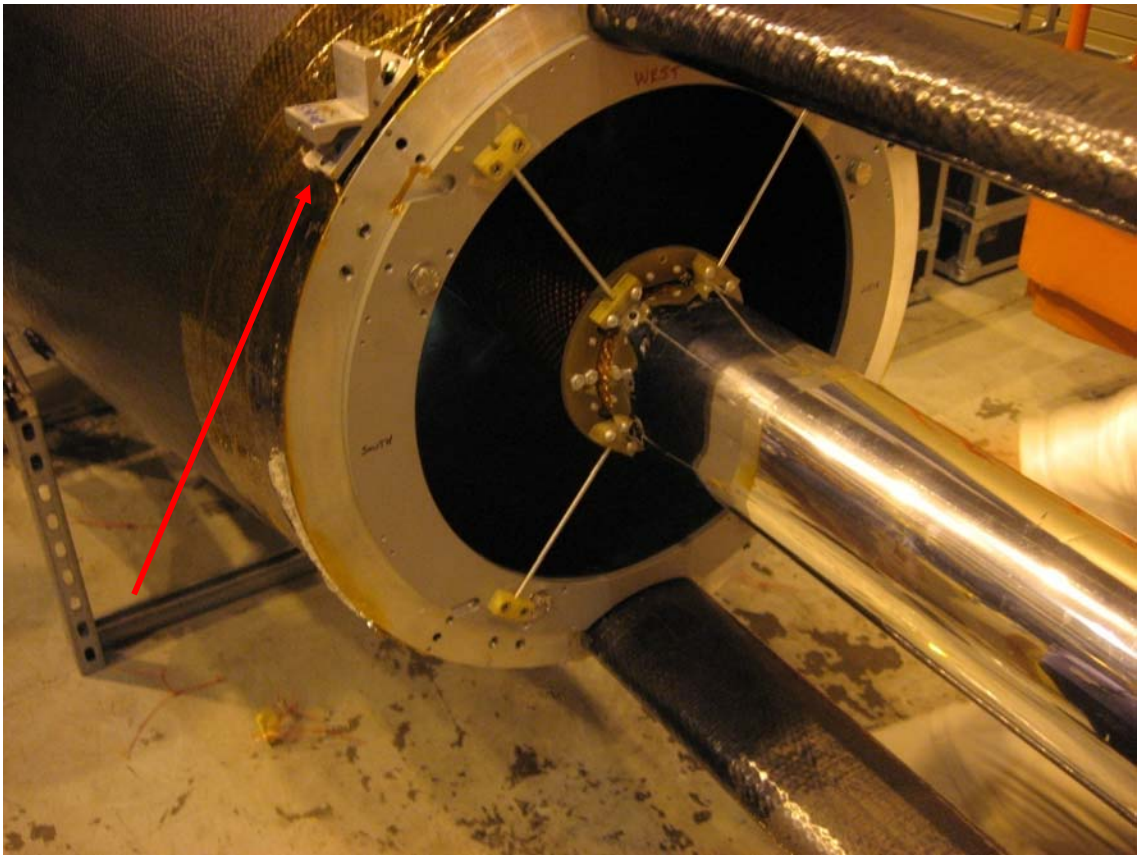

Figure 14: A mount point for SSD is shown attached to the existing East TPC cone. Four are required. The mounting scheme is fairly simple but future modifications to the cone must be aware of, and plan to provide, these mount points whenever the cone is changed.

6.2 Additional items to be integrated with the HFT project

It is important to have an integrated approach for the design of all components of the HFT and SSD. This requires an SSD integration engineer to actively review, and perhaps participate, in the design of the HFT and FGT and vice versa. When the SSD was originally built, there were problems with the SVT mechanics staying within the SSD integration envelope. This required a redesign of the SSD mechanical mounts in the field; hence our caution.

Therefore, it is important to employ a qualified integration engineer to ensure that the new mechanical systems for the HFT and FGT are compatible with the existing SSD detector. The design effort should include the following details:

- Use the existing mechanical mounts of the SSD.
- Ensure that the existing cables and cooling lines have adequate space. The cables from the SSD go both to the west and east ends of the detector. (The upgrade of the SSD will most likely use more cables and air hoses than before.)
- All three detectors, PIXEL, IST, and SSD, require air-cooling. While the PIXEL detector might need to operate at cooler temperatures, it is best if there is an integrated approach to cooling all three detectors. Using this approach, the cross talk from heat produced on each detector can be addressed.
- The SSD RDO boxes should be mounted on the TPC wheel. Space needs to be reserved for these components. In addition cooling needs to be supplied to these boxes.
- All three detectors are necessary to measure a displaced vertex. Therefore, the slowest readout will determine the speed of the HFT. The DAQ architecture of all three devices should be examined to ensure that one detector does not significantly impact the full system.

6.3 Preparations for Run 9 - Reinstallation of the SSD, Summer 2008

A roadmap for the first year of installation and commissioning activities is outlined in this section as an example of the work that will be required each year.

To install the SSD during the summer 2008 shutdown, several steps need to be taken immediately. First, the SSD has several ladders that must be repaired. These ladders will be sent back to Nantes. We have tested the SSD at BNL and made the following assessment of work needed to have a full functioning detector:

- Three ladders (6N, 7P, and 8P) and 5 modules (13P module 6, 16P module 12, 19P module 11, 20P module 4 and 15) have corrupt data.
- Three ladders with frequent HV trips during Run 7 have been diagnosed to have a high current (>200 μA). This problem may be due to a short circuit and/or a capacitor issue.

- One ladder (1N) and nine additional modules (3P module 14, 3N module 1, 5P module 1, 7N module 13, 14N modules 15 and 16, 16N module 1, 17P module 5, and 19P module 13) need tests with the more complete equipment in Nantes.
- 2 LV/HV connectors need to be changed.

These ladders and modules will be repaired and then shipped back to BNL for installation on the detector.

For installation, the STAR detector must be rolled back into the Assembly Hall so that the cone and beam pipe can be extracted. The support platform must be reinstalled and the cone removed. The SSD will then be mounted on the existing cone. The steps to reinstall it are:

1. Ship all the ladders to the STAR Assembly Hall
2. Install the cables and the new cooling hoses on the cone, put the hardshell back on
3. Install all ladders on the cone, connect the cables and the cooling hose to the SSD
4. Put the SSD, with the cone, back inside the TPC
5. Connect the SSD to the RDO boxes, perform a brief readout test (without cooling) to check if the ladders are properly connected
6. Test to make sure all of the ladders are working.

The next steps can be done irrespective of whether the SSD is in the WAH or in the Assembly Hall.

1. Move the SSD RDO boxes onto the TPC wheel
2. Install the new cooling system
3. Interface the cooling system to the slow control system. Install interlocks so that the SSD can only be operated when the cooling system is turned on. Changes have to be made to the Slow Control system for the new cooling system.

Cabling the detector on the cone in the STAR Assembly Hall will take one week with the assistance of a technician and an engineer from SUBATECH and the help of the STAR operations group. Then it will take a week to install the detector in STAR and test the SSD electronics. Three SUBATECH engineers are needed for this task. An additional week of testing is required. To accomplish these tasks, the SSD must be accessible for a total of three weeks in the Assembly Hall.

6.4 Integration with STAR DAQ in 2008

Because the SSD data stream causes the DAQ receiver boards to crash when there are L2 aborts, the SSD is not currently read-out for those triggers; thus limiting the usefulness of the SSD. By the time of the next run, the L2 problem needs to be solved. To facilitate this task, the SSD RDO boards have been moved to the third floor of the South platform.

The SSD and DAQ groups will work together before the summer 2008 shutdown to solve this problem.

6.5 Installation of the DAQ1000 patch in the summer of 2009

In preparation for Run 10, the HFT group will remove the west cone and replace it with a new one in the summer of 2009. This effort requires that the SSD group remove their detector and its cabling on the west end. It will take 2 days to remove the detector and the cables from the west end. One sector of three ladders will be equipped with the new electronics. Then three normal sectors plus the upgraded sector will be installed with two new RDO boards with their crates. This time will take two weeks with three engineers and the assistance of the STAR Operations group. After installation, it will take one week of testing by an engineer and a physicist. Therefore, the SSD should be accessible for three weeks in the Assembly Hall.

6.6 Installation of the full electronics upgrade in the summer of 2010

In preparation for run 11, the HFT group plans to remove the east cone and replace it with the refurbished west cone. To accomplish this task, once again the SSD will need to be removed with its cables on the east end. It will take a week of work for two engineers to dismount the sectors. Then, the ladder upgrade will take three weeks with the assistance of an engineer and a physicist and the STAR operations group. Once the ladders are upgraded, it will take 2 engineers a week to remount the sectors back on the cone. Finally, it will take one engineer, one physicist, and the STAR operations group a week to install and test the full system in STAR. Therefore, for this time period, it will be necessary to have STAR in the Assembly Hall for 6 weeks.

6.7 Specifications for the new TCD will be needed early

The design of the new SSD readout should proceed immediately so that it is ready when the HFT patch is installed for Run 10. This requires a complete definition of the proposed TCD architecture and a new TCD test board for testing the readout for the systems using the new trigger. Therefore, it is desirable for STAR to provide a TCD design early in the project. Alternatively, the SSD can use a mezzanine board for the current STAR trigger and provide to install another mezzanine board when the TCD specification is made, but since the second plan requires additional effort, it is most cost effective for STAR to specify the design of the TCD early in the upgrade project. A delay in specifying the new TCD will require additional money for the SSD design so that it can accommodate both the existing and new design.

7. Cost and Schedule

7.1 Upgrade for the SSD readout electronics

7.1.1 Resources needed in Nantes

The upgrade to the SSD readout requires the participation of Christophe Renard (SUBATECH electronic engineer), Stéphane Bouvier (SUBATECH project engineer), Gerard Guilloux (SUBATECH mechanical engineer), Louis-Marie Rigalleau (SUBATECH engineer) and a SUBATECH technician. Most of the design for the upgrade to the readout system will be carried out at SUBATECH, with participation during the production phase by a BNL engineer, who will continue to maintain the system after it is installed. The schedule for the upgrade is shown in Figure 15, while the details of Nantes' costs for the readout upgrade are given in Figure 16.

As soon as this proposal is approved, it will be necessary to write a formal MOU between STAR and the SSD institutions describing each group's commitments to the project. While we have had informal discussions, it is important to formally describe the scope of work and agree upon the financial details.

7.1.2 Resources needed from BNL

For the readout upgrade, a digital electronics engineer will be required at BNL to participate in the design, layout, and debugging of the upgraded electronics. It is essential that he/she take ownership of the new electronics, learn to diagnose problems, and repair the affected boards. (5/8 FTE integrated over the time of this project.)

Following completion of the upgrade, a continuing engineering effort (0.1 FTE) will be required. It is assumed that this will be contributed by BNL.

7.2 Cooling system replacement

The cooling system needs to be designed and implemented. A BNL mechanical designer is required for this effort. Estimated cost for the cooling system: $20K, in FY08, plus the engineering cost ($100K). The new system must be ready for installation in the summer of 2008.

7.3 Slow controls upgrade

Slow Controls needs to be redesigned and implemented using a Linux PC as a platform. Implementation of the Slow Controls upgraded software will be done on PCs, with Ethernet linking the various nodes in the system. This hardware will cost $15.0K and travel for the SC person to Nantes for integration will cost $5.0K.

A partial implementation must be ready for integration at Nantes in early 2009. The final system must be deployed in summer of 2009.

7.4 Solution to the L2 problem

The solution to the L2 problem requires no financial resources, but will involve scientific and engineering effort at BNL. This problem must be solved before Run 9.

7.5 Shipping and travel to Nantes

Shipping of the detector ladders to and from Nantes for the detailed test and repair is included in the table in Figure 16. There is, however, no provision for travel of BNL personnel to participate in this testing and repair; this travel might require additional funds to be spent at BNL and is included as a contingency item in FY08.

7.6 Replace CAEN HV/LV power supplies

The existing power supplies have caused some down time in Run 7. There are no spare crates for quick swaps, and the manufacturer no longer offers them for sale. We propose to replace them with more modern models, at a cost of $20K. This change will require a modification of the Slow Controls. To minimize this effort, we plan on selecting a model that uses an Ethernet interface.

7.7 Contingency

The cost of the readout upgrade is dominated by manpower and related costs. Hardware represents a small piece of the total. Contingency for the custom hardware is calculated at 30%. Additional travel for U.S. personnel should be planned for, as well. We estimate the travel contingency at three additional foreign trips.

7.8 Cost offsets due to BNL contributions

The US engineering effort ($162.5K for electronics engineer and $100K for mechanical design of the cooling system) is expected to be contributed by BNL and will effectively reduce the costs in the table (shown below) by $262.5K.

7.9 Cost offsets due to SUBATECH contributions

All engineering and technical effort to be provided by SUBATECH is assumed to be contributed labor and will not be costed to the project. Due to the differences in the US and French accounting systems, these costs are not included in the table, below.

7.10 Cost summary

FY08

• test and repair ladders (1 trip included)	$19.1K	SUBATECH
• 0.125 FTE BNL electronics engineer	$32.5K	BNL
• slow controls hardware	$15.0K	STAR
• prototype new readout system	$52.5K	SUBATECH
• replace power supplies	$20.0K	STAR
• new cooling system hardware	$20.0K	STAR
• cooling system engineering	$100.0K	BNL
• contingency (1 trip included)	$16.4K	
Total FY08	$275.5K	

FY09

• slow controls integration with new electronics	$5.0K	STAR
• full readout implementation	$102.7K	SUBATECH
• ¼ FTE BNL electronics engineer	$65.0K	BNL
• contingency (including travel)	$34.3K	
Total FY09	$207.0K	

FY10

• full readout installation	$15.4K	SUBATECH
• ¼ FTE BNL electronics engineer	$65.0K	BNL
• contingency (1 trip included)	$5.0K	
Total FY10	$85.4K	

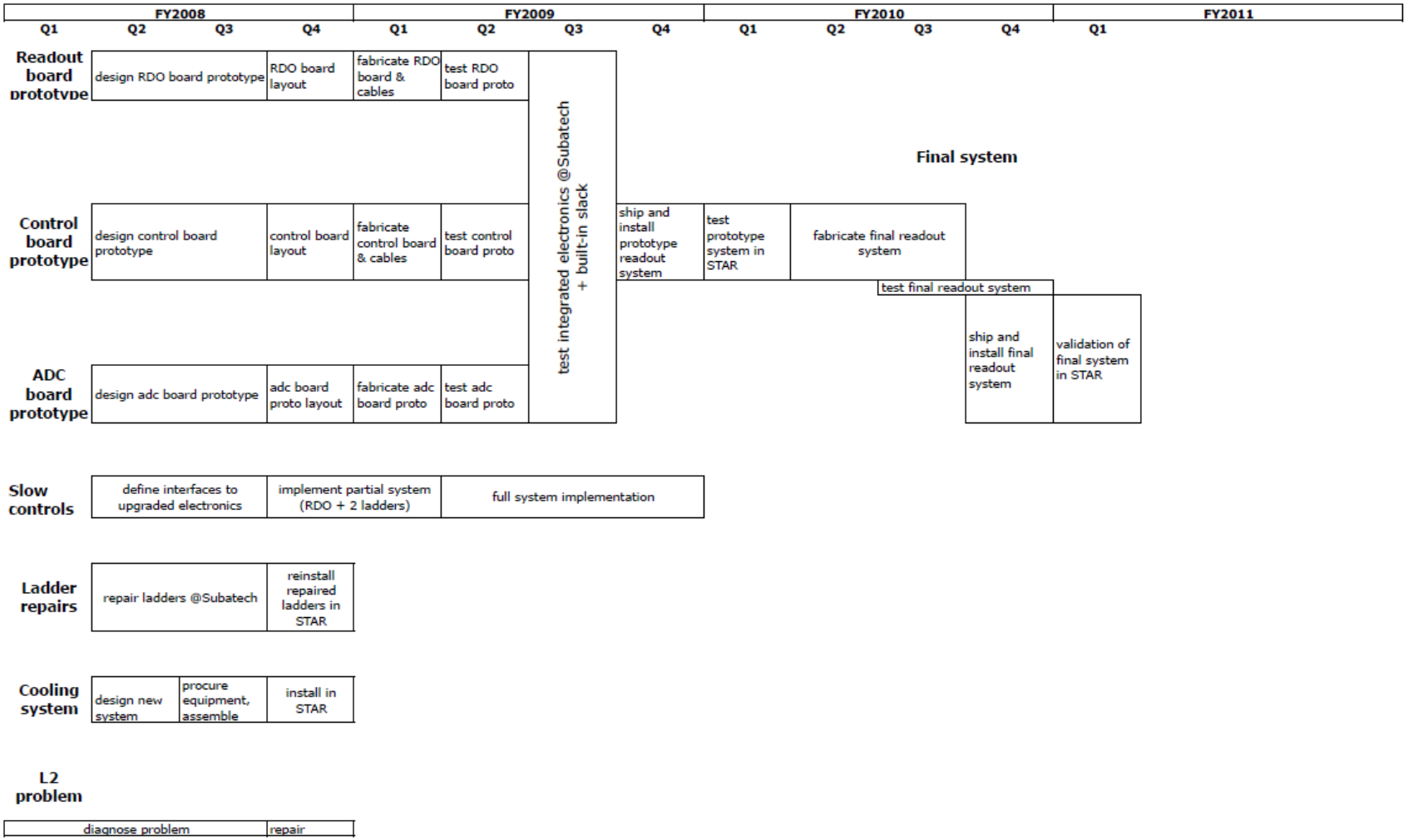

Figure 15: A simplified schedule and timeline for the SSD electronics upgrade activities. This schedule also drives the schedule for the other SSD upgrades including the cooling system upgrade, the solution to the L2 problem, and the Slow Controls upgrade.

STAR-SSD Upgrade cost estimate

Version 1.5 du 24 octobre 2007 - C.Renard - Subatech, EMN-IN2P3/CNRS-Université, Nantes, F44307, France

	SSD Upgrade	**SSD maintenance**	# days	# people	qty	travel (Nantes personnel)	equipment transport Subatech-BNL-Subatech	DAC1000 (SIU + 1/2 DRORC + fibers)	complete ssd_rdoU board	rdoU crate + power + cable	complete ssd_adcU + ssd_connectionU board	bus cable	trigger cable	mechanical adapter
reference price	*1 €*	*1 €*	*1*	*1*	*1*	*1,390 €*	*1,000 €*	*1,485 €*	*1,500 €*	*2,000 €*	*1,000 €*	*50 €*	*50 €*	*100 €*
bad ladders back to Subatech		1,000 €					1,000 €							
total 2007	**0 €**	**1,000 €**				**0 €**	**1,000 €**	**0 €**	**0 €**	**0 €**	**0 €**	**0 €**	**0 €**	**0 €**
ladder maintenance		0 €												
all ladders back to BNL		1,000 €					1,000 €							
ssd_bus_cableU	400 €				8							400 €		
tech meeting "specif Upgrade"	3,360 €		7	2		3,360 €								
SSD reinsertion on old cone + test		2,390 €	7	3		2,390 €								
SSD connection to STAR + test		3,360 €	7	2		3,360 €								
L2 test		3,060 €	14	1		3,060 €								
technical meeting "Upgrade"	3,360 €		7	2		3,360 €								
total 2008	**7,120 €**	**9,810 €**				**15,530 €**	**1,000 €**	**0 €**	**0 €**	**0 €**	**0 €**	**400 €**	**0 €**	**0 €**
ssd_rdoU	4,500 €				3				4,500 €					
ssd_crate	8,000 €				4					8,000 €				
ssd_adcU + ssd_connexionU	8,000 €				8						8,000 €			
DAQ1000 (DDL)	4,455 €				3			4,455 €						
trigger cable	150 €				3								150 €	
trigger + daq1000 at Subatech	1,000 €						1,000 €							
mecanical adapter	200 €				2									200 €
3 ladders removal from old cone	0 €		2	3										
cable installation IF new cone	4,360 €		7	2		3,360 €	1,000 €							
Upgrade installation on 3 ladders	5,790 €		7	3		4,790 €	1,000 €							
Upgrade insertion on cone + test	2,390 €		7	3		2,390 €								
SSD connection to STAR + test	1,930 €		7	1		1,930 €								
total 2009	**36,455 €**	**0 €**				**12,470 €**	**3,000 €**	**4,455 €**	**4,500 €**	**8,000 €**	**8,000 €**	**0 €**	**150 €**	**200 €**
ssd_rdoU	15,000 €				10				15,000 €					
ssd_adcU + ssd_connexionU	44,000 €				44						44,000 €			
ssd_bus_cableU	1,800 €				36							1,800 €		
DAQ1000 (DDL)	10,395 €				7			10,395 €						
trigger cable	150 €				3								150 €	
SSD removal from cone	0 €		7	3										
cable installation on cone	4,360 €		7	2		3,360 €	1,000 €							
Upgrade installation on all ladders	6,320 €		28	1		5,320 €	1,000 €							
Upgrade insertion on cone	3,360 €		7	2		3,360 €								
SSD connection to STAR + test	1,930 €		7	1		1,930 €								
total 2010	**82,025 €**	**0 €**				**13,970 €**	**2,000 €**	**10,395 €**	**15,000 €**	**0 €**	**44,000 €**	**1,800 €**	**150 €**	**0 €**
TOTAL 1	**125,600 €**	**10,810 €**	**230**			**41,970 €**	**7,000 €**	**14,850 €**	**19,500 €**	**8,000 €**	**52,000 €**	**2,200 €**	**300 €**	**200 €**
						30.8%	5.1%	10.1%	13.2%	5.4%	35.3%	1.5%	0.2%	0.1%

TOTAL	**136,410 €**

based on:

8 readout boards,5bus-cable/rdo, 1ladder-side/cable, 4adc-converter/ladder-side, 1daq1000/rdo + 2spares@bnl + 2spares@subatech
run X : 3 ladders Upgraded (2 rdoU, 2 crates, 6 adcU, 6 connectionU, 2 daq1000)@star + 1spare@subatech
run XI : all 20 ladders Upgraded (8 rdoU, 2 crates, 40 adcU, 40 connectionU, 8 daq1000)@star + 2spares@star + 2spares@subatech
SIU: 615 €; D-RORC (2 integrated DIU): 1540 €; 5m duplex optical patch cord: 55 €; 40m duplex optical patch cord: 80 €

Figure 16: A cost estimate for the SSD electronics upgrade; contingency is not included. Prices are in Euros. French labor costs are not charged to the project but STAR must purchase the hardware components and allocate travel funds for the French engineers.

8. References

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[8] http://www.star.bnl.gov/STAR/ssd/STAR_technique/STAR_Cooling.html. Note: you cannot use Internet Explorer (from Microsoft) to navigate to this page. You must use Mozilla Firefox or perhaps another non-Microsoft web browser.

[9] https://secure.vortec.com/store_products.php?catID=62, or http://www.newmantools.com/vor902.htm

[10] http://www.ryvac.com/power.html

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