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Exploration of GaTe for Gamma Detection

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***Abstract* - The layered III-VI semiconductor Gallium Telluride has potential for room temperature gamma ray spectroscopy applications due to its band gap of 1.67 eV, and average atomic number of 45 : 31 (Ga) and 52 (Te). The physical properties of GaTe are highly anisotropic due to covalent bonding within the layer and van der Waals bonding between layers. This work reports the results of surface and bulk processing, surface characterization, and electrical characterization of diodes formed on both the laminar and non-laminar GaTe surfaces. Alpha detection measurements were also performed.**

I. Introduction

While there are several conventional semiconductor materials used for gamma ray spectroscopy, there is interest in alternative materials due to the limitations in the currently employed technology. High purity germanium detectors have extremely high energy resolution (0.2 %); however, due to low energy bandgap of 0.66 eV, they must be cryogenically cooled. A room temperature alternative, Cadmium Zinc Telluride, is capable of achieving good energy resolution of between 1 to 2 %, although these crystals are generally quite small, around 1 cm^3. The layered III-VI semiconductor GaTe has potential for efficient room temperature gamma ray spectroscopy applications due to its indirect band gap of 1.67 eV [1] and atomic number of 52 (Te). Another layered III-VI semiconductor compound, GaSe, has already been shown to detect alpha particles [2].

GaTe has a monoclinic crystalline structure that is arranged into planes, shown in Fig. 1. In this work, "laminar" describes surfaces parallel to the crystal layers, which is also the cleavage plane. Conversely, the surfaces perpendicular to these planes are referred to as "non-laminar." The physical properties of GaTe are highly anisotropic due to covalent bonding within the layer and van der Waals bonding between layers. Reports have suggested that there is a high mobility orientation, for which charged carrier transport occurs parallel to the layers [3]. Similarly there is a low mobility orientation, with charged carrier transport perpendicular to the layers.

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In this work, the results of surface and bulk processing, surface characterization, and electrical characterization of both the laminar and non-laminar crystallographic orientations will be reported. Also the results of alpha detection measurements are shown.

II. Experimental Details

A. Crystal Growth

GaTe crystals were grown at EIC and Fisk University using stoichiometric amounts of high purity (7N) Ga and EIC's zone refined Te as starting materials to make a homogeneous polycrystalline ingot, Fig. 2. The polycrystalline ingot was then placed in a conically tipped thick-walled (≥3 mm) carbon coated quartz ampoule and sealed under a vacuum of 10^{-6} torr. The conical tip was specially designed to hold a GaTe seed crystal, which prevents secondary nucleation and allow growth along a preferred orientation. An axial low temperature gradient (~ 10°C/cm at the growth zone) was imposed by tuning the input power distribution into the heater to stabilize the solid-liquid interface. The sealed ampoule was then suspended in the Bridgman crystal growth furnace and connected to a slow-speed (0.2 rpm) motor. After which, the polycrystalline material was heated slowly (~ 10°C/hr) to 980°C for GaTe in computer controlled three-zone vertical furnace. The growth temperature was maintained by an Omega PID temperature controller. A computer-operated pre-programmed controller regulated its translational as well as

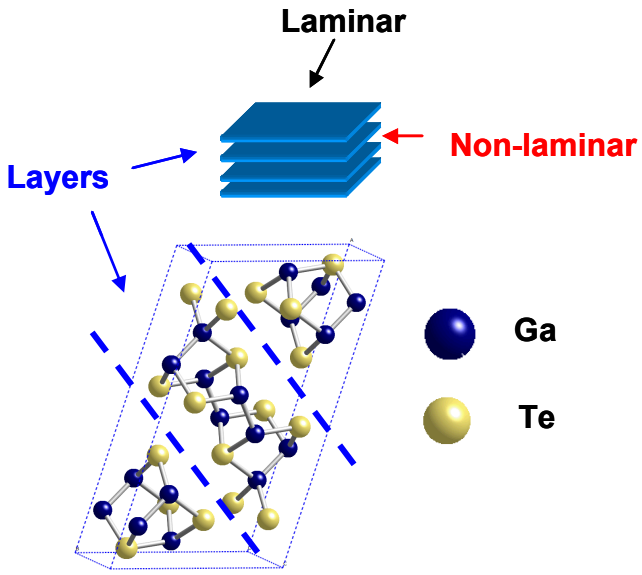

Fig. 1. Simulated crystal structure of monoclinic GaTe. Blue dashed lines indicate crystallographic layers.

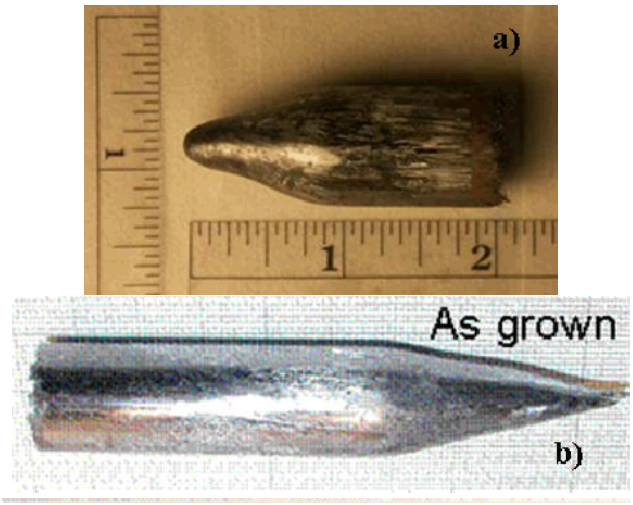

Fig. 2. Examples of grown GaTe crystals from EIC Laboratories (a) and Fisk University (b).

rotational motion. The ampoule containing the melt moves downward and the grown crystal is directionally solidified.

B. Material Processing and Characterization

Cleaving and sawing of the crystals was performed on the laminar and non-laminar surfaces of the crystals respectively. Lapping and polishing of both surfaces was performed using a Logitech PP5 precision polishing jig. Slurries of various grit size and wet chemical composition were evaluated by measuring surface roughness using a Zygo optical interferometer and by measuring chemical composition using energy dispersive x-ray spectrometry (EDS) and x-ray photoelectron spectroscopy (XPS).

A wet etching experiment of GaTe was also performed using a mixture of H_3PO_4, H_2O_2 and H_2O with the ratio of 1:1:10 by volume respectively. To create a pattern on the sample for use as an etch mask, photolithography, followed e-beam evaporation of 2000 Å of gold and metal liftoff was performed on a laminar face of the GaTe sample. The experiment consisted of exposing the sample to the etchant for durations of 1, 2, and 5 minutes and measuring the step height with a surface profilometer in between each etch step to determine the etch rate and surface roughness.

To fabricate diodes in which carrier transport will occur along the layers and across the layers, electrodes were deposited on the non-laminar and laminar sides of a Ge-doped GaTe crystal respectively. The samples were cleaved and polished resulting in a rectangular sample of approximately 2 mm x 2 mm x 5 mm shown schematically in Fig. 3. A solvent clean was performed before photolithography was carried out on two adjacent sides of the sample. A dilute HCl surface treatment was followed by electron beam evaporation of aluminum which was subsequently lifted off to form circular contacts with guard rings [2, 3]. The remaining two sides of the sample were coated with GaIn paint to form ohmic contacts. Current versus voltage and measurements were performed on the fabricated diodes.

A planar detector was fabricated on the laminar side of a 4 mm x 3.4 mm x 2.5 mm Ge-doped GaTe crystal. The sample

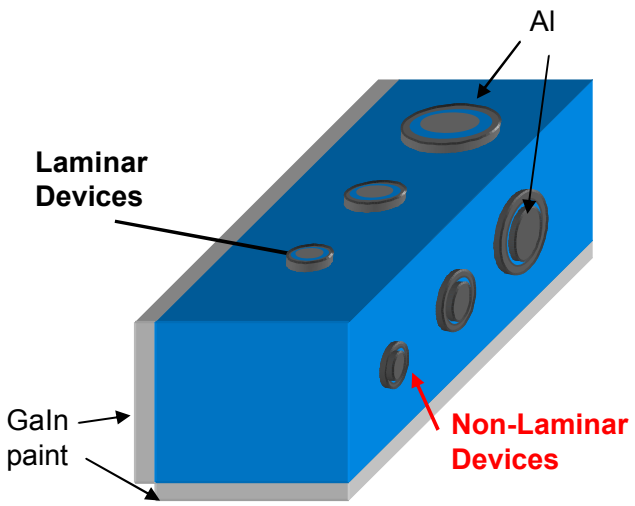

Fig. 3. Schematic diagram of fabricated diodes on laminar and non-laminar surfaces.

was cleaved and polished followed by a solvent clean. Prior to ebeam evaporation of an aluminum electrode a dilute HCl dip was performed. The bottom contact was formed by coating with GaIn paint to form an ohmic contact. The detector was placed in a vacuum chamber with an uncollimated 0.2 μCi ^{243,244}Cm alpha source. The measurement setup is as follows: the detector was attached to Ortec 142PC preamplifier followed by an Ortec 485 Amplifier with 3 x coarse gain using 2 μs integration time. The data acquisition time was 1 minute. When the chamber is unevacuated, the alphas are blocked by the air molecules in chamber. When the chamber is pumped down, the 5.8 MeV alpha particles strike the sample surface.

III. Results and Discussion

A. Surface Processing and Characterization

To prepare the surface for deposition of electrical contacts, the appropriate processing steps must be determined to minimize surface roughness and assure that the surface is stoichiometric. Cleaving appears to be the best way to prepare the laminar surface. In the inset to Fig. 4, the electron micrographs reveal that cleaved laminar surfaces are exceedingly smooth (bottom portion of micrograph inset Fig. 4a), while that the non-laminar surface is "stepped" due to the GaTe layered morphology. Interestingly, by qualitatively comparing the Ga/Te ratio for laminar versus the non-laminar surfaces, we find that the relative ratio varies by more than a factor of three, with the non-laminar surface being tellurium-rich (see EDS data in Fig. 4). The surfaces also reveal a significant amount of organic contaminants which can be removed. Overall, the surface region exhibits significant variation in the Ga/Te ratio depending on the crystallographic direction and the means of preparing the surface. This result is further supported by XPS data (Fig. 5), as obtained for two samples shown below, where the gallium-to-chalcogenide ratio is reduced to be 60-75% for the non-laminar surface (once again indicating that it is Te-rich). The XPS and EDS results may not agree quantitatively

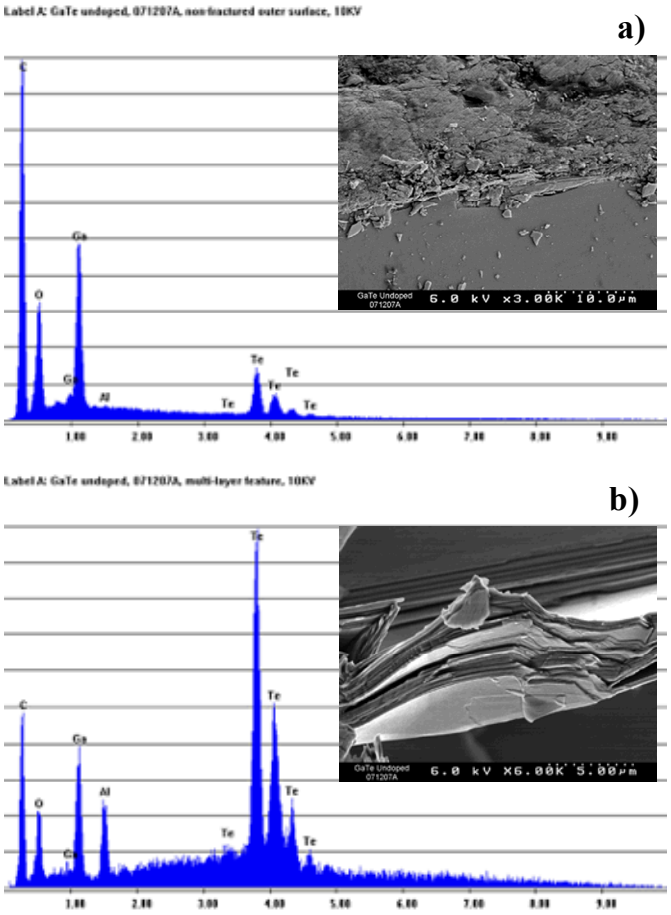

Fig. 4. EDS data of laminar (a) and non-laminar (b) surfaces which qualitatively shows that the non-laminar surface is enriched in tellurium. Inset shows electron micrographs of each surface.

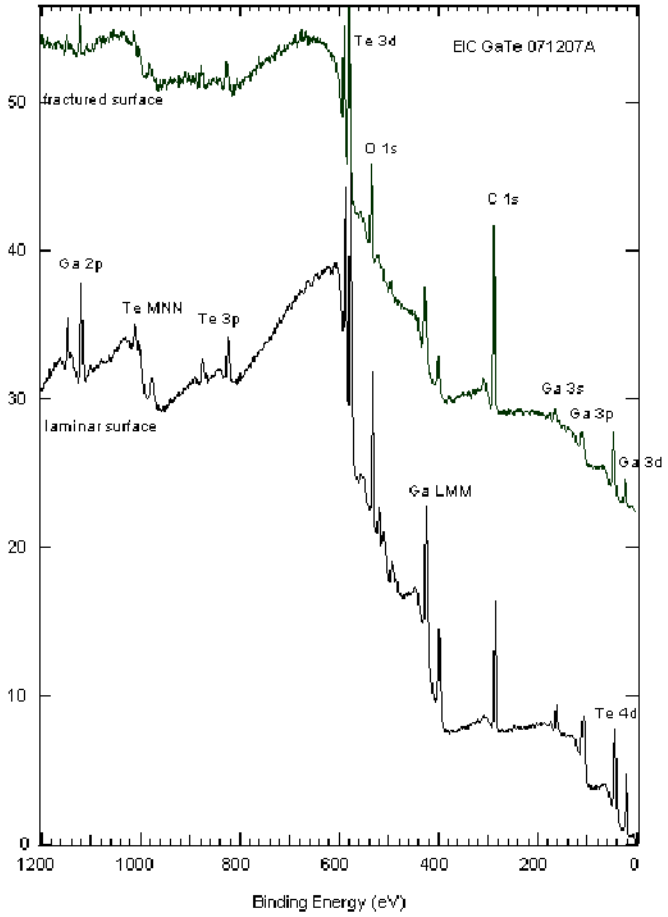

Fig. 5. XPS data obtained for GaTe crystals, for the fractured (non-laminar, upper) and cleaved (laminar, lower) surfaces, revealing that the non-laminar surface is Te-rich in both cases.

in part because EDS surveys depths of a few micrometers, while XPS only tests for the material properties within a few mono-layers.

While cleaving appears to be the best way to prepare the laminar surface, an attempt to improve the surface roughness of the sawn non-laminar surface was undertaken. Lapping and polishing on the non-laminar surface was developed, as would be required to deposit contacts (for implementation of photolithography). As pictured below in Fig. 6, based on "before" and "after" optical micrographs (at 5x), we see that the ridges have been largely removed using 0.3 µm alumina in silicone oil for 30 minutes (40 rpm, by hand). The RMS roughness was originally 950 nm, and then became 250 nm afterwards. If we look specifically *not* at the remaining ridges, the RMS roughness is 40 nm (leading to the reflective appearance). An interesting observation is that we have been by far more successful polishing the alloyed compound, $GaSe_{0.1}Te_{0.9}$, compared to the pure GaTe crystals. We interpret this as being due to the well-known hardening that results from having mixtures rather than pure substances, especially for the case of layered structures. Lastly we mention that 0.05 µm alumina grit was not sufficiently abrasive to diminish the ridges in the same amount of time (30 minutes).

The results of the wet etching experiment of GaTe are shown in Table 1, which compares the RMS surface roughness and etch rate in between the metallization in two different regions of the sample. After 5 minutes of etching, region 1 appeared dark non-reflective while region 2 had a metallic color and was reflective, Fig. 7. The surface roughness in the two regions was approximately the same. An etch rate of approximately 45 Å/s for the darker region and 60 Å/s for the more reflective portion of the sample was determined from the step height measurements indicating that the etch rate varies for different crystal grains. XPS was performed on the sample after etching and is shown in Fig. 8. The resulting surface is oxide free indicating that this surface treatment is also appropriate before metallization.

B. Electrical Characterization

TABLE I
SURFACE ROUGHNESS AND ETCH RATE COMPARISON FOR TWO AREAS ON THE SAMPLE AFTER 5 MIN ETCH IN H3PO4, H2O2 AND H2O, 1:1:10.

	Color	RMS Roughness (nm)	Etch rate (A/s)
1	Dark	173	45
2	Reflective	163	60

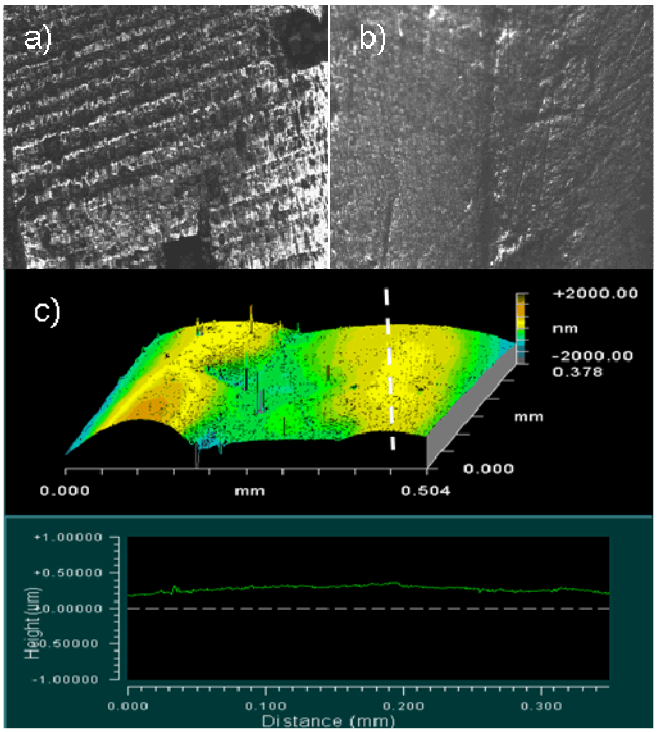

Fig. 6. Micrographs of non-laminar surface as sawn from boule (a) and after polishing (b). Surface roughness scan using Zygo optical interferometer showing 40nm RMS surface roughness (c).

Representative current versus voltage curves for the diodes with guard rings are shown in Fig. 9 on a log scale for transport directions parallel and perpendicular to the GaTe layers. The inset shows the I-V curve of the parallel device on a linear scale. Rectifying behavior was achieved for the parallel device; however there is a significant amount of reverse bias bulk leakage current. Diodes fabricated on the parallel direction show 3×10^4 more forward current density at $V_d = 1$ V than the perpendicular diode. Differences in mobility between the laminar and non-laminar directions only account for a factor of approximately 200 [5]. Because of the weak bond between layers, defects preferentially form along this direction giving rise to increase leakage current the parallel direction. It also possible that partial delamination of layers occurred, which would reduce the effective mobility in the perpendicular direction.

Fig. 10 shows the normalized I-V curves for diodes fabricated in both directions, with and without a guard ring. Without the guard ring, surface leakage dominates and there is a higher percentage of leakage current in the laminar diode, likely due the anisotropy of the mobility along the surface. Fig. 11 shows the difference in current with and without the microscope light for devices in both directions. The perpendicular devices show as much as a 5x increase in current density while devices with transport parallel to the layers show no such photo enhanced conductivity.

C. *Alpha Detection Measurement*

Alpha detection measurements were performed on the planar detector. The resulting spectrum is shown in Fig. 12. A

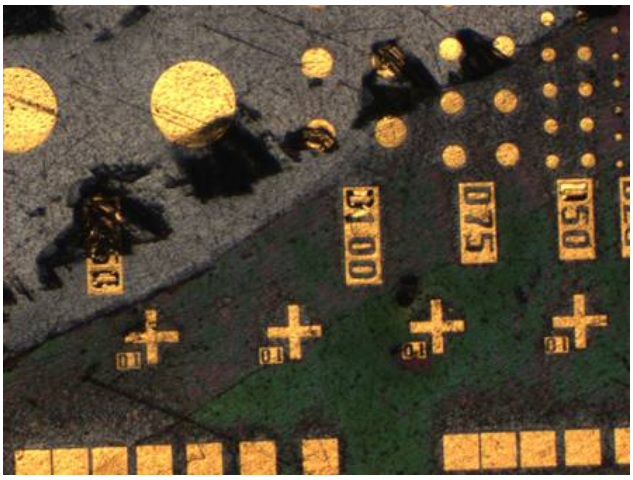

Fig. 7. Micrograph of patterned GaTe sample after 5mins of etching in H3PO4:H2O2:H2O solution.

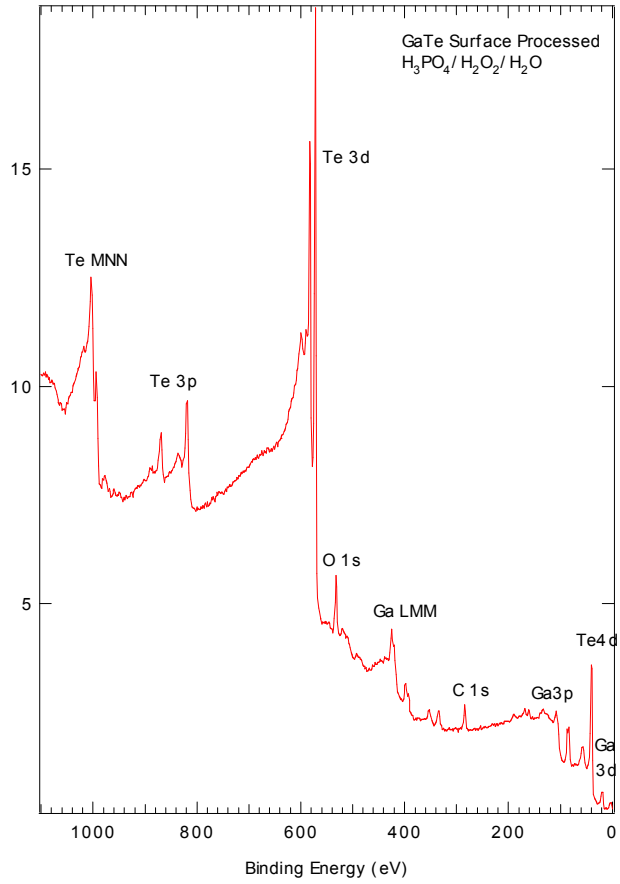

Fig. 8. XPS data obtained for GaTe crystals on laminar surface, after wet etching with $H_3PO_4/H_2O_2/H_2O$ showing oxide free surface.

clear increase in counts over a wide range of energies is observed when the alpha particles are incident on the sample demonstrating detection of the alpha particles.

IV. Conclusion

Diodes were fabricated on the layered semiconductor GaTe. Electrical characterization was performed showing rectifying behavior for the diodes fabricated on the non-laminar surface

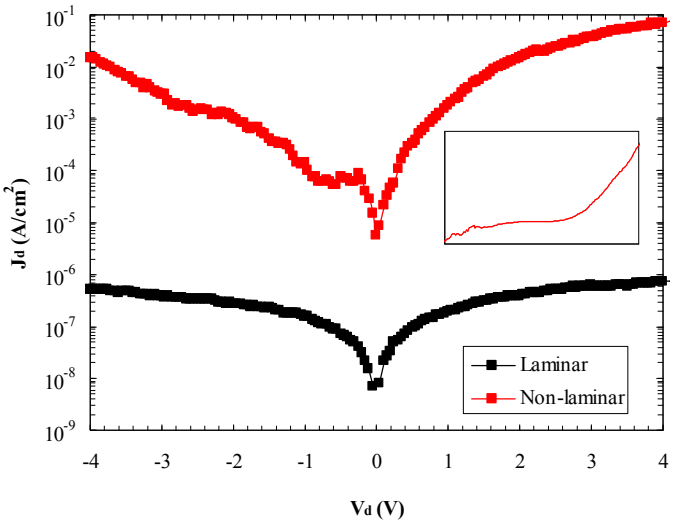

Fig. 9. I-V curves of 50 µm diameter Al-GaTe diodes fabricated on surfaces both laminar and non-laminar surfaces with guard rings. Inset shows non-laminar device on a linear scale.

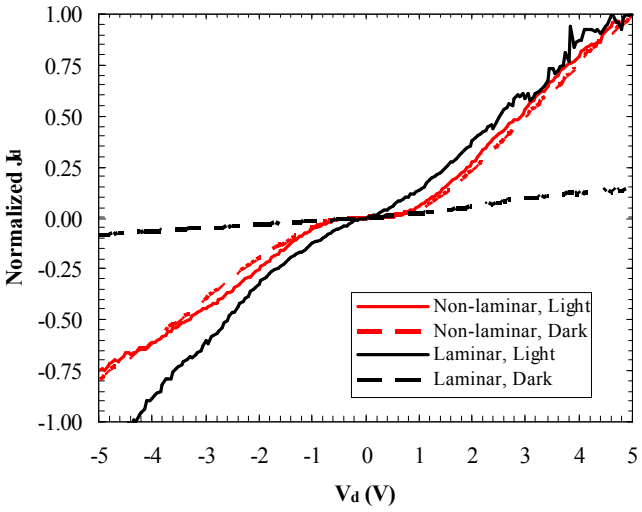

Fig. 11. Normalized current versus voltage for diodes in light and in dark and in both directions. Only laminar diodes show photo-enhanced conductivity.

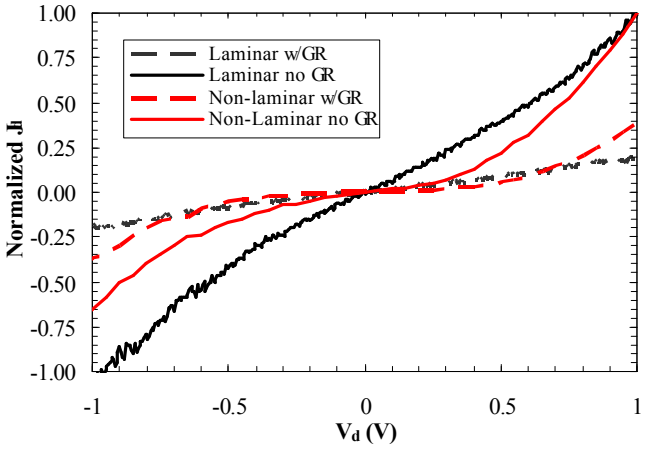

Fig. 10. Normalized current versus voltage for diodes with and without guard rings on laminar and non-laminar diodes.

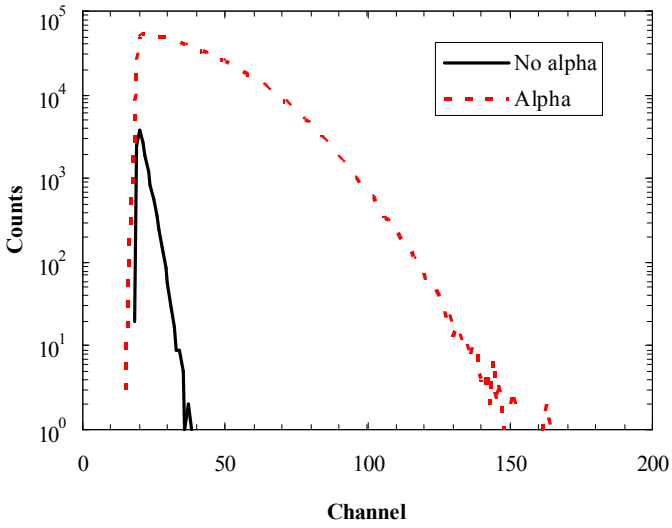

Fig. 12. Resulting spectrum from laminar planar GaTe detector using 5.8 MeV ^{243,244}Cm alpha source at 20 V/cm.

of the crystal. While the guard ring structure help to reduce the leakage component due to surface recombination, there is a significant amount of bulk leakage. An alpha spectrum has been shown, demonstrating that this material system has promise for semiconductor radiation detectors. Further effort is required to improve material quality and detector size to achieve high efficiency with the acceptable resolution levels for gamma detection applications.

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