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CIRCUIT DESIGN TO STABILIZE THE REFLECTOMETER LOCAL OSCILLATOR SIGNALS

C. C. Kung, G. J. Kramer, E. Johnson, W. Solomon, R. Nazikian, *Princeton Plasma Physics Laboratory, PO Box 451, Princeton, NJ 08543-0451*

Abstract—**Reflectometry, which uses the microwave radar technique to probe the magnetically confined fusion plasmas, is a very powerful tool to observe the density fluctuations in the fusion plasmas. Typically, two or more microwave beams of different frequencies are used to study the plasma density fluctuations. The frequency separation between these two beams of the PPPL designed reflectometer system upgrade on the DIII-D tokamak can be varied over 18 GHz. Due to the performance of the associated electronics, the local oscillator (LO) power level at the LO port of the I/Q demodulator suffers more than 12 dB of power fluctuations when the frequency separation is varied. Thus, the I/Q demodulator performance is impaired. In order to correct this problem, a power leveling circuit is introduced in the PPPL upgrade. According to the test results, the LO power fluctuation was regulated to be within 1 dB for greater than 16 dB of input power variation over the full dynamic bandwidth of the receiver.**

I. INTRODUCTION

Reflectometry is a very powerful tool to observe the density fluctuations in the magnetically confined fusion plasmas[1-3]. Because the regions of interest in the fusion plasmas are sensitive to the polarization of the probing frequencies, O-mode (polarization parallel to the magnetic field) and X-mode (polarization normal to the magnetic field) reflectometry are developed to probe different regions in these plasmas. A correlation reflectometer system radiates at least two different frequencies close to each other to probe slightly different plasma density layers. In terms of cross correlation of these different frequencies, information regarding the plasma density fluctuations can be extracted. Usually, a correlation reflectometer system has a fixed frequency at f_o and a tunable frequency with finite bandwidth centered at f_o so that correlations can be obtained between different locations in the plasma. Due to the electronic components limitation, an intermediate frequency (IF) has to be introduced in the reflectometer system design. This IF frequency has two functions. One is to serve as the LO frequency to drive the I/Q demodulators and the other is to serve as the carrier for the downconverted receive signals. Because the receive signals of the fixed frequency and the tunable frequency have to be simultaneously detected to obtain spatial correlations, the corresponding LO frequency for the tunable frequency I/Q demodulator has to be synchronized with this frequency change. However, the tunable frequency power may vary when the frequency is varied. Therefore, its associated demodulator might suffer LO power fluctuations. This condition is unfavorable for a proper operation of the I/Q demodulator.

A correlation reflectometer system designed by the University of California, Los Angles (UCLA) is currently used for the DIII-D experiment in General Atomics (GA)[4]. This reflectometer system consists of two BWO's operating between 50 GHz and 75 GHz as the probe sources for the DIII-D plasma (Fig. 1). The frequency difference between these two BWO's is used as the system IF frequency and LO signals to drive both I/Q demodulators. By using cross frequency mixing at the receiver front end, the plasma density fluctuation information can be extracted. Nevertheless, the LO power level in this scheme varies strongly across the frequency band due to the microwave power fluctuations of the BWO tubes. The microwave power fluctuation for the BWO tube can be more than 10 dB across its operating frequency range. Also, the associated mixer (NVV-11BB, Spacek Labs, Inc.) for generating the LO signals by mixing two BWO's signals is not uniform in conversion loss across the operating frequencies. Because the I/Q demodulator performance is directly related to the LO drive level, such a large LO power fluctuation (>10 dB) will definitely detrimentally impair the I/Q demodulator performance.

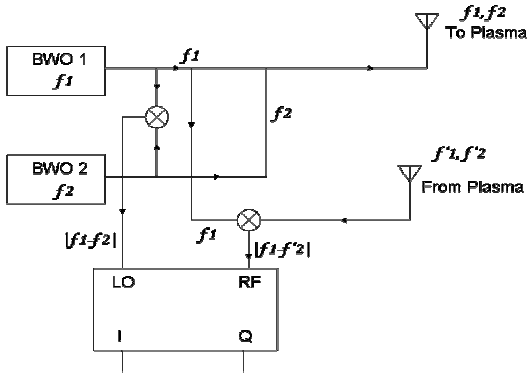

Fig. 1. Simplified UCLA Reflectometer circuit diagram. Another set of mixer and I/Q demodulator is used for extracting $|f'1-f2|$ signals.

All the mixer components rely on the nonlinear effect in the pn junction. Two well-defined parameters, the 1-dB compression point (P1dB) and the 3rd order intercept point (IP3) [5], are directly related to this nonlinear effect and are used to define the mixer performance. Typically, the power level difference between these two points is 10-15 dB. In order to fully utilize the nonlinear effect and optimize the performance, the LO drive level for the I/Q demodulator/mixer is usually at the mid-point of these two power levels. That is about 6-7 dB above the P1dB. If the LO power is higher than the required drive level, the spurious emissions levels will be much higher at the I/Q demodulator/mixer outputs. On the other hand, when the LO power is lower than the required level, the I/Q demodulator/mixer conversion loss will become much higher.

Moreover, some of the RF amplifiers have at least ±1 dB gain variation across their frequency band. Also, the I/Q demodulators/mixers have the conversion loss variations on the order of ±1 dB with a fixed power LO drive. Hence, the

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associated electronics performance will further deteriorate the I/Q demodulator performance and corrupt the desired I/Q signals. In order to correct this problem, a power leveling circuit was introduced to the UCLA reflectometer system. The components of this circuitry consists of a digital controlled attenuator and an RF detector in conjunction with a feedback loop (Fig. 2). The block diagram of the feedback loop with the analog-to-digital converter (ADC) is shown in Fig. 3.

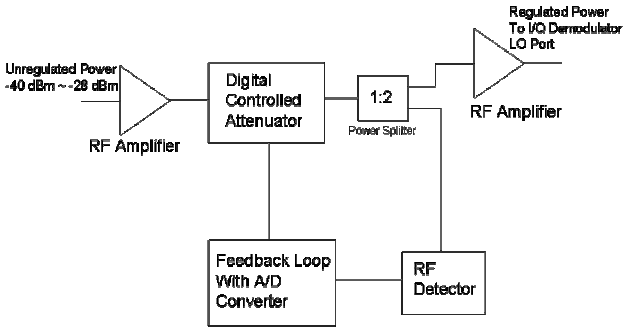

Fig. 2. A block diagram of the LO power leveling circuit.

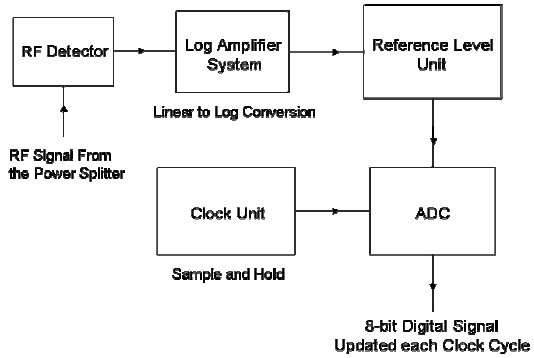

Fig. 3. A block diagram shows the key functional units of the feedback loop.

II. LO Power Leveling Circuit Design

A. RF Detection Circuitry

The block diagram of the feedback circuit to regulate the LO power is shown in Fig. 2. The LO power branching out from the UCLA system is between –28 dBm and –40 dBm (Fig. 2). The required LO power level to optimally drive the I/Q demodulator (Miteq, IR0118LC1Q) is between +10 dBm and +13 dBm. Thus, the available power level is too low and has too much power variation. A chain of RF amplifiers in the range of 1 GHz to 18 GHz is used to increase the power level to the range of +4 dBm and +16 dBm at the input of the digital controlled attenuator (Chelton, Al-5-03042, input P1dB at +18 dBm). This is the power range that will not overdrive the digital controlled attenuator to generate unwanted spurious emissions. In order to complete the gain control loop, a 2:1 power splitter is used to sample the power at the output of the digital controlled attenuator. A Midisco MDC 1101-S RF detector is connected to this power splitter to convert the RF power level to a dc signal.

B. Log Amplifier System

Because the RF detector output voltage is linearly proportional to the RF power and the digital controlled attenuator response is logarithmically reactive, a linear to log conversion is required (Fig. 3).

A buffer and amplification stage is introduced in the first stage of the circuit to provide good matching to the RF detector output and to raise the dc signal level to an adequate range so that the log amplifier in the following stage can convert this signal to a log signal.

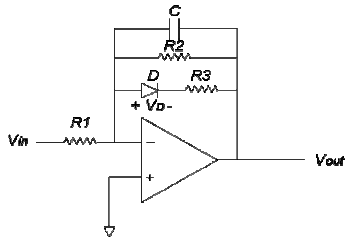

Fig. 4. Log amplifier circuit; *R2* and *C* are to limit the bandwidth and to prevent the high open loop gain when the diode is reversely biased; *R3* is used as a current limiter when the diode is forward biased.

The log amplifier itself is as simple as a diode across an op-amp (Fig. 4) [6]. *R2* and *C* in the circuit limit the bandwidth and prevent high open loop gain when the diode is reversely biased. *R3* limits the current when the diode is strongly forward biased. In order to achieve $V_{out} \approx -V_D \propto \log(V_{in}/R1) - k$, *R3* has to be much less than *R1* and *R2* so that the voltage drop across *R3* will be much smaller than V_D. Note that the offset constant k is directly related to the diode doping density. An 1N4148 diode, which has good log response between 0.1 mA and 50 mA, was chosen in this design. The corresponding voltage across the diode in this current range is between 0.4 V and 0.9 V. In order not to distort the log response at the output, a *10 Ω* resistor was selected for *R3*. Since the signal level is relatively low at the output of the log amplifier, an adjustable gain amplifier is used to boost the signal to the desired level to drive the reference level unit.

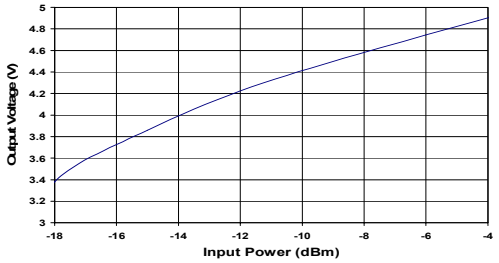

Fig. 5. The log amplifier system output voltage versus the power level at the RF detector input varying between -18 dBm and -4 dBm.

There is a 22-dB path loss when the digital controlled attenuator is at its mid-point in conjunction with the power splitter (Fig. 2). This suggests that the power level at the Midisco RF detector is in the range of –18 dBm to –6 dBm. The voltage response at the output of this log amplifier system, which is shown in Fig. 5, indeed varies logarithmically between 3.4 V and 4.9 V within this prescribed input power range.

This output voltages is then fed to the invert(–) input of an LM311 comparator, which serves as the first part of the reference level unit.

C. Reference Level Unit and ADC Functionality

The reference level unit (Fig. 6) consists of an LM311 comparator and an integrator. An LT1037 op-amp with a capacitor across its invert input and output serves as an integrator. The invert input(−) of this LM311 comparator is connected directly to the log amplifier system output.

The non-invert(+) input of this LM311 comparator is connected with an adjustable set voltage by using a variable resistor *R4*. This set voltage determines the desired power level at the output of the digital controlled attenuator. The set voltage range shall be between 3 V and 5 V (Fig. 5) to cover the power variations that are applied to the RF detector. The output of this comparator is sent to the integrator input through an adjustable resistor *R5*.

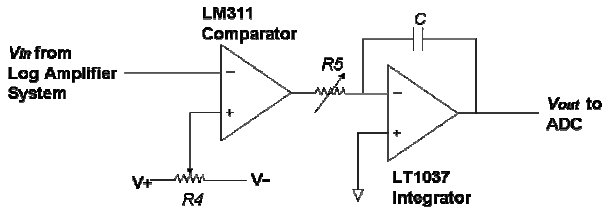

Fig. 6. An LM311 comparator and an LT1037 integrator form the reference level unit.

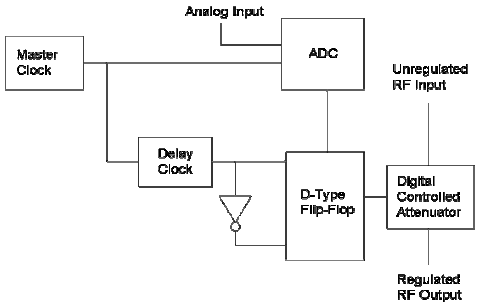

Fig. 7. The block diagram indicates the clock distribution to each circuit component. The delay clock provides D-type Flip-Flop data transfer clock and enable clock through an inverter.

When the RF detector senses a stronger LO signal, the voltage input to the comparator will be above the set voltage point and the capacitor in the integrator will be charged to provide a positive-swing voltage to the ADC (TLC0820AI analog to digital converter) (Fig. 7). Hence, a larger binary code will appear at the D-type Flip-Flop output at the end of this clock cycle. The attenuation level of the digital attenuator (Figs. 6 and 7) will then be increased to reduce the output power. Vice versa, if this power level becomes too low at the RF detector and the voltage input to the comparator is below the set voltage point, the capacitor in the integrator will be discharged to provide a negative-swing voltage to the ADC. A smaller binary code will appear at the D-type Flip-Flop output at the end of the clock cycle. The attenuation level at the digital attenuator will be decreased and the output power will become higher. If the LO power is almost constant, the comparator output will be a series of square pulses and the integrator output will be a series of triangular pulses. The repetition rate of these two waveforms will be equal to the clock frequency and the attenuation variation will be within 0.5 dB. It is shown in Fig. 6 that the set voltage point (desired power level) is controlled by variable resistor *R4* and the charging/discharging time constant is determined by variable resistor *R5*. The comparator and integrator output waveforms with constant input power are shown in Fig. 8. Notice that the faster the LO signal fluctuation is, the shorter the integration time constant (smaller *R5*) has to be. However, if the set voltage point is out of the range and/or charging/discharging time constant is too short, the whole gain controlled feedback loop will become unstable due to overcompensating the LO power fluctuation. Therefore, *R4* and *R5* have to be carefully adjusted to avoid such instability. Because the attenuator might misinterpret the loop condition when upper 3 bits are toggling to request attenuation and lower 5 bits are all presenting zero, upper 5 bits of the ADC are selected to drive the digital controlled attenuator to avoid this error scenario. In this case, the gain controlled feedback loop will also be insensitive to low level voltage perturbations in the integrator and will not over-react to power fluctuations of less than 0.5 dB.

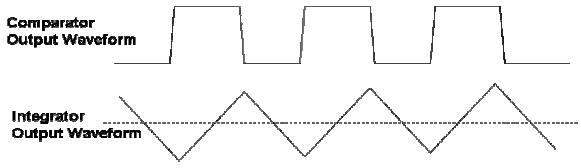

Fig. 8. The corresponding waveforms at the output of the comparator and the integrator in the reference level unit.

D. Digital Clock Circuit

In order to sample the RF signal strength and generate a 5-bit signal to control the digital controlled attenuator, a master clock and two derived clocks are required to coordinate this task (Fig. 7).

Since the master clock controls only the RF signal sampling and is unrelated to other data collection clocks, the clock jitter and frequency accuracy are not extremely important. Hence, we used an NE555 precision timer operating in its astable mode as the master clock [7]. Because the GA/UCLA reflectometer operates up to 1 kHz sweeping rate for the tunable frequency channel during plasma experiments, the LO power leveling rate should be at least 10 times faster than this sweeping rate. Thus, the repetition rate for the master clock was set to 160 kHz due to the limitation of the NE555 precision timer.

Usually a higher leveling rate provides better LO power leveling performance. However, higher leveling rate requires shorter capacitor charging/discharging time in the integrator. If *R5* in the integrator (Fig. 6) is large, the charging/discharging time will be long and the feedback loop will not be able to follow the power variation to reach the

stable LO power level. Therefore the integrator charging/discharging time is a trade-off between the leveling rate and the loop stabilization timing.

As shown in Fig. 7, this clock signal is fed directly to the ADC. Because the ADC needs at least 2.5 μS to convert the analog input voltage level into an 8-bit digital signal, a delay clock signal is needed to latch the output of the D-type Flip-Flop (SN74ABT377A) with previous data during this conversion. This delay clock circuit is accomplished with a second NE555 precision timer operating in its monostable mode [7]. The delay time for this clock was set to 3 μS which is 0.5 μS longer than the ADC conversion time. The 8-bit signal is then transferred and stored in the D-type Flip-Flop during this clock interval. An enable clock, which is derived from this delay clock by using an inverter, will enable the D-type Flip-Flop on its rising edge to pass and latch the 8-bit digital signal to the digital controlled attenuator. The clock distribution scheme is shown in Fig. 7. The clock and data conversion diagrams are shown in Fig. 9.

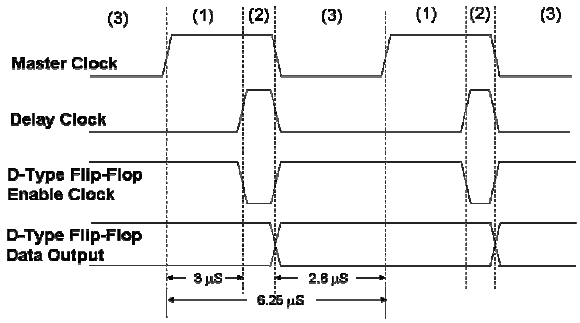

Fig. 9. (1)ADC is converting the analog signal to digital data (~3 μS); (2)Converted data is transferred and stored in the D-type Flip-Flop; (3)Converted data appears at the D-type Flip-Flop output to replace the old data and is latched during the next data conversion and transfer time.

III. Test Conditions and Results

A. Test Conditions

The gain controlled feedback loop was initially adjusted to provide –4 dBm at the digital controlled attenuator output when the input power at the RF detector was set at –13 dBm. This –4 dBm power level was then further amplified and split to the required LO power levels for two I/Q demodulators in the reflectometer system.

A 5-GHz signal source with a manual variable attenuator was used to test the prototype circuitry. This pseudo variable signal source was connected to LO power leveling circuit RF input port and an Agilent 8593E spectrum analyzer was connected to the circuit RF output port to monitor the power fluctuations (Fig. 2).

B. Test Results

According to the test results, a regulated output power level with less than 1-dB variation was obtained with this gain controlled feedback loop when the input power was varied from −43 dBm to −25 dBm. With this 18-dB range of power regulation, this circuit is well capable of leveling the power fluctuations between –40 dBm and –28 dBm in the UCLA reflectometer system.

At present, the PPPL designed IF electronics with this feedback circuit is integrated with the UCLA reflectometer system. By setting the Agilent 8593E spectrum analyzer at max-hold mode, the same results of less than 1-dB variation were observed for the LO power level when one of the BWO's was set at a fixed frequency and the other was dynamically tuned with a ramp generator.

IV. Summary

An LO power leveling circuitry was designed and successfully built for leveling the power variation between −40 dBm and −28 dBm in the frequency range up to 18 GHz. The key components of the leveling circuitry include a digitally controlled attenuator, an RF detector, and a feedback loop consisting of a clock unit, a reference level unit, and an ADC. Test results have shown that this feedback circuit is capable of leveling the LO power fluctuations to be within 1 dB in the frequency range up to 18 GHz when the associated input power is varied more than 16 dB. This LO power leveling circuitry was successfully installed and used during plasma operations in DIII-D.

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