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A monolithic time stretcher for precision time recording

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ABSTRACT: Identifying light mesons which contain only up/down quarks (pions) from those containing a strange quark (kaons) over the typical meter length scales of a particle physics detector requires instrumentation capable of measuring flight times with a resolution on the order of 20ps. In the last few years a large number of inexpensive, multi-channel Time-to-Digital Converter (TDC) chips have become available. These devices typically have timing resolution performance in the hundreds of ps regime. A technique is presented that is a monolithic version of "time stretcher" solution adopted for the Belle Time-Of-Flight system to address this gap between resolution need and intrinsic multi-hit TDC performance.

KEYWORDS: Analogue electronic circuits; VLSI circuits; Front-end electronics for detector readout.

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Contents

1. Background

Particle identification in the Belle experiment is based upon a composite system of subdetectors, as illustrated in figure 1. This hybrid system consists of ionization loss measurements (dE/dx) in the Central Drift Chamber (CDC), Cherenkov light emission measurement in the barrel and endcap Aerogel Chernkov Counters (ACC), and flight time measurement in the Time Of Flight (TOF) system. As indicated in the lower section of this figure, the three systems work together to cover the momentum range of interest.

Of these recording systems, the TOF system makes the most severe demands on time resolution. Indeed, given the 2ns spacing between RF buckets (and possible collisions), it is not known at recording time to which collision a given particle interaction in the TOF system corresponds.

Precision time recording in a very high rate environment requires an encoding scheme capable of continuous recording, with a minimum of deadtime per logged event. At the time of the construction of the Belle experiment [1] at the KEK B-factory [2], a decision was made to unify the entire detector readout (except for the silicon vertex detector) on the LeCroy 1877 Multi-hit TDC Module. This Fastbus module is based upon the MTD132A ASIC [3], which has a 0.5ns resolution encoding, comparable to a number of similar devices [4 – 6]. Given the limited manpower for DAQ system development and maintenance, this proved to be a wise choice. The intrinsic time resolution was quite adequate for recording the timing information from the CDC, as well as the amplitude information (through use of a charge-to-time converter) for the CDC and ACC.

The challenge then was to be able to record PMT hits with 20ps resolution, using a multi-hit TDC having 500ps least count, and for collisions potentially separated by only 2ns. This latter

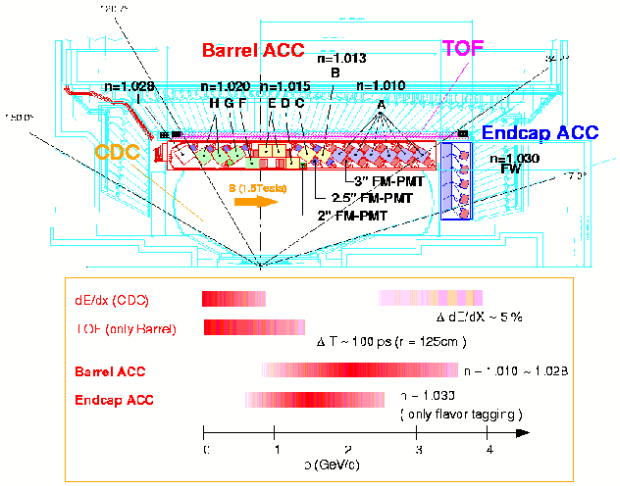

Figure 1. Depiction of the composite detector configuration used by Belle for particle identification.

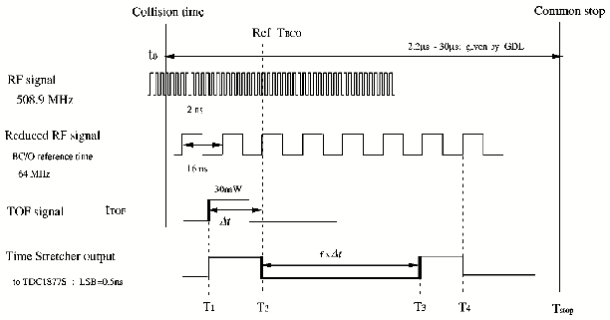

Figure 2. Timing diagram illustrating the operating principle of the Time Stretcher circuit, as explained in the text.

constraint meant that traditional techniques using a common start or stop could not be applied, since the bunch collision of interest was not known at the time at which the hits need to be recorded. Moreover, in order to avoid incurring additional error due to comparing a separate fiducial time, it is desirable to directly reference all time measurements to the accelerator RF clock. The solution adopted was a so-called Time Stretcher circuit, developed by one of the authors in conjunction with the LeCroy Corporation [8]. This work built upon valuable lessons learned in developing a similar recording system for the Particle Identification Detector system of the CPLEAR experiment [9]. The principle of operation is seen in figure 2. Hits are time-dilated with respect to the accelerator clock and recorded at coarser resolution, but in direct proportion to the stretch factor employed. Statistically, by also logging the raw hits, this stretch factor can be determined from the data.

As seen in figure 2, four timing edges are recorded for each hit signal. The leading edge corresponds to the actual output time of the discriminator. This rising edge is paired with a falling edge, corresponding to the 2nd accelerator reference clock (RF clock divided by 16) occuring after the initial hit timing. The interval of interest is then bounded to be between about 16-32 ns. With

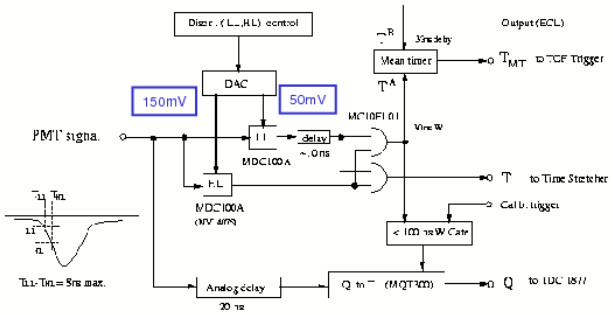

Figure 3. Time Of Flight Front-End Electronics readout flow. Precision timing is performed with a coarse, multi-hit TDC (LeCroy 1877) by means of a time-stetcher circuit.

a TDC least count of 0.5ns, a factor of twenty time expansion is needed – the stretch factor. In the figure the third edge corresponds to the time-expanded version of the interval between the rising and falling edges. A benefit of this technique is that it provides self-calibration. By recording a large number of events, the stretch factor can be extracted from the data itself since the raw and expanded signals are recorded. A 4th edge is provided, two clock rising edges after the 3rd edge, to provide a return to known state before next pulse. An obvious drawback in this scheme is that the deadtime for each hit will be something like 320 - 640ns, as will be discussed later.

In more detail, the signal chain of the current Belle TOF electronics [7], is sketched in figure 3.

High and low level discriminators are used, with the high-level used to reject background photon hits in the TOF and a low-level threshold used to provide the best possible leading edge timing. The charge of triggered events is also recorded with a charge to time (Q-to-T) ASIC, which is recorded with the same common TDC module. Charge recording is needed to correct for amplitude dependent timing effects in the discriminator itself.

2. Super B factory

The TOF readout system has worked well for almost a decade. Increased luminosity (already 60% over design) has lead to much higher single channel rates than had been specified in the design. From the beginning, the maximum design specification was 70kHz of single particle interaction rate for each channel. At this rate the expected inefficiency would be a few percent, comparable to the geometric inefficiency (due to cracks between scintillators).

Already the world's highest luminosity collider, the KEKB accelerator [2] can now produce in excess of one million B meson pairs per day. Upgrade plans call for increasing this luminosity by a factor of 30-50, providing huge data samples of 3rd generation quark and lepton decays. Precise interrogation of Standard Model predictions will be possible, if a clean operating environment can be maintained. Extrapolation of current occupancies to this higher luminosity mandates an upgrade of the readout electronics. The current system already suffers from significant loss of efficiency with higher background rates, as may be seen in figure 4.

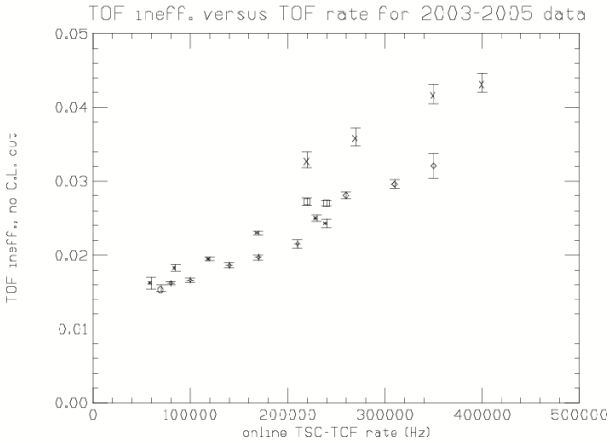

Figure 4. Composite TOF inefficiency for the last 3 years of running at Belle. Inefficiency grows with higher TOF singles rates, which have increased with increased luminosity, well beyond the 70kHz design specification.

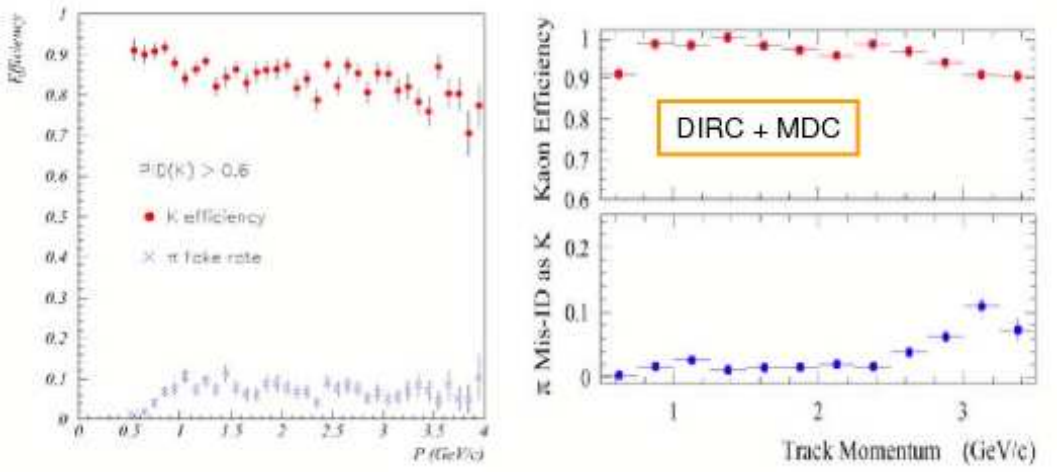

Figure 5. A direct comparison of PID technologies for the B-factory detectors. On the left, the performance of the Belle hybrid TOF/ACC system; on the right, a similar plot for the BaBar DIRC system. In both cases at lower momentum the K/π separation is enhanced through the use of drift-chamber dE/dx information. As may be seen, the overall fake rate is lower and efficiency higher for the DIRC.

3. Particle identification improvement

In considering an upgrade to the TOF readout electronics, it is worthwhile to consider the needs of an upgraded PID system for Belle. A comparative study of the Belle system, as depicted in figure 1, with that of BaBar [10] PID system is informative. It is clear in figure 5 the Direct Internally Reflected Cherenkov (DIRC) detector of BaBar has a higher efficiency and lower fake rate than the hybrid TOF/ACC scheme used by Belle.

Indeed, it was realized in the construction stage of Belle that such a DIRC-type detector would

have merits, and prototypes were explored [11]. While these results were very promising, the schedule risks led the collaboration to stick with technologies in which significant time and effort had already been invested.

Thinking about an upgrade, it is reasonable to revisit the choice of technology. In the intervening decade, significant progress has been made in the development of Ring Imaging CHerenkov (RICH) detectors [12, 13], as well as detectors based upon the arrival time of the Cherenkov photons, such at the Correlated Cherenkov Timing (CCT) [14] and Time Of Propagation (TOP) [15] counters.

Because of the great cost encumbered in the procurement and construction of the CsI crystal calorimeter, it is planned not to upgrade the barrel section. As a consequence, the volume available for the TOF/ACC replacement detector is rather limited. Therefore a RICH type detector has not been pursued. The most promising technologies to date are those illustrated in figure 6. The TOP concept uses timing in place of one of the projected spatial dimensions to reconstruct the Cherenkov emission ring. A focusing DIRC is principally using geometry to reconstruct the Cherenkov ring segments. However, in this case precision timing is still very useful for two important reasons. First it allows for the possibility of using timing to correct for chromatic dispersion in the emission angle of the Cherenkov photon. And second, fine timing allows time of flight to be measured using the quartz radiator bar.

Therefore, in both of the viable detector options considered, a large number of fine timing resolution recording channels are required. In the case of a finely segmented focusing DIRC [16] option, the number of readout channels could be comparable to that of the current silicon vertex detector. Clearly if such a detector is to be viable, significant integration of the readout electronics will be essential.

Not shown is a proposal for a multi-segmented TOF detector consisting of short scintillator bars. While this option remains viable (and the electronics presented would work well with such a system), the PID performance degradation of such a system is probably unacceptable. Of the choices listed, the most attractive in terms of performance is a focusing DIRC detector, if the issues of the photodetector and readout can be addressed.

Either as an upgrade of only the readout electronics or as a prototype for a higher channel count PID detector, it is worth considering improvements to the existing readout.

4. The monolithic time stretcher

The Time Stretcher technique has worked very well and Belle has been able to maintain approximately 100ps resolution performance with the TOF system. A slow degradation with time is consistent with loss of light output. Detailed Monte-Carlo simulation [17] has been able to reproduce much of the performance of the TOF system and the degradation is consistent with light loss due to crazing of the scintillator surface. A larger concern is the significant degradation of TOF system performance due to high hit rates. While the multi-hit TDC is capable of keeping up with high rates (though the limited number of recorded edges (16) also leads to inefficiency), by its very nature, the Time Stretcher output can not be significantly reduced. Recently, the clock speed was doubled, to help reduce this effect. Nevertheless, at ever higher hit rates, the deadtime leads to ever increasing inefficiency.

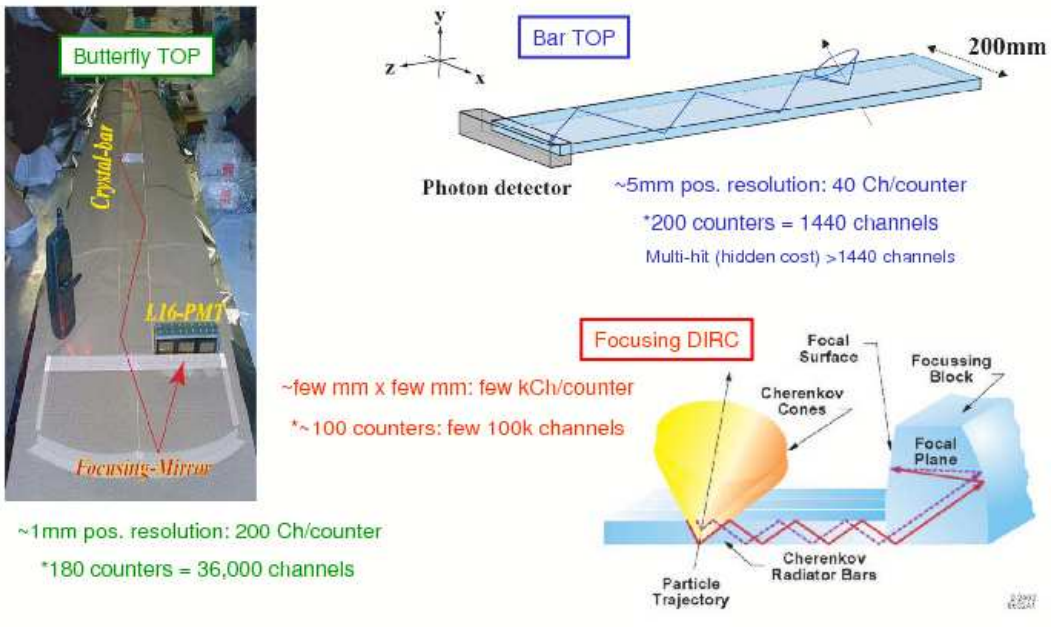

Figure 6. Concept figures of 3 of the Cherenkov ring imaging detectors that have been considered for the Belle detector upgrade. While simplest, the "Bar TOP" (Time-Of-Propagation) detector has been ruled out due to inadequate performance. Of the remaining two, the number of instrumented readout channels will depend upon the photodetector chosen, though will likely require many tens of thousands of readout channels, dictating a monolithic approach.

A logical solution to this problem is to introduce a device which has buffering. Also, while taking the effort to reduce the deadtime, it makes sense to consider a much more compact form-factor. This was done with the thought toward moving to a larger number of readout channels in a future Belle PID upgrade [18], as mentioned earlier. One proposed solution is the Monolithic Time Stretcher (MTS) chip, a prototype of which is shown in figure 7.

The fundamental logic of the device is identical to that currently in use with two major changes:

1. High density
2. Multi-hit

High density is achieved by replacing discrete Emitter-Coupled Logic components on daughter cards with a full custom integrated circuit. This higher integration permits having multiple time stretcher channels for each input. By toggling to a secondary output channel, the deadtime can be significantly reduced. Once a hit is processed in one output channel, the next is armed to process a subsequent hit.

In figure 7 the 8 channel repeating structure of each time stretcher circuit is clearly seen in the die photograph. The basics of the time-stretcher circuit are visible in figure 8. A one-shot circuit at the upper left leads to an immediate output signal, as well as starts charging current $I_{\rm hi}$. Pipelining of the hit signal continues for two clock cycles after which current $I_{\rm hi}$ is switched off and discharge

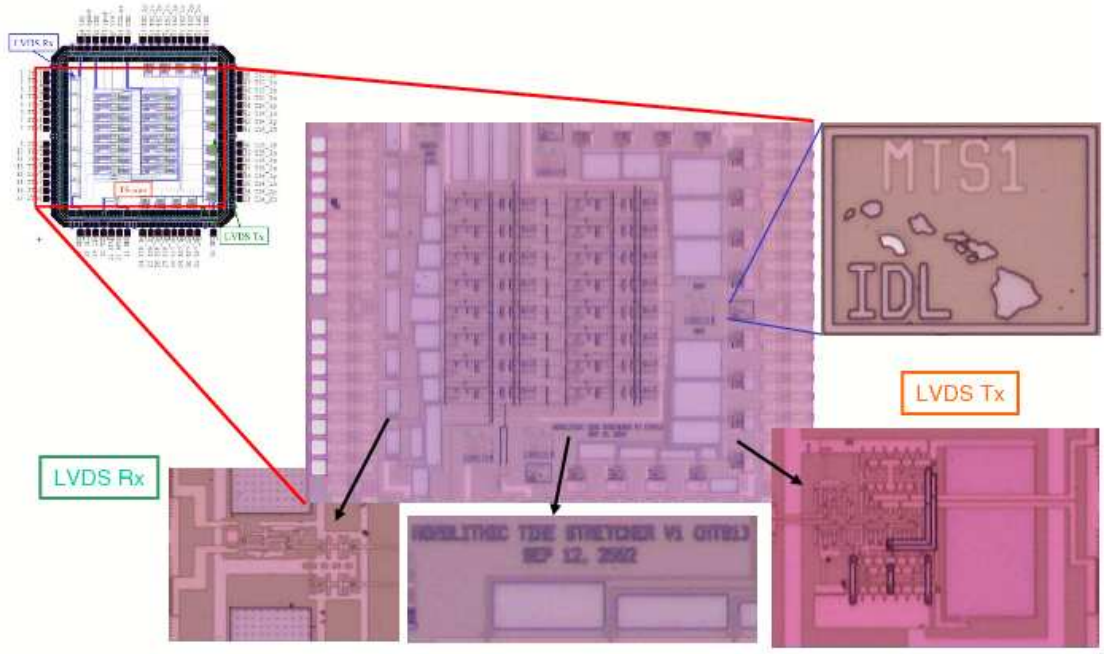

Figure 7. Floorplan drawing and die photographs of the Monolithic Time Strecther version 1 (MTS1) ASIC, an 8 channel device. All inputs and outputs are LVDS to reduce cross-talk.

current $I_{\rm lo}$ is switched on. A comparator monitors the voltage induced on the storage capacitor due to charging and discharging, providing an output signal to indicate the stretched time when the voltage is discharged.

The stretch factor is given by the ratio of the two currents: $SF = I_{\rm hi}/I_{\rm lo}$. Each input channel of the MTS1 has two time stretcher circuits, the second corresponding to the secondary output when the primary channel is active. Each output is recorded by a separate TDC channel. With this configuration at 10% deadtime for a single channel of time stretcher can be reduced to 1%. As the the incremental cost of additional TDC channels is rather low, it is possible consider additional buffering depths, which would reduce the deadtime by the dT^N, where N is the buffer depth, though that was not explored beyond a depth of two in this device.

Reduction of cross-talk and Electro-Magnetic Interference is enhanced by the use of Low Voltage Differential Signalling (LVDS) [20]. MTS1 is fabricated in the Taiwan Semiconductor Manufacturing Corporation 0.35μm CMOS process.

4.1 Form factor reduction

When considering a photodetector with a large number of channels, the form factor of this device is very attractive, as shown for comparison in figure 9, a substantial reduction in size has been achieved. On the left is a 16-channel Fastbus-sized Time Stretcher card used currently in the Belle experiment. Inset is a test board with one of the MTS1 packaged devices for comparison, where a dime has been placed on the board for scale.

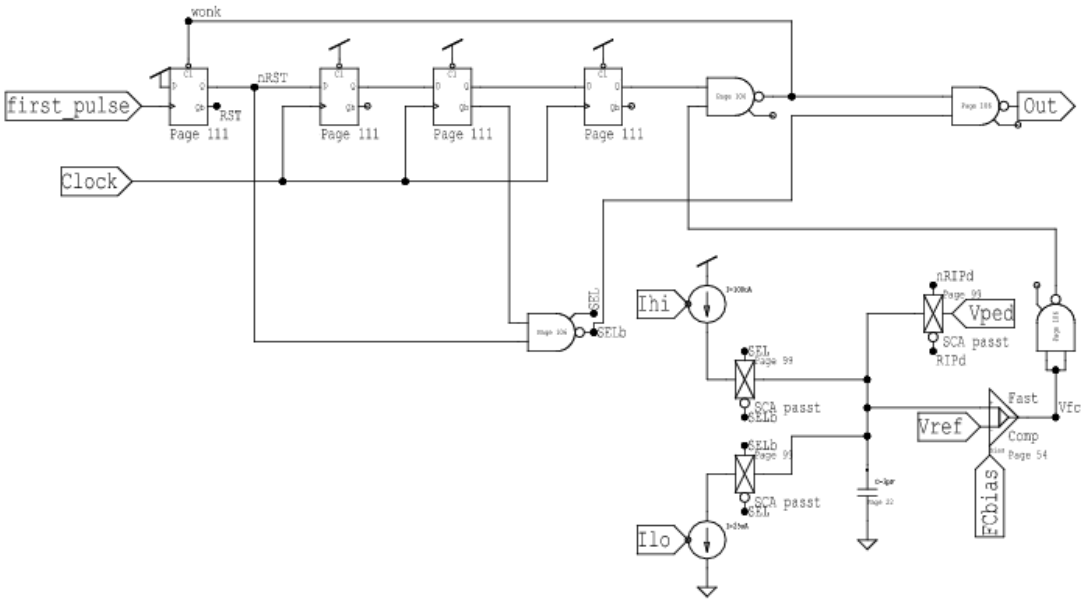

Figure 8. Schematic of the basic clocked time stretcher circuit.

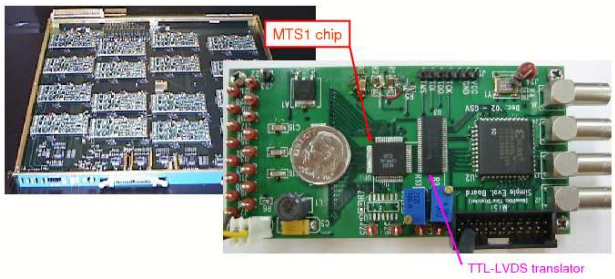

Figure 9. A form-factor comparison between the current Fastbus-sized, 16-channel Time Stretcher and the MTS1 chip on a test board. The test board occupies almost the same space as a single daughtercard channel on the TS motherboard, and has the same number of channels of time-stretching as the whole module.

With this level of integration it becomes feasible to consider integration of the time stretcher and TDC electronics on detector, as is being done for detector subsystems in the LHC experiments.

4.2 Test results

In order to test the performance of the MTS1, a multi-hit TDC should be used. As a demonstration of the power of this time stretching technique, an Field Programmable Gate Array (FPGA) can be used as this TDC [21], where the results from a simple Gray-code counter implementation of the hit time recording may be seen in figure 10. The RMS of the distribution is about 840ps for the Xilinx Spartan-3 device used. This resolution could be improved by use of a faster FPGA, though is sufficient to obtain the test results shown below.

Indeed, it is worth noting that this combined Time-Stetcher + FPGA technique is very powerful

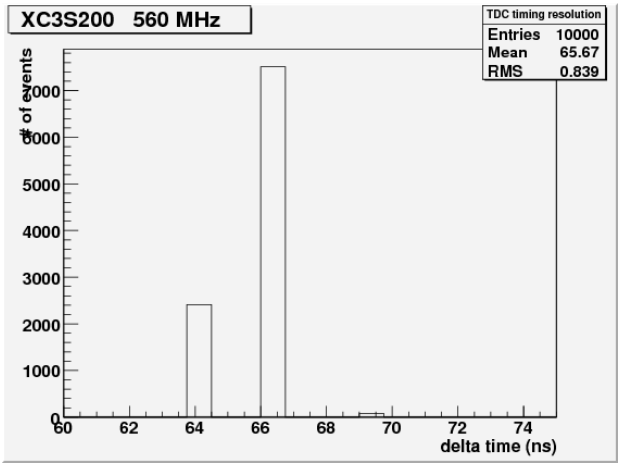

Figure 10. Timing resolution obtained for the FPGA-based TDC used in the MTS1 evaluatiton.

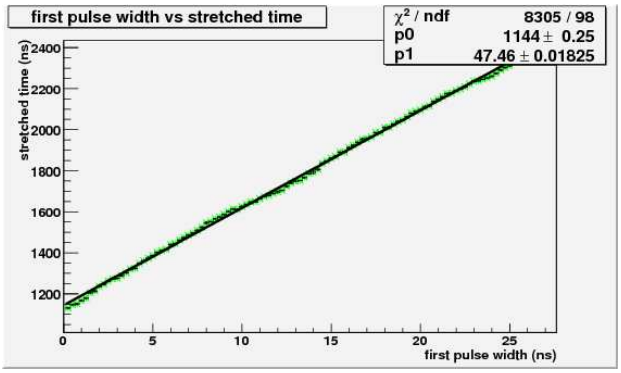

Figure 11. Scan of stretched times versus input reference time, within a single stretch clock cycle. In this case a stretch factor of about 47.5 was used.

for two important reasons:

1. low-cost, high-density TDC implementation
2. deep and flexible hit buffering and trigger matching logic

A test sweep of the MTS1 input is shown in figure 11, where it should be noted that due to the encoding scheme it is only meaningful to scan within a time expansion clock cycle period. A scan of expansion ratios was performed and the best results were obtained for stretch factors of 40-50.

As can be seen, there is some non-linearity in the expanded time. This is more clearly seen when a plot of the residual distribution is made by subtracting off the linear fit, as shown in figure 12. A periodic structure is seen, roughly consistent with the expansion clock period, if the negative timing dips are correlated to transition edges.

4.2.1 Timing resolution

As with the HPTDC device [19] developed at CERN for the ALICE detector, a fine calibration is

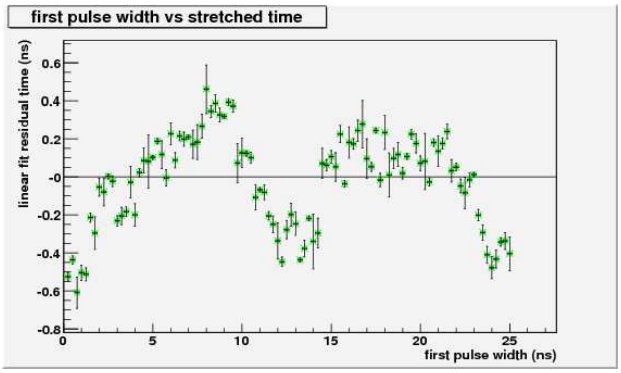

Figure 12. Residual distribution after a linear fit and application of the time stretch factor. An effect of expansion clock is clearly seen.

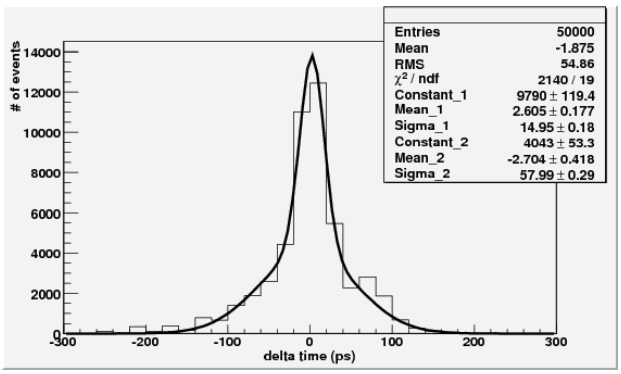

Figure 13. Timing resolution of the MTS1 + FPGA TDC when a non-linearity correction is applied. Non-gaussian tails are due to regions with larger jitter due to coupling of the reference clock into the ramping circuitry.

needed to obtain a precision comparable to the current Belle system. Applying such a calibration, determined in a separate data set, significantly improved linearity and residuals are obtained. The subsequent results are histogrammed in figure 13.

As can be seen, the timing resolution fits well to a double Gaussian, with a narrow sigma less than 20ps, which is comparable to (and actually slightly better than) the existing Belle system. This result is consistent with the expectation from the FPGA TDC used, where

$$\sigma_{\mathrm{TS}} = \frac{840\mathrm{ps}}{\mathrm{StretchFactor}} \simeq \frac{840\mathrm{ps}}{47.5} \approx 17\mathrm{ps} \tag{4.1}$$

and the measured sigma is about 15ps. It is possible that a finer resolution FPGA TDC would allow for an even more precise timing determination.

In practice the systematic effects of the upstream discriminator and its amplitude dependent threshold crossing (and comparator overdrive) dependence make any further improvements difficult. Nevertheless it is an interesting question for future exploration. This timing resolution is comparable to that obtained with the HPTDC after careful non-linearity calibration.

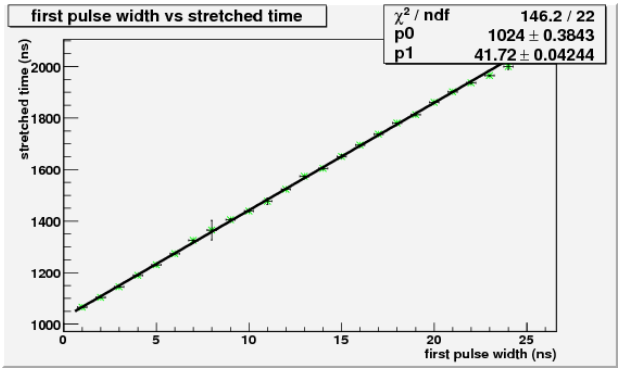

Figure 14. Cross-check measurement of the secondary MTS1 output channel, where the results are seen to be comparable to the primary channel, apart from a systematically smaller stretch factor as described in the text.

The broader Gaussian distribution and significant non-gaussian tails are correlated with expansion clock feedthrough to the ramping circuit. This could be improved in a future version with better layout isolation. The 0.35μm process used only had 3 metal routing layers available and migration to a finer feature size process would allow for dedicated shields and better power routing.

4.2.2 Multi-hit buffering

In order to reduce deadtime a second time-stretcher circuit, with a separate output, is provided for each input channel. This second circuit becomes armed when the primary stretcher circuit is running. Use of such a scheme can significantly reduce data loss due to arrival of subsequent hit during operation of the first stretcher circuit. The factor may be expressed as

$$F_{\text{dead}} = F_{\text{single}}^{N} \tag{4.2}$$

where N is the number of buffer stages. For N=2, the case prototyped here, a large existing deadtime of 20% could be reduced to 4%. Moreover, this technique can be extended to an even larger number of buffer channels, a realistic possibility when using a low cost FPGA-based TDC. In the case of 4 outputs, a 20% single time stretcher deadtime would become a completely negligible 1.6×10^{-3}.

Apart from the arming circuitry, the second time stretcher channel is identical to the primary. Testing was performed with double-pulse events and the result for the second channel is seen in figure 14.

Note that these secondary channels have a time-stretch factor that is systematically smaller. As the same reference currents are mirrored in all channels, it is believed that this is due to ramp window reduction due to latency in the arming logic.

4.2.3 Cross-talk

An important check of performance of the MTS1 is the impact of time stretcher operation on one channel while another is operating. This has been performed in figure 15, where the timing of the first channel is fixed and the timing relation of the signal in channel 2 is varied.

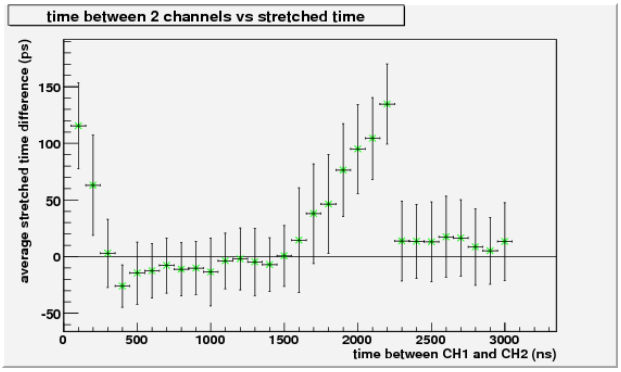

Figure 15. Timing shift due to adjacent channel crosstalk. As expected, impact is most sensitive during the initial current ramping and near stretched time threshold crossing.

The impact of operation of this second channel is clear during the ramping portion of the readout cycle, as well as the threshold crossing at the end of the ramping interval. While this effect can be calibrated out to some extent, just like effects of the clock feedthrough, this perturbation to the circuit would be better mitigated through better isolation in the IC layout.

5. Future prospects

An improved layout paired with future, higher clock frequency FPGAs could open the possibility of very dense channel count, sub-10ps resolution TDC recording.

For many applications the HPTDC is perfectly suitable and gives comparable time resolution to the MTS1 + FPGA TDC. In both cases a non-linearity correction is required to obtain this resolution. However the time encoding itself is only part of the issue for obtaining excellent timing resolution from a detector output. Correction for time slew in the discriminator threshold crossing is critical. Moreover the addition of many channels of high-speed discriminator inside a detector is a noise and power concern. Compact, high-speed waveform recording [22] may be a promising next evolutionary step in the readout of precision timing detectors.

Acknowledgments

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References

[1] BELLE collaboration, K. Abashian et al., *The Belle detector*, *Nucl. Instrum. Meth.* **A 479** (2002) 117.

[2] S. Kurokawa and E. Kikutani, *Overview of the KEKB accelerators*, *Nucl. Instrum. Meth.* **A 499** (2003) 1, and other papers included in this volume.

[3] G. Blanar and R. Sumner, *New time digitizer applications in particle physics experiments*, Proc. of the First International Conference on Electronics for Future Colliders, Editors G. Blanar and R. Sumner, LeCroy Corporation, New York (1991);

Technical Data Sheet, MTD132A, from LeCroy Corporation, 700 Chestnut Ridge Road, Chestnut Ridge, NY 11977.
A short list, not meant to be comprehensive:

[4] Y. Arai, *Development of frontend electronics and TDC LSI for the ATLAS MDT*, *Nucl. Instum. Meth.* **A 453** (2003) 365.

[5] W. Earle, E. Hazen, B. Safford and G. Varner, *A deadtimeless multihit TDC for the new g-2 experiment*, Prepared for 4th International Conference on Electronics for Future Colliders, Chestnut Ridge, NY, 11-12 May 1994, pp 223-232.

[6] M. Passaseo, E. Petrolo and S. Veneziano, *Design of a multihit TDC integrated circuit for drift chamber readout*, Prepared for 5th International Conference on Electronics for Future Colliders, Chestnut Ridge, NY, 10-11 May 1995, pp 139-142.

[7] H. Kichimi et al., *The Belle TOF system*, *Nucl. Instrum. Meth.* **A 453** (2000) 315.

[8] G. Varner *et al.*, *A time expanding multihit TDC for the Belle TOF detector at the KEK B-factory*, Conference Proceedings, LeCroy Conference on Electronics for Particle Physics (1997).

[9] D.H. Orlov, W.E. Earle, A. Go, E.S. Hazen, J.P. Miller and G.S. Varner, *A fast TDC for the CPLEAR experiment at CERN*, *Nucl. Instrum. Meth.* **A 333** (1993) 513.

[10] J. Schwiening et al., *Performance of the BABAR-DIRC*, *Nucl. Instrum. Meth.* **A 553** (2005) 317.

[11] C. Lu, D. Marlow, C. Mindas, E. Prebys, W. Sands and R. Wixted, *Detection of internally reflected Cherenkov light, results from the Belle DIRC prototype*, *Nucl. Instrum. Meth.* **A 371** (1996) 82.

[12] R. Ekelof, L.K. Resvanis and J. Seguinot, *Experimental techniques of Cherenkov light imaging*, *Nucl. Instrum. Meth.* **A 502** (2003) v.

[13] M. Artuso, *The CLEO RICH detector*, *Nucl. Instrum. Meth.* **A 554** (2005) 147.

[14] H. Kichimi, *The Cherenkov correlated timing detector: beam test results from quartz and acrylic bars*, *Nucl. Instrum. Meth.* **A 371** (1996) 91.

[15] T. Iijima, *Status of the TOP Counter R & D*, 3rd Workshop on Higher Luminosity B Factory, Shonan Village 2002 Proceedings, p 11-17.

[16] J. Benitez, *Development of a focusing DIRC*, 2006 IEEE Nuclear Science Symposium and Medical Imaging Conference, SLAC-PUB-12236.

[17] J.W. Nam et al., *A detailed Monte Carlo simulation for the Belle TOF system*, *Nucl. Instrum. Meth.* **A 491** (2002) 54.

[18] G. Varner, *High precision, high rate timing and other R&D Updates*, 5th Workshop on Higher Luminosity B Factory, Shuzenji (2004).

[19] J. Christiansen et al., *A data driven high performance time to digital converter*, 6th Workshop on Electronics for LHC Experiments, Krakow, Conf. Proceedings p.169-173 (2000).

[20] Low-voltage differential signaling (LVDS) uses high-speed analog circuit techniques to provide multi-gigabit data transfers on copper interconnects. It is defined under the Electronic Industries Alliance (EIA)-644-1995 standard.

[21] G. Varner, *The modern FPGA as discriminator, TDC and ADC*, 2006 *JINST* **1** P07001.

[22] G.S. Varner and L.L. Ruckman *The buffered large analog bandwidth recorder and digitizer with ordered readout*, in preparation for submission to *Nucl. Instrum. Meth.* **A**.